LINEAR TECHNOLOGY

1992 Linear Databook Supplement

MICRO SALES, INC.
MSi
210 Regency Court
Waukesha, WI 53186
414-786-1403
FAX: 414-786-1813
TIM SHINNERS

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Linear Technology Corporation

Linear Databook Supplement
1992

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CONTINUING PRODUCT EXCELLENCE

The founding theme of Linear Technology Corporation was to create a company capable of leading and directing linear circuit technology and design concepts of the future, and thus become the market's linear specialist. The Company believes that the total IC business has become so diverse and so complex that a single company will have great difficulty assembling the engineering talent necessary to lead in all areas of device technology.

Today, the customer base benefits by accessing the best product available in each functional area of the IC market from those vendors who are at the leading edge of performance and technology as a result of their "focused" strategy approach. The customer now has the choice of acquiring the best linear, the best microprocessor, the best memory products, etc., by choosing the best vendor in each area. In order to achieve the goal of becoming the market's first choice in the linear area. LTC has assembled the leading design, test, product, assembly, quality and process engineering talent in the industry, operating in what we feel is the most modern linear integrated circuit facility in production today.

This 1992 Databook Supplement contains new products introduced since the production of LTC's 1990 Databook. The offering of LTC products has continued to expand such that there are now over 325 basic product die types in the Company's product portfolio. These die types are the basis for over 2500 different devices available to order from the Company.

This was accomplished by fulfilling our commitment to advancing the state of the art in high performance analog functions. To do this, LTC developed the latest in bipolar, LTCMOS, micropower, high voltage, high speed and complementary process technologies. These products are 100% fabricated in LTC's state of the art wafer fab facilities which include a new area doubling LTC's capacity. Many of our products are now recognized as industry standard products setting new levels in the high performance analog market for parametric performance as well as in functional and value added engineering in our customers' applications. Simultaneously, LTC has focused on providing these new products with uncompromised quality, reliability and service.

Linear Technology Corporation remains committed to servicing the requirements of the Military/Aerospace Marketplace. Our MIL-STD-883 and SMD (Standard Military Drawings) products are tested to the latest revision requirements of MIL-STD-883. The Company also services JAN approved devices for both B and S level requirements as well as "S" level source control drawings. Both commercial and military outgoing quality levels are sampled over temperature with full lot traceability back to the original wafer from which the device was derived. A new addition to LTC's Mil/Aerospace product line is a line of radiation hardened devices. These products have individual data sheets which have guaranteed parametric performance limits for several different radiation levels.

Our commitment to designing and developing the next generation of high performance analog technology remains unchanged. Our goals of offering the best in quality, reliability and service to our customers are renewed to achieve even higher levels of performance and to remain focused on providing the highest performance yet lowest overall "cost to use" linear products.

LTC's successes are indicators of an acceptance of Linear Technology in the marketplace over these last ten years, for which we extend our sincere thanks and appreciation to our customers. It also sets new goals and expectations for our company to maintain the technical and business focus to meet your future needs. We are prepared to meet these challenges and remain... exclusively committed to linear.

Footnote: *The original 1990 Databook has been reprinted unchanged in format or content. Since its creation some of the products in the 1990 Databook have had some changes made to the data sheets due to additional package types such as surface mount, extended temperature ranges and parametric changes. Where possible we have cross referenced from the 1992 Supplement to the 1990 Databook to indicate these changes.*

1992 Linear Databook Supplement

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NOTES

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SECTION 1—GENERAL INFORMATION

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GENERAL ORDERING INFORMATION

I. ORDER ENTRY

Orders for products contained herein should be directed to: LINEAR TECHNOLOGY CORPORATION, 1630 McCarthy Boulevard, Milpitas, California 95035. Phone: 408-432-1900.

II. ORDERING INFORMATION

Minimum order value is $2000.00 per order; minimum value per line item is $500.00.

Each item must be ordered using the complete part number exactly as listed on the data sheet.

F.O.B.: Milpitas, California.

III. RELIABILITY PROGRAMS

Linear Technology Corporation currently offers the following Reliability Programs:

A. JAN QPL devices.
B. DESC drawings.
C. MIL-STD-883, Level B, latest revision for all military temperature range devices.
D. "R-Flow" Burn-In Program for commercial temperature range devices. Consult Factory regarding burn-in program.
E. Radiation Hardened (RH) products.

IV. PART NUMBER EXPLANATION

XXX XXXX X X J/883B

- 883B: Screening to MIL-STD-883, Level B, latest revision
- J: Package Style (see Cross Reference on Page 14-3)
- X (second): Temperature Range
  - M for Military
  - I for Industrial
  - C for Commercial
  - X for 200°C Extended Range*
- X (first): Letter indicates electrical grade of part
- XXXX: Generic or Product Part Number
- XXX: Designator
  - LF, LM, OP, REF, and SG are second source devices
  - LT are improved or proprietary devices
  - LTC indicates proprietary CMOS devices
  - RH indicates LTC's radiation hardened devices

V. PACKAGE SUFFIX EXPLANATION

Letter Designator	Description
D8	8-Lead Side Brazed Hermetic DIP
D	14, 16, 18, 20, and 24-Lead Side Brazed Hermetic DIP
H	Multi-Lead Metal Can
J8	8-Lead Ceramic DIP
J	14, 16, 18, and 20-Lead Ceramic DIP
K	TO-3 Metal Can (Steel)
M	3-Lead DD package Molded
N8	8-Lead Molded DIP
N	14, 16, 18, 20, 24, and 28-Lead Molded DIP
P	3-Lead TO-3P Molded
Q	5-Lead DD package Molded
R	7-Lead DD package Molded
S8	8-Lead Small Outline (SO) package (Note 1)

Letter Designator	Description
S	14, 16, 18, 20, 24, and 28-Lead Small Outline (SO) package (Note 1, 2)
ST	SOT-223 Molded
T	3 and 5-Lead TO-220 Molded
W	10-Lead Flatpack (Cerpak)
Y	7-Lead TO-220 Molded
Z	3-Lead TO-92 Molded

Note 1: Pinout and electrical specifications may differ from standard commercial grade N8 package. See SO data sheet for specific information.

Note 2: These devices are delivered in either 150 MIL (SO) or 300 MIL (SO-L) wide packages depending on device die size. See specific SO data sheet for pin counts and package dimensions.

ALTERNATE SOURCE CROSS REFERENCE GUIDE

P/N	LTC DIRECT REPL	P/N	LTC DIRECT REPL	P/N	LTC DIRECT REPL	P/N	LTC DIRECT REPL
AD101A	LM101A	ADS7800	LTC1272**	LF355A	LF355A	LM185BX-2.5	LT1034BM-2.5*
AD232	LTC1081*	CMP01	LT1011**		LT1055AC*	LM185BY-1.2	LT1034M-1.2*
AD235	LT1130**	CMP02	LT1011**	LF356A	LF356A	LM185BY-2.5	LT1034M-2.5*
AD237	LT1138**	DG201A	LTC201		LT1056AC*	LM196	LT1038M**
AD238	LT1139**	DG202	LTC202		LT1022AC*	LM199	LM199
AD239	LT1137**	DS1232	LTC1232	LF357	LT1022*	LM199A	LM199A
AD241	LT1136**	DS3695	LTC485*	LF398	LF398	LM199A-20	LM199A-20
AD381	LT1022**	EL2020	LT1223*	LF398A	LF398A	LM234-3	LM234-3
AD510J	OP07E*	EL2028	LT1220**	LF400	LT1122DC	LM234-6	LM234-6
	LT1001C*	EL2029	LT1221**		LT1122CC	LM308A	LM308A
AD510K	LT1001AC*	EL2030	LT1223**	LF400A	LT1122BC		LT1008C*
AD510L	LT1001AC*	EL2038	LT1222**		LT1122AC	LM311	LM311
AD510S	OP07A*	EL2039	LT1222**	LH0002	LT1010M**		LT311A*
	LT1001AM*	EL2040	LT1222**	LH0044	LT1001M*		LT1011C*
AD517	OP07**	EL2041	LT1220**	LH0070	LH0070	LM317	LM317
	LT1001**	EL2120	LT1190*, LT1223**		LT1031M*		LT317A*
AD518	LM118**	EL2130	LT1223**	LH2108	LH2108	LM317HV	LM317HV
	LT118A**	EL2232	LT1229**	LH2108A	LH2108A		LT317AHV*
AD524	LT1101**	HA2500	LT1220**	LM10	LM10	LM317KC	LM317T
AD536	LT1088**	HA2502	LT1220**	LM10B	LM10B		LM317AT*
AD580	LT580	HA2505	LT1220**	LM10C	LM10C	LM318	LM318
AD581	LT581	HA2510	LT118A**	LM101A	LM101A		LT318A*
	LT1031**		LM118**	LM107	LM107	LM319	LM319
AD586	LT1027*	HA2512	LT118A**	LM108	LM108		LT319A*
AD589	LT1034**		LM118A**		LT1008M*	LM323	LM323
AD636	LT1088**	HA2515	LT318A**	LM108A	LM108A		LT323A*
AD637	LT1088**		LM318**		LT1008M*		LT1003C**
AD642	LT1057**	HA2520	LT1220**	LM111	LM111	LM329A	LM329A
AD647	LT1057**	HA2541	LT1220**		LT111A*	LM329B	LM329B
AD705	LT1097	HA2544	LT1224**		LT1011M*	LM329C	LM329C
AD707	LT1097	HA5004	LT1223**	LM112	LT1012M*	LM329D	LM329D
AD711	LT1056**	HA5130-2	OP07A	LM113	LT1004M-1.2*	LM333	LT1033C*
AD712	LT1057**		LT1001AM*	LM117	LM117	LM333A	LT1033C
AD713	LT1058**	HA5130-5	OP07E		LT117A*	LM334	LM334
AD736	LT1088**		LT1001C*	LM117HV	LM117HV	LM336-2.5	LM336
AD737	LT1088**	HA5135-2	OP07		LT117AHV*		LT1009C*
AD744	LT1122		LT1001M*	LM118	LM118	LM336-5	LT1029C*
AD790	LT1016**	HA5135-5	OP07C		LT118A*	LM336B-2.5	LM336B
AD821	LT1006**		LT1001C*	LM119	LM119		LT1009C*
AD822	LT1013**	HAOP07	OP07		LT119A*	LM337	LM337
AD824	LT1014**		LT1001M*	LM123	LM123		LT337A*
AD840	LT1222**	HAOP07A	OP07A		LT123A*		LT1033C*
AD841	LT1220**		LT1001AM*		LT1003M*	LM337HV	LM337HV
AD842	LT1221**	HAOP07C	OP07C	LM124	LT1014M*		LT337AHV*
AD844	LT1223**		LT1001C*	LM129A	LM129A	LM338	LM338
AD845	LT1122	HAOP07E	OP07E	LM129B	LM129B		LT338A*
AD846	LT1223**		LT1001C*	LM129C	LM129C	LM350	LM350
AD847	LT1224**, LT1190**	ICL232	LT1081	LM133	LT1033M*		LT350A*
AD848	LT1225**, LT1191**	ICL7650	LTC1050*	LM134	LM134	LM368-5.0	LT1019AC-5*
AD849	LT1226**, LT1192**		LTC1052**	LM134-3	LM134-3	LM368-10.0	LT1019C-10**
AD7572	LTC1272**	ICL7652	LTC7652	LM134-6	LM134-6	LM368Y-5.0	LT1019AC-5*
AD7820	LTC1099*		LTC1052*	LM136-2.5	LT136-2.5	LM368Y-10.0	LT1019C-10**
AD9617	LT1223**	ICL7660	LTC1044*		LT1009M*	LM385-1.2	LM385-1.2
AD9618	LT1223**		LTC1054**	LM136-5	LT1029M**		LT1004C-1.2*
AD9686	LT1016**	ICL8069C	LM385-1.2	LM136A	LM136A	LM385-2.5	LM385-2.5
ADC032	LTC1091		LT1004C-1.2*		LT1009M*		LT1004C-2.5*
ADC0820	LTC1099*	ICL8069M	LM185-1.2	LM137	LM137	LM385BX-1.2	LT1034BC-1.2*
ADG201A	LTC201A		LT1004M-1.2*		LT137A	LM385BX-2.5	LT1034BC-2.5*
ADG202	LTC202	LF155	LF155		LT1033M**	LM385BY-1.2	LT1034C-1.2*
ADG221	LTC221		LT1055M	LM137HV	LM137HV	LM385BY-2.5	LT1034C-2.5*
ADG222	LTC222		LT1055M*		LT137AHV*	LM396	LT1038C**
ADOP07	OP07	LF155A	LF155A	LM138	LM138	LM399	LM399
	LT1001M*		LT1055AM		LT138A*	LM399A	LM399A
ADOP07A	OP07A		LT1055AM*	LM148	LT1014M*	LM399A-20	LM399A-20
	LT1001AM*	LF156	LF156	LM150	LM150	LM399A-50	LM399A-50
ADOP07C	OP07C		LT1056M		LT150A*	LM1524	SG1524
	LT1001C*		LT1056M*	LM158	LT1013M*		LT1524*
ADOP07D	OP07D		LT1022M*	LM168BY-5.0	LT1019M-5**	LM2575	LT1076**
	LT1001C*	LF156A	LF156A	LM168BY-10.0	LT1019M-10**	LM2576	LT1074**
ADOP07E	OP07E		LT1056AM	LM185-1.2	LM185-1.2	LM2577	LT1071**
	LT1001C*		LT1056AM*		LT1004M-1.2*	LM2935	LT1005**
ADOP27	OP27		LT1022AM*	LM185-2.5	LM185-2.5	LM2940	LT1086**
	LT1007**	LF198	LF198		LT1004M-2.5*	LM3524	SG3524
		LF198A	LF198A	LM185BX-1.2	LT1034BM-1.2*		LT3524*

*__LTC Improved Replacement:__ 100% Pin-for-pin compatible with better electrical specifications.

**__Similar Device:__ Please consult the data sheet to determine the suitability of the replacement for specific applications.

ALTERNATE SOURCE CROSS REFERENCE GUIDE

P/N	LTC DIRECT REPL
LP2950-5	LT1117-5**
LP2951	LT1120**
µA96172	LTC486
µA96174	LTC487
µA96176	LTC485
MAX162	LTC1272**
MAX163	LTC1272**
MAX232	LT1081*
MAX235	LT1130**
MAX237	LT1138**
MAX238	LT1139**
MAX239	LT1137**
MAX241	LT1136**
MAX400	LT1001
MAX420	LTC1150*
MAX422	LTC1150**
MAX428	LT1229
MAX430	LTC1150
MAX432	LTC1150**
MAX480	LT1077*
MAX630	LT1173**
MAX631	LT1173-5**
MAX632	LT1173-12**
MAX633	LT1173**
MAX634	LT1173**
MAX635	LT1173-5**
MAX636	LT1173-12**
MAX637	LT1173**
MAX638	LT1173-5**
MAX641	LT1173-5**
MAX642	LT1173-12**
MAX643	LT1173**
MAX654	LT1073-5
MAX655	LT1173-5**
MAX656	LT1073-5**
MAX657	LT1073**
MAX658	LT1173-5**
MAX659	LT1173-5**
MAX660	LT1054
MAX680	LT1026**
MAX690	LTC690
MAX691	LTC691
MAX694	LTC694
MAX695	LTC695
MAX699	LTC699
MAX1232	LTC1232
MC78T05	LM323T LT323AT*
MC1400AU2	LT1019CN8-2.5**
MC1400AU5	LT1019CN8-5**
MC1400AU10	LT1019CN8-10**
MC1400U2	LT1019CN8-2.5*
MC1400U5	LT1019CN8-5*
MC1400U10	LT1019CN8-10*
MC1558	LT1013M*
MC145406	LT1039-16*
MC34166	LT1074
MF5	LTC1059*
MF10	LTC1060 LTC1060*
MX7572	LTC1272*
MX7820	LTC1099*
NE1037	LT1037
NE5534	OP37* LT1037*
NE5534A	OP37* LT1037*
OP04	LT1013*
OP05	OP05 LT1001M*
OP05A	OP05A LT1001AM* LT1001M*
OP05C	OP05C LT1001C*
OP05E	OP05E LT1001C*
OP07	OP07 LT1001M*
OP07/714C	OP07C LT1001C*
OP07/714D	OP07D LT1001C*
OP07/714E	OP07E LT1001C*
OP07A	OP07A LT1001AM*
OP07C	OP07C LT1001C*
OP07E	OP07E LT1001C*
OP10	LT1002M*
OP10A	LT1002AM*
OP10C	LT1002C*
OP10E	LT1002C
OP11	LT1014*
OP12A	LT1012M*
OP12B	LT1012M*
OP12C	LT1012M*
OP12E	LT1012C*
OP12F	LT1012C*
OP12G	LT1012C*
OP14	LT1013**
OP15A	OP15A LT1055AM*
OP15B	OP15B LT1055M
OP15C	OP15C LT1055M*
OP15E	OP15E LT1055AC*
OP15F	OP15F LT1055C*
OP15G	OP15G LT1055C*
OP16A	OP16A LT1056AM*
OP16B	OP16B LT1056M*
OP16C	OP16C LT1056M*
OP16E	OP16E LT1056AC*
OP16F	OP16F LT1056C*
OP16G	OP16G LT1056C*
OP27	OP27
OP27A	OP27A LT1007AM*
OP27B	OP27A LT1007M LT1007M*
OP27C	OP27C LT1007M LT1007M*
OP27E	OP27E LT1007AC*
OP27F	OP27F LT1007C*
OP27G	OP27G LT1007C*
OP37A	OP37A LT1037AM*
OP37B	OP37A LT1037M LT1037M*
OP37C	OP37C LT1037M*
OP37E	OP37E LT1037AC*
OP37F	OP37E LT1037C*
OP37G	OP37G LT1037C*
OP42A	LT1122DM LT1122CM
OP42E	LT1122BC LT1122AC
OP42F	LT1122DC LT1122CC
OP42G	LT1122DC LT1122CC
OP77A	LT1001AM**
OP77B	LT1001M**
OP77E	LT1001AC**
OP77F	LT1001C**
OP77G	LT1001C**
OP97A	LT1012AM
OP97E	LT1012AC*
OP97F	LT1012D* LT1097*
OP160	LT1223**
OP177B	LT1001AM/883
OP177F	LT1001AC
OP177G	LT1001C LT1097C
OP207A	LT1002M*
OP207B	LT1002M*
OP207E	LT1002C*
OP207F	LT1002C*
OP215A	OP215A LT1057AM*
OP215B	OP215A* LT1057AM*
OP215C	OP215C LT1057M*
OP215E	OP215E LT1057C*
OP215F	OP215E* LT1057C*
OP215G	OP215G LT1057C*
OP220	LT1078*
OP221	LT1013*
OP227A	OP227A
OP227B	OP227A
OP227C	OP227C
OP227E	OP227E
OP227F	OP227E
OP227G	OP227G
OP260	LT1229**
OP270A	OP270A LT1124AM*
OP270E	OP270E
OP270F	OP270E LT1124C*
OP270G	OP270G LT1124C*
OP290	LT1078**
OP400A	LT1014AM**
OP400E	LT1014AC**
OP400F	LT1014AC**
OP420	LT1079*
OP421	LT1014*
OP470A	OP470A LT1125AM*
OP470E	OP470E
OP470F	OP470E LT1125C*
OP470G	OP470G LT1125C*
OP490	LT1079**
PM108	LM108 LT1008M*
PM108A	LM108A LT1008M*
PM155	LF155 LT1055M*
PM155A	LF155A LT1055M*
PM156	LF156 LT1056M*
PM156A	LF156A LT1056M*
PM308A	LM308A LT1008C*
PM355A	LF355A LT1055C*
PM356A	LF356A LT1056C*
PM1008	LT1008
PM1012	LT1012
PM1558	LT1013M*
PM2108	LH2108
PM2108A	LH2108A
RC714CH	OP07C LT1001C*
RC714EH	OP07E LT1001C*
REF01	REF01 LT1019M-10* LT1021-10**
REF01A	REF01A LT1021-10**
REF01C	REF01C LT1019C-10* LT1021-10**
REF01E	REF01E LT1021-10**
REF01H	REF01H LT1019C-10* LT1021-10**
REF02	REF02 LT1019M-5* LT1021-5**
REF02A	REF02A LT1021-5**
REF02C	REF02C LT1019C-5* LT1021-5**
REF02D	LT1019C-5* LT1021-5**
REF02E	REF02E LT1021-5**
REF02H	REF02H LT1019C-5* LT1021-5**
REF03	LT1019-2.5
REF43B	LT1019AM-2.5
REF43F	LT1019AC-2.5
REF43G	LT1019C-2.5
RM714H	OP07 LT1001M*
RM1558	LT1013M*
SE5534	OP37* LT1037*
SE5534A	OP37* LT1037*
SG101A	LM101A
SG108	LM108 LT1008M*
SG108A	LM108A LT1008M*

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ALTERNATE SOURCE CROSS REFERENCE GUIDE

P/N	LTC DIRECT REPL
SG111	LM111 LT111A LT1011M*
SG117	LM117
SG117A	LT117A
SG123	LM123
SG123A	LT123A LT1003M**
SG124	LT1014M*
SG137	LT137
SG137A	LT137A LT1033M**
SG138	LM138
SG138A	LT138A
SG150	LM150
SG150A	LT150A
SG311	LM311 LT311A* LT1011C*
SG317	LM317
SG317A	LT317A
SG323	LM323
SG323A	LT323A LT1003C**
SG337	LM337
SG337A	LT337A LT1033C**
SG338	LM338
SG338A	LT338A
SG350	LM350
SG350A	LT350A
SG1524	SG1524 LT1524*
SG1525A	SG1525A LT1525A*
SG1526	LT1526
SG1527A	SG1527A LT1527A*
SG1558	LT1013M*
SG3524	SG3524 LT3524*
SG3525A	SG3525A LT3525A*
SG3526	LT3526
SG3527A	SG3527A SG3527A* LT3527A*
SN75172	LTC486*
SN75174	LTC487*
SN75176	LTC485*
SN75186	LT1134**
TL431AP	LT1431*
TSC04	LM385-1.2
TSC05	LM385-2.5
TSC170	LT3846**
TSC171	LT3847**
TSC232	LT1080** LT1081**
TSC911	LTC1050*
TSC913	LT1078** LTC1051*
TSC914	LT1079** LTC1053*
TSC918	LTC7652**
TSC962	LTC1046**
TSC7650	LTC1050
TSC7652	LTC7652 LTC1052
TSC7660	LTC1044*
TSC9491	LM385-1.2 LT1004C-1.2
TSC9495	REF02 LT1019M-5 LT1021-5**
TSC9496	REF01E LT1021-10**
UC117	LM117 LT117A*
UC137	LM137 LT137A* LT1033M**
UC150	LM150 LT150A*
UC317	LM317 LT317A*
UC337	LM337 LT337A* LT1033C**
UC350	LM350 LT350A*
UC1524	SG1524 LT1524*
UC1525A	SG1525A LT1525A*
UC1527A	SG1527A LT1527A*
UC1846	LT1846
UC1847	LT1847
UC2525A	SG3525A LT3525A*
UC3524	SG3524 LT3524*
UC3527A	SG3527A LT3527A*
UC3842	LT1242*
UC3843	LT1243*
UC3844	LT1244*
UC3845	LT1245*

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SECTION 2—AMPLIFIERS

SECTION 2—AMPLIFIERS

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Op Amps

Precision

Dual Supply

Low V_{OS}

Zero-Drift

- LTC1050 (S, 5µV)
- LTC1051 (D, 5µV)
- LTC1052 (S, 5µV)
- LTC1053 (Q, 5µV)
- LTC1150 (S, 5µV)
- LTC1047 (D, 10µV)
- LTC1049 (S, 10µV)

Bipolar

- LT1001 (S, 25µV)
- LT1007 (S, 25µV)
- LT1012 (S, 25µV)
- LT1028 (S, 40µV)
- LT1077 (S, 40µV)
- LT1006 (S, 50µV)
- LT1024 (D, 50µV)
- LT1097 (S, 50µV)
- LT1002 (D, 60µV)
- LT1078 (D, 70µV)
- LT1079 (Q, 70µV)
- LT1124 (D, 70µV)
- LT1125 (Q, 100µV)
- LT1008 (S, 120µV)

Low I_B

Zero-Drift

- LTC1150 (S, 30pA)
- LTC1050 (S, 30pA)
- LTC1052 (S, 30pA)
- LTC1051 (D, 50pA)
- LTC1053 (Q, 50pA)
- LTC1047 (D, 50pA)
- LTC1049 (S, 50pA)

Bipolar

- LT1022 (S, 50pA)
- LT1055 (S, 50pA)
- LT1056 (S, 50pA)
- LT1057 (D, 50pA)
- LT1058 (Q, 50pA)
- LT1122 (S, 75pA)
- LT1008 (S, 100pA)
- LT1012 (S, 100pA)
- LT1024 (D, 120pA)
- LT1097 (S, 250pA)

Low Noise

- LT1028 (S, 1.1nV/√Hz)
- LT1115 (S, 1.1nV/√Hz)
- LT1007 (S, 3.8nV/√Hz)
- LT1037 (S, 3.8nV/√Hz)
- LT1124 (D, 4.2nV/√Hz)
- LT1125 (Q, 4.2nV/√Hz)
- LT1126 (D, 4.2nV/√Hz)
- LT1127 (Q, 4.2nV/√Hz)

Large A_{VOL}

- LT1007 (S, 7M)
- LT1028 (S, 7M)
- LT1037 (S, 7M)
- LT1115 (S, 7M)
- LT1124 (D, 5M)
- LT1125 (Q, 5M)
- LT1126 (D, 5M)
- LT1127 (D, 5M)
- LTC1049 (S, 3M)
- LTC1050 (S, 3M)
- LT1013 (D, 1.5M)
- LT1014 (Q, 1.5M)
- LT1006 (S, 1M)
- LT1077 (S, 1M)
- LT1078 (D, 1M)
- LT1079 (Q, 1M)
- LTC1051 (D, 1M)
- LTC1052 (S, 1M)
- LTC1053 (Q, 1M)
- LT1097 (S, 700k)
- LT1012 (S, 300k)

Single Supply

Low V_{OS}, Low Power

- LT1006 (S, 50µV, 520µA)
- LT1013 (D, 150µV, 0.9mA)
- LT1014 (Q, 180µV, 1.8mA)

Low V_{OS}, Micropower

- LTC1047 (D, 10µV, 55µA)
- LT1077 (S, 40µV, 60µA)
- LT1078 (D, 70µV, 100µA)
- LT1178 (D, 70µV, 36µA)
- LT1079 (Q, 100µV, 200µA)
- LT1179 (Q, 100µV, 72µA)

Low Power

Single or Dual Supplies

- LT1178 (D, 36µA)
- LT1077 (S, 60µA))
- LT1179 (Q, 72µA)
- LT1078 (D, 100µA)
- LT1079 (Q, 200µA)
- LT1006 (S, 520µA)
- LT1013 (D, 1mA)
- LT1014 (Q, 2mA)

High Speed

Fast Slew Rate Fast Settling

- LT1227 (S, 1100V/µs)
- LT1223 (S, 1000V/µs)*
- LT1229 (D, 1000V/µs)*
- LT1230 (Q, 1000V/µs)*
- LT1190 (S, 450V/µs)
- LT1191 (S, 450V/µs)
- LT1192 (S, 450V/µs)
- LT1224 (S, 250V/µs)
- LT1225 (S, 250V/µs)
- LT1226 (S, 250V/µs)
- LT1220 (S, 180V/µs)
- LT1221 (S, 180V/µs)
- LT1222 (S, 180V/µs)
- LT1122 (S, 80V/µs)
- LT1022 (S, 23V/µs)
- LT1056 (S, 12V/µs)
- LT1055 (S,10V/µs)
- LT1057 (D, 10V/µs)
- LT1058 (Q, 10V/µs)

Wide Bandwidth

Video

- LT1227 (S, 140MHz)*
- LT1223 (S, 100MHz)*
- LT1229 (D, 100MHz)*
- LT1230 (Q, 100MHz)*
- LT1191 (S, 90MHz)
- LT1193 (S, 70MHz)
- LT1190 (S, 50MHz)
- LT1192 (S, 40MHz)
- LT1194 (S, 40MHz)
- LT1217, (S, 10MHz)

Non-Video

- LT1224 (S, 45MHz)
- LT1220 (S, 45MHz)
- LT1222 (S, 40MHz)
- LT1226 (S, 40MHz)
- LT1221 (S, 37MHz)
- LT1225 (S, 30MHz)
- LT1028 (S, 25MHz)
- LM118 (S, 15MHz)
- LT1122 (S, 14MHz)
- LT1037 (S, 9MHz)

Low Power

- LT1200 (S, 1mA, 10MHz)
- LT1217 (S, 1mA, 10MHz)*

* Current Feedback Amplifier

MILITARY PRECISION OP AMPS

PART NUMBER	ELECTRICAL CHARACTERISTICS V_{OS} MAX (µV)	TC V_{OS} (µV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/µs)	NOISE MAX 10Hz (nV√Hz)	PACKAGES AVAILABLE	IMPORTANT FEATURES
SINGLE								
LT1001AM	15	0.6	2.0	450	0.15	18	H, J8	Extremely Low Offset Voltage, Low Noise, Low Drift
LT1001M	60	1.0	3.8	400	0.15	18	H, J8	
LT1006AM	50	1.3	15	1000	0.25	24†	H, J8	Single Supply Operation, Fully Specified for +5V Supply
LT1006M	80	1.8	25	700	0.25	24†	H, J8	
LT1007AM	25	0.6	35	7000	1.7	4.5	H, J8	Extremely Low Noise, Low Drift
LT1007M	60	1.0	55	5000	1.7	4.5	H, J8	
LT1008M	120	1.5	0.1	200	0.1	30	H	Low Bias Current, Low Power
LT1010M	90mV	0.6mV/°C†	150µA	0.995	75	90†	H, K	High Speed Buffer, Drives ±10V into 75Ω
LT1012M	35	1.5	0.1	200	0.1	30	H	Low V_{OS}, Low Power
LT1022AM	250	5.0	0.05	150	23	50	H	Very High Speed JFET Input Op Amp with Very Good DC Specs
LT1022M	600	9.0	0.05	120	18	60	H	
LT1028AM	40	0.8	90	7000	11	1.7	H, J8	Lowest Noise, High Speed, Low Drift
LT1028M	80	1.0	180	5000	11	1.9	H, J8	
LT1037AM	25	0.6	35	7000	11	4.5	H, J8	Extremely Low Noise, High Speed
LT1037M	60	1.0	55	5000	11	4.5	H, J8	
LT1055AM	150	4	0.05	150	10	50	H	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055M	400	8	0.05	120	7.5	60	H	
LT1056AM	180	4	0.05	150	12	50	H	
LT1056M	450	8	0.05	120	9	60	H	
LT1077AM	40	0.4	9	250	0.12	40	H, J8	Micropower, Single Supply, Precision, Low Noise
LT1077M	60	0.4	11	200	0.12	29†	H, J8	
LTC1050AM	5	0.05	0.035	3162	4†	0.6µVp-p**	H, J8	Auto Zeroed Precision Op Amp, No External Capacitors Required
LTC1050M	5	0.05	0.050	1000	4†	0.6µVp-p**	H, J8	
LTC1052M	5	0.05	0.03	1000	3†	0.5µVp-p**	H, J, J8	Low Noise, Auto Zeroed Precision Op Amp
LTC1150M	5	±0.05	0.03	10000	3†	0.6µVp-p**	H, J8	Auto Zeroed Precision Op Amp That Operates on ±15V Supplies. No External Capacitors Required
LF155A	2000	5	0.05	75	5	25†*	H	JFET Inputs, Low I Bias, No Phase Reversal, Guaranteed TC V_{OS} on All Grades
LF155	3500	15	0.10	50	5	25†*	H	
LF156A	2000	5	0.05	75	10	15†*	H	
LF156	3500	15	0.10	50	9	15†*	H	
LM10	2000	2†	20	120		50†	H, J8	On-Chip Reference Operates with +1.2V Single Battery
LM101A	2000	15	75	25	0.3	28†	H, J8	Uncompensated General Purpose
LM107	2000	15	75	25	0.3	28†	H, J8	Compensated General Purpose
LM108A	500	5	2	40	0.1	30†	H	Low Bias Current, Low Supply Current
LM108	2000	15	3	25	0.1	30†	H	
LM118	4000		250	25	50	42†	H	High Speed, 15MHz
LT118A	1000		250	200	50	42†	H, J8	High Speed, 15MHz
OP-05A	150	0.9	2	300	0.1	18	H, J8	Low Noise, Low Offset Drift with Time
OP-05	500	2.0	3	200	0.1	18	H, J8	
OP-07A	25	0.6	2	300	0.1	18	H, J8	Low Initial Offset, Low Noise, Low Drift
OP-07	75	1.3	3	200	0.1	18	H, J8	
OP-15A	500	5	0.05	100	10	20†*	H	Precicion JFET Input, Low I Bias, No Phase Reversal
OP-15B	1000	10	0.1	75	7.5	20†*	H	
OP-15C	3000	15	0.2	50	5	20†*	H	

† Typical Spec

* 100Hz Noise

** DC to 1Hz Noise

NOTE: See page 4-3 for DESC Cross Reference Numbers

MILITARY PRECISION OP AMPS

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V_{OS} MAX (µV)	TC V_{OS} (µV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/µs)	NOISE MAX 10Hz (nV√Hz)	PACKAGES AVAILABLE	
SINGLE								
OP-16A	500	5	0.5	100	18	$20^{\dagger *}$	H	Precicion JFET Input, High Speed, No Phase Reversal
OP-16B	1000	10	0.1	75	12	$20^{\dagger *}$	H	
OP-16C	3000	15	0.2	50	9	$20^{\dagger *}$	H	
OP-27A	25	0.6	40	1000	1.7	5.5	H, J8	Very Low Noise, Unity Gain Stable
OP-27C	100	1.8	80	700	1.7	8.0	H, J8	
OP-37A	25	0.6	40	1000	11	5.5	H, J8	Very Low Noise, Stable for Gain ≥ 5
OP-37C	100	1.8	80	700	11	8.0	H, J8	
OP-97A	25	0.6	±0.1	300	0.1	30	H, J8	Low Noise, Low Bias Current
DUAL								
LT1002AM	60	0.9	3.0	400	0.15	20	J	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002M	100	1.3	4.5	350	0.15	20	J	
LT1013AM	150	2.0	20	1500	0.2	$24^{\dagger}$	H, J8	Precision Dual Op Amp in 8-Pin Package
LT1013M	300	2.5	30	1200	0.2	$24^{\dagger}$	H, J8	
LT1024AM	50	1.5	0.12	250	0.1	33	D	Low V_{OS}, Low Power, Matching Specs
LT1024M	100	2.0	0.20	180	0.1	33	D	
LT1057AM	450	7	0.05	150	10	$26^{\dagger}$	H, J8	Low Offset, JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1057M	800	12	0.075	100	8	$26^{\dagger}$	H, J8	
LT1078AM	70	2.0	0.25	250	$0.07^{\dagger}$	40	H, J8	Micropower, Precision, Single Supply, Low Noise Dual
LT1078M	120	2.5	0.35	200	$0.07^{\dagger}$	$29^{\dagger}$	H, J8	
LT1124AM	170	1	55	1000	2.3	5.5	J8	Dual Precision Op Amp, Low Noise, High Speed
LT1124M	250	1.5	70	700	2.0	5.5	J8	
LT1126A	170	1.0	55	1000	7.2	5.5	J8	
LT1126	250	1.5	70	700	7.0	5.5	J8	
LT1178AM	70	2.2	5	140	0.013	75	H, J8	17µA Max, Single Supply, Precision Dual
LT1178M	120	3.0	6	110	0.013	$50^{\dagger}$	J, N	
LTC1051M	5	0.05	0.05	1000	$4^{\dagger}$	0.4µVp-p**	J8	Dual, Precision Auto Zeroed Op Amp. No External Capacitors Required.
LF412AM	1000	10	0.1	100	10	$20^{\dagger *}$	H, J8	High Performance Dual JFET Input Op Amp
LH2108A	500	5.0	2	40	0.1	$30^{\dagger}$	D	Dual, Low Bias Current, Side Brazed Package
LH2108	2000	15.0	2	25	0.1	$30^{\dagger}$	D	
OP-215A	1000	10	0.1	150	10	$20^{\dagger *}$	H, J8	High Performance Dual JFET Input Op Amp
OP-215C	3000	20	0.2	50	8	$20^{\dagger *}$	H, J8	
OP-227A	80	1.0	40	3000	1.7	6	J	Dual Matched OP-27
OP-227C	180	1.8	80	2000	1.7	9	J	
OP-237A	80	1.0	40	3000	10	6	J	Dual Matched OP-37
OP-237C	180	1.8	80	2000	10	9	J	
OP-270A	175	1	60	400	1.7	$3.6^{\dagger}$	J8	Dual Precision Op Amp, Low Noise
QUAD								
LT1014AM	180	2.0	20	1500	0.2	$24^{\dagger}$	J	Precision Quad Op Amp in 14-Pin Package
LT1014M	300	2.5	30	1200	0.2	$24^{\dagger}$	J	
LT1058AM	600	10	0.05	150	10	$26^{\dagger}$	J	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1058M	1000	15	0.075	100	8	$29^{\dagger}$	J	
LT1079AM	120	2.0	0.25	250	$0.07^{\dagger}$	40	J	Micropower, Precision, Single Supply, Low Noise Quad
LT1079M	150	2.5	0.35	200	$0.07^{\dagger}$	$26^{\dagger}$	J	
LT1125AM	170	1	55	1000	2.3	5.5	J	Quad Precision Op Amp, Low Noise, High Speed
LT1125M	250	1.5	70	700	2.0	55	J	
LT1127A	190	1.0	55	1000	7.2	5.5	J	
LT1127	290	1.5	70	700	7.0	5.5	J	
LT1179AM	100	2.2	3	140	0.013	75	J	17µA Max, Single Supply, Precision Quad
LT1179M	150	3.0	6	110	0.013	$50^{\dagger}$	J	
LTC1053M	5	0.05	0.05	1000	$4^{\dagger}$	0.4µVp-p**	J	Quad Precision Auto Zeroed Op Amp, No External Capacitors Required.
OP-470A	600	2	50	400	1.4	6.5	J	Quad Precision Op Amp, Low Noise

† Typical Spec * 100Hz Noise ** DC to 1Hz Noise **NOTE:** See page 4-3 for DESC Cross Reference Numbers

OP AMP SELECTION GUIDE

COMMERCIAL PRECISION OP AMPS

	ELECTRICAL CHARACTERISTICS							
PART NUMBER	V_{OS} MAX (µV)	TC V_{OS} (µV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/µs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	IMPORTANT FEATURES
SINGLE								
LT1001AC	25	0.6	2.0	450	0.15	18	H, J8, N8	Extremely Low Offset Voltage, Low Noise, Low Drift
LT1001C	60	1.0	3.8	400	0.15	18	H, J8, N8, S8	
LT1006AC	50	1.3	15	1000	0.25	24†	H, J8	Single Supply Operation, Fully Specified for +5V Supply
LT1006C	80	1.8	25	700	0.25	24†	H, J8, N8	
LT1006S8	400	3.5	25	700	0.25	25	S8	
LT1007AC	25	0.6	35	7000	1.7	4.5	H, J8, N8	Extremely Low Noise, Low Drift
LT1007C	60	1.0	55	5000	1.7	4.5	H, J8, N8, S	
LT1008C	120	1.5	0.1	200	0.1	30	H, N8	Low Bias Current, Low Power
LT1010C	100mV	0.6mV/°C†	250µA	0.995	75	90†	H, K, T	High Speed Buffer, Drives ±10V into 75Ω
LT1012C	25	0.6	100	300	0.1	30	H, N8	Low V_{OS}, Low Power
LT1012CA	50	1.5	0.15	200	0.1	30	H, N8	
LT1012D	60	1.7	150	200	0.1	30	H, N8	
LT1012S8	120	1.8	0.28	200	0.1	30	S8	
LT1022AC	250	5.0	0.05	150	23	50	H	Very High Speed JFET Input Op Amp with Very Good DC Specs
LT1022CH	600	9.0	0.05	120	18	60	H	
LT1022CN8	1000	15.0	0.05	100	18	60	N8	
LT1028AC	40	0.8	90	7000	11	1.7	H, J8, N8	Lowest Noise, High Speed, Low Drift
LT1028C	80	1.0	180	5000	11	1.9	H, J8, N8, S	
LT1037AC	25	0.6	35	7000	11	4.5	H, J8, N8	Extremely Low Noise, High Speed
LT1037C	60	1.0	55	5000	11	4.5	H, J8, N8, S	
LT1055AC	150	4	0.05	150	10	50	H	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055C	400	8	0.05	120	7.5	60	H	
LT1055CN8	700	12	0.05	120	7.5	60	N8	
LT1055S8	1500	15	0.1	120	7.5	70	S8	
LT1056AC	180	4	0.05	150	12	50	H	
LT1056C	450	8	0.05	120	9	60	H	
LT1056CN8	800	12	0.05	120	9	60	N8	
LT1056S8	1500	15	0.1	120	9.0	70	S8	
LT1077AC	40	0.4	9	250	0.12	40	H, J8, N8	Micropower, Single Supply, Precision, Low Noise
LT1077C	60	0.4	11	200	0.12	29†	H, J8, N8	
LT1077S8	150	3.0	11	240	0.05	28†	S8	
LT1097C	50	1.0	±0.250	700	0.1	16†	N8	Low Cost, Low Power Precision
LT1097S8	60	1.4	±0.350	700	0.1	16†	S8	
LT1115C	280	0.5 (Typ)	±380	2000	10	1.8	N8, S	Lowest Noise, Ultra Low Distortion Audio Optimized Op Amp
LTC1049C	10	0.1	±0.050	3162	0.8†	1.0µVp-p**	J8, N8	Auto Zeroed Precision Op Amp, No External Capacitors Required
LTC1050AC	5	0.05	0.035	3162	4†	0.6µVp-p**	H, J8, N8, S8	
LTC1050C	5	0.05	0.050	1000	4†	0.6µVp-p**	H, J8, N8, S8	
LTC1052C	5	0.05	0.03	1000	3†	0.5µVp-p**	H, N8, N	Low Noise, Auto Zeroed Precision Op Amp
LTC7652C	5	0.05	0.03	1000	3†	0.5µVp-p**	H, N8	
LTC1150	5	0.05	0.03	10000	3†	0.6µVp-p**	H, J8, N8, S8	Auto Zeroed Precision Op Amp That Operates on Standard ±15V Supplies. No External Capacitors Required
LF355A	2000	5	0.05	75	5	25†*	H, N8	JFET Inputs, Low I Bias, No Phase Reversal
LF356A	2000	5	0.05	75	10	15†*	H, N8	
LM10B	2000	2†	20	120	—	50†	H, J8	On-Chip Reference Operates with +1.2V Single Battery
LM10BL	2000	2†	20	60	—	50†	H, J8	
LM10C	4000	5†	30	80	—	50†	H, J8, N8	
LM10CL	4000	5†	30	40	—	50†	H, J8, N8	

† Typical Spec * 100Hz Noise ** DC to 1Hz Noise

NOTE: See page 4-3 for DESC Cross Reference Numbers

COMMERCIAL PRECISION OP AMPS

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/$\sqrt{Hz}$)	PACKAGES AVAILABLE	
SINGLE								
LM308A	500	5	7	60	0.1	$30^{\dagger}$	H, N8	Low Bias, Supply Current
LT318A	1000		250	200	50	$42^{\dagger}$	H, J8, N8	High Speed, 15MHz
LM318	10000		500	25	50	$42^{\dagger}$	H, J8, N8, S8	High Speed, 15MHz
OP-05C	1300	4.5	7	120	0.1	20	H, J8, N8	Low Noise, Low Offset Drift With Time
OP-05E	500	2.0	4	200	0.1	18	H, J8, N8	
OP-07C	150	1.8	7	120	0.1	20	H, J8, N8, S8	Low Initial Offset, Low Noise, Low Drift
OP-07E	75	1.3	4	200	0.1	18	H, J8, N8	
OP-15E	500	5	0.05	100	10	$20^{\dagger *}$	H, N8	Precision JFET Input, Low I Bias, No Phase Reversal
OP-15F	1000	10	0.1	75	7.5	$20^{\dagger *}$	H, N8	
OP-15G	3000	15	0.2	50	5	$20^{\dagger *}$	H, N8	
OP-16E	500	5	0.05	100	18	$20^{\dagger *}$	H, N8	Precision JFET Input, High Speed, No Phase Reversal
OP-16F	1000	10	0.1	75	12	$20^{\dagger *}$	H, N8	
OP-16G	3000	15	0.2	50	9	$20^{\dagger *}$	H, N8	
OP-27E	25	0.6	40	1000	1.7	5.5	H, J8, N8	Very Low Noise, Unity Gain Stable
OP-27G	100	1.8	80	700	1.7	8.0	H, N8	
OP-37E	25	0.6	40	1000	11	5.5	H, J8, N8	Very Low Noise, Stable for Gains ≥ 5
OP-37G	100	1.8	80	700	11	8.0	H, N8	
OP-97E	25	0.6	±0.1	300	0.1	30	H, N8	Low Power, Low I_B, Precision
DUAL								
LT1002AC	60	0.9	3.0	400	0.15	20	J, N	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002C	100	1.3	4.5	350	0.15	20	J, N	
LT1013AC	150	2.0	20	1500	0.2	$24^{\dagger}$	H, J8	Precision Dual Op Amp in 8-Pin Package
LT1013C	300	2.5	30	1200	0.2	$24^{\dagger}$	H, J8, N8	
LT1013D	800	5.0	30	1200	0.2	$24^{\dagger}$	N8, S8	
LT1024AC	50	1.5	0.12	250	0.1	33	N	Low V_{OS}, Low Power, Matching Specs
LT1024C	100	2.0	0.20	180	0.1	33	N	
LT1057AC	450	7	0.05	150	10	$26^{\dagger}$	H, J8	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1057ACN8	450	10	0.05	150	10	$26^{\dagger}$	N8	
LT1057C	800	12	0.075	100	8	$26^{\dagger}$	H, J8	
LT1057CN8	800	16	0.075	100	8	$26^{\dagger}$	N8	
LT1057S	2000	$5^{\dagger}$	0.1	100	8	$26^{\dagger}$	S	
LT1057IS	2000	$5^{\dagger}$	0.1	100	8	$26^{\dagger}$	S	
LT1078AC	70	2.0	8	250	$0.07^{\dagger}$	40	H, J8, N8	Micropower, Precision, Single Supply, Low Noise Dual
LT1078C	120	2.5	10	200	$0.07^{\dagger}$	$29^{\dagger}$	H, J8, N8, S	
LT1124AC	70	1	55	2000	3	5.5	N	Dual Precision Op Amp, Low Noise, High Speed
LT1124C	100	1.5	70	1500	2.7	5.5	J, N, S	
LT1126AC	70	1.0	20	2.0	8	5.5	N8	
LT1126C	100	1.5	30	1.5	8	5.5	J8, N8, S8	
LT1178AC	70	2.2	5	140	0.013	75	H, J8, N8	17μA Max, Single Supply, Precision Dual
LT1178C	120	3.0	6	110	0.013	$50^{\dagger}$	H, J8, N8	
LTC1047C	10	0.01	0.02	1000	$0.2^{\dagger}$	0.8μVp-p**	N8, S	No External Capacitors Required Dual, Precision Auto Zeroed Op Amp.
LTC1051C	5	0.05	0.05	1000	$4^{\dagger}$	0.4μVp-p**	J8, N8, S	
LF412AC	1000	10	0.1	100	10	$20^{\dagger *}$	H, J8, N8	High Performance Dual JFET Input Op Amp
OP-215E	1000	10	0.1	150	10	$20^{\dagger *}$	H, J8, N8	
OP-215G	3000	20	0.2	50	8	$20^{\dagger *}$	H, J8, N8	
OP-227E	80	1.0	40	3000	1.7	6	J, N	Dual Matched OP-27
OP-227G	180	1.8	80	2000	1.7	9	J, N	
OP-237E	80	1.0	40	3000	10	6	J, N	Dual Matched OP-37
OP-237G	180	1.8	80	2000	10	9	J, N	
OP-270A	75	1	20	750	1.7	6.5	J	Dual Op Amp, Low Noise
OP-270C	250	3	60	350	1.7	$3.6^{\dagger}$	N, S	

† Typical Spec * 100Hz Noise ** DC to 1Hz Noise **NOTE:** See page 4-3 for DESC Cross Reference Numbers

COMMERCIAL PRECISION OP AMPS

	ELECTRICAL CHARACTERISTICS							
PART NUMBER	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/$\sqrt{\text{Hz}}$)	PACKAGES AVAILABLE	IMPORTANT FEATURES
QUAD								
LT1014AC	180	2.0	20	1500	0.2	$24^\dagger$	J	Precision Quad Op Amp in 14-Pin Package
LT1014C	300	2.5	30	1200	0.2	$24^\dagger$	J, N	
LT1014D	800	5.0	30	1200	0.2	$24^\dagger$	N, S	
LT1058AC	600	10	0.05	150	10	$26^\dagger$	J	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1058ACN	600	15	0.05	150	10	$26^\dagger$	N	
LT1058C	1000	15	0.075	100	8	$26^\dagger$	J	
LT1058CN	1000	22	0.075	100	8	$26^\dagger$	N	
LT1079AC	120	2.0	8	250	$0.07^\dagger$	40	J, N	Micropower, Precision, Single Supply, Low Noise Quad
LT1079C	150	2.5	10	200	$0.07^\dagger$	$29^\dagger$	J, N, S	
LT1125AC	90	1	20	2000	3	5.5	N	Precision Quad Op Amp, Low Noise, High Speed
LT1125C	140	1.5	30	1500	2.7	5.5	J, N, S	
LT1127AC	90	1.0	20	2.0	8	5.5	N	
LT1127C	140	1.5	30	1.5	8	5.5	N, J, S	
LT1179AC	100	2.2	5	140	0.013	75	J, N	17μA Max, Single Supply, Precision Quad
LT1179C	150	3.0	6	110	0.013	$50^\dagger$	J, N	
LTC1053C	5	0.05	0.05	1000	$4^\dagger$	0.4μVp-p**	J, N	Quad, Precision Auto Zeroed Op Amp. No External Capacitors Required.
OP-470A	400	2	25	500	1.4	6.5	J	Quad Op Amp, Low Noise
OP-470C	1000	$2^\dagger$	60	400	1.4	6.5	N, S	

†Typical Spec   * 100Hz Noise   ** DC to 1Hz Noise

NOTE: See page 4-3 for DESC Cross Reference Numbers

MILITARY HIGH SPEED OP AMPS

PART NUMBER	ELECTRICAL CHARACTERISTICS							IMPORTANT FEATURES
	MIN SLEW RATE (V/μs)	TYP SETTLING TIME TO 0.01% (μs)	TYPICAL GAIN BANDWIDTH PRODUCT (MHz)	MIN A_{VOL} (V/mV)	MAX V_{OS} (μV)	I_B MAX (nA)	PACKAGES AVAILABLE	
SINGLE								
LT1022AM	23	1.5	8.5	150	250	0.05	H	Very Good DC Specs
LT1022M	18	1.5	8.0	120	600	0.05	H	
LT1028AM	11	*	75	7000	40	90	H, J8	Lowest Voltage Noise, Good DC Specs
LT1028M	11	*	75	5000	80	180	H, J8	
LT1037AM	11	*	60	7000	25	35	H, J8	Low Voltage Noise, Good DC Specs
LT1037M	11	*	60	5000	60	55	H, J8	
LT1055AM	10	1.5	5.5	150	150	0.05	H	Lowest Offset JFET Input Op Amps
LT1055M	7.5	1.5	4.5	120	400	0.05	H	
LT1056AM	12	1.5	6.5	150	180	0.05	H	
LT1056M	9	1.5	5.5	120	450	0.05	H	
LT1122AM	60	0.340** 0.540***	14	180	600	0.075	J8	JFET Input. Faster and Better DC Specs Than OP-42. A and C Grades Have 100% Tested Settling Time
LT1122BM	60	0.350**	14	180	600	0.075	J8	
LT1122CM	50	0.350** 0.590***	13	150	900	0.1	J8	
LT1122DM	50	0.360**	13	150	900	0.1	J8	Inverting Applications Can Use External Compensation to Get 150V/μs Slew Rate
LT1190	325	$0.140^{\dagger}$	50	8	14000	2500	J8	Color Video Performance, High Speed, Wide Bandwidth, High Output Drive
LT1191	325	$0.110^{\dagger}$	90	6	5000	2500	J8	
LT1192	325	$0.090^{\dagger}$	350	16	2500	2500	J8	
LT1193	350	$0.180^{\dagger}$	160	—	12000	3500	J8	High Speed, High Output Drive, High CMRR, Color Video, Preset Gain and Adj Gain
LT1194	350	$0.200^{\dagger}$	350	—	6000	3500	J8	
LT1223	800	$0.075^{\dagger}$	100	—	3000	—	J8, N8, S8	High Speed Plus Good DC Performance
LT1228	300	$0.045^{\dagger}$	100	—	15000	—	J8	Electronic DC Gain Control
LM118	50	$1^{\dagger}$	15	25	4000	250	H	Inverting Applications Can Use External Compensation to Get 150V/μs Slew Rate
LT118A	50	$1^{\dagger}$	15	200	1000	250	H, J8	Fast Slew Rate
OP-15A	10	4.5	6	100	500	0.05	H	Precision JFET Input, No Phase Reversal
OP-15B	7.5	4.5	5.7	75	1000	0.1	H	
OP-15C	5	4.7	5.4	50	3000	0.2	H	
OP-16A	18	3.8	8	100	500	0.05	H	Precision JFET Input, No Phase Reversal
OP-16B	12	3.8	7.6	75	1000	0.1	H	
OP-16C	9	4.0	7.2	50	3000	0.2	H	
DUAL								
LT1057AM	10	1.4	3.5	150	450	0.05	H, J8	Low Offset Voltage, JFET Input
LT1057M	8	1.4	3	100	800	0.075	H, J8	
LT1229	300	$0.045^{\dagger}$	100	—	15000	—	J8	Fast Slew Rate, Current Feedback Architecture
LF412AM	10	2.3	5.7	100	1000	0.1	H, J8	JFET Input
OP-215A	10	2.3	5.7	150	1000	0.1	H, J8	JFET Input
OP-215C	8	2.4	5.5	50	3000	0.2	H, J8	
OP-237A	10	*	40	3000	80	40	J	Dual Matched OP-37
OP-237C	10	*	40	2000	180	80	J	
QUAD								
LT1058AM	10	1.4	3.5	150	600	0.05	J	Lowest Offset Voltage, JFET Input Quad
LT1058M	8	1.4	3	100	1000	0.075	J	
LT1230	300	$0.045^{\dagger}$	100	—	15000	—	J	Fast Slew Rate, Current Feedback Architecture

† To 0.1% *Not recommended for Fast Settling Applications. **10V Step, to 1mV at Sum Node. ***Maximum Value, 10V Step, to 1mV at Sum Node.

NOTE: See page 4-3 for DESC Cross Reference Numbers

COMMERCIAL HIGH SPEED OP AMPS

	ELECTRICAL CHARACTERISTICS							
PART NUMBER	MIN SLEW RATE (V/µs)	TYP SETTLING TIME TO 0.01 % (µs)	TYPICAL GAIN BANDWIDTH PRODUCT (MHz)	MIN A_{VOL} (V/mV)	MAX V_{OS} (µV)	I_B MAX (nA)	PACKAGES AVAILABLE	IMPORTANT FEATURES
SINGLE								
LT1022AC	23	1.5	8.5	150	250	0.05	H	JFET Input, Very Good Specs
LT1022CH	18	1.5	8.0	120	600	0.05	H	
LT1022CN8	18	1.5	8.0	100	1000	0.05	N8	
LT1028AC	11	*	75	7000	40	90	H, J8, N8	Lowest Voltage Noise, Good DC Specs
LT1028C	11	*	75	5000	80	180	H, J8, N8, S	
LT1037AC	11	*	60	7000	25	35	H, J8, N8	Low Voltage Noise, Good DC Specs
LT1037C	11	*	60	5000	60	55	H, J8, N8, S	
LT1055AC	10	1.5	5.5	150	150	0.05	H	Lowest Offset Voltage, JFET Input Op Amp
LT1055C	7.5	1.5	4.5	120	400	0.05	H	
LT1055CN8	7.5	1.5	4.5	120	700	0.05	H8	
LT1055S8	7.5	1.5	4.5	120	1500	0.1	S8	
LT1056AC	12	1.5	6.5	150	180	0.05	H	Lowest Offset Voltage, JFET Input Op Amp
LT1056C	9	1.5	5.5	120	450	0.05	H	
LT1056CN8	9	1.5	5.5	120	800	0.05	N8	
LT1056S8	9	1.5	5.5	120	1500	0.1	S8	
LT1115C	10	*	70	2000	280	380	N8, S8	Optimized for Audio Applications
LT1122AC	60	0.340** 0.540***	14	180	600	0.075	J8, N8	JFET Input. Faster and Better DC Specs Than OP-42. A and C Have Grades 100% Tested Settling Time
LT1122BC	60	0.350**	14	180	600	0.075	J8, N8	
LT1122CC	50	0.350** 0.590***	13	150	900	0.1	J8, N8, S8	
LT1122DC	50	0.360**	13	150	900	0.1	J8, N8, S8	
LT1190C	450††	0.1†	50	45††	2††	500††	N8, S8	±5V Supply Color Video Op Amps
LT1191C	450††	0.1†	90	44††	1††	500††	N8, S8	
LT1192C	450††	0.1†	400 ($A_V \geq 5$)	40††	0.2††	500††	N8, S8	
LT1193	450††	0.1†	70	—	2††	500††	N8, S8	Color Video Differential Amplifier
LT1194C	450††	0.1†	40	—	2††	500††	N8, S8	
LT1200C	30	0.430†	11.0	4	1000	1000	N8, S8	Low Supply Current Op Amp
LT1217C	100	280†	10.0	3.1	3000	500	N8, S8	Low Power Current Feedback Amplifier
LT1220C	200	0.09†	45	20	1000	300	N8	Ultra High Speed, Good DC Specs
LT1221C	200	0.09†	150 ($A_V \geq 4$)	50	1000	300	N8	
LT1222C	200	0.09†	500 ($A_V \geq 10$)	100	1000	300	N8	
LT1223C	800	0.075†	100	3.1	3000	3000	N8, S8	Current Feedback Amplifier
LT1224	250	0.090†	45	3.3	2000	8000	J8, N8, S8	High Speed, DC Precision, Can Drive Unlimited Capacitive Load While Remaining Stable
LT1225	250	0.070†	150	12.5	1000	8000	J8, N8, S8	
LT1226	250	0.075†	1000	50	1000	8000	J8, N8, S8	
LT1227C	500	0.050†	140.0	1	10000	3000	N8, S8	Current Feedback Amplifier
LT1228	300	0.045†	100	—	10000	—	J8, N8, S8	Electronic DC Gain Control
LM318	50	1†	15	25	10000	500	H, J8, N8	Inverting Applications Can Use External Compensation to Set 150V/µs Slew Rate
LT318A	50	1†	15	200	1000	250	H, J8, N8, S8	
OP-15E	10	4.5	6	100	500	0.05	H, N8	Precision JFET Input, No Phase Reversal
OP-15F	7.5	4.5	5.7	75	1000	0.1	H, N8	
OP-15G	5	4.7	5.4	50	3000	0.2	H, N8	
OP-16E	18	3.8	8	100	500	0.05	H, N8	
OP-16F	12	3.8	7.6	75	1000	0.1	H, N8	
OP-16G	9	4.0	7.2	50	3000	0.2	H, N8	

† To 0.1%

†† Typical Value

* Not recommended for Fast Settling Applications.

** 10V Step, to 1mV at Sum Node.

*** Maximum Value, 10V Step, to 1mV at Sum Node.

NOTE: See page 4-3 for DESC Cross Reference Numbers

COMMERCIAL HIGH SPEED OP AMPS

	ELECTRICAL CHARACTERISTICS							
PART NUMBER	MIN SLEW RATE (V/µs)	TYP SETTLING TIME TO 0.01 % (µs)	TYPICAL GAIN BANDWIDTH PRODUCT (MHz)	MIN A_{VOL} (V/mV)	MAX V_{OS} (µV)	I_B MAX (nA)	PACKAGES AVAILABLE	IMPORTANT FEATURES
DUAL								
LT1057AC	10	1.4	3.5	150	450	0.05	H, J8	Low Offset Voltage, JFET Input
LT1057ACN8	10	1.4	3.5	150	450	0.05	N8	
LT1057C	8	1.4	3	100	800	0.075	H, J8	
LT1057CN8	8	1.4	3	100	800	0.075	N8	
LT1057S	8	1.4	3	100	2000	0.1	S	
LT1057IS	8	1.4	3	100	2000	0.1	S	
LT1229	300	0.045†	100	—	15000	—	N8, J8, S8	Fast Slew Rate, Current Feedback Architecture
LF412AC	10	2.3	5.7	100	1000	0.1	H, J8, N8	JFET Input
OP-215E	10	2.3	5.7	150	1000	0.1	H, J8, N8	JFET Input
OP-215G	8	2.4	5.5	50	3000	0.2	H, J8, N8	
OP-237E	10	*	40	3000	80	40	J, N	Dual Matched OP-37
OP-237G	10	*	40	2000	180	80	J, N	
QUAD								
LT1058AC	10	1.4	3.5	150	600	0.05	J	Lowest Offset Voltage, Quad JFET, Input Op Amp
LT1058ACN	10	1.4	3.5	150	600	0.05	N	
LT1058C	8	1.4	3	100	1000	0.075	J	
LT1058CN	8	1.4	3	—	1000	0.075	N	
LT1230	300	0.045†	100	—	15000	—	N, J, S	Fast Slew Rate, Current Feedback Architecture

† To 0.1% *Not recommended for Fast Settling Applications. **10V Step, to 1mV at Sum Node. ***Maximum Value, 10V Step, to 1mV at Sum Node.

NOTE: See page 4-3 for DESC Cross Reference Numbers

SELECTION BY DESIGN PARAMETER

LOW OFFSET VOLTAGE — Max Input Offset Voltage ($T_A = 25°C$)

≤ 15µV	≤ 25µV	≤ 75µV	≤ 150µV	≤ 1mV
LT1001AM	LT1001AC	LT1001	LT1002	LF412A
LTC1047	LT1007A	LT1002A (D)	LT1006	LH2108A (D)
LTC1049	LT1012A	LT1006A	LT1008	LM108A
LTC1050	LT1037A	LT1007	LT1012S8	LM308A
LTC1050A	OP-07A	LT1012	LT1013A (D)	LT1013 (D)
LTC1051	OP-27A	LT1012D	LT1024 (D)	LT1014 (Q)
LTC1052	OP-27E	LT1012S8	LT1028	LT1014A (Q)
LTC1053	OP-37A	LT1024A (D)	LT1055AM	LT1022 ALL
LTC1150	OP-37E	LT1037	LT1055AC	LT1055M
LTC7652		LT1077	LT1079A (Q)	LT1055C
		LT1078A (D)	LT1124 (D)	LT1056AM
		LT1097C	LT1125A (Q)	LT1056AC
		LT1097S8	LT1126 (D)	LT1056M
		LT1124A (D)	LT1127A (Q)	LT1056C
		LT1126A (D)	LT1178 (D)	LT1057 ALL (D)
		LT1178A (D)	LT1179 (Q)	LT1058 ALL (Q)
		OP-07E	LT1179A (Q)	LT1078 (D)
		OP-07	OP-05A	LT1079 (Q)
		OP-97A	OP-07C, D	LT1115C
		OP-97E	OP-27C	LT1122 ALL
			OP-37C	LT1125 (Q)
			OP-227A, E (D)	LT1127 (Q)
			OP-237A, E (D)	LT1191
				LT1192
				LT1220
				LT1221
				LT1222
				OP-05
				OP-05E
				OP-15A, E
				OP-15B, F
				OP-16A, E
				OP-16B, F
				OP-215A, E (D)

(D) — Dual Op Amp
(Q) — Quad Op Amp

SELECTION BY DESIGN PARAMETER

LOW BIAS CURRENT

Max Input Bias Current ($T_J = 25°C$)

≤ 0.2nA	≤ 3nA	≤ 5nA	≤ 10nA
LF155 ALL	LM108	LT1001	LM308A
LF156 ALL	LM108A	LT1002 (D)	LT1077A
LF412A ALL	LT1001A	LT1178A (D)	LT1078 (D)
LT1008	LT1002A (D)	LT1179A (Q)	LT1078A (D)
LT1012 ALL	LT1006 ALL	OP-05E	LT1079 (Q)
LT1022 ALL	OP-05	OP-07E	LT1079A (Q)
LT1024 ALL (D)	OP-05A		LT1178 (D)
LT1055 ALL	OP-07		LT1179 (Q)
LT1056 ALL	OP-07A		OP-05C
LT1057 ALL (D)			
LT1058 ALL (Q)			
LT1097			
LT1122 ALL			
LTC1047 (D)			
LTC1049 ALL			
LTC1050			
LTC1051			
LTC1052			
LTC1053			
LTC1150			
LTC7652			
OP-15 ALL			
OP-16 ALL			
OP-97A/E			
OP-215 ALL (D)			

(D) — Dual Op Amp
(Q) — Quad Op Amp

SINGLE SUPPLY OPERATION

(Inputs and Outputs Operate Down to Ground with +V, GND Voltage Supplies)

SINGLE	DUAL	QUAD
LT1006	LT1013	LT1014
LT1077	LT1078	LT1079
LTC1049	LT1178	LT1179
LTC1050	LTC1047	LTC1053
LTC1052	LTC1051	
LTC1150		

LOW OFFSET VOLTAGE DRIFT

Maximum Offset Voltage Drift

≤ 0.05μV/°C	≤ 0.6μV/°C	≤ 1μV/°C	≤ 1.5μV/°C	≤ 2.0μV/°C	≤ 3μV/°C	≤ 5μV/°C
LTC1047 (D)	LT1001A	LT1001	LT1002 (D)	LM10*	LT1006CN8	LH2108A (D)
LTC1050	LT1007A	LT1002A (D)	LT1006A	LM10B*	LT1013C (D)	LM10C*
LTC1050A	LT1012A	LT1007	LT1008	LT1006	LT1013M (D)	LM108A
LTC1051 (D)	LT1037A	LT1012C	LT1012M	LT1012D	LT1014C (Q)	LM308A
LTC1052	LTC1049 ALL	LT1037	LT1024A (D)	LT1012S8	LT1014M (Q)	LT1006S8
LTC1053 (Q)	OP-07A	LT1028 ALL	LT1124 (D)	LT1013A (D)	LT1078 (D)	LT1013D (D)
LTC1150	OP-27A/E	LT1124A (D)	LT1125 (Q)	LT1014A (Q)	LT1079 (Q)	LT1014D (Q)
	OP-37A/E	LT1125A (Q)	LT1126 (D)	LT1024 (D)	LT1178 (D)	LT1022A
		LT1126A (D)	LT1127 (Q)	LT1078A (D)	LT1179 (Q)	LT1055A
		LT1127A (Q)	OP-07	LT1079A (Q)		LT1056A
		OP-05A/E	OP-07E	OP-05		OP-05C
		OP-227A/E		OP-07C		OP-15A/E
		OP-237A/E		OP-27C/G		OP-16A/E
				OP-37C/G		
				OP-227C/G		
				OP-237C/G		

*Typical (D) — Dual Op Amp (Q) — Quad Op Amp

SELECTION BY DESIGN PARAMETER

LOW NOISE

Typ Equivalent Input Noise Voltage per $\sqrt{Hz}$, $f = 10Hz$, $R_S = 100\Omega$

$\le 1nV/\sqrt{Hz}$	$\le 25nV/\sqrt{Hz}$
LT1028 ALL	*LF155 ALL
LT1115	*LF156 ALL
	*LF355 ALL
	LT1001 ALL
	LT1002 ALL (D)
$\le 5nV/\sqrt{Hz}$	LT1006 ALL
LT1007 ALL	LT1008
LT1037 ALL	LT1012
LT1124 ALL (D)	LT1013 ALL (D)
LT1125 ALL (Q)	LT1014 ALL (D)
LT1126 ALL (D)	LT1022 ALL
LT1127 ALL (Q)	*LT1055 ALL
OP-27 ALL	*LT1056 ALL
OP-37 ALL	LTC7652
OP-227 ALL (D)	OP-05 ALL
OP-237 ALL (D)	OP-07 ALL
	*OP-15 ALL
	*OP-16 ALL

*100 Hz Noise (D) — Dual Op Amp

HIGH SLEW RATE

Typ Slew Rate

$\ge 10V/\mu s$	$\ge 50V/\mu s$	$\ge 100V/\mu s$
LF412A (D)	LM118/318	LT1190
LT1022 ALL	LT118A/318A	LT1191
LT1028 ALL	LT1010	LT1192
LT1037 ALL	LT1122 ALL	LT1193
LT1055 ALL	LT1200	LT1194
LT1056A		LT1217
LT1057A (D)		LT1220
LT1058A (Q)		LT1221
LT1115		LT1222
LT1126 ALL (D)		LT1223
LT1127 ALL (Q)		LT1224
OP-16A, B		LT1225
OP-16E, F		LT1226
OP-37 ALL		LT1227
OP-215A, E (D)		LT1228
OP-237 ALL (D)		LT1229 (D)
		LT1230 (Q)

(D) — Dual Op Amp (Q) — Quad Op Amp

LOW POWER

Maximum Supply Current (per Amplifier)

$\le 50\mu A$	$\le 60\mu A$	$\le 1mA$
LT1078A (D)	LT1077	LH2108A (D)
LT1079A (Q)	LT1078 (D)	LM108A
LT1178 (D)	LT1079 (Q)	LT1006
LT1178A (D)		LT1008
LT1179 (Q)		LT1012 ALL
LT1179A (Q)		LT1013 (D)
		LT1014 (Q)
		LT1024 (D)
		LT1079
		LTC1047
		LTC1049 ALL
		OP-97A/E

(D) — Dual Op Amp (Q) — Quad Op Amp

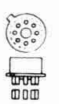
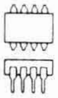
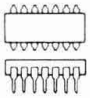
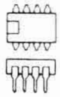
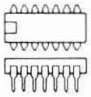
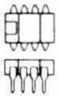
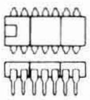
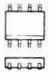
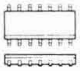
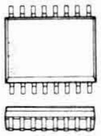
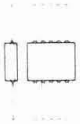
HIGH GAIN

Typ Open Loop Gain

$\ge 200\,\frac{V}{mV}$	$\ge 1000\,\frac{V}{mV}$
LT118A	LT1006A
LT318A	LT1007
LT1001	LT1012 ALL
LT1002 (D)	LT1013 (D)
LT1006	LT1014 (Q)
LT1008	LT1028
LT1077	LT1037
LT1078 (D)	LT1077
LT1079 (Q)	LT1078
LT1178 (D)	LT1079
LT1179 (Q)	LT1097
OP-05	LT1115
OP-07	LT1124
	LT1125
	LT1126
	LT1127
	LTC1049 ALL
	LTC1050
	LTC1051
	LTC1052
	LTC1053
	LTC7652
	OP-27
	OP-37
	OP-97A/E
	OP-227 (D)
	OP-237 (D)

(D) — Dual Op Amp (Q) — Quad Op Amp

PACKAGES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NOTES

SECTION 2—AMPLIFIERS

PRECISION OPERATIONAL AMPLIFIERS

LT1007CS8/LT1037CS8, Low Noise, High Speed Precision Operational Amplifiers 2-16
LT1013/LT1014, Dual/Quad Precision Operational Amplifiers 2-19
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LT1128, Unity Gain Stable Ultra-Low Noise Precision LT1028 Type Operational Amplifier 13-50
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PRECISION OPERATIONAL AMPLIFIERS, *ENHANCED* AND SECOND SOURCE

OP-270/OP-470, Dual/Quad Low Noise, Precision Operational Amplifiers 2-120

LINEAR TECHNOLOGY

LT1007CS8/LT1037CS8

Low Noise, High Speed Precision Operational Amplifiers

FEATURES

- *Guaranteed* 4.5nV/√Hz 10Hz Noise
- *Guaranteed* 3.8nV/√Hz 1kHz Noise
- 0.1Hz to 10Hz Noise, 60nVp-p, Typical
- *Guaranteed* 5 Million Min. Voltage Gain, R_L = 2kΩ
- *Guaranteed* 2 Million Min. Voltage Gain, R_L = 600Ω
- *Guaranteed* 60μV Max. Offset Voltage
- *Guaranteed* 1.0μV/°C Max. Drift with Temperature
- *Guaranteed* 11V/μsec Min. Slew Rate (LT1037)
- *Guaranteed* 110dB Min. CMRR

APPLICATIONS

- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Sine Wave Generators
- Tape Head Preamplifiers
- Microwave Preamplifiers

DESCRIPTION

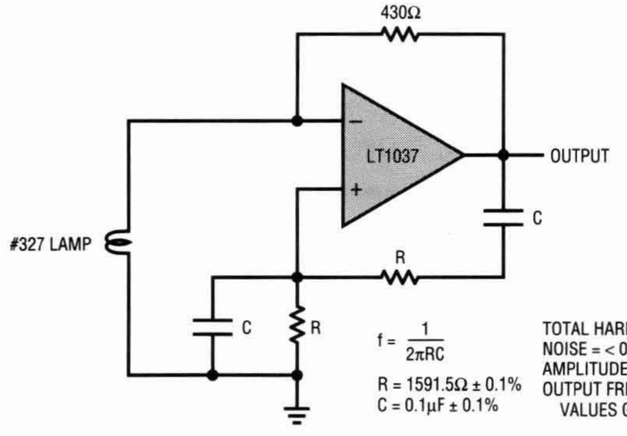
Next to the LT1028, the LT1007/LT1037 series features the lowest noise performance available to date for monolithic operational amplifiers: 2.5nV/√Hz wideband noise (less than the noise of a 400Ω resistor), 1/f corner frequency of 2Hz and 60nV peak-to-peak 0.1Hz to 10Hz noise. Low noise is combined with outstanding precision and speed specifications: 20μV offset voltage, 0.3μV/°C drift, 126dB common mode and power supply rejection, and 60MHz gain-bandwidth-product on the decompensated LT1037, which is stable for closed loop gains of 5 or greater.

The voltage gain of the LT1007/LT1037 is an extremely high 20 million driving a 2kΩ load and 12 million driving a 600Ω load to ±10V.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications have been spectacularly improved compared to competing amplifiers.

The sine wave generator application shown below utilizes the low noise and low distortion characteristics of the LT1037.

Ultra-Pure 1kHz Sine Wave Generator



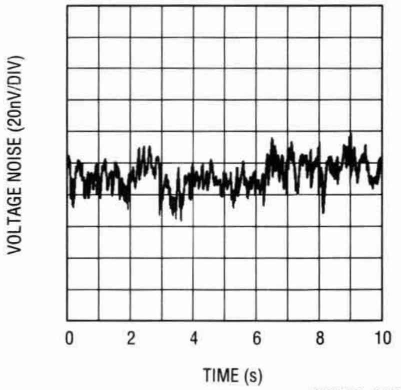
$f = \frac{1}{2\pi RC}$

R = 1591.5Ω ± 0.1%
C = 0.1μF ± 0.1%

TOTAL HARMONIC DISTORTION = < 0.0025%
NOISE = < 0.0001%
AMPLITUDE = ±8V
OUTPUT FREQUENCY = 1.000kHz FOR
VALUES GIVEN ±0.4%

LT1007CS8 • TA01

0.1Hz to 10Hz Noise

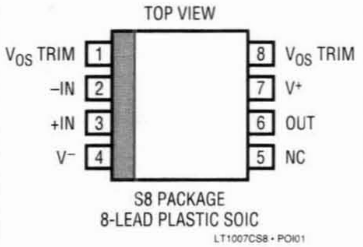


LT1007CS8 • TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Input Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Differential Input Current (Note 5)	±25mA
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	
All Devices	– 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SOIC

ORDER PART NUMBER
LT1007CS8 LT1037CS8
PART MARKING
1007 1037

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

				LT1007C LT1037C		
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	(Note 1)		20	60	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 2 and 3)		0.2	1.0	μV/Mo
I_{OS}	Input Offset Current			12	50	nA
I_B	Input Bias Current			±15	±55	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		0.06	0.13	μVp-p
	Input Noise Voltage Density	f_O = 10Hz (Note 3) f_O = 1000Hz (Note 3)		2.8 2.5	4.5 3.8	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz (Note 3) f_O = 1000Hz (Note 3)		1.5 0.4	4.0 0.6	pA/√Hz pA/√Hz
	Input Resistance—Common Mode			5		GΩ
	Input Voltage Range		±11.0	±12.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11V$	110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	106	126		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm12V$ $R_L \geq 1k\Omega$, $V_O = \pm10V$ $R_L \geq 600\Omega$, $V_O = \pm10V$	5.0 3.5 2.0	20.0 16.0 12.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.5 ±10.5	±13.5 ±12.5		V V
SR	Slew Rate LT1007 LT1037	$R_L \geq 2k\Omega$ $A_{VCL} \geq 5$	1.7 11	2.5 15		V/μs V/μs
GBW	Gain-Bandwidth Product LT1007 LT1037	f_O = 100kHz (Note 4) f_O = 10kHz (Note 4), ($A_{VCL} \geq 5$)	5.0 45	8.0 60		MHz MHz
Z_O	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		70		Ω
P_d	Power Dissipation LT1007 LT1037			80 85	140 140	mW mW

ELECTRICAL CHARACTERISTICS

V_S = ±15V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

					LT1007C LT1037C		
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	(Note 1)	●		35	110	µV
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Drift	(Note 6)	●		0.3	1.0	µV/°C
I_{OS}	Input Offset Current		●		15	70	nA
I_B	Input Bias Current		●		±20	±75	nA
	Input Voltage Range		●	±10.5	±11.8		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10.5V	●	106	120		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	●	102	120		dB
A_{VOL}	Large Signal Voltage Gain	R_L ≥ 2kΩ, V_O = ±10V	●	2.5	18.0		V/µV
		R_L ≥ 1kΩ, V_O = ±10V	●	2.0	14.0		V/µV
V_{OUT}	Maximum Output Voltage Swing	R_L ≥ 2kΩ	●	±12.0	±13.6		V
P_d	Power Dissipation		●		90	160	mW

The ● denotes the specifications which apply over full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 seconds after application of power.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5µV.

Note 3: This parameter is tested on a sample basis only.

Note 4: This parameter is guaranteed by design and is not tested.

Note 5: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Note 6: The Average Input Offset Drift performance is within the specifications unnulled or when nulled with a pot having a range of 8kΩ to 20kΩ.

LT1013/LT1014

Quad Precision Op Amp (LT1014)
Dual Precision Op Amp (LT1013)

FEATURES

■ Single Supply Operation Input Voltage Range Extends to Ground Output Swings to Ground while Sinking Current	
■ Pin Compatible to 1458 and 324 with Precision Specs	
■ *Guaranteed* Offset Voltage	150μV Max.
■ *Guaranteed* Low Drift	2μV/°C Max.
■ *Guaranteed* Offset Current	0.8nA Max.
■ *Guaranteed* High Gain	
5mA Load Current	1.5 Million Min.
17mA Load Current	0.8 Million Min.
■ *Guaranteed* Low Supply Current	500μA Max.
■ Low Voltage Noise, 0.1Hz to 10Hz	0.55μVp-p
■ Low Current Noise—Better than OP-07, 0.07 pA/√Hz	

APPLICATIONS

- Battery-Powered Precision Instrumentation
  - Strain Gauge Signal Conditioners
  - Thermocouple Amplifiers
  - Instrumentation Amplifiers
- 4mA–20mA Current Loop Transmitters
- Multiple Limit Threshold Detection
- Active Filters
- Multiple Gain Blocks

DESCRIPTION

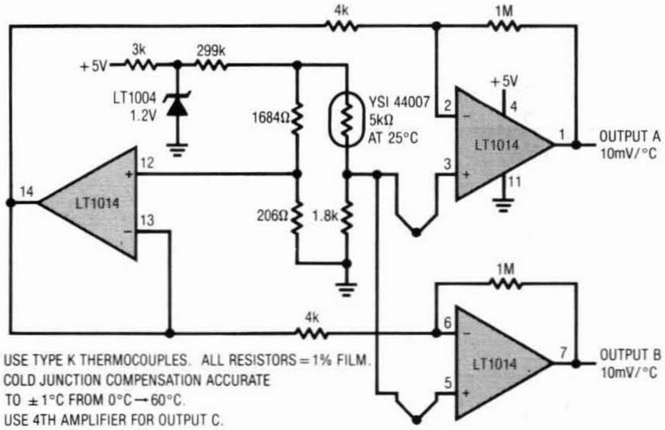
The LT1014 is the first precision quad operational amplifier which directly upgrades designs in the industry standard 14-pin DIP LM324/LM348/OP-11/4156 pin configuration. It is no longer necessary to compromise specifications, while saving board space and cost, as compared to single operational amplifiers.

The LT1014's low offset voltage of 50μV, drift of 0.3μV/°C, offset current of 0.15nA, gain of 8 million, common-mode rejection of 117dB, and power supply rejection of 120dB qualify it as four truly precision operational amplifiers. Particularly important is the low offset voltage, since no offset null terminals are provided in the quad configuration. Although supply current is only 350μA per amplifier, a new output stage design sources and sinks in excess of 20mA of load current, while retaining high voltage gain.

Similarly, the LT1013 is the first precision dual op amp in the 8-pin industry standard configuration, upgrading the performance of such popular devices as the MC1458/1558, LM158 and OP-221. The LT1013's specifications are similar to (even somewhat better than) the LT1014's.

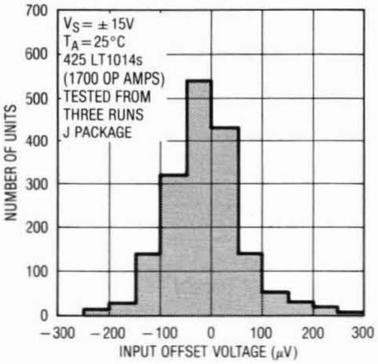
Both the LT1013 and LT1014 can be operated off a single 5V power supply: input common-mode range includes ground; the output can also swing to within a few millivolts of ground. Crossover distortion, so apparent on previous single-supply designs, is eliminated. A full set of specifications is provided with ±15V and single 5V supplies.

3 Channel Thermocouple Thermometer



USE TYPE K THERMOCOUPLES. ALL RESISTORS = 1% FILM.
COLD JUNCTION COMPENSATION ACCURATE
TO ±1°C FROM 0°C → 60°C.
USE 4TH AMPLIFIER FOR OUTPUT C.

LT1014 Distribution of Offset Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Differential Input Voltage .... ±30V
Input Voltage .... Equal to Positive Supply Voltage
.... 5V Below Negative Supply Voltage
Output Short Circuit Duration .... Indefinite
Storage Temperature Range
All Grades .... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.)............. 300°C
Operating Temperature Range
LT1013AM/LT1013M/
LT1014AM/LT1014M .... −55°C to 125°C
LT1013AC/LT1013C/LT1013D
LT1014AC/LT1014C/LT1014D............... 0°C to 70°C
LT1013I/LT1014I .... −40°C to 85°C

PACKAGE/ORDER INFORMATION

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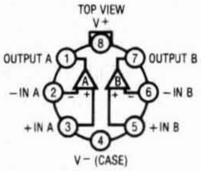
<td>

TOP VIEW
V+
OUTPUT A
OUTPUT B
−IN A
−IN B
+IN A
+IN B
A
B
1
2
3
4
5
6
7
8
V− (CASE)

H PACKAGE
8-LEAD TO-5 METAL CAN</td>
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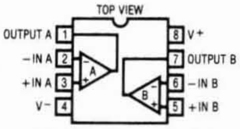
LT1013AMH
LT1013MH
LT1013ACH
LT1013CH</td>
<td>

TOP VIEW
OUTPUT A
−IN A
+IN A
V−
V+
OUTPUT B
−IN B
+IN B
A
B
1
2
3
4
5
6
7
8

J PACKAGE
8-LEAD CERAMIC DIP
N PACKAGE
8-LEAD PLASTIC DIP</td>
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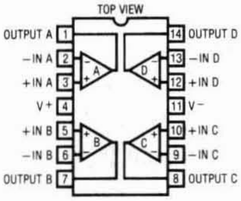
LT1013MJ8
LT1013ACJ8
LT1013CJ8
LT1013CN8
LT1013DN8
LT1013IN8</td>
<td>

TOP VIEW
OUTPUT A
−IN A
+IN A
V+
+IN B
−IN B
OUTPUT B
OUTPUT D
−IN D
+IN D
V−
+IN C
−IN C
OUTPUT C
A
B
C
D
1
2
3
4
5
6
7
8
9
10
11
12
13
14

J PACKAGE
14-LEAD CERAMIC DIP
N PACKAGE
14-LEAD PLASTIC DIP</td>
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LT1014MJ
LT1014ACJ
LT1014CJ
LT1014CN
LT1014DN
LT1014IN</td>
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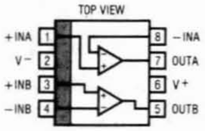
<td>

TOP VIEW
+INA
V−
+INB
−INB
−INA
OUTA
V+
OUTB
1
2
3
4
5
6
7
8

SO PACKAGE
8-LEAD PLASTIC SOIC
NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE STANDARD 8-PIN DUAL-IN-LINE CONFIGURATION</td>
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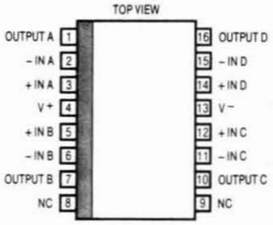
LT1013DS8
LT1013IS8
PART MARKING
1013
1013I</td>
<td>

TOP VIEW
OUTPUT A
−IN A
+IN A
V+
+IN B
−IN B
OUTPUT B
NC
OUTPUT D
−IN D
+IN D
V−
+IN C
−IN C
OUTPUT C
NC
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

S PACKAGE
16-LEAD PLASTIC SOL</td>
<td>ORDER PART NUMBER
LT1014DS
LT1014IS
PART MARKING
LT1014DS
LT1014IS</td>
</tr>
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ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM/AC LT1014AM/AC			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1013 LT1014 LT1013D/I, LT1014D/I	— — —	40 50 —	150 180 —	— — —	60 60 200	300 300 800	μV μV μV
	Long Term Input Offset Voltage Stability		—	0.4	—	—	0.5	—	μV/Mo.
I_{OS}	Input Offset Current		—	0.15	0.8	—	0.2	1.5	nA
I_B	Input Bias Current		—	12	20	—	15	30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz	—	0.55	—	—	0.55	—	μVp-p
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1000Hz$	— —	24 22	— —	— —	24 22	— —	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_0 = 10Hz$	—	0.07	—	—	0.07	—	$pA/\sqrt{Hz}$
	Input Resistance—Differential Common-Mode	(Note 1)	100 —	400 5	— —	70 —	300 4	— —	MΩ GΩ

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM/AC LT1014AM/AC			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	1.5	8.0	—	1.2	7.0	—	V/μV
		$V_O = \pm 10V$, $R_L = 600\Omega$	0.8	2.5	—	0.5	2.0	—	V/μV
	Input Voltage Range		+13.5	+13.8	—	+13.5	+13.8	—	V
			−15.0	−15.3	—	−15.0	−15.3	—	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.5V$, $-15.0V$	100	117	—	97	114	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	103	120	—	100	117	—	dB
	Channel Separation	$V_O = \pm 10V$, $R_L = 2k$	123	140	—	120	137	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	±13	±14	—	±12.5	±14	—	V
	Slew Rate		0.2	0.4	—	0.2	0.4	—	V/μs
I_S	Supply Current	Per Amplifier	—	0.35	0.50	—	0.35	0.55	mA

Note 1: This parameter is guaranteed by design and is not tested. Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1014s (or 100 LT1013s) typically 240 op amps (or 120) will be better than the indicated specification.

ELECTRICAL CHARACTERISTICS

$V_S^+ = +5V$, $V_S^- = 0V$, $V_{OUT} = 1.4V$, $V_{CM} = 0V$, $T_A = 25°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1013AM/AC LT1014AM/AC			LT1013C/D/I/M LT1014C/D/I/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1013	—	60	250	—	90	450	μV
		LT1014	—	70	280	—	90	450	μV
		LT1013D/I, LT1014D/I	—	—	—	—	250	950	μV
I_{OS}	Input Offset Current		—	0.2	1.3	—	0.3	2.0	nA
I_B	Input Bias Current		—	15	35	—	18	50	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = 5mV$ to $4V$, $R_L = 500\Omega$	—	1.0	—	—	1.0	—	V/μV
	Input Voltage Range		+3.5	+3.8	—	+3.5	+3.8	—	V
			0	−0.3	—	0	−0.3	—	V
V_{OUT}	Output Voltage Swing	Output Low, No Load	—	15	25	—	15	25	mV
		Output Low, 600Ω to Ground	—	5	10	—	5	10	mV
		Output Low, $I_{SINK} = 1mA$	—	220	350	—	220	350	mV
		Output High, No Load	4.0	4.4	—	4.0	4.4	—	V
		Output High, 600Ω to Ground	3.4	4.0	—	3.4	4.0	—	V
I_S	Supply Current	Per Amplifier	—	0.31	0.45	—	0.32	0.50	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$ unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1013AM			LT1014AM			LT1013M/LT1014M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	—	80	300	—	90	350	—	110	550	μV
		$V_S = +5V, 0V; V_O = +1.4V$											
		$-55°C \le T_A \le 100°C$	●	—	80	450	—	90	480	—	100	750	μV
		$V_{CM} = 0.1V, T_A = 125°C$		—	120	450	—	150	480	—	200	750	μV
		$V_{CM} = 0V, T_A = 125°C$		—	250	900	—	300	960	—	400	1500	μV
	Input Offset Voltage Drift	(Note 2)	●	—	0.4	2.0	—	0.4	2.0	—	0.5	2.5	μV/°C
I_{OS}	Input Offset Current		●	—	0.3	2.5	—	0.3	2.8	—	0.4	5.0	nA
		$V_S = +5V, 0V; V_O = +1.4V$	●	—	0.6	6.0	—	0.7	7.0	—	0.9	10.0	nA
I_B	Input Bias Current		●	—	15	30	—	15	30	—	18	45	nA
		$V_S = +5V, 0V; V_O = +1.4V$	●	—	20	80	—	25	90	—	28	120	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	●	0.5	2.0	—	0.4	2.0	—	0.25	2.0	—	V/μV
CMRR	Common-Mode Rejection	$V_{CM} = +13.0V, -14.9V$	●	97	114	—	96	114	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	100	117	—	100	117	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12	±13.8	—	±12	±13.8	—	±11.5	±13.8	—	V
		$V_S = +5V, 0V;$ $R_L = 600\Omega$ to Ground											
		Output Low	●	—	6	15	—	6	15	—	6	18	mV
		Output High	●	3.2	3.8	—	3.2	3.8	—	3.1	3.8	—	V
I_S	Supply Current Per Amplifier		●	—	0.38	0.60	—	0.38	0.60	—	0.38	0.7	mA
		$V_S = +5V, 0V; V_O = +1.4V$	●	—	0.34	0.55	—	0.34	0.55	—	0.34	0.65	mA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$ for LT1013I, LT1014I, $0°C \le T_A \le 70°C$ for LT1013C, LT1013D, LT1014C, LT1014D unless otherwise noted

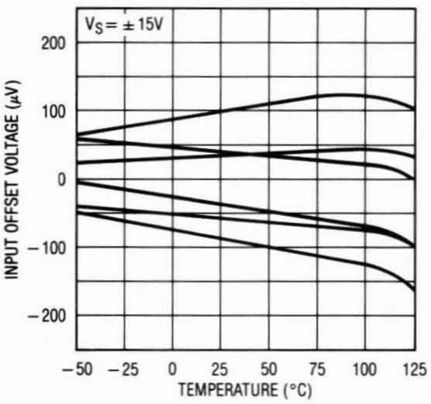
SYMBOL	PARAMETER	CONDITIONS		LT1013AC			LT1014AC			LT1013C/D/I LT1014C/D/I			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	—	55	240	—	65	270	—	80	400	μV
		LT1013D/I, LT1014D/I	●	—	—	—	—	—	—	—	230	1000	μV
		$V_S = +5V, 0V; V_O = 1.4V$	●	—	75	350	—	85	380	—	110	570	μV
		LT1013D/I, LT1014D/I $V_S = +5V, 0V; V_O = 1.4V$	●	—	—	—	—	—	—	—	280	1200	μV
	Average Input Offset Voltage Drift	(Note 2)	●	—	0.3	2.0	—	0.3	2.0	—	0.4	2.5	μV/°C
		LT1013D/I, LT1014D/I	●	—	—	—	—	—	—	—	0.7	5.0	μV/°C
I_{OS}	Input Offset Current		●	—	0.2	1.5	—	0.2	1.7	—	0.3	2.8	nA
		$V_S = +5V, 0V; V_O = 1.4V$	●	—	0.4	3.5	—	0.4	4.0	—	0.5	6.0	nA
I_B	Input Bias Current		●	—	13	25	—	13	25	—	16	38	nA
		$V_S = +5V, 0V; V_O = 1.4V$	●	—	18	55	—	20	60	—	24	90	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V, R_L = 2k$	●	1.0	5.0	—	1.0	5.0	—	0.7	4.0	—	V/μV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = +13.0V, -15.0V$	●	98	116	—	98	116	—	94	113	—	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2V$ to $\pm 18V$	●	101	119	—	101	119	—	97	116	—	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	±12.5	±13.9	—	±12.5	±13.9	—	±12.0	±13.9	—	V
		$V_S = +5V, 0V; R_L = 600\Omega$											
		Output Low	●	—	6	13	—	6	13	—	6	13	mV
		Output High	●	3.3	3.9	—	3.3	3.9	—	3.2	3.9	—	V
I_S	Supply Current per Amplifier		●	—	0.36	0.55	—	0.36	0.55	—	0.37	0.60	mA
		$V_S = +5V, 0V; V_O = 1.4V$	●	—	0.32	0.50	—	0.32	0.50	—	0.34	0.55	mA

Note 2: This parameter is not 100% tested.

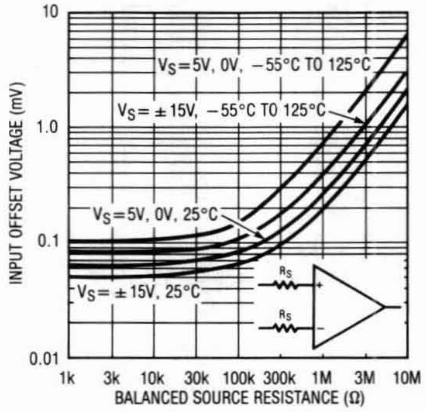
The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

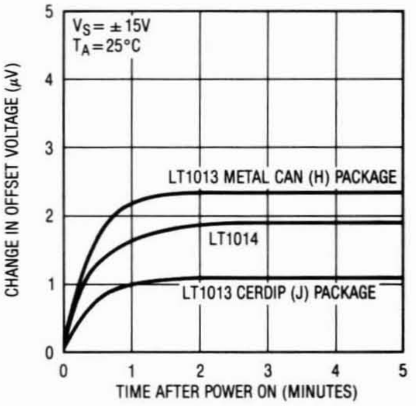
Offset Voltage Drift with Temperature of Representative Units



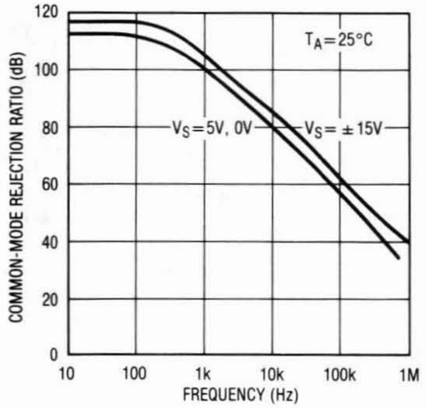
Offset Voltage vs Balanced Source Resistance



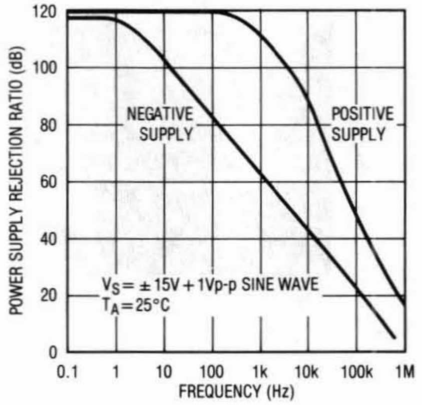
Warm-Up Drift



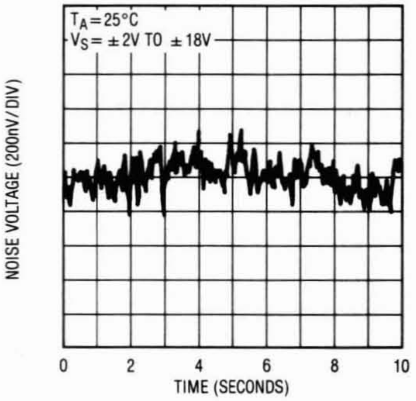
Common-Mode Rejection Ratio vs Frequency



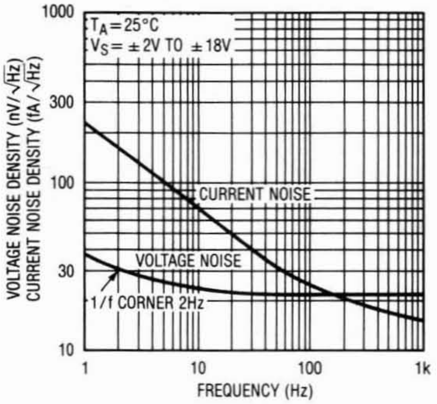
Power Supply Rejection Ratio vs Frequency



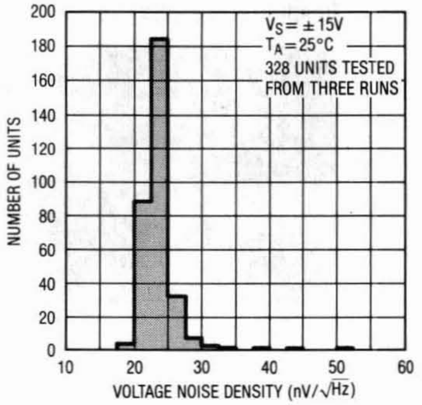
0.1Hz to 10Hz Noise



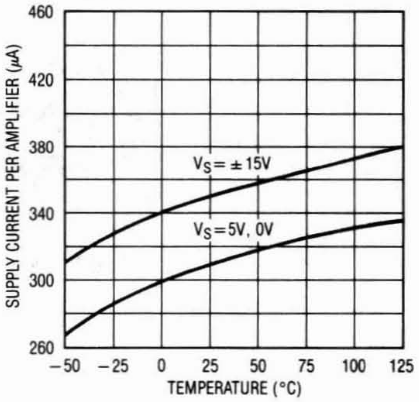
Noise Spectrum



10Hz Voltage Noise Distribution

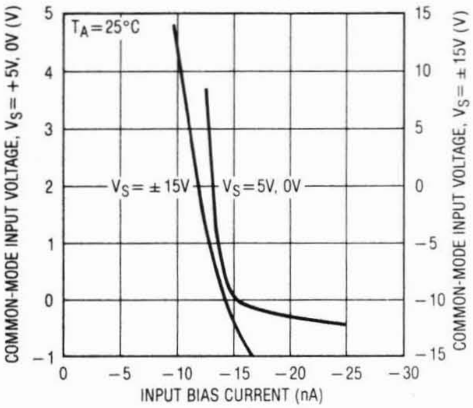


Supply Current vs Temperature

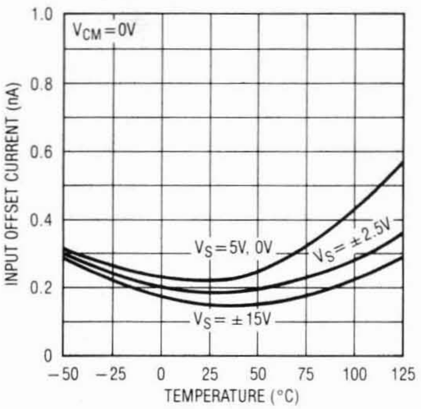


TYPICAL PERFORMANCE CHARACTERISTICS

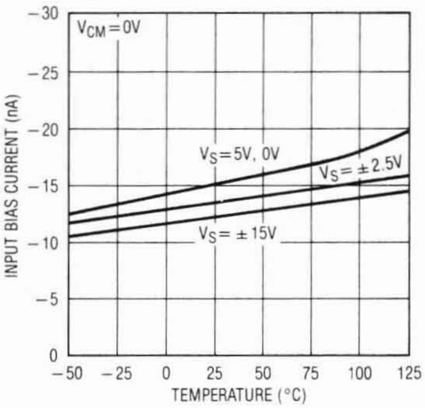
Input Bias Current vs Common-Mode Voltage



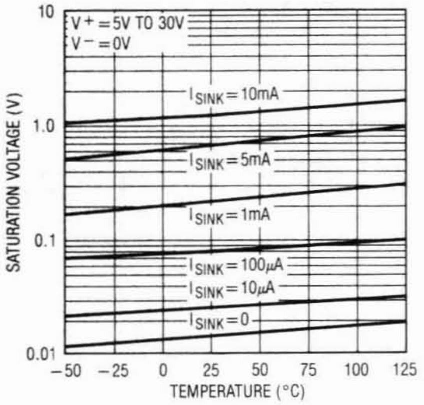
Input Offset Current vs Temperature



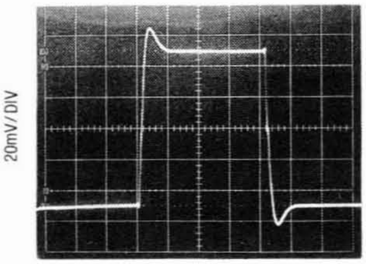
Input Bias Current vs Temperature



Output Saturation vs Sink Current vs Temperature

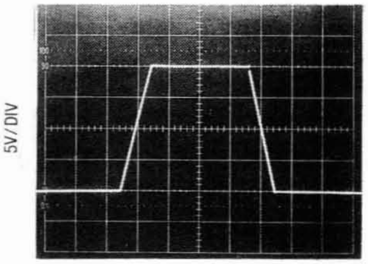


Small Signal Transient Response, $V_S = \pm 15V$



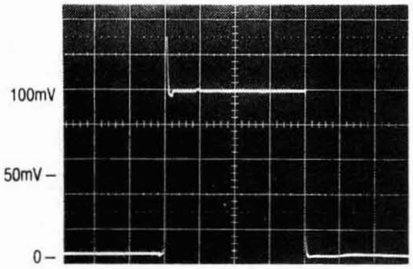
$A_V = +1$ 2μs/DIV

Large Signal Transient Response, $V_S = \pm 15V$



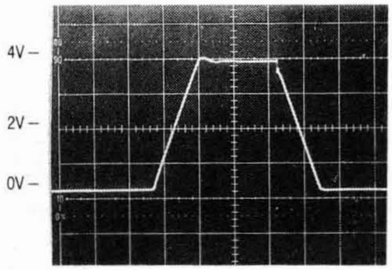
$A_V = +1$ 50μs/DIV

Small Signal Transient Response, $V_S = 5V, 0V$



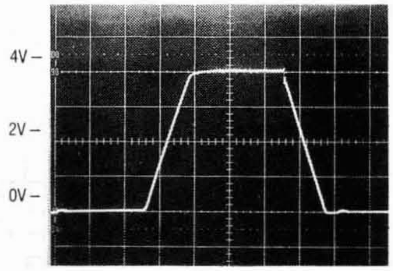
$A_V = +1$ 20μs/DIV
$R_L = 600\Omega$ TO GROUND
INPUT = 0V TO 100mV PULSE

Large Signal Transient Response, $V_S = 5V, 0V$



$A_V = +1$ 10μs/DIV
$R_L = 4.7k$ to 5V
INPUT = 0V TO 4V PULSE

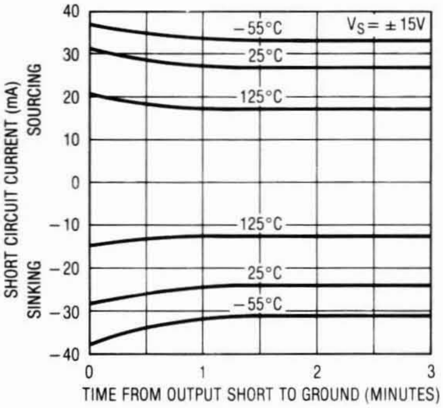
Large Signal Transient Response, $V_S = 5V, 0V$



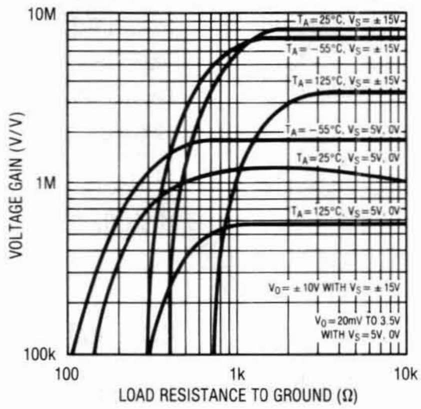
$A_V = +1$ 10μs/DIV
NO LOAD
INPUT = 0V TO 4V PULSE

TYPICAL PERFORMANCE CHARACTERISTICS

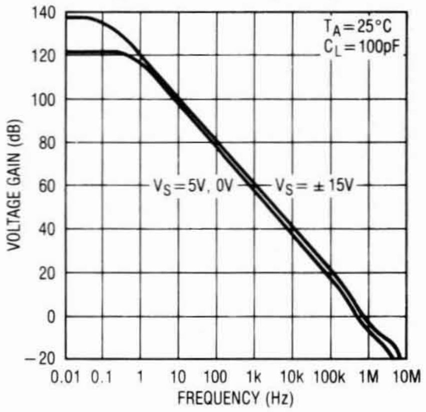
Output Short Circuit Current vs Time



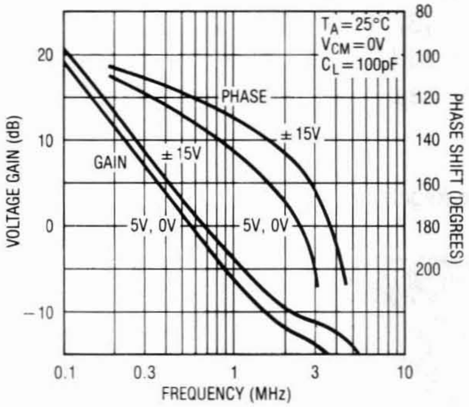
Voltage Gain vs Load Resistance



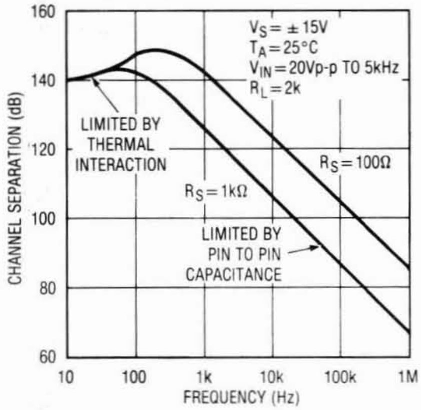
Voltage Gain vs Frequency



Gain, Phase vs Frequency



Channel Separation vs Frequency



APPLICATIONS INFORMATION

Single Supply Operation

The LT1013/1014 are fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range includes ground; the output swings within a few millivolts of ground. Single supply operation, however, can create special difficulties, both at the input and at the output. The LT1013/LT1014 have specific circuitry which addresses these problems.

At the input, the driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420:

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1013/1014, the 400Ω resistors, in series with the input (see schematic diagram), protect the devices even when the input is 5V below ground.

APPLICATIONS INFORMATION

(b) When the input is more than 400mV below ground (at 25°C), the input stage saturates (transistors Q3 and Q4) and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry (Q21, Q22, Q27, Q28), the LT1013/1014's outputs do not reverse, as illustrated below, even when the inputs are at −1.5V.

There is one circumstance, however, under which the phase reversal protection circuitry does not function: when the other op amp on the LT1013, or one specific amplifier of the other three on the LT1014, is driven hard into negative saturation at the output.

Phase reversal protection does not work on amplifier:
A when D's output is in negative saturation. B's and C's outputs have no effect.
B when C's output is in negative saturation. A's and D's outputs have no effect.
C when B's output is in negative saturation. A's and D's outputs have no effect.
D when A's output is in negative saturation. B's and C's outputs have no effect.

At the output, the aforementioned single supply designs either cannot swing to within 600mV of ground (OP-20) or cannot sink more than a few microamperes while swinging to ground (LM124, LM158). The LT1013/1014's all-NPN output stage maintains its low output resistance and high gain characteristics until the output is saturated.

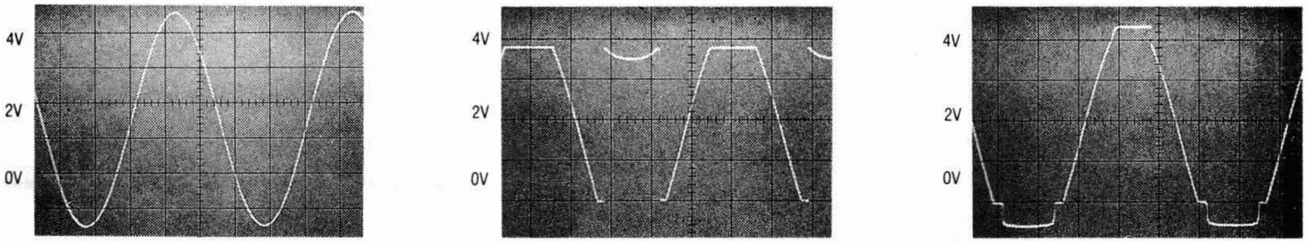
In dual supply operations, the output stage is crossover distortion-free.

Comparator Applications

The single supply operation of the LT1013/1014 lends itself to its use as a precision comparator with TTL compatible output:

In systems using both op amps and comparators, the LT1013/1014 can perform multiple duties; for example, on the LT1014, two of devices can be used as op amps and the other two as comparators.

Voltage Follower with Input Exceeding the Negative Common-Mode Range

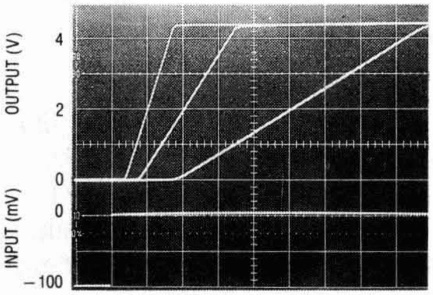


6Vp-p INPUT, −1.5V TO 4.5V

LM324, LM358, OP-20
EXHIBIT OUTPUT PHASE
REVERSAL

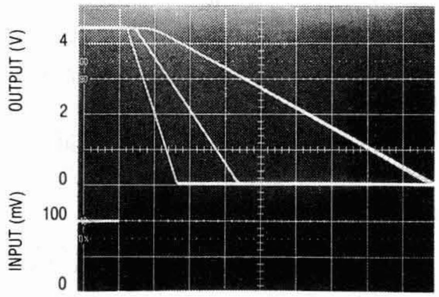
LT1013/LT1014
NO PHASE REVERSAL

Comparator Rise Response Time 10mV, 5mV, 2mV Overdrives



V_S=5V, 0V 50µs/DIV

Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives



V_S=5V, 0V 50µs/DIV

APPLICATIONS INFORMATION

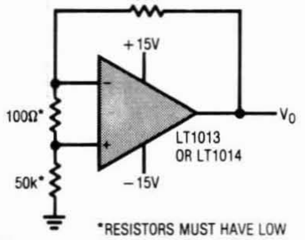
Low Supply Operation

The minimum supply voltage for proper operation of the LT1013/1014 is 3.4V (three Ni-Cad batteries). Typical supply current at this voltage is 290μA, therefore power dissipation is only one milliwatt per amplifier.

Noise Testing

For application information on noise testing and calculations, please see the LT1007 or LT1008 data sheet.

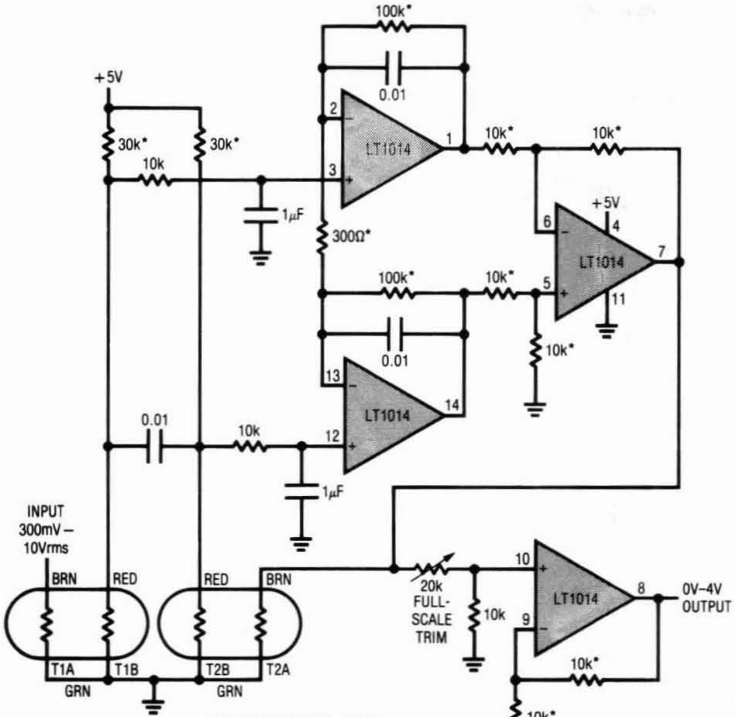
Test Circuit for Offset Voltage and Offset Drift with Temperature


50k*
+15V
100Ω*
50k*
LT1013
OR LT1014
–15V
V_O

*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.
**THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION, WITH SUPPLY VOLTAGES INCREASED TO ±20V.
$V_O = 1000V_{OS}$

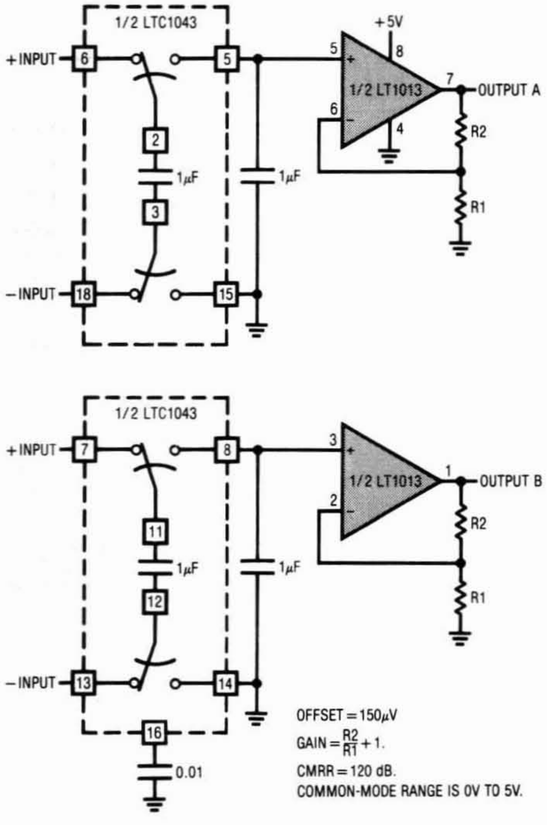
TYPICAL APPLICATIONS

50MHz Thermal rms to DC Converter


100k*
0.01
+5V
30k*
30k*
10k
1µF
300Ω*
LT1014
100k*
10k*
10k*
10k*
+5V
LT1014
10k*
0.01
LT1014
0.01
10k
1µF
INPUT
300mV –
10Vrms
BRN
RED
RED
BRN
T1A
T1B
T2B
T2A
GRN
GRN
20k
FULL-
SCALE
TRIM
10k
LT1014
10k*
10k*
0V–4V
OUTPUT

2% ACCURACY, DC—50MHz.
100:1 CREST FACTOR CAPABILITY.
*0.1% RESISTOR.
T1-T2 = YELLOW SPRINGS INST. CO. THERMISTOR COMPOSITE #44018.
ENCLOSE T1 AND T2 IN STYROFOAM.
7.5mW DISSIPATION.

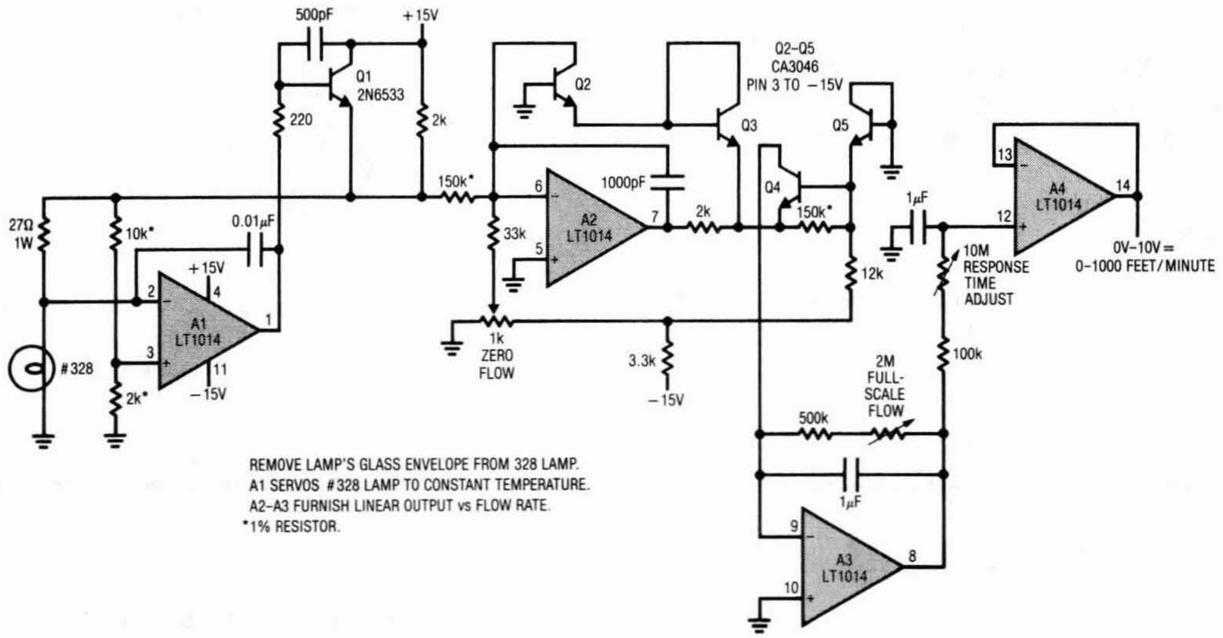
5V Single Supply Dual Instrumentation Amplifier


1/2 LTC1043
+INPUT
–INPUT
1µF
1µF
+5V
1/2 LT1013
OUTPUT A
R2
R1
1/2 LTC1043
+INPUT
–INPUT
1µF
1µF
0.01
1/2 LT1013
OUTPUT B
R2
R1

OFFSET = 150μV
GAIN = $\frac{R2}{R1} + 1$.
CMRR = 120 dB.
COMMON-MODE RANGE IS 0V TO 5V.

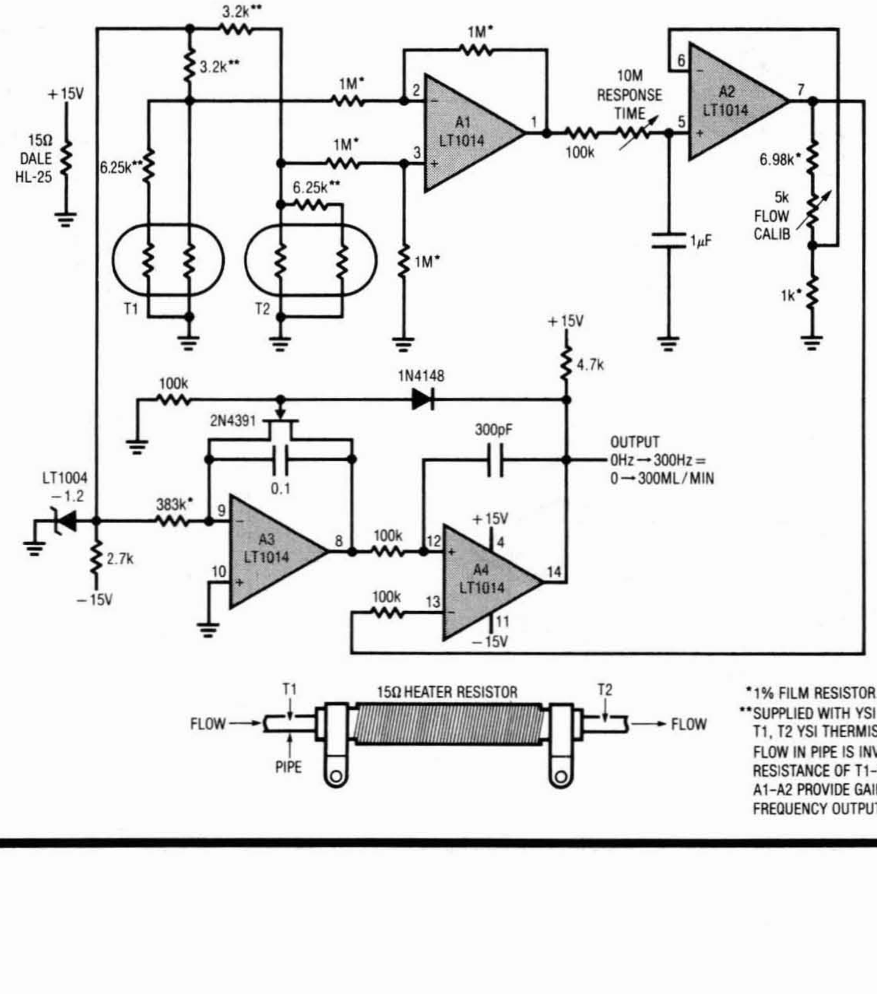
TYPICAL APPLICATIONS

Hot Wire Anemometer


500pF
+15V
Q1
2N6533
220
2k
Q2
Q3
Q2–Q5
CA3046
PIN 3 TO −15V
Q5
Q4
150k*
6
7
5
A2
LT1014
1000pF
2k
150k*
33k
1μF
12k
13
12
14
A4
LT1014
10M
RESPONSE
TIME
ADJUST
0V–10V =
0–1000 FEET/MINUTE
27Ω
1W
10k*
0.01μF
+15V
2
3
4
1
11
A1
LT1014
−15V
#328
2k*
1k
ZERO
FLOW
3.3k
−15V
100k
2M
FULL-
SCALE
FLOW
500k
1μF
9
10
8
A3
LT1014

REMOVE LAMP'S GLASS ENVELOPE FROM 328 LAMP.
A1 SERVOS #328 LAMP TO CONSTANT TEMPERATURE.
A2–A3 FURNISH LINEAR OUTPUT vs FLOW RATE.
*1% RESISTOR.

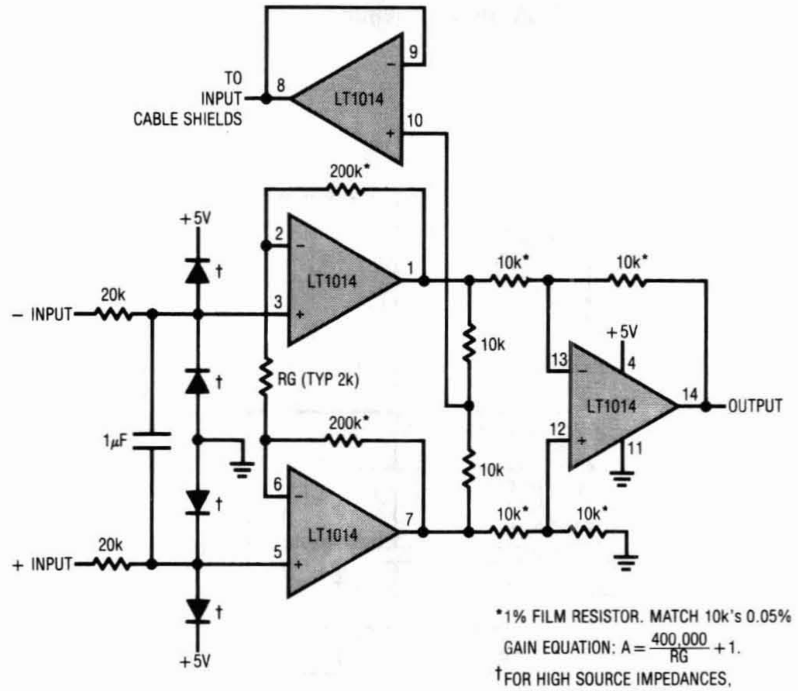
Liquid Flowmeter


3.2k**
3.2k**
1M*
1M*
1M*
+15V
15Ω
DALE
HL-25
6.25k**
6.25k**
T1
T2
1M*
2
3
1
A1
LT1014
10M
RESPONSE
TIME
100k
5
6
7
A2
LT1014
6.98k*
5k
FLOW
CALIB
1k*
1μF
+15V
4.7k
100k
1N4148
2N4391
300pF
0.1
OUTPUT
0Hz→300Hz =
0→300ML/MIN
LT1004
−1.2
383k*
2.7k
−15V
9
10
8
A3
LT1014
100k
100k
12
13
4
11
14
+15V
−15V
A4
LT1014
T1
15Ω HEATER RESISTOR
T2
FLOW
FLOW
PIPE

*1% FILM RESISTOR.
**SUPPLIED WITH YSI THERMISTOR NETWORK.
T1, T2 YSI THERMISTOR NETWORK = #44201.
FLOW IN PIPE IS INVERSELY PROPORTIONAL TO RESISTANCE OF T1–T2 TEMPERATURE DIFFERENCE.
A1–A2 PROVIDE GAIN. A3–A4 PROVIDE LINEARIZED FREQUENCY OUTPUT.

TYPICAL APPLICATIONS

5V Powered Precision Instrumentation Amplifier

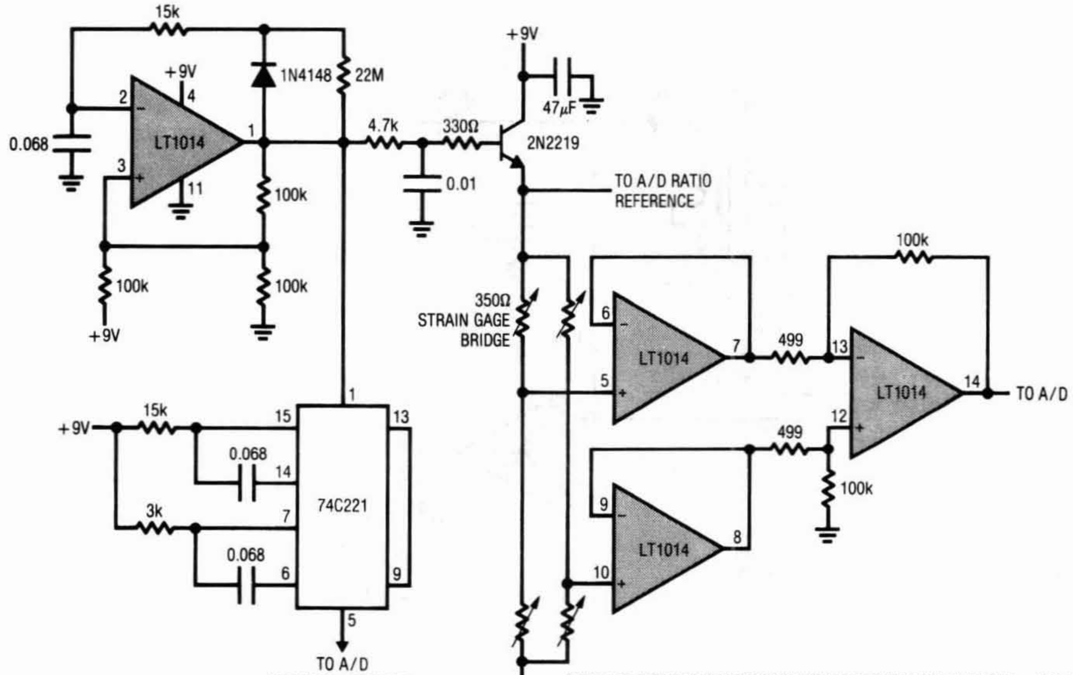

TO
INPUT
CABLE SHIELDS
LT1014
8
9
10
200k*
+5V
†
2
3
1
LT1014
20k
− INPUT
RG (TYP 2k)
200k*
1µF
6
5
7
LT1014
20k
+ INPUT
+5V
10k*
10k*
10k
10k
+5V
13
4
14
LT1014
12
11
OUTPUT
10k*
10k*

*1% FILM RESISTOR. MATCH 10k's 0.05%

GAIN EQUATION: $A = \frac{400{,}000}{RG} + 1.$

†FOR HIGH SOURCE IMPEDANCES, USE 2N2222 AS DIODES.

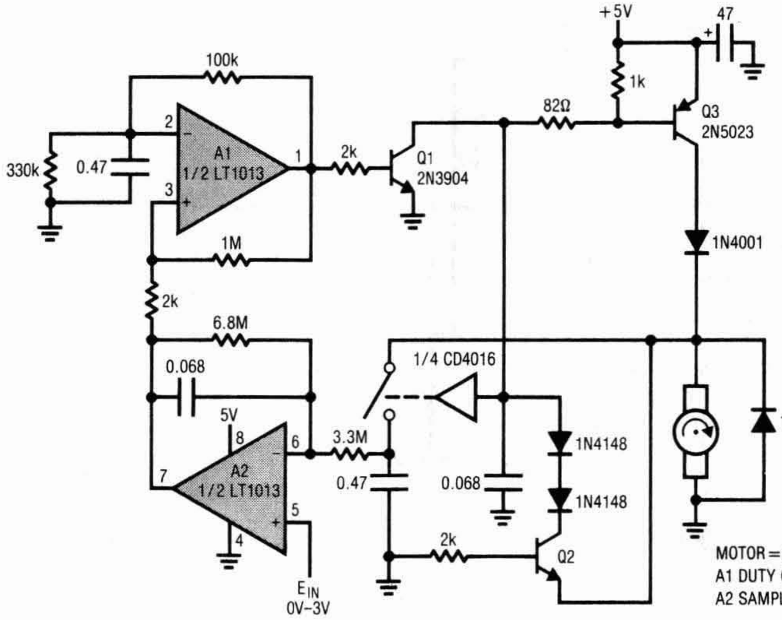
9V Battery Powered Strain Gage Signal Conditioner


15k
+9V
4
2
3
LT1014
1
11
0.068
1N4148
22M
100k
100k
100k
+9V
4.7k
330Ω
0.01
+9V
47µF
2N2219
TO A/D RATIO
REFERENCE
+9V
15k
3k
0.068
0.068
15
14
7
6
1
13
9
5
74C221
TO A/D
CONVERT COMMAND
350Ω
STRAIN GAGE
BRIDGE
6
5
LT1014
7
499
100k
13
12
LT1014
14
TO A/D
499
100k
9
10
LT1014
8

SAMPLED OPERATION GIVES LOW AVERAGE OPERATING CURRENT ≈650µA.
4.7k–0.01µF RC PROTECTS STRAIN BRIDGE FROM LONG TERM DRIFTS DUE TO HIGH ΔV/ΔT STEPS.

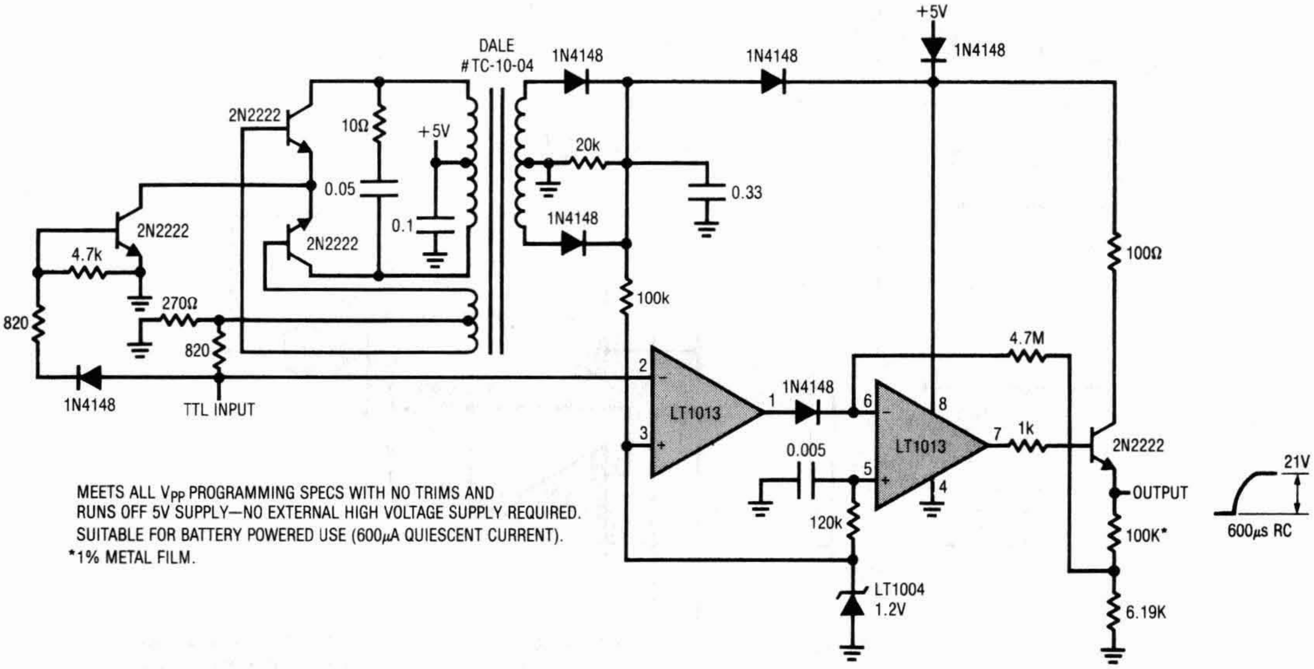
TYPICAL APPLICATIONS

5V Powered Motor Speed Controller No Tachometer Required


+5V
47
100k
1k
82Ω
Q3
2N5023
2
3
1
330k
0.47
A1
1/2 LT1013
2k
Q1
2N3904
1M
1N4001
2k
6.8M
0.068
1/4 CD4016
5V
8
6
3.3M
7
A2
1/2 LT1013
5
4
0.47
0.068
1N4148
1N4148
1N4001
2k
Q2
E_{IN}
0V–3V

MOTOR = CANON – FN30 – R13N1B.
A1 DUTY CYCLE MODULATES MOTOR.
A2 SAMPLES MOTORS BACK EMF.

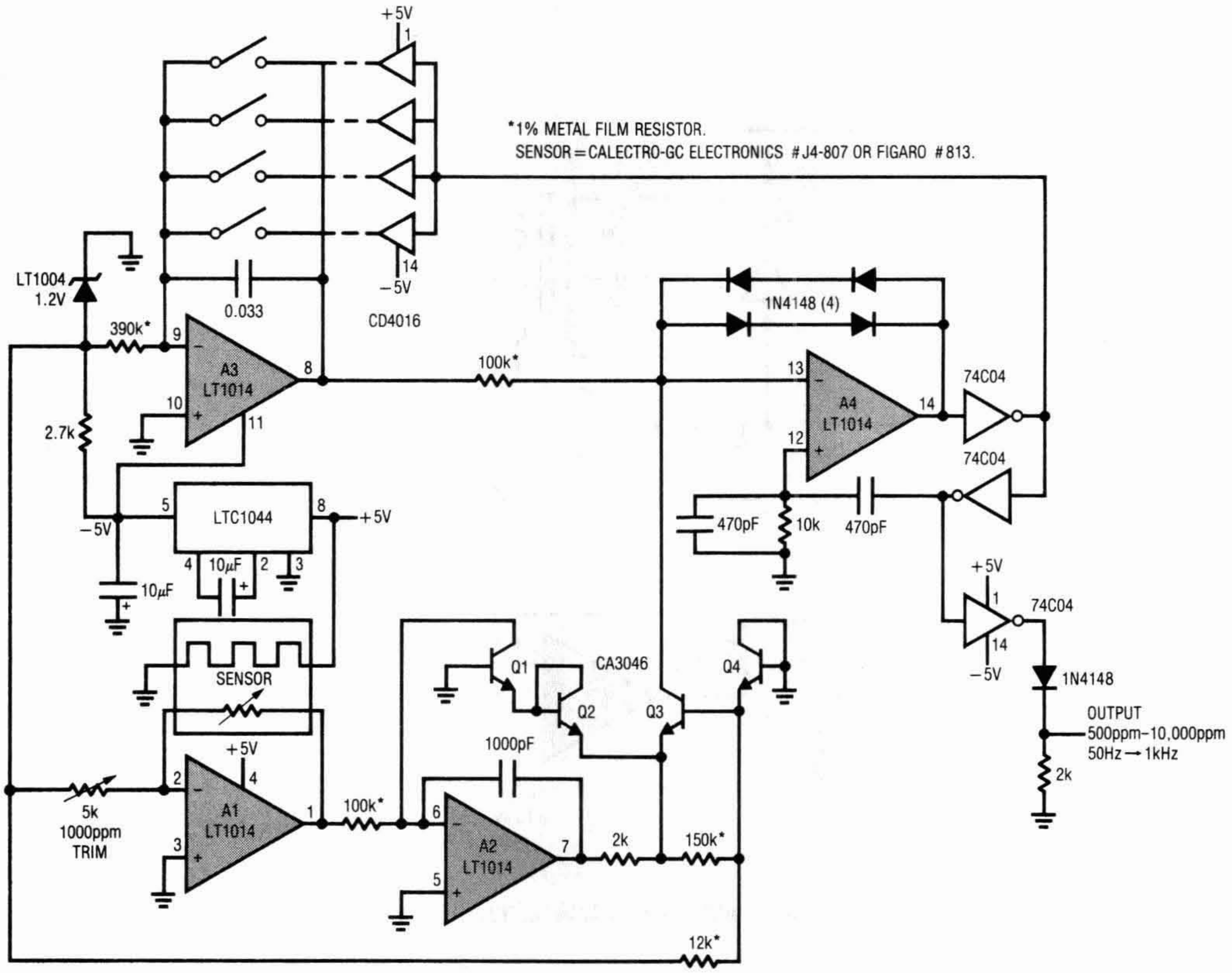
5V Powered EEPROM Pulse Generator


+5V
DALE
#TC-10-04
1N4148
1N4148
1N4148
2N2222
10Ω
+5V
20k
0.05
0.33
0.1
1N4148
2N2222
2N2222
4.7k
270Ω
820
820
100Ω
100k
1N4148
TTL INPUT
4.7M
2
1N4148
LT1013
1
6
8
3
0.005
5
LT1013
7
1k
2N2222
4
OUTPUT
120k
100K*
LT1004
1.2V
6.19K
21V
600µs RC

MEETS ALL V_{PP} PROGRAMMING SPECS WITH NO TRIMS AND RUNS OFF 5V SUPPLY—NO EXTERNAL HIGH VOLTAGE SUPPLY REQUIRED.
SUITABLE FOR BATTERY POWERED USE (600µA QUIESCENT CURRENT).
*1% METAL FILM.

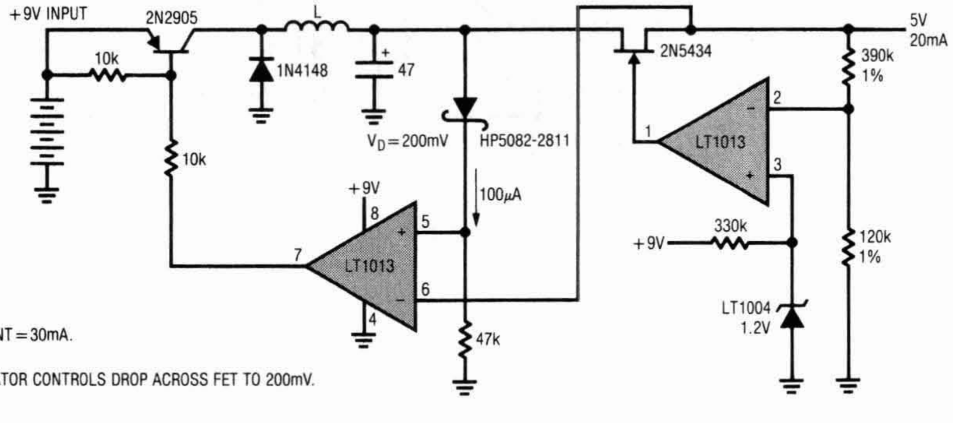
TYPICAL APPLICATIONS

Methane Concentration Detector with Linearized Output


+5V
1
14
−5V
CD4016
LT1004
1.2V
0.033
390k*
9
A3
LT1014
10
11
8
2.7k
100k*
1N4148 (4)
13
A4
LT1014
12
14
74C04
74C04
470pF
10k
470pF
5
LTC1044
8
+5V
−5V
4
10μF
2
3
10μF
SENSOR
+5V
1
74C04
14
−5V
1N4148
OUTPUT
500ppm–10,000ppm
50Hz → 1kHz
2k
CA3046
Q1
Q2
Q3
Q4
1000pF
+5V
2
4
A1
LT1014
3
1
100k*
6
A2
LT1014
5
7
2k
150k*
5k
1000ppm
TRIM
12k*

*1% METAL FILM RESISTOR.
SENSOR = CALECTRO-GC ELECTRONICS #J4-807 OR FIGARO #813.

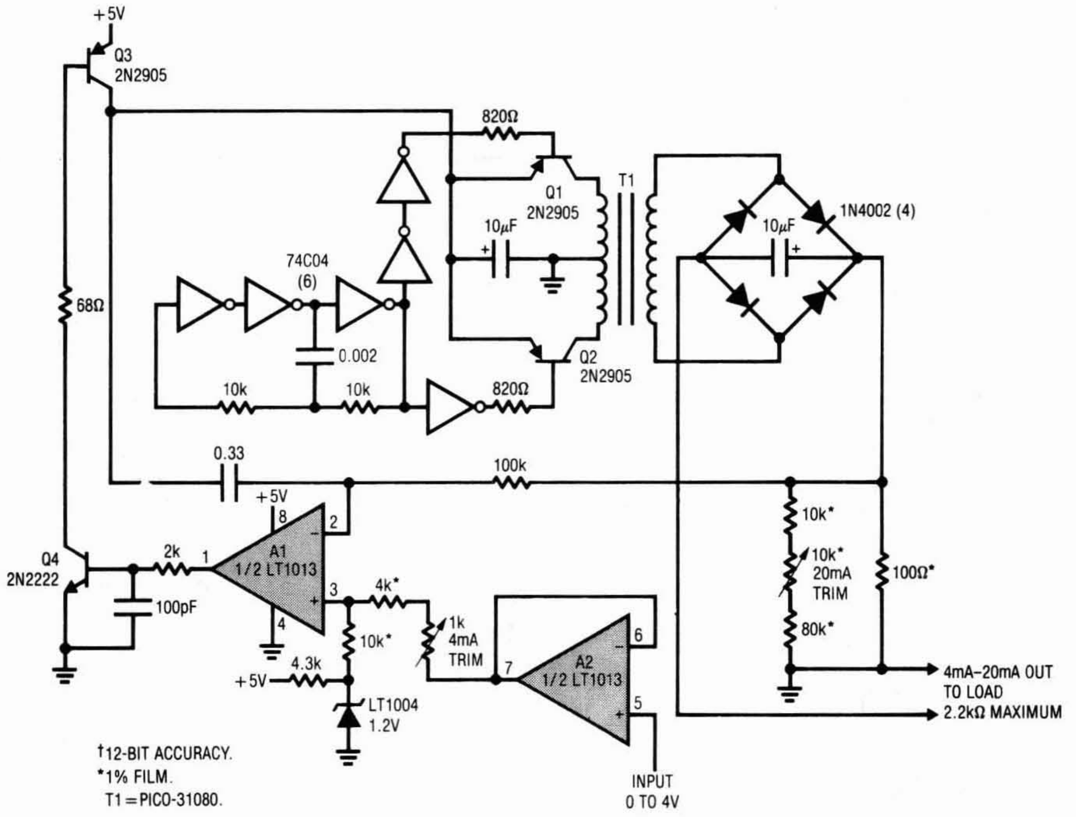
Low Power 9V to 5V Converter


+9V INPUT
2N2905
10k
L
1N4148
47
10k
VD = 200mV
HP5082-2811
100μA
+9V
8
5
7
LT1013
6
4
47k
2N5434
5V
20mA
390k
1%
2
1
LT1013
3
330k
+9V
120k
1%
LT1004
1.2V

L = DALE TE-3/Q3/TA.
SHORT CIRCUIT CURRENT = 30mA.
≈75% EFFICIENCY.
SWITCHING PREREGULATOR CONTROLS DROP ACROSS FET TO 200mV.

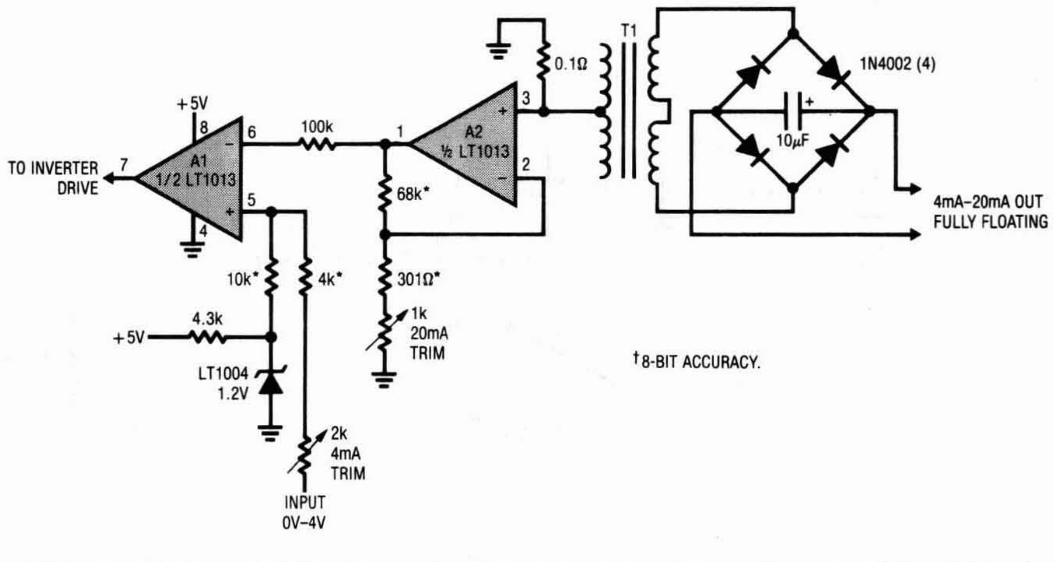
TYPICAL APPLICATIONS

5V Powered 4mA-20mA Current Loop Transmitter†


+5V
Q3
2N2905
820Ω
Q1
2N2905
T1
1N4002 (4)
10μF
10μF
74C04
(6)
68Ω
0.002
Q2
2N2905
10k
10k
820Ω
0.33
100k
+5V
8
2
Q4
2N2222
2k
1
A1
1/2 LT1013
3
4k*
100pF
4
1k
4mA
TRIM
10k*
4.3k
+5V
LT1004
1.2V
10k*
10k*
20mA
TRIM
100Ω*
80k*
6
A2
1/2 LT1013
7
5
4mA-20mA OUT
TO LOAD
2.2kΩ MAXIMUM
INPUT
0 TO 4V

†12-BIT ACCURACY.
*1% FILM.
T1 = PICO-31080.

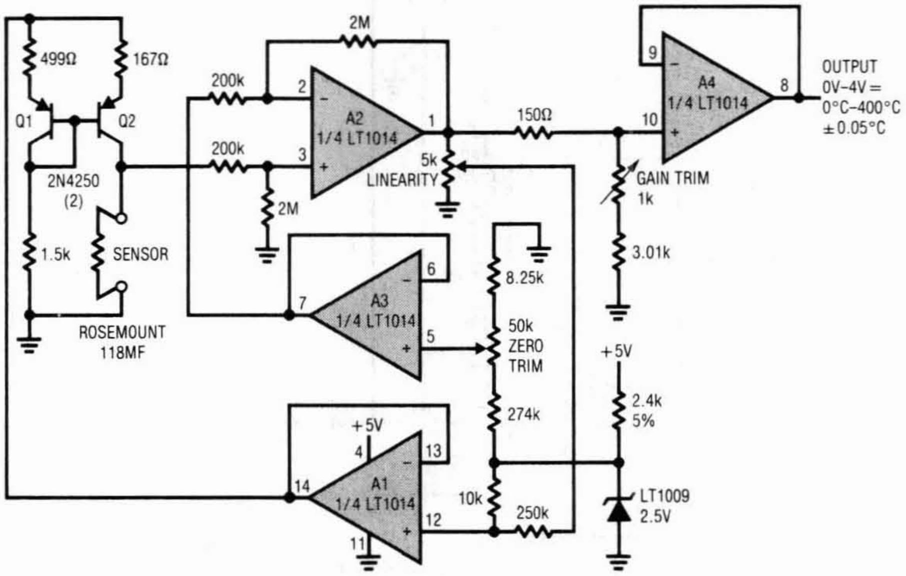
Fully Floating Modification to 4mA-20mA Current Loop†


T1
0.1Ω
1N4002 (4)
+5V
8
6
100k
1
3
A2
½ LT1013
2
TO INVERTER
DRIVE
7
A1
1/2 LT1013
5
4
10μF
68k*
4mA-20mA OUT
FULLY FLOATING
10k*
4k*
301Ω*
4.3k
+5V
1k
20mA
TRIM
LT1004
1.2V
2k
4mA
TRIM
INPUT
0V-4V

†8-BIT ACCURACY.

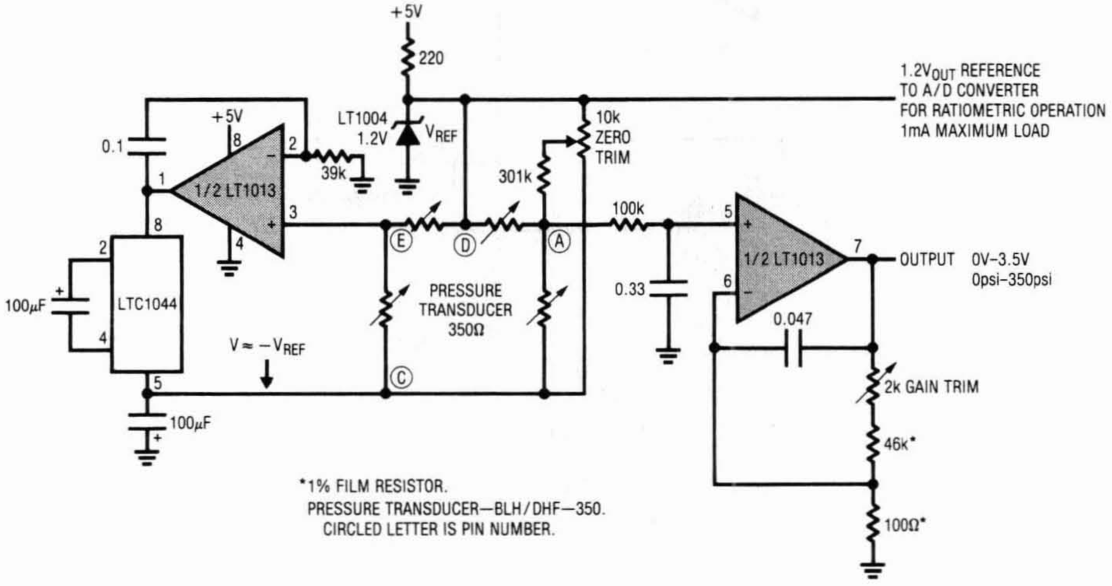
TYPICAL APPLICATIONS

5V Powered, Linearized Platinum RTD Signal Conditioner


2M
499Ω
167Ω
200k
2
A2
1/4 LT1014
1
Q1
Q2
200k
3
5k
LINEARITY
150Ω
2N4250
(2)
2M
1.5k
SENSOR
ROSEMOUNT
118MF
9
A4
1/4 LT1014
8
10
OUTPUT
0V–4V =
0°C–400°C
±0.05°C
GAIN TRIM
1k
3.01k
6
A3
1/4 LT1014
7
5
8.25k
50k
ZERO
TRIM
274k
+5V
2.4k
5%
+5V
4
13
14
A1
1/4 LT1014
12
11
10k
250k
LT1009
2.5V

ALL RESISTORS ARE TRW-MAR-6 METAL FILM.
RATIO MATCH 2M–200K ± 0.01%.
TRIM SEQUENCE:
 SET SENSOR TO 0° VALUE.
 ADJUST ZERO FOR 0V OUT.
 SET SENSOR TO 100°C VALUE.
 ADJUST GAIN FOR 1.000V OUT.
 SET SENSOR TO 400°C.
 ADJUST LINEARITY FOR 4.000V OUT, REPEAT AS REQUIRED.

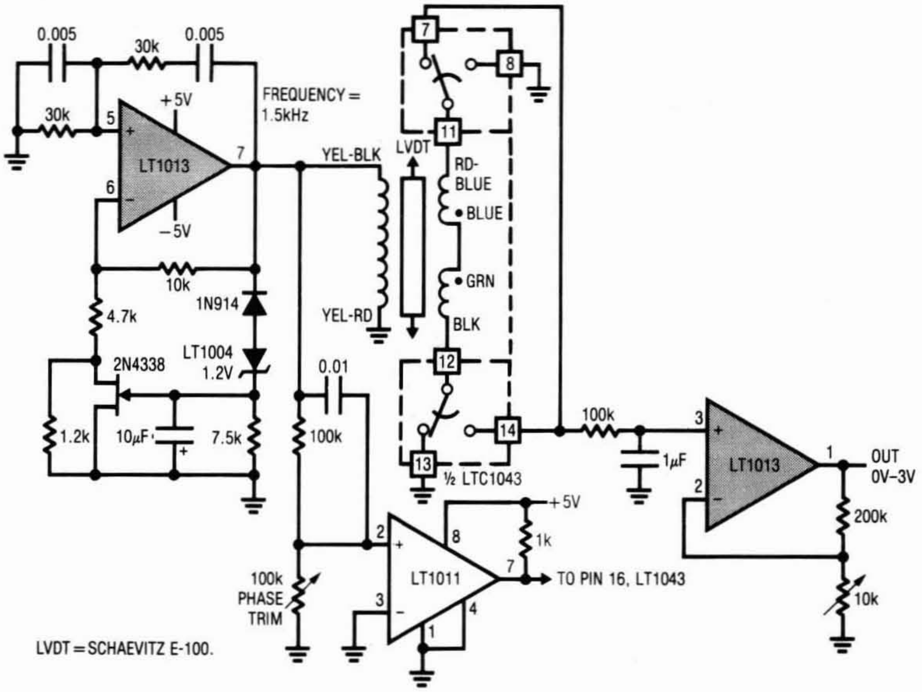
Strain Gage Bridge Signal Conditioner


+5V
220
1.2V$_{OUT}$ REFERENCE
TO A/D CONVERTER
FOR RATIOMETRIC OPERATION
1mA MAXIMUM LOAD
0.1
+5V
8
2
LT1004
1.2V
V$_{REF}$
10k
ZERO
TRIM
1/2 LT1013
1
3
39k
301k
4
8
100k
5
7
E
D
A
2
LTC1044
4
100μF
PRESSURE
TRANSDUCER
350Ω
0.33
1/2 LT1013
6
OUTPUT 0V–3.5V
0psi–350psi
0.047
V ≈ −V$_{REF}$
C
5
100μF
2k GAIN TRIM
46k*
100Ω*

*1% FILM RESISTOR.
PRESSURE TRANSDUCER—BLH/DHF—350.
CIRCLED LETTER IS PIN NUMBER.

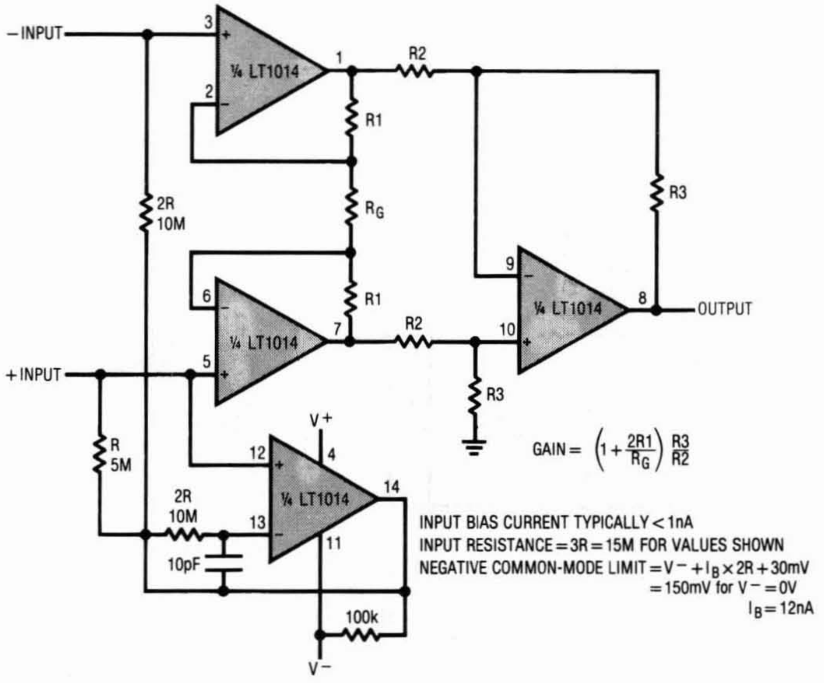
TYPICAL APPLICATIONS

LVDT Signal Conditioner


0.005
30k
0.005
30k
+5V
−5V
5
6
7
LT1013
FREQUENCY = 1.5kHz
10k
1N914
4.7k
2N4338
LT1004 1.2V
1.2k
10μF
7.5k
YEL-BLK
YEL-RD
LVDT
RD-BLUE
BLUE
GRN
BLK
7
8
11
12
13
14
½ LTC1043
0.01
100k
100k
PHASE TRIM
LT1011
2
3
8
7
4
1
+5V
1k
TO PIN 16, LT1043
100k
1μF
LT1013
3
2
1
OUT 0V–3V
200k
10k

LVDT = SCHAEVITZ E-100.

Triple Op Amp Instrumentation Amplifier with Bias Current Cancellation


−INPUT
+INPUT
¼ LT1014
¼ LT1014
¼ LT1014
¼ LT1014
3
2
1
6
5
7
9
10
8
12
13
4
11
14
R2
R2
R1
R1
R$_G$
R3
R3
2R 10M
R 5M
2R 10M
10pF
100k
V+
V−
OUTPUT

$$\text{GAIN} = \left(1 + \frac{2R1}{R_G}\right)\frac{R3}{R2}$$

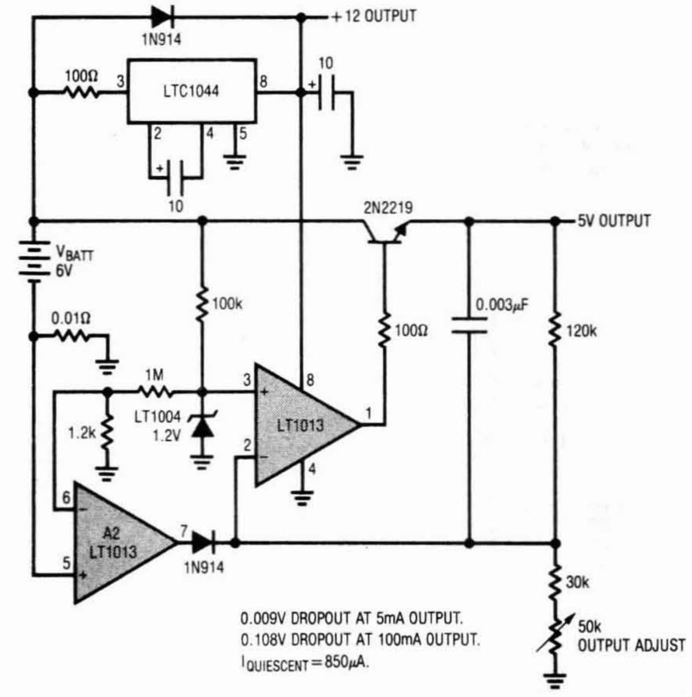
INPUT BIAS CURRENT TYPICALLY < 1nA

INPUT RESISTANCE = 3R = 15M FOR VALUES SHOWN

NEGATIVE COMMON-MODE LIMIT = $V^- + I_B \times 2R + 30mV$
= 150mV for $V^- = 0V$
$I_B = 12nA$

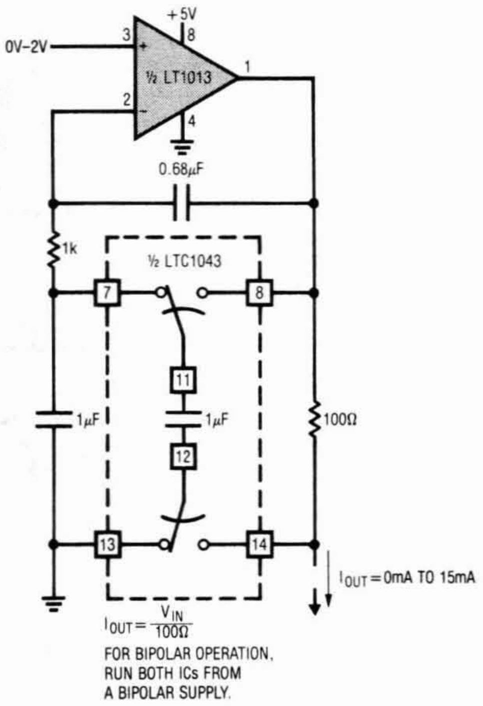
TYPICAL APPLICATIONS

Low Dropout Regulator for 6V Battery


1N914
+12 OUTPUT
100Ω
3
LTC1044
8
10
2
4
5
10
2N2219
5V OUTPUT
V_{BATT} 6V
100k
100Ω
0.003μF
120k
0.01Ω
1M
3
8
LT1004 1.2V
1.2k
LT1013
1
2
4
6
A2 LT1013
7
5
1N914
30k
50k OUTPUT ADJUST

0.009V DROPOUT AT 5mA OUTPUT.
0.108V DROPOUT AT 100mA OUTPUT.
$I_{QUIESCENT} = 850\mu A$.

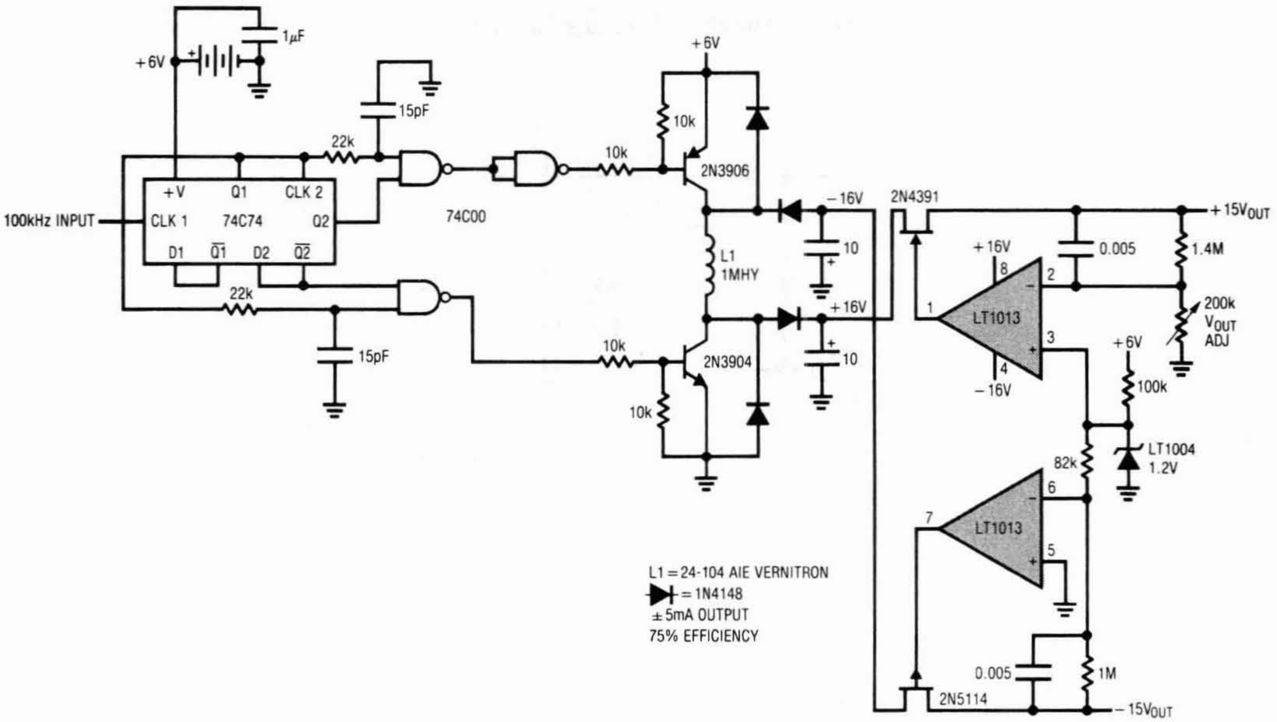
Voltage Controlled Current Source with Ground Referred Input and Output


+5V
0V–2V
3
8
½ LT1013
1
2
4
0.68μF
1k
½ LTC1043
7
8
11
1μF
1μF
12
100Ω
13
14
I_{OUT} = 0mA TO 15mA

$I_{OUT} = \frac{V_{IN}}{100\Omega}$

FOR BIPOLAR OPERATION,
RUN BOTH ICs FROM
A BIPOLAR SUPPLY.

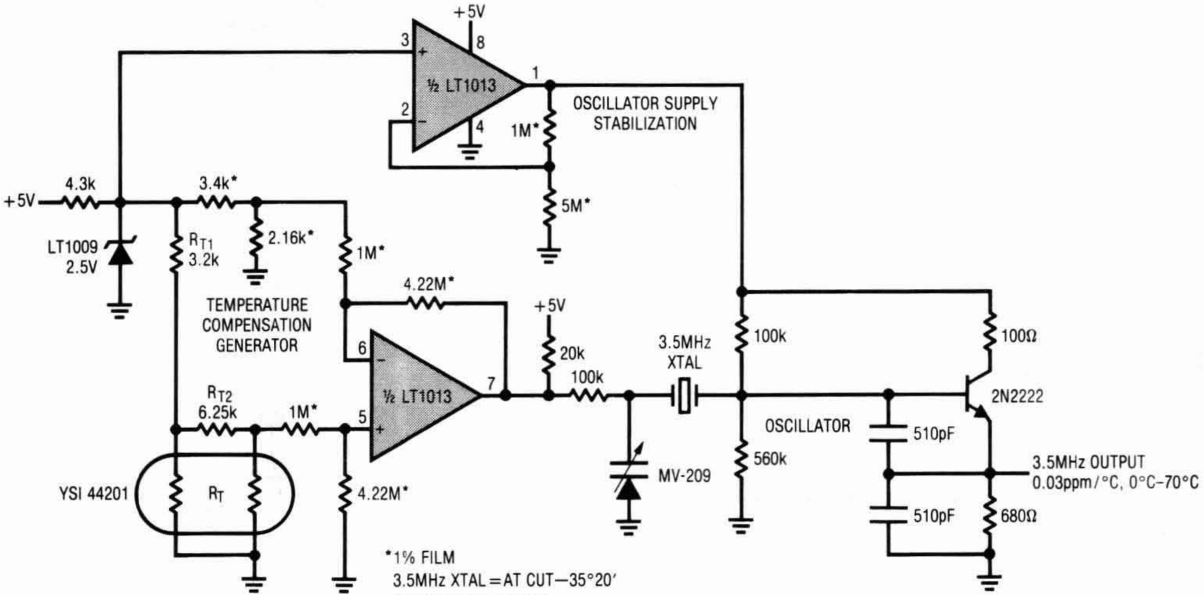
6V to ±15V Regulating Converter


1μF
+6V
15pF
22k
+V
Q1
CLK 2
100kHz INPUT
CLK 1
74C74
Q2
D1
$\overline{Q1}$
D2
$\overline{Q2}$
22k
15pF
74C00
+6V
10k
10k
2N3906
−16V
L1 1MHY
10
+16V
10
10k
2N3904
10k
2N4391
+15V_{OUT}
+16V
0.005
1.4M
8
2
1
LT1013
3
4
−16V
200k V_{OUT} ADJ
+6V
100k
LT1004 1.2V
82k
6
7
LT1013
5
0.005
1M
2N5114
−15V_{OUT}

L1 = 24-104 AIE VERNITRON
▶| = 1N4148
±5mA OUTPUT
75% EFFICIENCY

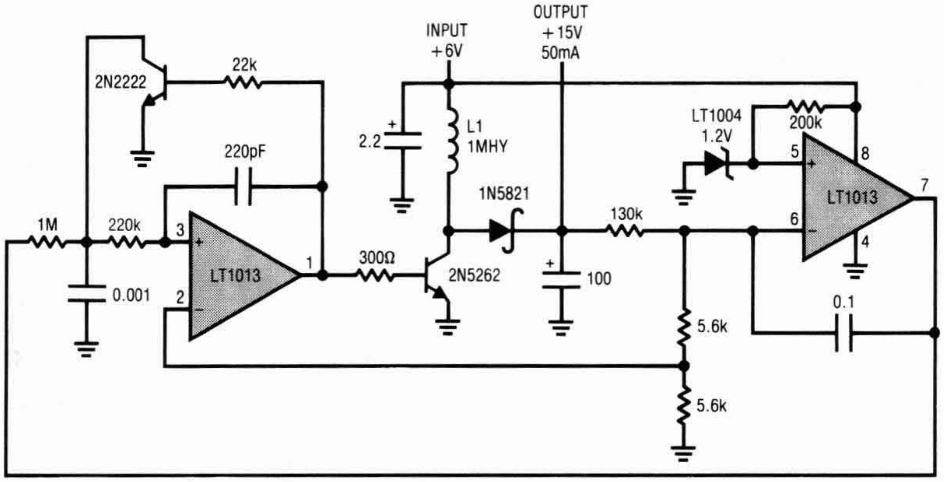
TYPICAL APPLICATIONS

Low Power, 5V Driven, Temperature Compensated Crystal Oscillator (TXCO)†


+5V
3
8
½ LT1013
1
2
4
1M*
OSCILLATOR SUPPLY
STABILIZATION
5M*
+5V
4.3k
3.4k*
LT1009
2.5V
R_{T1}
3.2k
2.16k*
1M*
4.22M*
TEMPERATURE
COMPENSATION
GENERATOR
+5V
6
½ LT1013
7
5
20k
100k
3.5MHz
XTAL
100k
100Ω
2N2222
R_{T2}
6.25k
1M*
OSCILLATOR
510pF
YSI 44201
R_T
4.22M*
MV-209
560k
3.5MHz OUTPUT
0.03ppm/°C, 0°C–70°C
510pF
680Ω

*1% FILM
3.5MHz XTAL = AT CUT—35°20′
MOUNT R_T NEAR XTAL
3mA POWER DRAIN
†THERMISTOR-AMPLIFIER-VARACTOR NETWORK GENERATES A TEMPERATURE COEFFICIENT OPPOSITE THE CRYSTAL TO MINIMIZE OVERALL OSCILLATOR DRIFT

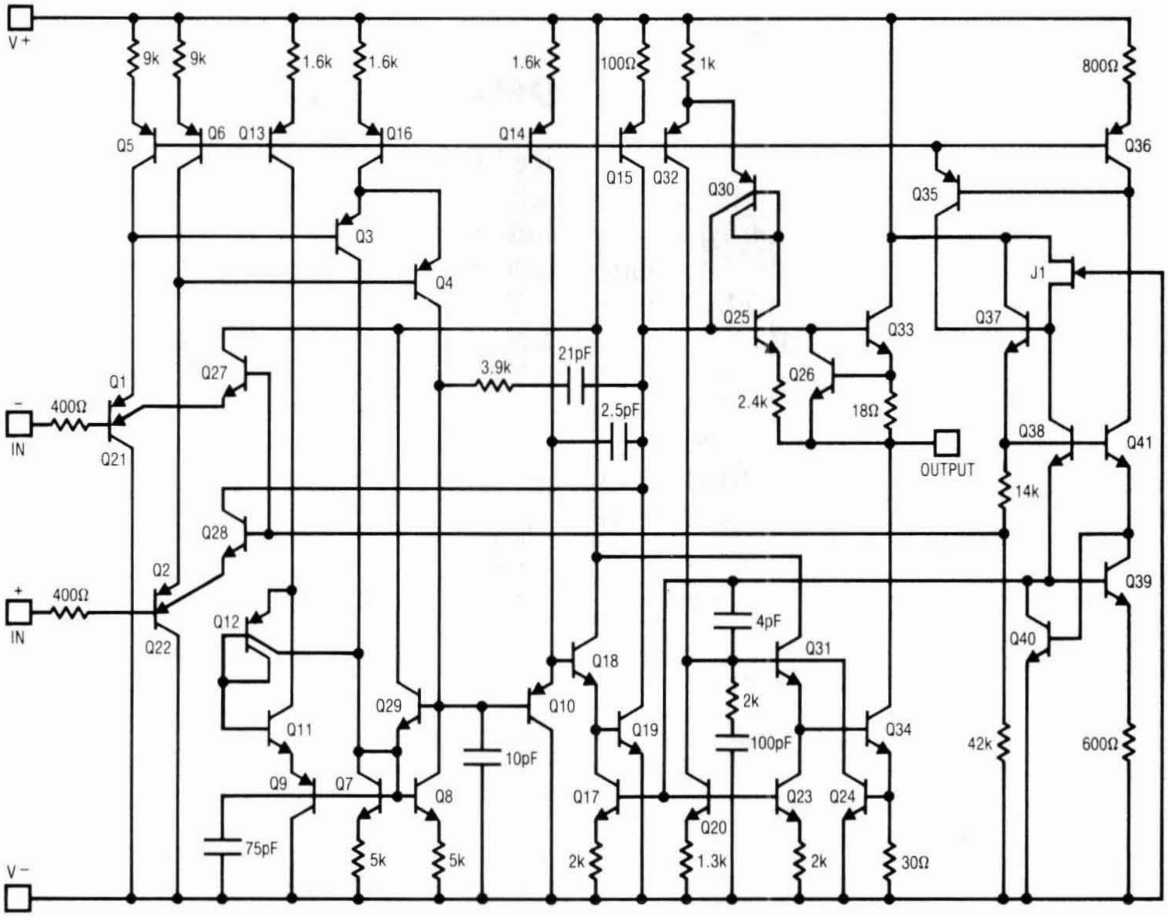
Step-Up Switching Regulator for 6V Battery


OUTPUT
+15V
50mA
INPUT
+6V
2N2222
22k
2.2
L1
1MHY
LT1004
1.2V
200k
5
8
220pF
1N5821
LT1013
7
1M
220k
3
130k
6
LT1013
1
300Ω
2N5262
100
4
0.001
2
0.1
5.6k
5.6k

L1 = AIE—VERNITRON 24-104
78% EFFICIENCY

SCHEMATIC DIAGRAM

½ LT1013, ¼ LT1014


V+
9k
9k
1.6k
1.6k
1.6k
100Ω
1k
800Ω
Q5
Q6
Q13
Q16
Q14
Q15
Q32
Q30
Q36
Q35
Q3
Q4
J1
Q25
Q33
Q37
Q27
Q1
3.9k
21pF
Q26
2.4k
18Ω
2.5pF
−
400Ω
IN
Q21
OUTPUT
Q38
Q41
14k
Q28
Q2
+
400Ω
IN
Q22
Q12
4pF
Q31
Q40
Q39
Q18
2k
Q29
Q10
Q19
100pF
Q34
42k
600Ω
Q11
10pF
Q9
Q7
Q8
Q17
Q23
Q24
Q20
75pF
5k
5k
2k
1.3k
2k
30Ω
V−

LT1028CS8

Ultra Low Noise Precision High Speed Op Amp

FEATURES

■ Available in 8-Pin SO Package	
■ Voltage Noise	1.2nV/√Hz Max at 1kHz
	0.9nV/√Hz Typ at 1kHz
	1.0nV/√Hz Typ at 10Hz
	$35nV_{P-P}$ Typ, 0.1Hz to 10Hz
■ Voltage and Current Noise 100% Tested	
■ Gain-Bandwidth Product	50MHz Min
■ Slew Rate	11V/µs Min
■ Offset Voltage	80µV Max
■ Voltage Gain	5 Million Min
■ Drift with Temperature	1µV/°C Max

APPLICATIONS

- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

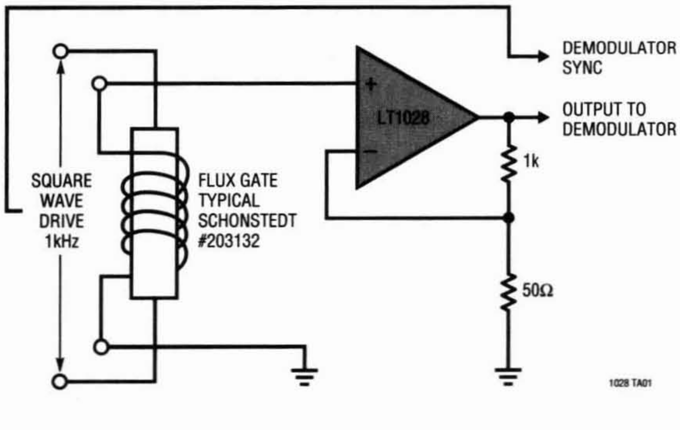
DESCRIPTION

The LT1028 achieves a new standard of excellence in noise performance with 0.9nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz), distortion-free output, and true precision parameters (0.2µV/°C drift, 20µV offset voltage, 30 million voltage gain). Although the LT1028 input stage operates at nearly 1mA of collector currents to achieve low voltage noise, input bias current is only 30nA.

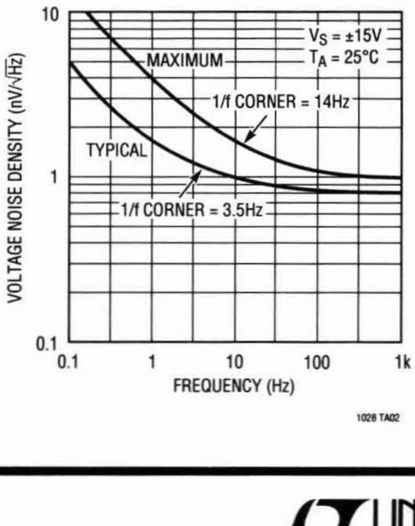
The LT1028's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028's contribution to total system noise will be negligible.

TYPICAL APPLICATION

Flux Gate Amplifier



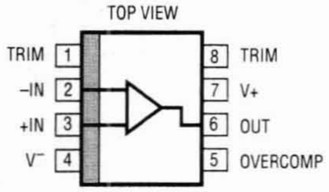
Flux Gate Amplifier



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Differential Input Current (Note 4)	±25mA
Input Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Operating Temperature Range	−40°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SOIC

ORDER PART NUMBER
LT1028CS8
PART MARKING
1028

ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)		20	80	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Note 2)		0.3		μV/Mo
I_{OS}	Input Offset Current	$V_{CM} = 0V$		18	100	nA
I_B	Input Bias Current	$V_{CM} = 0V$		±30	±180	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 3)		35	90	nV_{P-P}
	Input Noise Voltage Density	$f_O = 10Hz$ (Note 3) $f_O = 1000Hz$, 100% Tested		1.0 0.9	1.9 1.2	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_O = 10Hz$ (Note 3 and 5) $f_O = 1000Hz$, 100% Tested		4.7 1.0	12.0 1.8	$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
R_{IN}	Input Resistance Common Mode Differential Mode			 300 20		 MΩ kΩ
C_{IN}	Input Capacitance			5		pF
	Input Voltage Range		±11.0	±12.2		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11V$	110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	110	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_O = \pm12V$ $R_L \geq 1k\Omega$, $V_O = \pm10V$ $R_L \geq 600\Omega$, $V_O = \pm10V$	5.0 3.5 2.0	30.0 20.0 15.0		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±12.0 ±10.5	±13.0 ±12.2		V V
SR	Slew Rate	$A_{VCL} = -1$	11	15		V/μs
GBW	Gain-Bandwidth Product	$f_O = 20kHz$ (Note 6)	50	75		MHz
Z_O	Open Loop Output Impedance	$V_O = 0$, $I_O = 0$		80		Ω
I_S	Supply Current			7.6	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		30	125	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 7)	●		0.2	1.0	μV/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	●		22	130	nA
I_B	Input Bias Current	V_{CM} = 0V	●		±40	±240	nA
	Input Voltage Range		●	±10.5	±12.0		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10.5V	●	106	124		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	●	107	132		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_O = ±10V $R_L \ge 1k\Omega$, V_O = ±10V	● ●	3.0 2.5	25.0 18.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$ $R_L \ge 600\Omega$	● ●	±11.5 ±9.0	±12.7 ±10.5		V V
I_S	Supply Current		●		8.2	11.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 8)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		35	150	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		0.25	1.0	μV/°C
I_{OS}	Input Offset Current	V_{CM} = 0V	●		28	180	nA
I_B	Input Bias Current	V_{CM} = 0V	●		±45	±300	nA
	Input Voltage Range		●	±10.4	±11.8		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±10.4V	●	102	123		dB
PSRR	Power Supply Rejection Ratio	V_S = ±4.5V to ±18V	●	106	131		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, V_O = ±10V $R_L \ge 1k\Omega$, V_O = ±10V	● ●	2.5 2.0	20.0 14.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±11.0	±12.5		V
I_S	Supply Current		●		8.7	12.5	mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at T_A = 25°C, offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

Note 2: Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5μV.

Note 3: This parameter is tested on a sample basis only.

Note 4: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

Note 5: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after substracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

Note 7: This parameter is not 100% tested.

Note 8: The LT1028CS8s are not tested and are not quality-assurance-sampled at −40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from 0°C, 25°C, 70°C tests.

LT1057S/LT1057IS
LT1058S/LT1058IS

Dual JFET Input Precision High Speed Op Amp

FEATURES

- 13V/μs Slew Rate 8V/μs Min.
- 5MHz Gain-Bandwidth Product
- Fast Settling Time 1.3μs to 0.02%
- 300μV Offset Voltage (LT1057)
- 5μV/°C V_{OS} Drift
- 60pA Bias Current at 70°C
- Low Voltage Noise 13nV/√Hz at 1kHz
26nV/√Hz at 10Hz

APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample and Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage to Frequency Converters
- Frequency to Voltage Converters

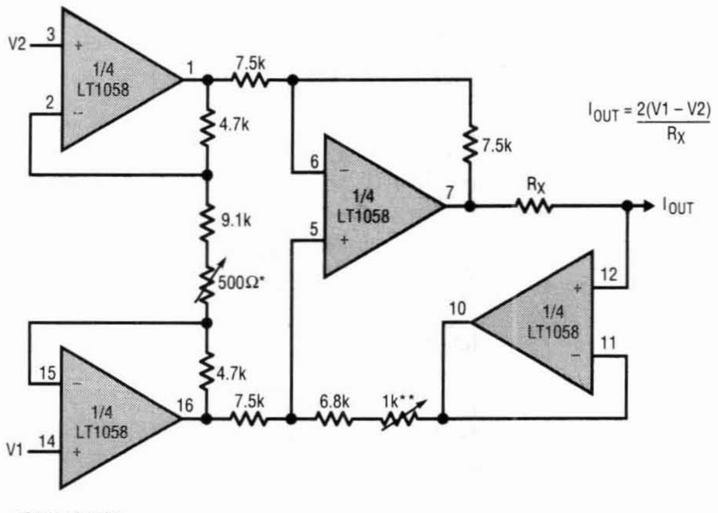
DESCRIPTION

The LT1057 is a matched JFET input dual op amp featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

The LT1058 is the lowest offset quad JFET input operational amplifier. It offers significant accuracy improvement over presently available JFET input quad operational amplifiers. It can replace four single precision JFET input op amps, while saving board space, power dissipation and cost.

For the first time, precision dual and quad JFET op amps are available in a surface mounted package. For extended operating temperatures ($-40°C \le T_A \le 85°C$) the LT1057IS and LT1058IS are offered.

Current Output, High Speed, High Input Impedance Instrumentation Amplifier



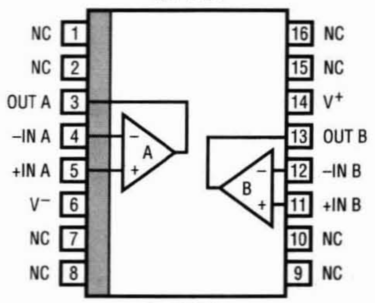
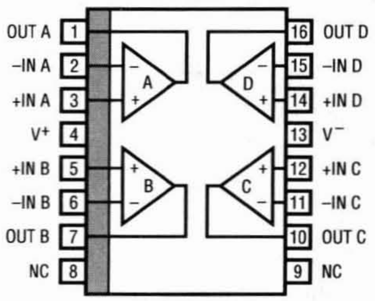
*GAIN ADJUST
**COMMON-MODE REJECTION ADJUST
BANDWIDTH ≈ 2MHz

LT1058S•TA01

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V
Differential Input Voltage	±40V
Input Voltage	±20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1057S, LT1058S	0°C to 70°C
LT1057IS, LT1058IS	−40°C to 85°C
Storage Temperature Range	
All Devices	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
TOP VIEW  NC 1 NC 2 OUT A 3 −IN A 4 +IN A 5 V⁻ 6 NC 7 NC 8 16 NC 15 NC 14 V⁺ 13 OUT B 12 −IN B 11 +IN B 10 NC 9 NC A B − + S PACKAGE 16-LEAD PLASTIC SOL	LT1057S LT1057IS
TOP VIEW  OUT A 1 −IN A 2 +IN A 3 V⁺ 4 +IN B 5 −IN B 6 OUT B 7 NC 8 16 OUT D 15 −IN D 14 +IN D 13 V⁻ 12 +IN C 11 −IN C 10 OUT C 9 NC A B C D − + S PACKAGE 16-LEAD PLASTIC SOL	LT1058S LT1058IS

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		LT1057 LT1058		0.3 0.35	2 2.5	mV
I_{OS}	Input Offset Current	Fully Warmed Up			5	50	pA
I_B	Input Bias Current	Fully Warmed Up			±10	±100	pA
	Input Resistance – Differential				0.4		TΩ
	– Common-Mode	V_{CM} = −11V to +8V V_{CM} = +8V to +11V			0.4 0.05		
	Input Capacitance				4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz	LT1057 LT1058		2.1 2.5		µVp-p
e_n	Input Noise Voltage Density	f_O = 10Hz f_O = 1kHz			26 13		nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz, 1kHz			1.8		fA/√Hz
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V	R_L = 2k R_L = 1k	100 50	300 220		V/mV
	Input Voltage Range			±10.5	14.3 −11.5		V

ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.5V$	LT1057	82	98		dB
			LT1058	80	98		
PSRR	Power Supply Rejection Ratio	$V_S = \pm10V$ to $\pm18V$		86	102		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$		±12	±13		V
SR	Slew Rate			8	13		V/μs
GBW	Gain-Bandwidth Product	f = 1MHz (Note 1)		3	5		MHz
I_S	Supply Current Per Amplifier				1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm10V$			130		dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$, (LT1057S, LT1058S) or $-40°C \le T_A \le 85°C$, (LT1057IS, LT1058IS), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		LT1057	●		0.5	2.5	mV
			LT1058S	●		0.6	3.0	
			LT1058IS	●		0.7	4.0	
	Average Temperature Coefficient of Input Offset Voltage			●		5		μV/°C
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70°C$				20	250	pA
		Warmed Up, $T_A = 85°C$				35	400	
I_B	Input Bias Current	Warmed Up, $T_A = 70°C$				±60	±400	pA
		Warmed Up, $T_A = 85°C$				±100	±700	
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm10V$, $R_L = 2k$	LT1057	●	50	200		V/mV
			LT1058	●	40	200		
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm10.5V$	LT1057	●	80	96		dB
			LT1058	●	78	96		
PSRR	Power Supply Rejection Ratio	$V_S = \pm10V$ to $\pm18V$	LT1057	●	84	100		dB
			LT1058	●	82	100		
V_{OUT}	Output Voltage Swing	$R_L = 2k$		●	±12	±12.8		V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Gain bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

LINEAR TECHNOLOGY

LT1057S8/LT1057IS8

Dual JFET Input Precision High Speed Op Amp

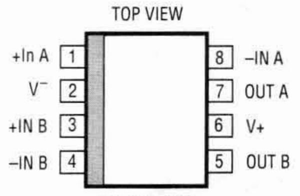
DESCRIPTION

The LT1057 is a matched JFET input dual op amp featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample-and-Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

ORDER PART NUMBER
LT1057S8 LT1057IS8
PART MARKING
1057

PLEASE NOTICE THAT THE LT1057S8 STANDARD SURFACE MOUNT PINOUT DIFFERS FROM THAT OF THE LT1057 STANDARD PLASTIC OR CERAMIC DUAL-IN-LINE PACKAGES.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range

LT1057S8 .... $0°C \leq T_A \leq 70°C$

LT1057IS8 .... $-40°C \leq T_A \leq 85°C$

ELECTRICAL CHARACTERISTICS

$V_S = \pm15V, T_A = 25°C, V_{CM} = 0V$, unless otherwise noted.
For electrical specifications not listed below, refer to the standard LT1057C datasheet with the changes noted on this page.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			220	1200	µV
		$0°C \leq T_A \leq 70°C$		400	1900	µV
		$-40°C \leq T_A \leq 85°C$		500	2300	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 4)	$0°C \leq T_A \leq 70°C$		4.0	16	µV/°C
		$-40°C \leq T_A \leq 85°C$		4.5	16	µV/°C
I_B	Input Bias Current	$-40°C \leq T_A \leq 85°C$		±100	±900	pA
I_{OS}	Input Offset Current	$-40°C \leq T_A \leq 85°C$		35	600	pA

Note 4: Not 100% production tested.

LT1077

Micropower, Single Supply, Precision Op Amp

FEATURES

- 60μA Max Supply Current
- 40μV Max Offset Voltage
- 350pA Max Offset Current
- 0.5μVp-p 0.1Hz to 10Hz Voltage Noise
- 2.5pAp-p 0.1Hz to 10Hz Current Noise
- 0.4μV/°C Offset Voltage Drift
- 250kHz Gain-Bandwidth-Product
- 0.12V/μs Slew Rate
- Single Supply Operation
  - Input Voltage Range Includes Ground
  - Output Swings to Ground while Sinking Current
  - No Pull-Down Resistors are Needed
- Output Sources and Sinks 5mA Load Current

APPLICATIONS

- Replaces OP-07, OP-77, AD707, LT1001, LT1012 at 10 to 60 Times Lower Power
- Battery or Solar Powered Systems
- 4mA to 20mA Current Loops
- Two Terminal Current Source
- Megaohm Source Resistance Difference Amplifier

DESCRIPTION

The LT1077 is a micropower precision operational amplifier optimized for single supply operation at 5V. ±15V specifications are also provided.

Micropower performance of competing devices is achieved at the expense of seriously degrading precision, noise, speed, and output drive specifications. The LT1077 reduces supply current without sacrificing other parameters. The offset voltage achieved is the lowest of any micropower op amp. Offset current, voltage and current noise, slew rate and gain-bandwidth product are all two to ten times better than on previous micropower op amps.

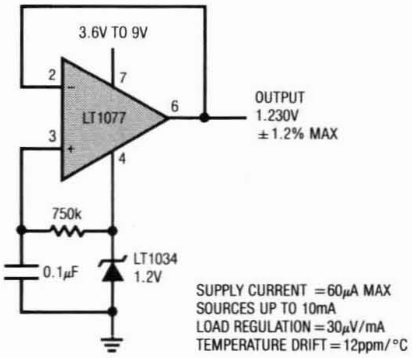
The 1/f corner of the voltage noise spectrum is at 0.7Hz. This results in low frequency (0.1Hz to 10Hz) noise performance which can only be found on devices with an order of magnitude higher supply current.

The LT1077 is completely plug-in compatible (including nulling) with all industry standard precision op amps. Thus, it can replace these precision op amps in many applications without sacrificing performance, yet with significant power savings.

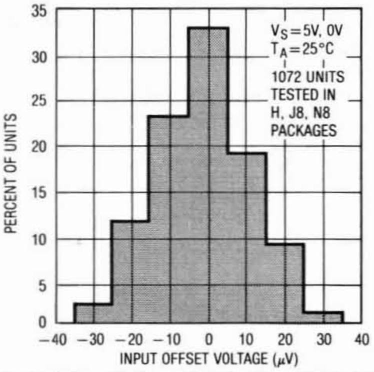
The LT1077 can be operated from one lithium cell or two Ni-Cad batteries. The input range goes below ground. The all-NPN output stage swings to ground while sinking current—no pull-down resistors are needed.

For dual and quad op amps with similar specifications please see the LT1078/LT1079 datasheet.

Self Buffered Micropower Reference



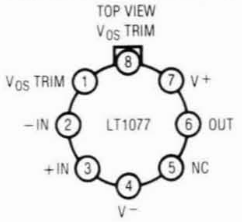
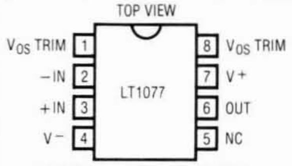
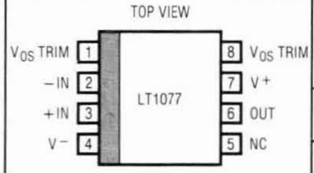
Distribution of Input Offset Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Differential Input Voltage .... ±30V
Input Voltage .... Equal to Positive Supply Voltage
.... 5V Below Negative Supply Voltage
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
LT1077AM/LT1077M .... –55°C to 125°C
LT1077AI/LT1077I .... –40°C to 85°C
LT1077AC/LT1077C/LT1077S8 .... 0°C to 70°C
Storage Temperature Range
All Grades .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW V_{OS} TRIM 8 V_{OS} TRIM 1 7 V+ –IN 2 LT1077 6 OUT +IN 3 5 NC 4 V– H PACKAGE 8-LEAD TO-5 METAL CAN	LT1077AMH LT1077MH LT1077ACH LT1077CH
 TOP VIEW V_{OS} TRIM 1 –IN 2 +IN 3 V– 4 LT1077 8 V_{OS} TRIM 7 V+ 6 OUT 5 NC J PACKAGE 8-LEAD CERAMIC DIP N PACKAGE 8-LEAD PLASTIC DIP	LT1077AMJ8 LT1077AIN8 LT1077MJ8 LT1077IN8 LT1077ACJ8 LT1077ACN8 LT1077CJ8 LT1077CN8
 TOP VIEW V_{OS} TRIM 1 –IN 2 +IN 3 V– 4 LT1077 8 V_{OS} TRIM 7 V+ 6 OUT 5 NC SO PACKAGE 8-LEAD PLASTIC SOIC	LT1077S8
	PART MARKING
	1077

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25°C$, unless noted.

			LT1077AM/AI/AC			LT1077M/I/C/S8			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage			9	40		10	60	μV
		LT1077S8					12	150	μV
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability			0.4			0.4		μV/Mo
I_{OS}	Input Offset Current			0.06	0.35		0.06	0.45	nA
I_B	Input Bias Current			7	9		7	11	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.5	1.1		0.5		μVp-p
	Input Noise Voltage Density	f_o = 10Hz (Note 2)		28	43		28		nV/√Hz
		f_o = 1000Hz (Note 2)		27	35		27		nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		2.5	4.5		2.5		pAp-p
	Input Noise Current Density	f_o = 10Hz (Note 2)		0.065	0.11		0.065		pA/√Hz
		f_o = 1000Hz		0.02			0.02		pA/√Hz
	Input Resistance	(Note 3)							
	Differential Mode		350	700		270	700		MΩ
	Common-Mode			6			6		GΩ
	Input Voltage Range		3.5	3.8		3.5	3.8		V
			0	−0.3		0	−0.3		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.5V	97	106		94	105		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V	102	118		100	117		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.03V to 4V, No Load	300	1000		240	1000		V/mV
		V_O = 0.03V to 3.5V, R_L = 50k	250	1000		200	1000		V/mV

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1077AM/AI/AC MIN	TYP	MAX	LT1077M/I/C/S8 MIN	TYP	MAX	UNITS
	Maximum Output Voltage Swing	Output Low, No Load		3.5	6		3.5	6	mV
		Output Low, 2k to GND		0.7	1.1		0.7	1.1	mV
		Output Low, $I_{SINK} = 100\mu A$		90	130		90	130	mV
		Output High, No Load	4.2	4.4		4.2	4.4		V
		Output High, 2k to GND	3.5	3.9		3.5	3.9		V
SR	Slew Rate	(Note 1)	0.05	0.08		0.05	0.08		V/μs
GBW	Gain Bandwidth Product	$f_o \leq 20kHz$		230			230		kHz
I_S	Supply Current			48	60		48	68	μA
	Offset Adjustment Range	$R_{pot} = 10k$, Wiper to V+	±500	±900		±500	±900		μV
	Minimum Supply Voltage	(Note 4)		2.2	2.3		2.2	2.3	V

ELECTRICAL CHARACTERISTICS

$V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, -55°C \leq T_A \leq 125°C$ for AM/M grades, $-40°C \leq T_A \leq 85°C$ for AI/I grades.

SYMBOL	PARAMETER	CONDITIONS		LT1077AM/AI MIN	TYP	MAX	LT1077M/I MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		50	200		60	260	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.4	1.6		0.5	2.0	μV/°C
I_{OS}	Input Offset Current		●		0.08	0.60		0.08	0.80	nA
I_B	Input Bias Current		●		8	11		8	13	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0.05V$ to 3.2V	●	92	104		88	103		dB
PSRR	Power Supply Rejection Ratio	$V_S = 3.1V$ to 12V	●	98	114		94	113		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to 3.5V, $R_L = 50k$	●	120	600		100	600		V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●		4.5	8		4.5	8	mV
		Output Low, $I_{SINK} = 100\mu A$	●		120	170		120	170	mV
		Output High, No Load	●	3.9	4.2		3.9	4.2		V
		Output High, 2k to GND	●	3.0	3.7		3.0	3.7		V
I_S	Supply Current		●		54	80		54	90	μA

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, 0°C \leq T_A \leq 70°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS		LT1077AC MIN	TYP	MAX	LT1077C/S8 MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		30	110		35	150	μV
		LT1077S8	●					40	280	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.4	1.6		0.5	2.0	μV/°C
		LT1077S8 (Note 5)						0.7	3.0	μV/°C
I_{OS}	Input Offset Current		●		0.07	0.45		0.07	0.60	nA
I_B	Input Bias Current		●		7	10		7	12	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to 3.4V	●	94	105		90	104		dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.6V$ to 12V	●	100	116		97	115		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to 3.5V, $R_L = 50k$	●	180	800		150	800		V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●		4.0	7		4.0	7	mV
		Output Low, $I_{SINK} = 100\mu A$	●		100	150		100	150	mV
		Output High, No Load	●	4.1	4.3		4.1	4.3		V
		Output High, 2k to GND	●	3.3	3.8		3.3	3.8		V
I_S	Supply Current		●		52	70		52	80	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1077AM/AI/AC MIN	LT1077AM/AI/AC TYP	LT1077AM/AI/AC MAX	LT1077M/I/C/S8 MIN	LT1077M/I/C/S8 TYP	LT1077M/I/C/S8 MAX	UNITS
V_{OS}	Input Offset Voltage			20	150		25	200	µV
		LT1077S8					30	300	µV
I_{OS}	Input Offset Current			0.06	0.35		0.06	0.45	nA
I_B	Input Bias Current			7	9		7	11	nA
	Input Voltage Range		13.5 – 15.0	13.8 – 15.3		13.5 – 15.0	13.8 – 15.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} + 13.5V, – 15V	100	109		97	108		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ± 18V	106	122		103	120		dB
A_{VOL}	Large Signal Voltage Gain	V_O = ± 10V, R_L = 50k	1000	8000		800	8000		V/mV
		V_O = ± 10V, R_L = 2k	400	1500		300	1500		V/mV
V_{OUT}	Maximum Output Voltage Swing	R_L = 50k	± 13.0	± 14.0		± 13.0	± 14.0		V
		R_L = 2k	± 11.0	± 13.2		± 11.0	± 13.2		V
SR	Slew Rate		0.07	0.12		0.07	0.12		V/µs
I_S	Supply Current			56	75		56	85	µA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $-55°C \le T_A \le 125°C$ for AM/M grades, $-40°C \le T_A \le 85°C$ for AI/I grades.

SYMBOL	PARAMETER	CONDITIONS		LT1077AM/AI MIN	LT1077AM/AI TYP	LT1077AM/AI MAX	LT1077M/I MIN	LT1077M/I TYP	LT1077M/I MAX	UNITS
V_{OS}	Input Offset Voltage		●		60	330		75	450	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.4	1.8		0.5	2.5	µV/°C
I_{OS}	Input Offset Current		●		0.08	0.60		0.08	0.80	nA
I_B	Input Bias Current		●		8	11		8	13	nA
A_{VOL}	Large Signal Voltage Gain	V_O = ± 10V, R_L = 5k	●	300	1000		250	1000		V/mV
CMRR	Common-Mode Rejection Ratio	V_{CM} = + 13V, – 14.9V	●	94	107		90	106		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ± 18V	●	100	118		97	116		dB
	Maximum Output Voltage Swing	R_L = 5k	●	± 11.0	± 13.5		± 11.0	± 13.5		V
I_S	Supply Current		●		60	95		60	105	µA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS		LT1077AC MIN	LT1077AC TYP	LT1077AC MAX	LT1077C/S8 MIN	LT1077C/S8 TYP	LT1077C/S8 MAX	UNITS
V_{OS}	Input Offset Voltage		●		40	230		50	320	µV
		LT1077S8	●					65	450	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.4	1.8		0.5	2.5	µV/°C
		LT1077S8 (Note 5)						0.8	3.5	µV/°C
I_{OS}	Input Offset Current		●		0.07	0.45		0.07	0.60	nA
I_B	Input Bias Current		●		7	10		7	12	nA
A_{VOL}	Large Signal Voltage Gain	V_O = ± 10V, R_L = 5k	●	500	2000		400	2000		V/mV
CMRR	Common-Mode Rejection Ratio	V_{CM} = 13V, – 15V	●	97	108		94	107		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ± 18V	●	103	120		100	118		dB
	Maximum Output Voltage Swing	R_L = 5k	●	± 11.0	± 13.6		± 11.0	± 13.6		V
I_S	Supply Current		●		59	85		59	95	µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Slew rate at 5V, 0V is guaranteed by inference from the slew rate measurement at ± 15V.

Note 2: This parameter is tested on a sample basis only. All noise parameters are tested with V_S = ± 2.5V, V_O = 0V.

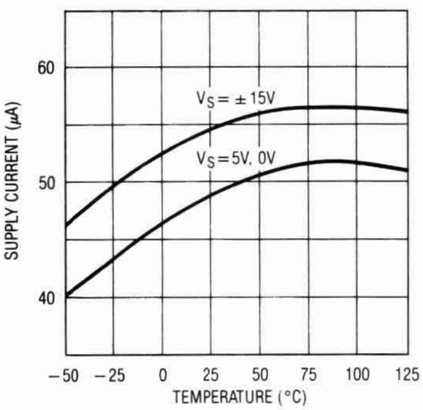
Note 3: This parameter is guaranteed by design and is not tested.

Note 4: Power supply rejection ratio is measured at the minimum supply voltage. The op amps actually work at 1.8V supply but with a typical offset skew of – 300µV.

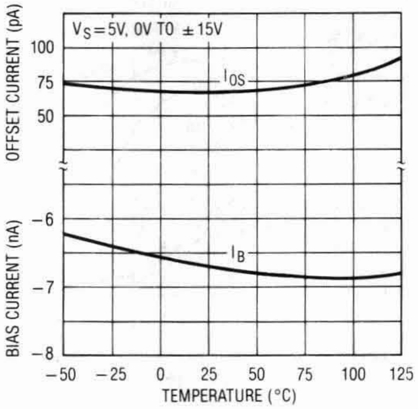
Note 5: This parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

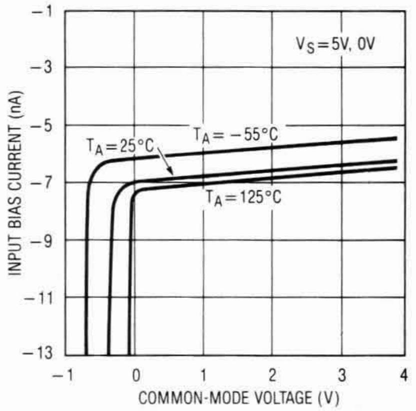
Supply Current vs Temperature



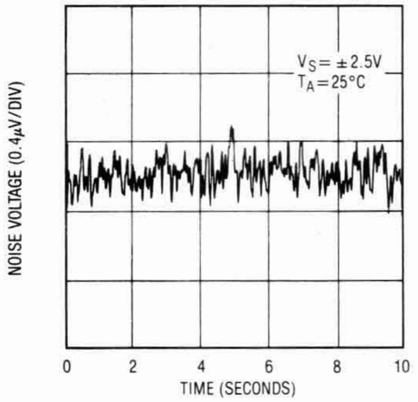
Input Bias and Offset Currents vs Temperature



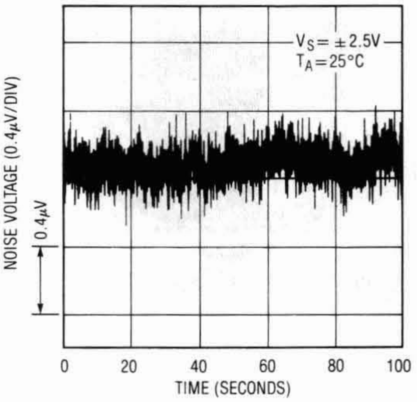
Input Bias Current vs Common-Mode Voltage



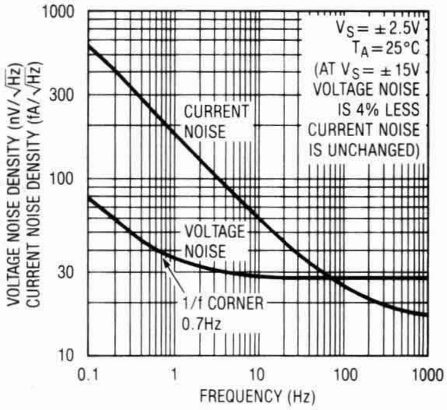
0.1Hz to 10Hz Noise



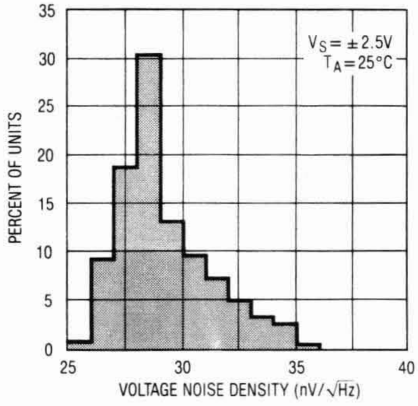
0.01Hz to 10Hz Noise



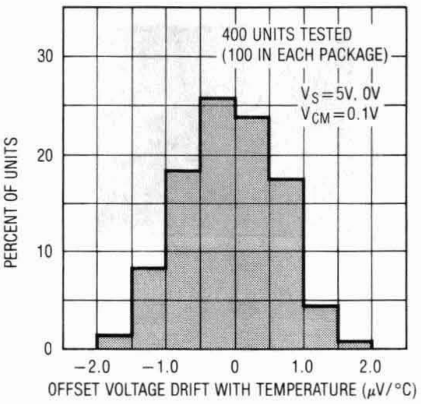
Noise Spectrum



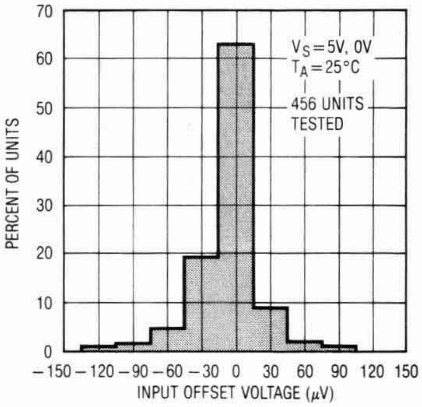
10Hz Voltage Noise Distribution



Distribution of Offset Voltage Drift with Temperature (In All Packages)

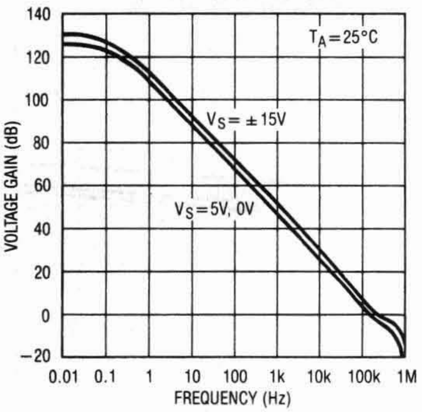


Distribution of Input Offset Voltage in Small Outline (S8) Package

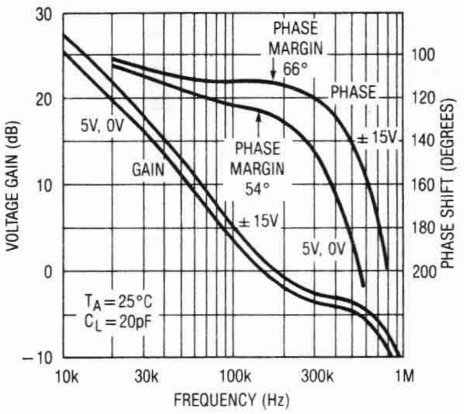


TYPICAL PERFORMANCE CHARACTERISTICS

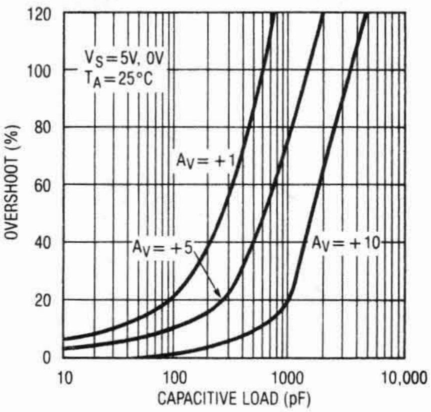
Voltage Gain vs Frequency



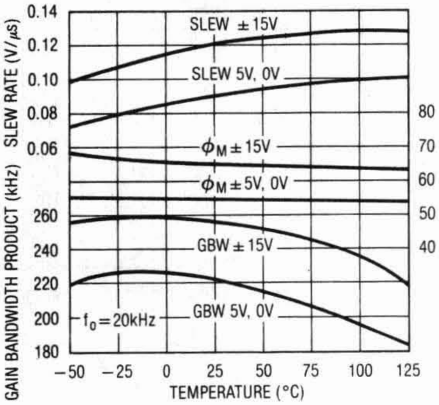
Gain, Phase vs Frequency



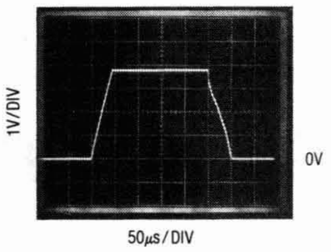
Capacitive Load Handling



Slew Rate, Gain Bandwidth Product and Phase Margin vs Temperature

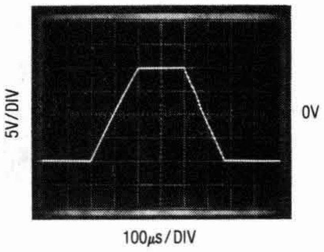


Large Signal Transient Response $V_S = 5V, 0V$



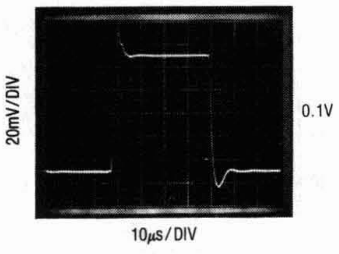
INPUT PULSE 0V TO 3.8V, $A_V = +1$, NO LOAD

Large Signal Transient Response $V_S = ±15V$



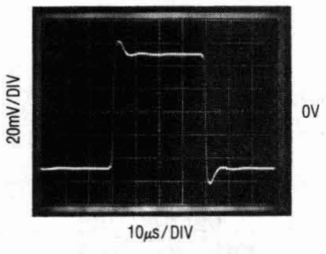
$A_V = +1$, NO LOAD

Small Signal Transient Response $V_S = 5V, 0V$



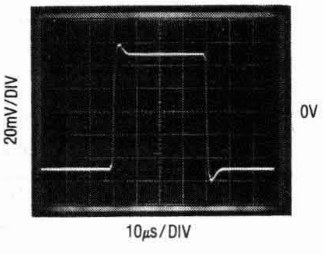
$A_V = +1$, $C_L = 15pF$, INPUT 50mV TO 150mV

Small Signal Transient Response $V_S = ±2.5V$



$A_V = +1$, $C_L = 15pF$

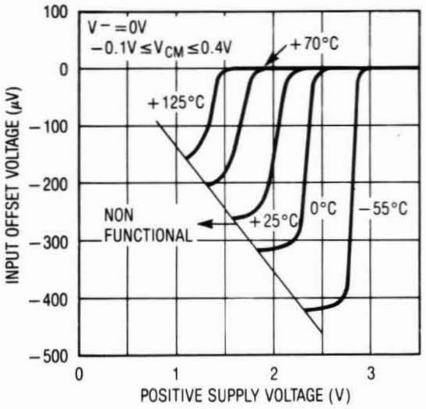
Small Signal Transient Response $V_S = ±15V$



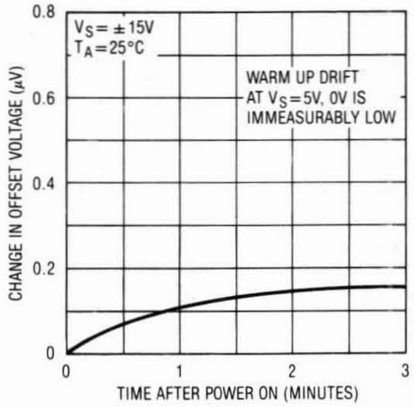
$A_V = +1$, $C_L = 15pF$

TYPICAL PERFORMANCE CHARACTERISTICS

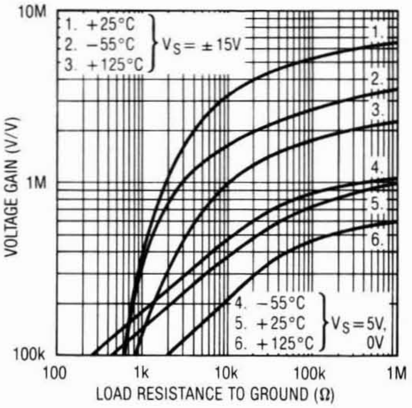
Minimum Supply Voltage



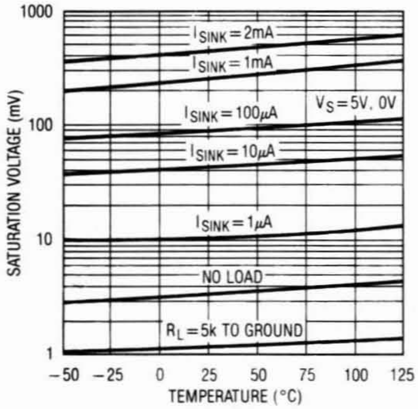
Warm-Up Drift



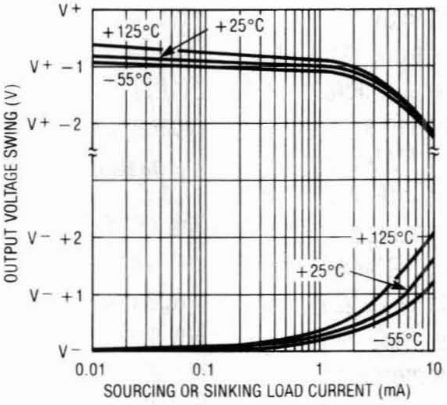
Voltage Gain vs Load Resistance



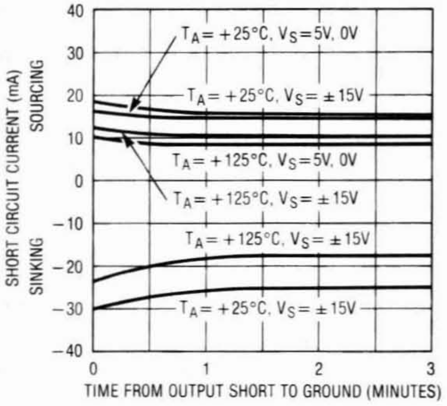
Output Saturation vs Temperature vs Sink Current



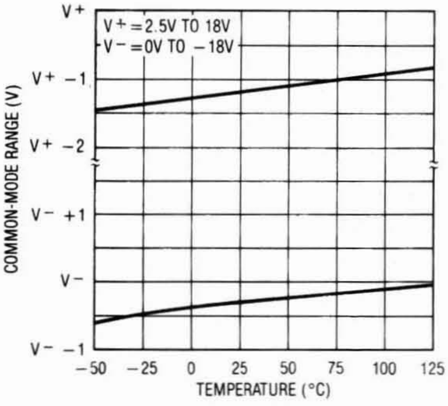
Output Voltage Swing vs Load Current



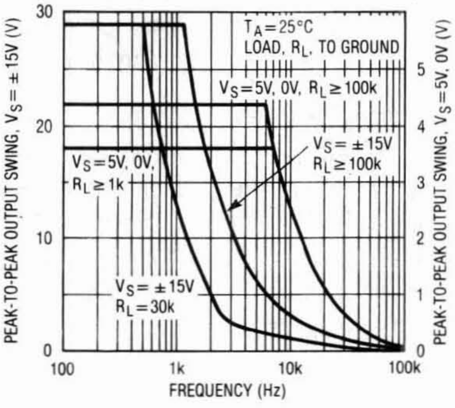
Short Circuit Current vs Time



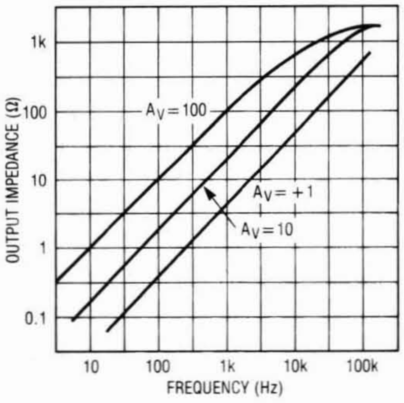
Common-Mode Range vs Temperature



Undistorted Output Swing vs Frequency

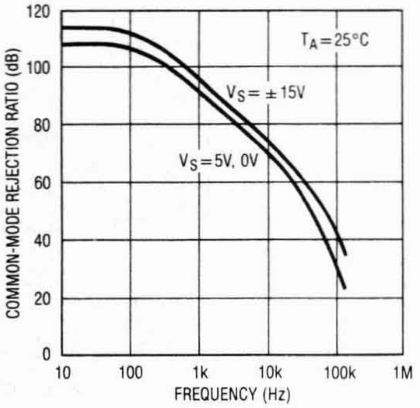


Closed Loop Output Impedance

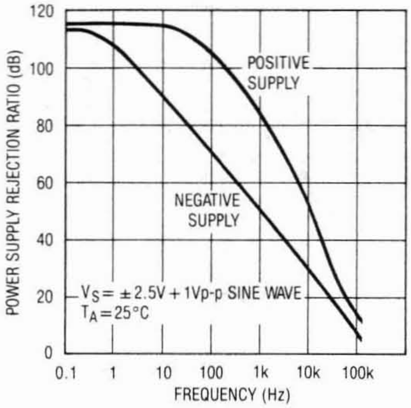


TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency



APPLICATIONS INFORMATION

The LT1077 is fully specified with $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 0.1V$. This set of operating conditions appears to be the most representative for battery powered micropower circuits. Offset voltage is internally trimmed to a minimum value at these supply voltages. When 9V or 3V batteries or ±2.5V dual supplies are used, bias and offset current changes will be minimal. Offset voltage changes will be just a few microvolts as given by the PSRR and CMRR specifications. For example, if PSRR = 114dB (= 2μV/V), at 9V the offset voltage change will be 8μV. Similarly, $V_S = \pm 2.5V$, $V_{CM} = 0$ is equivalent to a common-mode voltage change of 2.4V or a V_{OS} change of 7μV if CMRR = 110dB (3μV/V).

A full set of specifications is also provided at ±15V supply voltages for comparison with other devices and for completeness.

The LT1077 is pin compatible to, and directly replaces, such precision op amps as the OP-07, OP-77, AD707 and LT1001 with 30 to 60 times savings in supply current. The LT1077 is also a direct plug-in replacement for LT1012 and OP-97 devices with 10 times lower dissipation. Compatibility includes externally nulling the offset voltage, as all of the above devices are trimmed with a potentiometer between pins 1 and 8 and the wiper tied to V^+.

The LT1077 replaces and upgrades such micropower op amps as the OP-20, LM4250, and OP-90, provided that the external nulling circuitry (and set resistor in the case of the LM4250) are removed. Since the offset voltage of the LT1077 is extremely low, nulling will be unnecessary in most applications.

Single Supply Operation

The LT1077 is fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range goes below ground and the output swings within a few millivolts of ground while sinking current. All competing micropower op amps either cannot swing to within 600mV of ground (OP-20, OP-220, OP-420) or need a pull down resistor connected to the output to swing to ground (OP-90, OP-290, OP-490, HA5141/42/44). This difference is critical because in many applications these competing devices cannot be operated as micropower op amps and swing to ground simultaneously.

As an example, consider the difference amplifiers shown as Typical Applications. When the common-mode signal is high and the output low, the amplifier has to sink current. In the gain of 10 circuit, the competing devices require a 30k pull down resistor at the output to handle the specified signals. (The LT1077 does not need pull down resistors.) When the output is high the pull down resistor draws 80μA which dominates the micropower current budget.

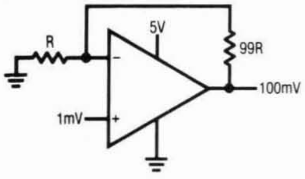
This situation is much worse in the gain of one circuit with $V^- = 0V$. At 100V common mode the output has to sink

APPLICATIONS INFORMATION

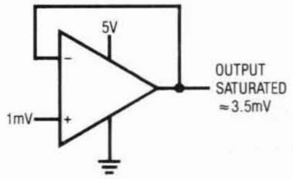
2µA. At a minimum output voltage of 20mV competing devices require a 10k pull down resistor. As the output now swings to 10V, this resistor draws 1mA of current.

Since the output of the LT1077 cannot go exactly to ground, but can only approach ground to within a few millivolts, care should be exercised to ensure that the output is not saturated. For example, a 1mV input signal will cause the amplifier to set up in its linear region in the gain 100 configuration shown below, but is not enough to make the amplifier function properly in the voltage follower mode.

Gain 100 Amplifier



Voltage Follower

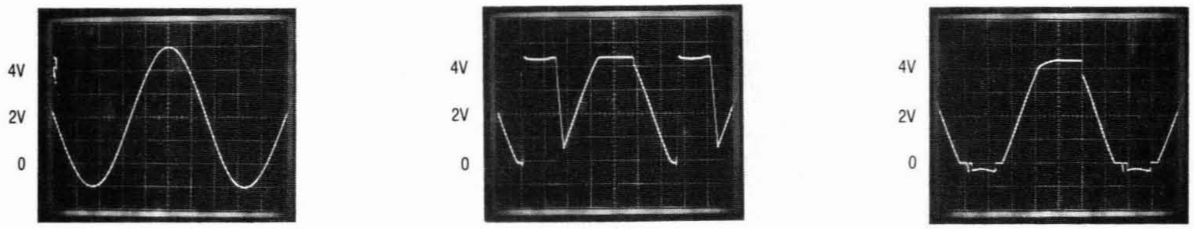


Single supply operation can also create difficulties at the input. The driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420 (a and b), OP-90/290/490 (b only):

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1077, resistors in series with the input protect the device even when the input is 5V below ground.

b) When the input is more than 400mV below ground (at 25°C), the input stage saturates and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry, the LT1077's output does not reverse, as illustrated below, even when the input is at −1.0V.

Voltage Follower with Input Exceeding the Negative Common-Mode Range (V_S = 5V, 0V)



1ms/DIV
6Vp-p INPUT, −1.0 TO +5.0V

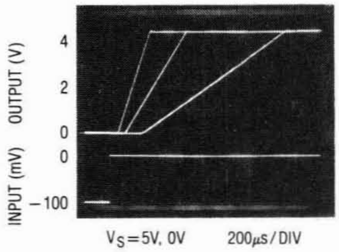
1ms/DIV
OP-90 EXHIBITS OUTPUT
PHASE REVERSAL

1ms/DIV
LT1077
NO PHASE REVERSAL

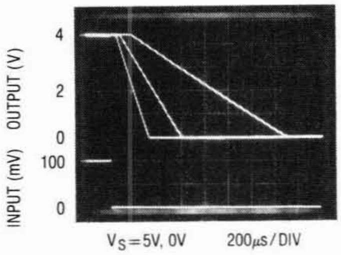
Comparator Applications

The single supply operation of the LT1077 and its ability to swing close to ground while sinking current lends itself to use as a precision comparator with TTL compatible output.

Comparator Rise Response Time to 10mV, 5mV, 2mV Overdrives

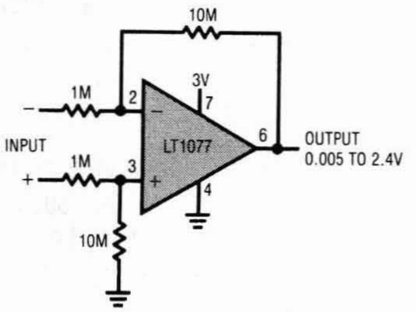


Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives



TYPICAL APPLICATIONS

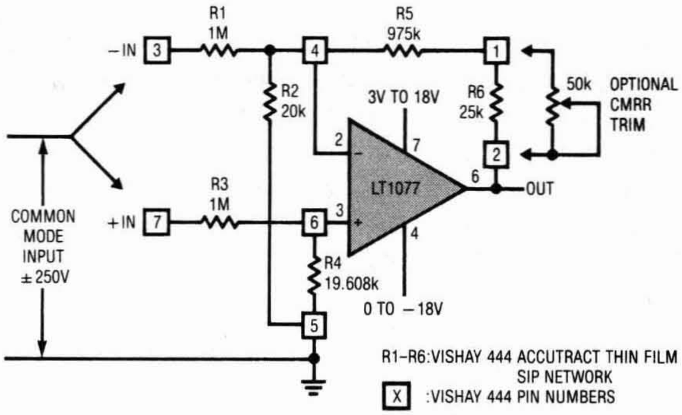
Megaohm Input Impedance Gain of 10 Difference Amplifier


10M
1M
−
INPUT
1M
+
2
3
3V
7
LT1077
6
4
OUTPUT
0.005 TO 2.4V
10M

BANDWIDTH = 20kHz
OUTPUT OFFSET = 0.7mV
OUTPUT NOISE = 80μV$_{pp}$ (0.1Hz TO 10Hz)
260μV RMS OVER FULL BANDWIDTH
SUPPLY CURRENT = 45μA

THE USEFULNESS OF DIFFERENCE AMPLIFIERS IS LIMITED BY THE FACT THAT THE INPUT RESISTANCE IS EQUAL TO THE SOURCE RESISTANCE. THE PICOAMPERE OFFSET CURRENT AND LOW CURRENT NOISE OF THE LT1077 ALLOWS THE USE OF 1MΩ SOURCE RESISTORS WITHOUT DEGRADATION IN PERFORMANCE. IN ADDITION, WITH MEGAOHM RESISTORS MICROPOWER OPERATION CAN BE MAINTAINED.

± 250V Common-Mode Range Difference Amplifier ($A_V = 1$)

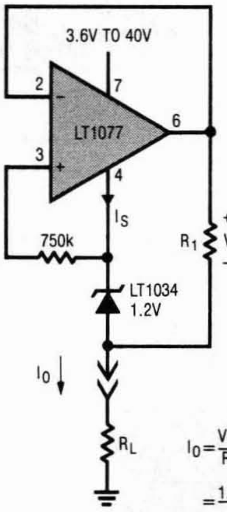

R1
1M
R5
975k
−IN
3
4
1
R2
20k
3V TO 18V
R6
25k
50k
OPTIONAL
CMRR
TRIM
2
2
7
6
LT1077
OUT
R3
1M
COMMON
MODE
INPUT
± 250V
+IN
7
6
3
4
R4
19.608k
0 TO −18V
5

R1–R6:VISHAY 444 ACCUTRACT THIN FILM SIP NETWORK
☒ :VISHAY 444 PIN NUMBERS

VISHAY INTERTECHNOLOGY, INC.
63 LINCOLN HIGHWAY
MALVERN, PA 19355

COMMON MODE REJECTION RATIO = 74dB (RESISTOR LIMITED)
WITH OPTIONAL TRIM = 108dB
OUTPUT OFFSET (TRIMMABLE TO ZERO) = 500μV
OUTPUT OFFSET DRIFT = 25μV/°C
INPUT RESISTANCE = 1M
COMMON MODE RANGE = ± 250V, V+ = 6.2V TO 18V, V− = −4.7V TO −18V
= ± 100V, V+ ≥ 3.2V, V− ≤ −1.8V
= + 100V, −13V, V+ ≥ 3.2V, V− = 0V

Two Terminal Current Source

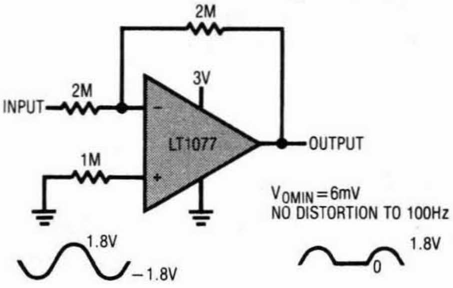

3.6V TO 40V
2
7
LT1077
6
3
4
I_S
750k
R_1
+
V_{R1}
−
LT1034
1.2V
I_O
R_L

$$I_O = \frac{V_{R1}}{R_1} + I_S$$

$$= \frac{1.230V}{R_1} + 50\mu A$$

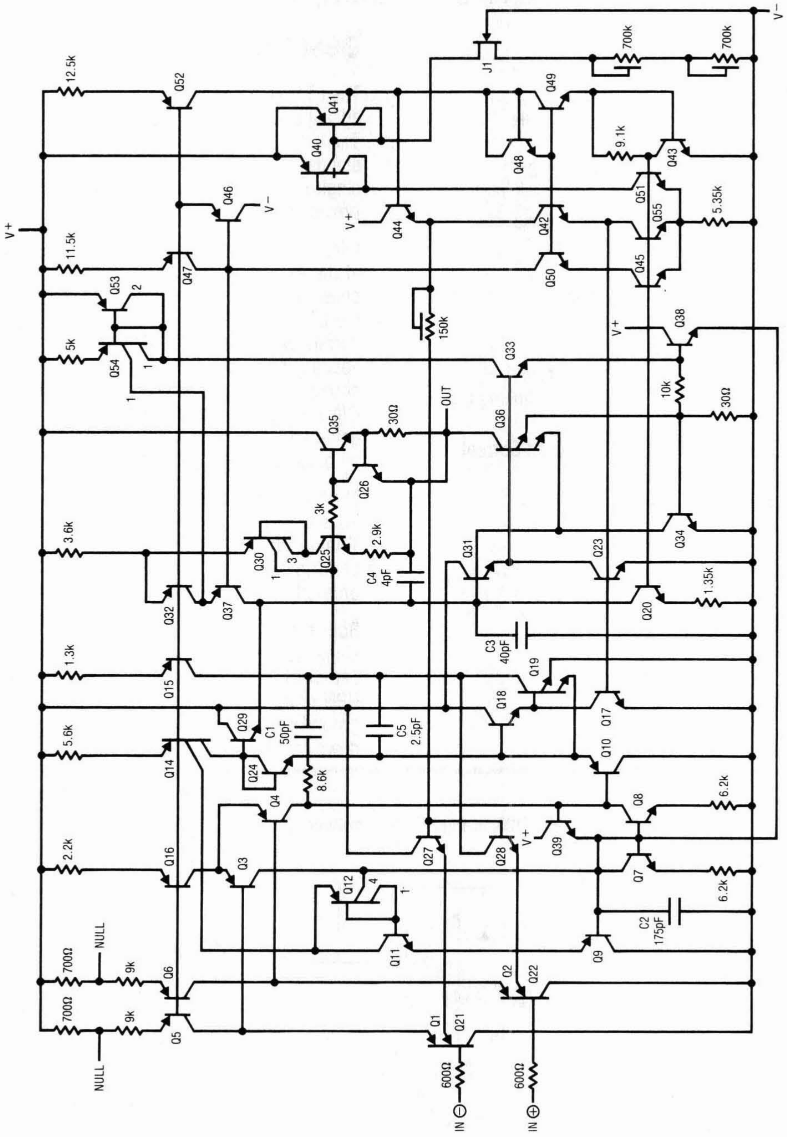
MINIMUM CURRENT = 50μA ($R_1 \rightarrow \infty$)
MAXIMUM CURRENT = 10.3mA (R_1 = 120Ω)

Half-Wave Rectifier


2M
3V
INPUT
2M
−
LT1077
OUTPUT
1M
+
1.8V
−1.8V
1.8V
0

V_{OMIN} = 6mV
NO DISTORTION TO 100Hz

SIMPLIFIED SCHEMATIC


V+
V−
NULL
NULL
700Ω
700Ω
9k
9k
2.2k
5.6k
1.3k
3.6k
5k
11.5k
12.5k
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
Q38
Q39
Q40
Q41
Q42
Q43
Q44
Q45
Q46
Q47
Q48
Q49
Q50
Q51
Q52
Q53
Q54
Q55
J1
C1
50pF
C2
175pF
C3
40pF
C4
4pF
C5
2.5pF
8.6k
3k
2.9k
30Ω
30Ω
10k
150k
1.35k
6.2k
6.2k
9.1k
5.35k
700k
700k
600Ω
600Ω
IN −
IN +
OUT
1
2
3
4

LINEAR TECHNOLOGY

LT1078/LT1079

Micropower, Dual and Quad, Single Supply, Precision Op Amps

FEATURES

- Available in 8-Pin SO Package
- 50µA Max Supply Current Per Amplifier
- 70µV Max Offset Voltage
- 180µV Max Offset Voltage in 8-Pin SO
- 250pA Max Offset Current
- 0.6µVp-p 0.1Hz to 10Hz Voltage Noise
- 3pAp-p 0.1Hz to 10Hz Current Noise
- 0.4µV/°C Offset Voltage Drift
- 200kHz Gain-Bandwidth Product
- 0.07V/µs Slew Rate
- Single Supply Operation
  - Input Voltage Range Includes Ground
  - Output Swings to Ground While Sinking Current
  - No Pull Down Resistors Needed
- Output Sources and Sinks 5mA Load Current

APPLICATIONS

- Battery or Solar Powered Systems
  - Portable Instrumentation
  - Remote Sensor Amplifier
  - Satellite Circuitry
- Micropower Sample-and-Hold
- Thermocouple Amplifier
- Micropower Filters

DESCRIPTION

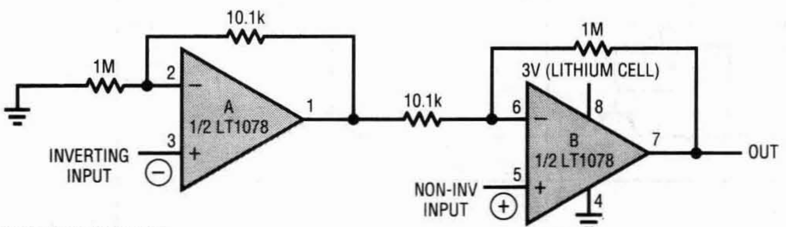
The LT1078 is a micropower dual op amp in 8-pin packages including the small outline surface mount package. The LT1079 is a micropower quad op amp offered in the standard 14-pin packages. Both devices are optimized for single supply operation at 5V. ±15V specifications are also provided.

Micropower performance of competing devices is achieved at the expense of seriously degrading precision, noise, speed, and output drive specifications. The design effort of the LT1078/1079 was concentrated on reducing supply current without sacrificing other parameters. The offset voltage achieved is the lowest on any dual or quad non-chopper stabilized op amp — micropower or otherwise. Offset current, voltage and current noise, slew rate and gain-bandwidth product are all two to ten times better than on previous micropower op amps.

The 1/f corner of the voltage noise spectrum is at 0.7Hz, at least three times lower than on any monolithic op amp. This results in low frequency (0.1Hz to 10Hz) noise performance which can only be found on devices with an order of magnitude higher supply current.

Both the LT1078 and LT1079 can be operated from a single supply (as low as one lithium cell or two Ni-cad batteries). The input range goes below ground. The all-NPN output stage swings to within a few millivolts of ground while sinking current — no power consuming pull down resistors are needed.

Single Battery, Micropower, Gain = 100, Instrumentation Amplifier

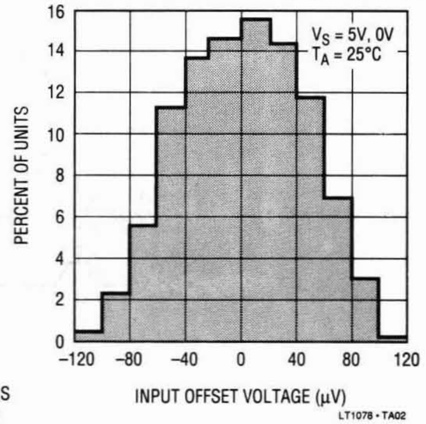


TYPICAL PERFORMANCE
INPUT OFFSET VOLTAGE = 40µV
INPUT OFFSET CURRENT = 0.2nA
TOTAL POWER DISSIPATION = 240µW
COMMON-MODE REJECTION = 110dB (AMPLIFIER LIMITED)
GAIN-BANDWIDTH PRODUCT = 200kHz

OUTPUT NOISE = 85µVp-p 0.1Hz TO 10Hz
= 300μV_{RMS} OVER FULL BANDWIDTH
INPUT RANGE = 0.03V TO 1.8V
OUTPUT RANGE = 0.03V TO 2.3V
($0.3mV \le V_{IN+} - V_{IN-} \le 23mV$)
OUTPUTS SINK CURRENT — NO PULL DOWN RESISTORS ARE NEEDED

LT1078 • TA01

Distribution of Input Offset Voltage (LT1078 and LT1079 in H, J, N Packages)

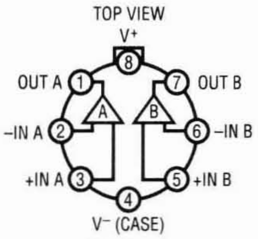


LT1078 • TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage	Equal to Positive Supply Voltage
	5V Below Negative Supply Voltage
Output Short Circuit Duration	Indefinite
Storage Temperature Range	
All Grades	– 65°C to 150°C
Operating Temperature Range	
LT1078AM/LT1078M/ LT1079AM/LT1079M	–55°C to 125°C
LT1078I/LT1079I	–40°C to 85°C
LT1078AC/LT1078C/LT1078S8/LT1078S16/ LT1079AC/LT1079C	0°C to 70°C
Lead Temperature (Soldering, 10 sec.)	300°C

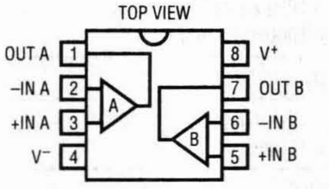
PACKAGE/ORDER INFORMATION


TOP VIEW
V+
8
OUT A 1
7 OUT B
A
B
–IN A 2
6 –IN B
+IN A 3
5 +IN B
4
V– (CASE)

H PACKAGE
8-LEAD TO-5 METAL CAN

LT1078 • POI01

ORDER PART NUMBER
LT1078AMH
LT1078MH
LT1078ACH
LT1078CH

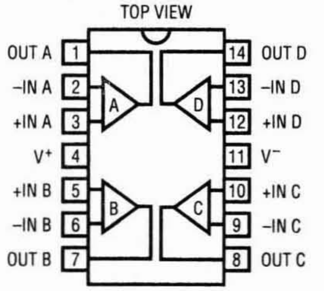

TOP VIEW
OUT A 1
–IN A 2
+IN A 3
V– 4
8 V+
7 OUT B
6 –IN B
5 +IN B
A
B

J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

LT1078 • POI02

ORDER PART NUMBER	
LT1078AMJ8	LT1078ACN8
LT1078MJ8	LT1078CN8
LT1078ACJ8	LT1078IN8
LT1078CJ8	

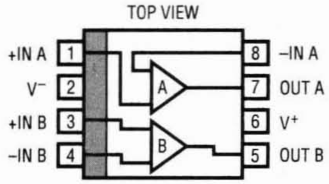

TOP VIEW
OUT A 1
–IN A 2
+IN A 3
V+ 4
+IN B 5
–IN B 6
OUT B 7
14 OUT D
13 –IN D
12 +IN D
11 V–
10 +IN C
9 –IN C
8 OUT C
A
D
B
C

J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

LT1078 • POI03

ORDER PART NUMBER	
LT1079AMJ	LT1079ACN
LT1079MJ	LT1079CN
LT1079ACJ	LT1079IN
LT1079CJ	

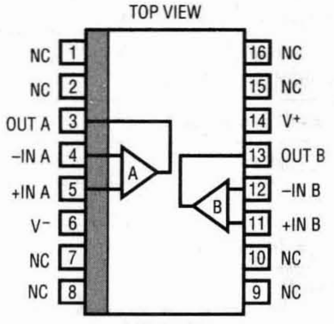

TOP VIEW
+IN A 1
V– 2
+IN B 3
–IN B 4
8 –IN A
7 OUT A
6 V+
5 OUT B
A
B

S8 PACKAGE
8-LEAD PLASTIC SOIC

NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-LEAD DIP PIN LOCATIONS. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE CONFIGURATION.

LT1078 • POI04

ORDER PART NUMBER	PART MARKING
LT1078IS8	1078I
LT1078S8	1078

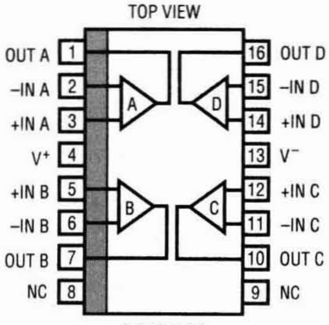

TOP VIEW
NC 1
NC 2
OUT A 3
–IN A 4
+IN A 5
V– 6
NC 7
NC 8
16 NC
15 NC
14 V+
13 OUT B
12 –IN B
11 +IN B
10 NC
9 NC
A
B

S PACKAGE
16-LEAD PLASTIC SOL

NOTE: THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGNS.

LT1078 • POI05

ORDER PART NUMBER
LT1078IS16
LT1078S16


TOP VIEW
OUT A 1
–IN A 2
+IN A 3
V+ 4
+IN B 5
–IN B 6
OUT B 7
NC 8
16 OUT D
15 –IN D
14 +IN D
13 V–
12 +IN C
11 –IN C
10 OUT C
9 NC
A
D
B
C

S PACKAGE
16-LEAD PLASTIC SOL

LT1078 • POI06

ORDER PART NUMBER
LT1079IS
LT1079S

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25°C, unless otherwise noted.

			LT1078AM/AC LT1079AM/AC			LT1078M/C/I/S LT1079M/C/I/S			
SYMBOL	**PARAMETER**	**CONDITIONS (Note 1)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	LT1078		30	70		40	120	µV
		LT1078IS8/LT1078S8					60	180	µV
		LT1079		35	100		40	150	µV
		LT1078IS16/S16, LT1079IS/S					60	300	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.4			0.5		µV/Mo
I_{OS}	Input Offset Current			0.05	0.25		0.05	0.35	nA
I_B	Input Bias Current			6	8		6	10	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.6	1.2		0.6		µVp-p
	Input Noise Voltage Density	f_O = 10Hz (Note 2)		29	45		29		nV/√Hz
		f_O = 1000Hz (Note 2)		28	37		28		nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		2.3	4.0		2.3		pAp-p
	Input Noise Current Density	f_O = 10Hz (Note 2)		0.06	0.10		0.06		pA/√Hz
		f_O = 1000Hz		0.02			0.02		pA/√Hz
	Input Resistance	(Note 3)							
	Differential Mode		400	800		300	800		MΩ
	Common-Mode			6			6		GΩ
	Input Voltage Range		3.5	3.8		3.5	3.8		V
			0	−0.3		0	−0.3		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.5V	97	110		94	108		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V	102	114		100	114		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.03V to 4V, No Load	200	1000		150	1000		V/mV
		V_O = 0.03V to 3.5V, R_L = 50k	150	600		120	600		V/mV
	Maximum Output Voltage Swing	Output Low, No Load		3.5	6		3.5	6	mV
		Output Low, 2k to GND		0.55	1.0		0.55	1.0	mV
		Output Low, I_{SINK} = 100µA		95	130		95	130	mV
		Output High, No Load	4.2	4.4		4.2	4.4		V
		Output High, 2k to GND	3.5	3.9		3.5	3.9		V
SR	Slew Rate	A_V = +1, V_S = ±2.5V	0.04	0.07		0.04	0.07		V/µs
GBW	Gain-Bandwidth Product	$f_O \leq$ 20kHz		200			200		kHz
I_S	Supply Current Per Amplifier			38	50		39	55	µA
	Channel Separation	ΔV_{IN} = 3V, R_L = 10k		130			130		dB
	Minimum Supply Voltage	(Note 4)		2.2	2.3		2.2	2.3	V

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, −40°C ≤ T_A ≤ 85°C for I grades, −55°C ≤ T_A ≤ 125°C for AM/M grades, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1078AM LT1079AM			LT1078M/I LT1079M/I			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1078	●		70	250		95	370	µV
		LT1079, LT1078IS8	●		80	280		100	400	µV
		LT1078IS16, LT1079IS	●					100	560	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		0.4	1.8		0.5	2.5	µV/°C
	(Note 5)	LT1078IS8	●					0.6	3.5	µV/°C
		LT1078IS16, LT1079IS	●					0.7	4.0	µV/°C
I_{OS}	Input Offset Current		●		0.07	0.50		0.07	0.70	nA
		LT1078I, LT1079I	●					0.1	1.0	nA
I_B	Input Bias Current		●		7	10		7	12	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0.05V to 3.2V	●	92	106		88	104		dB
PSRR	Power Supply Rejection Ratio	V_S = 3.1V to 12V	●	98	110		94	110		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.05V to 4V, No Load	●	110	600		80	600		V/mV
		V_O = 0.05V to 3.5V, R_L = 50k	●	80	400		60	400		V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●		4.5	8		4.5	8	mV
		Output Low, I_{SINK} = 100µA	●		125	170		125	170	mV
		Output High, No Load	●	3.9	4.2		3.9	4.2		V
		Output High, 2k to GND	●	3.0	3.7		3.0	3.7		V
I_S	Supply Current Per Amplifier		●		43	60		45	70	µA

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1078AC LT1079AC			LT1078C/S LT1079C/S			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1078	●		50	150		60	240	µV
		LT1079	●		60	180		70	270	µV
		LT1078S8	●					85	350	µV
		LT1078S16, LT1079S	●					90	480	µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		0.4	1.8		0.5	2.5	µV/°C
	(Note 5)	LT1078S8	●					0.6	3.5	µV/°C
		LT1078S16, LT1079S	●					0.7	4.0	µV/°C
I_{OS}	Input Offset Current		●		0.06	0.35		0.06	0.50	nA
I_B	Input Bias Current		●		6	9		6	11	nA
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.4V	●	94	108		90	106		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.6V to 12V	●	100	112		97	112		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.05V to 4V, No Load	●	150	750		110	750		V/mV
		V_O = 0.05V to 3.5V, R_L = 50k	●	110	500		80	500		V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●		4.0	7		4.0	7	mV
		Output Low, I_{SINK} = 100µA	●		105	150		105	150	mV
		Output High, No Load	●	4.1	4.3		4.1	4.3		V
		Output High, 2k to GND	●	3.3	3.8		3.3	3.8		V
I_S	Supply Current Per Amplifier		●		40	55		42	63	µA

ELECTRICAL CHARACTERISTICS V_S = ±15V, T_A = 25°C, unless otherwise noted.

			LT1078AM/AC LT1079AM/AC			LT1078M/C/I/S LT1079M/C/I/S			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	(Including LT1078IS8/S8) LT1078IS16/S16, LT1079IS/S		50	250		70 80	350 500	µV µV
I_{OS}	Input Offset Current			0.05	0.25		0.05	0.35	nA
I_B	Input Bias Current			6	8		6	10	nA
	Input Voltage Range		13.5 −15.0	13.8 −15.3		13.5 −15.0	13.8 −15.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} = +13.5V, −15V	100	114		97	114		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ±18V	102	114		100	114		dB
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 50k V_O = ±10V, R_L = 2k	1000 400	5000 1100		1000 300	5000 1100		V/mV V/mV
V_{OUT}	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±13.0 ±11.0	±14.0 ±13.2		±13.0 ±11.0	±14.0 ±13.2		V V
SR	Slew Rate		0.06	0.10		0.06	0.10		V/µs
I_S	Supply Current Per Amplifier			46	65		47	75	µA

ELECTRICAL CHARACTERISTICS

V_S = ±15V, −40°C ≤ T_A ≤ 85°C for I grades, −55°C ≤ T_A ≤ 125°C for AM/M grades, unless otherwise noted.

				LT1078AM LT1079AM			LT1078M/I LT1079M/I			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	(Including LT1078IS8) LT1078IS16, LT1079IS	● ●		90	430		120 130	600 825	µV µV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift (Note 5)	 LT1078IS8 LT1078IS16, LT1079IS	● ● ●		0.5	1.8		0.6 0.7 0.8	2.5 3.8 5.0	µV/°C µV/°C µV/°C
I_{OS}	Input Offset Current	 LT1078I, LT1079I	● ●		0.07	0.50		0.07 0.1	0.70 1.0	nA nA
I_B	Input Bias Current		●		7	10		7	12	nA
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 5k	●	200	700		150	700		V/mV
CMRR	Common-Mode Rejection Ratio	V_{CM} = +13V, −14.9V	●	94	110		90	110		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ±18V	●	98	110		94	110		dB
	Maximum Output Voltage Swing	R_L = 5k	●	±11.0	±13.5		±11.0	±13.5		V
I_S	Supply Current Per Amplifier		●		52	80		54	95	µA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

				LT1078AC LT1079AC			LT1078C/S LT1079C/S			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage		●		70	330		90	460	μV
		LT1078S8	●					100	540	μV
		LT1078S16, LT1079S	●					115	750	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		0.5	1.8		0.6	2.5	μV/°C
	(Note 5)	LT1078S8	●					0.7	3.8	μV/°C
		LT1078S16, LT1079S	●					0.8	5.0	μV/°C
I_{OS}	Input Offset Current		●		0.06	0.35		0.06	0.50	nA
I_B	Input Bias Current		●		6	9		6	11	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 5k$	●	300	1200		250	1200		V/mV
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 13V, -15V$	●	97	112		94	112		dB
PSRR	Power Supply Rejection Ratio	$V_S = 5V$, 0V to $\pm 18V$	●	100	112		97	112		dB
	Maximum Output Voltage Swing	$R_L = 5k$	●	±11.0	±13.6		±11.0	±13.6		V
I_S	Supply Current Per Amplifier		●		49	73		50	85	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1079s (or 100 LT1078s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only. All noise parameters are tested with $V_S = \pm 2.5V$, $V_O = 0V$.

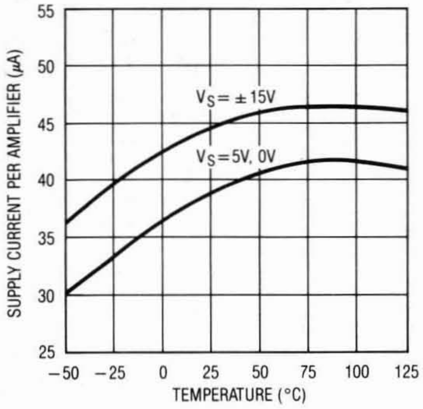
Note 3: This parameter is guaranteed by design and is not tested.

Note 4: Power supply rejection ratio is measured at the minimum supply voltage. The op amps actually work at 1.8V supply but with a typical offset skew of −300μV.

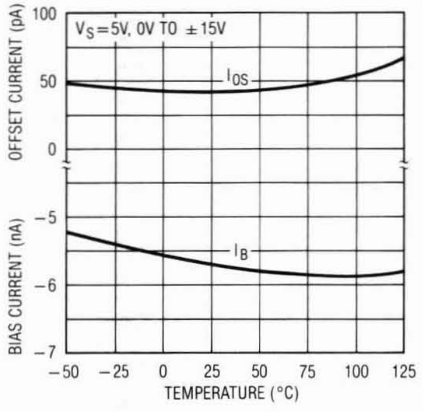
Note 5: This parameter is not 100% tested.

TYPICAL PERFORMANCE CHARACTERISTICS

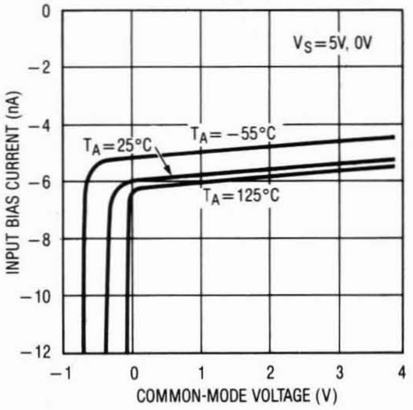
Supply Current vs Temperature



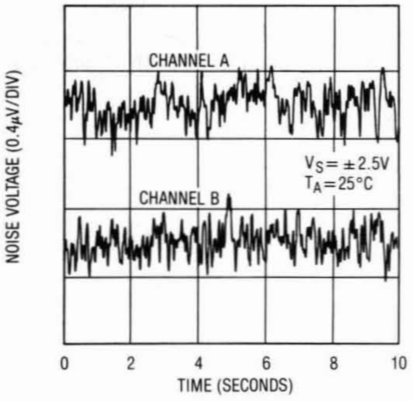
Input Bias and Offset Currents vs Temperature



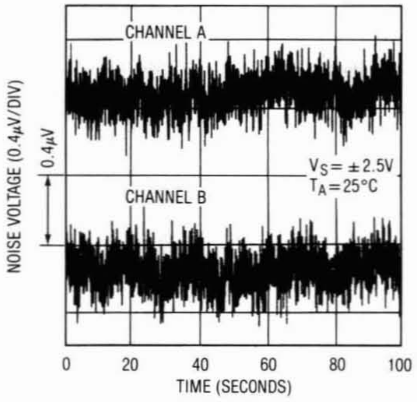
Input Bias Current vs Common-Mode Voltage



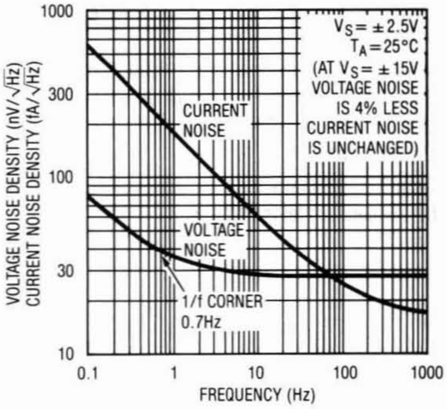
0.1Hz to 10Hz Noise



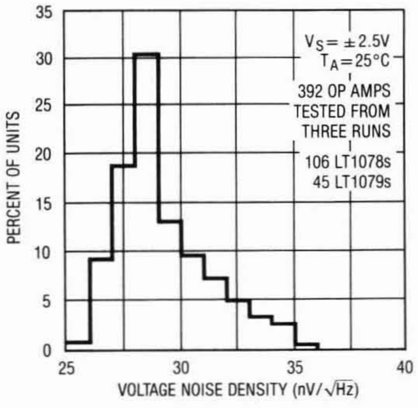
0.01Hz to 10Hz Noise



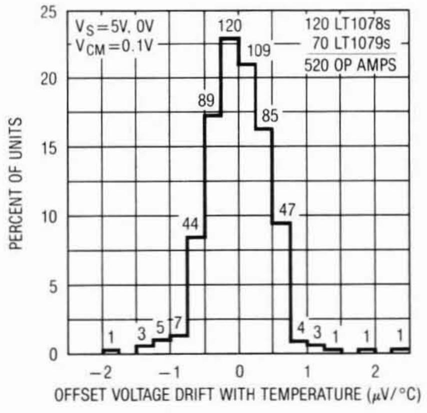
Noise Spectrum



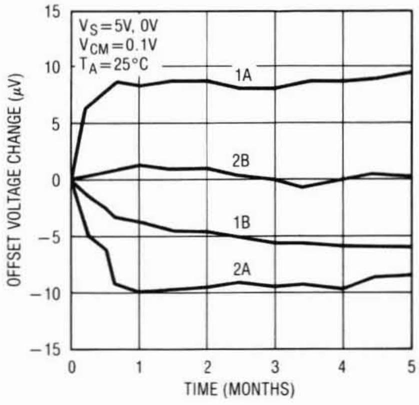
10Hz Voltage Noise Distribution



Distribution of Offset Voltage Drift with Temperature (In All Packages Except Surface Mount)

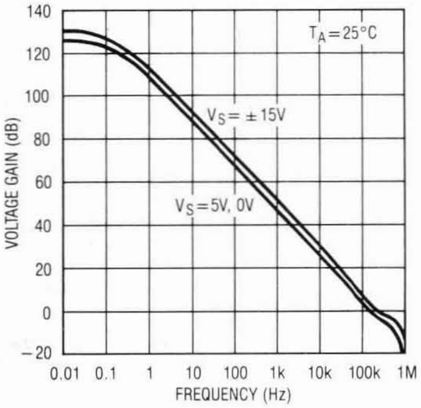


Long Term Stability of Two Representative Units (LT1078)

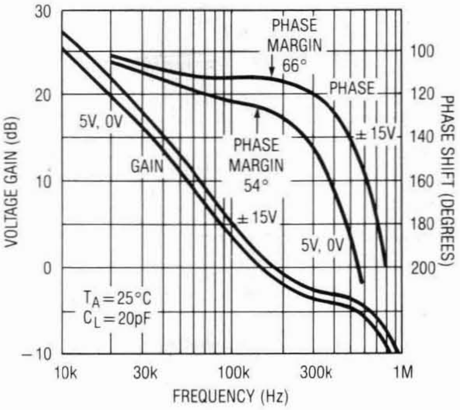


TYPICAL PERFORMANCE CHARACTERISTICS

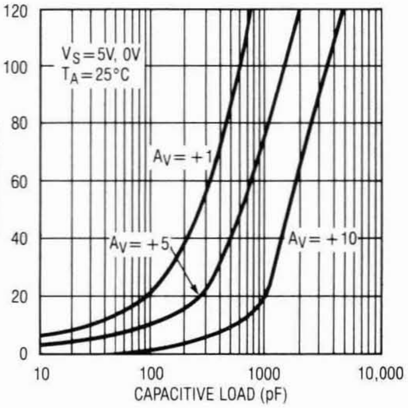
Voltage Gain vs Frequency



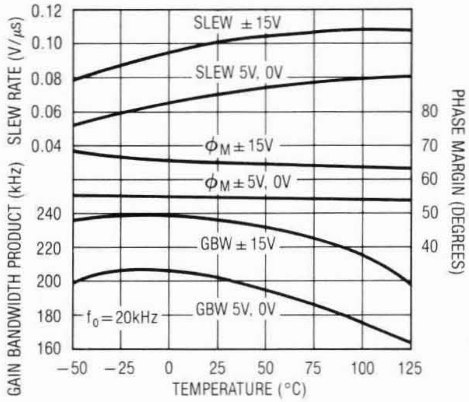
Gain, Phase vs Frequency



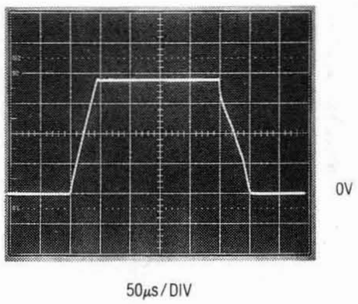
Capacitive Load Handling



Slew Rate, Gain Bandwidth Product and Phase Margin vs Temperature

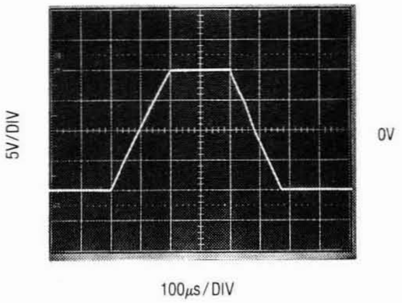


Large Signal Transient Response $V_S = 5V, 0V$



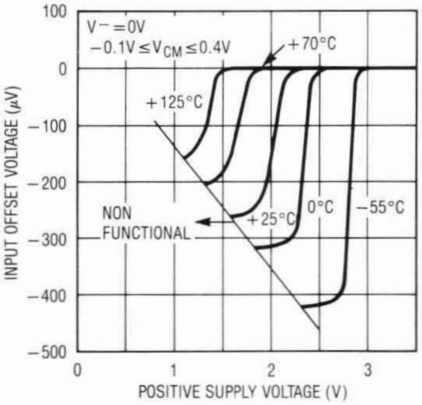
INPUT PULSE 0V TO 3.8V, $A_V = +1$, NO LOAD

Large Signal Transient Response $V_S = \pm 15V$

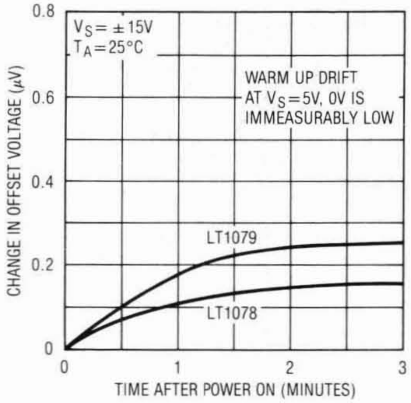


$A_V = +1$, NO LOAD

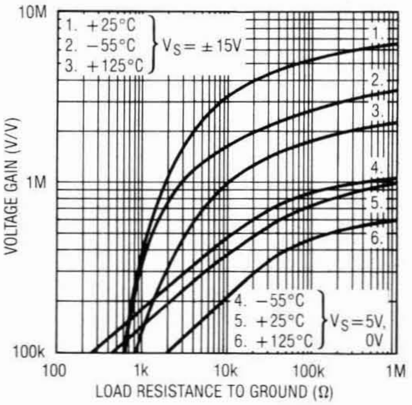
Minimum Supply Voltage



Warm-Up Drift

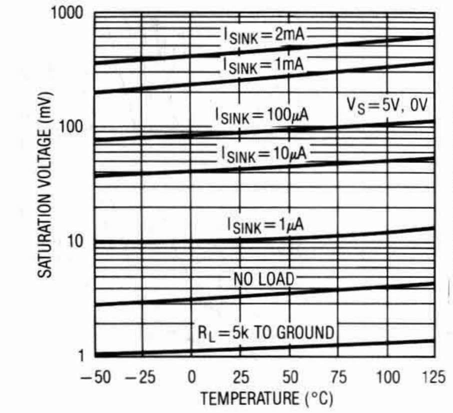


Voltage Gain vs Load Resistance

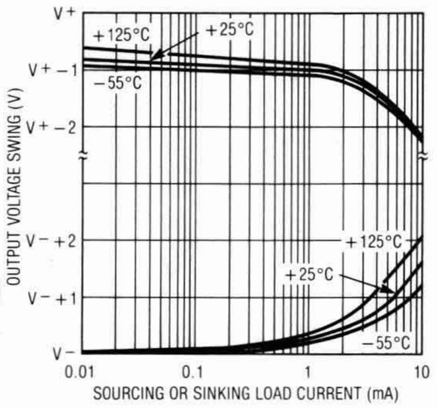


TYPICAL PERFORMANCE CHARACTERISTICS

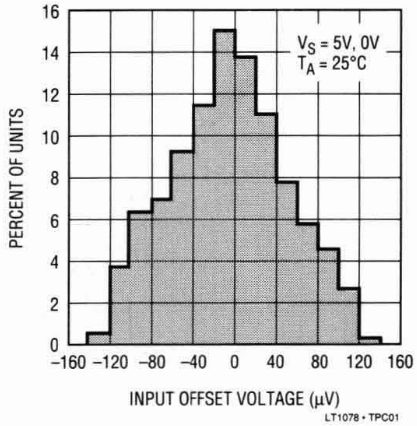
Output Saturation vs Temperature vs Sink Current



Output Voltage Swing vs Load Current

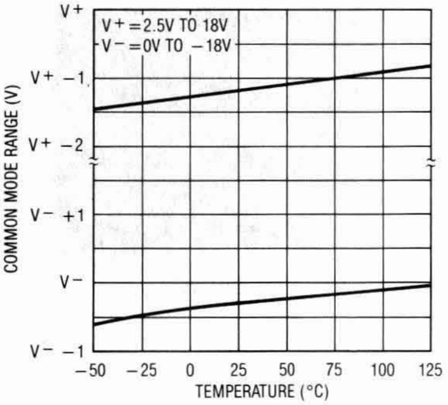


Distribution of Input Offset Voltage (LT1078 in 8-Pin SO Package)

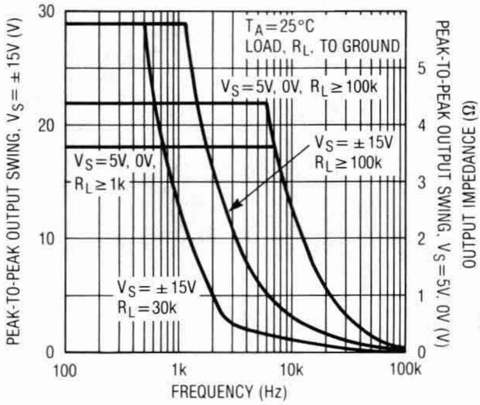


LT1078 • TPC01

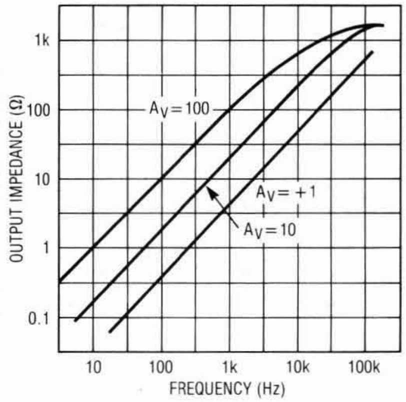
Common Mode Range vs Temperature



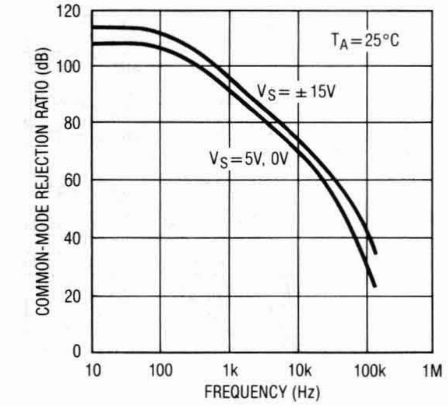
Undistorted Output Swing vs Frequency



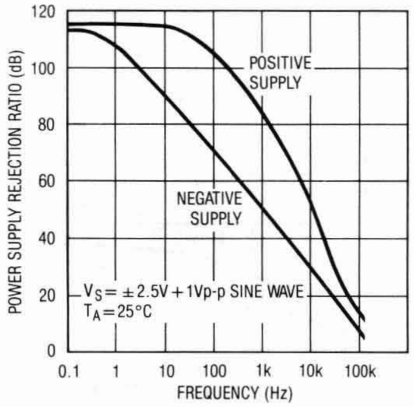
Closed Loop Output Impedance



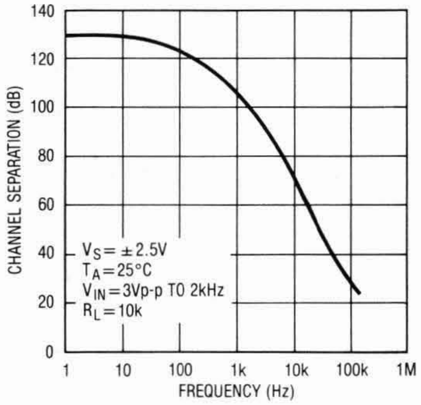
Common-Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency

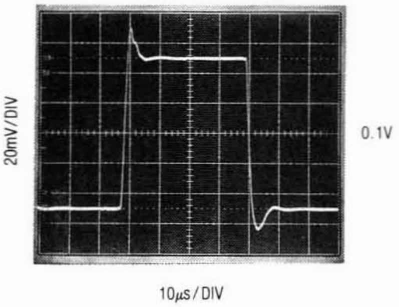


Channel Separation vs Frequency



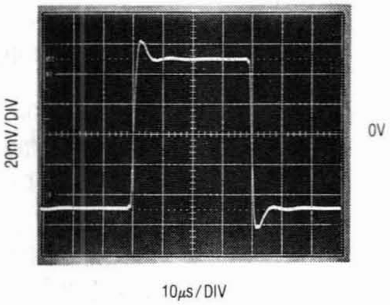
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Transient Response
$V_S = 5V, 0V$



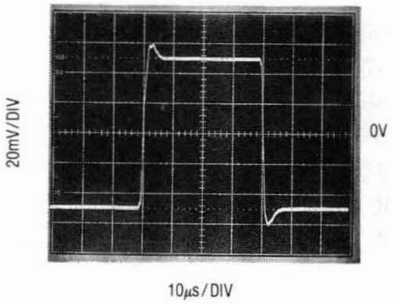
$A_V = +1$, $C_L = 15pF$, INPUT 50mV TO 150mV

Small Signal Transient Response
$V_S = \pm 2.5V$



$A_V = +1$, $C_L = 15pF$

Small Signal Transient Response
$V_S = \pm 15V$



$A_V = +1$, $C_L = 15pF$

APPLICATIONS INFORMATION

The LT1078/LT1079 devices are fully specified with $V^+ = 5V$, $V^- = 0$, $V_{CM} = 0.1V$. This set of operating conditions appears to be the most representative for battery powered micropower circuits. Offset voltage is internally trimmed to a minimum value at these supply voltages. When 9V or 3V batteries or ± 2.5V dual supplies are used, bias and offset current changes will be minimal. Offset voltage changes will be just a few microvolts as given by the PSRR and CMRR specifications. For example, if PSRR = 114dB (= 2μV/V), at 9V the offset voltage change will be 8μV. Similarly, $V_S = \pm 2.5V$, $V_{CM} = 0$ is equivalent to a common-mode voltage change of 2.4V or a V_{OS} change of 7μV if CMRR = 110dB (3μV/V).

A full set of specifications is also provided at ± 15V supply voltages for comparison with other devices and for completeness.

Single Supply Operation

The LT1078/LT1079 are fully specified for single supply operation, i.e., when the negative supply is 0V. Input common-mode range goes below ground and the output swings within a few millivolts of ground while sinking current. All competing micropower op amps either cannot swing to within 600mV of ground (OP-20, OP-220, OP-420)

APPLICATIONS INFORMATION

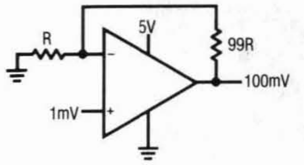
or need a pull down resistor connected to the output to swing to ground (OP-90, OP-290, OP-490, HA5141/42/44). This difference is critical because in many applications these competing devices cannot be operated as micropower op amps and swing to ground simultaneously.

As an example, consider the instrumentation amplifier shown on the front page. When the common-mode signal is low and the output is high, amplifier A has to sink current. When the common-mode signal is high and the output low, amplifier B has to sink current. The competing devices require a 12k pull down resistor at the output of amplifier A and a 15k at the output of B to handle the specified signals. (The LT1078 does not need pull down resistors.) When the common-mode input is high and the output is high these pull down resistors draw 300μA (150μA each), which is excessive for micropower applications.

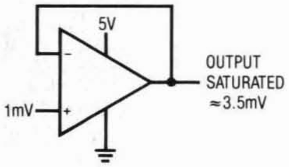
The instrumentation amplifier is by no means the only application requiring current sinking capability. In 7 of the 9 single supply applications shown in this data sheet the op amps have to be able to sink current. In two of the applications the first amplifier has to sink only the 6nA input bias current of the second op amp. The competing devices, however, cannot even sink 6nA without a pull down resistor.

Since the output of the LT1078/LT1079 cannot go exactly to ground, but can only approach ground to within a few millivolts, care should be exercised to ensure that the output is not saturated. For example, a 1 mV input signal will cause the amplifier to set up in its linear region in the gain 100 configuration shown below, but is not enough to make the amplifier function properly in the voltage follower mode.

Gain 100 Amplifier



Voltage Follower

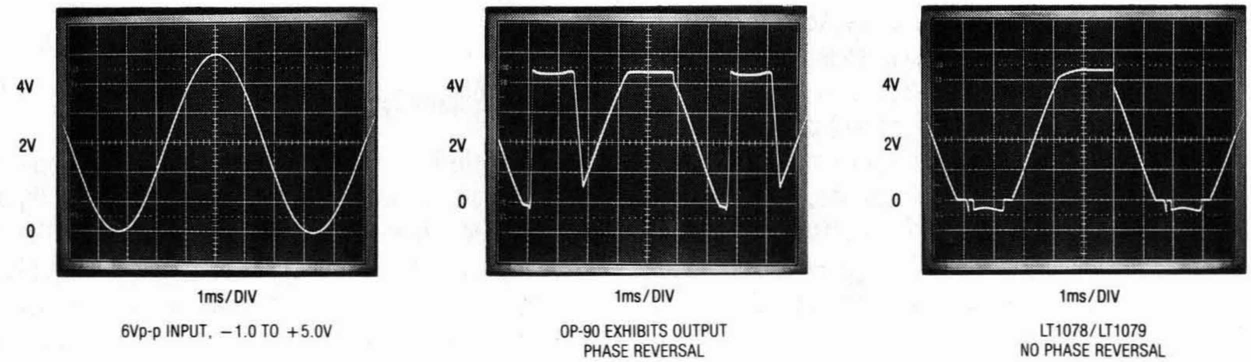


Single supply operation can also create difficulties at the input. The driving signal can fall below 0V—inadvertently or on a transient basis. If the input is more than a few hundred millivolts below ground, two distinct problems can occur on previous single supply designs, such as the LM124, LM158, OP-20, OP-21, OP-220, OP-221, OP-420 (a and b), OP-90/290/490 (b only):

a) When the input is more than a diode drop below ground, unlimited current will flow from the substrate (V^- terminal) to the input. This can destroy the unit. On the LT1078/LT1079, resistors in series with the input protect the devices even when the input is 5V below ground.

b) When the input is more than 400mV below ground (at 25°C), the input stage saturates and phase reversal occurs at the output. This can cause lock-up in servo systems. Due to a unique phase reversal protection circuitry, the LT1078/LT1079's output does not reverse, as illustrated below, even when the inputs are at −1.0V.

Voltage Follower with Input Exceeding the Negative Common-Mode Range (V_S = 5V, 0V)



1ms/DIV
6Vp-p INPUT, −1.0 TO +5.0V

1ms/DIV
OP-90 EXHIBITS OUTPUT
PHASE REVERSAL

1ms/DIV
LT1078/LT1079
NO PHASE REVERSAL

APPLICATIONS INFORMATION

Matching Specifications

In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The two and three op amp instrumentation amplifier configurations shown in this data sheet are examples. Matching characteristics are not 100% tested on the LT1078/79.

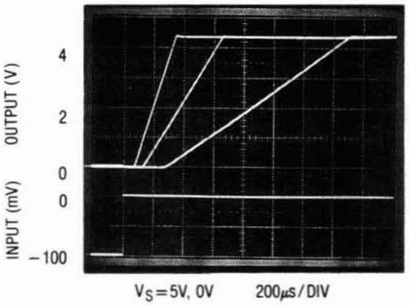
Some specifications are guaranteed by definition. For example, 70μV maximum offset voltage implies that mismatch cannot be more than 140μV. 97dB (= 14μV/V) CMRR means that worst case CMRR match is 91dB (= 28μV/V). However, the following table can be used to estimate the expected matching performance at $V_S = 5V$, 0V between the two sides of the LT1078, and between amplifiers A and D, and between amplifiers B and C of the LT1079.

PARAMETER		LT1078AM/AC LT1079AM/AC		LT1078M/C LT1079M/C		UNITS
		50% YIELD	98% YIELD	50% YIELD	98% YIELD	
V_{OS} Match, ΔV_{OS}	LT1078	30	110	50	190	μV
	LT1079	40	150	50	250	
Temperature Coefficient ΔV_{OS}		0.5	1.2	0.6	1.8	μV/°C
Average Non-Inverting I_B		6	8	6	10	nA
Match of Non-Inverting I_B		0.12	0.4	0.15	0.5	nA
CMRR Match		120	100	117	97	dB
PSRR Match		117	105	117	102	dB

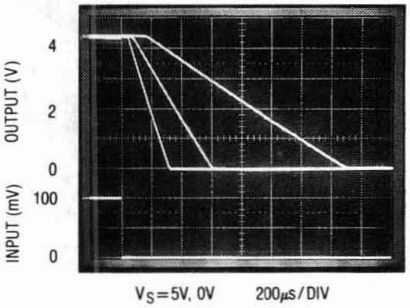
Comparator Applications

The single supply operation of the LT1078/1079 and its ability to swing close to ground while sinking current lends itself to use as a precision comparator with TTL compatible output.

Comparator Rise Response Time to 10mV, 5mV, 2mV Overdrives

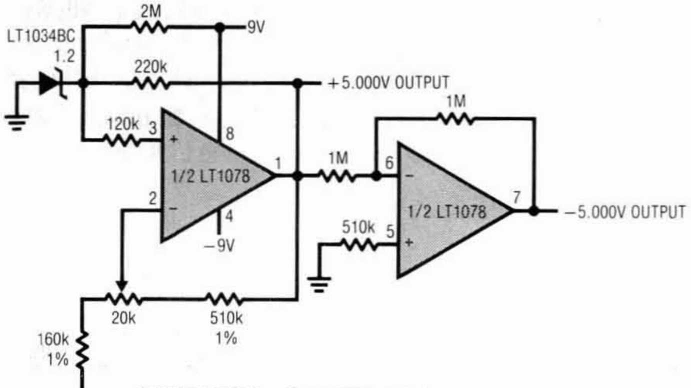


Comparator Fall Response Time to 10mV, 5mV, 2mV Overdrives



TYPICAL APPLICATIONS

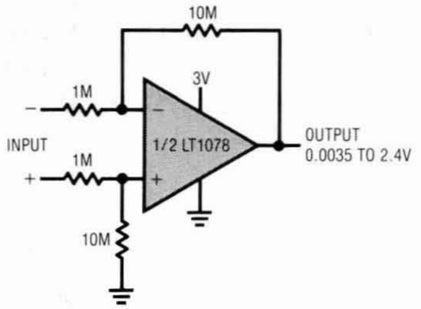
Micropower, 10ppm/°C, ± 5V Reference


LT1034BC
1.2
2M
9V
220k
+5.000V OUTPUT
120k
3
8
1/2 LT1078
1
2
4
−9V
1M
1M
6
7
1/2 LT1078
−5.000V OUTPUT
510k
5
20k
510k
1%
160k
1%

SUPPLY CURRENT: +9V BATTERY = 115μA
−9V BATTERY = 85μA
OUTPUT NOISE: 36μV$_{pp}$, 0.1Hz TO 10Hz

THE LT1078 CONTRIBUTES LESS THAN 3% OF THE TOTAL OUTPUT NOISE AND DRIFT WITH TIME AND TEMPERATURE. THE ACCURACY OF THE −5V OUTPUT DEPENDS ON THE MATCHING OF THE TWO 1M RESISTORS.

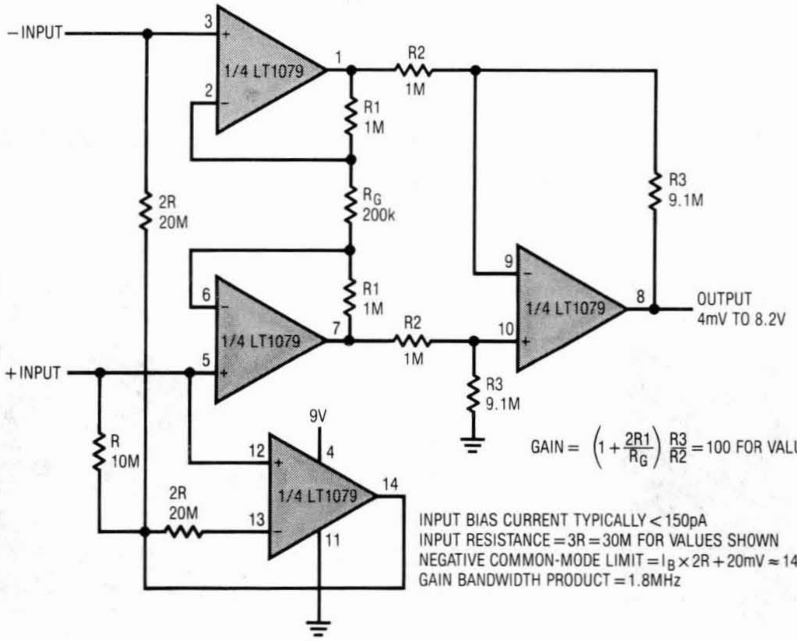
Gain of 10 Difference Amplifier


10M
3V
1M
−
INPUT
1M
+
1/2 LT1078
OUTPUT
0.0035 TO 2.4V
10M

BANDWIDTH = 20kHz
OUTPUT OFFSET = 0.7mV
OUTPUT NOISE = 80μV$_{pp}$ (0.1Hz TO 10Hz)
260μV RMS OVER FULL BANDWIDTH

THE USEFULNESS OF DIFFERENCE AMPLIFIERS IS LIMITED BY THE FACT THAT THE INPUT RESISTANCE IS EQUAL TO THE SOURCE RESISTANCE. THE PICOAMPERE OFFSET CURRENT AND LOW CURRENT NOISE OF THE LT1078 ALLOWS THE USE OF 1MΩ SOURCE RESISTORS WITHOUT DEGRADATION IN PERFORMANCE. IN ADDITION, WITH MEGAOHM RESISTORS MICROPOWER OPERATION CAN BE MAINTAINED.

Picoampere Input Current, Triple Op Amp Instrumentation Amplifier with Bias Current Cancellation

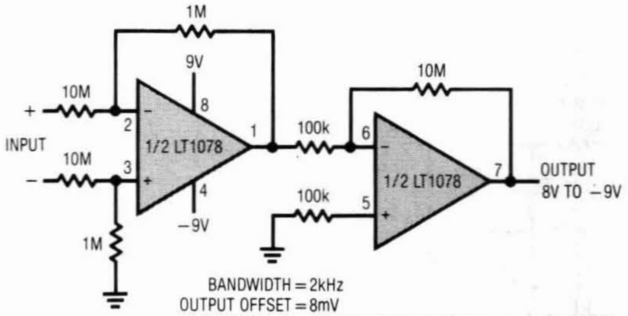

−INPUT
3
1/4 LT1079
2
1
R2
1M
R1
1M
R$_G$
200k
2R
20M
R3
9.1M
9
6
R1
1M
1/4 LT1079
7
R2
1M
10
1/4 LT1079
8
OUTPUT
4mV TO 8.2V
+INPUT
5
R3
9.1M
9V
R
10M
12
4
1/4 LT1079
14
2R
20M
13
11

$\text{GAIN} = \left(1 + \frac{2R1}{R_G}\right) \frac{R3}{R2} = 100$ FOR VALUES SHOWN

INPUT BIAS CURRENT TYPICALLY < 150pA
INPUT RESISTANCE = 3R = 30M FOR VALUES SHOWN
NEGATIVE COMMON-MODE LIMIT = $I_B \times 2R + 20mV \approx 140mV$
GAIN BANDWIDTH PRODUCT = 1.8MHz

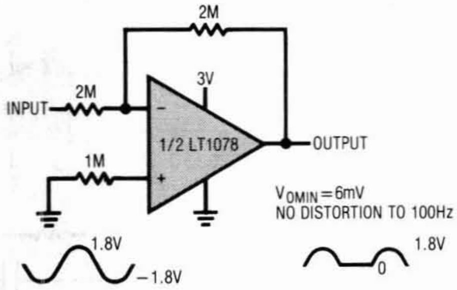
TYPICAL APPLICATIONS

+85V, –100V Common Mode Range Instrumentation Amplifier ($A_V = 10$)


1M
9V
10M
10M
+
INPUT
–
10M
8
2
1/2 LT1078
1
3
4
–9V
1M
100k
100k
6
5
1/2 LT1078
7
OUTPUT
8V TO –9V

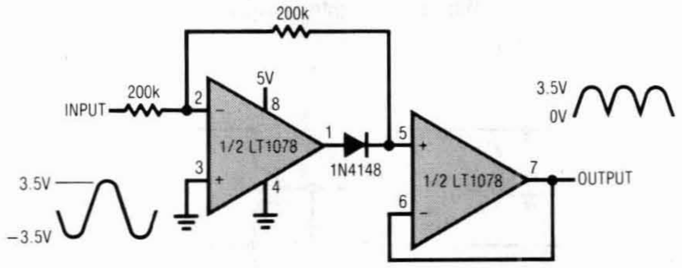
BANDWIDTH = 2kHz
OUTPUT OFFSET = 8mV
OUTPUT NOISE = 0.8mV$_{pp}$ (0.1Hz to 10 Hz)
= 1.4mV RMS OVER FULL BANDWIDTH
(DOMINATED BY RESISTOR NOISE)
INPUT RESISTANCE = 10MΩ

Half-Wave Rectifier


2M
3V
INPUT
2M
1/2 LT1078
OUTPUT
1M
1.8V
–1.8V
1.8V
0

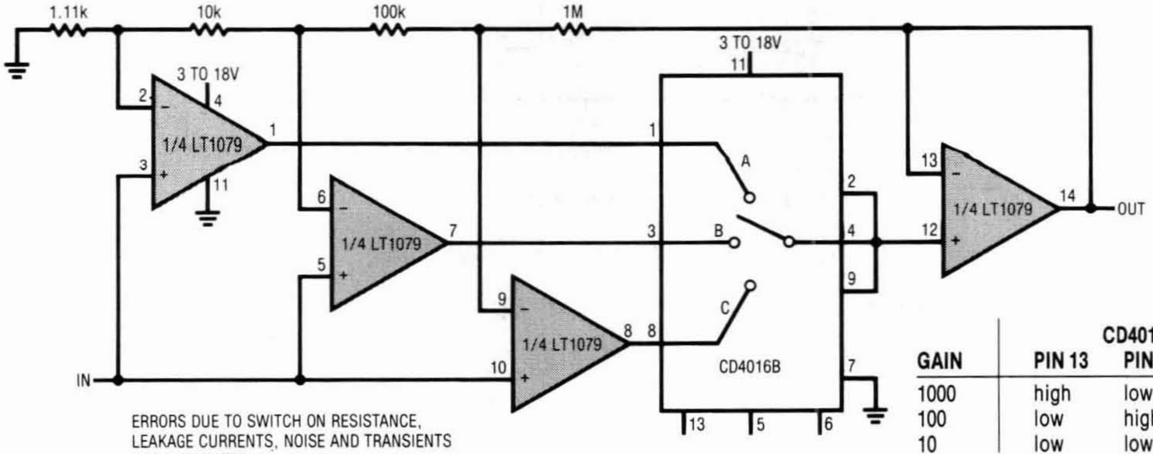
V_{OMIN} = 6mV
NO DISTORTION TO 100Hz

Absolute Value Circuit (Full-Wave Rectifier)


200k
5V
INPUT
200k
2
8
1/2 LT1078
1
3
4
1N4148
5
1/2 LT1078
7
6
OUTPUT
3.5V
0V
3.5V
–3.5V

V_{OMIN} = 4mV
NO DISTORTION TO 100Hz

Programmable Gain Amplifier (Single Supply)

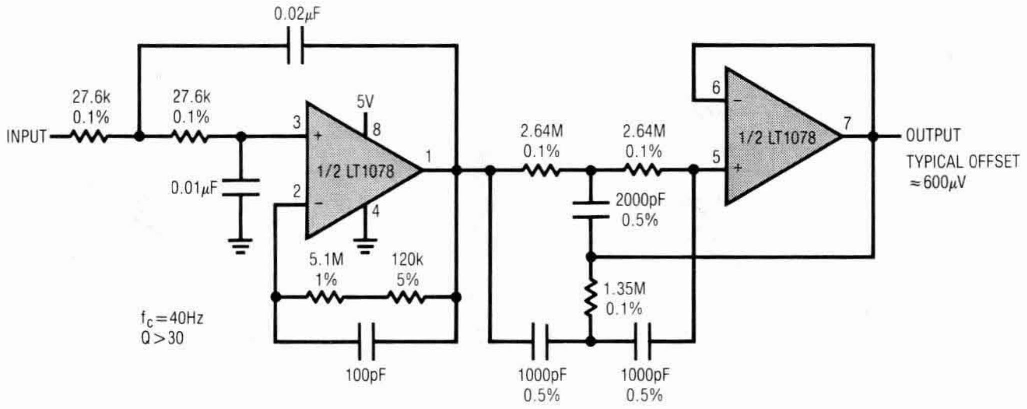

1.11k
10k
100k
1M
3 TO 18V
2
4
1/4 LT1079
1
3
11
6
1/4 LT1079
7
5
9
1/4 LT1079
8
10
IN
3 TO 18V
11
1
A
3
B
C
8
CD4016B
2
4
9
7
13
5
6
13
12
1/4 LT1079
14
OUT

ERRORS DUE TO SWITCH ON RESISTANCE, LEAKAGE CURRENTS, NOISE AND TRANSIENTS ARE ELIMINATED.

	CD4016B		
GAIN	**PIN 13**	**PIN 5**	**PIN 6**
1000	high	low	low
100	low	high	low
10	low	low	high

TYPICAL APPLICATIONS

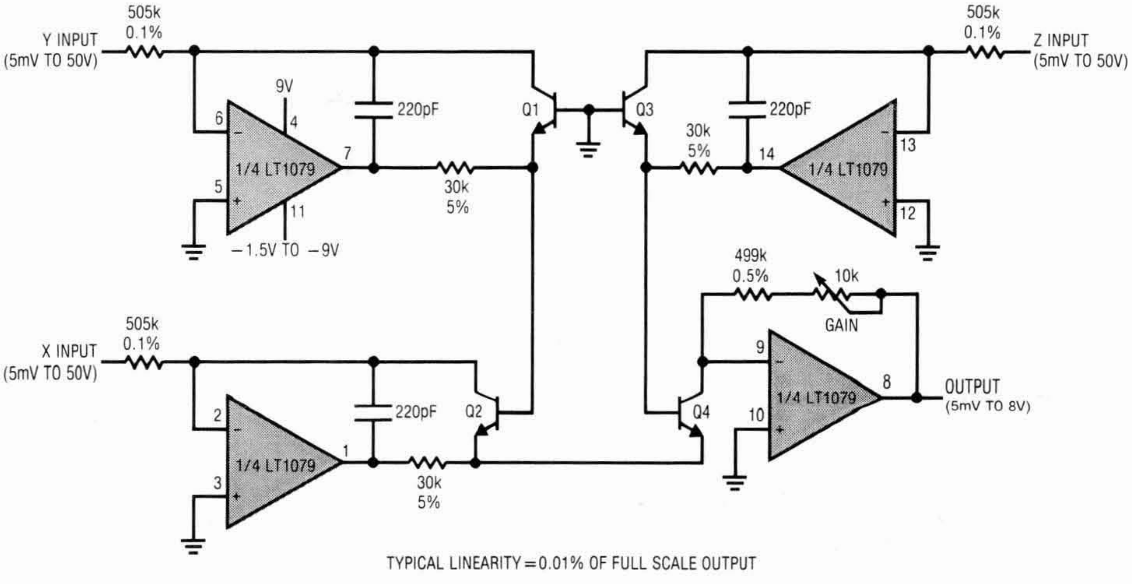
Single Supply, Micropower, Second Order Low Pass Filter with 60Hz Notch


0.02μF
INPUT
27.6k
0.1%
27.6k
0.1%
0.01μF
5V
3
8
2
4
1/2 LT1078
1
5.1M
1%
120k
5%
100pF
2.64M
0.1%
2.64M
0.1%
2000pF
0.5%
1.35M
0.1%
1000pF
0.5%
1000pF
0.5%
6
5
7
1/2 LT1078
OUTPUT

$f_c = 40Hz$
$Q > 30$

TYPICAL OFFSET
≈600μV

Micropower Multiplier/Divider


Y INPUT
(5mV TO 50V)
505k
0.1%
9V
6
4
5
7
11
1/4 LT1079
−1.5V TO −9V
220pF
30k
5%
Q1
Q3
505k
0.1%
Z INPUT
(5mV TO 50V)
220pF
30k
5%
14
13
12
1/4 LT1079
499k
0.5%
10k
GAIN
X INPUT
(5mV TO 50V)
505k
0.1%
2
3
1
1/4 LT1079
220pF
Q2
30k
5%
Q4
9
10
8
1/4 LT1079
OUTPUT
(5mV TO 8V)

Q1–Q4 = MAT−04

$OUTPUT = \frac{(X)(Y)}{(Z)}$, POSITIVE INPUTS ONLY

TYPICAL LINEARITY = 0.01% OF FULL SCALE OUTPUT

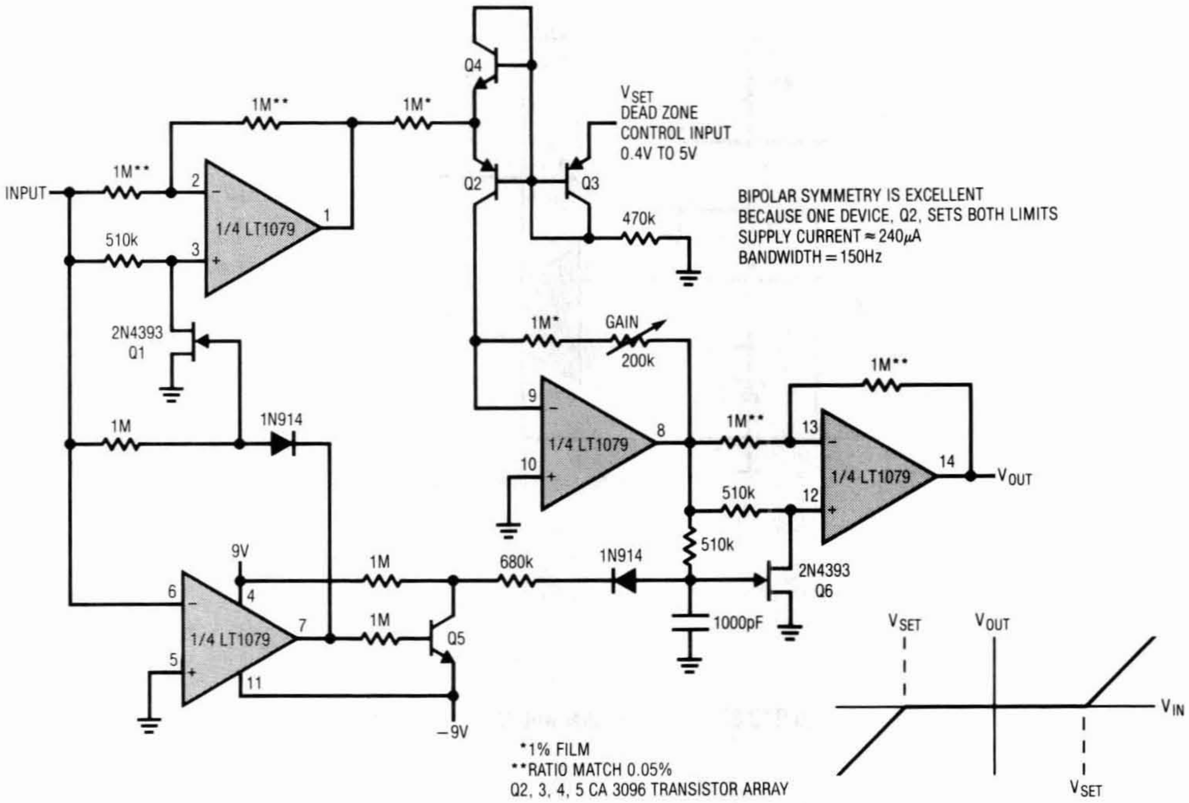
$NEGATIVE\ SUPPLY\ CURRENT = 165\mu A + \frac{X+Y+Z+OUT}{500k}$

$POSITIVE\ SUPPLY\ CURRENT = 165\mu A + \frac{OUT}{500k}$

BANDWIDTH (< $3V_{pp}$ SIGNAL): X AND Y INPUTS = 10kHz
Z INPUT = 4kHz

TYPICAL APPLICATIONS

Micropower Dead Zone Generator

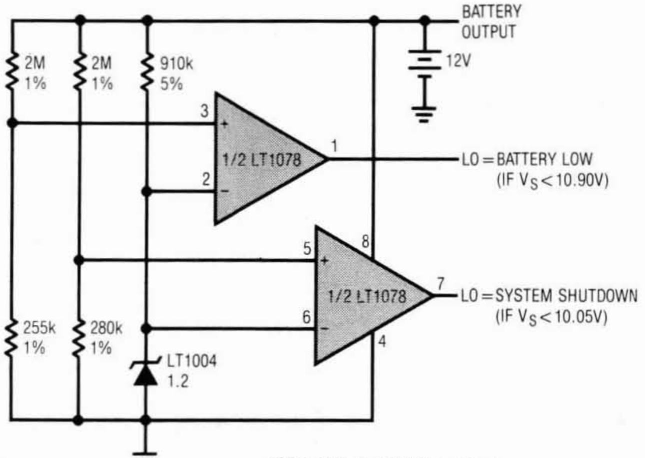

INPUT
1M**
1M**
1M*
510k
2
3
1
1/4 LT1079
Q4
Q2
Q3
VSET
DEAD ZONE
CONTROL INPUT
0.4V TO 5V
470k
2N4393
Q1
1M
1N914
1M*
GAIN
200k
9
10
8
1/4 LT1079
1M**
1M**
510k
13
12
14
1/4 LT1079
VOUT
510k
2N4393
Q6
1000pF
9V
6
4
5
7
11
1/4 LT1079
1M
1M
680k
1N914
Q5
−9V
VSET
VOUT
VIN
VSET

BIPOLAR SYMMETRY IS EXCELLENT
BECAUSE ONE DEVICE, Q2, SETS BOTH LIMITS
SUPPLY CURRENT ≈ 240μA
BANDWIDTH = 150Hz

*1% FILM
**RATIO MATCH 0.05%
Q2, 3, 4, 5 CA 3096 TRANSISTOR ARRAY

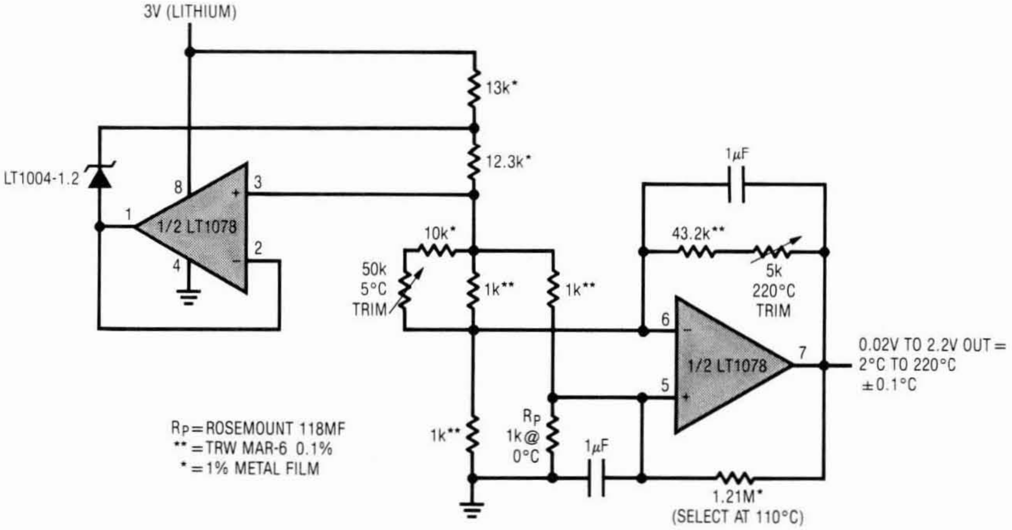
TYPICAL APPLICATIONS

Lead Acid Low Battery Detector with System Shutdown


BATTERY OUTPUT
12V
2M 1%
2M 1%
910k 5%
3
2
1/2 LT1078
1
LO = BATTERY LOW (IF V_S < 10.90V)
5
6
8
4
1/2 LT1078
7
LO = SYSTEM SHUTDOWN (IF V_S < 10.05V)
255k 1%
280k 1%
LT1004 1.2

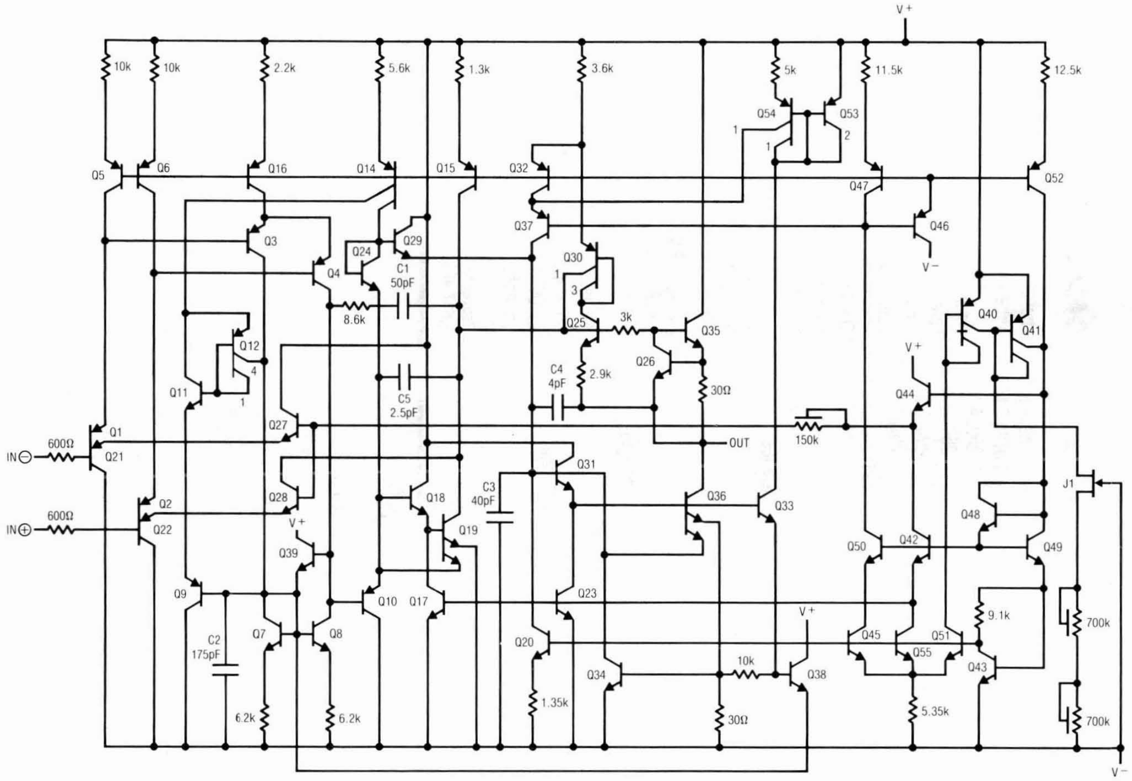
TOTAL SUPPLY CURRENT ≈ 105μA

Platinum RTD Signal Conditioner with Curvature Correction


3V (LITHIUM)
13k*
12.3k*
LT1004-1.2
8
3
1
1/2 LT1078
2
4
10k*
50k 5°C TRIM
1k**
1k**
1μF
43.2k**
5k 220°C TRIM
6
5
1/2 LT1078
7
0.02V TO 2.2V OUT = 2°C TO 220°C ±0.1°C
1k**
R_P 1k@ 0°C
1μF
1.21M* (SELECT AT 110°C)

R_P = ROSEMOUNT 118MF
** = TRW MAR-6 0.1%
* = 1% METAL FILM

SIMPLIFIED SCHEMATIC


1/2 LT1078
1/4 LT1079
V+
10k
10k
2.2k
5.6k
1.3k
3.6k
5k
11.5k
12.5k
Q54
Q53
1
1
2
Q5
Q6
Q16
Q14
Q15
Q32
Q47
Q52
Q46
V−
Q3
Q29
Q37
Q24
Q4
C1
50pF
Q30
1
3
8.6k
Q25
3k
Q35
Q40
Q41
Q12
4
1
C5
2.5pF
C4
4pF
2.9k
Q26
30Ω
V+
Q44
Q11
Q1
Q21
Q27
150k
OUT
IN⊖
600Ω
IN⊕
600Ω
Q2
Q22
Q28
Q18
C3
40pF
Q31
Q36
Q33
J1
Q48
Q19
V+
Q39
Q50
Q42
Q49
Q9
Q10
Q17
Q23
9.1k
700k
C2
175pF
Q7
Q8
Q20
V+
Q45
Q51
Q55
Q43
10k
Q34
Q38
6.2k
6.2k
1.35k
30Ω
5.35k
700k
V−

LT1097

Low Cost, Low Power Precision Op Amp

FEATURES

■ Offset Voltage	50μV Max
■ Offset Voltage Drift	1.0μV/°C Max
■ Bias Current	250pA Max
■ Offset Current	250pA Max
■ Bias and Offset Current Drift	4pA/°C Max
■ Supply Current	560μA Max
■ 0.1Hz to 10Hz Noise	0.5μVp-p, 2.2pAp-p
■ CMRR	115dB Min
■ Voltage Gain	117dB Min
■ PSRR	114dB Min
■ *Guaranteed* Operation on Two NiCad Batteries	
■ Price (1000's) for Above Specs	$0.97

APPLICATIONS

- Replaces OP-07/OP-77/OP-97/OP-177/AD707/LT1001 with Improved Price/Performance
- High Impedance Difference Amplifiers
- Logarithmic Amplifiers (Wide Dynamic Range)
- Thermocouple Amplifiers
- Precision Instrumentation
- Active Filters (with Small Capacitors)

DESCRIPTION

The LT1097 achieves a new standard in combining low price and outstanding precision performance.

On all operational amplifier datasheets, the specifications listed on the front page are for highly selected, expensive grades, while the specs for the low cost grades are buried deep in the datasheet.

The LT1097 does not have any selected grades, the outstanding specifications shown in the features section are for its only grade — priced at 97 cents in thousands.

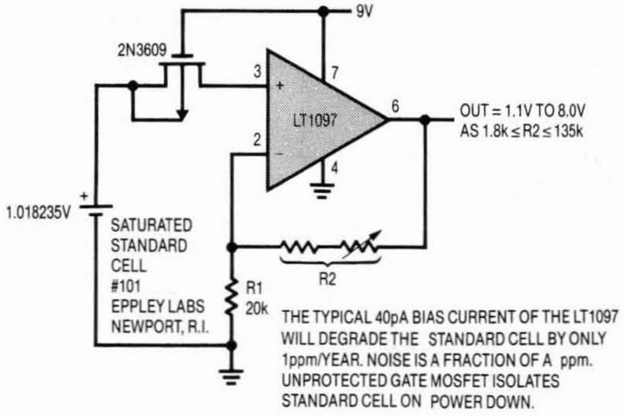
The design effort of the LT1097 concentrated on optimizing the performance of all precision specs — at only 350μA of supply current. Typical values are 10μV offset voltage, 40pA bias and offset currents, 0.2μV/°C and 0.4pA/°C drift. Common mode and power supply rejections, voltage gain are typically in excess of 128dB.

All parameters that are important for precision, low power op amps have been optimized. Consequently, using the LT1097, error budget calculations in most applications are unnecessary.

Protected by U.S. patents 4,575,685; 4,775,884 and 4,837,496

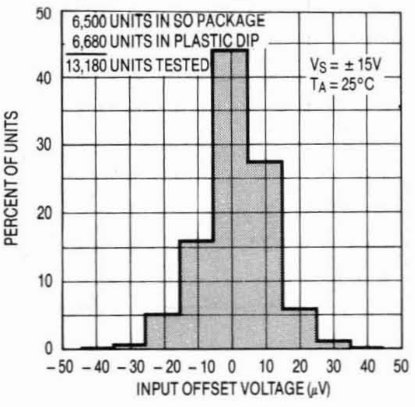
TYPICAL APPLICATION

Saturated Standard Cell Amplifier



THE TYPICAL 40pA BIAS CURRENT OF THE LT1097 WILL DEGRADE THE STANDARD CELL BY ONLY 1ppm/YEAR. NOISE IS A FRACTION OF A ppm. UNPROTECTED GATE MOSFET ISOLATES STANDARD CELL ON POWER DOWN.

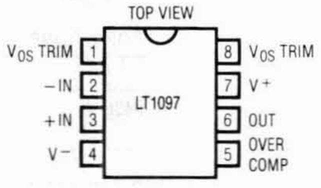
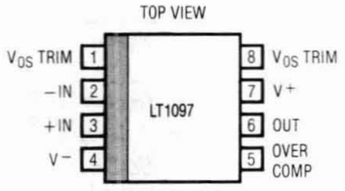
Input Offset Voltage Distribution



ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ± 20V
Differential Input Current (Note 1) .... ± 10mA
Input Voltage .... ± 20V
Output Short Circuit Duration .... Indefinite
Operating Temperature Range .... – 40°C to 85°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW V_{OS} TRIM 1 –IN 2 +IN 3 V– 4 LT1097 8 V_{OS} TRIM 7 V+ 6 OUT 5 OVER COMP N PACKAGE 8-LEAD PLASTIC DIP	LT1097CN8
 TOP VIEW V_{OS} TRIM 1 –IN 2 +IN 3 V– 4 LT1097 8 V_{OS} TRIM 7 V+ 6 OUT 5 OVER COMP SO PACKAGE 8-LEAD PLASTIC SOIC	LT1097S8 PART MARKING 1097

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless noted.

			LT1097CN8			LT1097S8			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage			10	50		10	60	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		μV/Mo
I_{OS}	Input Offset Current			40	250		60	350	pA
I_B	Input Bias Current			± 40	± 250		± 50	± 350	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μVp-p
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 1000Hz$		16 14			16 14		nV/√Hz nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz		2.2			2.4		pAp-p
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 1000Hz$		0.030 0.008			0.035 0.008		pA/√Hz pA/√Hz
	Input Resistance Differential Mode Common-Mode	(Note 2)	30	80 10^{12}		25	70 8×10^{11}		MΩ Ω
	Input Voltage Range		± 13.5	± 14.3		± 13.5	± 14.3		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	115	130		115	130		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.2V$ to $\pm 20V$	114	130		114	130		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 12V$, $R_L = 10k$ $V_O = \pm 10V$, $R_L = 2k$	700 250	2500 1000		700 250	2500 1000		V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 10k$ $R_L = 2k$	± 13 ± 11.5	± 13.8 ± 13.0		± 13 ± 11.5	± 13.8 ± 13.0		V V
SR	Slew Rate		0.1	0.2		0.1	0.2		V/μs
GBW	Gain Bandwidth Product			700			700		kHz
I_S	Supply Current			350	560		350	560	μA
	Offset Adjustment Range	$R_{pot} = 10k$, Wiper to V+		± 600			± 600		μV
	Minimum Supply Voltage	(Note 3)	± 1.2	—		± 1.2	—		V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

				LT1097CN8			LT1097S8			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage		●		20	100		20	130	μV
	Average Temperature Coefficient of Input Offset Voltage	(Note 4)	●		0.2	1.0		0.2	1.4	μV/°C
I_{OS}	Input Offset Current		●		60	430		75	570	pA
	Average Temperature Coefficient of Input Offset Current	(Note 4)	●		0.4	4		0.5	5	pA/°C
I_B	Input Bias Current		●		±60	±430		±75	±570	pA
	Average Temperature Coefficient of Input Bias Current	(Note 4)	●		0.4	4		0.5	5	pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \ge 10k\Omega$	●	450	2000		450	2000		V/mV
		$V_{OUT} = \pm 10V$, $R_L \ge 2k\Omega$	●	180	800		180	800		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	112	128		112	128		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.3V$ to $\pm 20V$	●	111	128		111	128		dB
	Input Voltage Range		●	±13.5	±14.2		±13.5	±14.2		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±13.7		±13	±13.7		V
I_S	Supply Current		●		380	700		380	700	μA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 5)

				LT1097CN8			LT1097S8			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage		●		25	130		30	170	μV
	Average Temperature Coefficient of Input Offset Voltage		●		0.3	1.2		0.3	1.6	μV/°C
I_{OS}	Input Offset Current		●		70	600		85	750	pA
	Average Temperature Coefficient of Input Offset Current		●		0.5	5		0.6	6	pA/°C
I_B	Input Bias Current		●		±70	±600		±85	±750	pA
	Average Temperature Coefficient of Input Bias Current		●		0.5	5		0.6	6	pA/°C
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L \ge 10k\Omega$	●	300	1700		300	1700		V/mV
		$V_{OUT} = \pm 10V$, $R_L \ge 2k\Omega$	●		700			700		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	●	108	127		108	127		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 1.5V$ to $\pm 20V$	●	108	127		108	127		dB
	Input Voltage Range		●	±13.5	±14.0		±13.5	±14.0		V
V_{OUT}	Output Voltage Swing	$R_L = 10k\Omega$	●	±13	±13.6		±13	±13.6		V
I_S	Supply Current		●		400	800		400	800	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Differential input voltages greater than 1V will cause excessive current to flow through the input protection diodes unless limiting resistance is used.

Note 2: This parameter is guaranteed by design and is not tested.

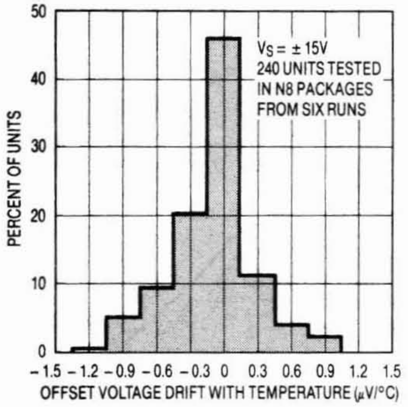
Note 3: Power supply rejection ratio is measured at the minimum supply voltage.

Note 4: This parameter is not 100% tested.

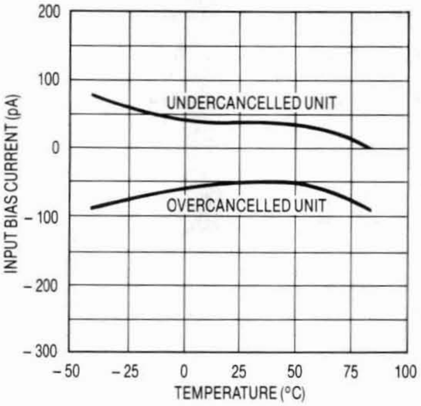
Note 5: The LT1097 is not tested and is not quality-assurance-sampled at −40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from 0°C, 25°C and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

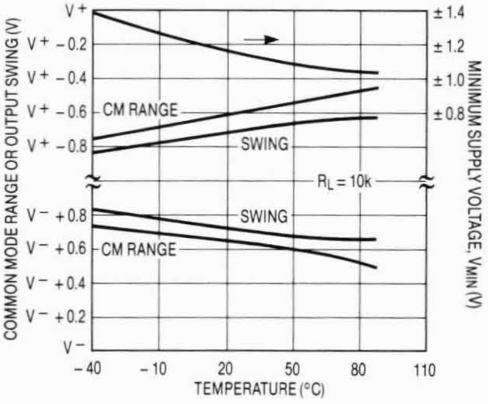
Distribution of Offset Voltage Drift with Temperature



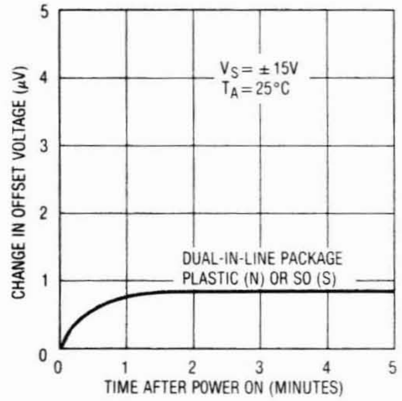
Input Bias Current vs Temperature



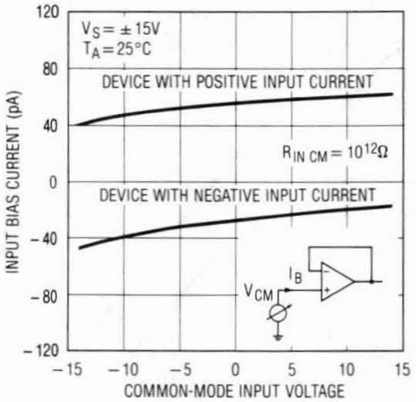
Minimum Supply Voltage, Common Mode Range and Voltage Swing at V_{MIN}



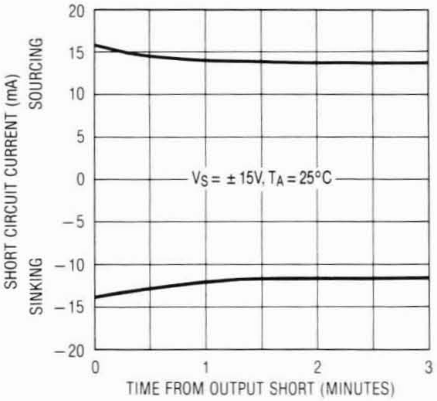
Warm-Up Drift



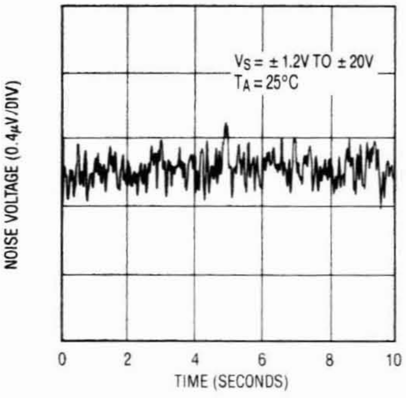
Input Bias Current Over Common Mode Range



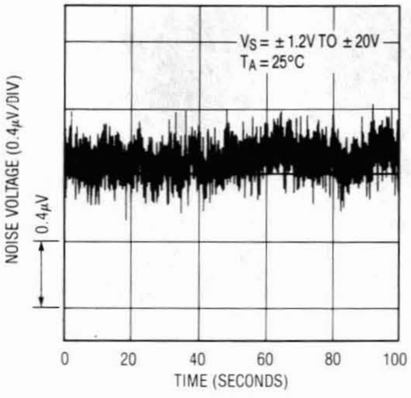
Output Short Circuit Current vs Time



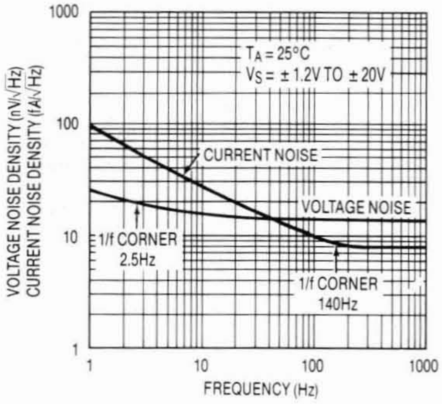
0.1Hz to 10Hz Noise



0.01Hz to 10Hz Noise

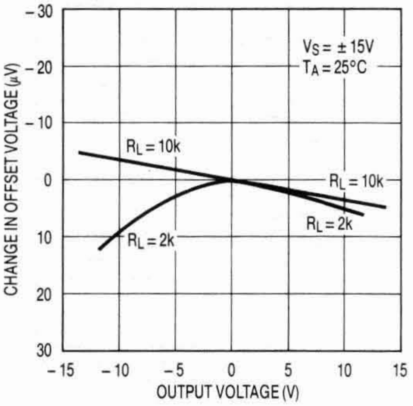


Noise Spectrum

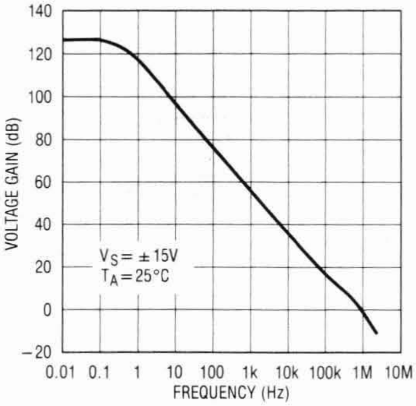


TYPICAL PERFORMANCE CHARACTERISTICS

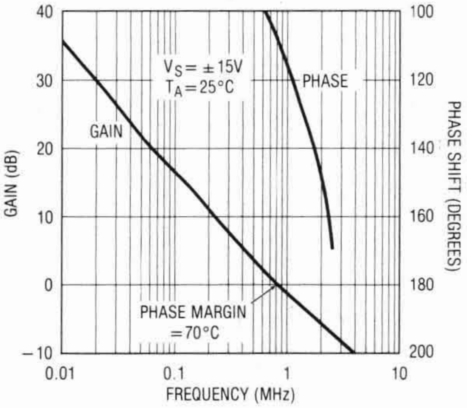
Voltage Gain



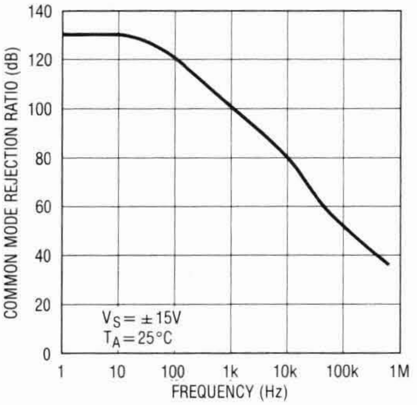
Voltage Gain vs Frequency



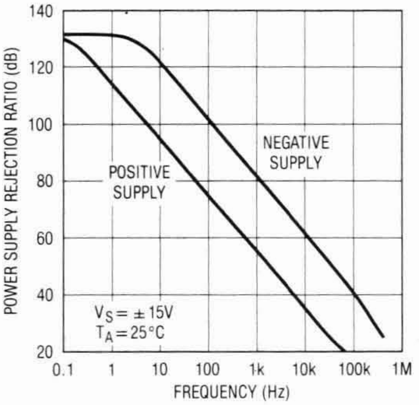
Gain, Phase Shift vs Frequency



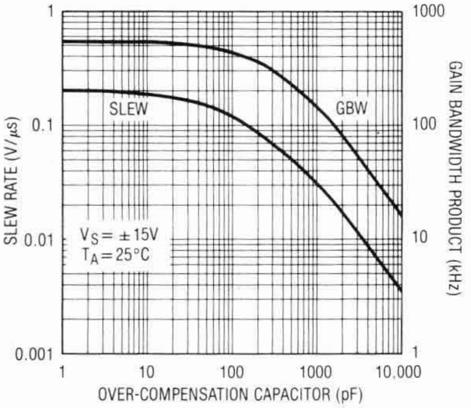
Common Mode Rejection vs Frequency



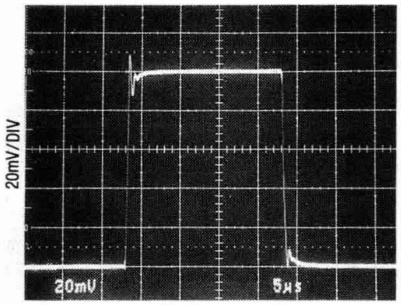
Power Supply Rejection vs Frequency



Slew Rate, Gain Bandwidth Product vs Over-Compensation Capacitor

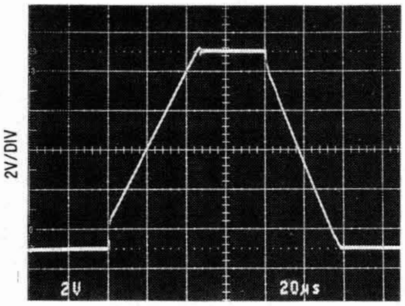


Small Signal Transient Response



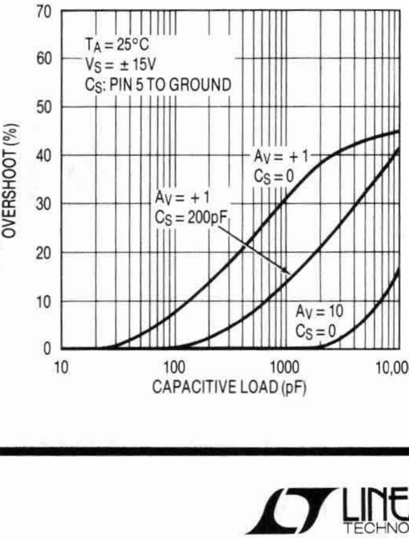
$A_V = +1$, $C_{LOAD} = 100pF$, 5μs/DIV

Large Signal Transient Response



$A_V = +1$, 20μs/DIV

Capacitive Load Handling

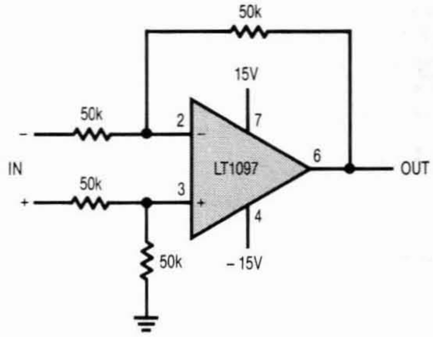


APPLICATIONS INFORMATION

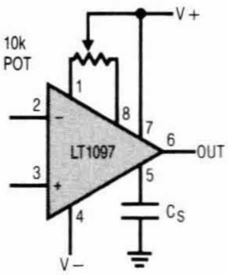
The LT1097 is pin compatible to, and directly replaces such precision op amps as the OP-07, OP-77, AD707, OP-97, OP-177, LM607, and LT1001 with improved price/performance. Compatibility includes externally nulling the offset voltage, as all of the above devices are trimmed with a potentiometer between pins 1 and 8 and the wiper tied to V+.

The simple difference amplifier can be used to illustrate the all-around excellence of the LT1097. The 50k input resistance is selected to be large enough compared to input signal source resistances. Simultaneously, the 50k resistors should not dominate the precision and noise error budget. Assuming perfect matching between the four resistors, the following table summarizes the input referred performance obtained using the LT1097 and other popular, low-cost precision op amps.

± 27V Common Mode Range Difference Amplifier



Frequency Compensation and Optional Offset Nulling



Input offset voltage can be adjusted over a ± 600μV range with a 10k potentiometer.

The LT1097 is internally compensated for unity gain stability. As shown on the Capacitive Load Handling plot, the LT1097 is stable with any capacitive load. However, the overcompensation capacitor, C_S, can be used to reduce overshoot with heavy capacitive loads, to narrow noise bandwidth, or to stabilize circuits with gain in the feedback loop.

Guaranteed Performance, $V_S = \pm 15V$, $T_A = 25°C$

PARAMETER/UNITS	LT1097CN8	OP-77GP	AD707JN	OP-177GP	OP-97FP
Error Terms in μV					
V_{OS} Max	50	100	90	60	75
I_{OS} Max x 25k	6	70	50	70	4
Gain Min, 10V Out	14	5	3	5	50
CMRR, Min, ± 25V In	22	20	13	22	39
PSRR, Min, $V_S = \pm 15V \pm 10\%$	6	9	9	9	9
Sum of All Error Terms, μV	98	204	165	166	177
0.1Hz to 10Hz Noise, μVp-p Typ					
Voltage Noise	0.50	0.38	0.23	0.38	0.50
Current Noise x 50k	0.11	0.75	0.70	0.75	0.10
Resistor Noise	0.55	0.55	0.55	0.55	0.55
RMS Sum μVp-p	0.75	1.00	0.92	1.00	0.75
Drift with Temp, μV/°C					
TCV_{OS} Max	1.0	1.2	1.0	1.2	2.0
TCI_{OS} Max x 25k	0.1	2.1	1.0	2.1	0.2
Sum of Drift Terms μV/°C	1.1	3.3	2.0	3.3	2.2
Supply Current Max, mA	0.56	2.0	3.0	2.0	0.60
Price, 1000's, $	0.97	SIMILAR OR HIGHER			HIGHER

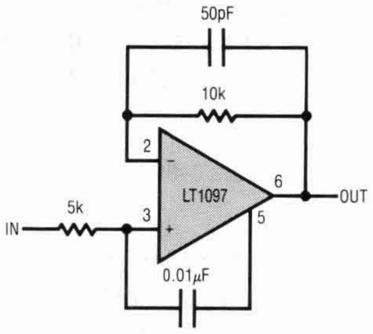
APPLICATIONS INFORMATION

The availability of the compensation terminal permits the use of feedforward frequency compensation to enhance slew rate. The voltage follower feedforward scheme bypasses the amplifier's gain stages and slews at nearly 10V/μs.

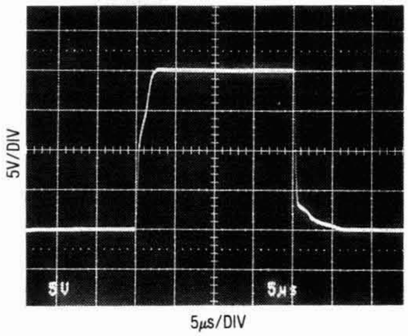
The inputs of the LT1097 are protected with back-to-back diodes. In the voltage follower configuration, when the input is driven by a fast, large signal pulse (>1V), the input protection diodes effectively short the output to the input during slewing, and a current, limited only by the output short circuit protection will flow through the diodes.

The use of a feedback resistor, as shown in the voltage follower feedforward diagram, is recommended because this resistor keeps the current below the short circuit limit, resulting in faster recovery and settling of the output.

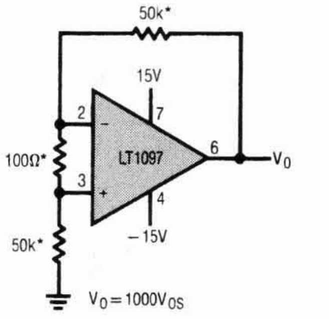
Follower Feedforward Compensation


50pF
10k
2
LT1097
6
OUT
5k
IN
3
5
0.01μF

Pulse Response of Feedforward Compensation



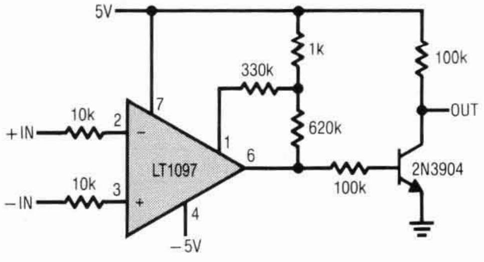
Test Circuit for Offset Voltage and its Drift with Temperature


50k*
15V
2
7
100Ω*
LT1097
6
V_O
3
4
−15V
50k*
$V_O = 1000V_{OS}$

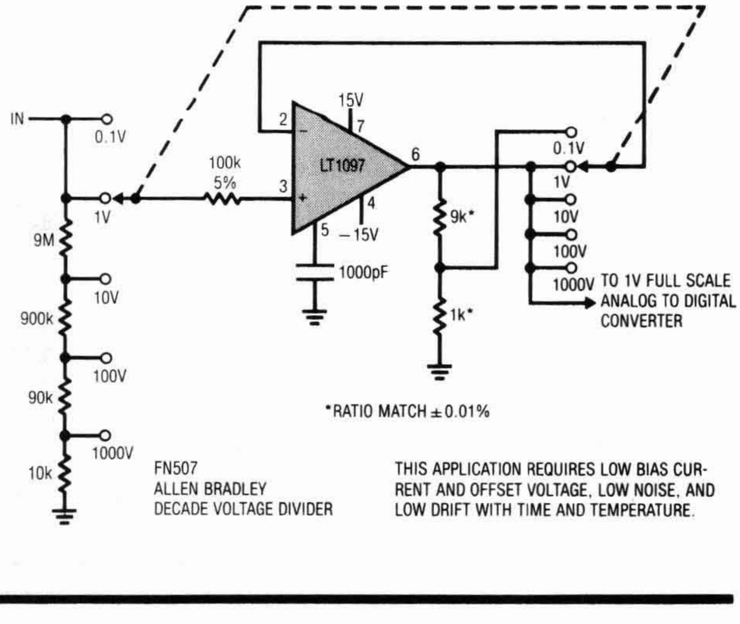
*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL

TYPICAL APPLICATIONS

Low Power Comparator with <10μV Hysteresis


5V
1k
100k
330k
OUT
10k
+IN
2
7
620k
1
6
LT1097
2N3904
100k
10k
−IN
3
4
−5V

Input Amplifier for 4 1/2 Digit Voltmeter

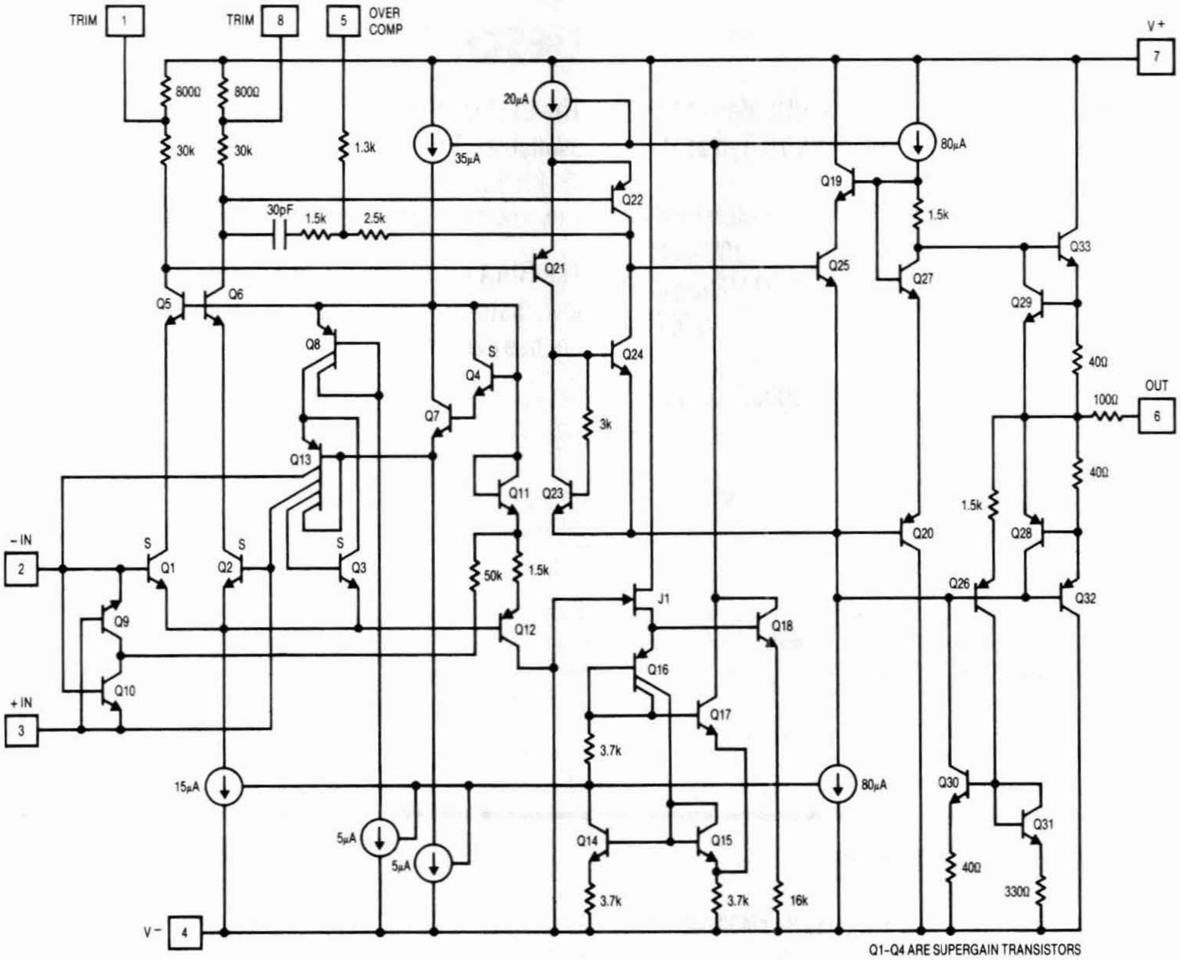

IN
0.1V
15V
2
7
LT1097
6
100k
5%
3
1V
4
5
−15V
9k*
0.1V
1V
10V
100V
1000V
1000pF
9M
10V
900k
1k*
100V
90k
1000V
10k
TO 1V FULL SCALE ANALOG TO DIGITAL CONVERTER

*RATIO MATCH ±0.01%

FN507
ALLEN BRADLEY
DECADE VOLTAGE DIVIDER

THIS APPLICATION REQUIRES LOW BIAS CURRENT AND OFFSET VOLTAGE, LOW NOISE, AND LOW DRIFT WITH TIME AND TEMPERATURE.

SCHEMATIC DIAGRAM


TRIM 1
TRIM 8
5 OVER COMP
V+ 7
800Ω
800Ω
30k
30k
1.3k
30pF
1.5k
2.5k
20μA
35μA
80μA
15μA
5μA
5μA
80μA
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
J1
S
S
S
S
−IN 2
+IN 3
V− 4
OUT 6
100Ω
40Ω
40Ω
1.5k
1.5k
1.5k
50k
3k
3.7k
3.7k
3.7k
16k
40Ω
330Ω

Q1–Q4 ARE SUPERGAIN TRANSISTORS

LINEAR TECHNOLOGY

LT1115

Ultra-Low Noise, Low Distortion, Audio Op Amp

FEATURES

■ Voltage Noise	1.2nV/√Hz Max at 1kHz 0.9nV/√Hz Typ at 1kHz
■ Voltage and Current Noise 100% Tested	
■ Gain-Bandwidth Product	40MHz Min
■ Slew Rate	10V/μs Min
■ Voltage Gain	2 Million Min
■ Low THD@10kHz, $A_V = -10$, $R_L = 600\Omega$, $V_O = 7V_{RMS}$	0.002%
■ Low IMD, CCIF Method, $A_V = +10$, $R_L = 600\Omega$, $V_O = 7V_{RMS}$	0.0002%

APPLICATIONS

- High Quality Audio Preamplifiers
- Low Noise Microphone Preamplifiers
- Very Low Noise Instrumentation Amplifiers
- Low Noise Frequency Synthesizers
- Infrared Detector Amplifiers
- Hydrophone Amplifiers
- Low Distortion Oscillators

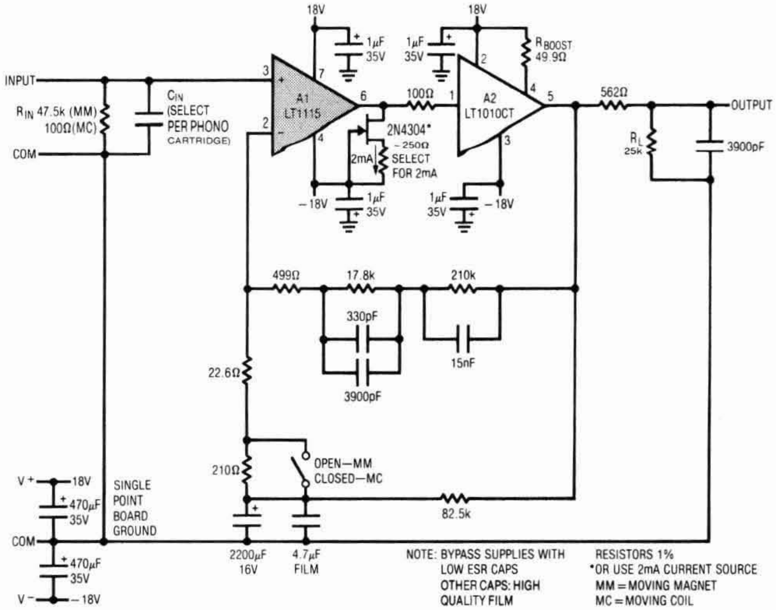
DESCRIPTION

The LT1115 is the lowest noise audio operational amplifier available. This ultra-low noise performance (0.9nV/√Hz @1kHz) is combined with high slew rates (>15V/μs) and very low distortion specifications.

The RIAA circuit shown below using the LT1115 has very low distortion and little deviation from ideal RIAA response (see graph).

TYPICAL APPLICATION

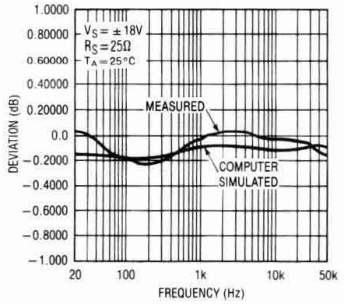
RIAA Phonograph Preamplifier (40/60db Gain)


18V
18V
1μF 35V
1μF 35V
R BOOST 49.9Ω
INPUT
R IN 47.5k (MM) 100Ω(MC)
C IN (SELECT PER PHONO CARTRIDGE)
COM
3
2
7
4
A1 LT1115
6
100Ω
1
2
A2 LT1010CT
4
5
3
2N4304*
~250Ω SELECT FOR 2mA
2mA
−18V
1μF 35V
1μF 35V
−18V
562Ω
OUTPUT
R L 25k
3900pF
499Ω
17.8k
210k
330pF
3900pF
15nF
22.6Ω
210Ω
OPEN—MM
CLOSED—MC
82.5k
V+ 18V
470μF 35V
SINGLE POINT BOARD GROUND
COM
470μF 35V
V− −18V
2200μF 16V
4.7μF FILM

NOTE: BYPASS SUPPLIES WITH LOW ESR CAPS
OTHER CAPS: HIGH QUALITY FILM

RESISTORS 1%
*OR USE 2mA CURRENT SOURCE
MM = MOVING MAGNET
MC = MOVING COIL

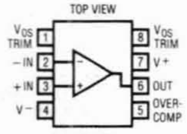
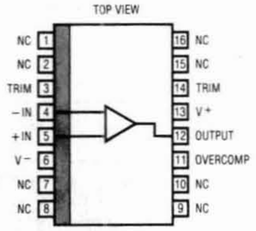
Measured Deviation from RIAA Response. Input@1kHz = 1mV$_{RMS}$ Pre-Emphasized.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Differential Input Current (Note 4)	±25mA
Input Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW V_{OS} TRIM 1 −IN 2 +IN 3 V− 4 8 V_{OS} TRIM 7 V+ 6 OUT 5 OVER-COMP N PACKAGE 8-LEAD PLASTIC DIP	LT1115CN8
 TOP VIEW NC 1 NC 2 TRIM 3 −IN 4 +IN 5 V− 6 NC 7 NC 8 16 NC 15 NC 14 TRIM 13 V+ 12 OUTPUT 11 OVERCOMP 10 NC 9 NC S PACKAGE 16-LEAD PLASTIC SOL	LT1115CS

ELECTRICAL CHARACTERISTICS $V_S = \pm 18V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1115C MIN	LT1115C TYP	LT1115C MAX	UNITS
THD	Total Harmonic Distortion @ 10kHz	$A_V = -10$, $V_O = 7V_{RMS}$, $R_L = 600$		<0.002		%
IMD	Inter-Modulation Distortion (CCIF)	$A_V = 10$, $V_O = 7V_{RMS}$, $R_L = 600$		<0.0002		%
V_{OS}	Input Offset Voltage	(Note 1)		50	200	μV
I_{OS}	Input Offset Current	$V_{CM} = 0V$		30	200	nA
I_B	Input Bias Current	$V_{CM} = 0V$		±50	±380	nA
e_n	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 1000Hz$, 100% tested		1.0 0.9	 1.2	nV/√Hz nV/√Hz
	Wideband Noise	DC to 20kHz		120		nV_{RMS}
	Corresponding Voltage Level re 0.775V			−136		dB
i_n	Input Noise Current Density (Note 2)	$f_o = 10Hz$ $f_o = 1000Hz$, 100% tested		4.7 1.2	 2.2	pA/√Hz pA/√Hz
	Input Resistance Common-Mode Differential Mode			 250 15		 MΩ kΩ
	Input Capacitance			5		pF
	Input Voltage Range		±13.5	±15.0		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	104	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 19V$	104	126		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_o = \pm 14.5V$ $R_L \geq 1k\Omega$, $V_o = \pm 13V$ $R_L \geq 600\Omega$, $V_o = \pm 10V$	2.0 1.5 1.0	20 15 10		V/μV V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	No Load $R_L \geq 2k\Omega$ $R_L \geq 600\Omega$	±15.5 ±14.5 ±11.0	±16.5 ±15.5 ±14.5		V V V
SR	Slew Rate	$A_{VCL} = -1$	10	15		V/μs
GBW	Gain-Bandwidth Product	$f_o = 20kHz$ (Note 3)	40	70		MHz
Z_o	Open Loop Output Impedance	$V_o = 0$, $I_o = 0$		70		Ω
I_S	Supply Current			8.5	11.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 18V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1115C MIN	 TYP	 MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 1)	●		75	280	μV
$\Delta V_{OS}/\Delta T$	Average Input Offset Drift				0.5		μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		40	300	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±70	±550	nA
	Input Voltage Range		●	±13	±14.8		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	100	123		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 2k\Omega$, $V_o = \pm 13V$ $R_L \ge 1k\Omega$, $V_o = \pm 11V$	●	1.5 1.0	15 10		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	No Load $R_L \ge 2k\Omega$ $R_L \ge 600\Omega$	●	±15 ±13.8 ±10	±16.3 ±15.3 ±14.3		V V V
I_S	Supply Current		●		9.3	13	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power.

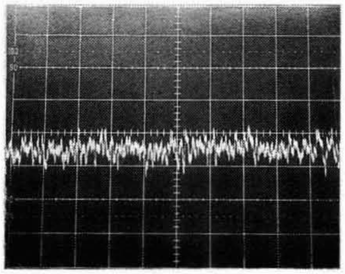
Note 2: Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise.

Note 3: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

Note 4: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.8V, the input current should be limited to 25mA.

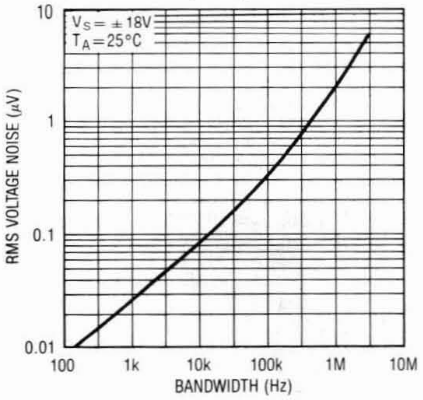
TYPICAL PERFORMANCE CHARACTERISTICS

Wideband Noise, DC to 20kHz

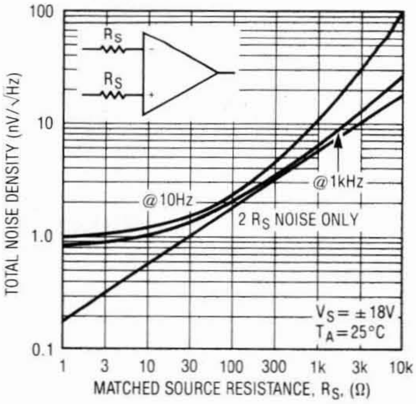


VERTICAL SCALE = 0.5μV/DIV
HORIZONTAL SCALE = 0.5ms/DIV

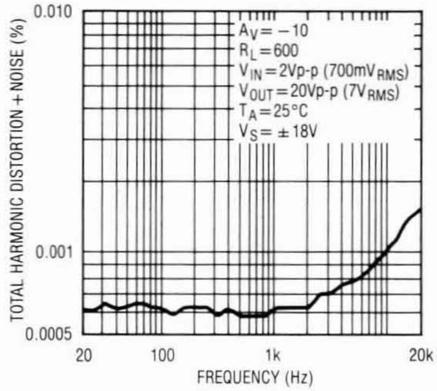
Wideband Voltage Noise (0.1Hz to Frequency Indicated)

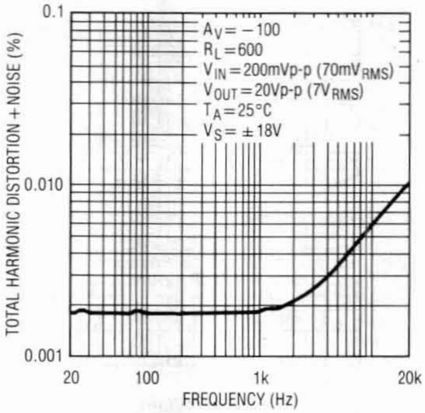


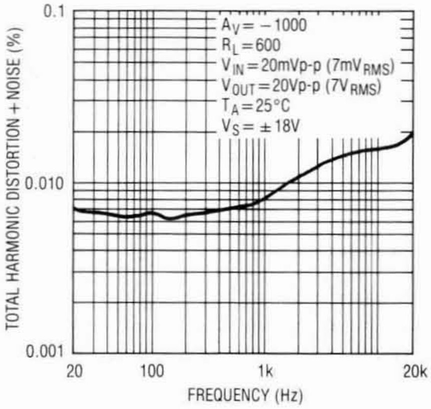
Total Noise vs Matched Source Resistance

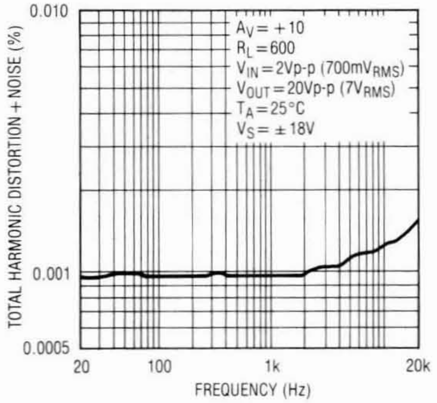


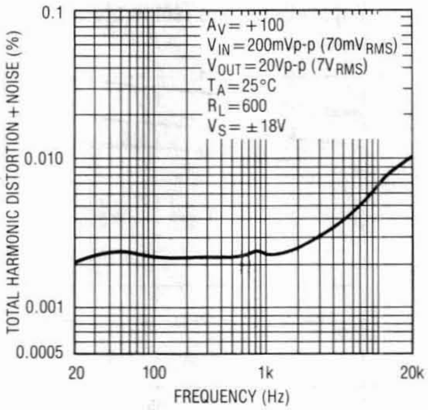
TYPICAL PERFORMANCE CHARACTERISTICS

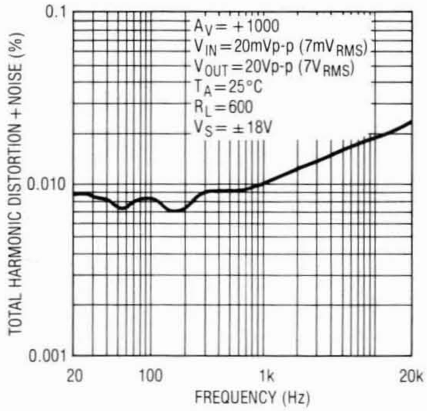

THD + Noise vs Frequency ($A_V = -10$)

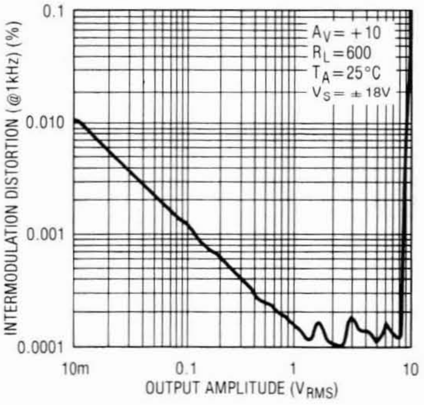

THD + Noise vs Frequency ($A_V = -100$)

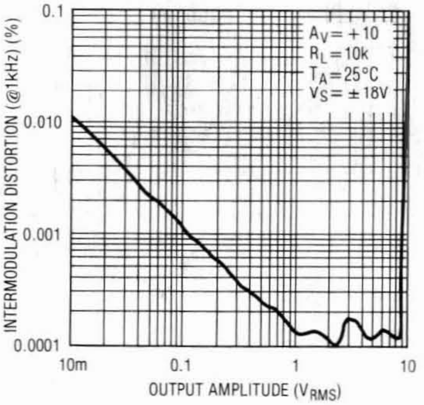

THD + Noise vs Frequency ($A_V = -1000$)

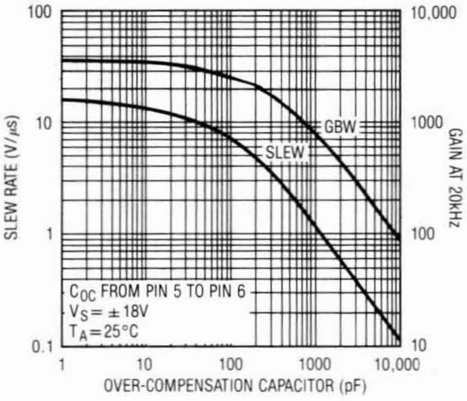

THD + Noise vs Frequency ($A_V = +10$)


THD + Noise vs Frequency ($A_V = +100$)


THD + Noise vs Frequency ($A_V = +1000$)


CCIF IMD Test (Twin Equal Amplitude Tones at 13 and 14kHz)*

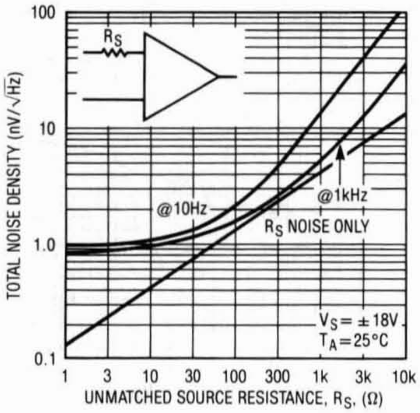

CCIF IMD Test (Twin Equal Amplitude Tones at 13 and 14kHz)*


Slew Rate, Gain-Bandwidth-Product vs Over-Compensation Capacitor

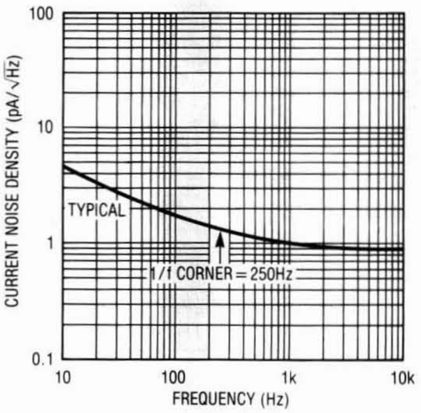
*See CCIF Test Note at end of "Typical Performance Characteristics."

TYPICAL PERFORMANCE CHARACTERISTICS

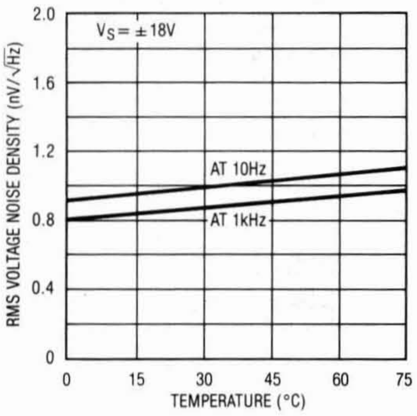
Total Noise vs Unmatched Source Resistance



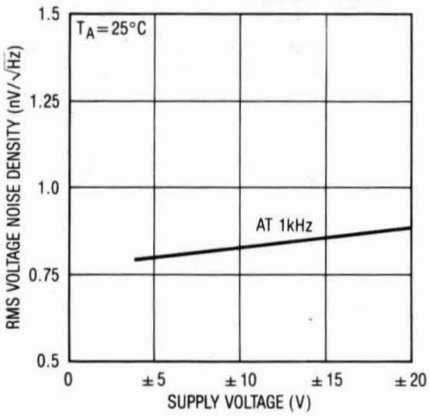
Current Noise Spectrum



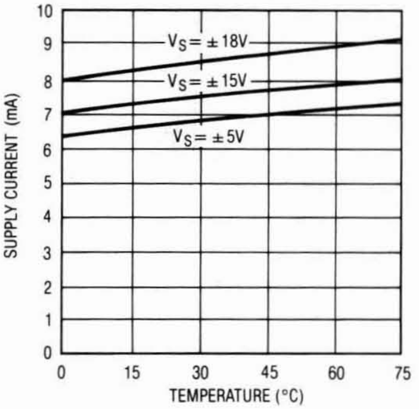
Voltage Noise vs Temperature



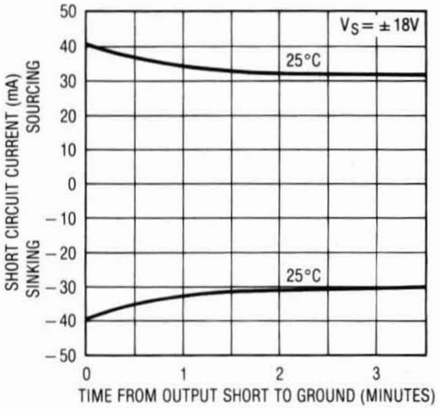
Voltage Noise vs Supply Voltage



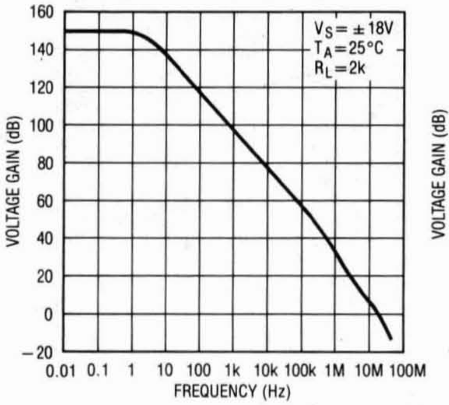
Supply Current vs Temperature



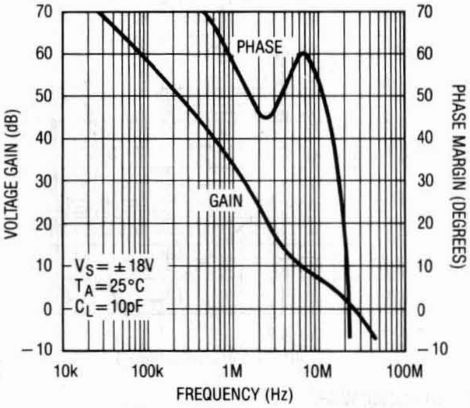
Output Short Circuit Current vs Time



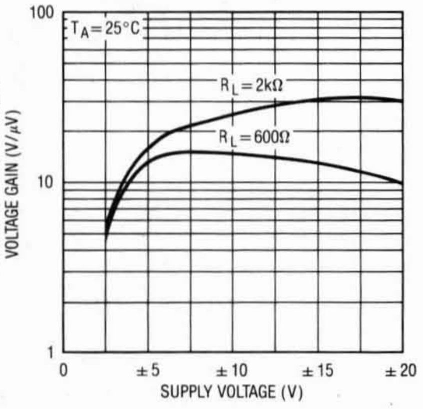
Voltage Gain vs Frequency



Gain, Phase vs Frequency

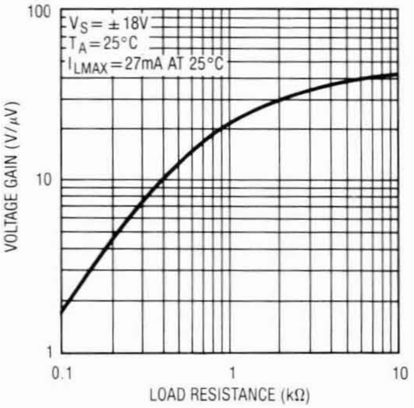


Voltage Gain vs Supply Voltage

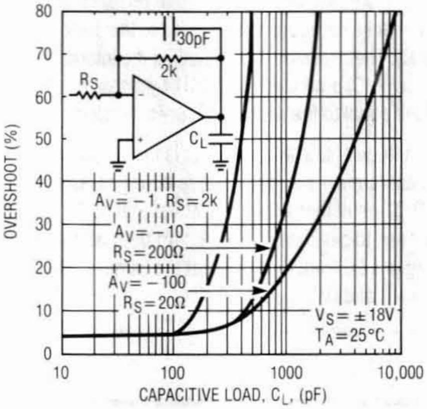


TYPICAL PERFORMANCE CHARACTERISTICS

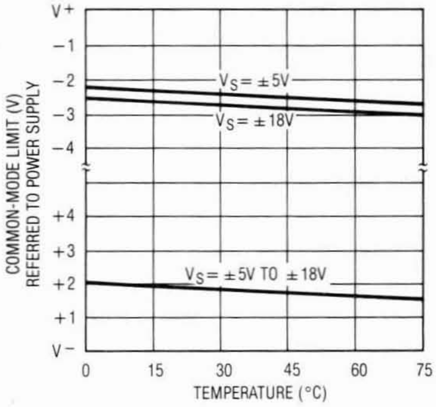
Voltage Gain vs Load Resistance



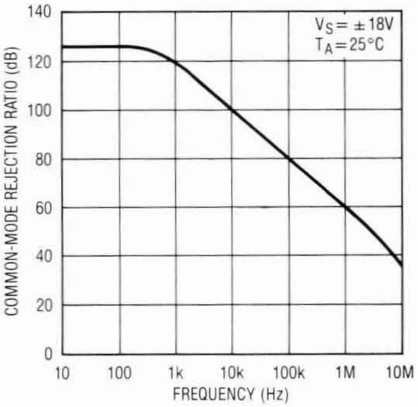
Capacitance Load Handling



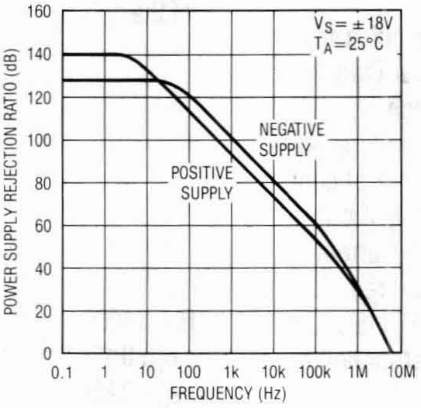
Common-Mode Limit Over Temperature



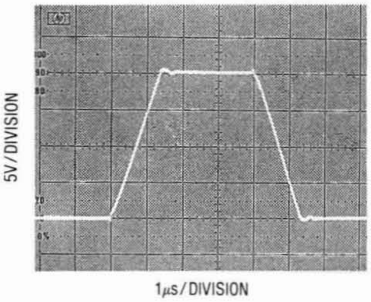
Common-Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency

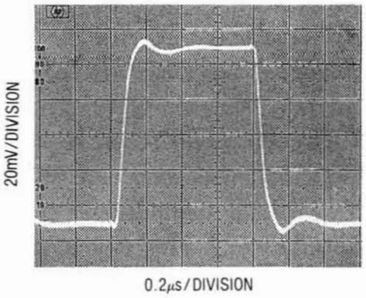


Large Signal Transient Response



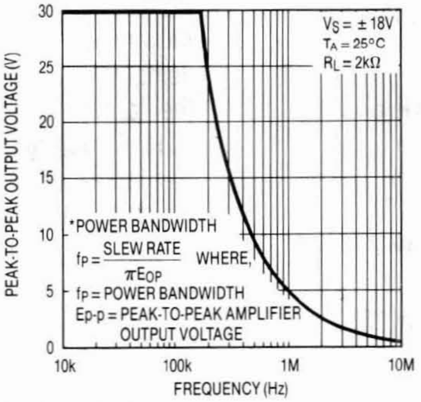
$A_V = -1, R_S = R_f = 2k, C_f = 30pF$

Small Signal Transient Response



$A_V = -1, R_S = R_f = 2kΩ$
$C_f = 30pF, C_L = 80pF$

Maximum Output vs Frequency (Power Bandwidth*)



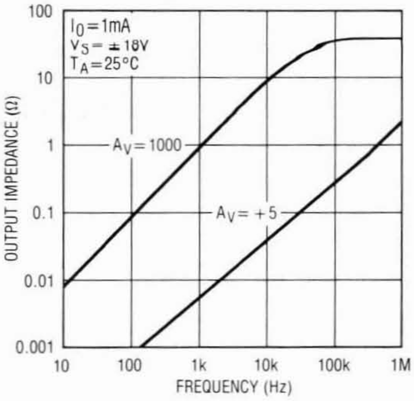
*POWER BANDWIDTH

$f_P = \frac{\text{SLEW RATE}}{\pi E_{OP}}$ WHERE,

f_P = POWER BANDWIDTH

$E_{P\text{-}P}$ = PEAK-TO-PEAK AMPLIFIER OUTPUT VOLTAGE

Closed Loop Output Impedance



TYPICAL PERFORMANCE CHARACTERISTICS

CCIF Testing

Note: The CCIF twin-tone intermodulation test inputs two closely spaced equal amplitude tones to the device under test (DUT). The analyzer then measures the intermodulation distortion (IMD) produced in the DUT by measuring the difference tone equal to the spacing between the tones.

The amplitude of the IMD test input is in sinewave peak equivalent terms. As an example, selecting an amplitude of 1.000V will result in the complex IMD signal having the same 2.828V peak-to-peak amplitude that a 1.000V sinewave has. Clipping in a DUT will thus occur at the same input amplitude for THD + N and IMD modes.

APPLICATIONS INFORMATION —NOISE

Voltage Noise vs Current Noise

The LT1115's less than 1nV/√Hz voltage noise matches that of the LT1028 and is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1115's current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise (e_n), current noise (i_n) and resistor noise (r_n).

Total Noise vs Source Resistance

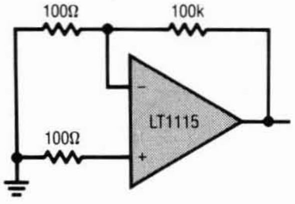
The total input referred noise of an op amp is given by

$$e_t = [e_n^2 + r_n^2 + (i_n R_{eq})^2]^{1/2}$$

where R_{eq} is the total equivalent source resistance at the two inputs

and $r_n = \sqrt{4kTR_{eq}} = 0.13\sqrt{R_{eq}}$ in nV/√Hz at 25°C

As a numerical example, consider the total noise at 1kHz of the gain of 1000 amplifier shown below.



$$R_{eq} = 100\Omega + 100\Omega \| 100k \approx 200\Omega$$
$$r_n = 0.13\sqrt{200} = 1.84\text{nV}/\sqrt{\text{Hz}}$$
$$e_n = 0.85\text{nV}/\sqrt{\text{Hz}}$$
$$i_n = 1.0\text{pA}/\sqrt{\text{Hz}}$$
$$e_t = [0.85^2 + 1.84^2 + (1.0 \times 0.2)^2]^{1/2} = 2.04\text{nV}/\sqrt{\text{Hz}}$$

$$\text{output noise} = 1000\, e_t = 2.04\mu\text{V}/\sqrt{\text{Hz}}$$

At very low source resistance ($R_{eq} < 40\Omega$) voltage noise dominates. As R_{eq} is increased resistor noise becomes the largest term—as in the example above—and the LT1115's voltage noise becomes negligible. As R_{eq} is further increased, current noise becomes important. At 1kHz, when R_{eq} is in excess of 20kΩ, the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

APPLICATIONS INFORMATION — NOISE

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the 1/f corner of current noise is typically at 250Hz. At 10Hz when $R_{eq} > 1k\Omega$, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1kΩ because the resistor noise contribution is less. When $R_S > 1k\Omega$ total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier's inherent noise.

In summary, the LT1115 is the optimum amplifier for noise performance—provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise—as the source resistance is increased beyond the LT1115's level of usefulness.

Best Op Amp for Lowest Total Noise vs Source Resistance

SOURCE RESISTANCE (Note 1)	BEST OP AMP AT LOW FREQ (10Hz)	BEST OP AMP WIDEBAND (1kHz)
0 to 400Ω	LT1028/1115	LT1028/1115
400Ω to 4kΩ	LT1007/1037	LT1028/1115
4kΩ to 40kΩ	LT1001*	LT1007/1037
40kΩ to 500kΩ	LT1012*	LT1001*
500kΩ to 5MΩ	LT1012* or LT1055	LT1012*
>5M	LT1055	LT1055

Note 1: Source resistance is defined as matched or unmatched, e.g., $R_S = 1k\Omega$ means: 1kΩ at each input, or 1kΩ at one input and zero at the other.

* These op amps are best utilized in applications requiring less bandwidth than audio.

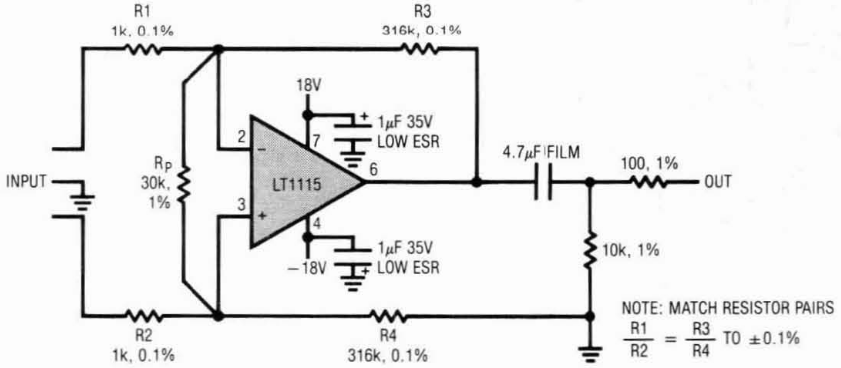
APPLICATIONS INFORMATION — GENERAL

The LT1115 is a very high performance op amp, but not necessarily one which is optimized for universal application. Because of very low voltage noise and the resulting high gain-bandwidth product, the device is most applicable to relatively high gain applications. Thus, while the LT1115 will provide notably superior performance to the 5534 in most applications, the device may require circuit modifications to be used at very low noise gains.

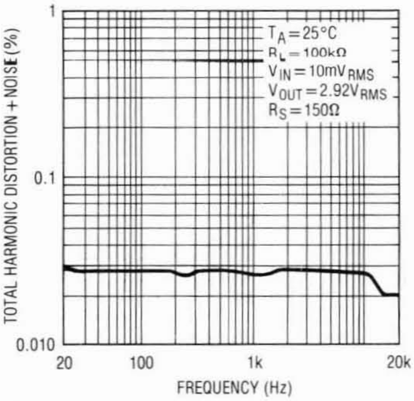
The part is not generally applicable for unity gain followers or inverters. In general, it should always be used with good low impedance bypass capacitors on the supplies, low impedance feedback values, and minimal capacitive loading. Ground plane construction is recommended, as is a compact layout.

TYPICAL APPLICATIONS

Figure 1. Balanced Transformerless Microphone Preamp

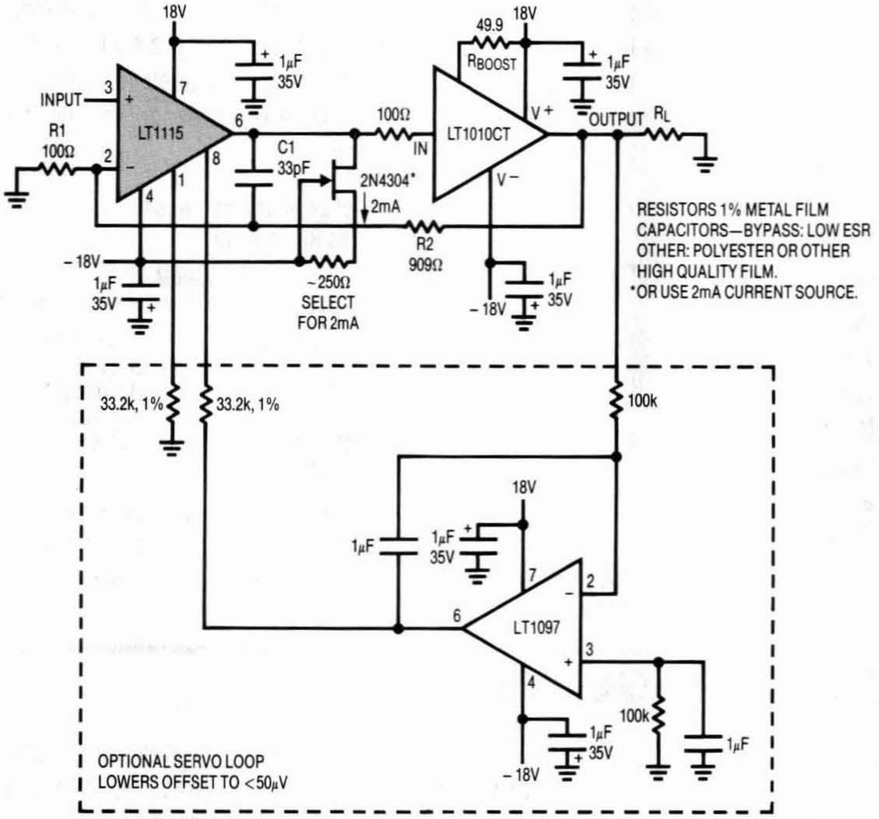


THD + Noise vs Frequency (Figure 1)



TYPICAL APPLICATIONS

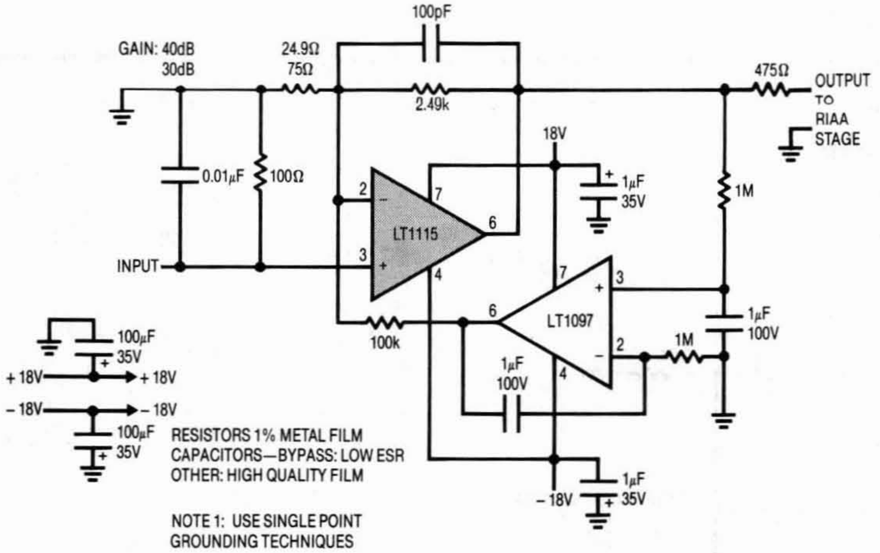
Figure 2. Low Noise DC Accurate × 10 Buffered Line Amplifier


18V
1µF 35V
INPUT
R1 100Ω
LT1115
C1 33pF
100Ω
49.9
RBOOST
18V
1µF 35V
IN
LT1010CT
V+
V−
OUTPUT
RL
2N4304*
2mA
R2 909Ω
−18V
1µF 35V
~250Ω SELECT FOR 2mA
−18V
1µF 35V
33.2k, 1%
33.2k, 1%
100k
18V
1µF
1µF 35V
LT1097
100k
1µF
1µF 35V
−18V
OPTIONAL SERVO LOOP LOWERS OFFSET TO <50µV

RESISTORS 1% METAL FILM
CAPACITORS—BYPASS: LOW ESR
OTHER: POLYESTER OR OTHER HIGH QUALITY FILM.
*OR USE 2mA CURRENT SOURCE.

NOTE 1: USE SINGLE POINT GROUND.
NOTE 2: USE ≥470µF CAPACITORS AT EACH INCOMING SUPPLY TERMINAL (I.E. AT BOARD EDGE).
NOTE 3: FOR BETTER NOISE PERFORMANCE AT SLIGHTLY LESS DRIVE CAPABILITY: R1 = 43Ω, R2 = 392Ω, DELETE C1.

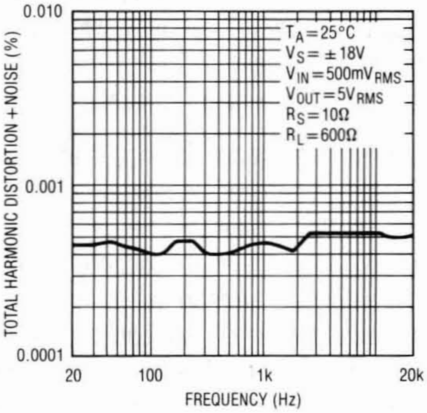
Figure 3. RIAA Moving Coil "Pre-Pre" Amplifier
(+40/+30dB Gain Low Noise Servo'd Amplifier)


GAIN: 40dB
30dB
24.9Ω
75Ω
100pF
2.49k
475Ω
OUTPUT TO RIAA STAGE
0.01µF
100Ω
INPUT
18V
1µF 35V
LT1115
1M
LT1097
100k
1µF 100V
1M
1µF 100V
100µF 35V
+18V
+18V
−18V
−18V
100µF 35V
1µF 35V
−18V

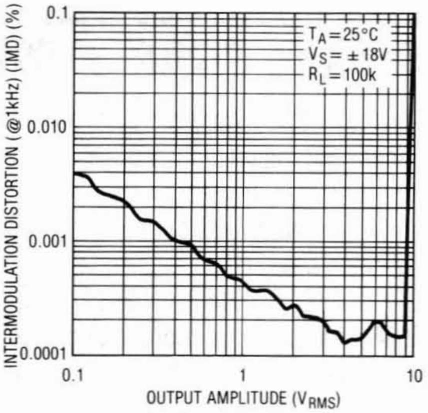
RESISTORS 1% METAL FILM
CAPACITORS—BYPASS: LOW ESR
OTHER: HIGH QUALITY FILM

NOTE 1: USE SINGLE POINT GROUNDING TECHNIQUES

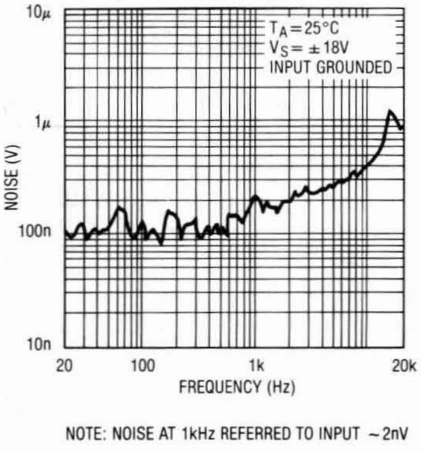
THD + Noise vs Frequency (Figure 2)



CCIF IMD Test (Twin Tones at 13 and 14kHz) (Figure 3)



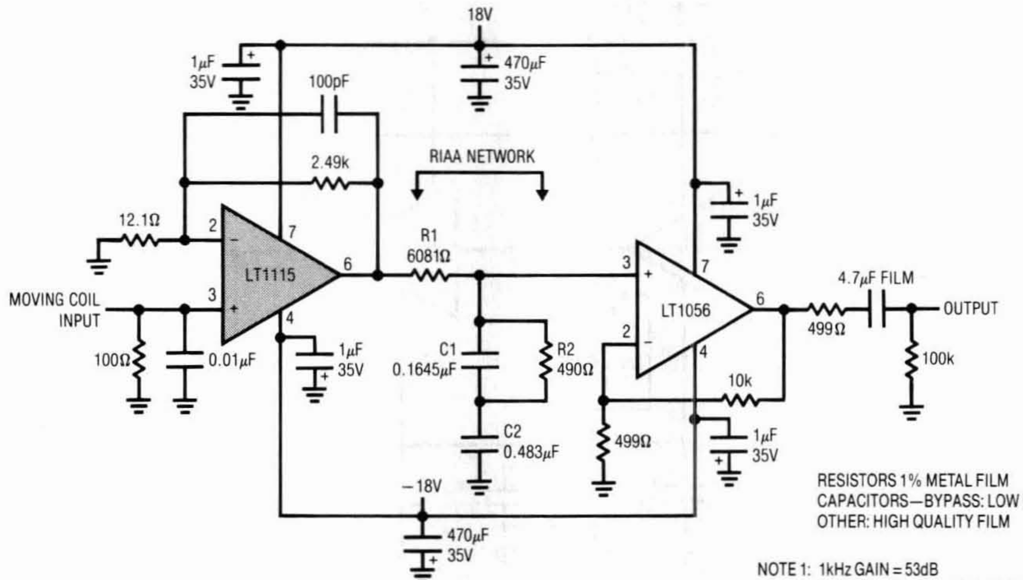
Noise vs Frequency (Figure 3)



NOTE: NOISE AT 1kHz REFERRED TO INPUT ~2nV

TYPICAL APPLICATIONS

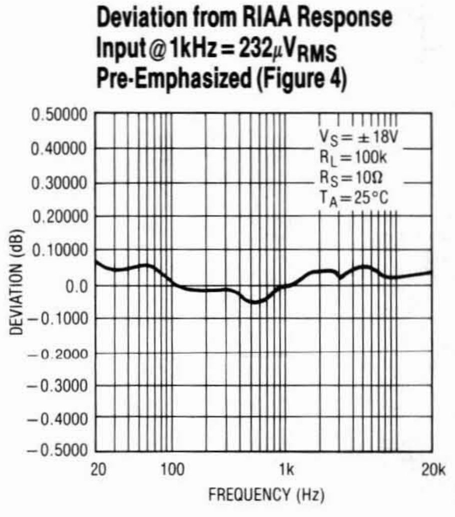
Figure 4. Moving Coil Passive RIAA Phonograph Pre-Amp

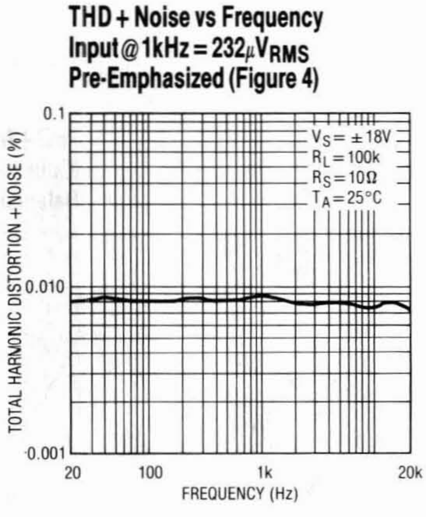

18V
1µF
35V
100pF
470µF
35V
2.49k
RIAA NETWORK
12.1Ω
2
7
6
3
4
LT1115
MOVING COIL
INPUT
100Ω
0.01µF
1µF
35V
R1
6081Ω
C1
0.1645µF
R2
490Ω
C2
0.483µF
−18V
470µF
35V
3
7
2
6
4
LT1056
1µF
35V
4.7µF FILM
499Ω
OUTPUT
100k
10k
1µF
35V
499Ω

RESISTORS 1% METAL FILM
CAPACITORS—BYPASS: LOW ESR
OTHER: HIGH QUALITY FILM

NOTE 1: 1kHz GAIN = 53dB
NOTE 2: IN RIAA NETWORK VALUES SHOWN ARE MEASURED AND PRODUCE THE "DEVIATION FROM RIAA" GRAPH SHOWN. THE CALCULATED EXACT VALUES ARE:

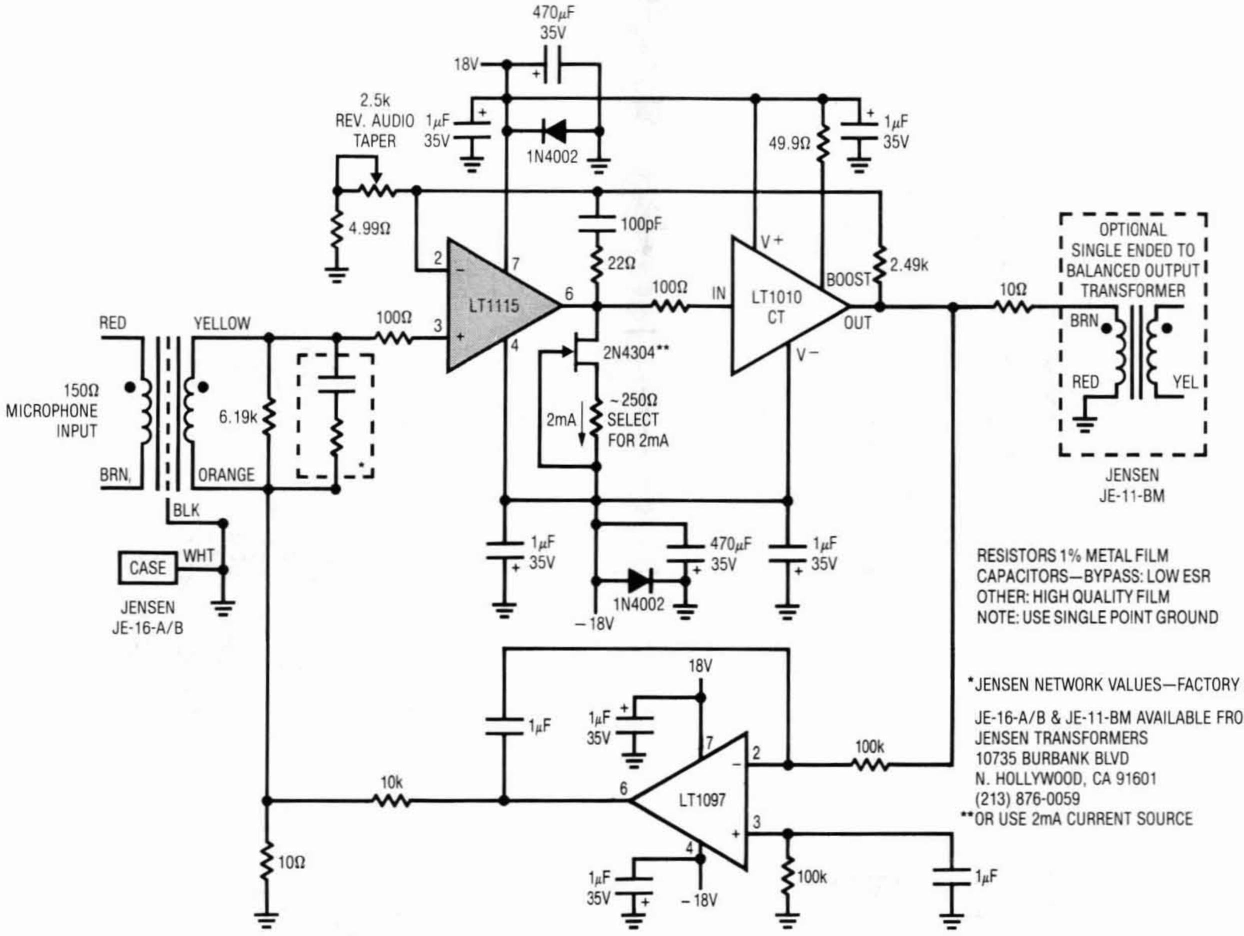
R1-6249Ω C1-0.161µF
R2-504Ω C2-0.47µF


Deviation from RIAA Response
Input @ 1kHz = 232µV$_{RMS}$
Pre-Emphasized (Figure 4)


THD + Noise vs Frequency
Input @ 1kHz = 232µV$_{RMS}$
Pre-Emphasized (Figure 4)

TYPICAL APPLICATIONS

Figure 5. High Performance Transformer Coupled Microphone Pre-Amp


470µF
35V
18V
2.5k
REV. AUDIO
TAPER
1µF
35V
1N4002
49.9Ω
1µF
35V
4.99Ω
100pF
22Ω
2.49k
V+
BOOST
LT1115
LT1010
CT
IN
OUT
V−
100Ω
100Ω
10Ω
2N4304**
~250Ω
SELECT
FOR 2mA
2mA
RED
YELLOW
150Ω
MICROPHONE
INPUT
6.19k
BRN
ORANGE
BLK
WHT
CASE
JENSEN
JE-16-A/B
1µF
35V
470µF
35V
1N4002
−18V
1µF
35V
OPTIONAL
SINGLE ENDED TO
BALANCED OUTPUT
TRANSFORMER
BRN
RED
YEL
JENSEN
JE-11-BM
18V
1µF
1µF
35V
100k
10k
LT1097
1µF
35V
−18V
100k
1µF
10Ω
2
3
4
6
7

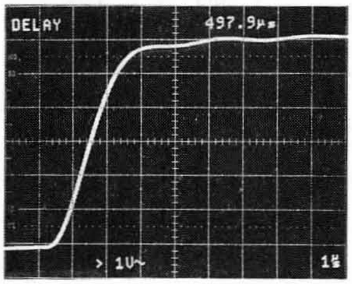
RESISTORS 1% METAL FILM
CAPACITORS—BYPASS: LOW ESR
OTHER: HIGH QUALITY FILM
NOTE: USE SINGLE POINT GROUND

*JENSEN NETWORK VALUES—FACTORY SELECTED.

JE-16-A/B & JE-11-BM AVAILABLE FROM:
JENSEN TRANSFORMERS
10735 BURBANK BLVD
N. HOLLYWOOD, CA 91601
(213) 876-0059

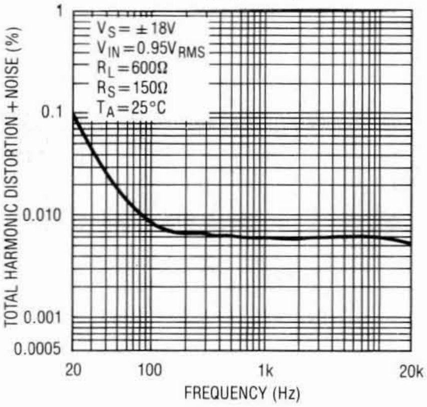
**OR USE 2mA CURRENT SOURCE

Risetime of High Performance Transformer Coupled Microphone Pre-Amp (Figure 5)

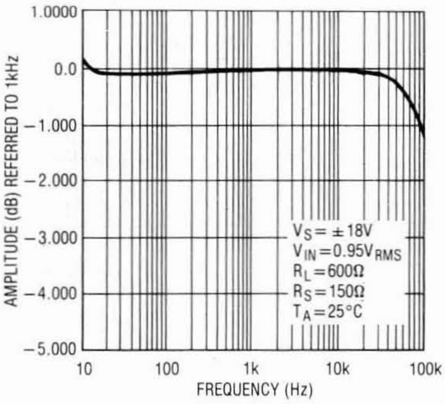


RISETIME OF PRE-AMP
$A_V = 20dB$
$V_{IN} = 400mV$,
2kHz SQUARE WAVE MEASURED AT SINGLE ENDED OUTPUT BEFORE TRANSFORMER

THD + Noise vs Frequency (Gain = 20dB) Balanced In/ Balanced Out (Figure 5)

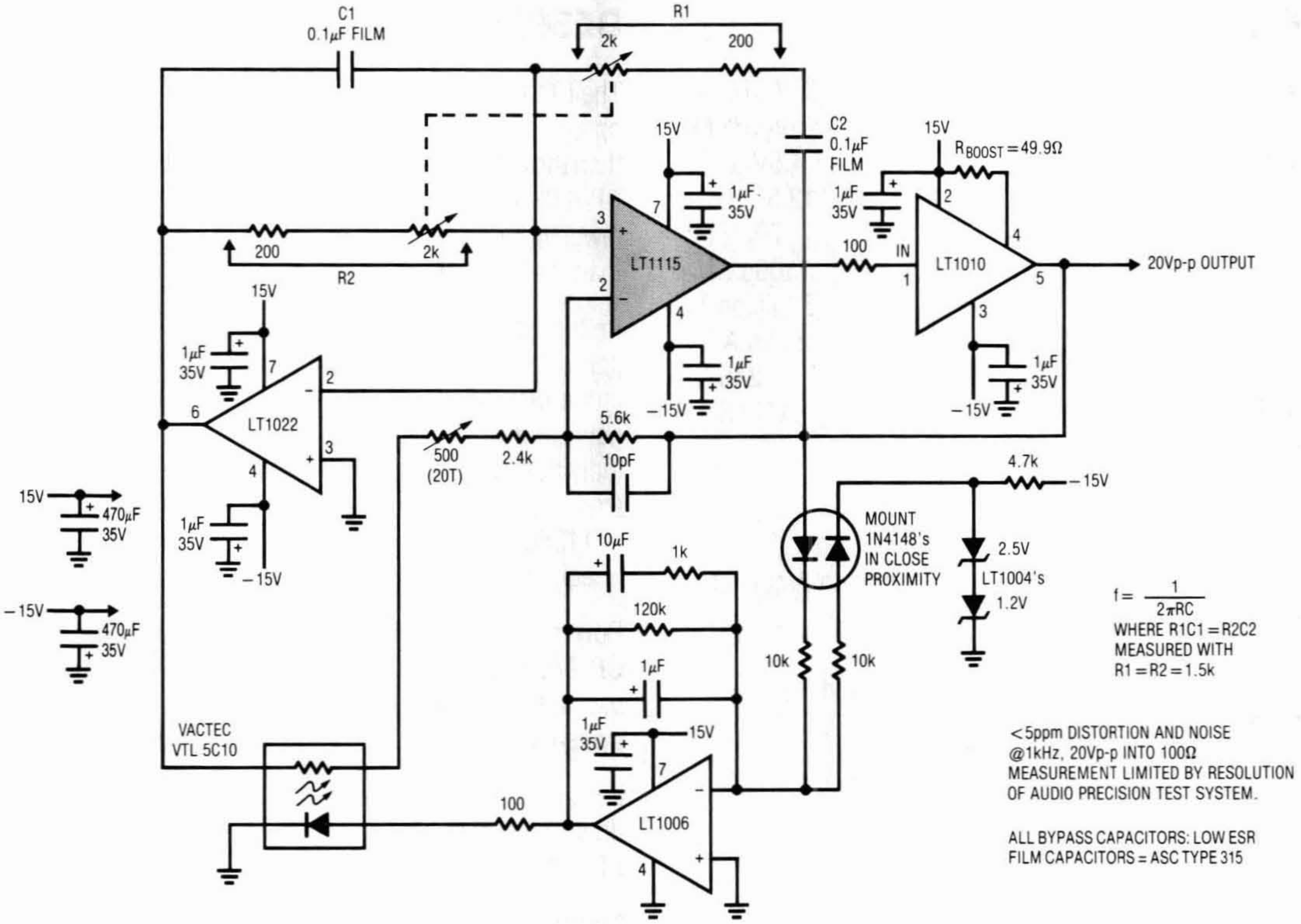


Frequency Response (Gain = 20dB) Balanced In/ Balanced Out (Figure 5)



TYPICAL APPLICATIONS

Figure 6. Ultra Low THD Oscillator (Sine Wave) (<5ppm Distortion)


C1
0.1μF FILM
R1
2k
200
C2
0.1μF
FILM
15V
1μF
35V
7
3
2
4
LT1115
−15V
15V
R_{BOOST} = 49.9Ω
1μF
35V
2
4
100
IN
1
LT1010
5
3
1μF
35V
−15V
20Vp-p OUTPUT
200
2k
R2
15V
1μF
35V
7
6
2
LT1022
3
4
1μF
35V
−15V
15V
470μF
35V
−15V
470μF
35V
500
(20T)
2.4k
5.6k
10pF
4.7k
−15V
MOUNT
1N4148's
IN CLOSE
PROXIMITY
2.5V
LT1004's
1.2V
10μF
1k
120k
1μF
10k
10k
1μF
35V
15V
7
VACTEC
VTL 5C10
100
LT1006
4

$f = \frac{1}{2\pi RC}$

WHERE R1C1 = R2C2
MEASURED WITH
R1 = R2 = 1.5k

<5ppm DISTORTION AND NOISE @1kHz, 20Vp-p INTO 100Ω MEASUREMENT LIMITED BY RESOLUTION OF AUDIO PRECISION TEST SYSTEM.

ALL BYPASS CAPACITORS: LOW ESR FILM CAPACITORS = ASC TYPE 315

LT1124/LT1125

Dual/Quad Low Noise, High Speed Precision Op Amps

FEATURES

■ 100% Tested Low Voltage Noise	2.7nV/√Hz Typ 4.2nV/√Hz Max
■ Slew Rate	4.5V/μs Typ
■ Gain Bandwidth Product	12.5MHz Typ
■ Offset Voltage, Prime Grade	70μV Max
Low Grade	100μV Max
■ High Voltage Gain	5 Million Min
■ Supply Current Per Amplifier	2.75mA Max
■ Common Mode Rejection	112dB Min
■ Power Supply Rejection	116dB Min
■ Available in 8-Pin SO Package	

APPLICATIONS

- Two and Three Op Amp Instrumentation Amplifiers
- Low Noise Signal Processing
- Active Filters
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Tape Head Preamplifiers
- Infrared Detectors

DESCRIPTION

The LT1124 dual and LT1125 quad are high performance op amps that offer higher gain, slew rate, and bandwidth than the industry standard OP-27 and competing OP-270/OP-470 op amps. In addition, the LT1124/LT1125 have lower I_B and I_{OS} than the OP-27; lower V_{OS} and noise than the OP-270/OP-470.

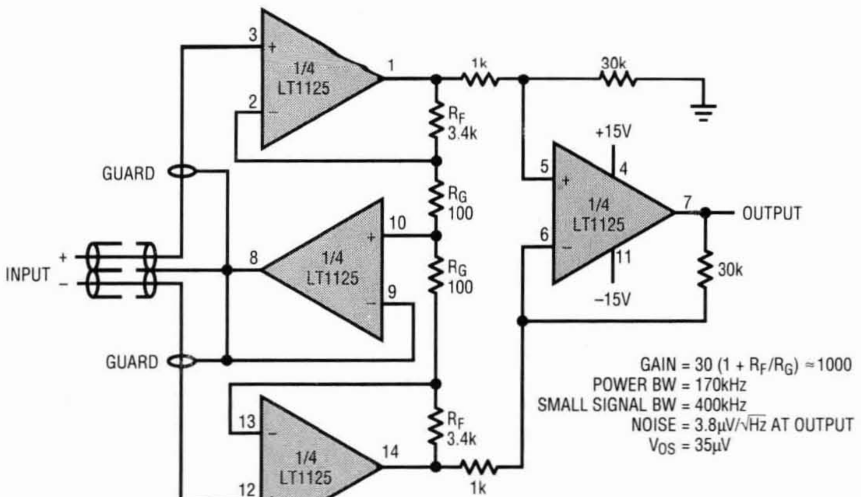
In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Slew rate, gain bandwidth, and 1kHz noise are 100% tested for each individual amplifier. Consequently, the specifications of even the lowest cost grades (the LT1124C and the LT1125C) have been spectacularly improved compared to equivalent grades of competing amplifiers.

Power consumption of the LT1124 is one half of two OP-27s. Low power and high performance in an 8-pin SO package make the LT1124 a first choice for surface mounted systems and where board space is restricted.

For a decompensated version of these devices, with three times higher slew rate and bandwidth, please see the LT1126/LT1127 data sheet.

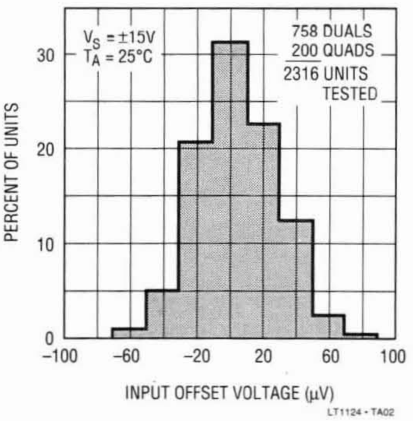
Protected by U.S. patents 4,775,884 and 4,837,496.

Instrumentation Amplifier with Shield Driver



GAIN = 30 (1 + R_F/R_G) ≈ 1000
POWER BW = 170kHz
SMALL SIGNAL BW = 400kHz
NOISE = 3.8μV/√Hz AT OUTPUT
V_{OS} = 35μV

Input Offset Voltage Distribution (All Packages, LT1124 and LT1125)

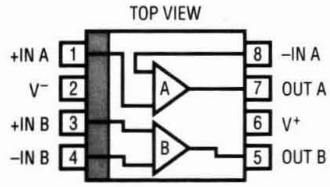
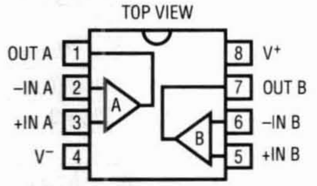
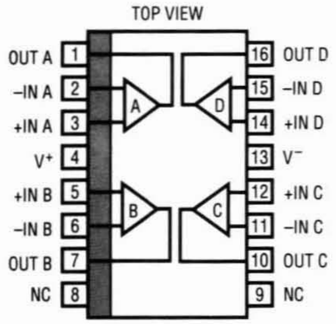
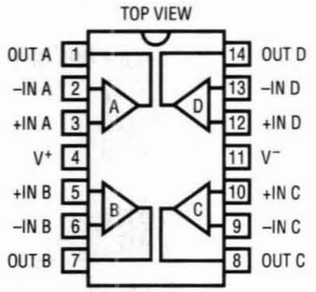


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Input Voltages	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Differential Input Current (Note 5)	±25mA
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Temperature Range	
LT1124AM/LT1124M LT1125AM/LT1125M	–55°C to 125°C
LT1124AC/LT1124C LT1125AC/LT1125C	–40°C to 85°C
Storage Temperature Range	
All Grades	–65°C to 150°C

PACKAGE/ORDER INFORMATION

 TOP VIEW +IN A 1 V⁻ 2 +IN B 3 –IN B 4 8 –IN A 7 OUT A 6 V⁺ 5 OUT B A B S8 PACKAGE 8-LEAD PLASTIC SOIC NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-PIN DIP CONFIGURATION. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE PIN LOCATIONS LT1124 • POI01	ORDER PART NUMBER LT1124CS8 PART MARKING 1124	 TOP VIEW OUT A 1 –IN A 2 +IN A 3 V⁻ 4 8 V⁺ 7 OUT B 6 –IN B 5 +IN B A B J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP LT1124 • POI02	ORDER PART NUMBER LT1124AMJ8 LT1124MJ8 LT1124CJ8 LT1124ACN8 LT1124CN8
 TOP VIEW OUT A 1 –IN A 2 +IN A 3 V⁺ 4 +IN B 5 –IN B 6 OUT B 7 NC 8 16 OUT D 15 –IN D 14 +IN D 13 V⁻ 12 +IN C 11 –IN C 10 OUT C 9 NC A B C D S PACKAGE 16-LEAD PLASTIC SOL LT1124 • POI03	LT1125CS	 TOP VIEW OUT A 1 –IN A 2 +IN A 3 V⁺ 4 +IN B 5 –IN B 6 OUT B 7 14 OUT D 13 –IN D 12 +IN D 11 V⁻ 10 +IN C 9 –IN C 8 OUT C A B C D J PACKAGE 14-LEAD CERAMIC DIP N PACKAGE 14-LEAD PLASTIC DIP LT1124 • POI04	LT1125AMJ LT1125MJ LT1125CJ LT1125ACN LT1125CN

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

			LT1124AM/AC LT1125AM/AC			LT1124M/C LT1125M/C			
SYMBOL	**PARAMETER**	**CONDITIONS (Note 1)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	LT1124		20	70		25	100	μV
		LT1125		25	90		30	140	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		μV/Mo
I_{OS}	Input Offset Current	LT1124		5	15		6	20	nA
		LT1125		6	20		7	30	nA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1124AM/AC LT1125AM/AC MIN	TYP	MAX	LT1124M/C LT1125M/C MIN	TYP	MAX	UNITS
I_B	Input Bias Current			±7	±20		±8	±30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 7 and 8)		70	200		70		nVp-p
	Input Noise Voltage Density	f_O = 10Hz (Note 3)		3.0	5.5		3.0	5.5	nV/√Hz
		f_O = 1000Hz (Note 2)		2.7	4.2		2.7	4.2	nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz		1.3			1.3		pA/√Hz
		f_O = 1000Hz		0.3			0.3		pA/√Hz
V_{CM}	Input Voltage Range		±12.0	±12.8		±12.0	±12.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$	112	126		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	116	126		110	124		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	5.0	17.0		3.0	15.0		V/μV
		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	2.0	4.0		1.5	3.0		V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	±13.0	±13.8		±12.5	±13.8		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	3.0	4.5		2.7	4.5		V/μs
GBW	Gain-Bandwidth Product	f_O =100kHz (Note 2)	9.0	12.5		8.0	12.5		MHz
Z_O	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		75			75		Ω
I_S	Supply Current Per Amplifier			2.3	2.75		2.3	2.75	mA
	Channel Separation	$f \leq 10Hz$ (Note 8) $V_O = \pm 10V$, $R_L = 2k\Omega$	134	150		130	150		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)		LT1124AM LT1125AM MIN	TYP	MAX	LT1124M LT1125M MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1124	●		50	170		60	250	μV
		LT1125	●		55	190		70	290	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 4)	●		0.3	1.0		0.4	1.5	μV/°C
I_{OS}	Input Offset Current	LT1124	●		18	45		20	60	nA
		LT1125	●		18	55		20	70	nA
I_B	Input Bias Current		●		±18	±55		±20	±70	nA
V_{CM}	Input Voltage Range		●	±11.3	±12		±11.3	±12		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.3V$	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	110	122		104	120		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	●	3.0	10.0		2.0	10.0		V/μV
		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	●	1.0	3.0		0.7	2.0		V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.6		±12.0	±13.6		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	●	2.3	3.8		2.0	3.8		V/μs
I_S	Supply Current Per Amplifier		●		2.5	3.25		2.5	3.25	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

				LT1124AC LT1125AC			LT1124C LT1125C			
SYMBOL	**PARAMETER**	**CONDITIONS (Note 1)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	LT1124	●		35	120		45	170	µV
		LT1125	●		40	140		50	210	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 4)	●		0.3	1.0		0.4	1.5	µV/°C
I_{OS}	Input Offset Current	LT1124	●		6	25		7	35	nA
		LT1125	●		7	35		8	45	nA
I_B	Input Bias Current		●		±8	±35		±9	±45	nA
V_{CM}	Input Voltage Range		●	±11.5	±12.4		±11.5	±12.4		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.5V$	●	109	125		102	122		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	112	125		107	122		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 10k\Omega$, $V_O = \pm 10V$	●	4.0	15.0		2.5	14.0		V/µV
		$R_L \ge 2k\Omega$, $V_O = \pm 10V$	●	1.5	3.5		1.0	2.5		V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12.5	±13.7		±12.0	±13.7		V
SR	Slew Rate	$R_L \ge 2k\Omega$ (Notes 2 and 6)	●	2.6	4.0		2.4	4.0		V/µs
I_S	Supply Current Per Amplifier		●		2.4	3.0		2.4	3.0	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 9)

				LT1124AC LT1125AC			LT1124C LT1125C			
SYMBOL	**PARAMETER**	**CONDITIONS (Note 1)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	LT1124	●		40	140		50	200	µV
		LT1125	●		45	160		55	240	µV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		0.3	1.0		0.4	1.5	µV/°C
I_{OS}	Input Offset Current	LT1124	●		15	40		17	55	nA
		LT1125	●		15	50		17	65	nA
I_B	Input Bias Current		●		±15	±50		±17	±65	nA
V_{CM}	Input Voltage Range		●	±11.4	±12.2		±11.4	±12.2		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.4V$	●	107	124		101	121		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4V$ to $\pm 18V$	●	111	124		106	121		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 10k\Omega$, $V_O = \pm 10V$	●	3.5	12.0		2.2	12.0		V/µV
		$R_L \ge 2k\Omega$, $V_O = \pm 10V$	●	1.2	3.2		0.8	2.3		V/µV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12.5	±13.6		±12.0	±13.6		V
SR	Slew Rate	$R_L \ge 2k\Omega$ (Note 6)	●	2.4	3.9		2.1	3.9		V/µs
I_S	Supply Current Per Amplifier		●		2.4	3.25		2.4	3.25	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1125's (or 100 LT1124's) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: This parameter is 100% tested for each individual amplifier.

Note 3: This parameter is sample tested only.

Note 4: This parameter is not 100% tested.

Note 5: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.4V, the input current should be limited to 25mA.

Note 6: Slew rate is measured in $A_V = -1$; input signal is ±7.5V, output measured at ±2.5V.

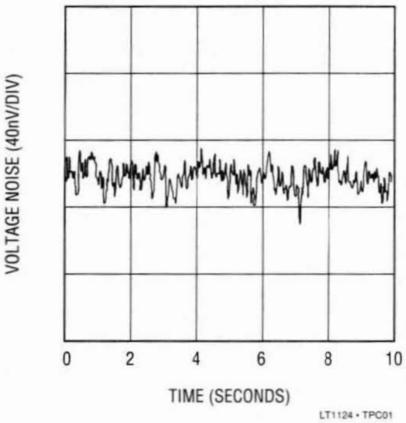
Note 7: 0.1Hz to 10Hz noise can be inferred from the 10Hz noise voltage density test. See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section of the LT1007 or LT1028 data sheets.

Note 8: This parameter is guaranteed but not tested.

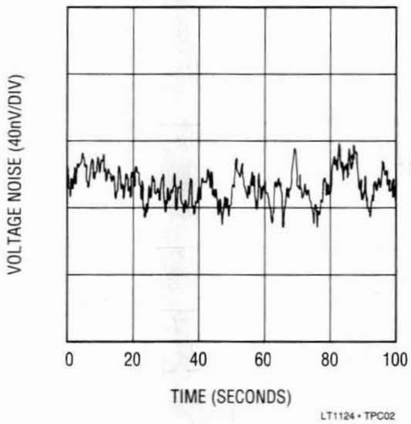
Note 9: The LT1124/LT1125 are not tested and are not quality-assurance-sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from –55°C, 0°C, 25°C, 70°C and/or 125°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

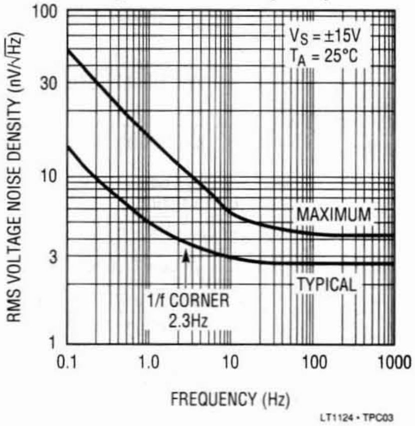
0.1Hz to 10Hz Voltage Noise



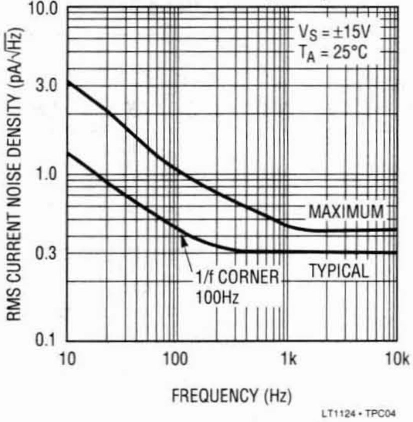
0.01Hz to 1Hz Voltage Noise



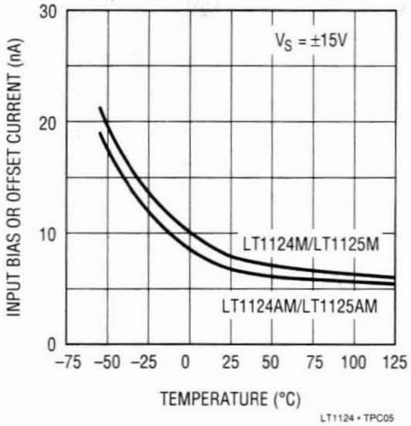
Voltage Noise vs Frequency



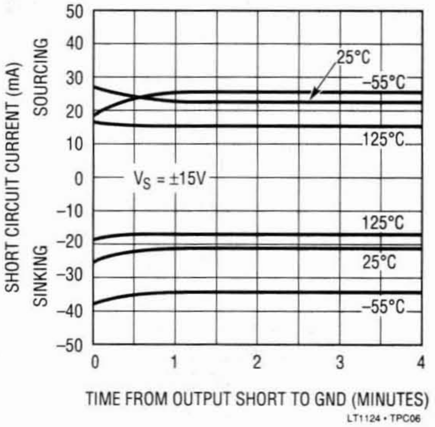
Current Noise vs Frequency



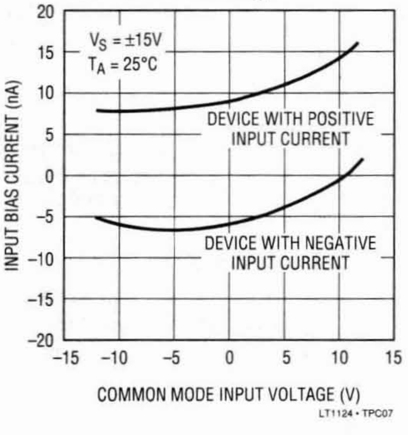
Input Bias or Offset Current vs Temperature



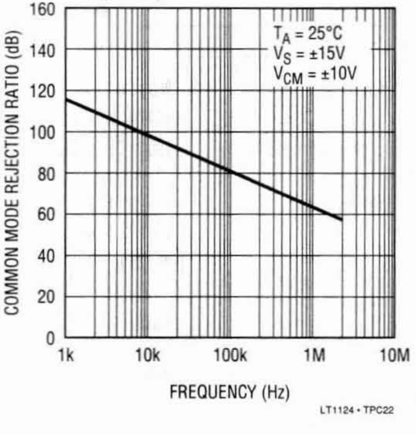
Output Short Circuit Current vs Time



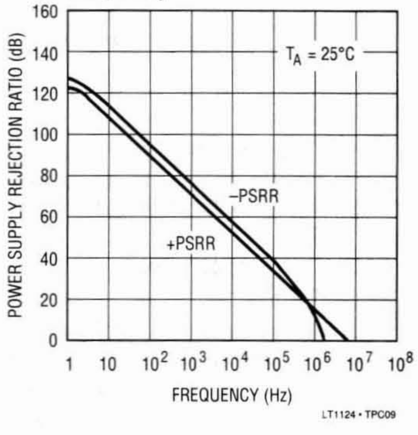
Input Bias Current Over the Common Mode Range



Common Mode Rejection Ratio vs Frequency

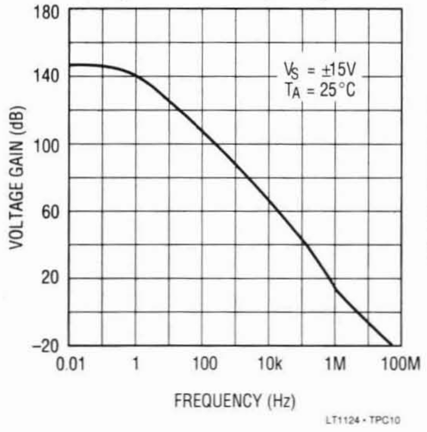


Power Supply Rejection Ratio vs Frequency



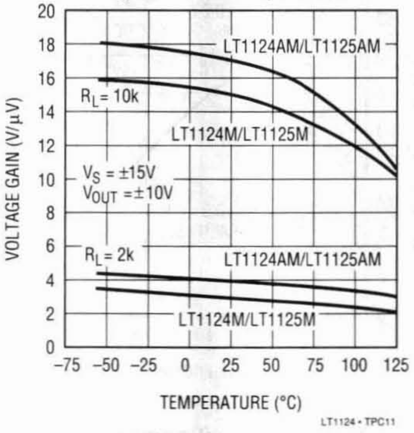
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain vs Frequency



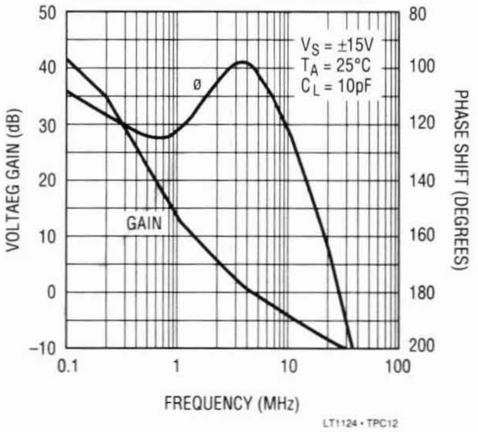
LT1124 • TPC10

Voltage Gain vs Temperature



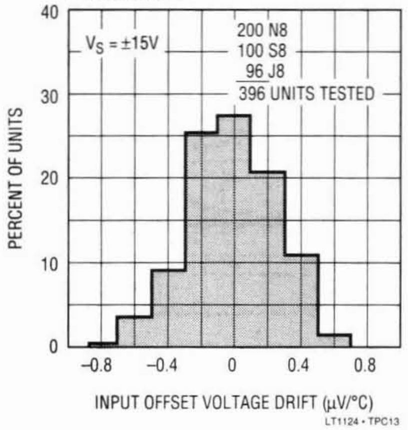
LT1124 • TPC11

Gain, Phase Shift vs Frequency



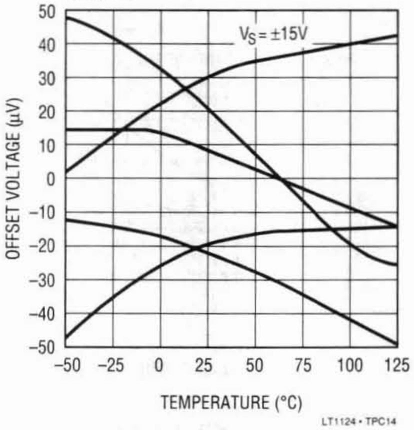
LT1124 • TPC12

Input Offset Voltage Drift Distribution



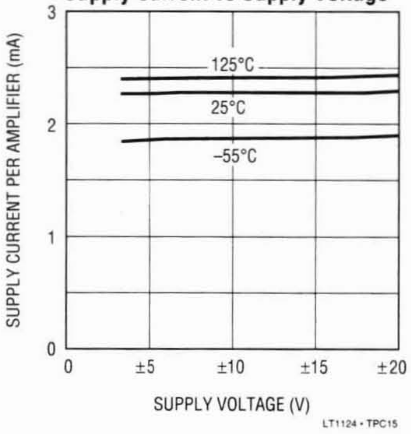
LT1124 • TPC13

Offset Voltage Drift with Temperature of Representative Units



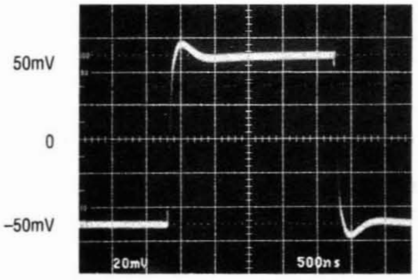
LT1124 • TPC14

Supply Current vs Supply Voltage



LT1124 • TPC15

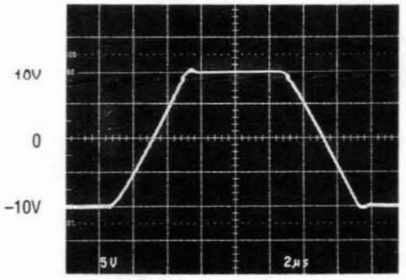
Small Signal Transient Response



A_{VCL} = +1, V_S = ±15V OR ±5V
C_L = 15pF

LT1124 • TPC16

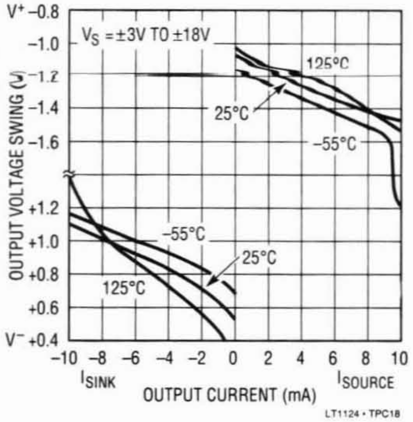
Large Signal Transient Response



A_{VCL} = –1, V_S = ±15V

LT1124 • TPC17

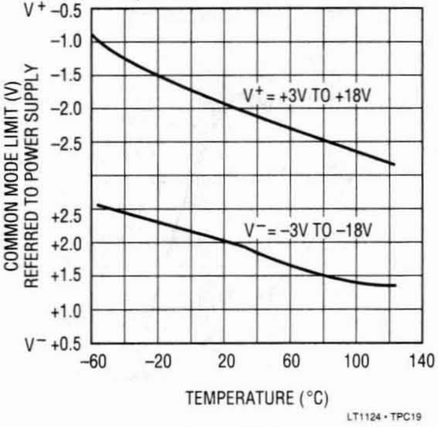
Output Voltage Swing vs Load Current



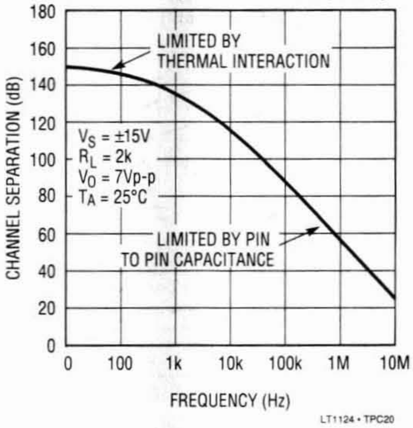
LT1124 • TPC18

TYPICAL PERFORMANCE CHARACTERISTICS

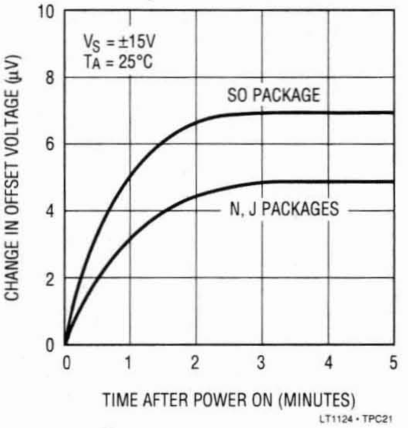
Common Mode Limit vs Temperature



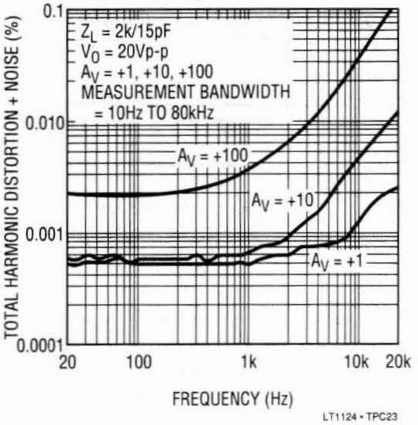
Channel Separation vs Frequency



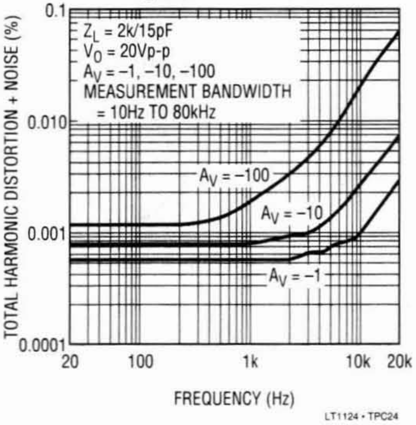
Warm-Up Drift



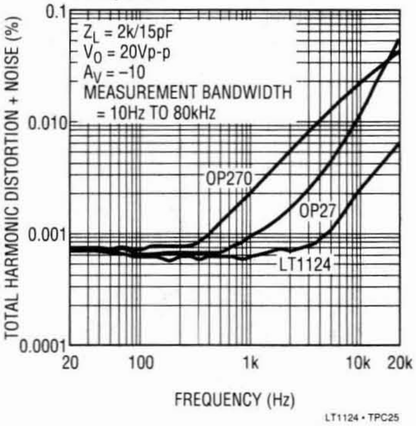
Total Harmonic Distortion and Noise vs Frequency for Non-Inverting Gain



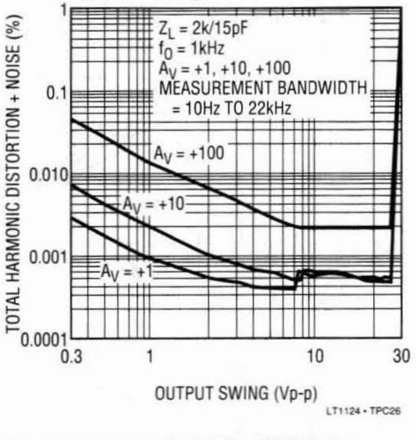
Total Harmonic Distortion and Noise vs Frequency for Inverting Gain



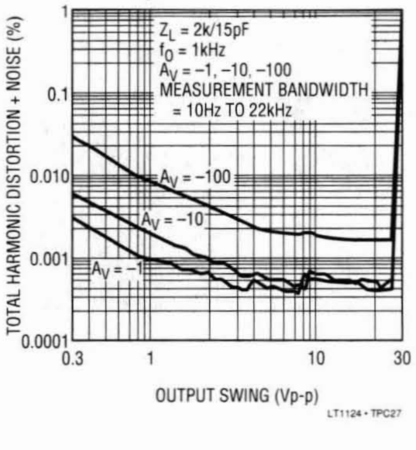
Total Harmonic Distortion and Noise vs Frequency for Competitive Devices



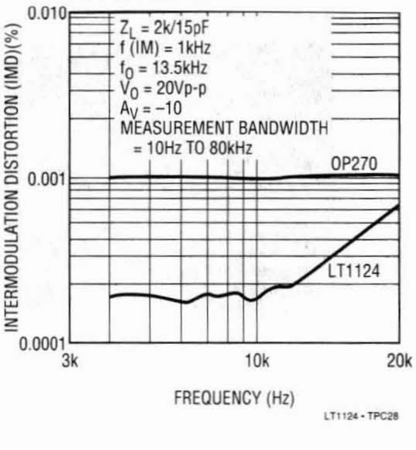
Total Harmonic Distortion and Noise vs Output Amplitude for Non-Inverting Gain



Total Harmonic Distortion and Noise vs Output Amplitude for Inverting Gain



Intermodulation Distortion (CCIF Method)* vs Frequency LT1124 and OP270



*See LT1115 data sheet for definition of CCIF testing

APPLICATIONS INFORMATION

The LT1124 may be inserted directly into OP-270 sockets. The LT1125 plugs into OP-470 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

Matching Specifications

In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The three op amp instrumentation amplifier configuration shown in this data sheet is an example. Matching characteristics are not 100% tested on the LT1124/LT1125.

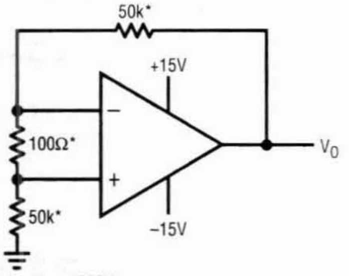
Some specifications are guaranteed by definition. For example, 70μV maximum offset voltage implies that mismatch cannot be more than 140μV. 112dB (= 2.5μV/V) CMRR means that worst case CMRR match is 106dB (5μV/V). However, the following table can be used to estimate the expected matching performance between the two sides of the LT1124, and between amplifiers A and D, and between amplifiers B and C of the LT1125.

Offset Voltage and Drift

Thermocouple effects, caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier unless proper care is exercised. Air currents should be minimized, package leads should be short, the two input leads should be close together and maintained at the same temperature.

The circuit shown to measure offset voltage is also used as the burn-in configuration for the LT1124/LT1125, with the supply voltages increased to ±16V.

Test Circuit for Offset Voltage and Offset Voltage Drift with Temperature



$V_O = 1000V_{OS}$

*RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL

LT1124 • TA05

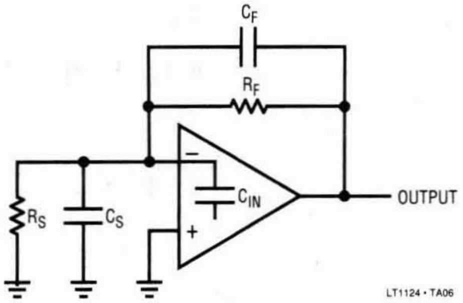
Expected Match

PARAMETER		LT1124AM/AC LT1125AM/AC 50% YIELD	98% YIELD	LT1124M/C LT1125M/C 50% YIELD	98% YIELD	UNITS
V_{OS} Match, ΔV_{OS}	LT1124	20	110	30	130	μV
	LT1125	30	150	50	180	μV
Temperature Coefficient Match		0.35	1.0	0.5	1.5	μV/°C
Average Non-Inverting I_B		6	18	7	25	nA
Match of Non-Inverting I_B		7	22	8	30	nA
CMRR Match		126	115	123	112	dB
PSRR Match		127	118	127	114	dB

APPLICATIONS INFORMATION

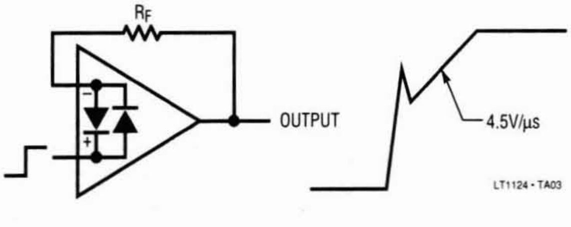
High Speed Operation

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 2pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_FC_F$, the effect of the feedback pole is completely removed.



Unity Gain Buffer Applications

When $R_F \le 100\Omega$ and the input is driven with a fast, large signal pulse (>1V), the output waveform will look as shown.



During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short circuit protection, will be drawn by the signal generator. With $R_F \ge 500\Omega$, the output is capable of handling the current requirements ($I_L \le 20mA$ at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

Noise Testing

Each individual amplifier is tested to $4.2nV/\sqrt{Hz}$ voltage noise; i.e., for the LT1124 two tests, for the LT1125 four tests are performed. Noise testing for competing multiple op amps, if done at all, may be sample tested or tested using the circuit below.

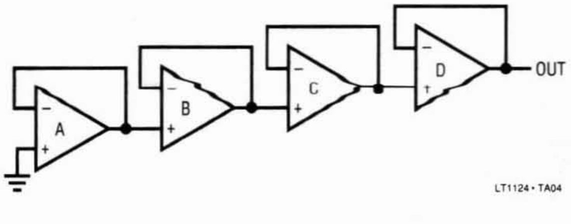
$$e_{n\,OUT} = \sqrt{(e_{nA})^2 + (e_{nB})^2 + (e_{nC})^2 + (e_{nD})^2}$$

If the LT1125 were tested this way, the noise limit would be $\sqrt{4 \times (4.2nV/\sqrt{Hz})^2} = 8.4nV/\sqrt{Hz}$. But is this an effective screen? What if three of the four amplifiers are at a typical $2.7nV/\sqrt{Hz}$, and the fourth one was contaminated and has $6.9nV/\sqrt{Hz}$ noise?

$$\text{RMS Sum} = \sqrt{(2.7)^2 + (2.7)^2 + (2.7)^2 + (6.9)^2} = 8.33nV/\sqrt{Hz}$$

This passes an $8.4nV/\sqrt{Hz}$ spec, yet one of the amplifiers is 64% over the LT1125 spec limit. Clearly, for proper noise measurement, the op amps have to be tested individually.

Competing Quad Op Amp Noise Test Method



PERFORMANCE COMPARISON

The following table summarizes the performance of the LT1124/LT1125 compared to the low cost grades of alternate approaches.

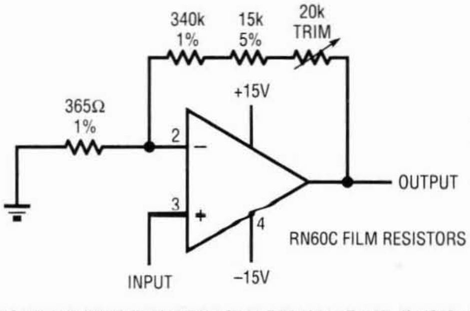
The comparison shows how the specs of the LT1124/LT1125 not only stand up to the industry standard OP-27, but in most cases are superior. Normally dual and quad performance is degraded when compared to singles, for the LT1124/LT1125 this is not the case.

Guaranteed performance, $V_S = \pm 15V$, $T_A = 25°C$, low cost devices.

PARAMETER/UNITS		LT1124CN8 LT1125CN	OP-27 GP	OP-270 GP	OP-470 GP	UNITS
Voltage Noise, 1kHz		4.2 100% Tested	4.5 Sample Tested	– No Limit	5.0 Sample Tested	$nV/\sqrt{Hz}$
Slew Rate		2.7 100% Tested	1.7 Not Tested	1.7	1.4	V/µs
Gain Bandwidth Product		8.0 100% Tested	5.0 Not Tested	– No Limit	– No Limit	MHz
Offset Voltage	LT1124	100	100	250	–	µV
	LT1125	140	–	–	1000	µV
Offset Current	LT1124	20	75	20	–	nA
	LT1125	30	–	–	30	nA
Bias Current		30	80	60	60	nA
Supply Current/Amp		2.75	5.67	3.25	2.75	mA
Voltage Gain, $R_L = 2k$		1.5	0.7	0.35	0.4	V/µV
Common Mode Rejection Ratio		106	100	90	100	dB
Power Supply Rejection Ratio		110	94	104	105	dB
S8 Package		Yes - LT1124	Yes	No	–	

TYPICAL APPLICATIONS

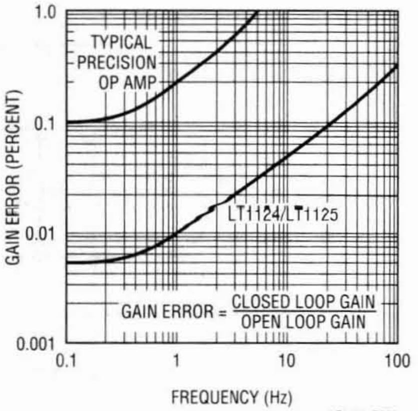
Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz



THE HIGH GAIN AND WIDE BANDWIDTH OF THE LT1124/LT1125, IS USEFUL IN LOW FREQUENCY HIGH CLOSED LOOP GAIN AMPLIFIER APPLICATIONS. A TYPICAL PRECISION OP AMP MAY HAVE AN OPEN LOOP GAIN OF ONE MILLION WITH 500kHz BANDWIDTH. AS THE GAIN ERROR PLOT SHOWS, THIS DEVICE IS CAPABLE OF 0.1% AMPLIFYING ACCURACY UP TO 0.3Hz ONLY. EVEN INSTRUMENTATION RANGE SIGNALS CAN VARY AT A FASTER RATE. THE LT1124/LT1125 "GAIN PRECISION — BANDWIDTH PRODUCT" IS 75 TIMES HIGHER, AS SHOWN.

LT1124 • TA07

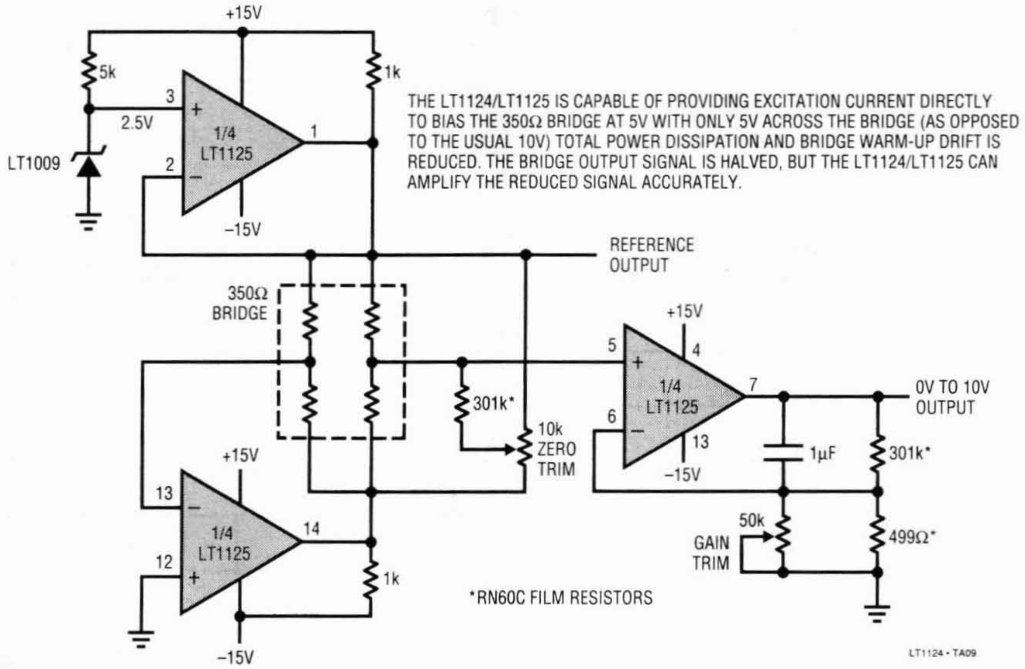
Gain Error vs Frequency Closed Loop Gain = 1000



LT1124 • TA08

TYPICAL APPLICATIONS

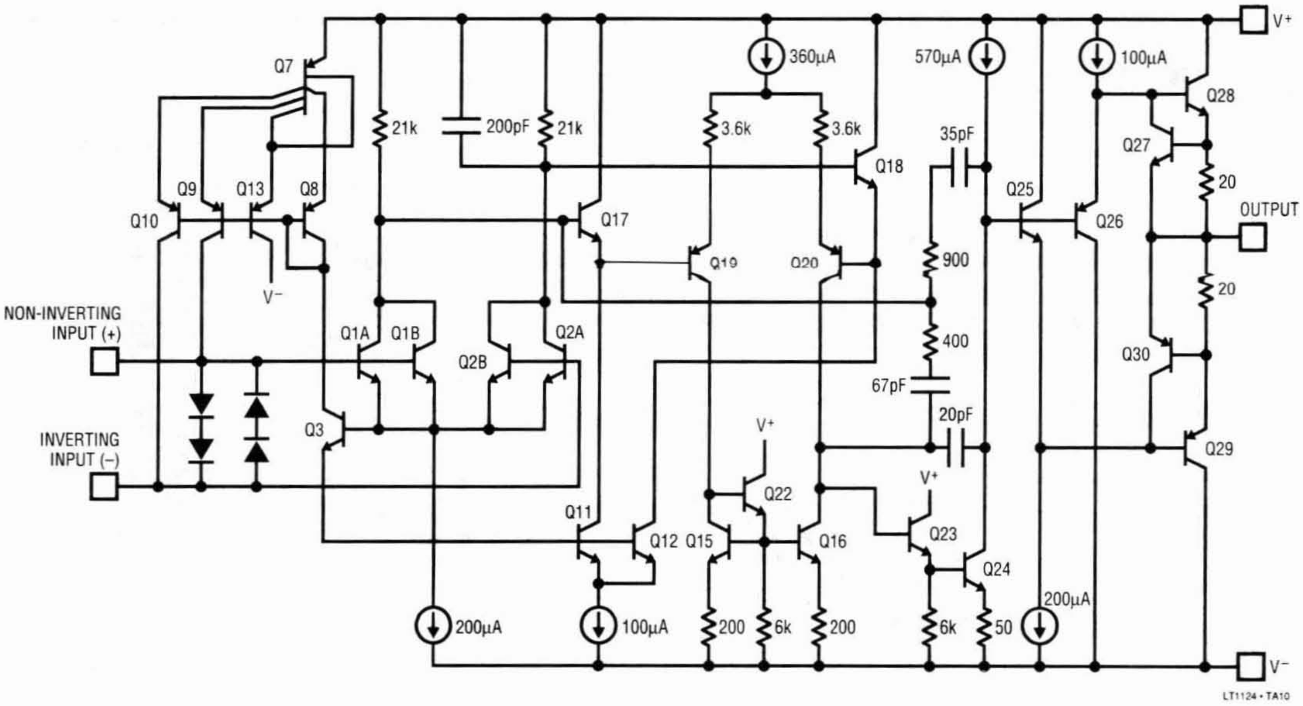
Strain Gauge Signal Conditioner with Bridge Excitation


+15V
5k
1k
3
2.5V
1/4
LT1125
1
LT1009
2
–15V
REFERENCE
OUTPUT
350Ω
BRIDGE
+15V
5
4
1/4
LT1125
7
0V TO 10V
OUTPUT
301k*
10k
ZERO
TRIM
6
13
–15V
1μF
301k*
+15V
13
1/4
LT1125
14
12
50k
GAIN
TRIM
499Ω*
1k
–15V
LT1124 • TA09

THE LT1124/LT1125 IS CAPABLE OF PROVIDING EXCITATION CURRENT DIRECTLY TO BIAS THE 350Ω BRIDGE AT 5V WITH ONLY 5V ACROSS THE BRIDGE (AS OPPOSED TO THE USUAL 10V) TOTAL POWER DISSIPATION AND BRIDGE WARM-UP DRIFT IS REDUCED. THE BRIDGE OUTPUT SIGNAL IS HALVED, BUT THE LT1124/LT1125 CAN AMPLIFY THE REDUCED SIGNAL ACCURATELY.

*RN60C FILM RESISTORS

SCHEMATIC DIAGRAM (1/2 LT1124, 1/4 LT1125)


V+
Q7
360μA
570μA
100μA
21k
200pF
21k
3.6k
3.6k
Q28
35pF
Q27
Q18
20
Q9
Q13
Q8
Q25
Q10
Q17
Q26
OUTPUT
Q19
Q20
900
20
V–
NON-INVERTING
INPUT (+)
Q1A
Q1B
Q2A
400
Q2B
Q30
67pF
20pF
INVERTING
INPUT (–)
Q3
V+
Q29
V+
Q22
Q11
Q23
Q12
Q15
Q16
Q24
200μA
200μA
100μA
200
6k
200
6k
50
V–
LT1124 • TA10

LINEAR TECHNOLOGY

LT1126/LT1127

Dual/Quad Decompensated Low Noise, High Speed Precision Op Amps

FEATURES

■ 100% Tested Low Voltage Noise	2.7nV/√Hz Typ 4.2nV/√Hz Max
■ Slew Rate	11V/μs Typ
■ Gain-Bandwidth Product	65MHz Typ
■ Offset Voltage, Prime Grade	70μV Max
Low Grade	100μV Max
■ High Voltage Gain	5 Million Min
■ Supply Current Per Amplifier	3.1mA Max
■ Common Mode Rejection	112dB Min
■ Power Supply Rejection	116dB Min
■ Available in 8-Pin SO Package	

APPLICATIONS

- Two and Three Op Amp Instrumentation Amplifiers
- Low Noise Signal Processing
- Active Filters
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Tape Head Preamplifiers
- Microphone Preamplifiers
- Accelerometer Amplifiers
- Infrared Detectors

DESCRIPTION

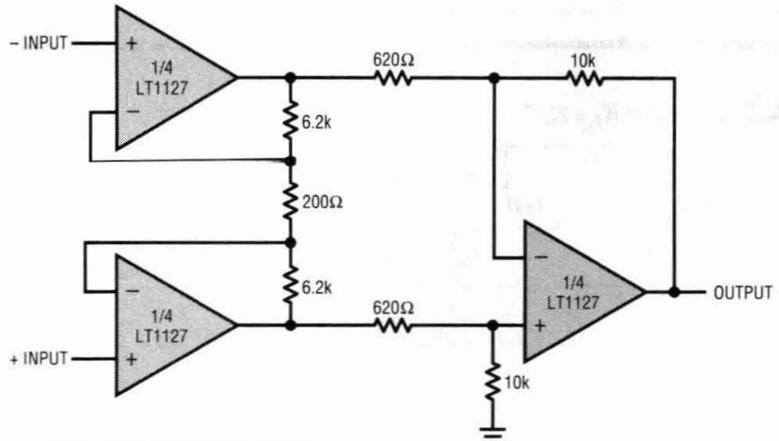
The LT1126 dual and LT1127 quad are high performance, decompensated op amps that offer higher slew rate and bandwidth than the LT1124 dual and the LT1125 quad operational amplifiers. The enhanced AC performance is available without degrading DC specs of the LT1124/LT1125. Both LT1126/LT1127 are stable in a gain of 10 or more.

In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Slew rate, gain-bandwidth, and 1kHz noise are 100% tested for each individual amplifier. Consequently, the specifications of even the lowest cost grades (the LT1126C and the LT1127C) have been enhanced.

Power consumption of the dual LT1126 is less than one half of two OP-37s. Low power and high performance in an 8-pin SO package makes the LT1126 a first choice for surface mounted systems and where board space is restricted.

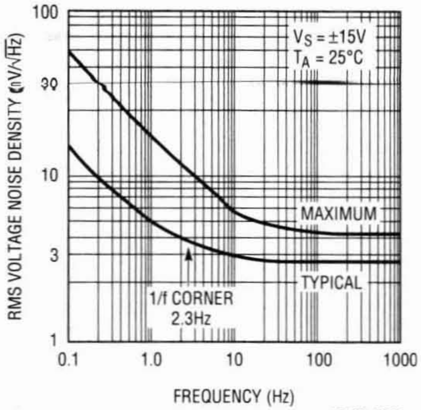
Protected by U.S. patents 4,775,884 and 4,837,496.

Low Noise, Wide Bandwidth Instrumentation Amplifier



GAIN = 1000, BANDWIDTH = 480kHz
INPUT REFERRED NOISE = 4.5nV/√Hz AT 1kHz, 6μV$_{RMS}$ OVER BANDWIDTH

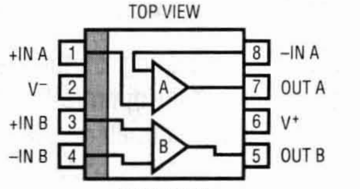
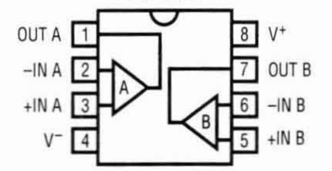
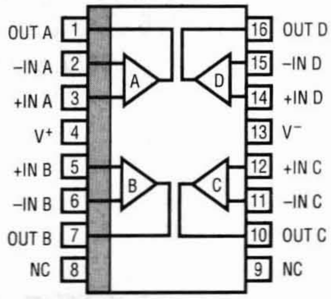
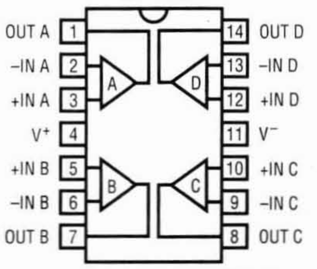
Voltage Noise vs Frequency



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Input Voltage	Equal to Supply Voltage
Output Short Circuit Duration	Indefinite
Differential Input Current (Note 5)	±25mA
Lead Temperature (Soldering, 10 sec.)	300°C
Operating Temperature Range	
LT1126AM/LT1126M LT1127AM/LT1127M	–55°C to 125°C
LT1126AC/LT1126C LT1127AC/LT1127C	–40°C to 85°C
Storage Temperature Range	
All Grades	–65°C to 150°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
TOP VIEW  S8 PACKAGE 8-LEAD PLASTIC SOIC NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-PIN DIP CONFIGURATION. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD LT1013DS8 SO PACKAGE PIN LOCATIONS LT1126 • POI01	LT1126CS8 S8 PART MARKING 1126	TOP VIEW  J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP LT1126 • POI02	LT1126AMJ8 LT1126MJ8 LT1126CJ8 LT1126ACN8 LT1126CN8
TOP VIEW  S PACKAGE 16-LEAD PLASTIC SOL LT1126 • POI03	LT1127CS	TOP VIEW  J PACKAGE 14-LEAD CERAMIC DIP N PACKAGE 14-LEAD PLASTIC DIP LT1126 • POI04	LT1127AMJ LT1127MJ LT1127CJ LT1127ACN LT1127CN

+IN A 1
V⁻ 2
+IN B 3
–IN B 4
8 –IN A
7 OUT A
6 V⁺
5 OUT B
A
B

OUT A 1
–IN A 2
+IN A 3
V⁻ 4
8 V⁺
7 OUT B
6 –IN B
5 +IN B
A
B

OUT A 1
–IN A 2
+IN A 3
V⁺ 4
+IN B 5
–IN B 6
OUT B 7
NC 8
16 OUT D
15 –IN D
14 +IN D
13 V⁻
12 +IN C
11 –IN C
10 OUT C
9 NC
A
B
C
D

OUT A 1
–IN A 2
+IN A 3
V⁺ 4
+IN B 5
–IN B 6
OUT B 7
14 OUT D
13 –IN D
12 +IN D
11 V⁻
10 +IN C
9 –IN C
8 OUT C
A
B
C
D

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 1)	LT1126AM/AC LT1127AM/AC MIN	TYP	MAX	LT1126M/C LT1127M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1126		20	70		25	100	µV
		LT1127		25	90		30	140	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		µV/Mo
I_{OS}	Input Offset Current	LT1126		5	15		6	20	nA
		LT1127		6	20		7	30	nA
I_B	Input Bias Current			±7	±20		±8	±30	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Notes 7 and 8)		70	200		70		nVp-p

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

			LT1126AM/AC LT1127AM/AC			LT1126M/C LT1127M/C			
SYMBOL	**PARAMETER**	**CONDITIONS (Note 1)**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
	Input Noise Voltage Density	f_O = 10Hz (Note 3) f_O = 1000Hz (Note 2)		3.0 2.7	5.5 4.2		3.0 2.7	5.5 4.2	nV/√Hz nV/√Hz
i_n	Input Noise Current Density	f_O = 10Hz f_O = 1000Hz		1.3 0.3			1.3 0.3		pA/√Hz pA/√Hz
V_{CM}	Input Voltage Range		±12.0	±12.8		±12.0	±12.8		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	112	126		106	124		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	116	126		110	124		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_O = \pm10V$ $R_L \geq 2k\Omega$, $V_O = \pm10V$	5.0 2.0	17.0 4.0		3.0 1.5	15.0 3.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	±13.0	±13.8		±12.5	±13.8		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	8.0	11		8.0	11		V/μs
GBW	Gain-Bandwidth Product	f_O = 10kHz (Note 2)	45	65		45	65		MHz
Z_O	Open Loop Output Resistance	$V_O = 0$, $I_O = 0$		75			75		Ω
I_S	Supply Current Per Amplifier			2.6	3.1		2.6	3.1	mA
	Channel Separation	f ≤ 10Hz (Note 8) $V_O = \pm10V$, $R_L = 2k\Omega$	134	150		130	150		dB

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

				LT1126AM LT1127AM			LT1126M LT1127M			
SYMBOL	**PARAMETER**	**CONDITIONS (Note 1)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	LT1126 LT1127	● ●		50 55	170 190		60 70	250 290	μV μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	(Note 4)	●		0.3	1.0		0.4	1.5	μV/°C
I_{OS}	Input Offset Current	LT1126 LT1127	● ●		18 18	45 55		20 20	60 70	nA nA
I_B	Input Bias Current		●		±18	±55		±20	±70	nA
V_{CM}	Input Voltage Range		●	±11.3	±12		±11.3	±12		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11.3V$	●	106	122		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	●	110	122		104	120		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_O = \pm10V$ $R_L \geq 2k\Omega$, $V_O = \pm10V$	● ●	3.0 1.0	10.0 3.0		2.0 0.7	10.0 2.0		V/μV V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12.5	±13.6		±12.0	±13.6		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Notes 2 and 6)	●	7.2	10		7.0	10		V/μs
I_S	Supply Current Per Amplifier		●		2.8	3.5		2.8	3.5	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1127s (or 100 LT1126s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: This parameter is 100% tested for each individual amplifier.

Note 3: This parameter is sample tested only.

Note 4: This parameter is not 100% tested.

Note 5: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.4V, the input current should be limited to 25mA.

Note 6: Slew rate is measured in $A_V = -10$; input signal is ±1V, output measured at ±5V.

Note 7: 0.1Hz to 10Hz noise can be inferred from the 10Hz noise voltage density test. See the test circuit and frequency response curve for 0.1Hz to 10Hz tester in the Applications Information section of the LT1007 or LT1028 datasheets.

Note 8: This parameter is guaranteed but not tested.

Note 9: The LT1126 and LT1127 are not tested and are not quality assurance sampled at −40°C and at 85°C. These specifications are guaranteed by design, correlation and/or inference from −55°C, 0°C, 25°C, 70°C and/or 125°C tests.

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

					LT1126AC LT1127AC			LT1126C LT1127C		
SYMBOL	**PARAMETER**	**CONDITIONS (Note 1)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	LT1126	●		35	120		45	170	μV
		LT1127	●		40	140		50	210	μV
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift	(Note 4)	●		0.3	1.0		0.4	1.5	μV/°C
I_{OS}	Input Offset Current	LT1126	●		6	25		7	35	nA
		LT1127	●		7	35		8	45	nA
I_B	Input Bias Current		●		±8	±35		±9	±45	nA
V_{CM}	Input Voltage Range		●	±11.5	±12.4		±11.5	±12.4		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11.5V$	●	109	125		102	122		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	●	112	125		107	122		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 10k\Omega$, $V_O = \pm10V$	●	4.0	15.0		2.5	14.0		V/μV
		$R_L \ge 2k\Omega$, $V_O = \pm10V$	●	1.5	3.5		1.0	2.5		V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12.5	±13.7		±12.0	±13.7		V
SR	Slew Rate	$R_L \ge 2k\Omega$ (Notes 2 and 6)	●	7.5	10.5		7.3	10.5		V/μs
I_S	Supply Current Per Amplifier		●		2.7	3.3		2.7	3.3	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-40°C \le T_A \le 85°C$, unless otherwise noted. (Note 9)

					LT1126AC LT1127AC			LT1126C LT1127C		
SYMBOL	**PARAMETER**	**CONDITIONS (Note 1)**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	LT1126	●		40	140		50	200	μV
		LT1127	●		45	160		55	240	μV
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Drift		●		0.3	1.0		0.4	1.5	μV/°C
I_{OS}	Input Offset Current	LT1126	●		15	40		17	55	nA
		LT1127	●		15	50		17	65	nA
I_B	Input Bias Current		●		±15	±50		±17	±65	nA
V_{CM}	Input Voltage Range		●	±11.4	±12.2		±11.4	±12.2		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11.4V$	●	107	124		101	121		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4V$ to $\pm18V$	●	111	124		106	121		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \ge 10k\Omega$, $V_O = \pm10V$	●	3.5	12.0		2.2	12.0		V/μV
		$R_L \ge 2k\Omega$, $V_O = \pm10V$	●	1.2	3.2		0.8	2.3		V/μV
V_{OUT}	Maximum Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12.5	±13.6		±12.0	±13.6		V
SR	Slew Rate	$R_L \ge 2k\Omega$ (Note 6)	●	7.3	10.2		7.1	10.2		V/μs
I_S	Supply Current Per Amplifier		●		2.8	3.4		2.8	3.4	mA

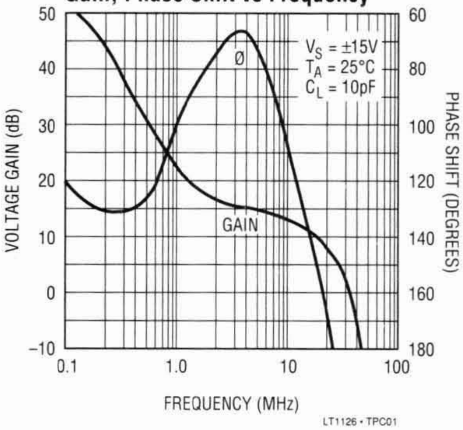
TYPICAL PERFORMANCE CHARACTERISTICS

The typical behavior of many LT1126/LT1127 parameters is identical to the LT1124/LT1125. Please refer to the LT1124/LT1125 data sheet for the following performance characteristics:

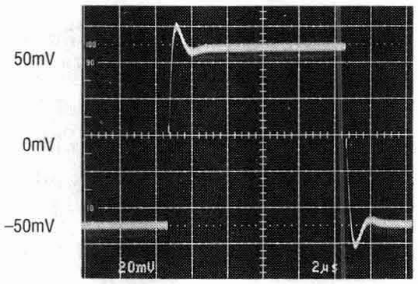
0.1Hz to 10Hz Voltage Noise
0.01Hz to 1Hz Voltage Noise
Current Noise vs Frequency
Input Bias or Offset Current vs Temperature
Output Short Circuit Current vs Time
Input Bias Current Over the Common Mode Range
Voltage Gain vs Temperature
Input Offset Voltage Drift Distribution
Offset Voltage Drift with Temperature of Representative Units
Output Voltage Swing vs Load Current
Common Mode Limit vs Temperature
Channel Separation vs Frequency
Warm-Up Drift
Power Supply Rejection Ratio vs Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

Gain, Phase Shift vs Frequency

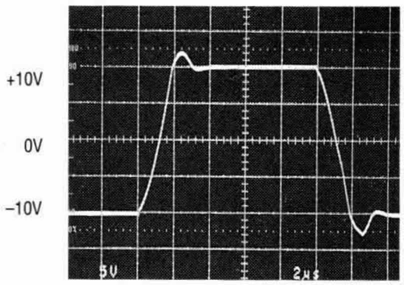


Small Signal Transient Response



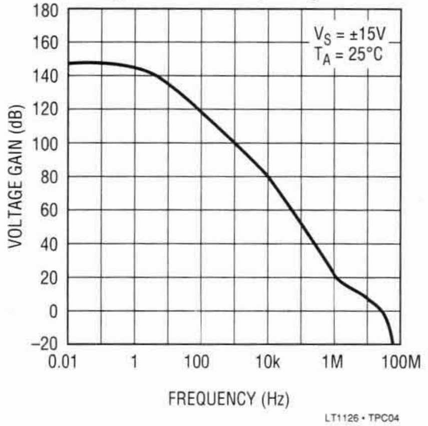
A_{VCL} = −10, V_S = ±15V OR ±5V
C_L = 15pF

Large Signal Transient Response

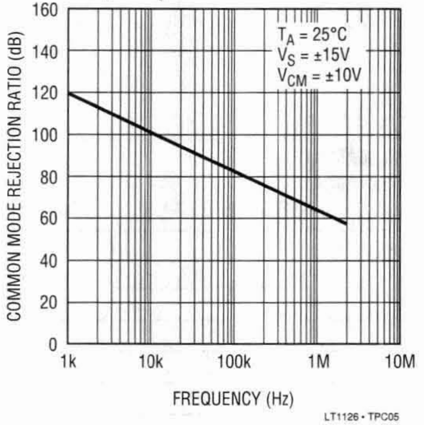


A_{VCL} = −10, V_S = ±15V

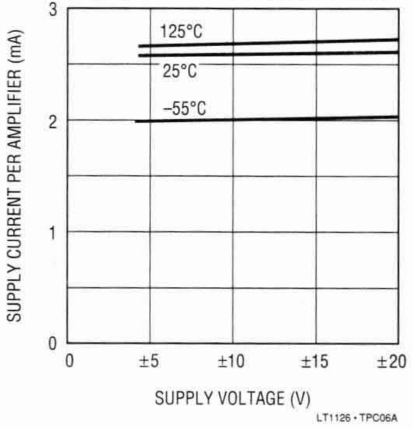
Voltage Gain vs Frequency



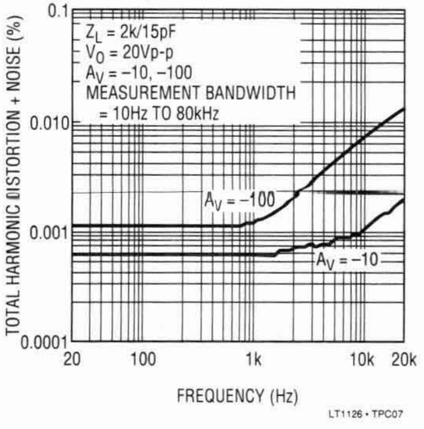
Common Mode Rejection Ratio vs Frequency



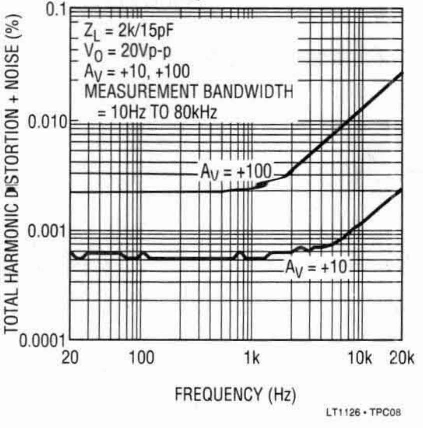
Supply Current vs Supply Voltage



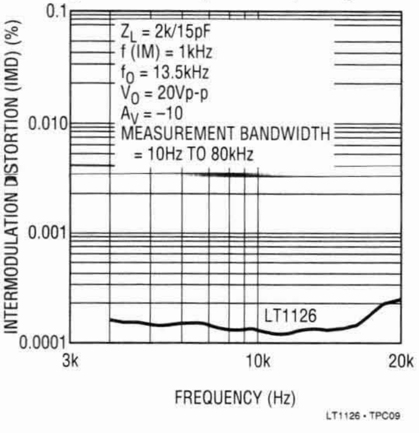
Total Harmonic Distortion and Noise vs Frequency for Inverting Gain



Total Harmonic Distortion and Noise vs Frequency for Non-Inverting Gain



Intermodulation Distortion (CCIF Method)* vs Frequency



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*See LT1115 data sheet for definition of CCIF testing

APPLICATIONS INFORMATION

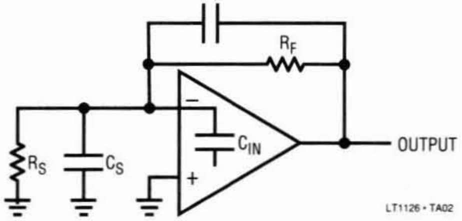
Matching Specifications

In many applications the performance of a system depends on the matching between two op amps, rather than the individual characteristics of the two devices. The three op amp instrumentation amplifier configuration shown in this data sheet is an example. Matching characteristics are not 100% tested on the LT1126/LT1127.

Some specifications are guaranteed by definition. For example, 70µV maximum offset voltage implies that mismatch cannot be more than 140µV. 112dB (= 2.5µV/V) CMRR means that worst case CMRR match is 106dB (5µV/V). However, the following table can be used to estimate the expected matching performance between the two sides of the LT1126, and between amplifiers A and D, and between amplifiers B and C of the LT1127.

High Speed Operation

When the feedback around the op amp is resistive (R_F), a pole will be created with R_F, the source resistance and capacitance (R_S, C_S), and the amplifier input capacitance ($C_{IN} \approx 2pF$). In low closed loop gain configurations and with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S (C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.

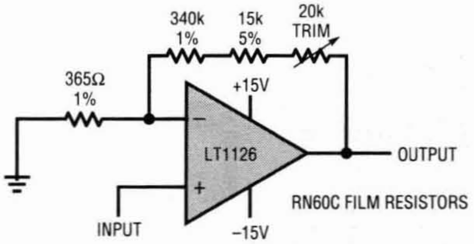


Expected Match

PARAMETER		LT1126AM/AC LT1127AM/AC 50% YIELD	 98% YIELD	LT1126M/C LT1127M/C 50% YIELD	 98% YIELD	UNITS
V_{OS} Match, ΔV_{OS}	LT1126	20	110	30	130	µV
	LT1127	30	150	50	180	µV
Temperature Coefficient Match		0.35	1.0	0.5	1.5	µV/°C
Average Non-Inverting I_B		6	18	7	25	nA
Match of Non-Inverting I_B		7	22	8	30	nA
CMRR Match		126	115	123	112	dB
PSRR Match		127	118	127	114	dB

TYPICAL APPLICATIONS

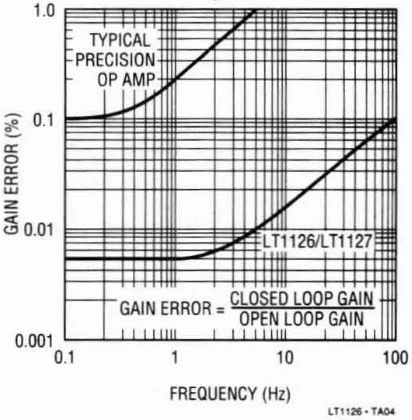
Gain 1000 Amplifier with 0.01% Accuracy, DC to 5Hz



THE HIGH GAIN AND WIDE BANDWIDTH OF THE LT1126/LT1127 IS USEFUL IN LOW FREQUENCY HIGH CLOSED LOOP GAIN AMPLIFIER APPLICATIONS. A TYPICAL PRECISION OP AMP MAY HAVE AN OPEN LOOP GAIN OF ONE MILLION WITH 500kHz BANDWIDTH. AS THE GAIN ERROR PLOT SHOWS, THIS DEVICE IS CAPABLE OF 0.1% AMPLIFYING ACCURACY UP TO 0.3Hz ONLY. EVEN INSTRUMENTATION RANGE SIGNALS CAN VARY AT A FASTER RATE. THE LT1126/LT1127 "GAIN PRECISION — BANDWIDTH PRODUCT" IS 330 TIMES HIGHER, AS SHOWN.

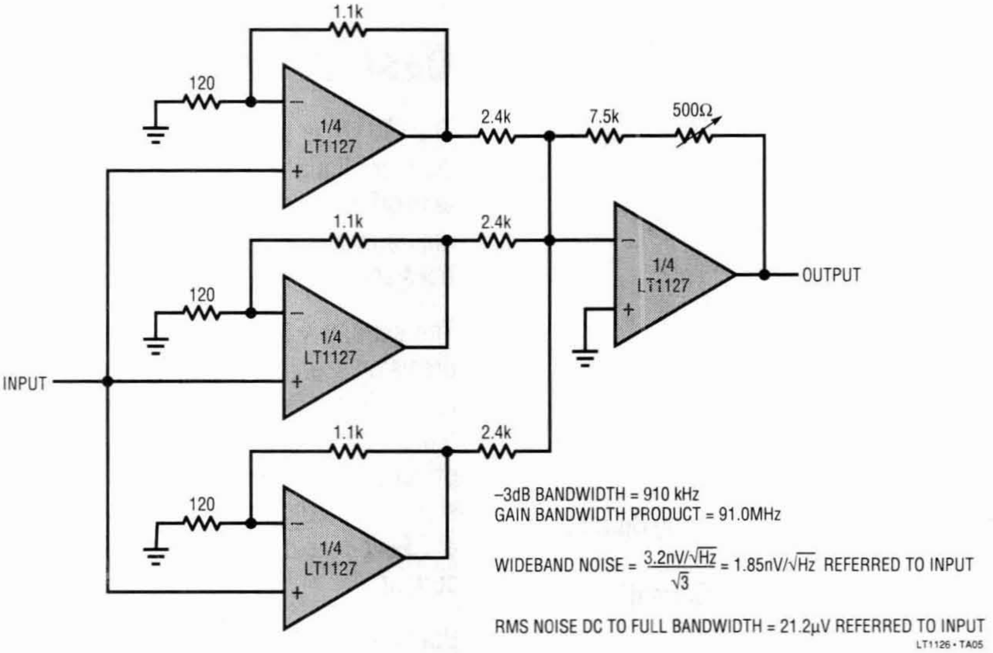
LT1126 • TA03

Gain Error vs Frequency
Closed Loop Gain = 1000



TYPICAL APPLICATIONS

Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance


1.1k
120
1/4
LT1127
2.4k
7.5k
500Ω
1.1k
2.4k
120
1/4
LT1127
1/4
LT1127
OUTPUT
INPUT
1.1k
2.4k
120
1/4
LT1127

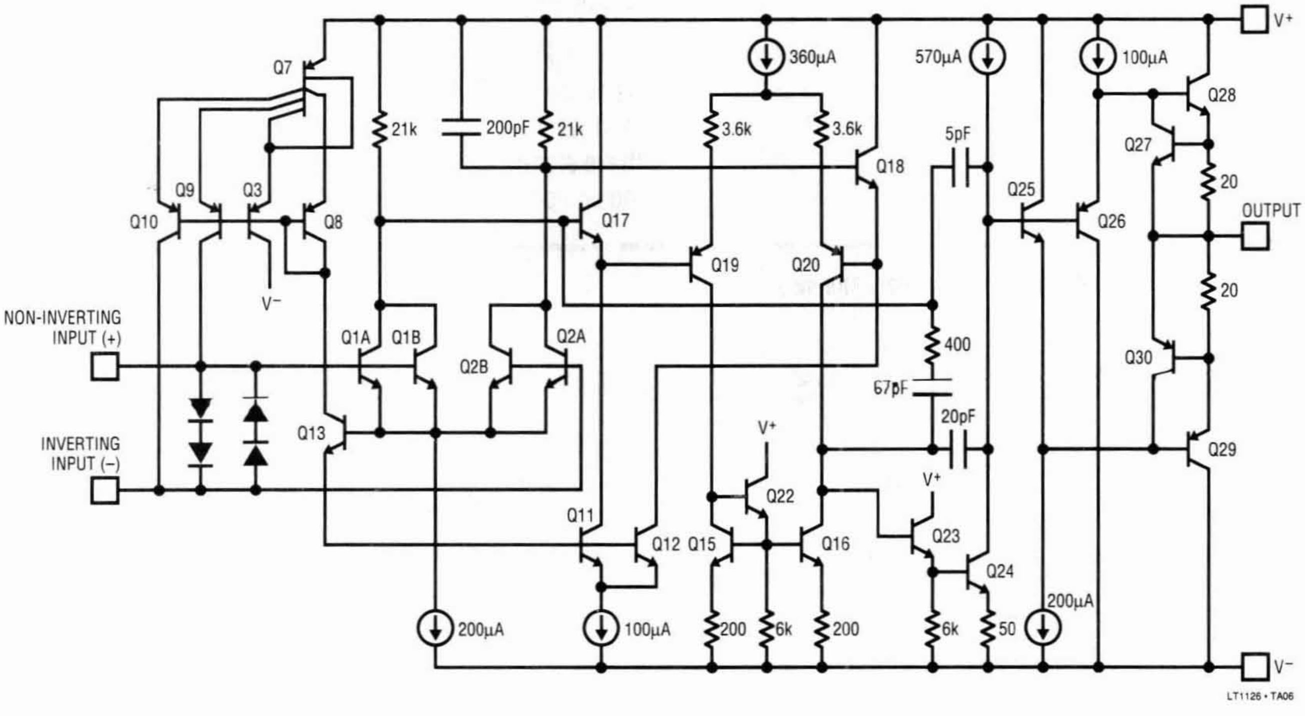
–3dB BANDWIDTH = 910 kHz
GAIN BANDWIDTH PRODUCT = 91.0MHz

WIDEBAND NOISE = $\frac{3.2nV/\sqrt{Hz}}{\sqrt{3}}$ = 1.85nV/$\sqrt{Hz}$ REFERRED TO INPUT

RMS NOISE DC TO FULL BANDWIDTH = 21.2μV REFERRED TO INPUT

LT1126 • TA05

SCHEMATIC DIAGRAM (1/2 LT1126, 1/4 LT1127)


V+
Q7
360μA
570μA
100μA
Q28
21k
200pF
21k
3.6k
3.6k
5pF
Q27
Q18
20
Q9
Q3
Q25
OUTPUT
Q10
Q8
Q17
Q26
Q19
Q20
V–
20
NON-INVERTING INPUT (+)
Q1A
Q1B
Q2A
400
Q2B
Q30
67pF
Q13
20pF
V+
Q29
INVERTING INPUT (–)
Q22
V+
Q11
Q12
Q15
Q16
Q23
Q24
200μA
200μA
100μA
200
6k
200
6k
50
V–

LT1126 • TA06

LT1178/LT1179

17μA Max, Dual and Quad, Single Supply, Precision Op Amps

FEATURES

- 17μA Max Supply Current per Amplifier
- 70μV Max Offset Voltage
- 250pA Max Offset Current
- 5nA Max Input Bias Current
- 0.9μVp-p 0.1Hz to 10Hz Voltage Noise
- 1.5pAp-p 0.1Hz to 10Hz Current Noise
- 0.5μV/°C Offset Voltage Drift
- 85kHz Gain-Bandwidth-Product
- 0.04V/μs Slew Rate
- Single Supply Operation
  - Input Voltage Range Includes Ground
  - Output Swings to Ground while Sinking Current
  - No Pull Down Resistors are Needed
- Output Sources and Sinks 5mA Load Current

APPLICATIONS

- Battery or Solar Powered Systems
  - Portable Instrumentation
  - Remote Sensor Amplifier
  - Satellite Circuitry
- Micropower Sample and Hold
- Thermocouple Amplifier
- Micropower Filters

DESCRIPTION

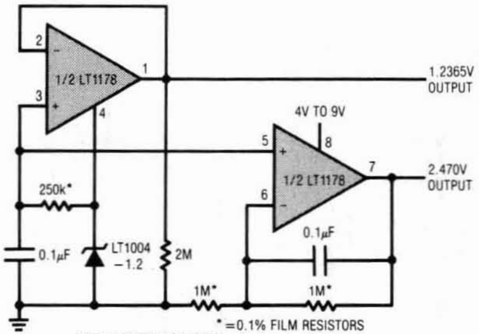
The LT1178 is a micropower dual op amp in the standard 8-pin configuration; the LT1179 is a micropower quad op amp offered in the standard 14-pin packages. Both devices are optimized for single supply operation at 5V. Specifications are also provided at ± 15V supplies.

The extremely low supply current is combined with true precision specifications: offset voltage is 30μV, offset current is 50pA. Both offset parameters have low drift with temperature. The 1.5pAp-p current noise and picoampere offset current permit the use of megaohm level source resistors without introducing serious errors. Voltage noise, at 0.9μVp-p, is remarkably low considering the low supply current.

Both the LT1178 and LT1179 can be operated from a single supply (as low as one lithium cell or two Ni-cad batteries). The input range goes below ground. The all-NPN output stage swings to within a few millivolts of ground while sinking current—no power consuming pull down resistors are needed.

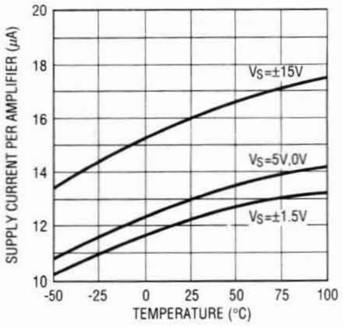
For applications where three times higher supply current is acceptable, the micropower LT1077 single, LT1078 dual and LT1079 quad are recommended. The LT1077/78/79 have significantly higher bandwidth, slew rate; lower voltage noise and better output drive capability.

Self-Buffered, Dual Output, Micropower Reference



* = 0.1% FILM RESISTORS
TOTAL BATTERY CURRENT = 28μA
OUTPUT ACCURACY = ± 0.4% MAX
TEMPERATURE COEFFICIENT = 20ppm/°C
LOAD REGULATION = 25ppm/mA, $I_L \leq 5mA$, $V^+ \geq 5V$
LINE REGULATION = 10ppm/V

Supply Current vs Temperature

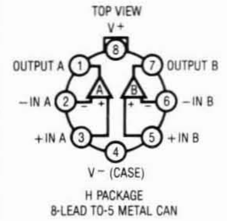


ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ± 22V
Differential Input Voltage .... ± 30V
Input Voltage .... Equal to Positive Supply Voltage
.... 5V Below Negative Supply Voltage
Output Short Circuit Duration .... Indefinite

Operating Temperature Range
LT1178I/LT1179I .... – 40°C to 85°C
LT1178C/LT1178S/LT1179C/LT1179S .... 0°C to 70°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

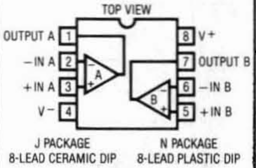
PACKAGE/ORDER INFORMATION


TOP VIEW
V+
8
OUTPUT A 1
7 OUTPUT B
– IN A 2
6 – IN B
+ IN A 3
5 + IN B
4
A
B
V – (CASE)

H PACKAGE
8-LEAD TO-5 METAL CAN

ORDER PART NUMBER

LT1178ACH
LT1178CH

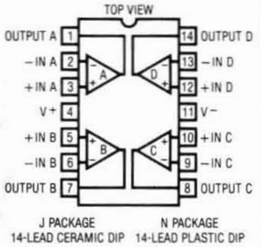

TOP VIEW
OUTPUT A 1
– IN A 2
+ IN A 3
V – 4
8 V+
7 OUTPUT B
6 – IN B
5 + IN B
A
B

J PACKAGE
8-LEAD CERAMIC DIP

N PACKAGE
8-LEAD PLASTIC DIP

ORDER PART NUMBER

LT1178ACJ8
LT1178CJ8
LT1178ACN8
LT1178CN8
LT1178IN8

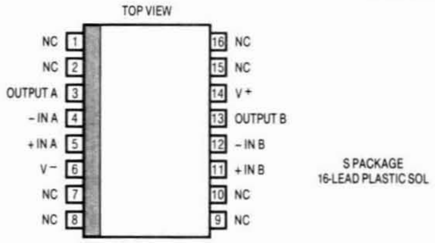

TOP VIEW
OUTPUT A 1
– IN A 2
+ IN A 3
V+ 4
+ IN B 5
– IN B 6
OUTPUT B 7
14 OUTPUT D
13 – IN D
12 + IN D
11 V –
10 + IN C
9 – IN C
8 OUTPUT C
A
B
C
D

J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

ORDER PART NUMBER

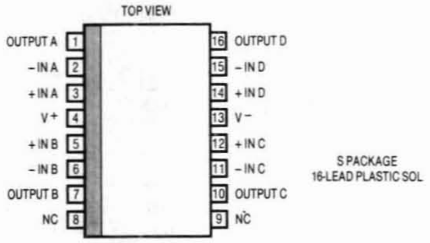
LT1179ACJ
LT1179CJ
LT1179ACN
LT1179CN
LT1179IN


TOP VIEW
NC 1
NC 2
OUTPUT A 3
– IN A 4
+ IN A 5
V – 6
NC 7
NC 8
16 NC
15 NC
14 V+
13 OUTPUT B
12 – IN B
11 + IN B
10 NC
9 NC

S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER

LT1178S


TOP VIEW
OUTPUT A 1
– IN A 2
+ IN A 3
V+ 4
+ IN B 5
– IN B 6
OUTPUT B 7
NC 8
16 OUTPUT D
15 – IN D
14 + IN D
13 V –
12 + IN C
11 – IN C
10 OUTPUT C
9 NC

S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER

LT1179S

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS (NOTE 1)	LT1178AC/1179AC MIN	LT1178AC/1179AC TYP	LT1178AC/1179AC MAX	LT1178I/C/S/1179I/C/S MIN	LT1178I/C/S/1179I/C/S TYP	LT1178I/C/S/1179I/C/S MAX	UNITS
V_{OS}	Input Offset Voltage	LT1178		30	70		40	120	μV
		LT1179		35	100		40	150	μV
		LT1178S					80	450	μV
		LT1179S					90	600	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.5			0.6		μV/Mo
I_{OS}	Input Offset Current			0.05	0.25		0.05	0.35	nA
I_B	Input Bias Current			3	5		3	6	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.9	2.0		0.9		μVp-p
	Input Noise Voltage Density	f_o = 10Hz (Note 2)		50	75		50		nV/√Hz
		f_o = 1000Hz (Note 2)		49	65		49		nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		1.5	2.5		1.5		pAp-p
	Input Noise Current Density	f_o = 10Hz (Note 2)		0.03	0.07		0.03		pA/√Hz
		f_o = 1000Hz		0.01			0.01		pA/√Hz
	Input Resistance	(Note 3)							
	Differential Mode		0.8	2.0		0.6	2.0		GΩ
	Common-Mode			12			12		GΩ
	Input Voltage Range		3.5	3.9		3.5	3.9		V
			0	– 0.3		0	– 0.3		V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3.5V	93	103		90	102		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.2V to 12V	94	104		92	104		dB

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = 25°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS (NOTE 1)	LT1178AC/1179AC			LT1178I/C/S/1179I/C/S			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.03V$ to 4V, No Load (Note 3)	140	700		110	700		V/mV
		$V_O = 0.03V$ to 3.5V, $R_L = 50k$	80	200		70	200		V/mV
	Maximum Output Voltage Swing	Output Low, No Load		6.5	9		6.5	9	mV
		Output Low, 2k to GND		0.2	0.6		0.2	0.6	mV
		Output Low, $I_{SINK} = 100\mu A$		120	160		120	160	mV
		Output High, No Load	4.2	4.4		4.2	4.4		V
		Output High, 2k to GND	3.5	3.8		3.5	3.8		V
SR	Slew Rate	$A_V = +1, C_L = 10pF$ (Note 3)	0.013	0.025		0.013	0.025		V/μs
GBW	Gain Bandwidth Product	$f_0 \leq 5kHz$		60			60		kHz
I_S	Supply Current per Amplifier			13	18		14	21	μA
		$V_S = \pm 1.5V, V_O = 0V$		12	17		13	20	μA
	Channel Separation	$\Delta V_{IN} = 3V, R_L = 10k$		130			130		dB
	Minimum Supply Voltage	(Note 4)		2.0	2.2		2.0	2.2	V

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, -40°C \leq T_A \leq 85°C$ for I grades, $0°C \leq T_A \leq 70°C$ for S grades, unless noted. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		LT1178I/1179I			LT1178S/1179S			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1178	●		80	315		120	650	μV
		LT1179	●		80	345		130	800	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.6	3.0		0.8	4.5	μV/°C
I_{OS}	Input Offset Current		●		0.07	0.7		0.06	0.50	nA
I_B	Input Bias Current		●		4	8		3	7	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0.05V$ to 3.2V I grade $V_{CM} = 0V$ to 3.4V S grade	●	84	98		86	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = 3.0V$ to 12V I grade $V_S = 2.5V$ to 12V S grade	●	86	100		88	102		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to 4V, No Load (Note 3)	●	55	350		80	500		V/mV
		$V_O = 0.05V$ to 3.5V, $R_L = 50k$	●	35	130		45	160		V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●		9	13		8	11	mV
		Output Low, $I_{SINK} = 100\mu A$	●		160	220		140	190	mV
		Output High, No Load	●	3.9	4.2		4.1	4.3		V
		Output High, 2k to GND	●	3.0	3.7		3.3	3.8		V
I_S	Supply Current per Amplifier		●		15	27		15	24	μA

ELECTRICAL CHARACTERISTICS $V_S = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, 0°C \leq T_A \leq 70°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS		LT1178AC/1179AC			LT1178C/1179C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1178	●		50	170		65	250	μV
		LT1179	●		60	200		70	290	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.5	2.2		0.6	3.0	μV/°C
I_{OS}	Input Offset Current		●		0.06	0.35		0.06	0.50	nA
I_B	Input Bias Current		●		3	6		3	7	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = 0V$ to 3.4V	●	90	101		86	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.5V$ to 12V	●	90	102		88	102		dB
A_{VOL}	Large Signal Voltage Gain	$V_O = 0.05V$ to 4V, No Load (Note 3)	●	105	500		80	500		V/mV
		$V_O = 0.05V$ to 3.5V, $R_L = 50K$	●	55	160		45	160		V/mV
	Maximum Output Voltage Swing	Output Low, No Load	●		8	11		8	11	mV
		Output Low, $I_{SINK} = 100\mu A$	●		140	190		140	190	mV
		Output High, No Load	●	4.1	4.3		4.1	4.3		V
		Output High, 2k to GND	●	3.3	3.8		3.3	3.8		V
I_S	Supply Current per Amplifier		●		14	21		15	24	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS	LT1178AC/1179AC MIN	TYP	MAX	LT1178I/C/S/1179I/C/S MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	 LT1178S LT1179S		80	350		100 150 160	480 900 1050	μV μV μV
I_{OS}	Input Offset Current			0.05	0.25		0.05	0.35	nA
I_B	Input Bias Current			3	5		3	6	nA
	Input Voltage Range		13.5 −15.0	13.9 −15.3		13.5 −15.0	13.9 −15.3		V V
CMRR	Common-Mode Rejection Ratio	V_{CM} + 13.5V, −15V	97	106		94	106		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ±18V	96	112		94	112		dB
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 50k V_O = ±10V, No Load	300 600	1200 2500		250 400	1000 2500		V/mV V/mV
V_{OUT}	Maximum Output Voltage Swing	R_L = 50k R_L = 2k	±13.0 ±11.0	±14.2 ±12.7		±13.0 ±11.0	±14.2 ±12.7		V V
SR	Slew Rate	A_V = +1	0.02	0.04		0.02	0.04		V/μs
GBW	Gain Bandwidth Product	$f_O \leq$ 5kHz		85			85		kHz
I_S	Supply Current per Amplifier			16	21		17	25	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $-40°C \leq T_A \leq 85°C$ for I grades, $0°C \leq T_A \leq 70°C$ for S grades, unless noted.

SYMBOL	PARAMETER	CONDITIONS		LT1178I/1179I MIN	TYP	MAX	LT1178S/1179S MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1178 LT1179	● ●		130 130	740 740		190 200	1150 1300	μV μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.7	4.0		0.9	5.5	μV/°C
I_{OS}	Input Offset Current		●		0.07	0.7		0.06	0.35	nA
I_B	Input Bias Current		●		4	8		3	7	nA
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 50k	●	100	500		150	750		V/mV
CMRR	Common-Mode Rejection Ratio	V_{CM} = +13V, −14.9V	●	88	103		91	104		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ±18V	●	88	109		91	110		dB
	Maximum Output Voltage Swing	R_L = 5k	●	±11.0	±13.5		±11.0	±13.5		V
I_S	Supply Current per Amplifier		●		19	30		18	28	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, 0°C \leq T_A \leq 70°C$, unless noted.

SYMBOL	PARAMETER	CONDITIONS		LT1178AC/1179AC MIN	TYP	MAX	LT1178C/1179C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		100	480		130	660	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)	●		0.6	2.8		0.7	4.0	μV/°C
I_{OS}	Input Offset Current		●		0.06	0.35		0.06	0.35	nA
I_B	Input Bias Current		●		3	6		3	7	nA
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L = 50k	●	200	800		150	750		V/mV
CMRR	Common-Mode Rejection Ratio	V_{CM} = 13V, −15V	●	94	104		91	104		dB
PSRR	Power Supply Rejection Ratio	V_S = 5V, 0V to ±18V	●	93	110		91	110		dB
	Maximum Output Voltage Swing	R_L = 5k	●	±11.0	±13.6		±11.0	±13.6		V
I_S	Supply Current per Amplifier		●		17	24		18	28	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Typical parameters are defined as the 60% yield of parameter distributions of individual amplifiers; i.e., out of 100 LT1179s (or 100 LT1178s) typically 240 op amps (or 120) will be better than the indicated specification.

Note 2: This parameter is tested on a sample basis only. All noise parameters are tested with V_S = ±2.5, V_O = 0V.

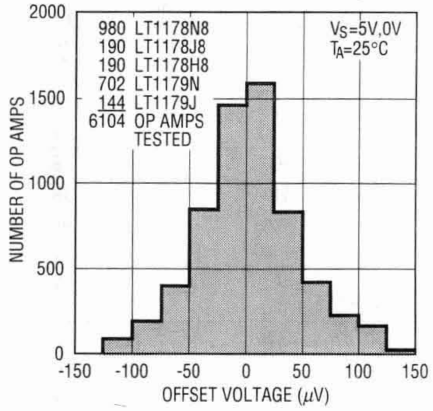
Note 3: This parameter is guaranteed by design and is not tested.

Note 4: Power supply rejection ratio is measured at the minimum supply voltage. The op amps actually work at 1.7V supply but with a typical offset skew of −300μV.

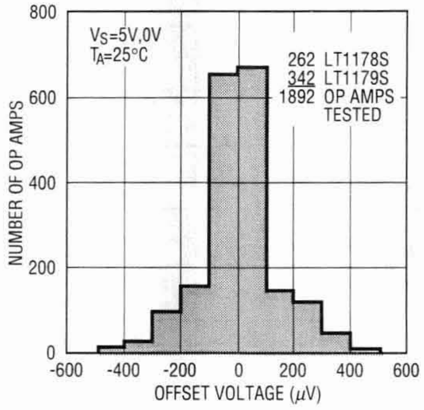
Note 5: This parameter is not 100% tested.

Note 6: During testing at −40°C, the 5V power supply turn on time is less than 0.5 seconds.

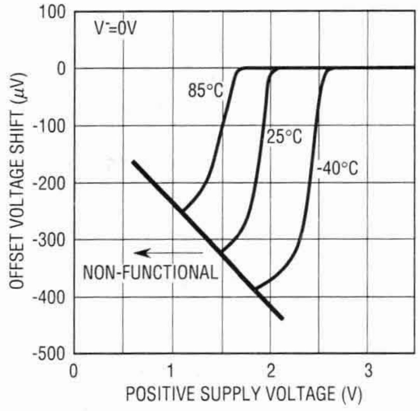
TYPICAL PERFORMANCE CHARACTERISTICS



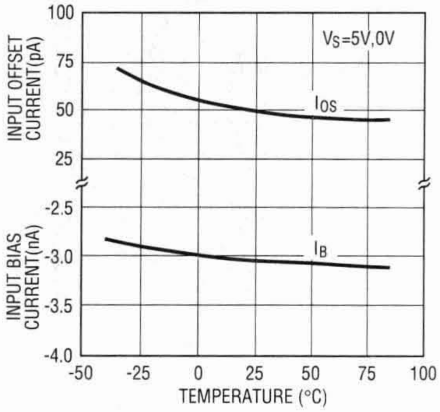
Input Offset Voltage Distribution N, J, H Package



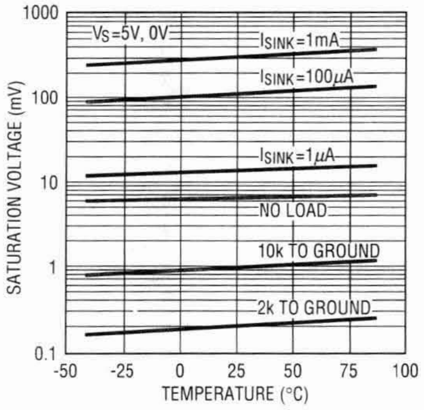
Input Offset Voltage Distribution Surface Mount Package



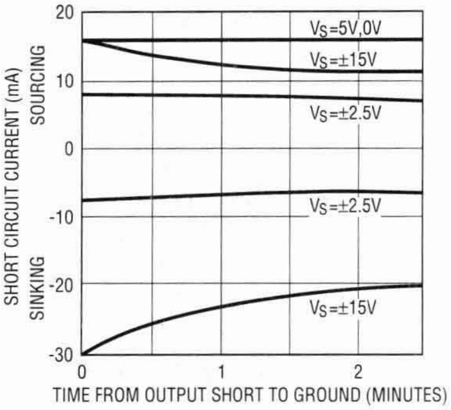
Minimum Supply Voltage



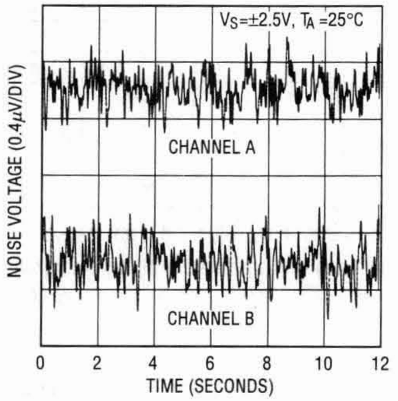
Input Bias and Offset Currents vs Temperature



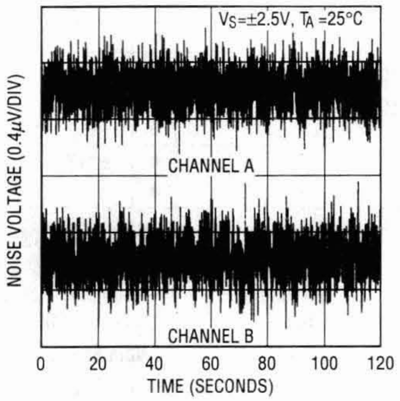
Output Saturation vs Temperature vs Sink Current



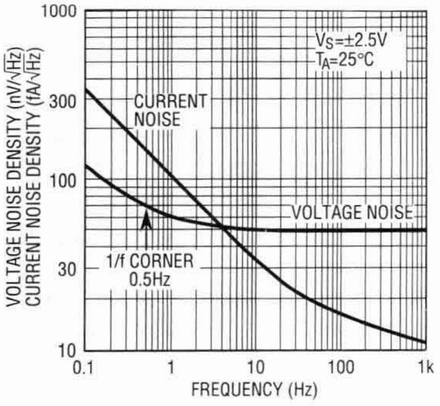
Short Circuit Current



0.1Hz to 10Hz Noise



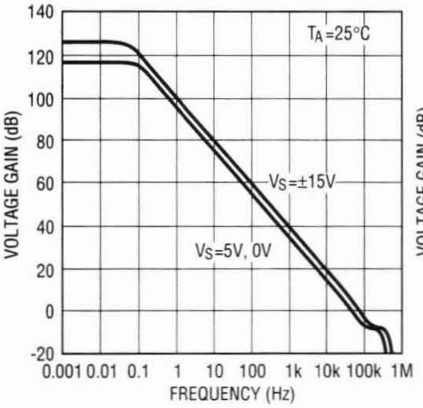
0.01Hz to 10Hz Noise



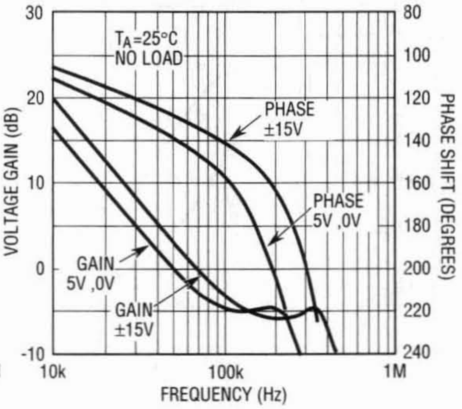
Noise Spectrum

TYPICAL PERFORMANCE CHARACTERISTICS

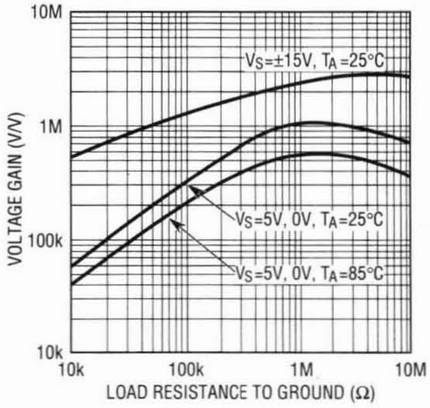
Voltage Gain vs Frequency



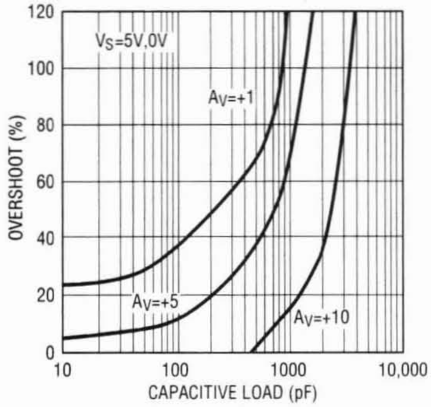
Gain, Phase vs Frequency



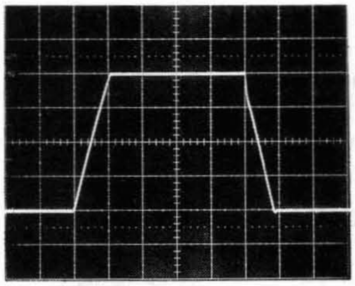
Voltage Gain vs Load Resistance



Capacitive Load Handling

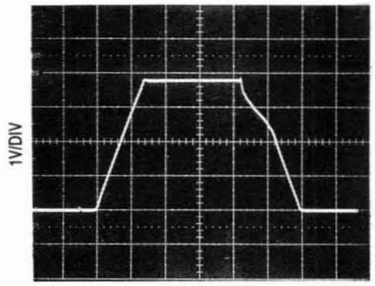


Large Signal Transient Response $V_S = ±15V$



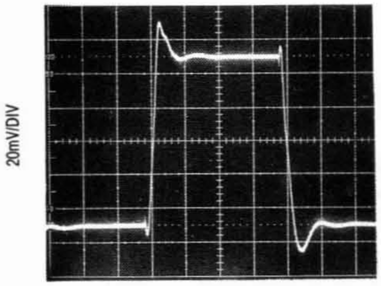
500µs/DIV
$A_V = +1, C_L = 12pF$

Large Signal Transient Response $V_S = 5V, 0V$



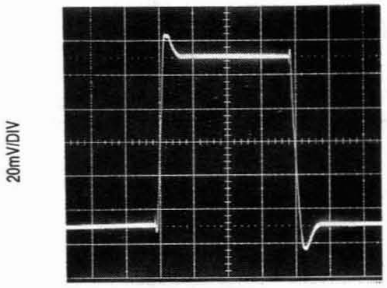
100µs/DIV
INPUT PULSE = 0V TO 3.8V
$A_V = +1, C_L = 12pF$

Small Signal Transient Response $V_S = ±2.5V$



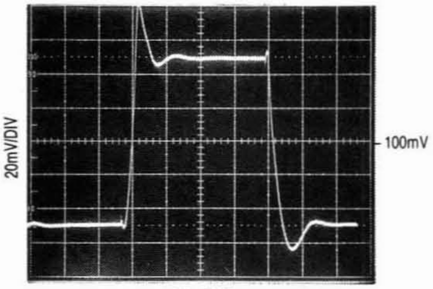
20µs/DIV
$A_V = +1, C_L = 12pF$

Small Signal Transient Response $V_S = ±15V$



20µs/DIV
$A_V = +1, C_L = 12pF$

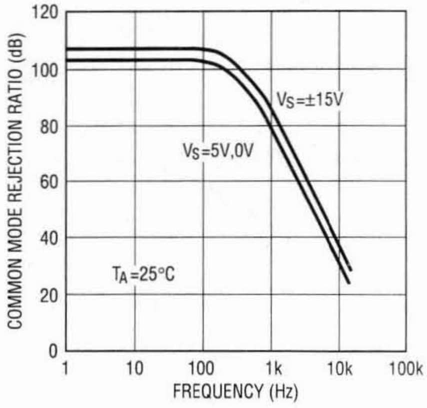
Small Signal Transient Response $V_S = 5V, 0V$



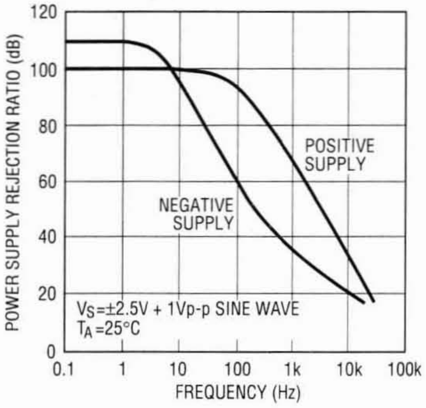
20µs/DIV
$A_V = +1, C_L = 12pF$, INPUT 50 TO 150mV

TYPICAL PERFORMANCE CHARACTERISTICS

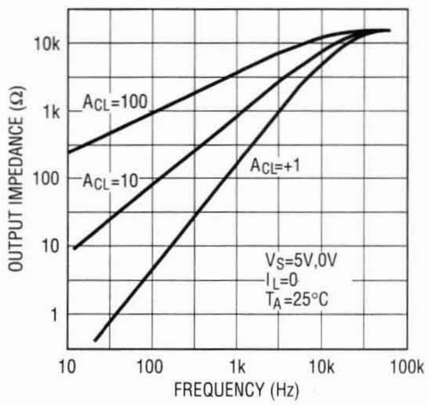
Common Mode Rejection Ratio vs Frequency



Power Supply Rejection Ratio vs Frequency



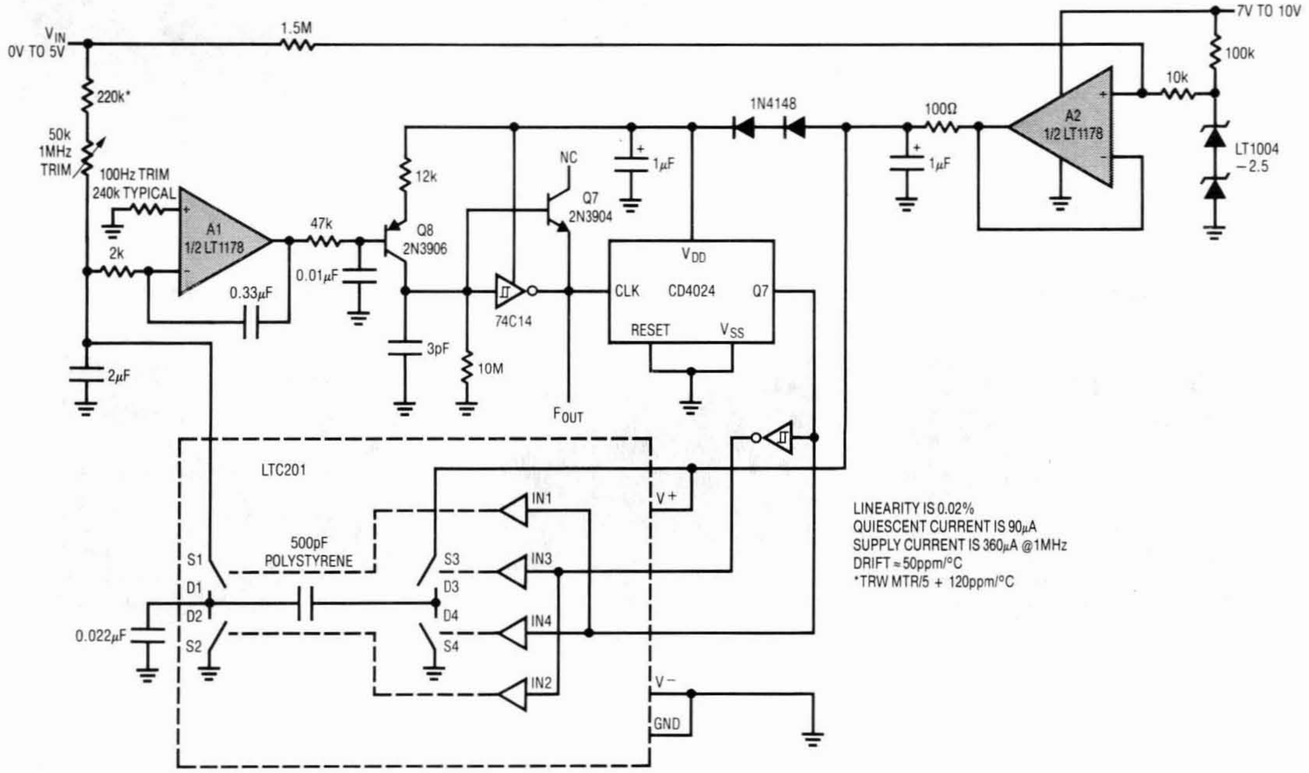
Closed Loop Output Impedance



APPLICATIONS INFORMATION

Please see the LT1078/LT1079 data sheet for applications information. All comments relating to specifications, single supply operation and phase reversal protection are directly applicable to the LT1178/LT1179.

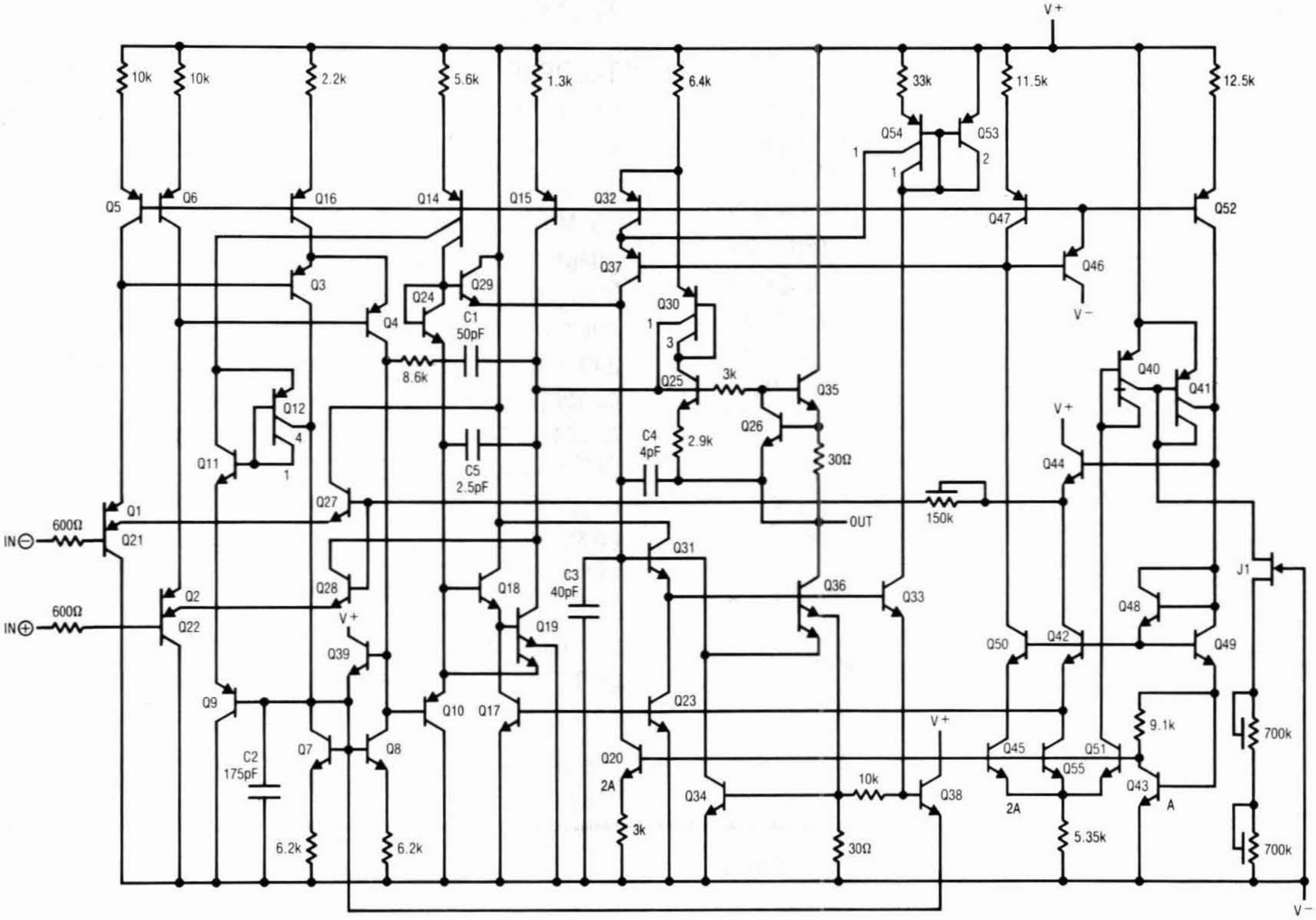
Micropower 100Hz to 1MHz V-to-F Converter


V_{IN}
0V TO 5V
1.5M
7V TO 10V
100k
10k
220k*
50k
1MHz
TRIM
100Hz TRIM
240k TYPICAL
2k
A1
1/2 LT1178
0.33µF
47k
0.01µF
12k
Q8
2N3906
NC
Q7
2N3904
1µF
1N4148
100Ω
1µF
A2
1/2 LT1178
LT1004
–2.5
V_{DD}
CLK
CD4024
Q7
RESET
V_{SS}
74C14
3pF
10M
F_{OUT}
2µF
LTC201
V+
IN1
S1
D1
D2
S2
500pF
POLYSTYRENE
S3
D3
D4
S4
IN3
IN4
IN2
V–
GND
0.022µF

LINEARITY IS 0.02%
QUIESCENT CURRENT IS 90µA
SUPPLY CURRENT IS 360µA @1MHz
DRIFT ≈ 50ppm/°C
*TRW MTR/5 + 120ppm/°C

SIMPLIFIED SCHEMATIC

1/2 LT1178
1/4 LT1179


V+
10k
10k
2.2k
5.6k
1.3k
6.4k
33k
11.5k
12.5k
Q54
Q53
1
1
2
Q5
Q6
Q16
Q14
Q15
Q32
Q47
Q52
Q37
Q46
V−
Q3
Q29
Q24
C1
50pF
Q30
1
3
Q4
8.6k
Q25
3k
Q35
Q40
Q41
Q12
4
C4
4pF
2.9k
Q26
30Ω
V+
Q11
1
C5
2.5pF
Q44
Q1
Q27
OUT
150k
IN⊖
600Ω
Q21
Q31
J1
C3
40pF
Q36
Q28
Q18
Q33
Q48
Q2
IN⊕
600Ω
Q22
V+
Q19
Q50
Q42
Q49
Q39
Q9
Q10
Q17
Q23
9.1k
700k
C2
175pF
Q7
Q8
Q20
V+
Q45
Q51
Q55
2A
10k
Q43
Q34
Q38
2A
A
6.2k
6.2k
3k
30Ω
5.35k
700k
V−

OP-270/OP-470

Dual/Quad Low Noise, Precision Operational Amplifiers

FEATURES

■ Low Noise	5nV/√Hz @ 1kHz Max
■ Input Offset Voltage	OP-270: 75μV Max OP-470: 400μV Max
■ Low Offset Voltage Drift	OP-270: 1μV/°C Max OP-470: 2μV/°C Max
■ Very High Gain	OP-270: 1500V/mV Min OP-470: 1000V/mV Min
■ Outstanding CMRR	OP-270: 106dB Min OP-470: 110dB Min
■ Slew Rate	3.0V/μs Typ
■ Gain Bandwidth Product	6MHz Typ
■ Industry Standard Pinouts	

APPLICATIONS

- Two and Three Op Amp Instrumentation Amplifiers
- Low Noise Signal Processing
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Accelerometer Amplifiers
- Infrared Detectors

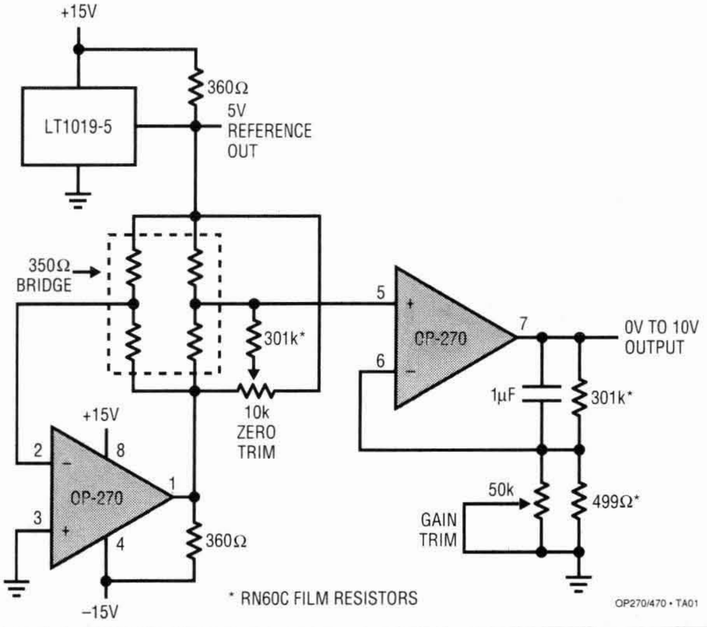
DESCRIPTION

The OP-270 dual and OP-470 quad are high performance op amps with 80nVp-p noise, from 0.1Hz to 10Hz, offering comparable performance to the industry standard OP-27.

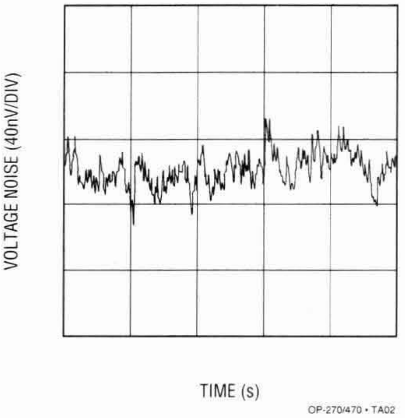
The OP-270 (OP-470) feature input offset voltage below 75μV (400μV) and offset drift under 1μV/°C (2μV/°C), guaranteed over the full military temperature range. Open-loop gain of the OP-270 (OP-470) is over 1.5 million (1.0 million) into a 10kΩ load ensuring excellent gain accuracy and linearity, even in high-gain applications. Input bias current is under ±20nA (±25nA) which reduces errors due to signal source resistance. The OP-270's (OP-470's) CMRR of over 106dB (110dB) and PSRR of less than 3.2μV/V (1.8μV/V) significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the dual OP-270 (quad OP-470) is one-third less than two (four) OP-27's, a significant advantage for power conscious applications. The OP-270 and OP-470 are unity-gain stable with a gain bandwidth product of 6MHz and a slew rate of 3.0V/μs.

For applications requiring higher performance, see the LT1124 and LT1125 data sheets.

Strain Gauge Signal Conditioner with Bridge Excitation



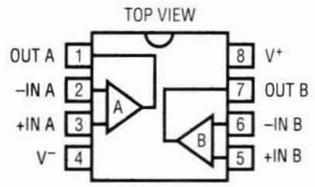
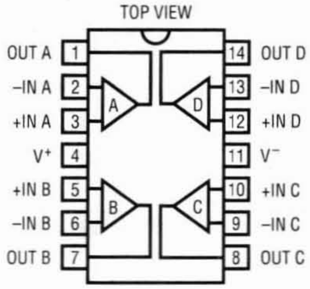
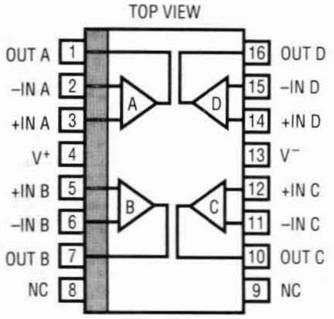
0.1Hz to 10Hz Voltage Noise



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage (Note 4)	±1.0V
Differential Input Current (Note 4)	±25mA
Input Voltages	Equal to Supply Voltages
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
OP270A/OP470A	−55°C to 125°C
OP270E/OP470E OP270G/OP470G	−40°C to 85°C
Storage Temperature Range	
All Grades	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

 TOP VIEW OUT A 1 −IN A 2 +IN A 3 V⁻ 4 8 V⁺ 7 OUT B 6 −IN B 5 +IN B A B OP270/470 • POI03J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP	 TOP VIEW OUT A 1 −IN A 2 +IN A 3 V⁺ 4 +IN B 5 −IN B 6 OUT B 7 14 OUT D 13 −IN D 12 +IN D 11 V⁻ 10 +IN C 9 −IN C 8 OUT C A B C D OP270/470 • POI02J PACKAGE 14-LEAD CERAMIC DIP N PACKAGE 14-LEAD PLASTIC DIP	 TOP VIEW OUT A 1 −IN A 2 +IN A 3 V⁺ 4 +IN B 5 −IN B 6 OUT B 7 NC 8 16 OUT D 15 −IN D 14 +IN D 13 V⁻ 12 +IN C 11 −IN C 10 OUT C 9 NC A B C D OP270/470 • POI01S PACKAGE 16-LEAD PLASTIC SOL
ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER
OP-270AJ8 OP-270EJ8 OP-270GN8	OP-470AJ OP-470EJ OP-470GN	OP-470GS

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

			OP-270A/E			OP-470A/E			OP-270G OP-470G			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	OP-270		10	75					50	250	µV
		OP-470					100	400		400	1000	µV
I_{OS}	Input Offset Current	OP-270 $V_{CM} = 0V$		5	15					6	20	nA
		OP-470 $V_{CM} = 0V$					6	20		12	30	nA
I_B	Input Bias Current	$V_{CM} = 0V$		±7	±20		±7	±25		±15	±60	nA
e_n p-p	Input Noise Voltage	0.1Hz to 10Hz (Note 1)		80	200		80	200		80	200	nVp-p
e_n	Input Noise Voltage Density	$f_O = 10Hz$ (Note 2)		3.6	6.5		3.6	6.5		3.6	6.5	nV/√Hz
		$f_O = 100Hz$ (Note 2)		3.2	5.5		3.2	5.5		3.2	5.5	nV/√Hz
		$f_O = 1000Hz$ (Note 2)		3.2	5.0		3.2	5.0		3.2	5.0	nV/√Hz

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-270A/E			OP-470A/E			OP-270G OP-470G			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
i_n	Input Noise Current Density	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$		1.5 0.5 0.4			1.5 0.5 0.4			1.5 0.5 0.4		$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 10k\Omega$ $V_{OUT} = \pm10V$, $R_L = 2k\Omega$	1500 750	5000 2000		1000 500	5000 2000		800 400	2000 1000		V/mV V/mV
V_{CM}	Input Voltage Range	(Note 3)	±12	±12.5		±12	±12.5		±12	±12.5		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	±12	±13.5		±12	±13.5		±12	±13.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	106	125		110	125		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$		0.56	3.2		0.56	1.8		1.0	5.6	μV/V
SR	Slew Rate		1.7	3.0		1.7	3.0		1.7	3.0		V/μs
I_S	Supply Current	OP-270 No Load OP-470 No Load		4.5	6.5		 9.0	 11.0		4.0 9.0	6.5 11.0	mA mA
GBW	Gain Bandwidth Product	$A_V = +10$		6			6			6		MHz
CS	Channel Separation	$V_{OUT} = 20Vp\text{-}p$, $f_O = 10Hz$ (Note 1)	125	175		125	175		125	175		dB
C_{IN}	Input Capacitance			3			3			3		pF

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-55°C \leq T_A \leq 125°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		OP-270A			OP-470A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●		30	175		140	600	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift		●		0.2	1.0		0.4	2.0	μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		10	45		10	55	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±15	±60		±15	±50	nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 10k\Omega$, $V_{OUT} = \pm10V$ $R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	● ●	750 400	3000 1500		750 400	3000 1500		V/mV V/mV
V_{CM}	Input Voltage Range	(Note 3)	●	±11	±12		±11	±12		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	±12	±13		±12	±13		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11V$	●	100	120		100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	●		1.0	5.6		1.0	5.6	μV/V
I_S	Supply Current All Amplifiers	No Load	●		5.0	7.5		10	13	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This parameter is guaranteed but not 100% tested.

Note 2: This parameter is sample tested only.

Note 3: This parameter is guaranteed by the CMRR test.

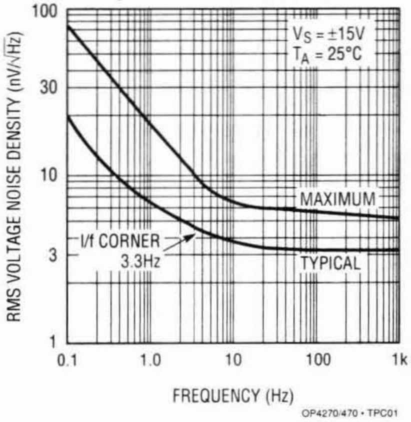
Note 4: The inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±1.4V, the input current should be limited to 25mA.

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $-40°C \le T_A \le 85°C$, unless otherwise noted.

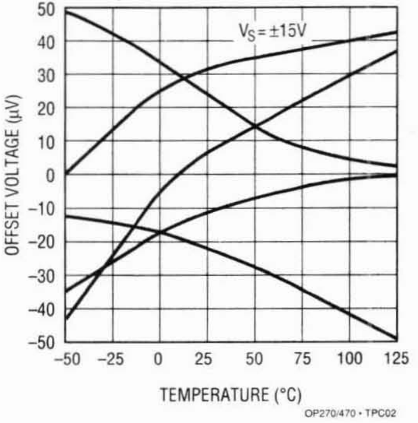
					OP-270E			OP-470E			OP-270G OP-470G		
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	OP-270	●		25	150					100	400	μV
		OP-470	●					120	500		500	1500	μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift	OP-270	●		0.2	1.0					0.7	3.0	μV/°C
		OP-470	●					0.4	2.0		2.0		μV/°C
I_{OS}	Input Offset Current	$V_{CM} = 0V$	●		15	30		17	20		17	50	nA
I_B	Input Bias Current	$V_{CM} = 0V$	●		±15	±60		±17	±50		±18	±75	nA
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L \ge 10k\Omega$	●	1000	2000		800	2000		600	1500		V/mV
		$V_{OUT} = \pm10V$, $R_L \ge 2k\Omega$	●	500	1000		400	1000		300	800		V/mV
V_{CM}	Input Voltage Range	(Note 3)	●	±11	±12		±11	±12		±11	±12		V
V_{OUT}	Output Voltage Swing	$R_L \ge 2k\Omega$	●	±12	±13		±12	±13		±12	±13		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm11V$	●	100	120		100	120		90	110		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	●		0.7	5.6		0.7	5.6		1.8	10	μV/V
I_S	Supply Current All Amplifiers	OP-270 No Load	●		4.8	7.2					4.8	7.2	mA
		OP-470 No Load	●					9.6	13		9.6	13	mA

TYPICAL PERFORMANCE CHARACTERISTICS

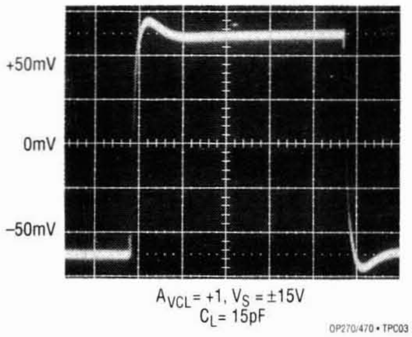
Voltage Noise vs Frequency



Offset Voltage Drift with Temperature of Representative Units



Small Signal Transient Response



$A_{VCL} = +1$, $V_S = \pm15V$
$C_L = 15pF$

NOTES

SECTION 2—AMPLIFIERS

HIGH SPEED AMPLIFIERS

LT1190, Ultra High Speed Operational Amplifier (Av ≥ 1) 2-126
LT1191, Ultra High Speed Operational Amplifier (Av ≥ 1) 2-137
LT1192, Ultra High Speed Operational Amplifier (Av ≥ 5) 2-148
LT1193, Video Difference Amplifier, Adjustable Gain 2-159
LT1194, Video Difference Amplifier, Gain of 10 2-171
LT1200, Low Power High Speed Operational Amplifier 2-182
LT1217, Low Power High Speed Current Feedback Amplifier 2-190
LT1220, Very High Speed Operational Amplifier (Av ≥ 1) 2-198
LT1221, Very High Speed Operational Amplifier (Av ≥ 4) 2-210
LT1222, Low Noise, Very High Speed Operational Amplifier (Av ≥ 10) 2-218
LT1223, 100MHz Current Feedback Amplifier 2-226
LT1224, Very High Speed Operational Amplifier (Av ≥ 1) 2-237
LT1225, Very High Speed Operational Amplifier (Av ≥ 5) 2-245
LT1226, Low Noise Very High Speed Operational Amplifier (Av ≥ 25) 2-253
LT1227, 140MHz Video Current Feedback Amplifier 13-65
LT1228, 100MHz Current Feedback Amplifier with DC Gain Control 2-261
LT1229/LT1230, Dual and Quad 100MHz Current Feedback Amplifiers 2-280

Ultra High Speed Operational Amplifier

FEATURES

■ Gain Bandwidth Product, $A_V = +1$	50MHz
■ Slew Rate	450V/µs
■ Low Cost	
■ Output Current	±50mA
■ Settling Time	140ns to 0.1%
■ Differential Gain Error	0.1%, ($R_L = 1k$)
■ Differential Phase Error	0.06°, ($R_L = 1k$)
■ High Open Loop Gain	15V/mV Min
■ Single Supply +5V Operation	
■ Output Shutdown	

APPLICATIONS

- Video Cable Drivers
- Video Signal Processing
- Fast Integrators
- Pulse Amplifiers
- D/A Current to Voltage Conversion

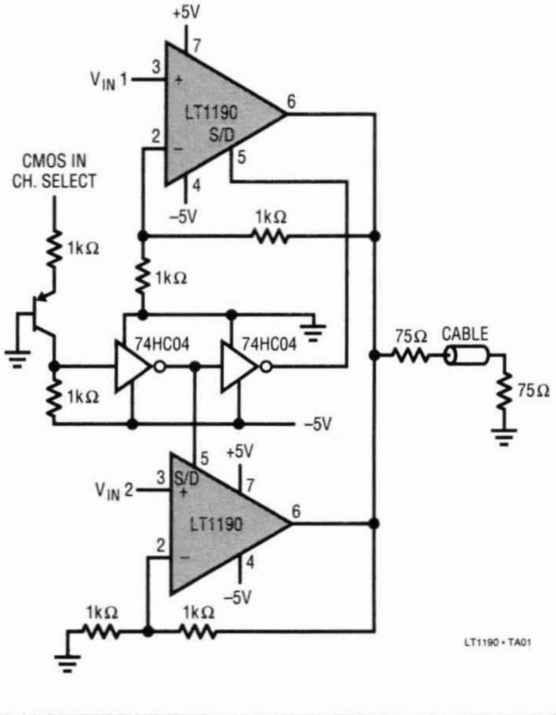
DESCRIPTION

The LT1190 is a video operational amplifier optimized for operation on ±5V, and a single +5V supply. Unlike many high speed amplifiers, this amplifier features high open loop gain, over 85dB, and the ability to drive heavy loads to a full power bandwidth of 20MHz at 7Vp-p. In addition to its very fast slew rate, the LT1190 features a unity gain stable bandwidth of 50MHz, and a 75° phase margin, making it extremely easy to use.

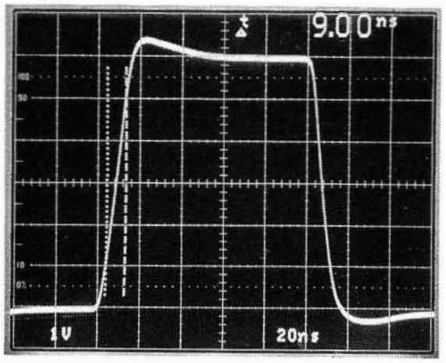
Because the LT1190 is a true operational amplifier, it is an ideal choice for wideband signal conditioning, fast integrators, active filters, and applications requiring speed, accuracy, and low cost.

The LT1190 is available in 8-pin miniDIPs and SO packages with standard pinouts. The normally unused pin 5 is used for a shutdown feature that shuts off the output and reduces power dissipation to a mere 15mW.

Video MUX Cable Driver



Inverter Pulse Response



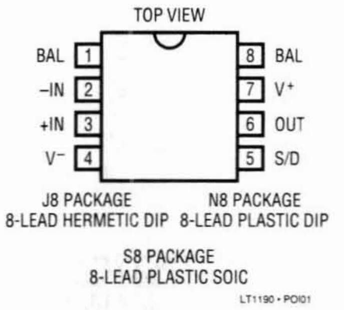
$A_V = -1$, $C_L = 10pF$ SCOPE PROBE

LT1190 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	18V
Differential Input Voltage	±6V
Input Voltage	$\pm V_S$
Output Short Circuit Duration (Note 1)	Continuous
Operating Junction Temperature Range	
LT1190M	−55°C to 150°C
LT1190C	0°C to 150°C
Max. Junction Temperature	See Pkg. Descriptions
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1190MJ8 LT1190CJ8 LT1190CN8 LT1190CS8
S8 PART MARKING
1190

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER		CONDITIONS	LT1190M/C			UNITS
				MIN	TYP	MAX	
V_{OS}	Input Offset Voltage				3.0	10.0	mV
I_{OS}	Input Offset Current				0.2	1.7	μA
I_B	Input Bias Current				±0.5	±2.5	μA
e_n	Input Noise Voltage		$f_O = 10kHz$		50		$nV/\sqrt{Hz}$
i_n	Input Noise Current		$f_O = 10kHz$		4.0		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Differential Mode			130		kΩ
		Common Mode			5.0		MΩ
C_{IN}	Input Capacitance		$A_V = +1$		2.2		pF
	Input Voltage Range		(Note 2)	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio		$V_{CM} = -2.5V$ to $+3.5V$	60	70		dB
PSRR	Power Supply Rejection Ratio		$V_S = \pm 2.375V$ to $\pm 8.0V$	60	70		dB
A_{VOL}	Large Signal Voltage Gain		$R_L = 1k$, $V_O = \pm 3.0V$	10	22		V/mV
			$R_L = 100\Omega$, $V_O = \pm 3.0V$	2.5	6		
			$V_S = \pm 8V$, $R_L = 100\Omega$, $V_O = \pm 5V$	3.5	12		
V_{OUT}	Output Voltage Swing		$V_S = \pm 5V$, $R_L = 1k$	±3.7	±4.0		V
			$V_S = \pm 8V$, $R_L = 1k$	±6.7	±7.0		
SR	Slew Rate		$A_V = -1$, $R_L = 1k$, (Note 3, 8)	325	450		V/μs
FPBW	Full Power Bandwidth		$V_O = 6Vp\text{-}p$, (Note 4)	17.2	23.9		MHz
GBW	Gain Bandwidth Product				50		MHz
t_{r1}, t_{f1}	Rise Time, Fall Time		$A_V = +50$, $V_O = \pm 1.5V$, 20% to 80%, (Note 8)	175	250	325	ns
t_{r2}, t_{f2}	Rise Time, Fall Time		$A_V = +1$, $V_O = \pm 125mV$, 10% to 90%		1.9		ns
t_{PD}	Propagation Delay		$A_V = +1$, $V_O = \pm 125mV$, 50% to 50%		2.4		ns
	Overshoot		$A_V = +1$, $V_O = \pm 125mV$		5		%
t_s	Settling Time		3V Step, 0.1%, (Note 5)		140		ns
Diff A_V	Differential Gain		$R_L = 150\Omega$, $A_V = +2$, (Note 6)		0.35		%
Diff Ph	Differential Phase		$R_L = 150\Omega$, $A_V = +2$, (Note 6)		0.16		Deg. p-p

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A = 25°C$, $C_L \leq 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1190M/C MIN	 TYP	 MAX	UNITS
I_S	Supply Current			32	38	mA
	Shutdown Supply Current	Pin 5 at V^-		1.3	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		20	50	μA
t_{on}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		100		ns
t_{off}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		400		ns

ELECTRICAL CHARACTERISTICS

$V_S+ = +5V$, $V_S- = 0V$, $V_{CM} = +2.5V$, $T_A = 25°C$, $C_L \leq 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1190M/C MIN	 TYP	 MAX	UNITS
V_{OS}	Input Offset Voltage				3.0	11.0	mV
I_{OS}	Input Offset Current				0.2	1.2	μA
I_B	Input Bias Current				±0.5	±1.5	μA
	Input Voltage Range	(Note 2)		+2.0		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = +2.0V$ to $+3.5V$		55	70		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 100\Omega$ to Ground, $V_O = +1.0V$ to $+3.0V$		2.5	7.0		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$ to Ground	V_{OUT} High	3.6	3.8		V
			V_{OUT} Low		0.25	0.4	
SR	Slew Rate	$A_V = -1$, $V_O = +1V$ to $+3V$			250		V/μs
GBW	Gain Bandwidth Product				47		MHz
I_S	Supply Current			24.5	29	36	mA
	Shutdown Supply Current	Pin 5 at V^-			1.2	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			20	50	μA

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $-55°C \leq T_A \leq 125°C$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1190M MIN	 TYP	 MAX	UNITS
V_{OS}	Input Offset Voltage		●		5.0	14.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		16		μV/°C
I_{OS}	Input Offset Current		●		0.2	2.0	μA
I_B	Input Bias Current		●		±0.5	±2.5	μA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	55	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 5.0V$	●	55	70		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 1k$, $V_O = \pm 3.0V$	●	8	16		V/mV
		$R_L = 100\Omega$, $V_O = \pm 3.0V$	●	1.0	2.5		
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	±3.7	±3.9		V
I_S	Supply Current		●		32	38	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 7)	●		1.5	2.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		μA

ELECTRICAL CHARACTERISTICS $V_S = \pm5V$, $0°C \le T_A \le 70°C$, pin 5 open circuit unless otherwise noted.

				LT1190C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage		●		3.0	11.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		16		µV/°C
I_{OS}	Input Offset Current		●		0.2	1.7	µA
I_B	Input Bias Current		●		±0.5	±2.5	µA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	58	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm5.0V$	●	58	70		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 1k$, $V_O = \pm3.0V$	●	9	20		V/mV
		$R_L = 100\Omega$, $V_O = \pm3.0V$	●	2.0	6.0		
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	±3.70	±3.9		V
I_S	Supply Current		●		32	38	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 7)	●		1.4	2.1	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: Exceeding the input common mode range may cause the output to invert.

Note 3: Slew rate is measured between ±1V on the output, with a ±3V input step.

Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

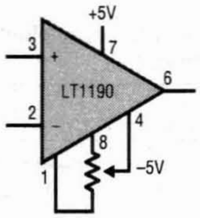
Note 5: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985. $A_V = -1$, $R_L = 1k$.

Note 6: NTSC (3.58MHz). For $R_L = 1k$, Diff $A_V = 0.1\%$, Diff Ph = 0.06°.

Note 7: See Applications section for shutdown at elevated temperatures. Do not operate the shutdown above $T_J > 125°C$.

Note 8: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

Optional Offset Nulling Circuit

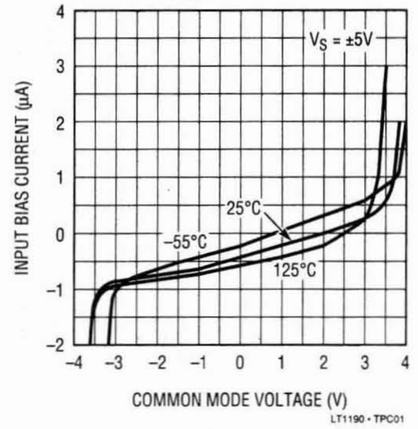


INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±150mV
RANGE WITH A 1kΩ TO 10kΩ POTENTIOMETER.

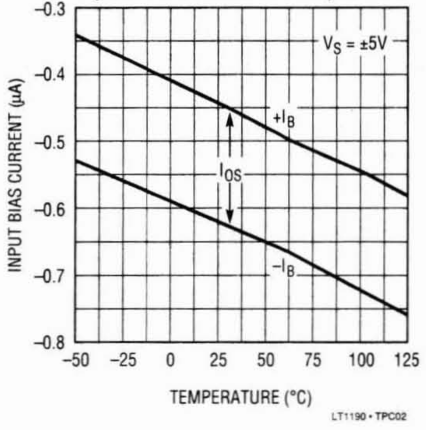
LT1190 • TA03

TYPICAL PERFORMANCE CHARACTERISTICS

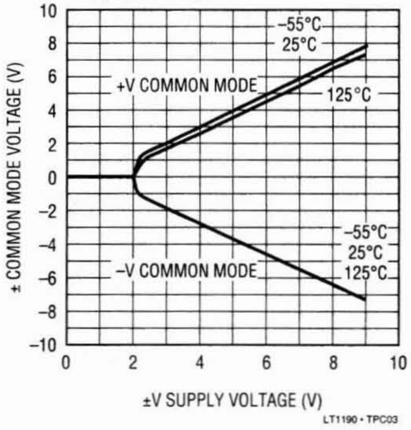
Input Bias Current vs Common Mode Voltage



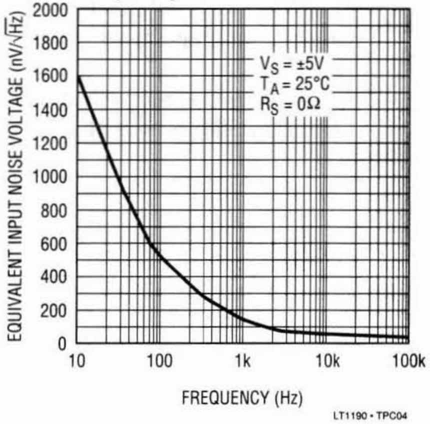
Input Bias Current vs Temperature



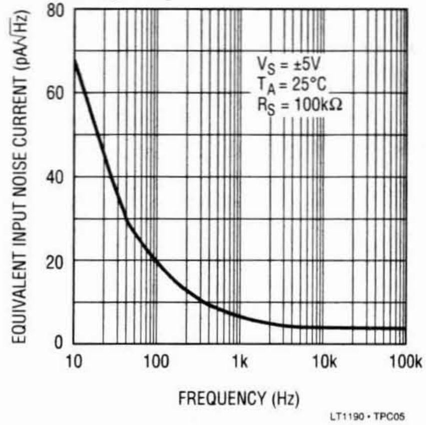
Common Mode Voltage vs Supply Voltage



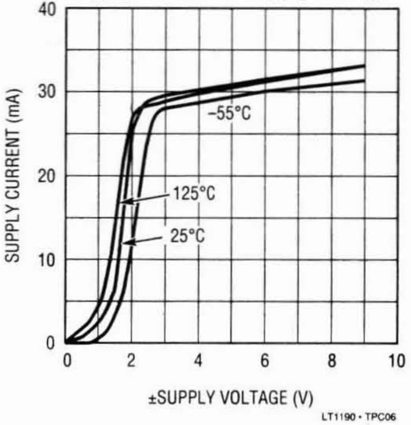
Equivalent Input Noise Voltage vs Frequency



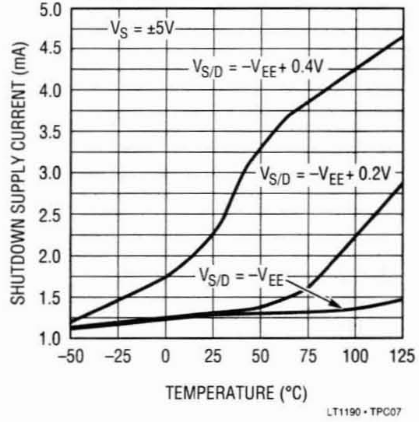
Equivalent Input Noise Current vs Frequency



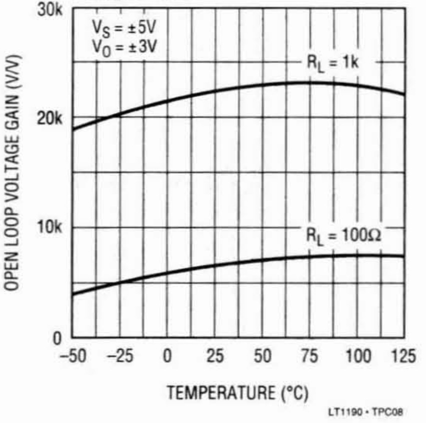
Supply Current vs Supply Voltage



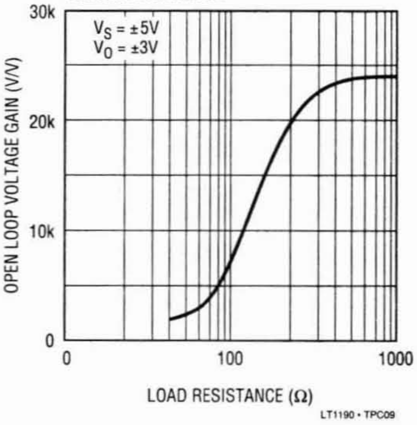
Shutdown Supply Current vs Temperature



Open Loop Voltage Gain vs Temperature

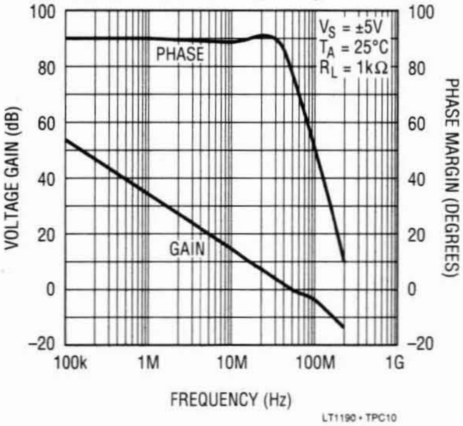


Open Loop Voltage Gain vs Load Resistance

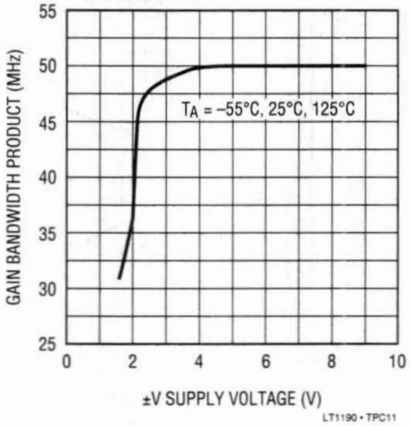


TYPICAL PERFORMANCE CHARACTERISTICS

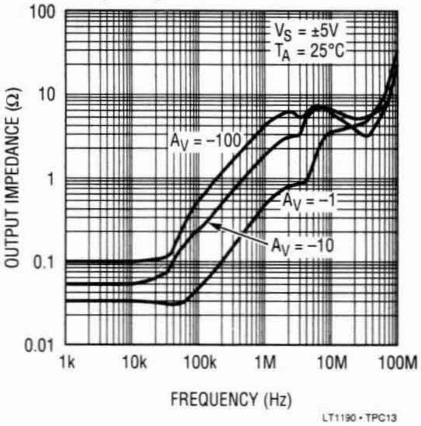
Gain, Phase vs Frequency



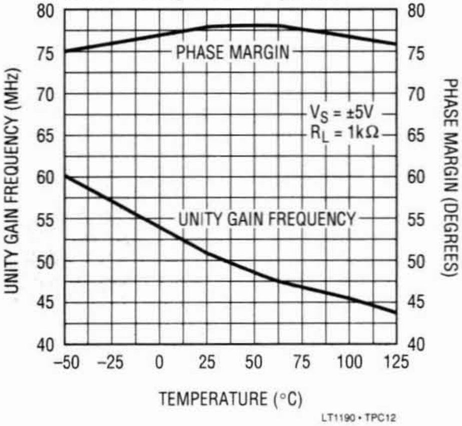
Gain Bandwidth Product vs Supply Voltage



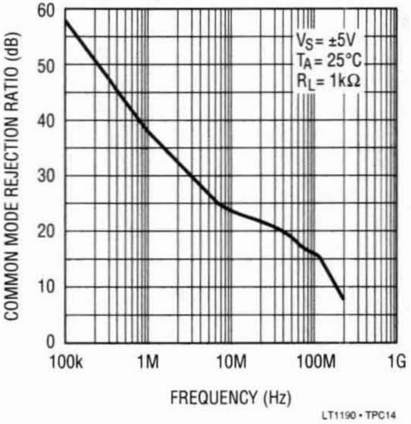
Output Impedance vs Frequency



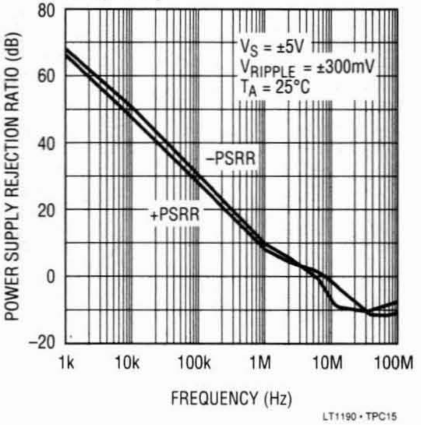
Unity Gain Frequency and Phase Margin vs Temperature



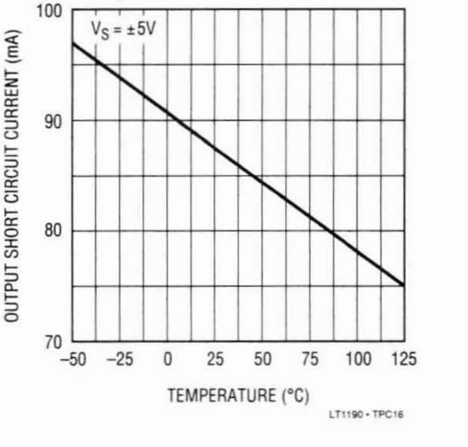
Common Mode Rejection Ratio vs Frequency



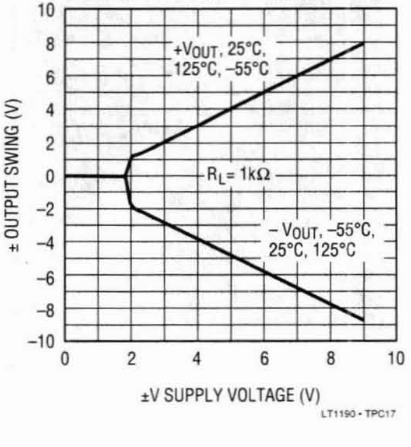
Power Supply Rejection Ratio vs Frequency



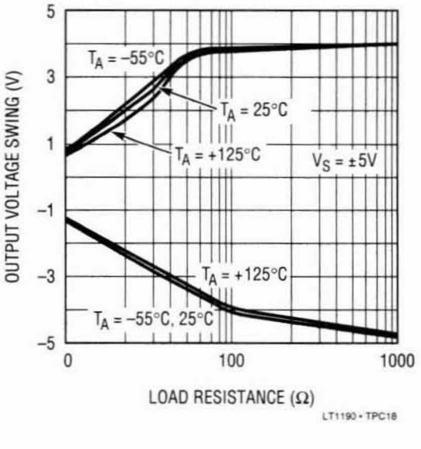
Output Short Circuit Current vs Temperature



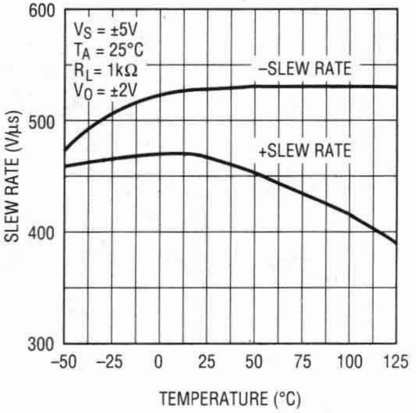
± Output Swing vs Supply Voltage



Output Voltage Swing vs Load Resistance

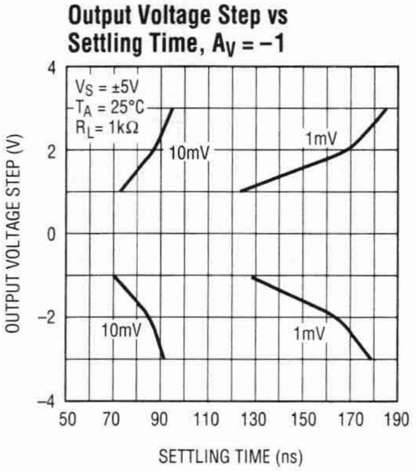


TYPICAL PERFORMANCE CHARACTERISTICS



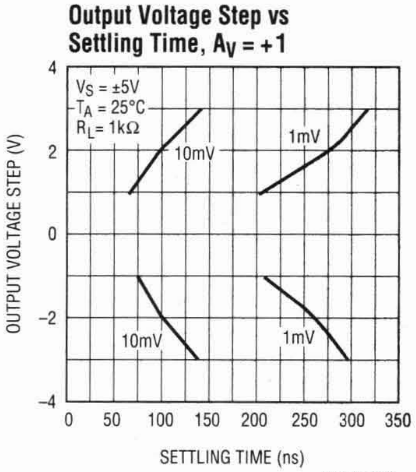
Slew Rate vs Temperature

LT1190 • TPC19



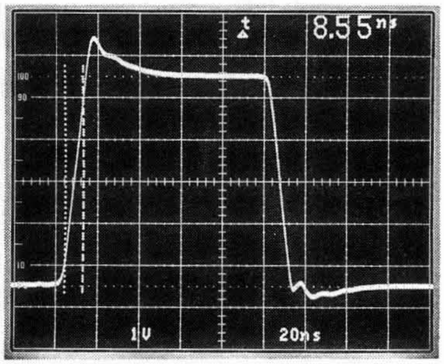
Output Voltage Step vs Settling Time, A_V = –1

LT1190 • TPC20



Output Voltage Step vs Settling Time, A_V = +1

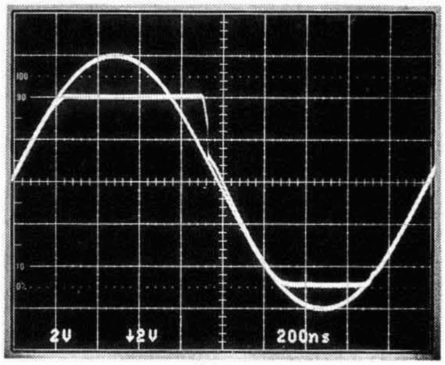
LT1190 • TPC21



Large Signal Transient Response

A_V = +1, C_L = 10pF SCOPE PROBE

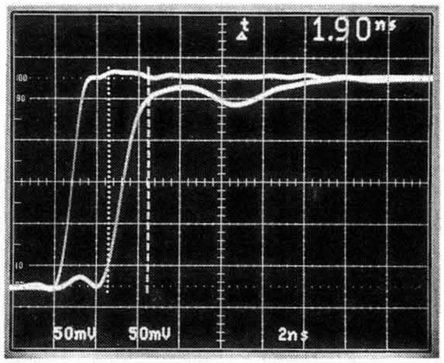
LT1190 • TPC22



Output Overload

A_V = –1, V_{IN} = 12Vp-p

LT1190 • TPC23



Small Signal Transient Response

A_V = +1, SMALL SIGNAL RISE TIME, WITH FET PROBES

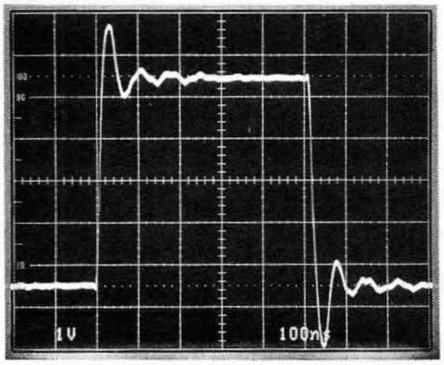
LT1190 • TPC24

APPLICATIONS INFORMATION

Power Supply Bypassing

The LT1190 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, $R_L = 1k\Omega$.

No Supply Bypass Capacitors

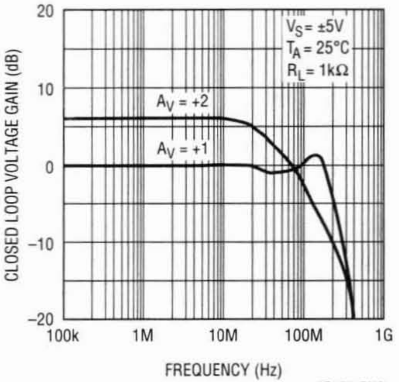


$A_V = -1$, IN DEMO BOARD, $R_L = 1k\Omega$

LT1190 • TA04

Supply bypassing can also affect the response in the frequency domain. It is possible to see a slight 1dB rise in the frequency response at 130MHz depending on the gain configuration, supply bypass, inductance in the supply leads, and printed circuit board layout. This can be further minimized by not using a socket.

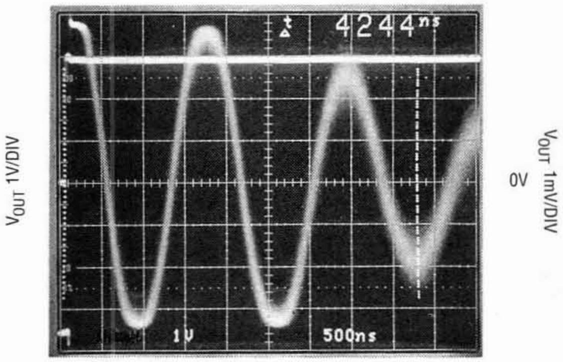
Closed Loop Voltage Gain vs Frequency



LT1190 • TA05

In most applications, and those requiring good settling time, it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/div, when amplified to 1mV/div the settling time to 2mV is 4.244µs for the 0.1µF bypass; the time drops to 163ns with multiple bypass capacitors.

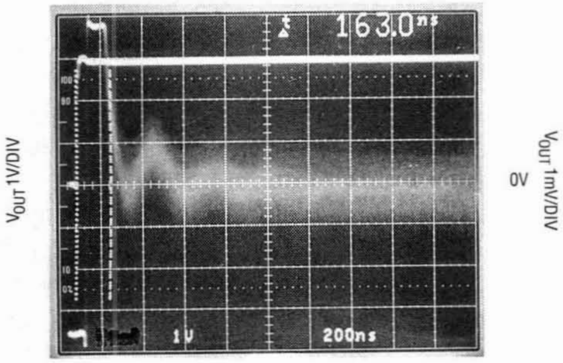
Settling Time Poor Bypass



SETTLING TIME TO 2mV, $A_V = -1$
SUPPLY BYPASS CAPACITORS = 0.1µF

LT1190 • TA06

Settling Time Good Bypass



SETTLING TIME TO 2mV, $A_V = -1$
SUPPLY BYPASS CAPACITORS = 0.1µF + 4.7µF TANTALUM

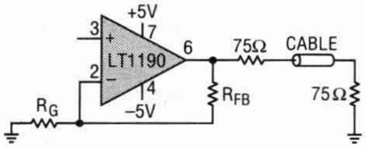
LT1190 • TA07

APPLICATIONS INFORMATION

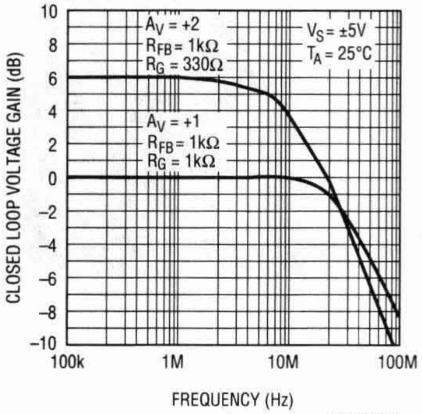
Cable Terminations

The LT1190 operational amplifier has been optimized as a low cost video cable driver. The ±50mA guaranteed output current enables the LT1190 to easily deliver 7.5Vp-p into 100Ω, while operating on ±5V supplies, or 2.6Vp-p on a single 5V supply.

Double Terminated Cable Driver



Cable Driver Voltage Gain vs Frequency



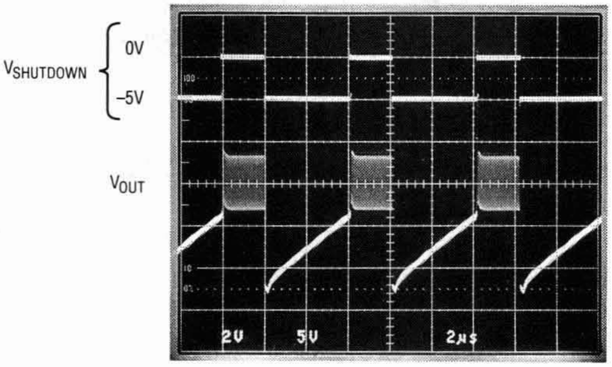
LT1190 • TA08

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. This can be compensated for by taking a gain of 2, or 6dB in the amplifier. The cable driver has a –3dB bandwidth in excess of 30MHz while driving the 150Ω load.

Using the Shutdown Feature

The LT1190 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 15kΩ in parallel with the feedback resistors. The amplifiers must be used in a non-inverting configuration for MUX applications. In inverting configurations the input signal is fed to the output through the feedback components. The following scope photos show that with very high R_L, the output is truly high impedance; the output slowly decays toward ground. Additionally, when the output is loaded with as little as 1kΩ the amplifier shuts off in 400ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

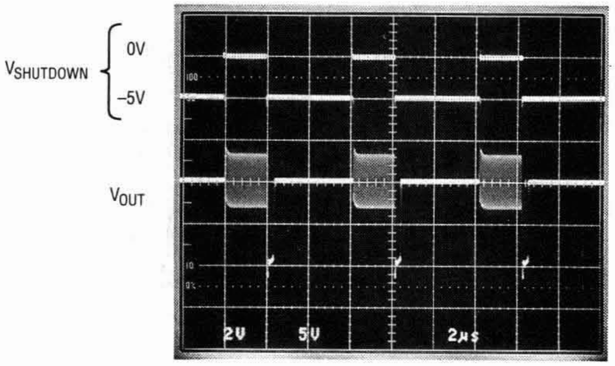
Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, $A_V = +1$, R_L = SCOPE PROBE

LT1190 • TA09

Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, $A_V = +1$, $R_L = 1k\Omega$

LT1190 • TA10

APPLICATIONS INFORMATION

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperatures it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

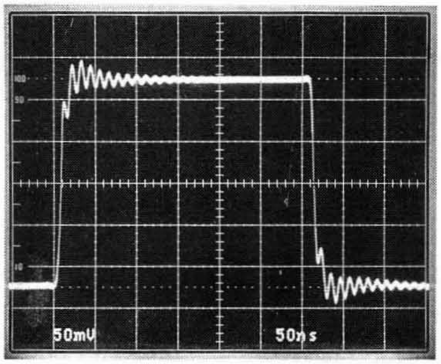
Murphy Circuits

There are several precautions the user should take when using the LT1190 in order to realize its full capability. Although the LT1190 can drive a 50pF load, isolating the capacitance with 10Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

Other precautions include:

1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).
2. Do not use high source impedances. The input capacitance of 2pF, and $R_S = 10k\Omega$ for instance, will give an 8MHz –3dB bandwidth.
3. PC board socket may reduce stability.
4. A feedback resistor of 1kΩ or lower reduces the effects of stray capacitance at the inverting input. (For instance, closed loop gain of +2 can use $R_{FB} = 300\Omega$ and $R_G = 300\Omega$.)

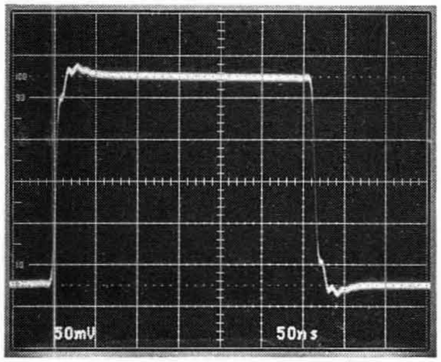
Driving Capacitive Load



$A_V = -1$, IN DEMO BOARD, $C_L = 50pF$

LT1190 • TA11

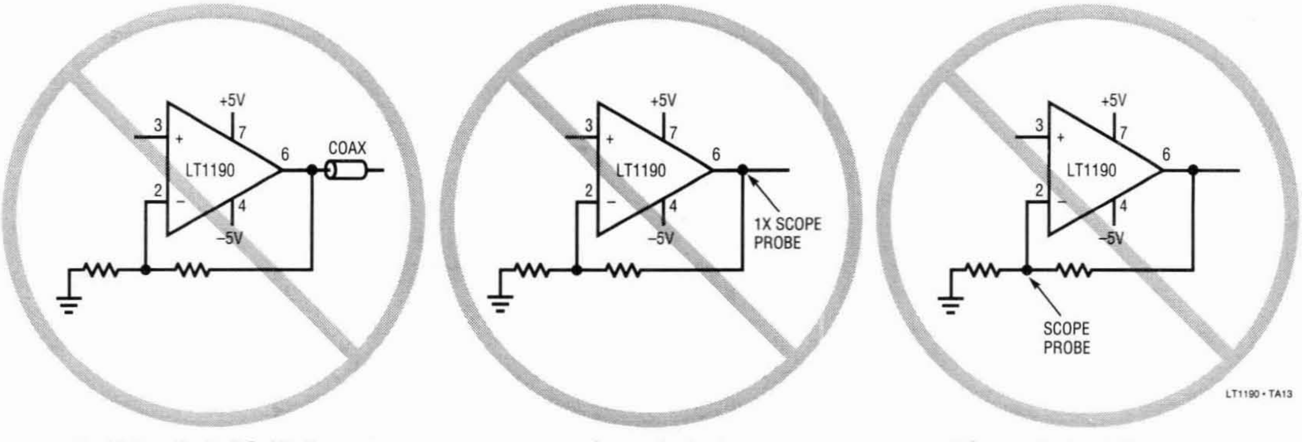
Driving Capacitive Load



$A_V = -1$, IN DEMO BOARD, $C_L = 50pF$ WITH 10Ω ISOLATING RESISTOR

LT1190 • TA12

Murphy Circuits



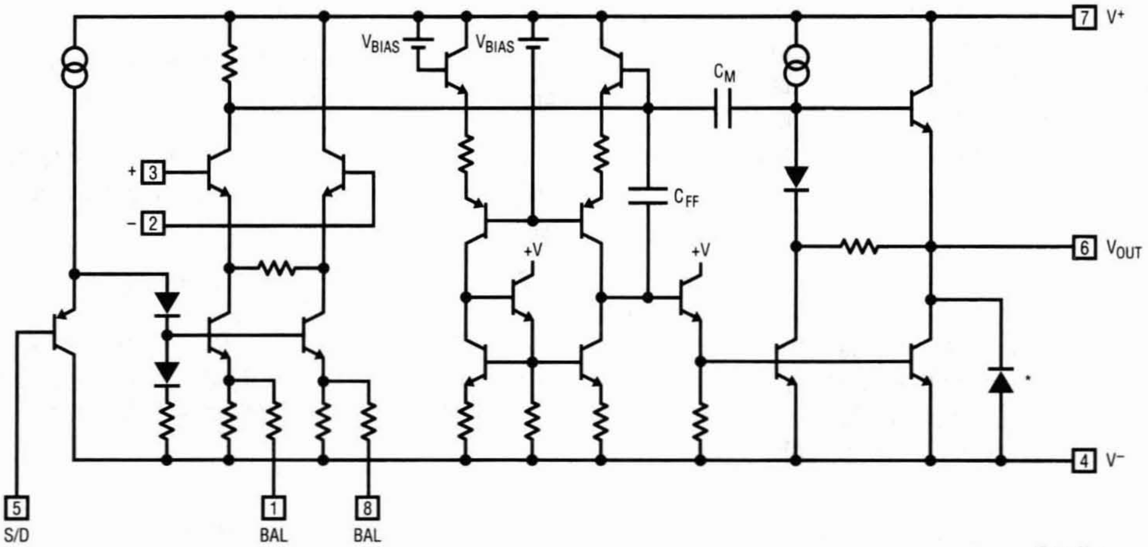
LT1190 • TA13

An Unterminated Cable Is a Large Capacitive Load

A 1X Scope Probe Is a Large Capacitive Load

A Scope Probe on the Inverting Input Reduces Phase Margin

SIMPLIFIED SCHEMATIC


7 V+
VBIAS
VBIAS
CM
+ 3
– 2
CFF
+V
+V
6 VOUT
4 V–
5 S/D
1 BAL
8 BAL
LT1190 • TA14

* SUBSTRATE DIODE, DO NOT FORWARD BIAS

Ultra High Speed Operational Amplifier

FEATURES

Gain Bandwidth Product, $A_V = +1$	90MHz
Slew Rate	450V/µs
Low Cost	
Output Current	±50mA
Settling Time	110ns to 0.1%
Differential Gain Error	0.07%, ($R_L = 1k$)
Differential Phase Error	0.02°, ($R_L = 1k$)
High Open Loop Gain	25V/mV Min
Single Supply +5V Operation	
Output Shutdown	

APPLICATIONS

- Video Cable Drivers
- Video Signal Processing
- Fast Integrators
- Pulse Amplifiers
- D/A Current to Voltage Conversion

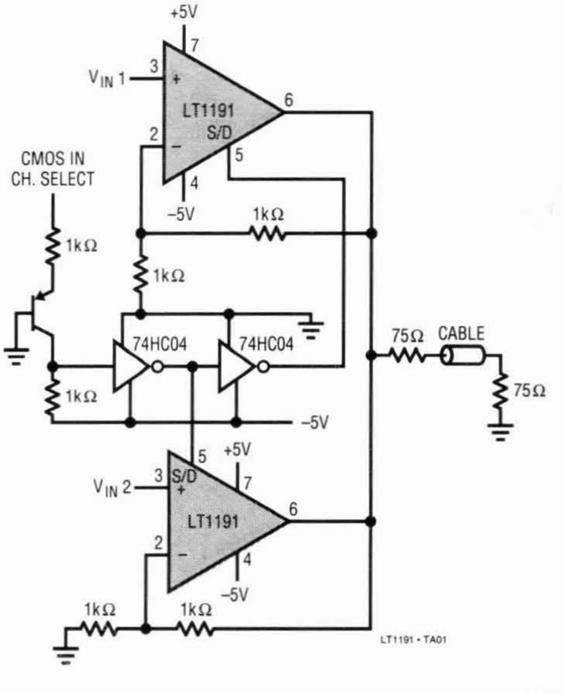
DESCRIPTION

The LT1191 is a video operational amplifier optimized for operation on ±5V, and a single +5V supply. Unlike many high speed amplifiers, this amplifier features high open loop gain, over 90dB, and the ability to drive heavy loads to a full power bandwidth of 20MHz at 7Vp-p. In addition to its very fast slew rate, the LT1191 features a unity gain stable bandwidth of 90MHz.

Because the LT1191 is a true operational amplifier, it is an ideal choice for wideband signal conditioning, fast integrators, active filters, and applications requiring speed, accuracy, and low cost.

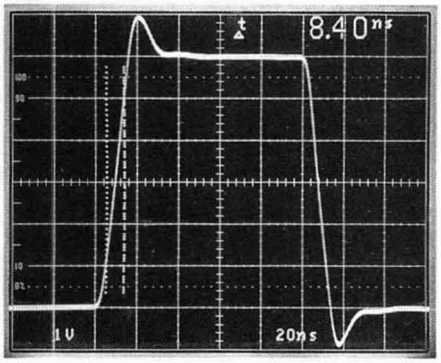
The LT1191 is available in 8-pin miniDIPs and SO packages with standard pinouts. The normally unused pin 5 is used for a shutdown feature that shuts off the output and reduces power dissipation to a mere 15mW.

Video MUX Cable Driver



LT1191 • TA01

Inverter Pulse Response



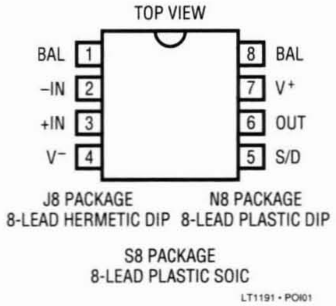
$A_V = -1$, $C_L = 10pF$ SCOPE PROBE

LT1191 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage .... ± 6V
Input Voltage .... ± V_S
Output Short Circuit Duration (Note 1) .... Continuous
Operating Junction Temperature Range
LT1191M .... −55°C to 150°C
LT1191C .... 0°C to 150°C
Max. Junction Temperature .... See Pkg. Descriptions
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1191MJ8 LT1191CJ8 LT1191CN8 LT1191CS8
S8 PART MARKING
1191

ELECTRICAL CHARACTERISTICS

$V_S = \pm5V$, $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER		CONDITIONS	LT1191M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage				1.0	5.0	mV
I_{OS}	Input Offset Current				0.2	1.7	μA
I_B	Input Bias Current				±0.5	±2.5	μA
e_n	Input Noise Voltage		$f_0 = 10kHz$		25		nV/√Hz
i_n	Input Noise Current		$f_0 = 10kHz$		4.0		pA/√Hz
R_{IN}	Input Resistance	Differential Mode			70		kΩ
		Common Mode			5.0		MΩ
C_{IN}	Input Capacitance		$A_V = +1$		2.0		pF
	Input Voltage Range		(Note 2)	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio		$V_{CM} = -2.5V$ to $+3.5V$	60	75		dB
PSRR	Power Supply Rejection Ratio		$V_S = \pm2.375V$ to $\pm8.0V$	60	75		dB
A_{VOL}	Large Signal Voltage Gain		$R_L = 1k$, $V_O = \pm3.0V$	20	45		V/mV
			$R_L = 100\Omega$, $V_O = \pm3.0V$	6.0	12		
			$V_S = \pm8V$, $R_L = 100\Omega$, $V_O = \pm5V$	9.0	17		
V_{OUT}	Output Voltage Swing		$V_S = \pm5V$, $R_L = 1k$	±3.7	±4.0		V
			$V_S = \pm8V$, $R_L = 1k$	±6.7	±7.0		
SR	Slew Rate		$A_V = -2$, $R_L = 1k$, (Note 3, 8)	325	450		V/μs
FPBW	Full Power Bandwidth		$V_O = 6Vp$-p, (Note 4)	17.2	23.9		MHz
GBW	Gain Bandwidth Product				90		MHz
t_{r1}, t_{f1}	Rise Time, Fall Time		$A_V = +50$, $V_O = \pm1.5V$, 20% to 80%, (Note 8)	100	130	160	ns
t_{r2}, t_{f2}	Rise Time, Fall Time		$A_V = +1$, $V_O = \pm125mV$, 10% to 90%		1.25		ns
t_{PD}	Propagation Delay		$A_V = +1$, $V_O = \pm125mV$, 50% to 50%		2.2		ns
	Overshoot		$A_V = +1$, $V_O = \pm125mV$		25		%
t_s	Settling Time		3V Step, 0.1%, (Note 5)		110		ns
Diff A_V	Differential Gain		$R_L = 150\Omega$, $A_V = +2$, (Note 6)		0.15		%
Diff Ph	Differential Phase		$R_L = 150\Omega$, $A_V = +2$, (Note 6)		0.09		Deg. p-p

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1191M/C MIN	 TYP	 MAX	UNITS
I_S	Supply Current			32	38	mA
	Shutdown Supply Current	Pin 5 at V^-		1.3	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		20	50	µA
t_{on}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		100		ns
t_{off}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		400		ns

ELECTRICAL CHARACTERISTICS

$V_S+ = +5V$, $V_S- = 0V$, $V_{CM} = +2.5V$, $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1191M/C MIN	 TYP	 MAX	UNITS
V_{OS}	Input Offset Voltage				2.0	7.0	mV
I_{OS}	Input Offset Current				0.2	1.2	µA
I_B	Input Bias Current				±0.5	±1.5	µA
	Input Voltage Range	(Note 2)		+2.0		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = +2.0V$ to $+3.5V$		55	70		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 100\Omega$ to Ground, $V_O = +1.0V$ to $+3.0V$		6.0	9.0		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$ to Ground	V_{OUT} High	3.6	3.8		V
			V_{OUT} Low		0.25	0.4	
SR	Slew Rate	$A_V = -1$, $V_O = +1V$ to $+3V$			250		V/µs
GBW	Gain Bandwidth Product				80		MHz
I_S	Supply Current				29	36	mA
	Shutdown Supply Current	Pin 5 at V^-			1.2	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			20	50	µA

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $-55°C \le T_A \le 125°C$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1191M MIN	 TYP	 MAX	UNITS
V_{OS}	Input Offset Voltage		●		2.0	8.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		8.0		µV/°C
I_{OS}	Input Offset Current		●		0.2	2.0	µA
I_B	Input Bias Current		●		±0.5	±2.5	µA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	55	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 5.0V$	●	55	70		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 1k$, $V_O = \pm 3.0V$	●	16	32		V/mV
		$R_L = 100$, $V_O = \pm 3.0V$	●	2.0	5.0		
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	±3.7	±3.9		V
I_S	Supply Current		●		32	38	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 7)	●		1.5	2.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		µA

ELECTRICAL CHARACTERISTICS $V_S = \pm5V$, $0°C \le T_A \le 70°C$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1191C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		2.0	6.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		8.0		μV/°C
I_{OS}	Input Offset Current		●		0.2	1.7	μA
I_B	Input Bias Current		●		±0.5	±2.5	μA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	58	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm5.0V$	●	58	70		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 1k$, $V_O = \pm3.0V$	●	20	40		V/mV
		$R_L = 100$, $V_O = \pm3.0V$	●	5.0	9.0		
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	±3.7	±3.9		V
I_S	Supply Current		●		32	38	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 7)	●		1.4	2.1	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: Exceeding the input common mode range may cause the output to invert.

Note 3: Slew rate is measured between ±1V on the output, with a ±1.5V input step.

Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

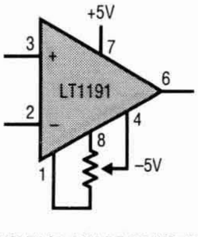
Note 5: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985. $A_V = -1$, $R_L = 1k$.

Note 6: NTSC (3.58MHz). For $R_L = 1k$, Diff $A_V = 0.07\%$, Diff Ph = 0.02°.

Note 7: See Applications section for shutdown at elevated temperatures. Do not operate the shutdown above $T_J > 125°C$.

Note 8: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

Optional Offset Nulling Circuit

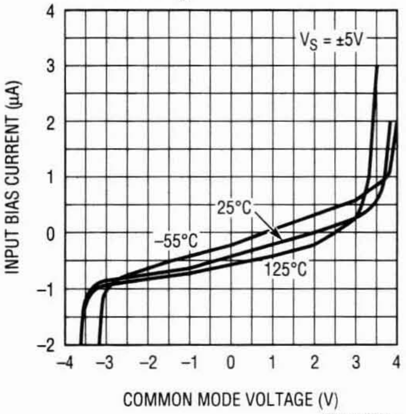


INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±100mV RANGE WITH A 1kΩ TO 10kΩ POTENTIOMETER.

LT1191 • TA03

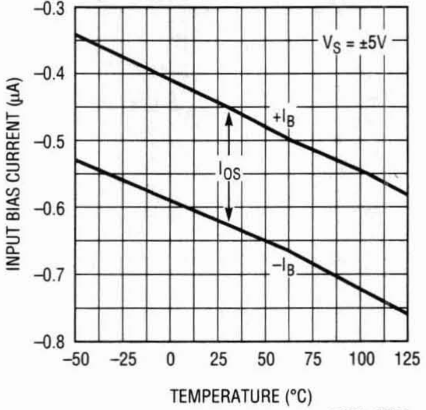
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Common Mode Voltage



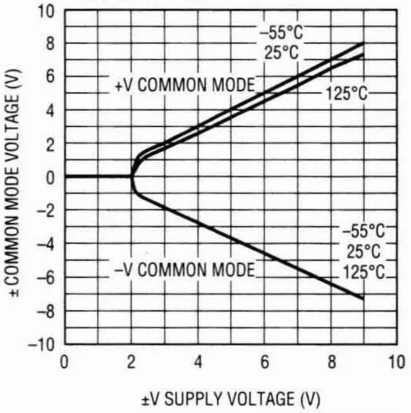
LT1191 • TPC01

Input Bias Current vs Temperature



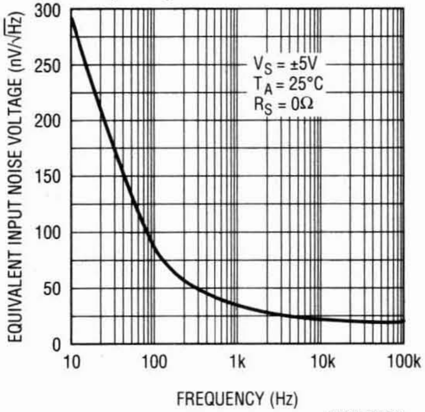
LT1191 • TPC02

Common Mode Voltage vs Supply Voltage



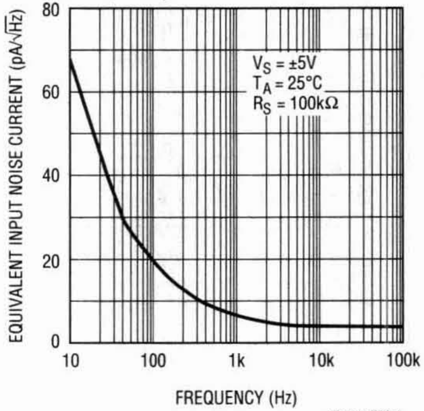
LT1191 • TPC03

Equivalent Input Noise Voltage vs Frequency



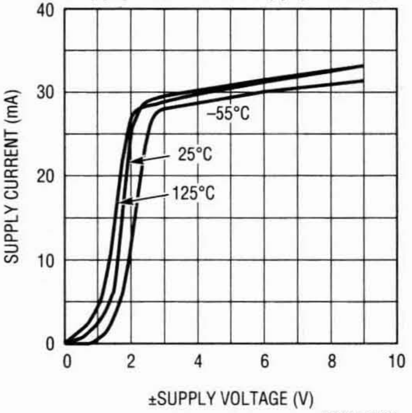
LT1191 • TPC04

Equivalent Input Noise Current vs Frequency



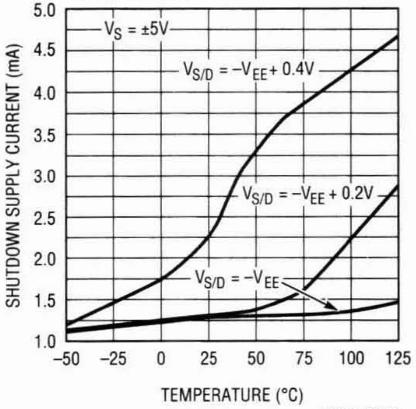
LT1191 • TPC05

Supply Current vs Supply Voltage



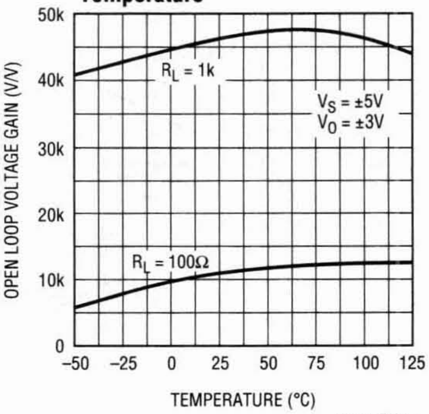
LT1191 • TPC06

Shutdown Supply Current vs Temperature



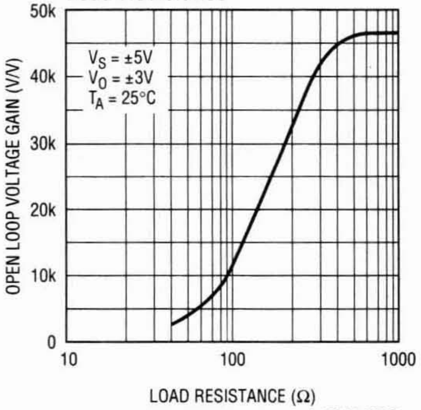
LT1191 • TPC07

Open Loop Voltage Gain vs Temperature



LT1191 • TPC08

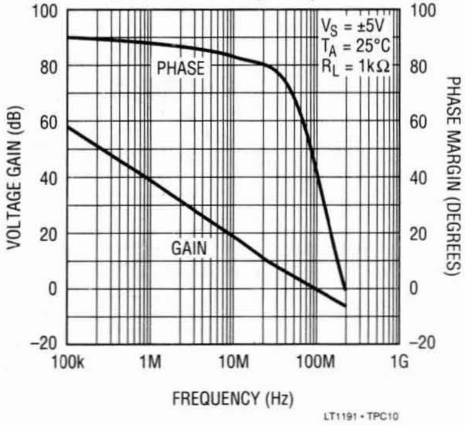
Open Loop Voltage Gain vs Load Resistance



LT1191 • TPC09

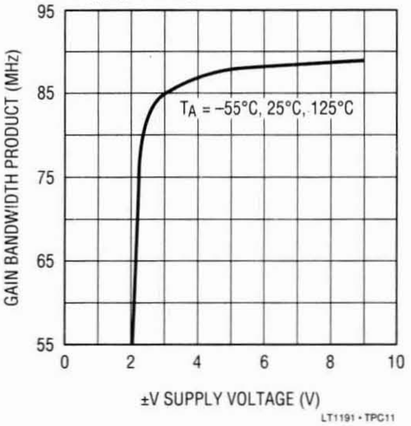
TYPICAL PERFORMANCE CHARACTERISTICS

Gain, Phase vs Frequency



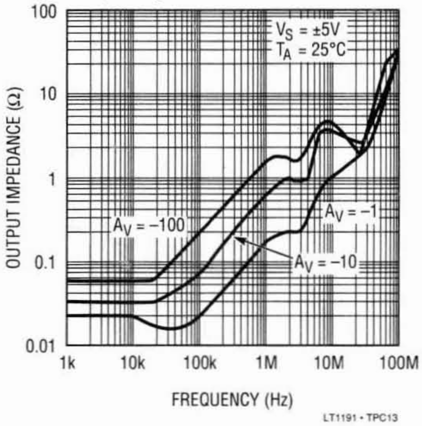
LT1191 • TPC10

Gain Bandwidth Product vs Supply Voltage



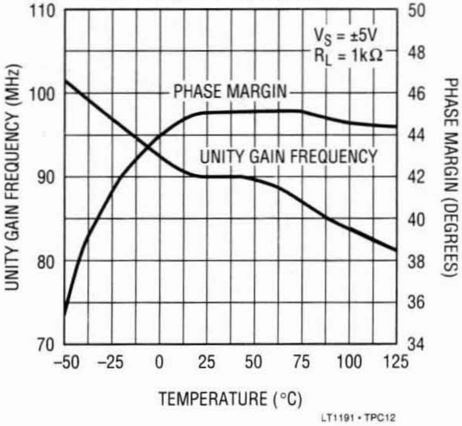
LT1191 • TPC11

Output Impedance vs Frequency



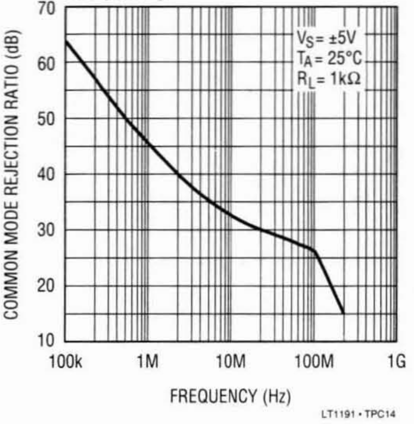
LT1191 • TPC13

Unity Gain Frequency and Phase Margin vs Temperature



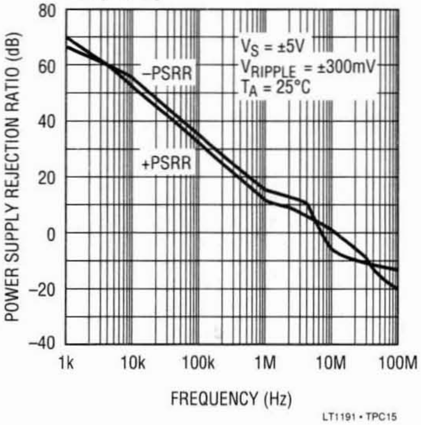
LT1191 • TPC12

Common Mode Rejection Ratio vs Frequency



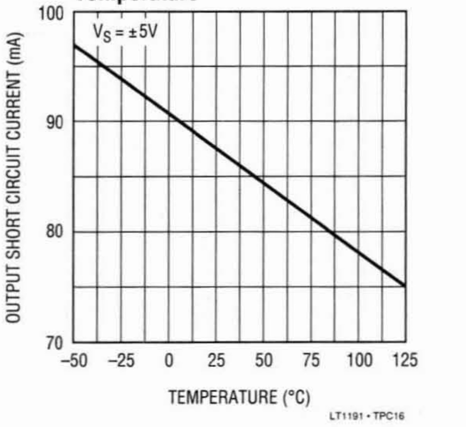
LT1191 • TPC14

Power Supply Rejection Ratio vs Frequency



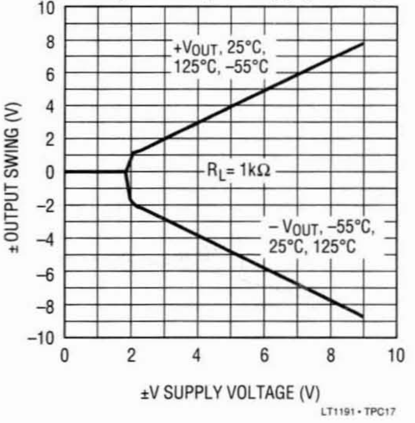
LT1191 • TPC15

Output Short Circuit Current vs Temperature



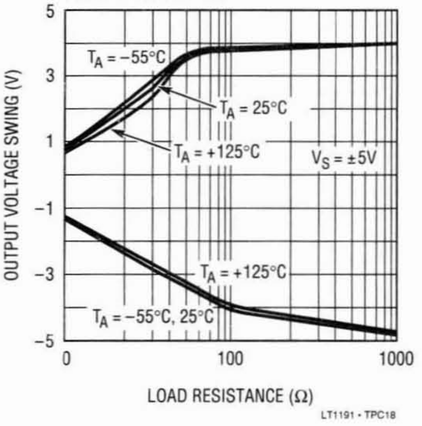
LT1191 • TPC16

± Output Swing vs Supply Voltage



LT1191 • TPC17

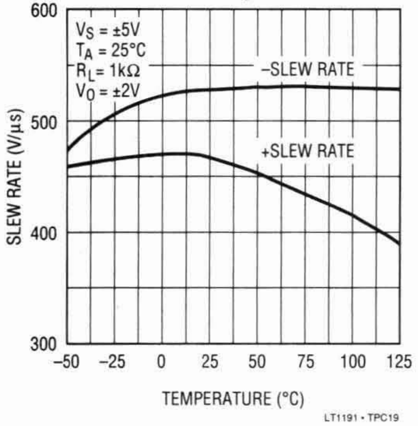
Output Voltage Swing vs Load Resistance



LT1191 • TPC18

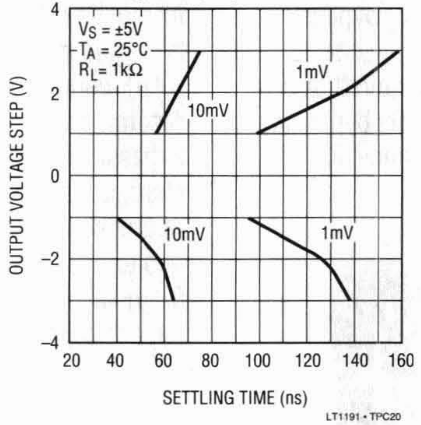
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Temperature



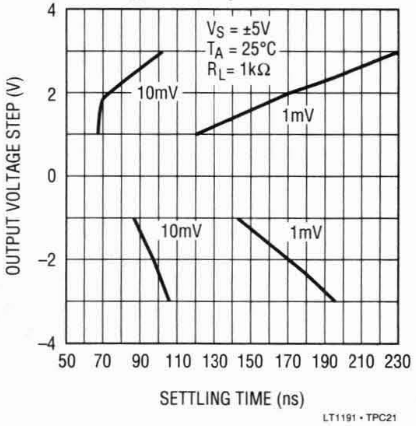
LT1191 • TPC19

Output Voltage Step vs Settling Time, $A_V = -1$



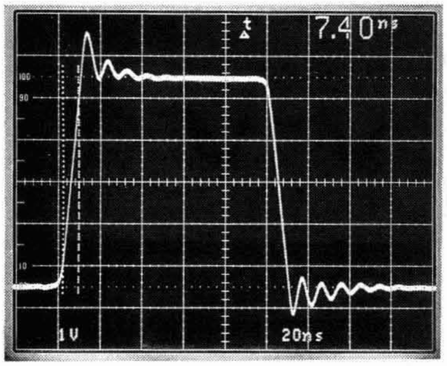
LT1191 • TPC20

Output Voltage Step vs Settling Time, $A_V = +1$



LT1191 • TPC21

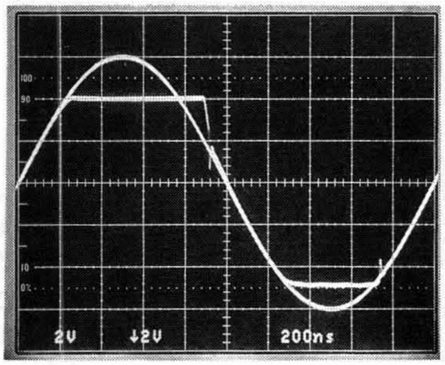
Large Signal Transient Response



A_V = +1, C_L = 10pF SCOPE PROBE

LT1191 • TPC22

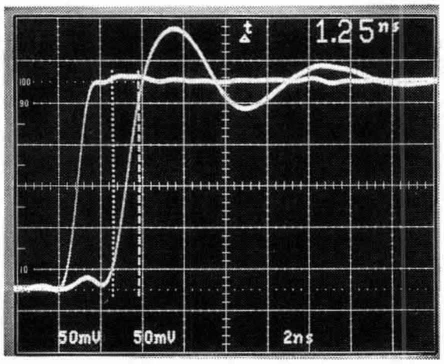
Output Overload



A_V = –1, V_{IN} = 12Vp-p

LT1191 • TPC23

Small Signal Transient Response



A_V = +1, SMALL SIGNAL RISE TIME, WITH FET PROBES

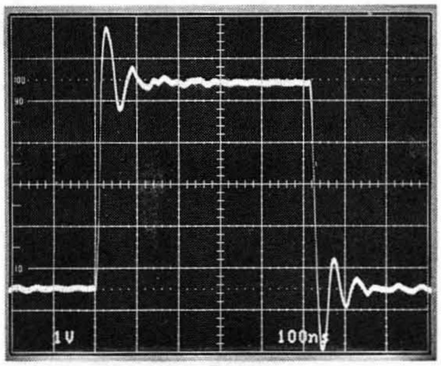
LT1191 • TPC24

APPLICATIONS INFORMATION

Power Supply Bypassing

The LT1191 is quite tolerant of power supply bypassing. In some applications a 0.1μF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, $R_L = 1k\Omega$.

No Supply Bypass Capacitors

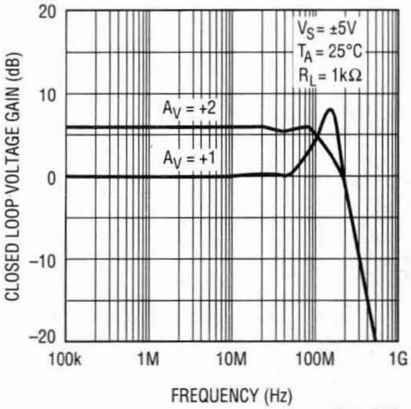


$A_V = -1$, IN DEMO BOARD, $R_L = 1k\Omega$

LT1191 • TA04

Supply bypassing can also affect the response in the frequency domain. It is possible to see a slight rise in the frequency response at 130MHz depending on the gain configuration, supply bypass, inductance in the supply leads, and printed circuit board layout. This can be further minimized by not using a socket.

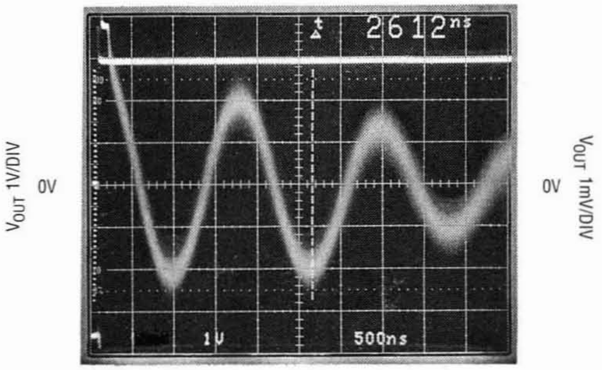
Closed Loop Voltage Gain vs Frequency



LT1191 • TA05

In most applications, and those requiring good settling time, it is important to use multiple bypass capacitors. A 0.1μF ceramic disc in parallel with a 4.7μF tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/div, when amplified to 1mV/div the settling time to 2mV is 2.61μs for the 0.1μF bypass; the time drops to 143ns with multiple bypass capacitors.

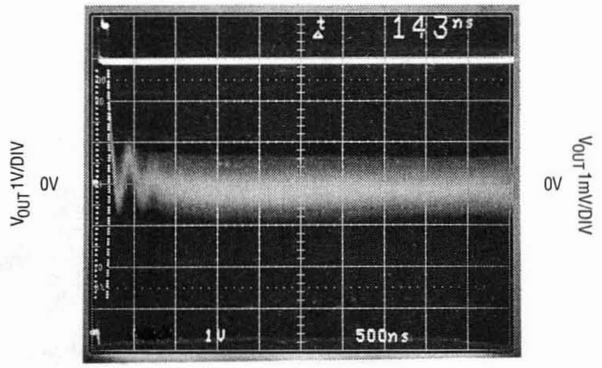
Settling Time Poor Bypass



SETTLING TIME TO 2mV, $A_V = -1$
SUPPLY BYPASS CAPACITORS = 0.1μF

LT1191 • TA06

Settling Time Good Bypass



SETTLING TIME TO 2mV, $A_V = -1$
SUPPLY BYPASS CAPACITORS = 0.1μF + 4.7μF TANTALUM

LT1191 • TA07

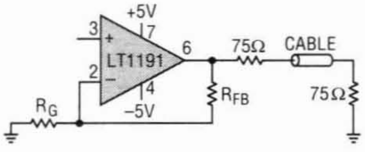
APPLICATIONS INFORMATION

Cable Terminations

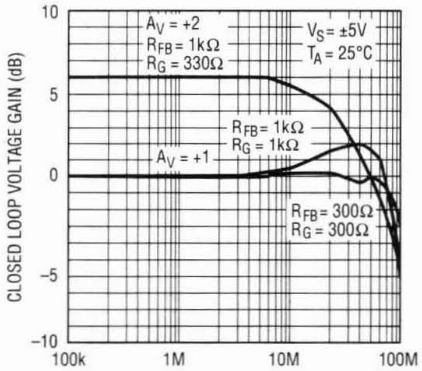
The LT1191 operational amplifier has been optimized as a low cost video cable driver. The ±50mA guaranteed output current enables the LT1191 to easily deliver 7.5Vp-p into 100Ω, while operating on ±5V supplies, or 2.6Vp-p on a single 5V supply.

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. This can be compensated for by taking a gain of 2, or 6dB in the amplifier. The cable driver has a –3dB bandwidth of 100MHz while driving the 150Ω load. Note the response can be improved by lowering the impedance of the feedback elements.

Double Terminated Cable Driver



Cable Driver Voltage Gain vs Frequency

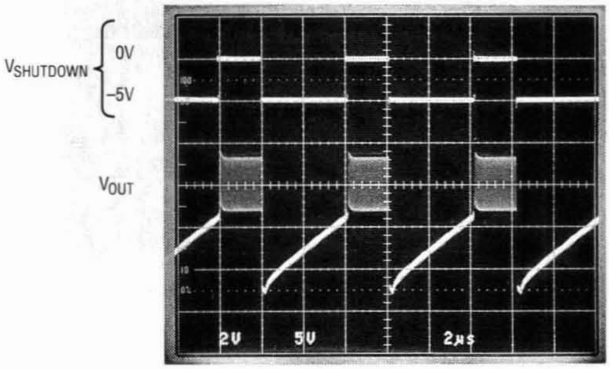


LT1191 • TA08

Using the Shutdown Feature

The LT1191 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V⁻. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 15kΩ in parallel with the feedback resistors. The amplifiers must be used in a non-inverting configuration for MUX applications. In inverting configurations the input signal is fed to the output through the feedback components. The following scope photos show that with very high R_L, the output is truly high impedance; the output slowly decays toward ground. Additionally, when the output is loaded with as little as 1kΩ the amplifier shuts off in 400ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

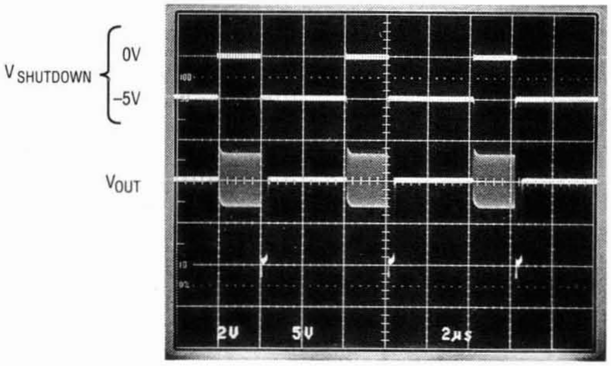
Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, $A_V = +1$, $R_L = \infty$

LT1191 • TA09

Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, $A_V = +1$, $R_L = 1k\Omega$

LT1191 • TA10

APPLICATIONS INFORMATION

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperatures it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

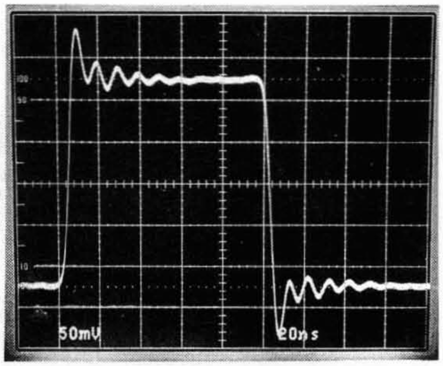
Murphy Circuits

There are several precautions the user should take when using the LT1191 in order to realize its full capability. Although the LT1191 can drive a 30pF load, isolating the capacitance with 10Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

Other precautions include:

1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).
2. Do not use high source impedances. The input capacitance of 2pF, and $R_S = 10k\Omega$ for instance, will give an 8MHz −3dB bandwidth.
3. PC board socket may reduce stability.
4. A feedback resistor of 1kΩ or lower reduces the effects of stray capacitance at the inverting input. (For instance, closed loop gain of +2 can use $R_{FB} = 300\Omega$ and $R_G = 300\Omega$.)

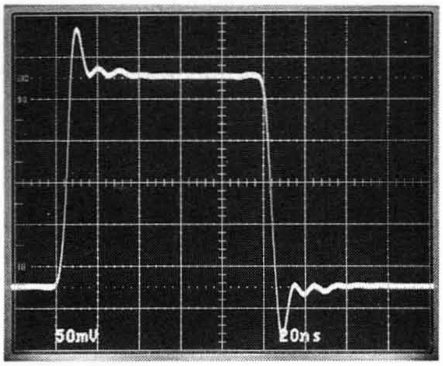
Driving Capacitive Load



$A_V = -1$, IN DEMO BOARD, $C_L = 30pF$

LT1191 • TA11

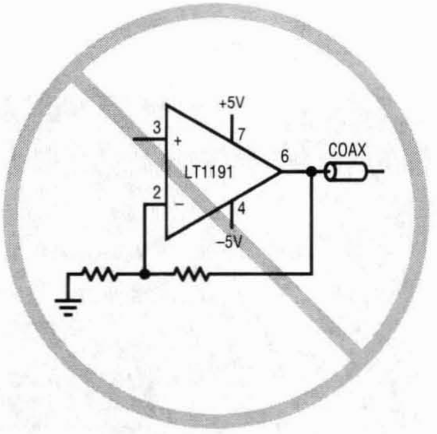
Driving Capacitive Load



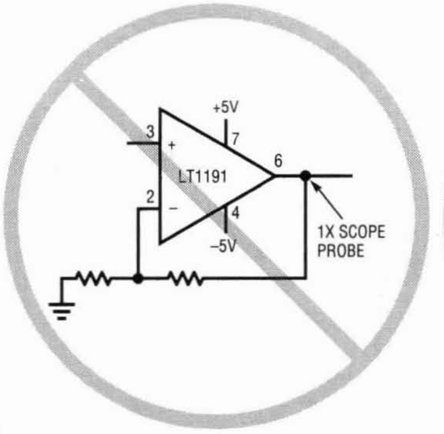
$A_V = -1$, IN DEMO BOARD, $C_L = 30pF$ WITH 10Ω ISOLATING RESISTOR

LT1191 • TA12

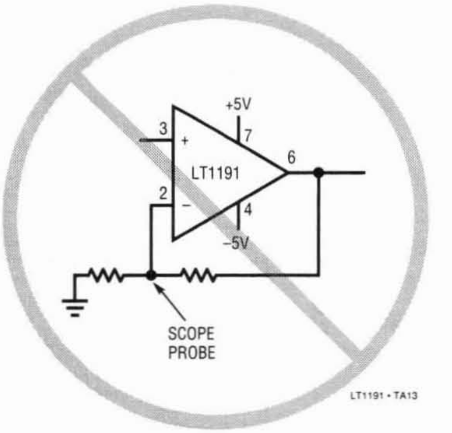
Murphy Circuits



An Unterminated Cable Is a Large Capacitive Load



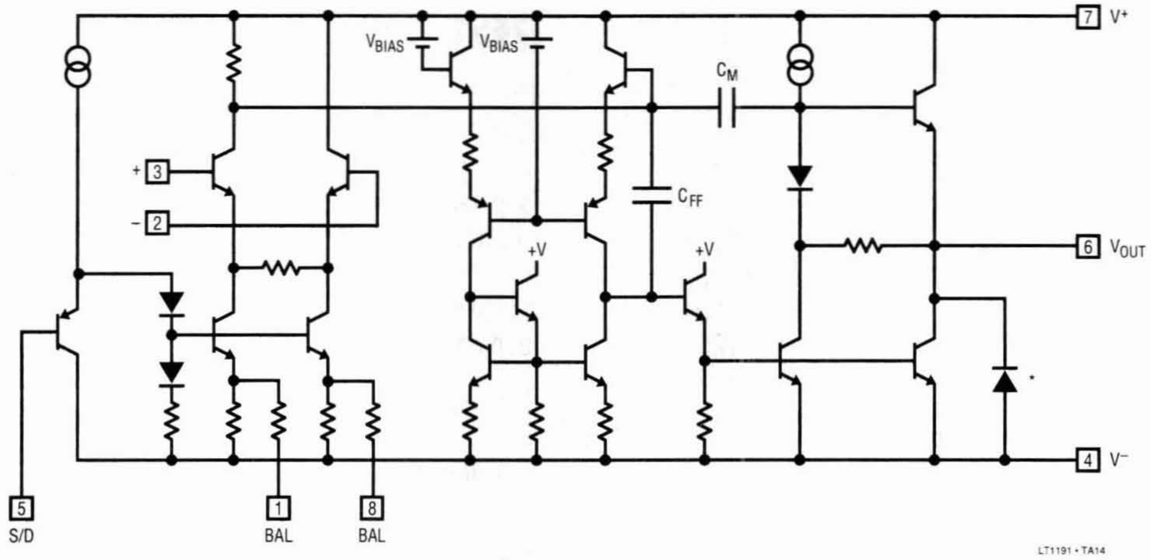
A 1X Scope Probe Is a Large Capacitive Load



LT1191 • TA13

A Scope Probe on the Inverting Input Reduces Phase Margin

SIMPLIFIED SCHEMATIC


7 V+
VBIAS
VBIAS
CM
+ 3
− 2
CFF
+V
+V
6 VOUT
*
4 V−
5 S/D
1 BAL
8 BAL
LT1191 • TA14

* SUBSTRATE DIODE, DO NOT FORWARD BIAS

LT1192

Ultra High Speed Operational Amplifier

FEATURES

■ Gain Bandwidth Product, $A_V = +5$	350MHz
■ Slew Rate	450V/μs
■ Low Cost	
■ Output Current	± 50mA
■ Settling Time	90ns to 0.1%
■ Differential Gain Error	0.1% ($R_L = 1k\Omega$)
■ Differential Phase Error	0.01° ($R_L = 1k\Omega$)
■ High Open Loop Gain	125V/mV Min
■ Single Supply +5V Operation	
■ Output Shutdown	

APPLICATIONS

- Video Cable Drivers
- Video Signal Processing
- Photo-Diode Amplifier
- Pulse Amplifiers
- D/A Current to Voltage Conversion

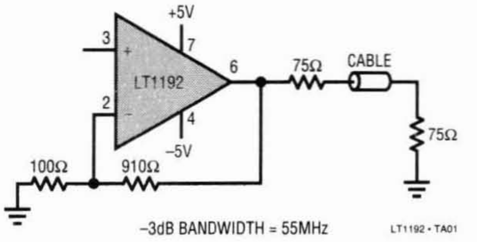
DESCRIPTION

The LT1192 is a video operational amplifier optimized for operation on ± 5V, and a single +5V supply. Unlike many high speed amplifiers, this amplifier features high open loop gain, over 100dB, and the ability to drive heavy loads to a full power bandwidth of 20MHz at 7Vp-p. In addition to its very fast slew rate, the LT1192 has a high gain bandwidth of 350MHz, and is compensated for a closed loop gain of 5 or greater.

Because the LT1192 is a true operational amplifier, it is an ideal choice for wideband signal conditioning, active filters, and applications requiring speed, accuracy, and low cost.

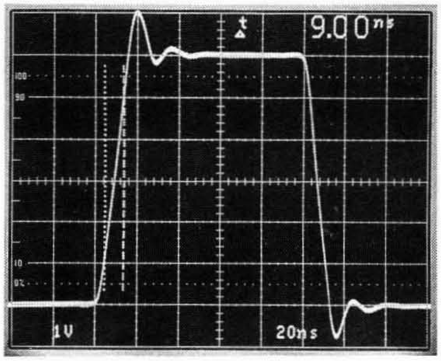
The LT1192 is available in 8-pin miniDIPs and SO packages with standard pinouts. The normally unused pin 5 is used for a shutdown feature that shuts off the output and reduces power dissipation to a mere 15mW.

Double Terminated Cable Driver



−3dB BANDWIDTH = 55MHz

Inverter Pulse Response



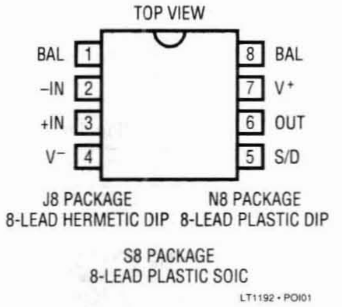
$A_V = -5$, $C_L = 10pF$ SCOPE PROBE

LT1192 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage .... ± 6V
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Continuous
Operating Junction Temperature Range
LT1192M .... −55°C to 150°C
LT1192C .... 0°C to 150°C
Max. Junction Temperature .... See Pkg. Descriptions
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1192MJ8 LT1192CJ8 LT1192CN8 LT1192CS8
S8 PART MARKING
1192

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER		CONDITIONS	LT1192M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage				0.2	2.5	mV
I_{OS}	Input Offset Current				0.2	1.7	μA
I_B	Input Bias Current				±0.5	±2.5	μA
e_n	Input Noise Voltage		$f_O = 10kHz$		9.0		nV/√Hz
i_n	Input Noise Current		$f_O = 10kHz$		4.0		pA/√Hz
R_{IN}	Input Resistance	Differential Mode			16		kΩ
		Common Mode			5.0		MΩ
C_{IN}	Input Capacitance		$A_V = +10$		1.8		pF
	Input Voltage Range		(Note 2)	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio		$V_{CM} = -2.5V$ to $+3.5V$	70	85		dB
PSRR	Power Supply Rejection Ratio		$V_S = \pm 2.375V$ to $\pm 8.0V$	70	85		dB
A_{VOL}	Large Signal Voltage Gain		$R_L = 1k$, $V_O = \pm 3.0V$	100	180		V/mV
			$R_L = 100\Omega$, $V_O = \pm 3.0V$	16	35		
			$V_S = \pm 8V$, $R_L = 100\Omega$, $V_O = \pm 5V$	20	60		
V_{OUT}	Output Voltage Swing		$V_S = \pm 5V$, $R_L = 1k$	±3.7	±4.0		V
			$V_S = \pm 8V$, $R_L = 1k$	±6.7	±7.0		
SR	Slew Rate		$A_V = -10$, $R_L = 1k$, (Note 3, 8)	325	450		V/μs
FPBW	Full Power Bandwidth		$V_O = 6Vp\text{-}p$, (Note 4)	17.2	23.9		MHz
GBW	Gain Bandwidth Product				350		MHz
t_{r1}, t_{f1}	Rise Time, Fall Time		$A_V = +50$, $V_O = \pm 1.5V$, 20% to 80%, (Note 8)	23	35	50	ns
t_{r2}, t_{f2}	Rise Time, Fall Time		$A_V = +5$, $V_O = \pm 125mV$, 10% to 90%		2.7		ns
t_{PD}	Propagation Delay		$A_V = +5$, $V_O = \pm 125mV$, 50% to 50%		3.5		ns
	Overshoot		$A_V = +5$, $V_O = \pm 125mV$		50		%
t_s	Settling Time		3V Step, 0.1%, (Note 5)		90		ns
Diff A_V	Differential Gain		$R_L = 150\Omega$, $A_V = +10$, (Note 6)		0.23		%
Diff Ph	Differential Phase		$R_L = 150\Omega$, $A_V = +10$, (Note 6)		0.15		Deg. p-p

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1192M/C MIN	 TYP	 MAX	UNITS
I_S	Supply Current			32	38	mA
	Shutdown Supply Current	Pin 5 at V^-		1.3	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		20	50	μA
t_{on}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		100		ns
t_{off}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		400		ns

ELECTRICAL CHARACTERISTICS

$V_S+ = +5V$, $V_S- = 0V$, $V_{CM} = +2.5V$, $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1192M/C MIN	 TYP	 MAX	UNITS
V_{OS}	Input Offset Voltage				0.4	4.0	mV
I_{OS}	Input Offset Current				0.2	1.2	μA
I_B	Input Bias Current				±0.5	±1.5	μA
	Input Voltage Range	(Note 2)		+2.0		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = +2.0V$ to $+3.5V$		60	80		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 100\Omega$ to Ground, $V_O = +1.0V$ to $+3.0V$		30	50		V/mV
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$ to Ground	V_{OUT} High	3.6	3.8		V
			V_{OUT} Low		0.25	0.4	
SR	Slew Rate	$A_V = -5$, $V_O = +1V$ to $+3V$			250		V/μs
GBW	Gain Bandwidth Product				350		MHz
I_S	Supply Current				29	36	mA
	Shutdown Supply Current	Pin 5 at V^-			1.2	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			20	50	μA

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $-55°C \le T_A \le 125°C$, pin 5 open circuit unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1192M MIN	 TYP	 MAX	UNITS
V_{OS}	Input Offset Voltage		●		0.4	3.5	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		2.0		μV/°C
I_{OS}	Input Offset Current		●		0.2	2.0	μA
I_B	Input Bias Current		●		±0.5	±2.5	μA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	65	85		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 5.0V$	●	70	90		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 1k$, $V_O = \pm 3.0V$	●	55	90		V/mV
		$R_L = 100\Omega$, $V_O = \pm 3.0V$	●	5.0	14		
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	±3.7	±3.9		V
I_S	Supply Current		●		32	38	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 7)	●		1.5	2.5	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		μA

ELECTRICAL CHARACTERISTICS $V_S = \pm5V$, $0°C \le T_A \le 70°C$, pin 5 open circuit unless otherwise noted.

				LT1192C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage		●		0.4	3.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		2.0		µV/°C
I_{OS}	Input Offset Current		●		0.2	1.7	µA
I_B	Input Bias Current		●		±0.5	±2.5	µA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	68	85		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm5.0V$	●	70	90		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 1k$, $V_O = \pm3.0V$	●	90	140		V/mV
		$R_L = 100\Omega$, $V_O = \pm3.0V$	●	10	30		
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	±3.7	±3.9		V
I_S	Supply Current		●		32	38	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 7)	●		1.4	2.1	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: Exceeding the input common mode range may cause the output to invert.

Note 3: Slew rate is measured between ±1V on the output, with a ±0.3V input step.

Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

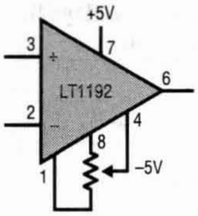
Note 5: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985. $A_V = -5$, $R_L = 1k$.

Note 6: NTSC (3.58MHz). For $R_L = 1k$, Diff $A_V = 0.1\%$, Diff Ph = 0.01°. Diff A_V and Diff Ph can be reduced for $A_V < 10$.

Note 7: See Applications section for shutdown at elevated temperatures. Do not operate the shutdown above $T_J > 125°C$.

Note 8: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

Optional Offset Nulling Circuit

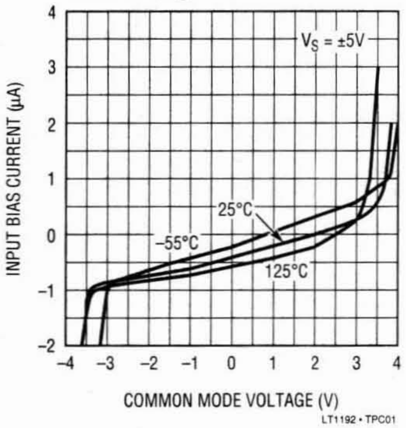


INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±20mV RANGE WITH A 1kΩ TO 10kΩ POTENTIOMETER.

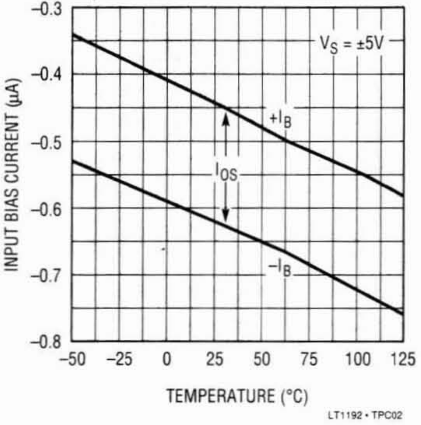
LT1192 • TA03

TYPICAL PERFORMANCE CHARACTERISTICS

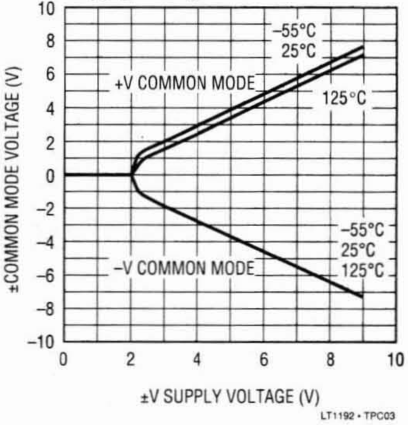
Input Bias Current vs Common Mode Voltage



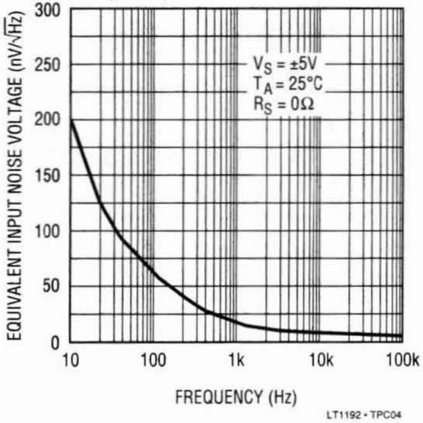
Input Bias Current vs Temperature



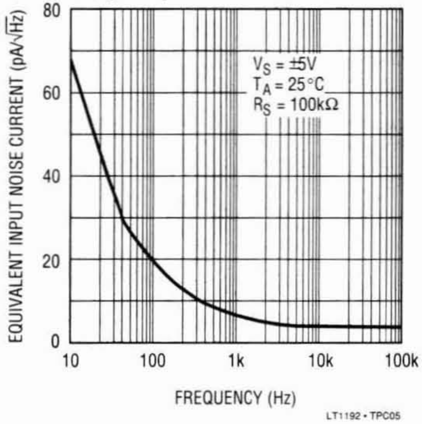
Common Mode Voltage vs Supply Voltage



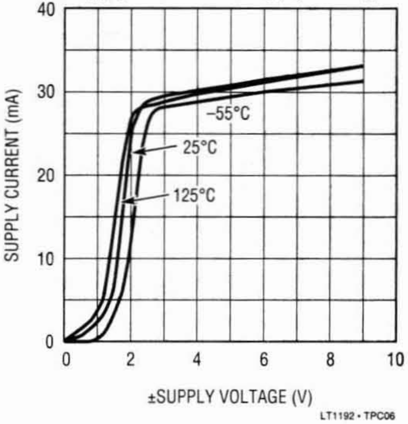
Equivalent Input Noise Voltage vs Frequency



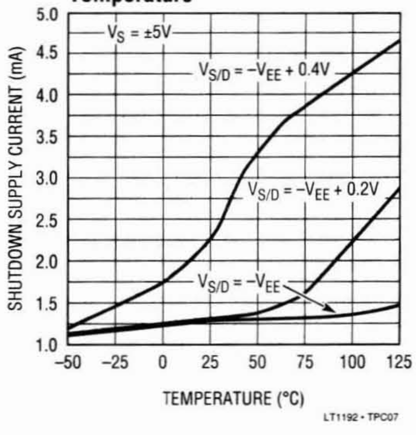
Equivalent Input Noise Current vs Frequency



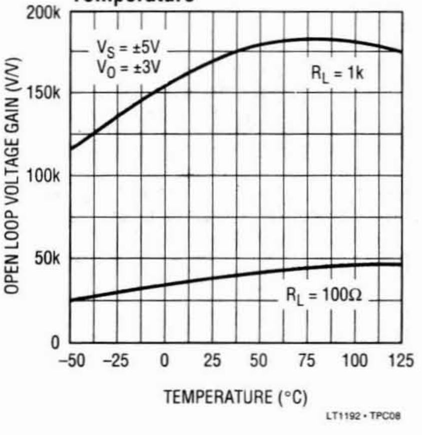
Supply Current vs Supply Voltage



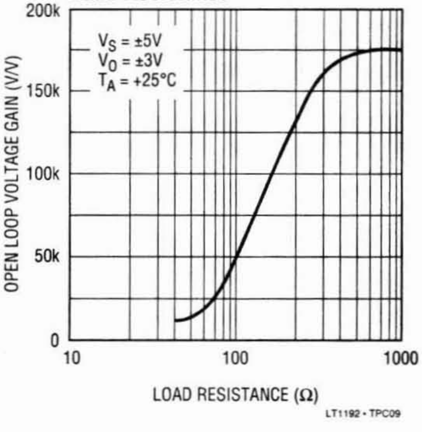
Shutdown Supply Current vs Temperature



Open Loop Voltage Gain vs Temperature

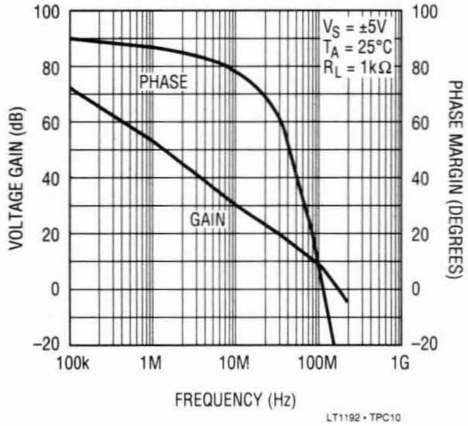


Open Loop Voltage Gain vs Load Resistance

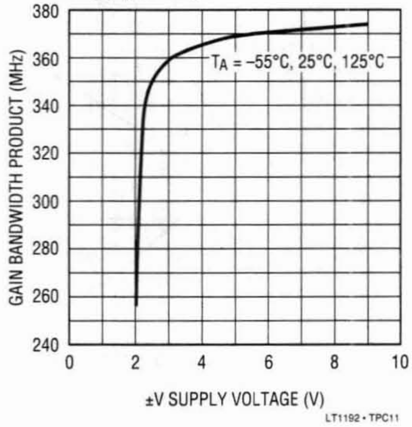


TYPICAL PERFORMANCE CHARACTERISTICS

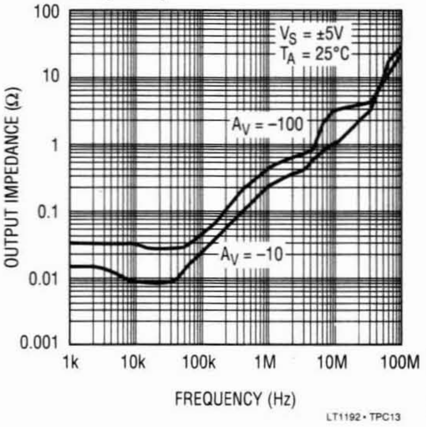
Gain, Phase vs Frequency



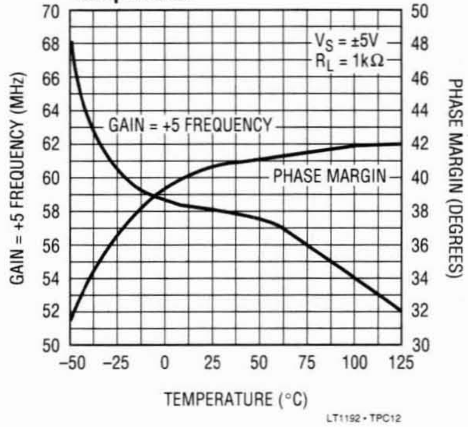
Gain Bandwidth Product vs Supply Voltage



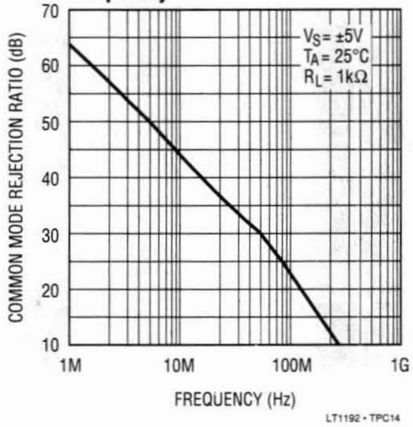
Output Inpedance vs Frequency



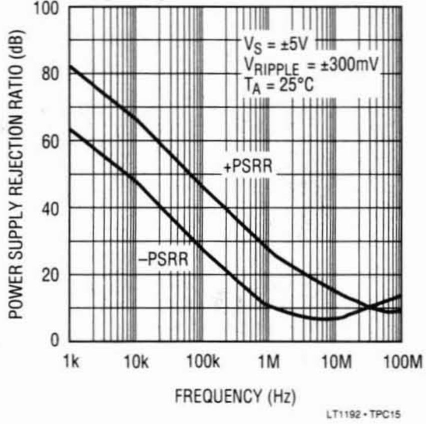
Gain and Phase Margin vs Temperature



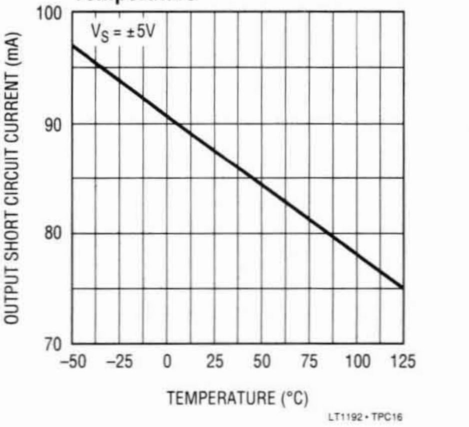
Common Mode Rejection Ratio vs Frequency



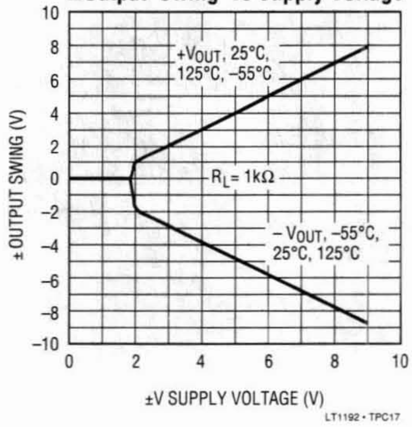
Power Supply Rejection Ratio vs Frequency



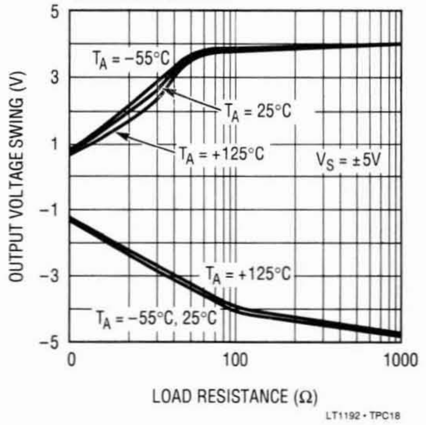
Output Short Circuit Current vs Temperature



±Output Swing vs Supply Voltage

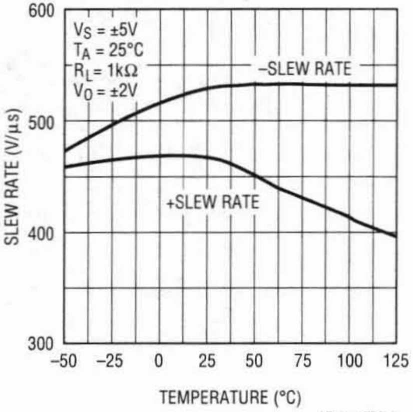


Output Voltage Swing vs Load Resistance



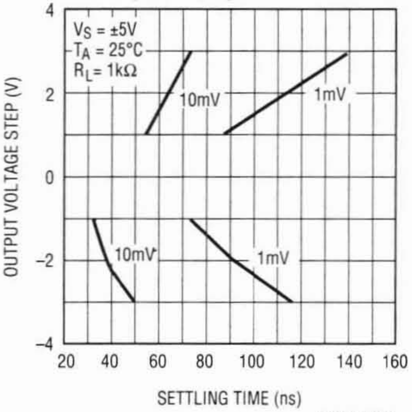
TYPICAL PERFORMANCE CHARACTERISTICS

Slew Rate vs Temperature



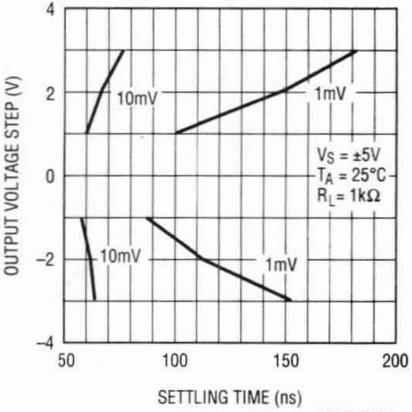
LT1192 • TPC19

Output Voltage Step vs Settling Time, A_V = –5



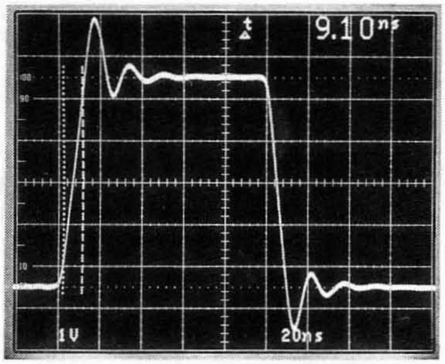
LT1192 • TPC20

Output Voltage Step vs Settling Time, A_V = +5



LT1192 • TPC21

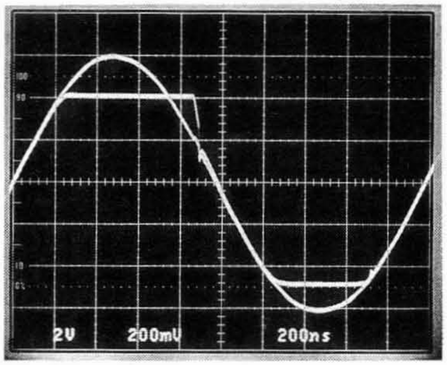
Large Signal Transient Response



A_V = +5, C_L = 10pF SCOPE PROBE

LT1192 • TPC22

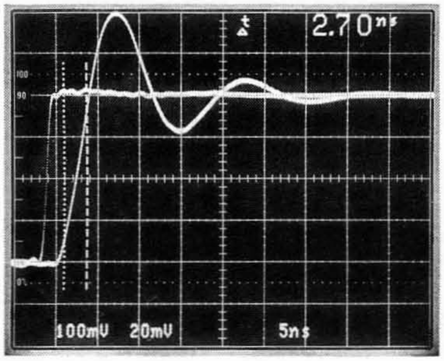
Output Overload



A_V = +10, V_{IN} = 1.2Vp-p

LT1192 • TPC24

Small Signal Transient Response



A_V = +5 SMALL SIGNAL RISE TIME, WITH FET PROBES

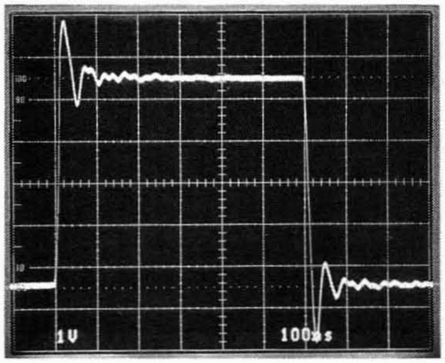
LT1192 • TPC23

APPLICATIONS INFORMATION

Power Supply Bypassing

The LT1192 is quite tolerant of power supply bypassing. In some applications a 0.1μF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, $R_L = 1k\Omega$.

No Supply Bypass Capacitors

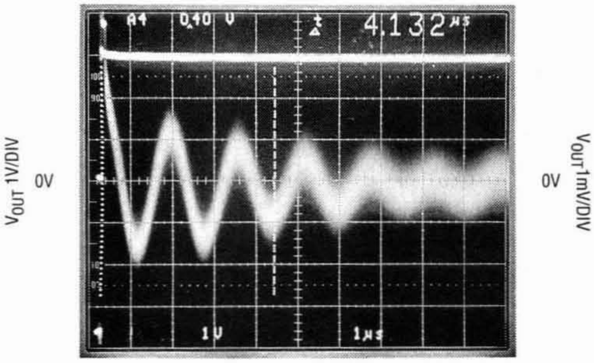


$A_V = -5$, IN DEMO BOARD, $R_L = 1k\Omega$

LT1192 • TA04

In most applications, and those requiring good settling time, it is important to use multiple bypass capacitors. A 0.1μF ceramic disc in parallel with a 4.7μF tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/div, when amplified to 1mV/div the settling time to 1mV is 4.132μs for the 0.1μF bypass; the time drops to 140ns with multiple bypass capacitors.

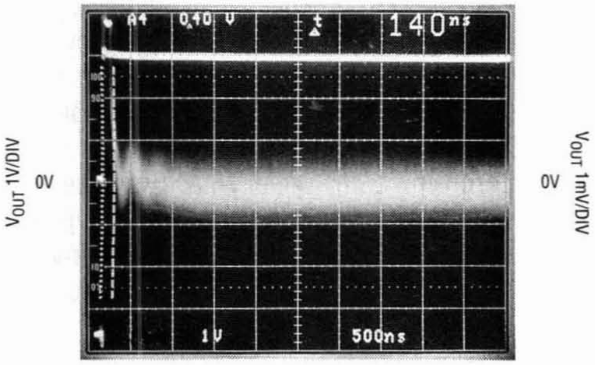
Settling Time Poor Bypass



SETTLING TIME TO 1mV, $A_V = -1$
SUPPLY BYPASS CAPACITORS = 0.1μF

LT1192 • TA05

Settling Time Good Bypass



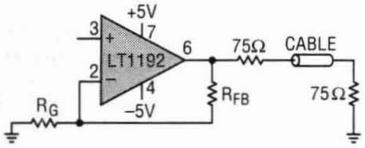
SETTLING TIME TO 1mV, $A_V = -1$ SUPPLY
BYPASS CAPACITORS = 0.1μF + 4.7μF TANTALUM

LT1192 • TA06

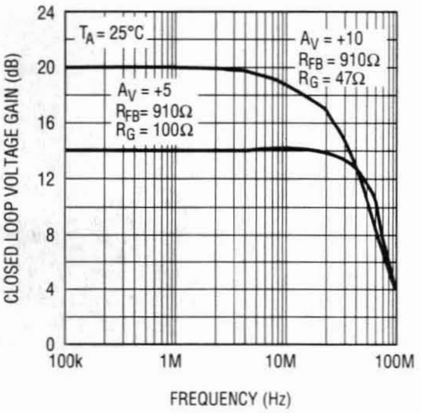
Cable Terminations

The LT1192 operational amplifier has been optimized as a low cost video cable driver. The ±50mA guaranteed output current enables the LT1192 to easily deliver 7.5Vp-p into 100Ω, while operating on ±5V supplies, or 2.6Vp-p on a single 5V supply.

Double Terminated Cable Driver



Cable Driver Voltage Gain vs Frequency



LT1192 • TA07

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With

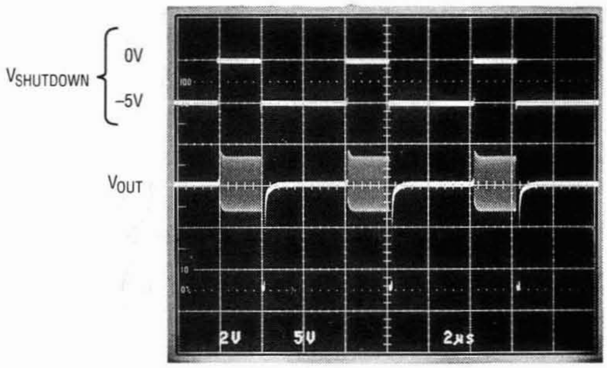
APPLICATIONS INFORMATION

single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. For a cable driver with a gain of +5 (op amp gain of +10) the –3dB bandwidth is 56MHz with only 0.25dB of peaking.

Using the Shutdown Feature

The LT1192 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 15kΩ in parallel with the feedback resistors. The amplifiers must be used in a non-inverting configuration for MUX applications. In inverting configurations the input signal is fed to the output through the feedback components. When the output is loaded with as little as 1kΩ from the amplifier's feedback resistors, the amplifier shuts off in 400ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN, A_V = +10, R_L = 1k

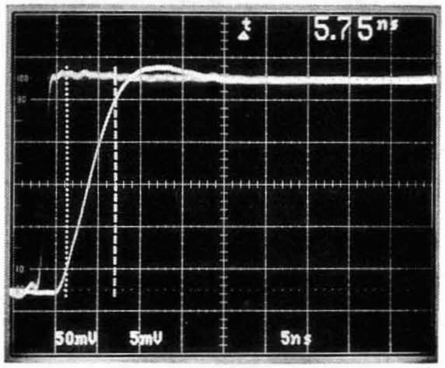
LT1192 • TA08

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperatures it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

Operating with Low Closed Loop Gains

When using de-compensated amplifiers it should be realized that peaking in the frequency domain, and overshoot and ringing in the time domain occur as closed loop gain is lowered. The LT1192 is stable to a closed loop gain of +5, however, peaking and ringing can be minimized by increasing the closed loop gain. For instance, the LT1192 peaks +5dB when used in a gain of +5, but peaks by less than 0.5dB for a closed loop gain of +10. Likewise, the overshoot drops from 50% to 4% for gains of +10.

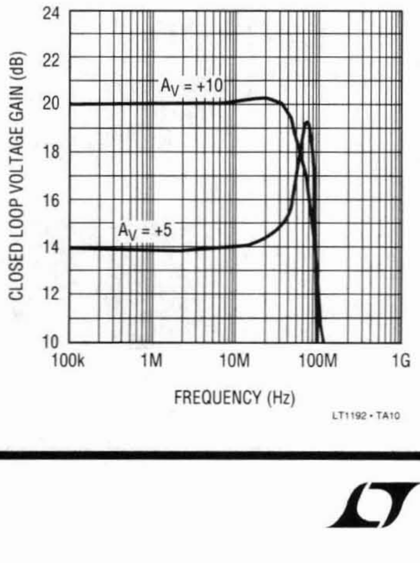
Small Signal Transient Response



A_V = +10 SMALL SIGNAL RISE TIME, WITH FET PROBES

LT1192 • TA09

Closed Loop Voltage Gain vs Frequency



LT1192 • TA10

APPLICATIONS INFORMATION

Murphy Circuits

There are several precautions the user should take when using the LT1192 in order to realize its full capability. Although the LT1192 can drive a 50pF load, isolating the capacitance with 20Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

Other precautions include:

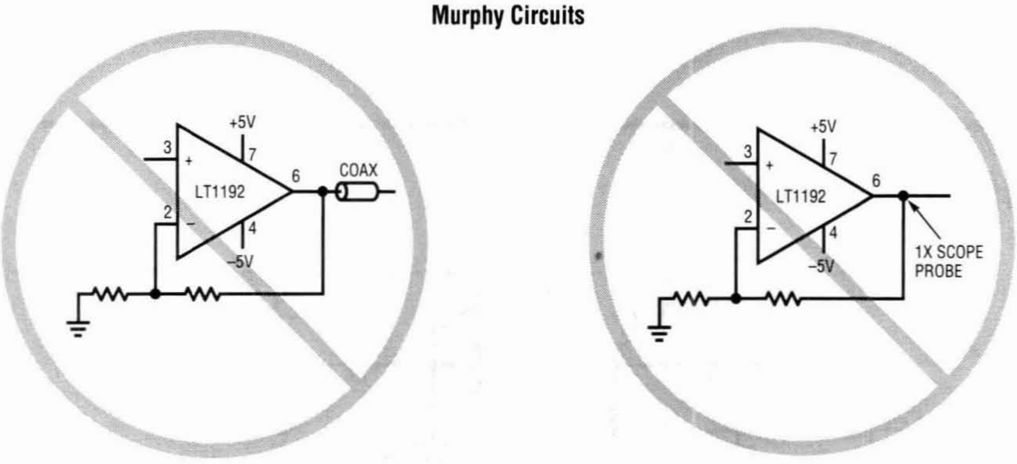
1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).

2. Do not use high source impedances. The input capacitance of 2pF, and R_S = 10kΩ for instance, will give an 8MHz −3dB bandwidth.

3. PC board socket may reduce stability.

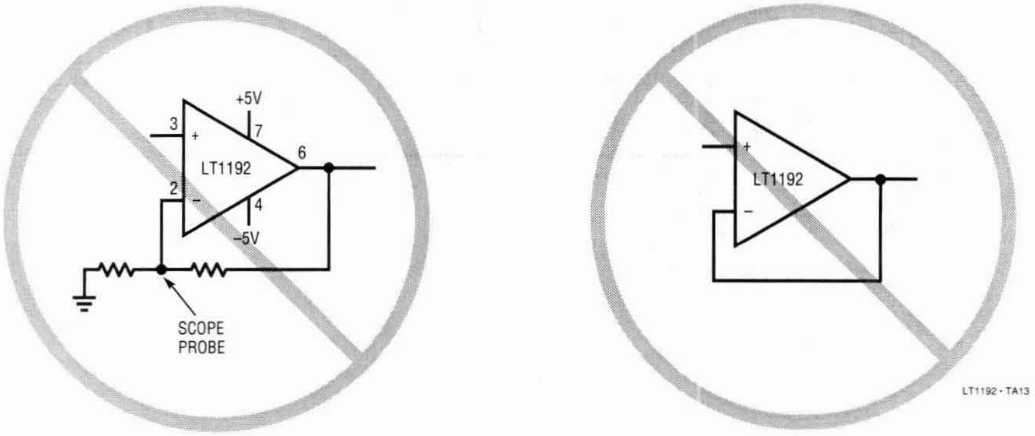
4. A feedback resistor of 1kΩ or lower reduces the effects of stray capacitance at the inverting input.

Murphy Circuits


+5V
3
+
7
LT1192
6
COAX
2
−
4
−5V
+5V
3
+
7
LT1192
6
2
−
4
−5V
1X SCOPE PROBE

An Unterminated Cable Is a Large Capacitive Load

A 1X Scope Probe Is a Large Capacitive Load

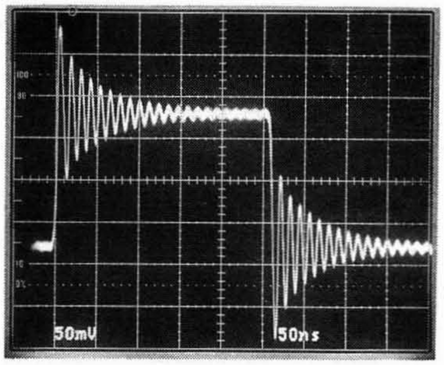

+5V
3
+
7
LT1192
6
2
−
4
−5V
SCOPE PROBE
+
LT1192
−
LT1192 • TA13

A Scope Probe on the Inverting Input Reduces Phase Margin

LT1192 Is Stable for Gains ≥ +5V/V

APPLICATIONS INFORMATION

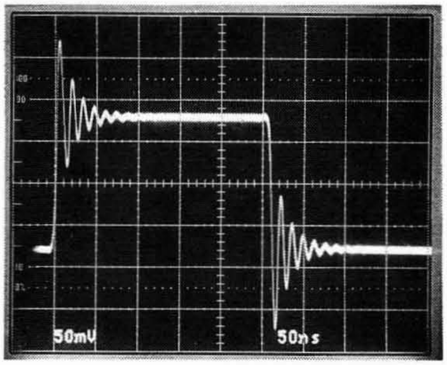
Driving Capacitive Load



$A_V = -5$, IN DEMO BOARD, $C_L = 50pF$

LT1192 • TA11

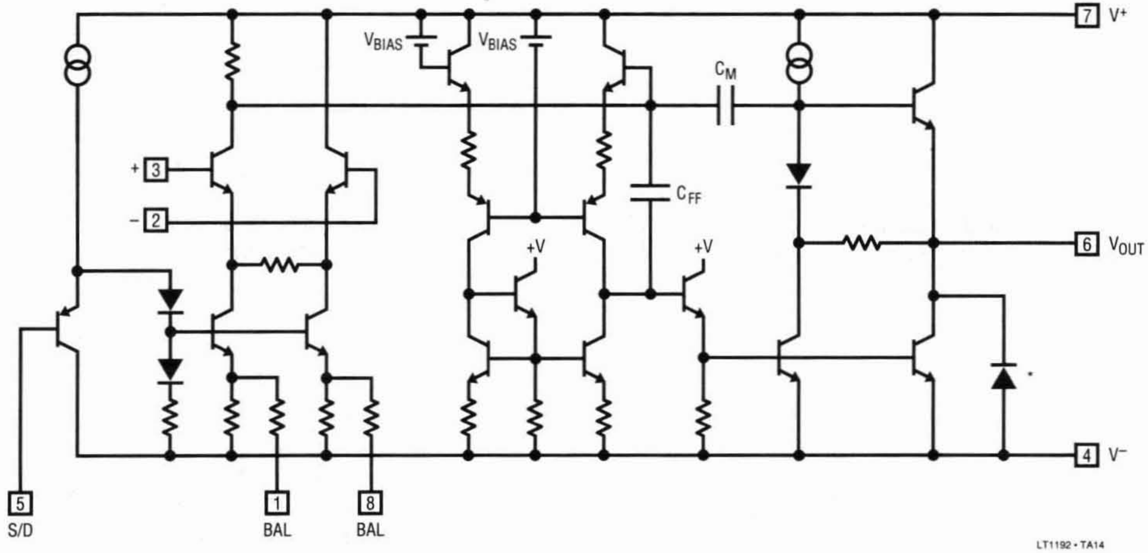
Driving Capacitive Load



$A_V = -5$, IN DEMO BOARD, $C_L = 50pF$ WITH 20Ω ISOLATING RESISTOR

LT1192 • TA12

SIMPLIFIED SCHEMATIC


7 V+
VBIAS
VBIAS
CM
+ 3
– 2
CFF
+V
+V
6 VOUT
4 V–
5 S/D
1 BAL
8 BAL
*

LT1192 • TA14

* SUBSTRATE DIODE, DO NOT FORWARD BIAS

LT1193

Video Difference Amplifier

FEATURES

- Differential or Single-Ended Gain Block (Adjustable)
- −3dB Bandwidth, $A_V = \pm 2$ 80MHz
- Slew Rate 500V/μs
- Low Cost
- Output Current ±50mA
- Settling Time 180ns to 0.1%
- CMRR @ 10MHz >40dB
- Differential Gain Error 0.2%
- Differential Phase Error 0.08°
- Single +5V Operation
- Drives Cables Directly
- Output Shutdown

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Cable Drivers
- Oscillators
- Tape and Disc Drive Systems

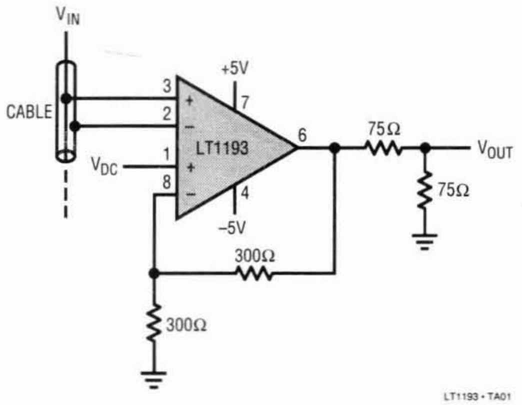
DESCRIPTION

The LT1193 is a video difference amplifier optimized for operation on ±5V, and a single +5V supply. This versatile amplifier features uncommitted high input impedance (+) and (−) inputs, and can be used in differential or single-ended configurations. Additionally, a second set of inputs give gain adjustment and DC control to the differential amplifier.

The LT1193's high slew rate, 500V/μs, wide bandwidth, 80MHz, and ±50mA output current, make it ideal for driving cables directly. The shutdown feature reduces the power dissipation to a mere 15mW, and allows multiple amplifiers to drive the same cable.

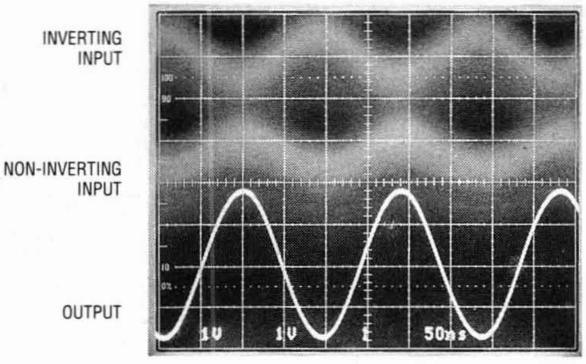
The LT1193 is available in 8-pin miniDIPs and SO packages.

Cable Sense Amplifier for Loop Through Connections with DC Adjust



LT1193 • TA01

Recovered Signal from Common Mode Noise



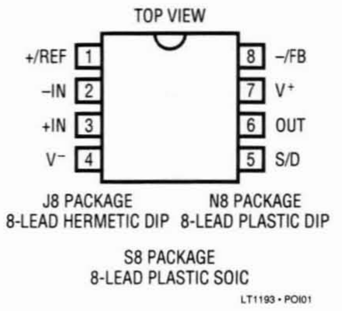
5MHz SINE WAVE RECOVERED FROM COMMON MODE NOISE, $A_V = +2$

LT1193 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage .... ± 6V
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Continuous
Operating Junction Temperature Range
  LT1193M .... −55°C to 150°C
  LT1193C .... 0°C to 150°C
Max. Junction Temperature .... See Pkg. Descriptions
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1193MJ8 LT1193CJ8 LT1193CN8 LT1193CS8
S8 PART MARKING
1193

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 2), $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1193M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs, (Note 3)		2.0	12.0	mV
I_{OS}	Input Offset Current	Either Input		0.2	3.0	µA
I_B	Input Bias Current	Either Input		±0.5	±3.5	µA
e_n	Input Noise Voltage	$f_O = 10kHz$		50		nV/√Hz
i_n	Input Noise Current	$f_O = 10kHz$		4.0		pA/√Hz
R_{IN}	Input Resistance	Either Input		100		kΩ
C_{IN}	Input Capacitance	Either Input		2.0		pF
$V_{IN\ LIM}$	Input Voltage Limit	(Note 4)		1.3		V
	Input Voltage Range		−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	60	75		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 8V$	60	75		dB
V_{OUT}	Output Voltage Swing	$V_S = \pm 5V$, $R_L = 1k$	±3.8	±4.0		V
		$V_S = \pm 8V$, $R_L = 1k$	±6.8	±7.0		
		$V_S = \pm 8V$, $R_L = 100\Omega$	6.4	6.6		
G_E	Gain Error	$V_O = \pm 3V$, $R_L = 1k$		0.1	1.0	%
		$R_L = 100\Omega$		0.1	1.2	
SR	Slew Rate	$V_O = \pm 2V$, $R_L = 300\Omega$, (Note 5, 10)	350	500		V/µs
FPBW	Full Power Bandwidth	$V_O = 6Vp\text{-}p$, (Note 6)	18.5	26.5		MHz
BW	Small Signal Bandwidth			9.0		MHz
t_r, t_f	Rise Time, Fall Time	$A_V = +50$, $V_O = \pm 1.5V$, 20% to 80% (Note 10)	110	160	210	ns
t_{PD}	Propagation Delay	$R_L = 1k$, $V_O = \pm 125mV$, 50% to 50%		15		ns
	Overshoot	$V_O = \pm 50mV$		0		%
t_s	Settling Time	3V Step, 0.1%, (Note 7)		180		ns
Diff A_V	Differential Gain	$R_L = 150\Omega$, $A_V = +2$, (Note 8)		0.2		%
Diff Ph	Differential Phase	$R_L = 150\Omega$, $A_V = +2$, (Note 8)		0.08		Deg. p-p
I_S	Supply Current			35	43	mA
	Shutdown Supply Current	Pin 5 at V^-		1.3	2.0	mA

ELECTRICAL CHARACTERISTICS

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 2), $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

			LT1193M/C			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-		20	50	μA
t_{on}	Turn On Time	Pin 5 from V^- to Ground, $R_L = 1k$		300		ns
t_{off}	Turn Off Time	Pin 5 from Ground to V^-, $R_L = 1k$		200		ns

ELECTRICAL CHARACTERISTICS

$V_{S+} = +5V$, $V_{S-} = 0V$, $V_{REF} = +2.5V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to V_{REF}, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 2), $T_A = 25°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

				LT1193M/C			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	Both Inputs, (Note 3)			3.0	15	mV
I_{OS}	Input Offset Current	Either Input			0.2	3.0	μA
I_B	Input Bias Current	Either Input			±0.5	±3.5	μA
	Input Voltage Range			+2.0		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = +2.0V$ to $+3.5V$		55	70		dB
V_{OUT}	Output Voltage Swing	$R_L = 100\Omega$ to Ground	V_{OUT} High	3.6	3.8		V
			V_{OUT} Low		0.25	0.4	
SR	Slew Rate	$V_O = +1V$ to $+3V$			250		V/μs
BW	Small Signal Bandwidth				8.0		MHz
I_S	Supply Current				32	40	mA
	Shutdown Supply Current	Pin 5 at V^-			1.3	2.0	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-			20	50	μA

ELECTRICAL CHARACTERISTICS

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB2} = 1k$ (Note 2), $T_A = -55°C \le T_A \le 125°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

				LT1193M			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		●		2.0	16	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		20		μV/°C
I_{OS}	Input Offset Current		●		0.8	5.0	μA
I_B	Input Bias Current		●		±1.0	±5.5	μA
	Input Voltage Range		●	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	53	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm5.0V$	●	53	70		dB
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	3.6	4.0		V
		$V_S = \pm8V$, $R_L = 100\Omega$	●	6.0	6.5		
G_E	Gain Error	$V_O = \pm3V$, $R_L = 1k$	●		0.2	1.2	%
I_S	Supply Current		●		35	43	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 9)	●		1.3	2.2	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		μA

ELECTRICAL CHARACTERISTICS

$V_S = \pm5V$, $V_{REF} = 0V$, $R_{FB1} = 900\Omega$ from pins 6 to 8, $R_{FB2} = 100\Omega$ from pin 8 to ground, $R_L = R_{FB1} + R_{FB2} = 1k$ (Note 2), $T_A = 0°C \le T_A \le 70°C$, $C_L \le 10pF$, pin 5 open circuit, unless otherwise noted.

				LT1193C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage		●		2.0	14	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift		●		20		µV/°C
I_{OS}	Input Offset Current		●		0.2	3.5	µA
I_B	Input Bias Current		●		±0.5	±4.0	µA
	Input Voltage Range		●	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$	●	55	70		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm5.0V$	●	55	70		dB
V_{OUT}	Output Voltage Swing	$R_L = 1k$	●	3.7	4.0		V
		$R_L = 100\Omega$	●	6.2	6.6		
G_E	Gain Error	$V_O = \pm3V$, $R_L = 1k$	●		0.2	1.2	%
I_S	Supply Current		●		35	43	mA
	Shutdown Supply Current	Pin 5 at V^-, (Note 9)	●		1.3	2.1	mA
$I_{S/D}$	Shutdown Pin Current	Pin 5 at V^-	●		20		µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: When $R_L = 1k$ is specified, the load resistor is $R_{FB1} + R_{FB2}$, but when $R_L = 100\Omega$ is specified, then an additional 100Ω is added to the output.

Note 3: V_{OS} measured at the output (pin 6) is the contribution from both input pair, and is input referred.

Note 4: $V_{IN\ LIM}$ is the maximum voltage between $-V_{IN}$ and $+V_{IN}$ (pin 2 and pin 3) for which the output can respond.

Note 5: Slew rate is measured between ±2V on the output, with a ±1V input step, $A_V = +3$.

Note 6: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

Note 7: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

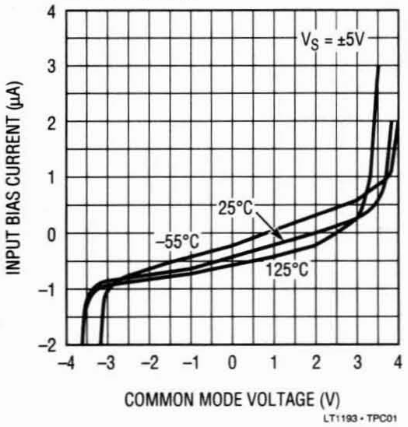
Note 8: NTSC (3.58MHz).

Note 9: See Applications section for shutdown at elevated temperatures. Do not operate the shutdown above $T_J > 125°C$.

Note 10: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

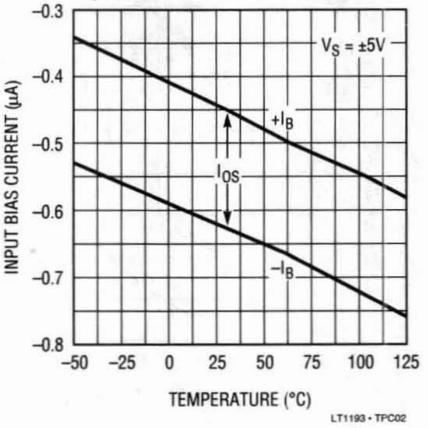
TYPICAL PERFORMANCE CHARACTERISTICS

Input Bias Current vs Common Mode Voltage



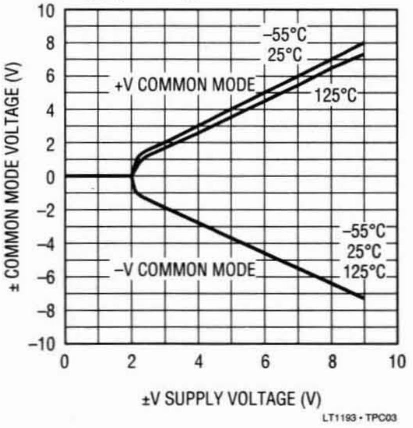
LT1193 • TPC01

Input Bias Current vs Temperature



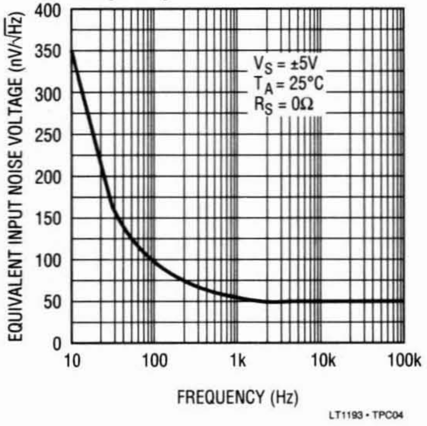
LT1193 • TPC02

Common Mode Voltage vs Supply Voltage



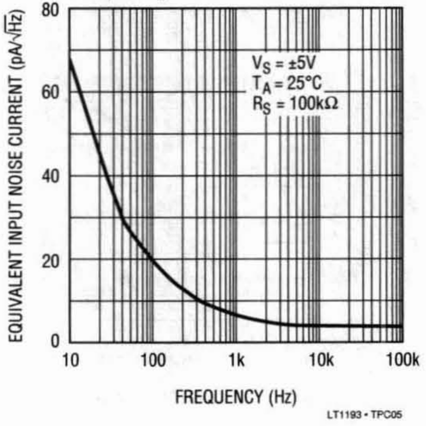
LT1193 • TPC03

Equivalent Input Noise Voltage vs Frequency



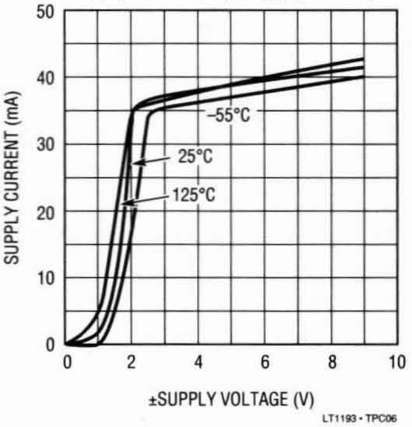
LT1193 • TPC04

Equivalent Input Noise Current vs Frequency



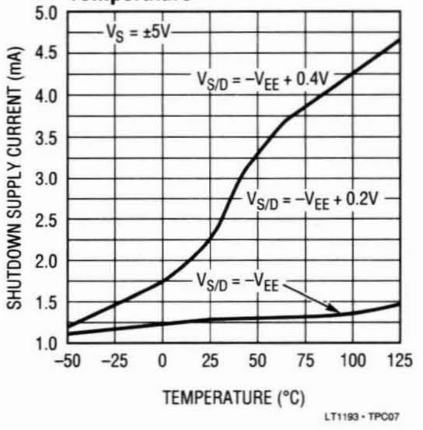
LT1193 • TPC05

Supply Current vs Supply Voltage



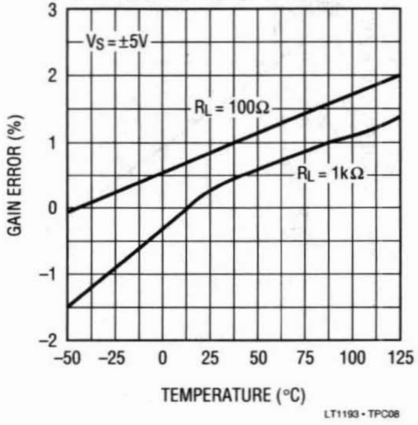
LT1193 • TPC06

Shutdown Supply Current vs Temperature



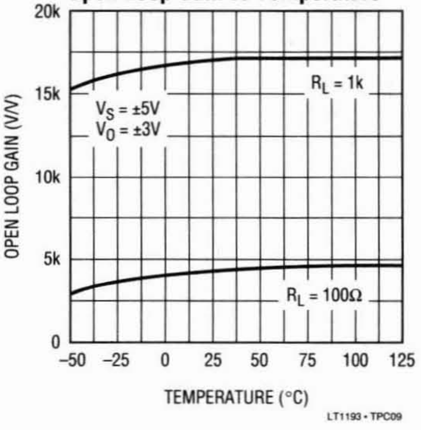
LT1193 • TPC07

Gain Error vs Temperature



LT1193 • TPC08

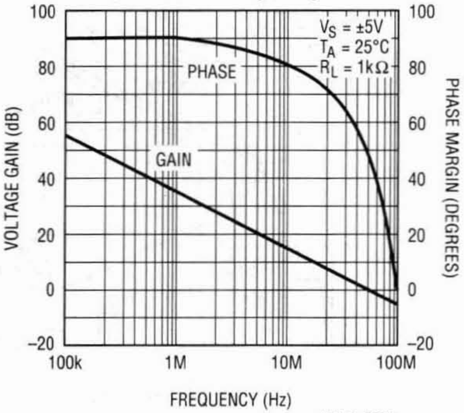
Open Loop Gain vs Temperature



LT1193 • TPC09

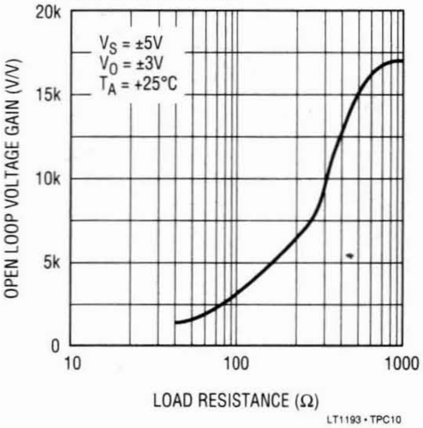
TYPICAL PERFORMANCE CHARACTERISTICS

Gain, Phase vs Frequency



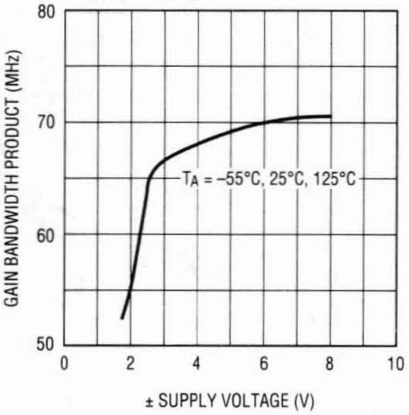
LT1193 • TPC11

Open Loop Voltage Gain vs Load Resistance



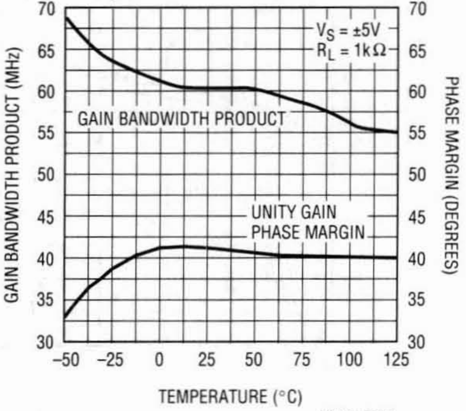
LT1193 • TPC10

Gain Bandwidth Product vs Supply Voltage



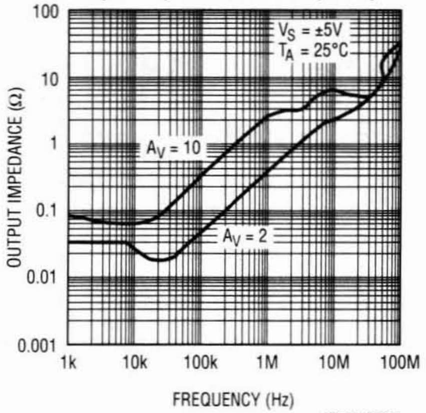
LT1193 • TPC12

Gain Bandwidth Product and Unity Gain Phase Margin vs Temperature



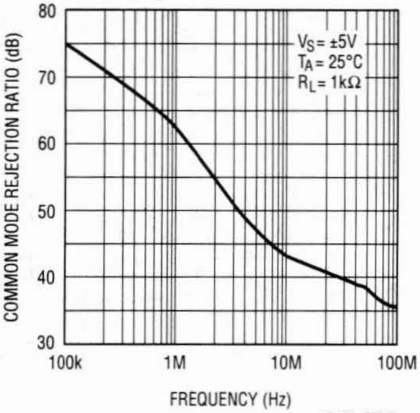
LT1193 • TPC13

Output Impedance vs Frequency



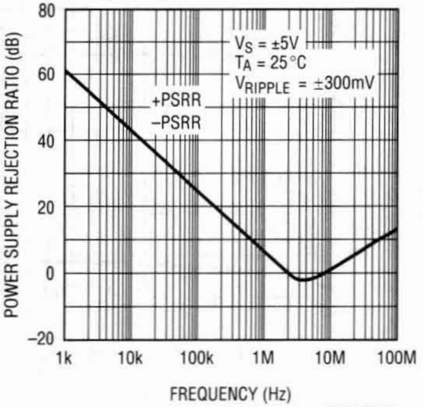
LT1193 • TPC14

Common Mode Rejection Ratio vs Frequency



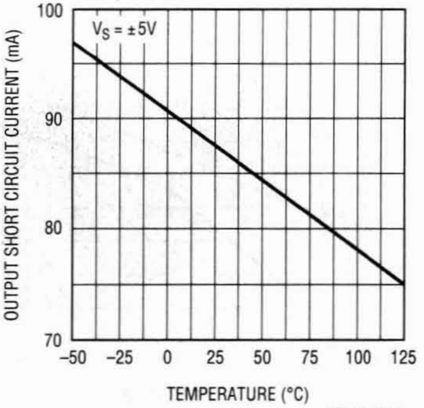
LT1193 • TPC15

Power Supply Rejection Ratio vs Frequency



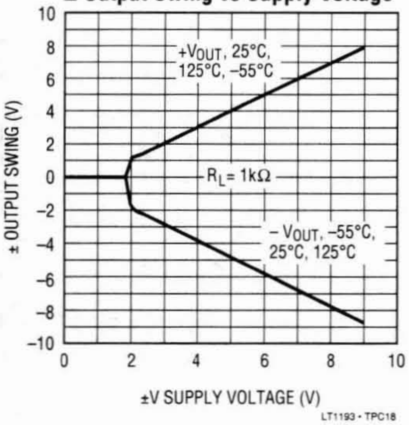
LT1193 • TPC16

Output Short Circuit Current vs Temperature



LT1193 • TPC17

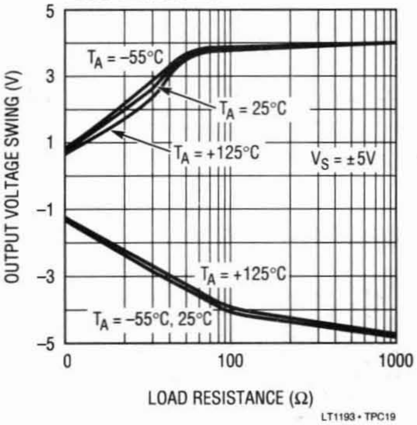
± Output Swing vs Supply Voltage



LT1193 • TPC18

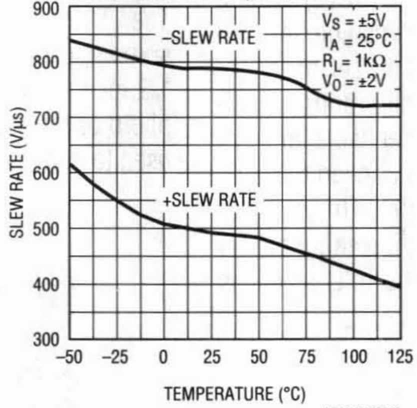
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Load Resistance



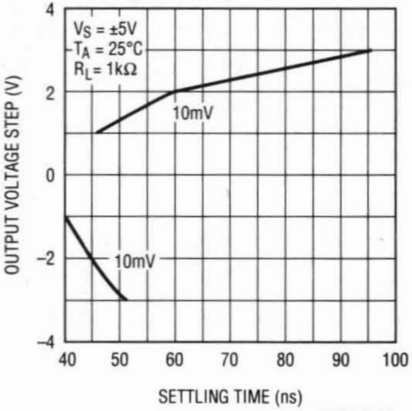
LT1193 • TPC19

Slew Rate vs Temperature



LT1193 • TPC20

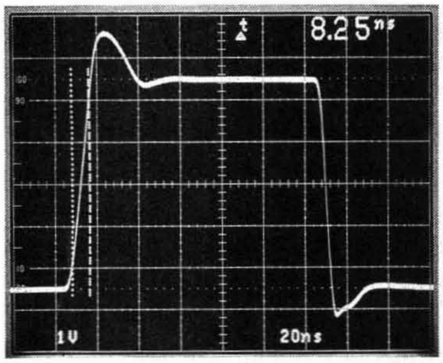
Output Voltage Step vs Settling Time, A_V = +2



LT1193 • TPC21

2

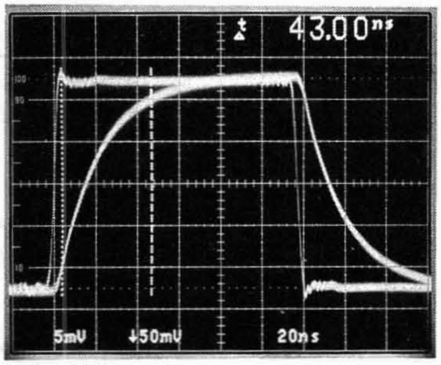
Large Signal Transient Response



A_V = +2, R_L = 150Ω, R_{FB} = 300Ω, R_G = 300Ω

LT1193 • TPC22

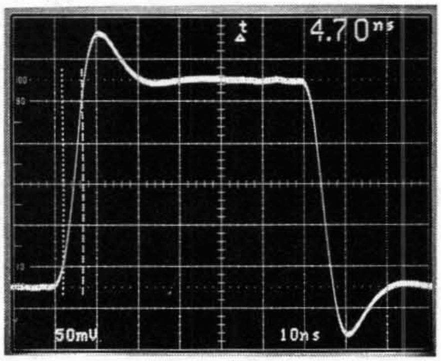
Small Signal Transient Response



A_V = −10, SMALL SIGNAL RISE TIME = 43ns

LT1193 • TPC23

Small Signal Transient Response

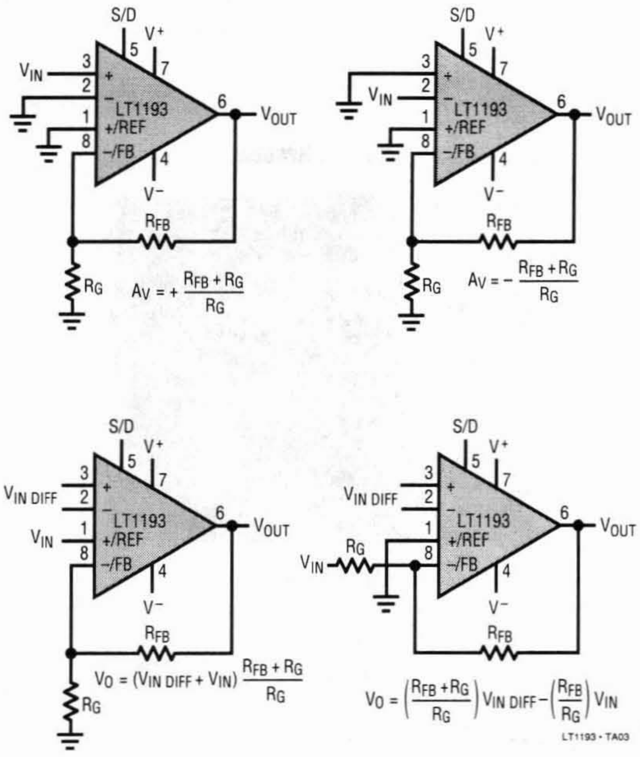


A_V = +2, R_{FB} = 300Ω, R_G = 300Ω, OVERSHOOT = 25%,
RISE TIME = 4.7ns

LT1193 • TPC24

APPLICATIONS INFORMATION

The LT1193 is a video difference amplifier which has two uncommitted high input impedance (+) and (–) inputs. The amplifier has one set of inputs which can be used for reference and feedback. Additionally, this set of inputs give gain adjust, and DC control to the differential amplifier. The voltage gain of the LT1193 is set like a conventional operational amplifier. Feedback is applied to pin 8, and it is optimized for gains of 2 or greater. The amplifier can be operated single-ended by connecting either the (+) or (–) inputs to the +/Reference pin 1. The voltage gain is set by the resistors: $(R_{FB} + R_G)/R_G$.



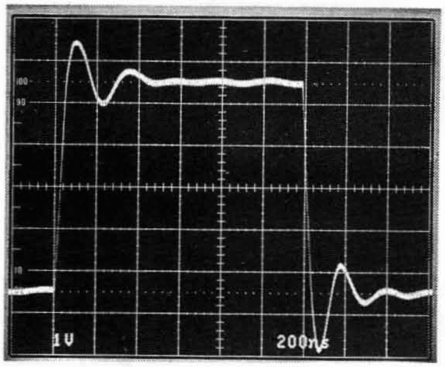
LT1193 • TA03

The primary usefulness of the LT1193 is in converting high speed differential signals to a single-ended output. The amplifier has common mode rejection beyond 50MHz, and a full power bandwidth of 40MHz at 4Vp-p. Like the single-ended case, the differential voltage gain is set by the external resistors: $(R_{FB} + R_G)/R_G$. The maximum input differential signal for which the output will respond is approximately ±1.3V.

Power Supply Bypassing

The LT1193 is quite tolerant of power supply bypassing. In some applications a 0.1µF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, $R_L = 1k\Omega$.

No Supply Bypass Capacitors

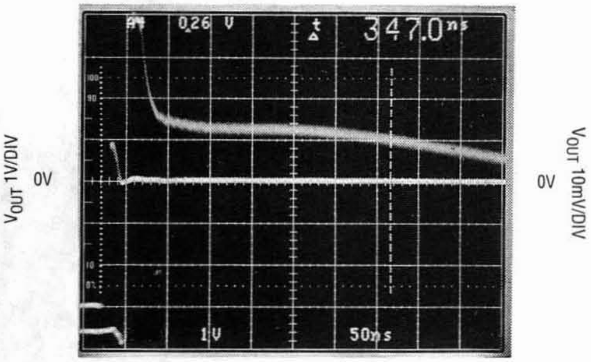


$A_V = +10$, IN DEMO BOARD, $R_L = 1k\Omega$

LT1193 • TA04

In many applications and those requiring good settling time it is important to use multiple bypass capacitors. A 0.1µF ceramic disc in parallel with a 4.7µF tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/div, when

Settling Time Poor Bypass

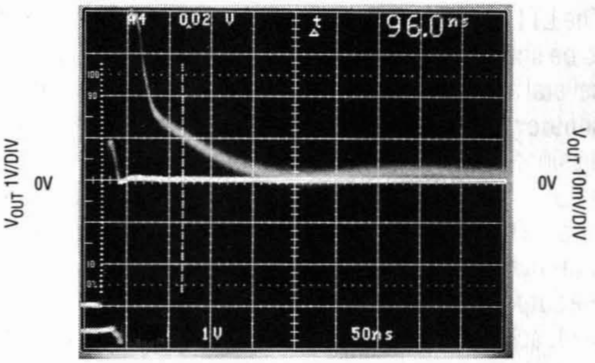


SETTLING TIME TO 10mV, $A_V = 2$
SUPPLY BYPASS CAPACITORS = 0.1µF

LT1193 • TA05

APPLICATIONS INFORMATION

Settling Time Good Bypass



SETTLING TIME TO 10mV, A_V = 2
SUPPLY BYPASS CAPACITORS = 0.1µF + 4.7µF TANTALUM

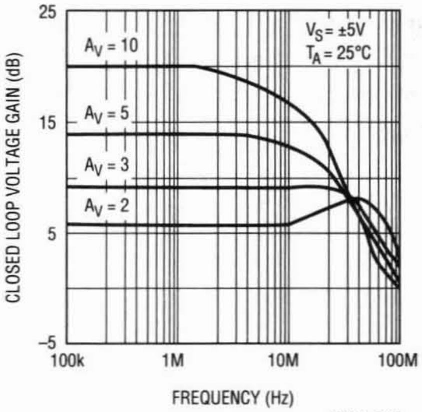
LT1193 • TA06

amplified to 10mV/div the settling time to 10mV is 347ns for the 0.1µF bypass; the time drops to 96ns with multiple bypass capacitors.

Operating With Low Closed Loop Gains

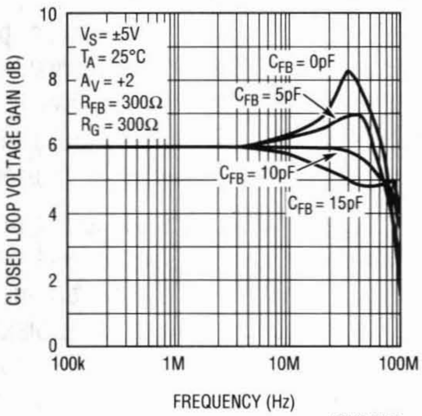
The LT1193 has been optimized for closed loop gains of 2 or greater; the frequency response illustrates the obtainable closed loop bandwidths. For a closed loop gain of 2 the response peaks about +2dB. Peaking can be minimized by keeping the feedback elements below 1kΩ, and can be eliminated by placing a capacitor across the feedback resistor, (feedback zero). This peaking shows up as time domain overshoot of about 40%. With the feedback capacitor it is eliminated.

Closed Loop Voltage Gain vs Frequency



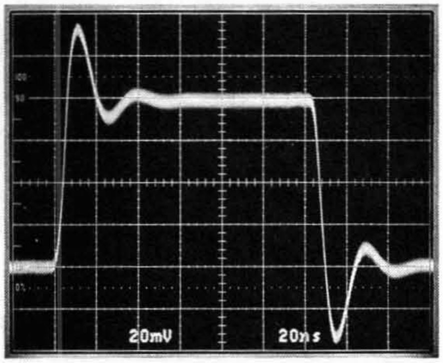
LT1193 • TA07

Closed Loop Voltage Gain vs Frequency



LT1193 • TA08

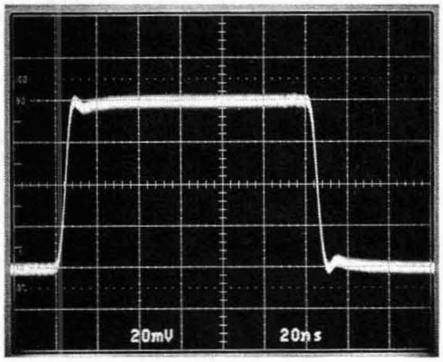
Small Signal Transient Response



A_V = +2, OVERSHOOT = 40%, R_{FB} = 1k, R_G = 1k

LT1193 • TA09

Small Signal Transient Response



A_V = +2, WITH 8pF FEEDBACK CAPACITOR
RISE TIME = 3.75ns, R_{FB} = 1k, R_G = 1k

LT1193 • TA10

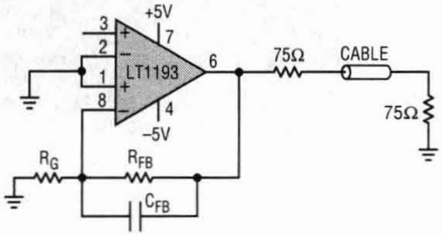
APPLICATIONS INFORMATION

Cable Terminations

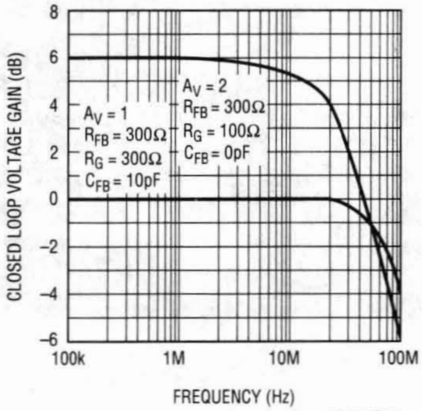
The LT1193 video difference amplifier has been optimized as a low cost cable driver. The ±50mA guaranteed output current enables the LT1193 to easily deliver 7.5Vp-p into 100Ω, while operating on ±5V supplies, and gains >3. On a single 5V supply the LT1193 can swing 2.6Vp-p for gains ≥2.

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. The cable driver has a –3dB bandwidth of 80MHz while driving a 150Ω load.

Double Terminated Cable Driver



Closed Loop Voltage Gain vs Frequency

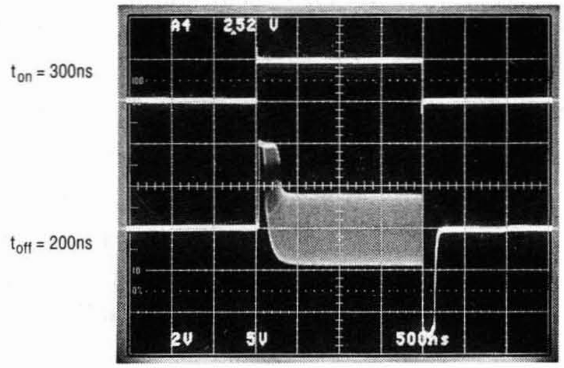


LT1193 • TA11

Using the Shutdown Feature

The LT1193 has a unique feature that allows the amplifier to be shutdown for conserving power, or for multiplexing several amplifiers onto a common cable. The amplifier will shutdown by taking pin 5 to V^-. In shutdown, the amplifier dissipates 15mW while maintaining a true high impedance output state of 15kΩ in parallel with the feedback resistors. The amplifiers may be connected inverting, non-inverting or differential for MUX applications. When the output is loaded with as little as 1kΩ from the amplifier's feedback resistors, the amplifier shuts off in 200ns. This shutoff can be under the control of HC CMOS operating between 0V and –5V.

Output Shutdown



1MHz SINE WAVE GATED OFF WITH SHUTDOWN PIN,
$A_V = +3$, $R_{FB} = 1k\Omega$, $R_G = 500\Omega$

LT1193 • TA12

The ability to maintain shutoff is shown on the curve Shutdown Supply Current vs Temperature in the Typical Performance Characteristics section. At very high elevated temperatures it is important to hold the shutdown pin close to the negative supply to keep the supply current from increasing.

APPLICATIONS INFORMATION

Murphy Circuits

There are several precautions the user should take when using the LT1193 in order to realize its full capability. Although the LT1193 can drive a 30pF in gains as low as 2, isolating the capacitance with 10Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

Other precautions include:

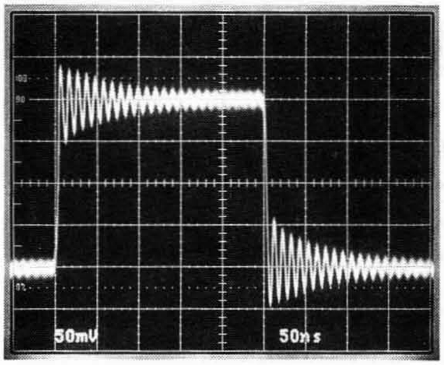
1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).

2. Do not use high source impedances. The input capacitance of 2pF, and $R_S = 10k\Omega$ for instance, will give an 8MHz –3dB bandwidth.

3. PC board socket may reduce stability.

4. A feedback resistor of 1kΩ or lower reduces the effects of stray capacitance at the inverting input. (For instance, closed loop gain of ±2 can use $R_{FB} = 300\Omega$ and $R_G = 300\Omega$.)

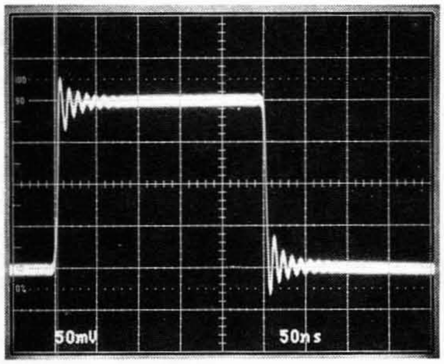
Driving Capacitive Load



$A_V = +2$, IN DEMO BOARD, $C_L = 30pF$
$R_{FB} = 1k$, $R_G = 1k$

LT1193 • TA14

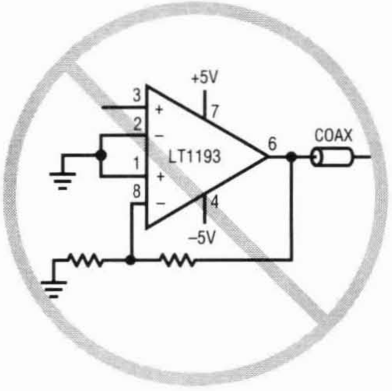
Driving Capacitive Load



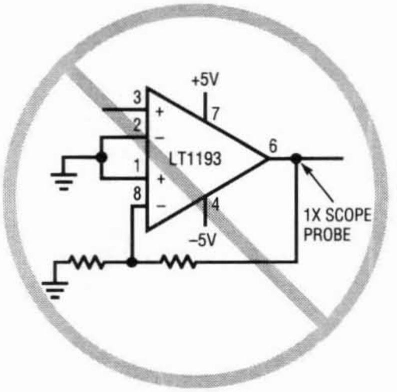
$A_V = +2$, IN DEMO BOARD, $C_L = 30pF$
WITH 10Ω ISOLATING RESISTOR

LT1193 • TA15

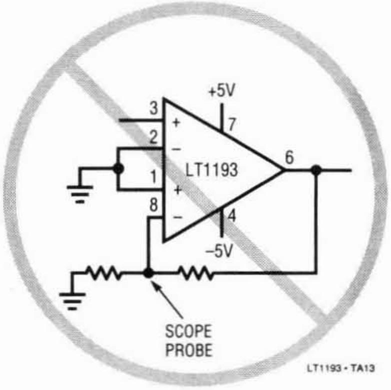
Murphy Circuits



An Unterminated Cable Is a Large Capacitive Load



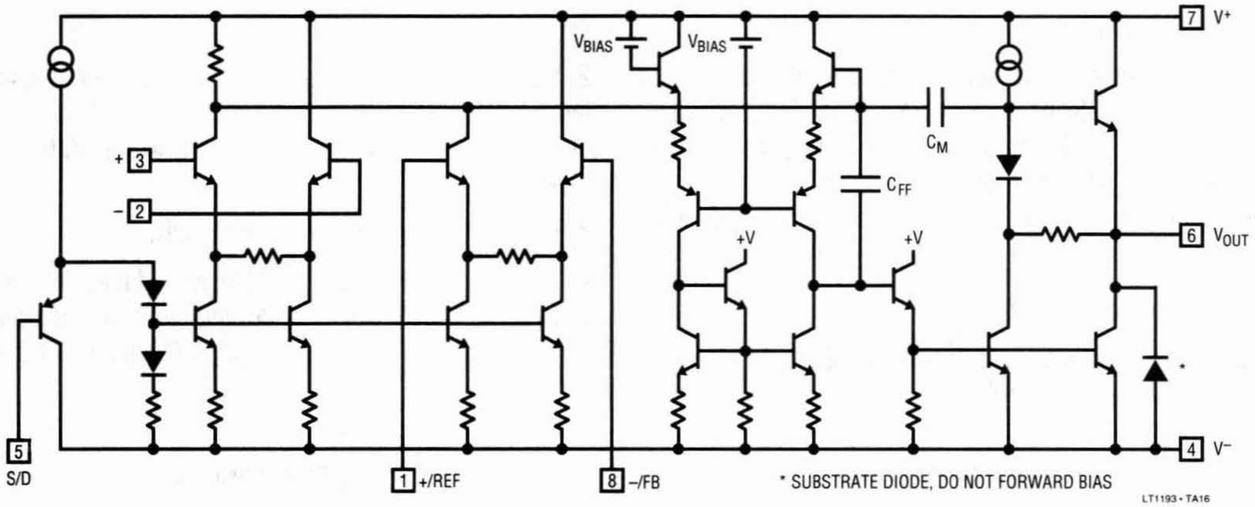
A 1X Scope Probe Is a Large Capacitive Load



LT1193 • TA13

A Scope Probe on the Inverting Input Reduces Phase Margin

SIMPLIFIED SCHEMATIC


7 V+
V_BIAS
V_BIAS
+ 3
– 2
C_M
C_FF
+V
+V
6 V_OUT
5 S/D
1 +/REF
8 –/FB
4 V–
*
LT1193 • TA16

* SUBSTRATE DIODE, DO NOT FORWARD BIAS

LT1194

Video Difference Amplifier

FEATURES

■ Differential or Single-Ended Gain Block	±10 (20dB)
■ –3dB Bandwidth	35MHz
■ Slew Rate	500V/μs
■ Low Cost	
■ Output Current	±50mA
■ Settling Time	200ns to 0.1%
■ CMRR @ 10MHz	45dB
■ Differential Gain Error	0.2%
■ Differential Phase Error	0.08°
■ Input Amplitude Limiting	
■ Single +5V Operation	
■ Drives Cables Directly	

APPLICATIONS

- Line Receivers
- Video Signal Processing
- Gain Limiting
- Oscillators
- Tape and Disc Drive Systems

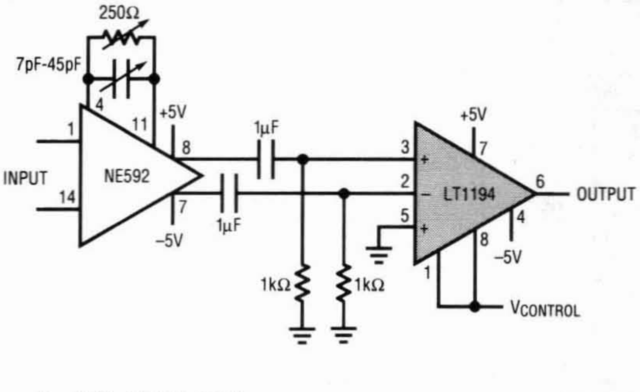
DESCRIPTION

The LT1194 is a video difference amplifier optimized for operation on ±5V, and a single +5V supply. The amplifier has a fixed gain of 20dB, and features adjustable input limiting to control tough over-drive applications. It has uncommitted high input impedance (+) and (–) inputs, and can be used in differential or single-ended configurations.

The LT1194's high slew rate, 500V/μs, wide bandwidth, 35MHz, and ±50mA output current, make it ideal for driving cables directly. This versatile amplifier is easy to use for video, or applications requiring speed, accuracy, and low cost.

The LT1194 is available in 8-pin miniDIPs and SO packages.

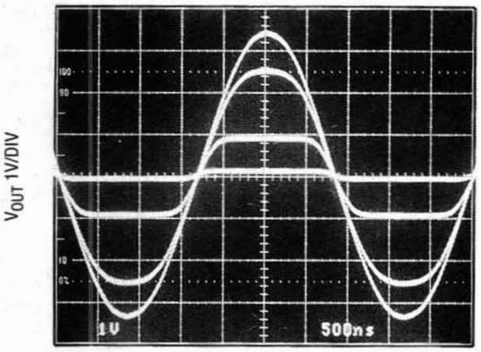
Wideband Differential Amplifier with Limiting



A_V = 1000, –3dB BW = 35MHz

LT1194 • TA01

Sine Wave Reduced by Limiting



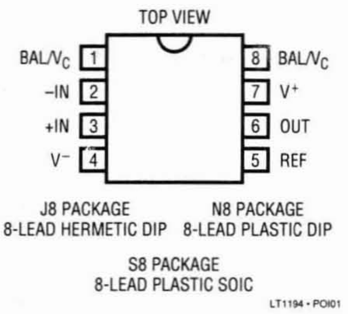
200kHz SINE WAVE WITH $V_{CONTROL}$ = –5V, –4V, –3V, –2V

LT1194 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Differential Input Voltage .... ±6V
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Continuous
Operating Junction Temperature Range
  LT1194M .... −55°C to 150°C
  LT1194C .... 0°C to 150°C
Max. Junction Temperature .... See Pkg. Descriptions
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1194MJ8 LT1194CJ8 LT1194CN8 LT1194CS8
S8 PART MARKING
1194

ELECTRICAL CHARACTERISTICS

$V_S = \pm5V$, $V_{REF} = 0V$, Null pins 1 and 8 open circuit, $T_A = 25°C$, $C_L \le 10pF$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LT1194M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage				1.0	6.0	mV
I_{OS}	Input Offset Current				0.2	3.0	μA
I_B	Input Bias Current				±0.5	±3.5	μA
e_n	Input Noise Voltage	$f_O = 10kHz$			15		$nV/\sqrt{Hz}$
i_n	Input Noise Current	$f_O = 10kHz$			4.0		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	Either Input			30		kΩ
C_{IN}	Input Capacitance	Either Input			2.0		pF
	Input Voltage Range			−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$		65	80		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm8V$		65	80		dB
V_{OMAX}	Maximum Output Signal	$V_S = \pm8V$, (Note 2)		±3.9	±4.3		V
V_{LIM}	Output Voltage Limit	$V_i = \pm0.5V$, $V_C = +2V$, (Note 3)			±20	±120	mV
V_{OUT}	Output Voltage Swing	$V_S = \pm8V$, $V_{REF} = +3V$	$R_L = 1k$	+6.6	+6.9		V
			$R_L = 100\Omega$	+6.3	+6.7		
		$V_S = \pm8V$, $V_{REF} = -3V$	$R_L = 1k$	−6.7	−7.4		
			$R_L = 100\Omega$	−6.4	−6.7		
		$V_S = \pm5V$, $V_{REF} = 0V$, $R_L = 1k$		±3.8	±4.0		
G_E	Gain Error	$V_O = \pm3V$	$R_L = 1k$		0.5	3.0	%
			$R_L = 100\Omega$		0.5	3.0	
SR	Slew Rate	$V_O = \pm1V$, $R_L = 1k$, (Note 4, 8)		350	500		V/μs
FPBW	Full Power Bandwidth	$V_O = 6Vp\text{-}p$, (Note 5)		18.5	26.5		MHz
BW	Small Signal Bandwidth				35		MHz
t_r, t_f	Rise Time, Fall Time	$R_L = 1k$, $V_O = \pm500mV$, 20% to 80%, (Note 8)		4.0	6.0	8.0	ns
t_{PD}	Propagation Delay	$R_L = 1k$, $V_O = \pm125mV$, 50% to 50%			6.5		ns
	Overshoot	$V_O = \pm125mV$			0		%

ELECTRICAL CHARACTERISTICS

V_S = ±5V, V_{REF} = 0V, Null pins 1 and 8 open circuit, T_A = 25°C, C_L ≤ 10pF, unless otherwise noted.

			LT1194M/C			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
t_S	Settling Time	3V Step, 0.1%, (Note 6)		200		ns
Diff A_V	Differential Gain	R_L = 150Ω, (Note 7)		0.2		%
Diff Ph	Differential Phase	R_L = 150Ω, (Note 7)		0.08		Deg p-p
I_S	Supply Current			35	43	mA

ELECTRICAL CHARACTERISTICS

V_S+ = +5V, V_S− = 0V, V_{REF} = +2.5V, Null pins 1 and 8 open circuit, T_A = 25°C, C_L ≤ 10pF, unless otherwise noted.

				LT1194M/C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage				2.0	8.0	mV
I_{OS}	Input Offset Current				0.2	3.0	μA
I_B	Input Bias Current				±0.5	±3.0	μA
	Input Voltage Range			+2.0		+3.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = +2.0V to +3.5V		55	70		dB
V_{LIM}	Output Voltage Limit	V_i = ±0.5V, V_C = +2V, (Note 3)			±20	±120	mV
V_{OUT}	Output Voltage Swing	R_L = 100Ω to Ground	V_{OUT} High	3.6	3.8		V
			V_{OUT} Low		0.25	0.4	
SR	Slew Rate	V_O = +1V to +3V			250		V/μs
BW	Small Signal Bandwidth				32		MHz
I_S	Supply Current				32	40	mA

ELECTRICAL CHARACTERISTICS

V_S+ = ±5V, V_{REF} = 0V, Null pins 1 and 8 open circuit, −55°C ≤ T_A ≤ 125°C, unless otherwise noted.

					LT1194M			
SYMBOL	**PARAMETER**	**CONDITIONS**			**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage			●		1.0	9.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			●		6.0		μV/°C
I_{OS}	Input Offset Current			●		0.8	5.0	μA
I_B	Input Bias Current			●		±1.0	±5.5	μA
	Input Voltage Range			●	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	V_{CM} = −2.5V to +3.5V		●	58	80		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±5.0V		●	60	80		dB
V_{LIM}	Output Voltage Limit	V_i = ±0.5V, V_C = +2V, (Note 3)		●		±20	±150	mV
V_{OUT}	Output Voltage Swing	V_S = ±8V V_{REF} = +3V	R_L = 1k	●	+6.0	+6.6		V
			R_L = 100Ω	●	+5.9	+6.5		
		V_S = ±8V V_{REF} = −3V	R_L = 1k	●	−6.1	−6.7		
			R_L = 100Ω	●	−6.0	−6.5		
G_E	Gain Error	V_O = ±3V, R_L = 1k		●		1.0	5.0	%
I_S	Supply Current			●		35	43	mA

ELECTRICAL CHARACTERISTICS

$V_S+ = \pm5V$, $V_{REF} = 0V$, Null pins 1 and 8 open circuit, $0°C \le T_A \le 70°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			LT1194C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage			●		1.0	7.0	mV
$\Delta V_{OS}/\Delta T$	Input V_{OS} Drift			●		6.0		µV/°C
I_{OS}	Input Offset Current			●		0.2	3.5	µA
I_B	Input Bias Current			●		±0.5	±4.0	µA
	Input Voltage Range			●	−2.5		+3.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = -2.5V$ to $+3.5V$		●	60	80		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm5.0V$		●	60	80		dB
V_{LIM}	Output Voltage Limit	$V_i = \pm0.5V$, $V_C = +2V$, (Note 3)		●		±20	±130	mV
V_{OUT}	Output Voltage Swing	$V_S = \pm8V$ $V_{REF} = +3V$	$R_L = 1k$	●	+6.2	+6.9		V
			$R_L = 100\Omega$	●	+6.1	+6.7		
		$V_S = \pm8V$ $V_{REF} = -3V$	$R_L = 1k$	●	−6.4	−7.2		
			$R_L = 100\Omega$	●	−6.2	−6.6		
G_E	Gain Error	$V_O = \pm3V$, $R_L = 1k$		●		1.0	4.0	%
I_S	Supply Current			●		35	43	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.

Note 2: There are two limitations on signal swing. Output swing is limited by clipping or saturation in the output stage. Input swing is controlled by an adjustable input limiting function. On $V_S = \pm5V$, the overload characteristic is output limiting, but on ±8V the overload characteristic is input limiting. V_{OMAX} is measured with the null pins open circuit.

Note 3: Output amplitude is reduced by the input limiting function. The input limiting function occurs when the null pins, 1 and 8, are tied together and raised to a potential 0.3V or more above the negative supply.

Note 4: Slew rate is measured between ±1V on the output, with a ±0.3V input step.

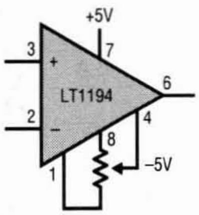
Note 5: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

Note 6: Settling time measurement techniques are shown in "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985.

Note 7: NTSC (3.58MHz).

Note 8: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged part (S suffix).

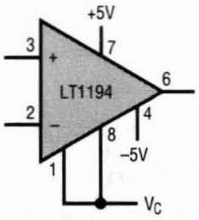
Optional Offset Nulling Circuit



INPUT OFFSET VOLTAGE CAN BE ADJUSTED OVER A ±250mV RANGE WITH A 1kΩ TO 10kΩ POTENTIOMETER

LT1194 • TA03

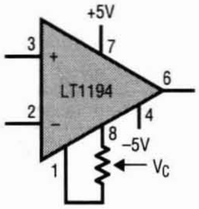
Input Limiting Connection



(NOTE 3)

LT1194 • TA04

Input Limiting with Offset Nulling

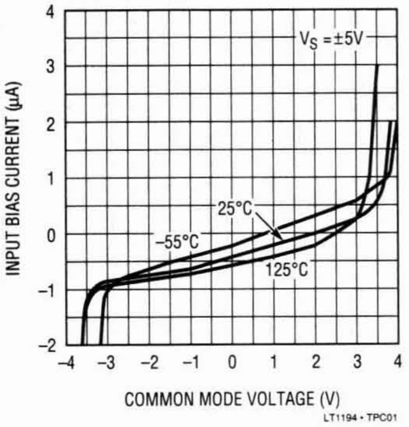


(NOTE 3)

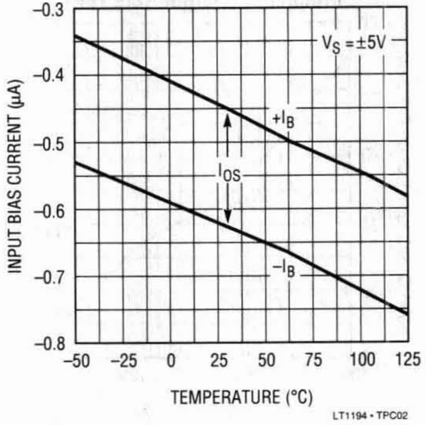
LT1194 • TA05

TYPICAL PERFORMANCE CHARACTERISTICS

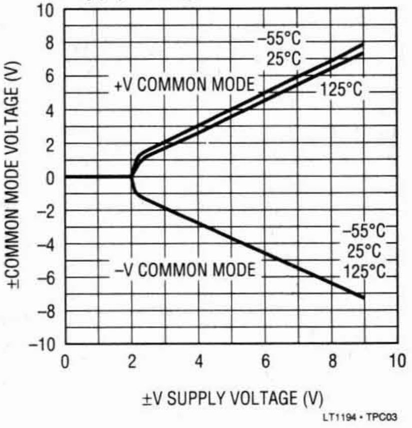
Input Bias Current vs Common Mode Voltage



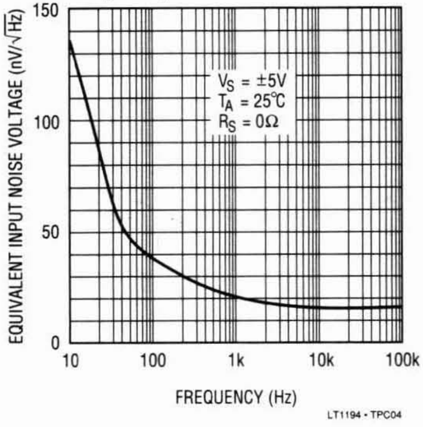
Input Bias Current vs Temperature



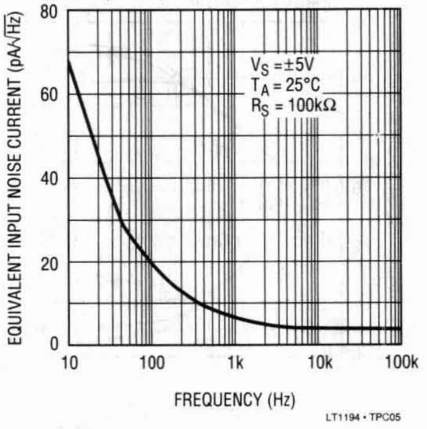
Common Mode Voltage vs Supply Voltage



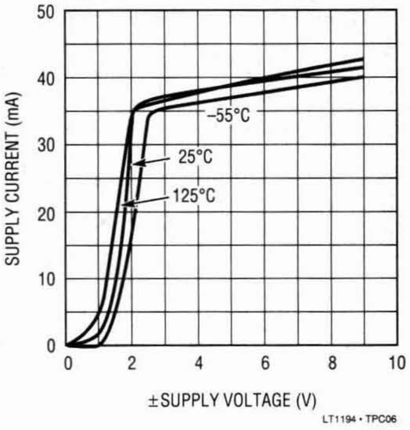
Equivalent Input Noise Voltage vs Frequency



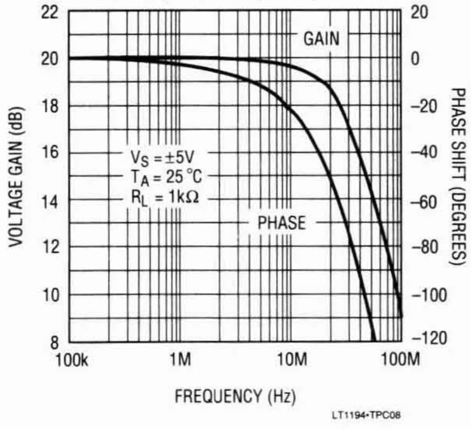
Equivalent Input Noise Current vs Frequency



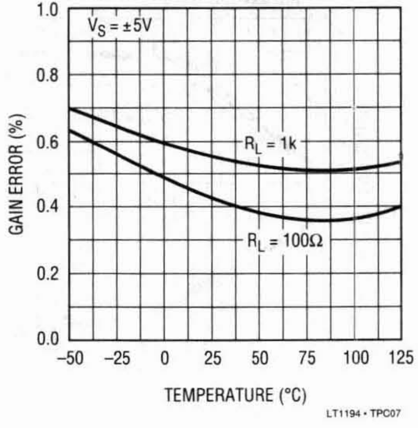
Supply Current vs Supply Voltage



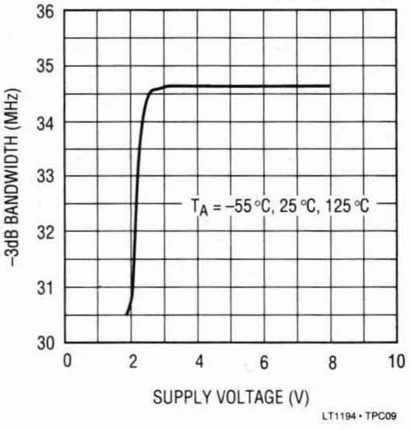
Gain, Phase vs Frequency



Gain Error vs Temperature

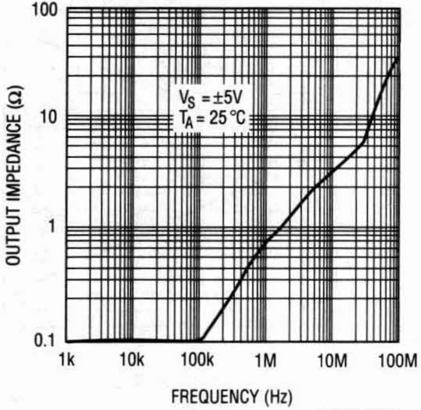


−3dB Bandwidth vs Supply Voltage



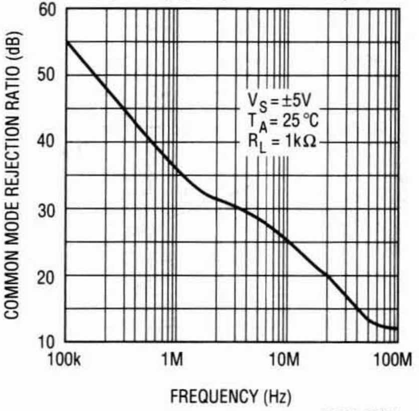
TYPICAL PERFORMANCE CHARACTERISTICS

Output Impedance vs Frequency



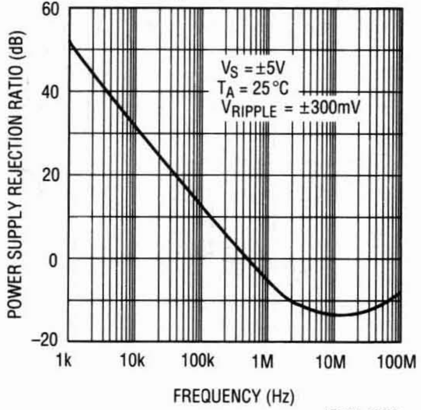
LT1194 • TPC10

Common Mode Rejection Ratio vs Frequency (Output Referred)



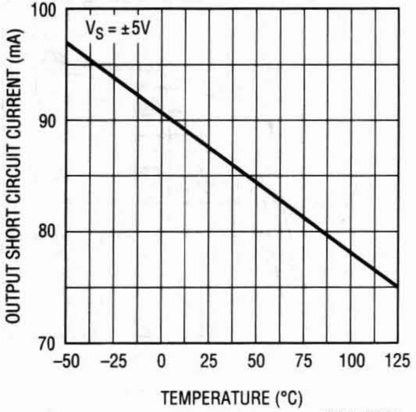
LT1194 • TPC11

Power Supply Rejection Ratio vs Frequency (Output Referred)



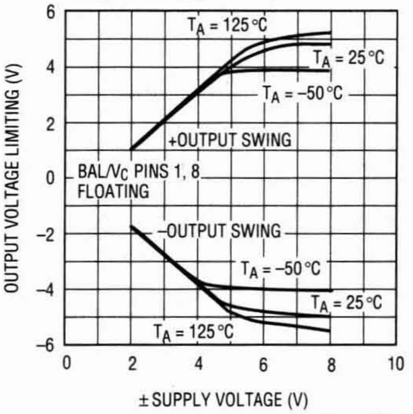
LT1194 • TPC12

Output Short Circuit Current vs Temperature



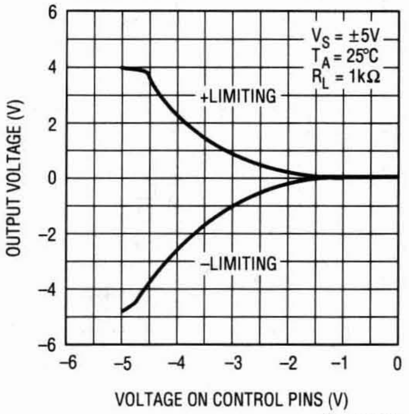
LT1194 • TPC13

Output Voltage Limiting vs Supply Voltage



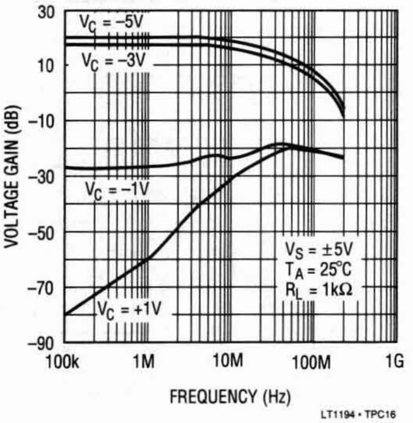
LT1194 • TPC14

Output Voltage vs Voltage On Control Pins



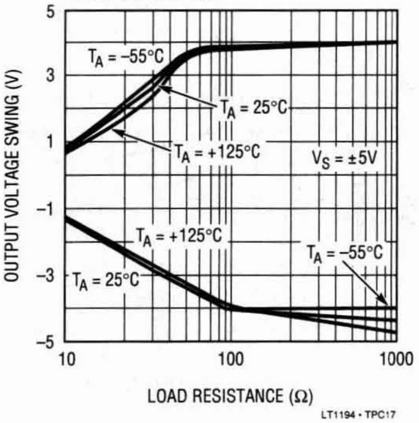
LT1194 • TPC15

Voltage Gain vs Frequency with Control Voltage



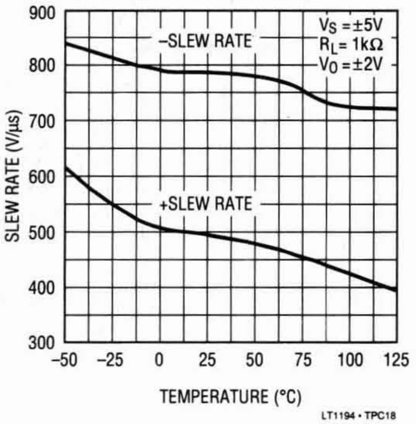
LT1194 • TPC16

Output Voltage Swing vs Load Resistance



LT1194 • TPC17

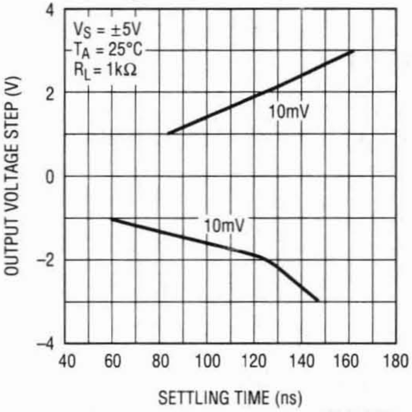
Slew Rate vs Temperature



LT1194 • TPC18

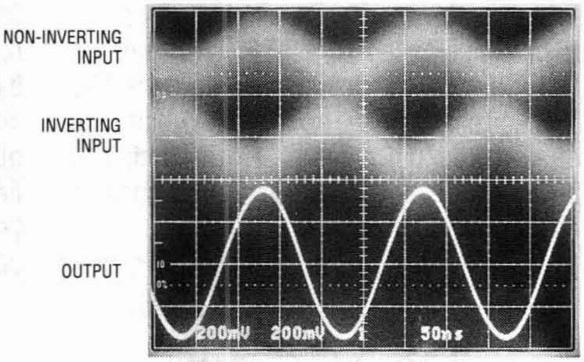
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Step vs Settling Time



LT1194 • TPC19

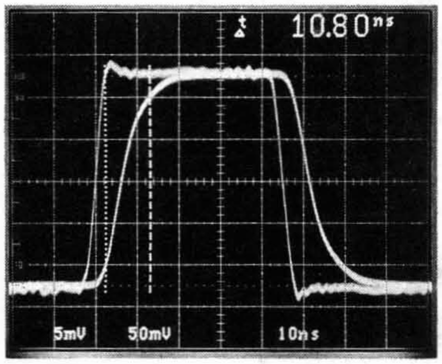
Common Mode Rejection



5MHz SINE WAVE RECOVERED FROM COMMON MODE NOISE

LT1194 • TPC22

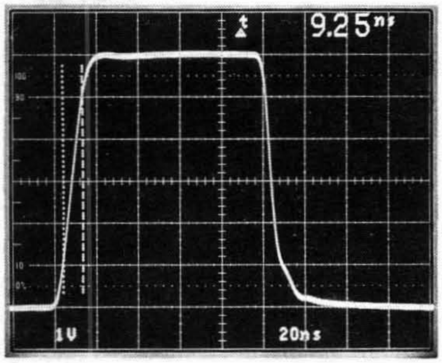
Small Signal Transient Response



RISE TIME = 10.8ns, PROPAGATION DELAY = 6ns

LT1194 • TPC21

Large Signal Transient Response



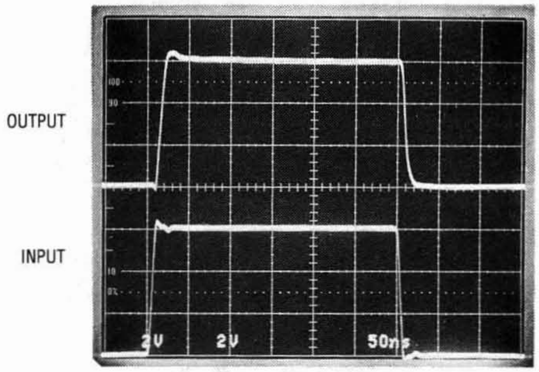
$R_L = 150\Omega$, + SR = 430V/μs, −SR = 500V/μs

LT1194 • TPC20

APPLICATIONS INFORMATION

The LT1194 is a video difference amplifier with a fixed gain of 10 (20dB). The amplifier has two uncommitted high input impedance (+) and (–) inputs which can be used either differentially or single-ended. The LT1194 includes a Limiting feature which allows the amplifier to reduce its output as a function of DC voltage on the BAL/V_C pins. The Limiting feature uses input differential pair limiting to prevent overload in subsequent stages. This technique allows extremely fast limiting action.

Input Limiting



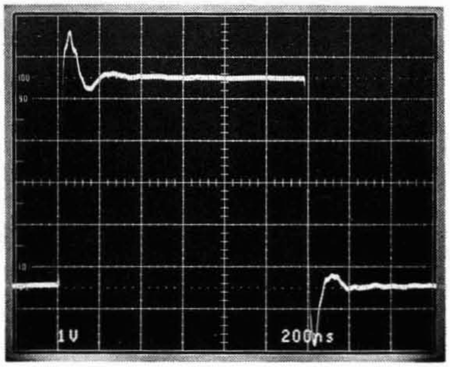
20dB INPUT OVERDRIVE V_C = –4.2V

LT1194 • TA06

Power Supply Bypassing

The LT1194 is quite tolerant of power supply bypassing. In some applications a 0.1μF ceramic disc capacitor placed 1/2 inch from the amplifier is all that is required. A scope photo of the amplifier output with no supply bypassing is used to demonstrate this bypassing tolerance, R_L = 1kΩ.

No Supply Bypass

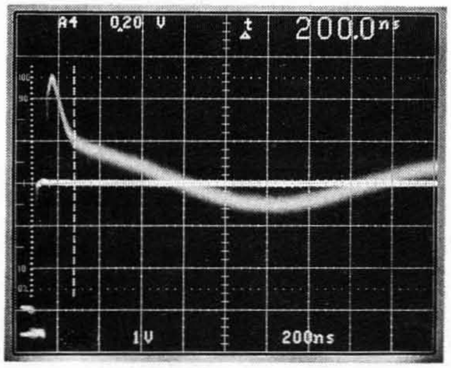


IN DEMO BOARD, R_L = 1kΩ

LT1194 • TA07

In many applications, and those requiring good settling time, it is important to use multiple bypass capacitors. A 0.1μF ceramic disc in parallel with a 4.7μF tantalum is recommended. Two oscilloscope photos with different bypass conditions are used to illustrate the settling time characteristics of the amplifier. Note that although the output waveform looks acceptable at 1V/div, when amplified to 10mV/div the settling time to 10mV is 200ns. The time drops to 162ns with multiple bypass capacitors, and does not exhibit the characteristic power supply ringing.

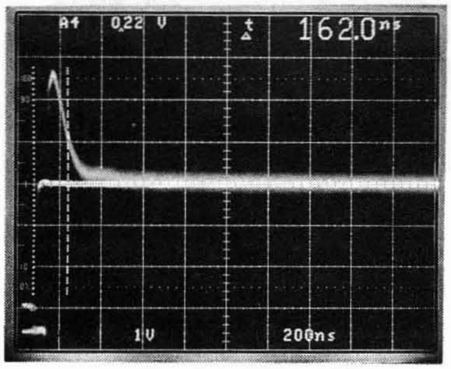
Settling Time Poor Bypass



SETTLING TIME TO 10mV,
SUPPLY BYPASS CAPACITORS = 0.1μF

LT1194 • TA08

Settling Time Good Bypass



SETTLING TIME TO 10mV, SUPPLY BYPASS
CAPACITORS = 0.1μF + 4.7μF TANTALUM

LT1194 • TA09

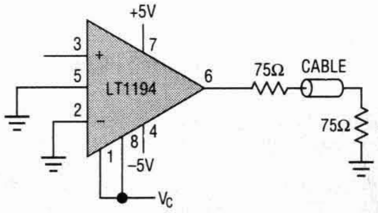
APPLICATIONS INFORMATION

Cable Terminations

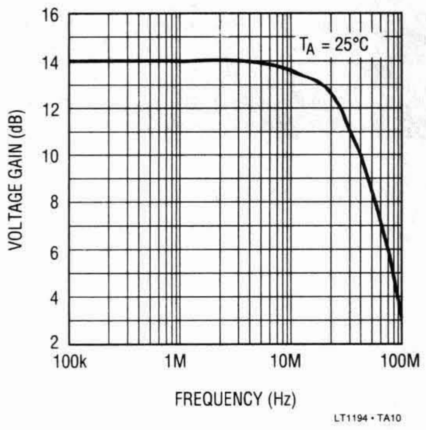
The LT1194 video difference amplifier has been optimized as a low cost cable driver. The ±50mA guaranteed output current enables the LT1194 to easily deliver 7.5Vp-p into 100Ω, while operating on ±5V supplies, or 2.6Vp-p on a single 5V supply.

When driving a cable it is important to terminate the cable to avoid unwanted reflections. This can be done in one of two ways: single termination or double termination. With single termination, the cable must be terminated at the receiving end (75Ω to ground) to absorb unwanted energy. The best performance can be obtained by double termination (75Ω in series with the output of the amplifier, and 75Ω to ground at the other end of the cable). This termination is preferred because reflected energy is absorbed at each end of the cable. When using the double termination technique it is important to note that the signal is attenuated by a factor of 2, or 6dB. For a cable driver with a gain of +5 (LT1194 gain of +10), the –3dB bandwidth is over 30MHz with no peaking.

Double Terminated Cable Driver



Voltage Gain vs Frequency



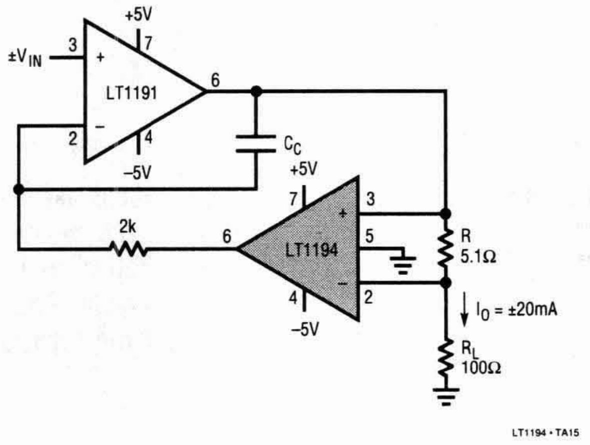
A Voltage Controlled Current Source

The LT1194 can be used to make a fast, precise, voltage controlled current source. The LT1194 high speed differential amplifier senses the current delivered to the load. The input signal V_{IN}, applied to the (+) input of the LT1191, will appear at the (–) input if the feedback loop is properly closed. In steady state the input signal appears at the output of the LT1194, and 1/10 of this signal is applied across the sense resistor. Thus the output current is simply:

$$I_O = \frac{V_{IN}}{R \times 10}$$

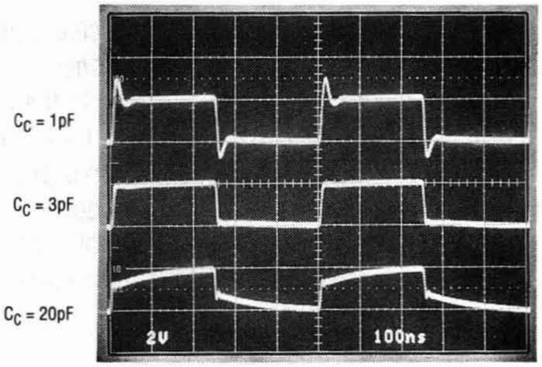
The compensation capacitor C_C forces the LT1191 to be the dominate pole for the loop, while the LT1194 is fast enough to be transparent in the feedback path. The ratio of the load resistor to the sense resistor should be approximately 10:1 or greater for easy compensation. For the example shown the load resistor is 100Ω, the sense resistor is 5.1Ω, and various loop compensation capacitors cause the output to exhibit an underdamped, critically, and overdamped response.

Voltage Controlled Current Source



APPLICATIONS INFORMATION

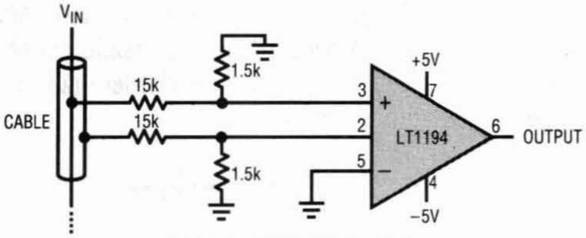
Output Current Response



±20mA CURRENT SOURCE WITH DIFFERENT COMPENSATION CAPACITORS

LT1194 • TA16

Differential Video Loop Thru Amplifier for Power Down Applications



1% RESISTOR WORST CASE CMRR = 22dB
TYPICALLY = 38dB

LT1194 • TA17

Murphy Circuits

There are several precautions the user should take when using the LT1194 in order to realize its full capability. Although the LT1194 can drive a 50pF capacitive load, isolating the capacitance with 10Ω can be helpful. Precautions primarily have to do with driving large capacitive loads.

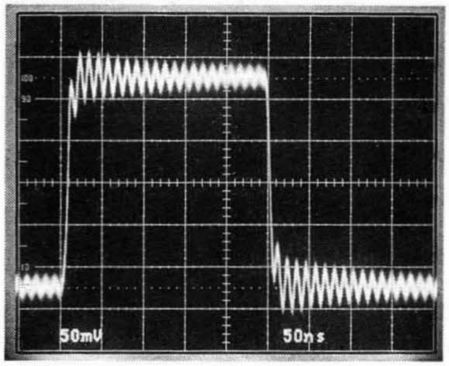
Other precautions include:

1. Use a ground plane (see Design Note 50, High Frequency Amplifier Evaluation Board).

2. Do not use high source impedances. The input capacitance of 2pF, and R_S = 10kΩ, for instance, will give an 8MHz −3dB bandwidth.

3. PC board socket may reduce stability.

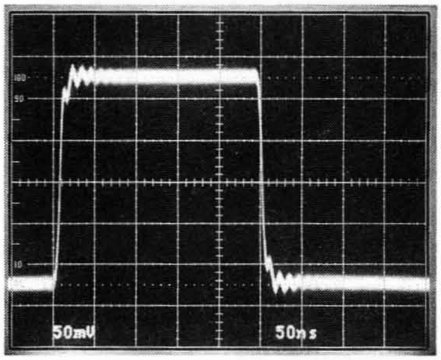
Driving Capacitive Load



LT1194 IN DEMO BOARD, C_L = 50pF

LT1194 • TA11

Driving Capacitive Load

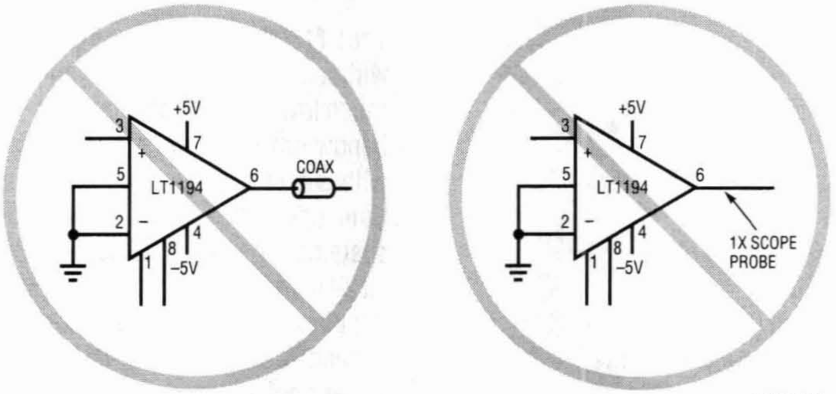


LT1194 IN DEMO BOARD, C_L = 50pF
WITH 10Ω ISOLATING RESISTOR

LT1194 • TA12

APPLICATIONS INFORMATION

Murphy Circuits

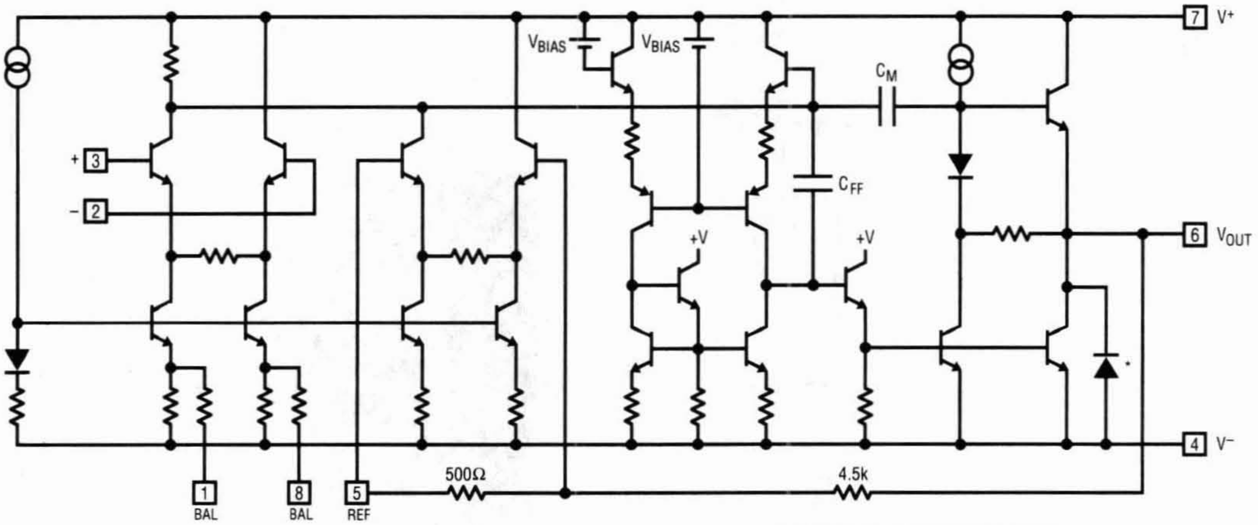

+5V
3
+
7
5
LT1194
6
COAX
2
−
4
8
1
−5V
+5V
3
+
7
5
LT1194
6
2
−
4
8
1
−5V
1X SCOPE
PROBE

LT1194 • TA13

An Unterminated Cable Is a Large Capacitive Load

A 1X Scope Probe Is a Large Capacitive Load

SIMPLIFIED SCHEMATIC


7 V+
V_BIAS
V_BIAS
C_M
+ 3
− 2
C_FF
+V
+V
6 V_OUT
*
4 V−
500Ω
4.5k
1 BAL
8 BAL
5 REF

* SUBSTRATE DIODE, DO NOT FORWARD BIAS

LT1194 • TA14

LINEAR TECHNOLOGY

LT1200

Low Power High Speed Operational Amplifier

FEATURES

- 1mA Supply Current
- 50V/µs Slew Rate
- 11MHz Gain Bandwidth
- Unity Gain Stable
- 430ns Settling Time to 0.1%, 10V Step
- 6V/mV DC Gain, $R_L = 2k\Omega$
- 1mV Maximum Input Offset Voltage
- 50nA Input Offset Current
- 500nA Input Bias Current
- ±12V Minimum Output Swing into 2kΩ
- Wide Supply Range ±2.5V to ±15V
- Drives All Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems

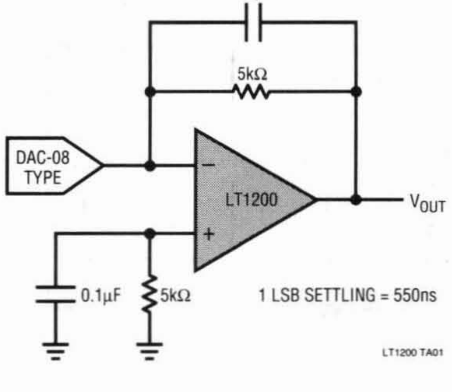
DESCRIPTION

The LT1200 is a low power high speed operational amplifier with excellent DC performance. The LT1200 features much lower supply current than devices with comparable bandwidth and slew rate. The circuit is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. The output is capable of driving a 2kΩ load to ±12V with ±15V supplies and a 500Ω load to ±3V on ±5V supplies. The circuit is also capable of driving large capacitive loads which makes it useful in buffer or cable driver applications.

The LT1200 is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

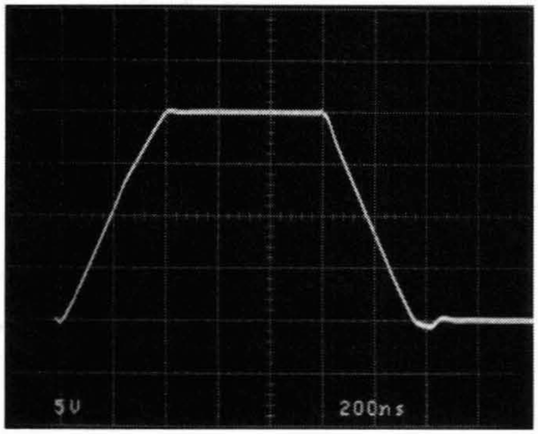
TYPICAL APPLICATION

DAC Current to Voltage Converter



1 LSB SETTLING = 550ns

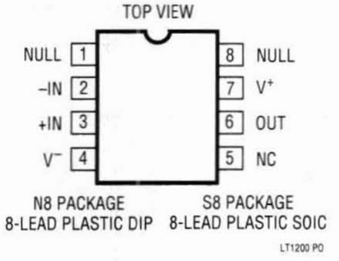
Inverter Pulse Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage .... ±6V
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range
LT1200C .... 0°C to 70°C
Maximum Junction Temperature
Plastic Package .... 150°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1200CN8 LT1200CS8
S8 PART MARKING
1200

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	1.0	mV
I_{OS}	Input Offset Current			50	100	nA
I_B	Input Bias Current			0.5	1.0	μA
e_n	Input Noise Voltage	f = 10kHz		30		nV/√Hz
i_n	Input Noise Current	f = 10kHz		0.7		pA/√Hz
R_{IN}	Input Resistance	$V_{CM} = \pm12V$	48	90		MΩ
	Input Resistance	Differential		500		kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range⁺		12	14		V
	Input Voltage Range⁻			−13	−12	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	80	90		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 5k\Omega$ $V_{OUT} = \pm10V$, $R_L = 2k\Omega$	4 3	8 6		V/mV V/mV
V_{OUT}	Output Swing	$R_L = 2k\Omega$	12.0	13.8		±V
I_{OUT}	Output Current	$V_{OUT} = \pm12V$	6	12		mA
SR	Slew Rate	$A_{VCL} = -2$, (Note 3)	30	50		V/μs
	Full Power Bandwidth	10V Peak, (Note 4)		0.8		MHz
GBW	Gain Bandwidth	f = 0.1MHz		11		MHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +1$, 10% to 90%, 0.1V		18		ns
	Overshoot	$A_{VCL} = +1$, 0.1V		25		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		18		ns
t_s	Settling Time	10V Step, 0.1%		430		ns
R_O	Output Resistance	$A_{VCL} = +1$, f = 0.1MHz		1.1		Ω
I_S	Supply Current			1	1.4	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		1.0	3.0	mV
I_{OS}	Input Offset Current			50	100	nA
I_B	Input Bias Current			0.5	1.0	µA
	Input Voltage Range$^+$		2.5	4		V
	Input Voltage Range$^-$			−3	−2.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 2.5V$	80	100		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 2.5V$, $R_L = 2k\Omega$ $V_{OUT} = \pm 2.5V$, $R_L = 1k\Omega$	2.5 2.0	5 4		V/mV V/mV
V_{OUT}	Output Voltage	$R_L = 500\Omega$	3.0	4.0		±V
I_{OUT}	Output Current	$V_{OUT} = \pm 3V$	6	12		mA
SR	Slew Rate	$A_{VCL} = -2$, (Note 3)	20	33		V/µs
	Full Power Bandwidth	3V Peak, (Note 4)		1.7		MHz
GBW	Gain Bandwidth	f = 0.1MHz		8.5		MHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +1$, 10%-90%, 0.1V		23		ns
	Overshoot	$A_{VCL} = +1$, 0.1V		20		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		23		ns
t_s	Settling Time	−2.5V to 2.5V, 0.1%		300		ns
I_S	Supply Current			1	1.4	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm 15V$, (Note 2) $V_S = \pm 5V$, (Note 2)		0.5 1.0	2.0 3.5	mV mV
	Input V_{OS} Drift			11		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ and $V_S = \pm 5V$		50	150	nA
I_B	Input Bias Current	$V_S = \pm 15V$ and $V_S = \pm 5V$		0.5	1.2	µA
CMRR	Common Mode Rejection Ratio	$V_S = \pm 15V$, $V_{CM} = \pm 12V$; $V_S = \pm 5V$, $V_{CM} = \pm 2.5V$	80	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	80	90		dB
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 5k\Omega$ $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$ $V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 2k\Omega$ $V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 1k\Omega$	3.5 2.5 2.0 1.6	8 6 5 4		V/mV V/mV V/mV V/mV
V_{OUT}	Output Swing	$V_S = \pm 15V$, $R_L = 2k\Omega$ $V_S = \pm 5V$, $R_L = 500\Omega$	12.0 3.0	13.8 4.0		±V ±V
I_{OUT}	Output Current	$V_S = \pm 15V$, $V_{OUT} = \pm 12V$ $V_S = \pm 5V$, $V_{OUT} = \pm 3V$	6 6	12 12		mA mA
SR	Slew Rate	$V_S = \pm 15V$, $A_{VCL} = -2$, (Note 3) $V_S = \pm 5V$, $A_{VCL} = -2$, (Note 3)	27 18	50 33		V/ms V/ms
I_S	Supply Current	$V_S = \pm 15V$ and $V_S = \pm 5V$		1	1.6	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

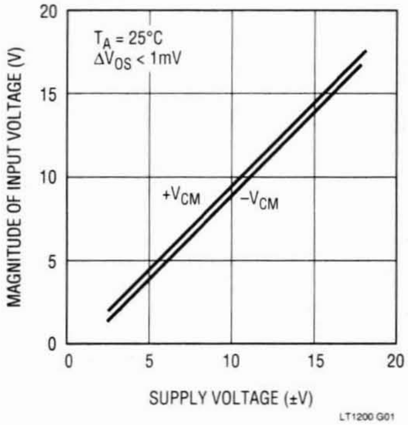
Note 2: Input offset voltage is tested with automated test equipment in <1 second.

Note 3: Slew rate is measured in a gain of −2 between ±10V on the output with ±6V on the input for ±15V supplies and ±2V on the output with ±1.75V on the input for ±5V supplies.

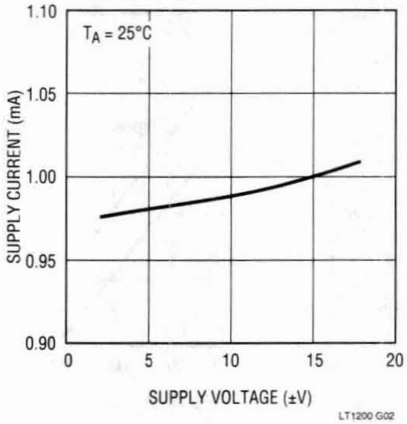
Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

TYPICAL PERFORMANCE CHARACTERISTICS

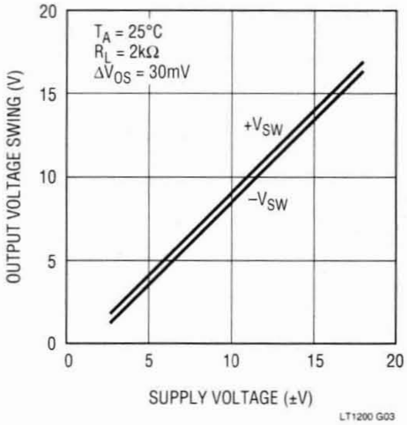
Input Common Mode Range vs Supply Voltage



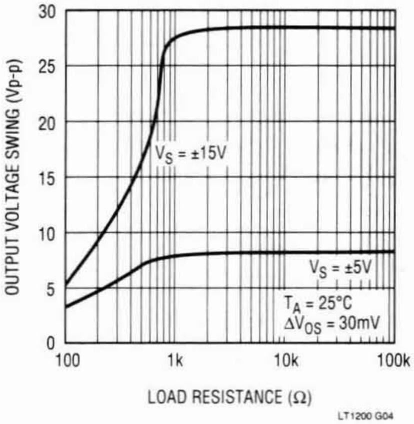
Supply Current vs Supply Voltage



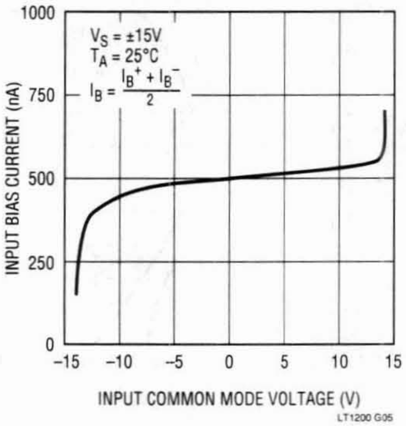
Output Voltage Swing vs Supply Voltage



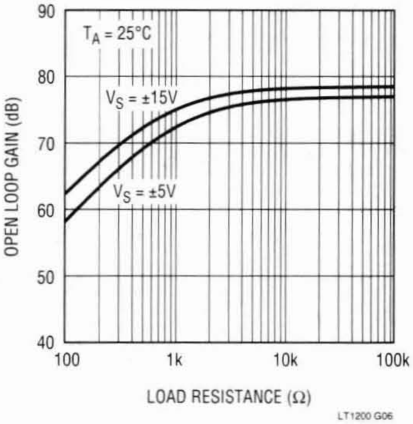
Output Voltage Swing vs Resistive Load



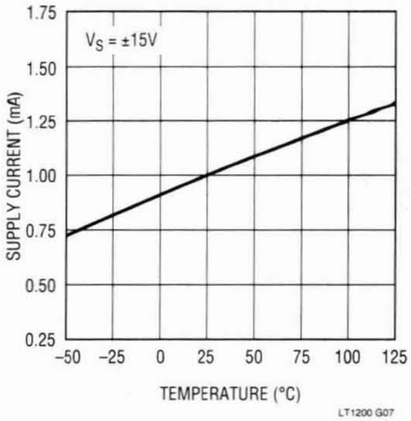
Input Bias Current vs Input Common Mode Voltage



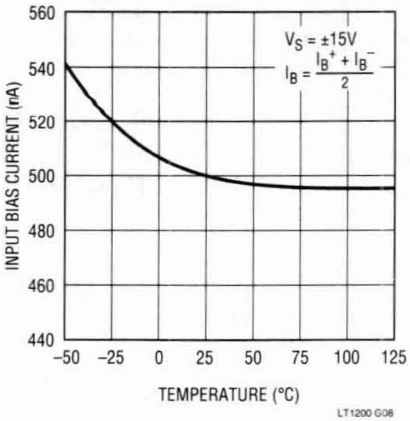
Open Loop Gain vs Resistive Load



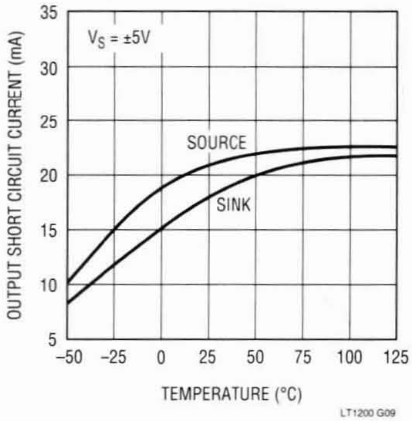
Supply Current vs Temperature



Input Bias Current vs Temperature

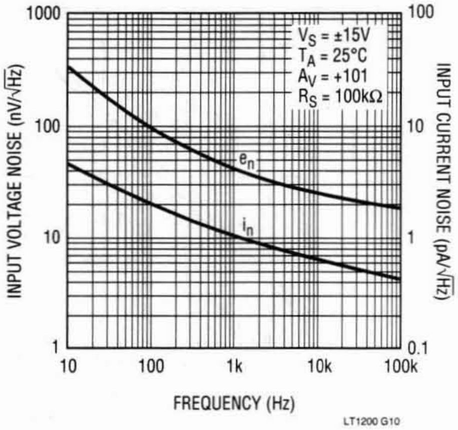


Output Short-Circuit Current vs Temperature

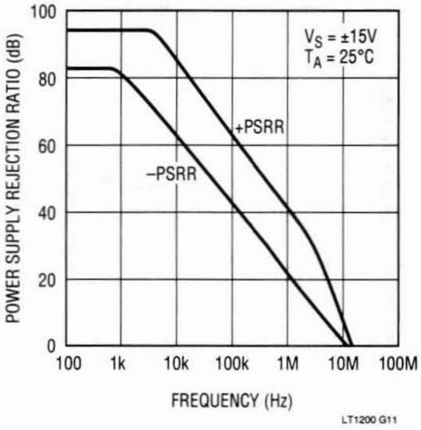


TYPICAL PERFORMANCE CHARACTERISTICS

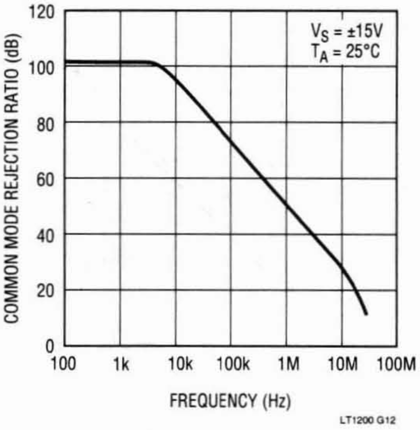
Input Noise Spectral Density



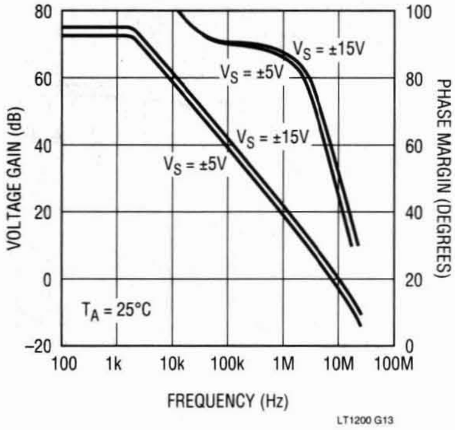
Power Supply Rejection Ratio vs Frequency



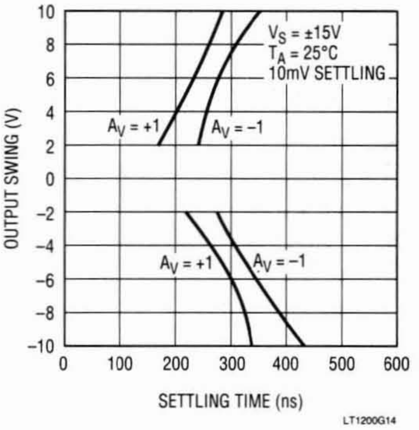
Common Mode Rejection Ratio vs Frequency



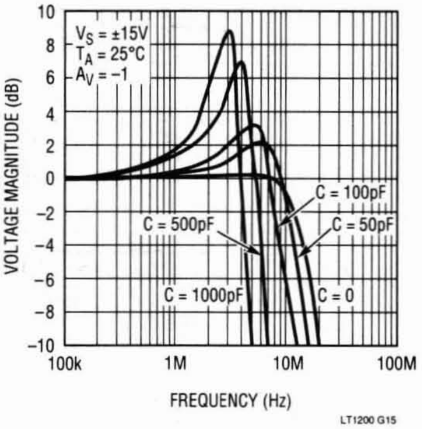
Voltage Gain and Phase vs Frequency



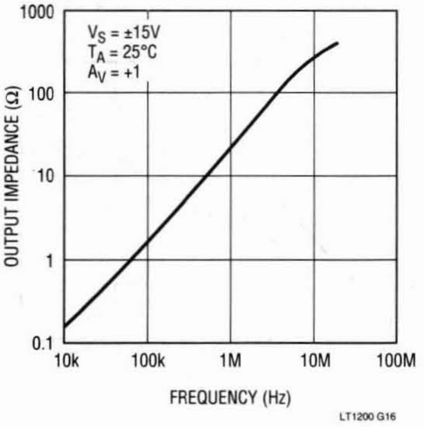
Output Swing vs Settling Time



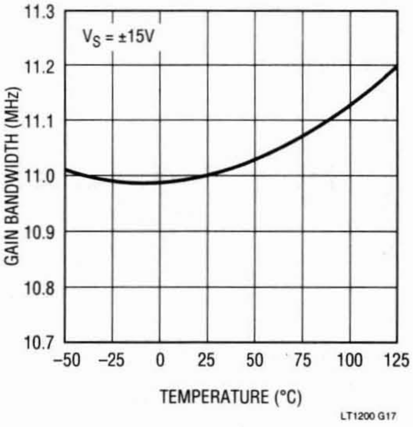
Frequency Response vs Capacitive Load



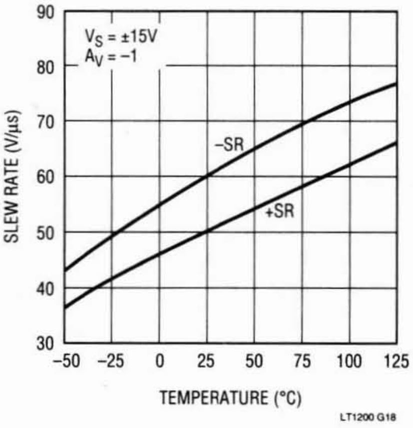
Closed Loop Output Impedance vs Frequency



Gain Bandwidth vs Temperature



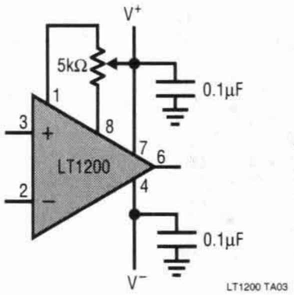
Slew Rate vs Temperature



APPLICATIONS INFORMATION

The LT1200 may be inserted directly into many applications, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1200 is shown below.

Offset Nulling



Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF), and use of low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low-profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking. If feedback resistors greater than 5kΩ are used, a parallel capacitor of value:

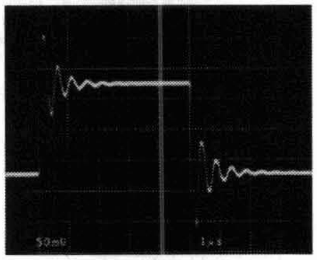
$$C_F \geq R_G \times \frac{C_{IN}}{R_F}$$

should be used to cancel the input pole and optimize dynamic performance. For unity gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

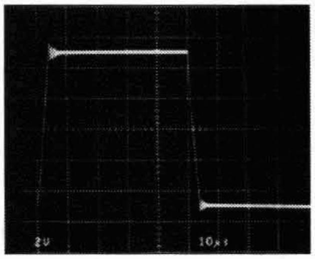
Capacitive Loading

The LT1200 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. The photo of the small signal response with 1000pF load shows 50% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited by the short-circuit current.

$A_V = -1$, $C_L = 1000pF$



$A_V = +1$, $C_L = 10,000pF$



DAC Current to Voltage Converter

The wide bandwidth, high slew rate and fast settling time of the LT1200 make it well suited for current to voltage conversion after current output D/A converters. A typical application is shown on page one with a DAC-08 type converter with a full-scale output of 2mA. A compensation capacitor is used across the feedback resistor to null the pole at the inverting input caused by the DAC output capacitance. The combination of the LT1200 and DAC settles to 40mV in 550ns for a 10V to 0V step and 450ns for a 0V to 10V step.

Input Considerations

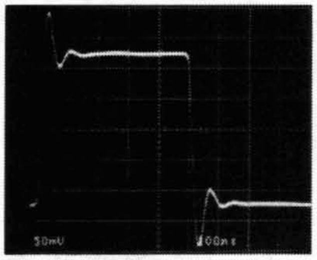
Resistors in series with the inputs are recommended for the LT1200 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

APPLICATIONS INFORMATION

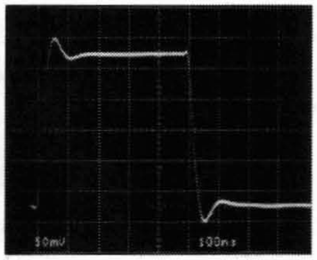
Transient Response

The LT1200 gain bandwidth is 11MHz when measured at 100kHz. The actual frequency response in unity gain is considerably higher than 11MHz due to peaking caused by a second pole beyond the unity gain crossover. This is reflected in the 45° phase margin and shows up as overshoot in the unity gain small signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of one response.

Small Signal, $A_V = +1$



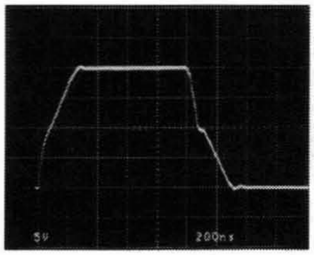
Small Signal, $A_V = -1$



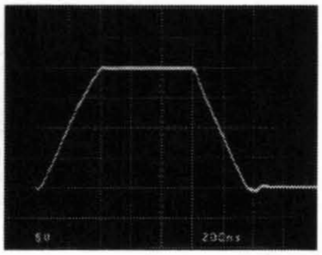
The large signal reponse in both inverting and noninverting gain shows symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge due to the rapid change in input common mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1200 so that the falling edge slew rate is enhanced which balances the noninverting slew rate.

The large signal, unity gain response shows the characteristic noninverting response of an op amp with an input slew rate much faster than that of the amplifier. In this case the input is slewing at greater than 1000V/μs.

Large Signal, $A_V = +1$



Large Signal, $A_V = -1$

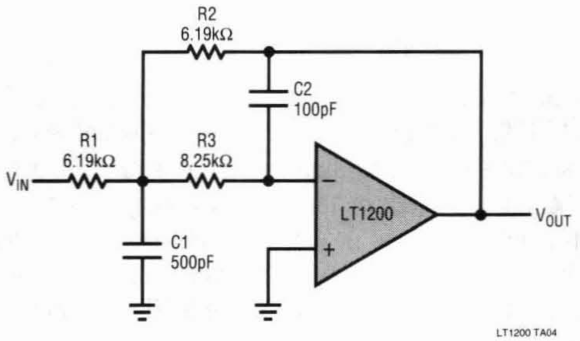


Low Voltage Operation

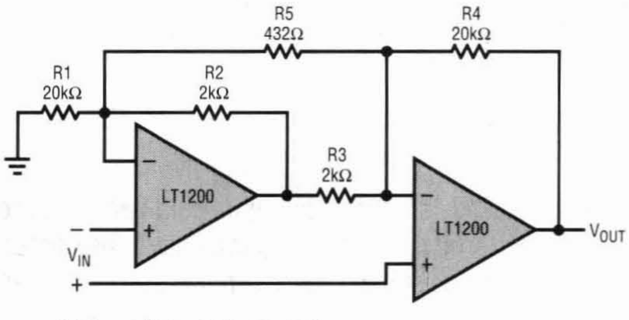
The LT1200 is functional at room temperature with only 3V of total supply voltage. Under this condition, however, the undistorted output swing is only $0.8V_{P-P}$. A more realistic condition is operation at ±2.5V supplies (or 5V and ground). Under these conditions at room temperature the typical input common mode range is +2.2V to −1.5V, and a 1MHz, $2.5V_{P-P}$ sine wave can be faithfully reproduced. With 5V total supply voltage the gain bandwidth is reduced to 6MHz and the slew rate is reduced to 20V/μs.

TYPICAL APPLICATIONS

100kHz, 2nd Order Butterworth Filter



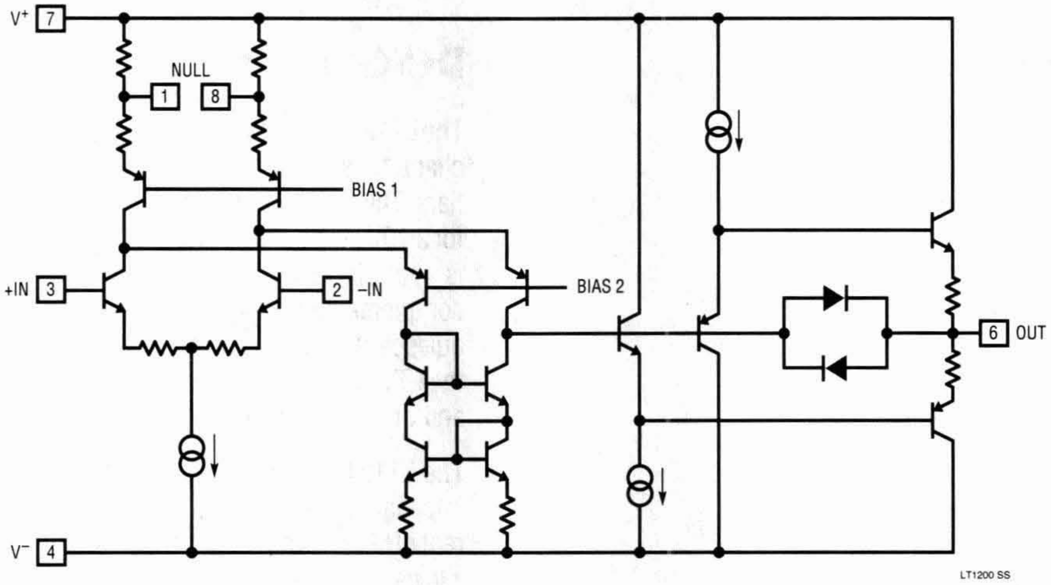
Two Op Amp Instrumentation Amplifier



$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION
BW = 125kHz

SIMPLIFIED SCHEMATIC


V+ 7
NULL
1
8
BIAS 1
+IN 3
2 –IN
BIAS 2
6 OUT
V– 4
LT1200 SS

LT1217

Low Power 10MHz Current Feedback Amplifier

FEATURES

- 1mA Quiescent Current
- 50mA Output Current (Minimum)
- 10MHz Bandwidth
- 500V/µs Slew Rate
- 280ns Settling Time to 0.1%
- Wide Supply Range, ±5V to ±15V
- 1mV Input Offset Voltage
- 100nA Input Bias Current
- 100MΩ Input Resistance

APPLICATIONS

- Video Amplifiers
- Buffers
- IF and RF Amplification
- Cable Drivers
- 8, 10, 12-Bit Data Acquisition Systems

DESCRIPTION

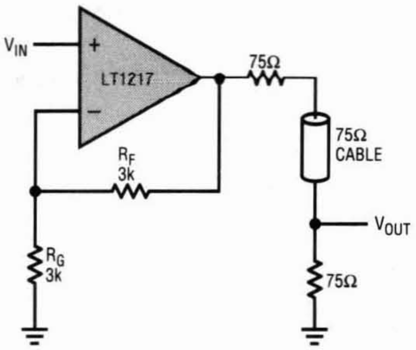
The LT1217 is a 10MHz current feedback amplifier with DC characteristics better than many voltage feedback amplifiers. This versatile amplifier is fast, 280ns settling to 0.1% for a 10V step thanks to its 500V/µs slew rate. The LT1217 is manufactured on Linear Technology's proprietary complementary bipolar process resulting in a low 1mA quiescent current. To reduce power dissipation further, the LT1217 can be turned off, eliminating the load current and dropping the supply current to 350µA.

The LT1217 is excellent for driving cables and other low impedance loads thanks to a minimum output drive current of 50mA. Operating on any supplies from ±5V to ±15V allows the LT1217 to be used in almost any system. Like other current feedback amplifiers, the LT1217 has high gain bandwidth at high gains. The bandwidth is over 1MHz at a gain of 100.

The LT1217 comes in the industry standard pinout and can upgrade the performance of many older products.

TYPICAL APPLICATION

Cable Driver

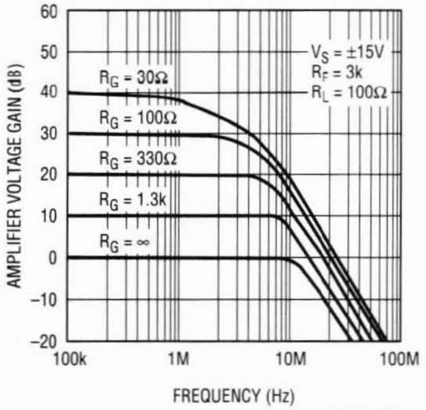


$A_V = 1 + \frac{R_F}{R_G}$

AT AMPLIFIER OUTPUT.
6dB LESS AT V_{OUT}.

LT1217 • TA01

Voltage Gain vs Frequency

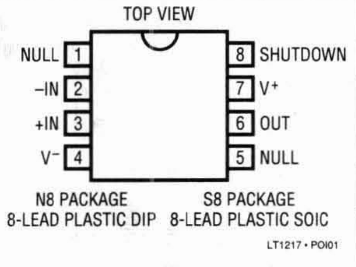


LT1217 • TA02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±18V
Input Current .... ±10mA
Input Voltage .... Equal to Supply Voltage
Output Short Circuit Duration (Note 1) .... Continuous
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Junction Temperature .... 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1217CN8 LT1217CS8
S8 PART MARKING
1217

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 0°C$ to $70°C$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$	●		±1	±3	mV
I_{IN+}	Non-Inverting Input Current	$V_{CM} = 0V$	●		±100	±500	nA
I_{IN-}	Inverting Input Current	$V_{CM} = 0V$	●		±100	±500	nA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1k, R_G = 10Ω			6.5		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz, R_F = 1k, R_G = 10Ω			0.7		pA/√Hz
R_{IN}	Input Resistance	$V_{IN} = \pm10V$	●	20	100		MΩ
C_{IN}	Input Capacitance				1.5		pF
	Input Voltage Range		●	±10	±12		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm10V$	●	60	66		dB
	Inverting Input Current Common Mode Rejection	$V_{CM} = \pm10V$	●		5	20	nA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	●	68	76		dB
	Non-Inverting Input Current Power Supply Rejection	$V_S = \pm4.5V$ to $\pm18V$	●		2	20	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm4.5V$ to $\pm18V$	●		10	50	nA/V
A_V	Large Signal Voltage Gain	R_{LOAD} = 2k, $V_{OUT} = \pm10V$ R_{LOAD} = 400Ω, $V_{OUT} = \pm10V$	● ●	90 70	105		dB dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN-}$	R_{LOAD} = 2k, $V_{OUT} = \pm10V$ R_{LOAD} = 400Ω, $V_{OUT} = \pm10V$	● ●	5 1.5	45		MΩ MΩ
V_{OUT}	Output Swing	R_{LOAD} = 2k R_{LOAD} = 200Ω	● ●	±12 ±10	±13		V V
I_{OUT}	Output Current	R_{LOAD} = 0Ω	●	50	100		mA
SR	Slew Rate (Note 2, 3)	R_F = 3k, R_G = 3k	●	100	500		V/µs
BW	Bandwidth	R_F = 3k, R_G = 3k, V_{OUT} = 100mV			10		MHz
t_r	Rise Time, Fall Time (Note 3)	R_F = 3k, R_G = 3k, V_{OUT} = 1V	●		30	40	ns
t_{PD}	Propagation Delay	R_F = 3k, R_G = 3k, V_{OUT} = 1V			25		ns
	Overshoot	R_F = 3k, R_G = 3k, V_{OUT} = 1V			5		%
t_s	Settling Time, 0.1%	R_F = 3k, R_G = 3k, V_{OUT} = 10V			280		ns
I_S	Supply Current	V_{IN} = 0V	●		1	2	mA
	Supply Current, Shutdown	Pin 8 Current = 50µA	●		350	1000	µA

The ● denotes specifications which apply over the operating temperature range.

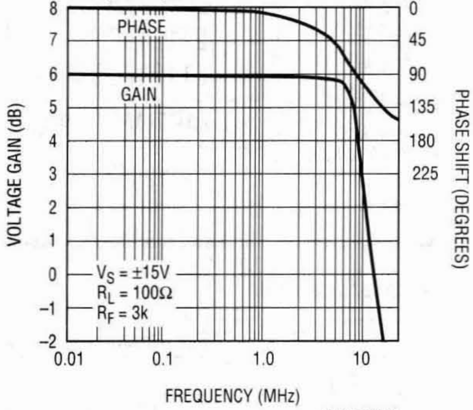
Note 1: A heat sink may be required.

Note 2: Non-Inverting operation, $V_{OUT} = \pm10V$, measured at ±5V.

Note 3: AC parameters are 100% tested on the plastic DIP packaged parts (N suffix), and are sample tested on every lot of the SO packaged parts (S suffix).

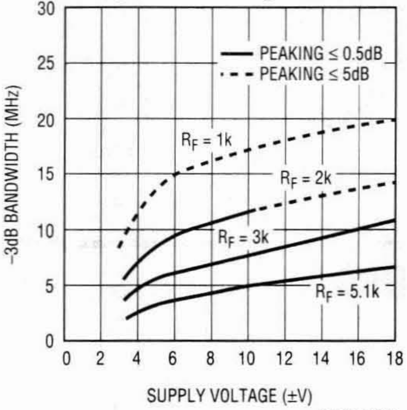
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain and Phase vs Frequency, Gain = 6dB



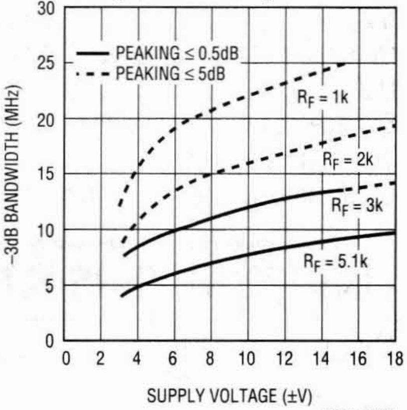
LT1217 • TPC01

–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 100Ω



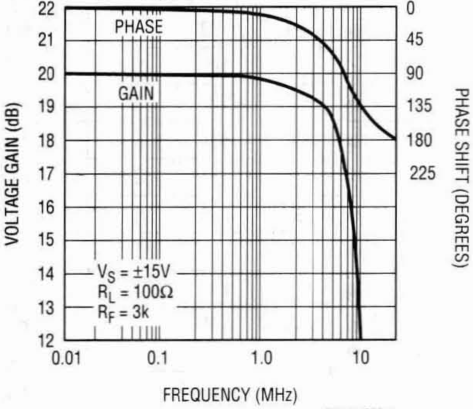
LT1217 • TPC02

–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 1kΩ



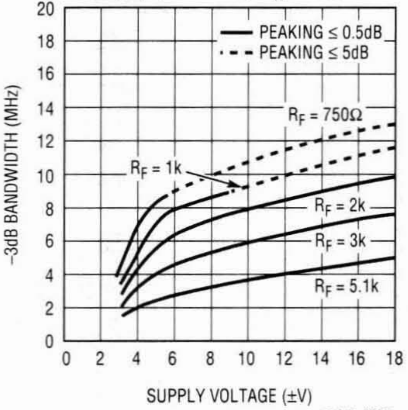
LT1217 • TPC03

Voltage Gain and Phase vs Frequency, Gain = 20dB



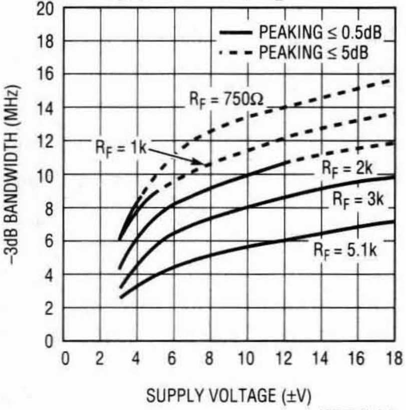
LT1217 • TPC04

–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 100Ω



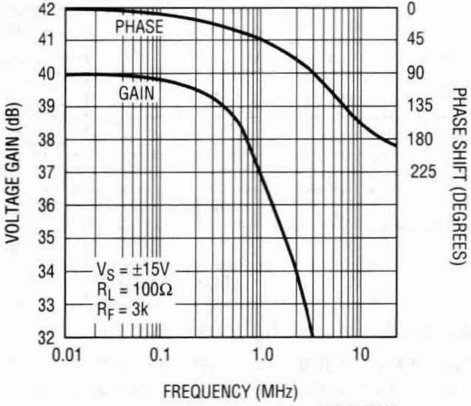
LT1217 • TPC05

–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 1kΩ



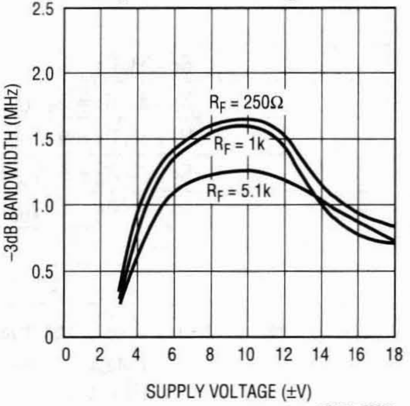
LT1217 • TPC06

Voltage Gain and Phase vs Frequency, Gain = 40dB



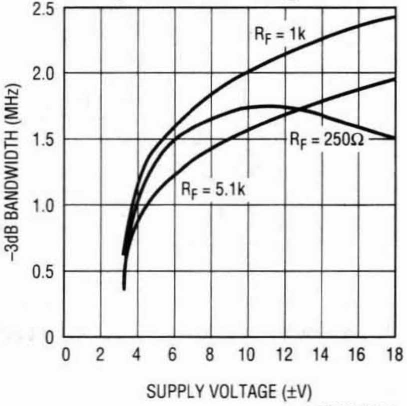
LT1217 • TPC07

–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 100Ω



LT1217 • TPC08

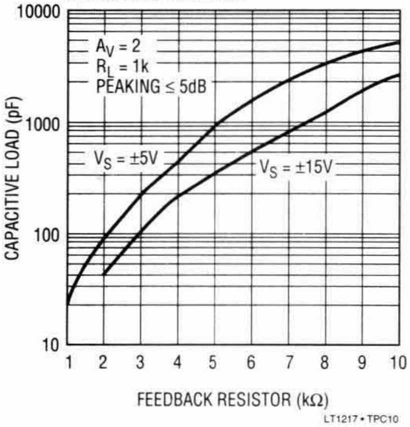
–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 1kΩ



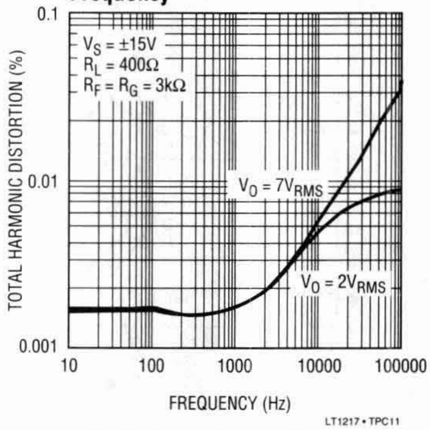
LT1217 • TPC09

TYPICAL PERFORMANCE CHARACTERISTICS

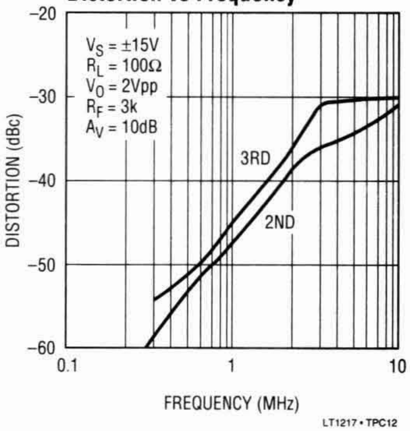
Maximum Capacitive Load vs Feedback Resistor



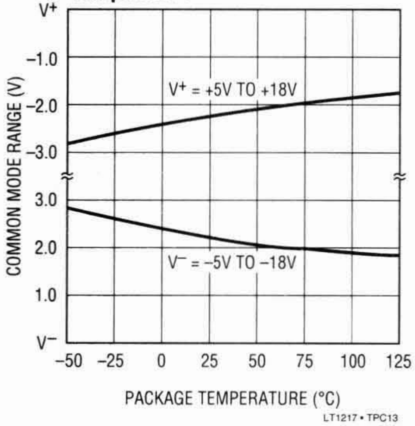
Total Harmonic Distortion vs Frequency



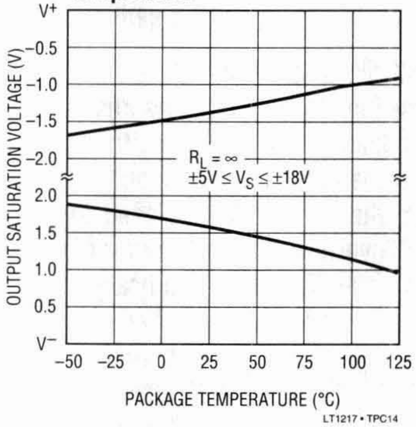
2nd and 3rd Harmonic Distortion vs Frequency



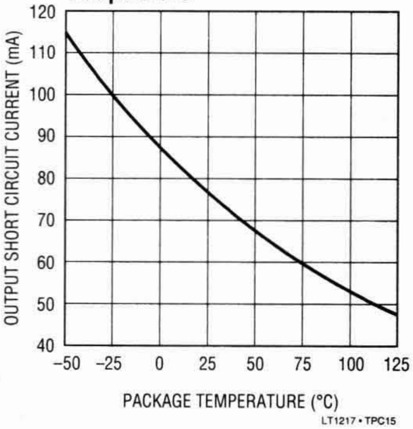
Input Common Mode Limit vs Temperature



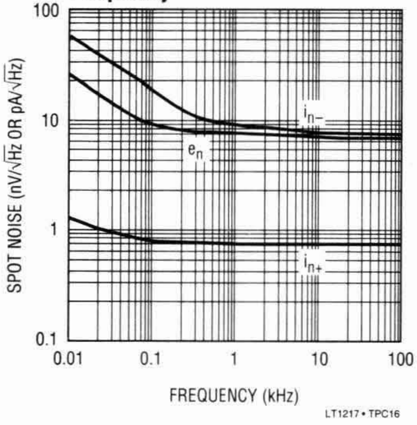
Output Saturation Voltage vs Temperature



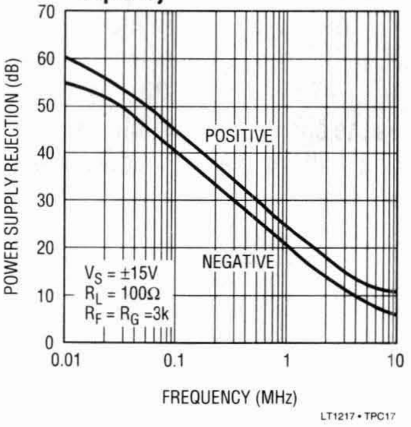
Output Short Circuit Current vs Temperature



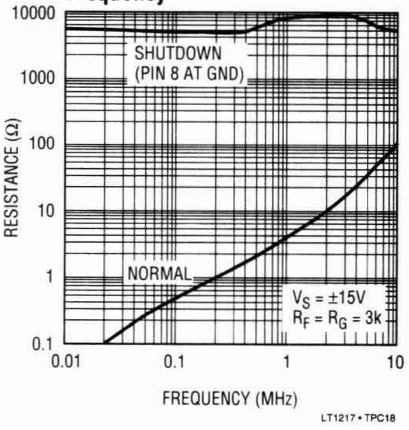
Spot Noise Voltage and Current vs Frequency



Power Supply Rejection vs Frequency

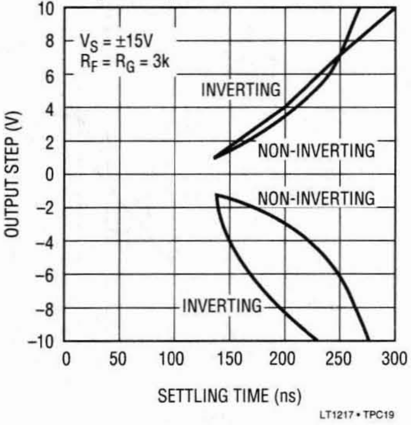


Output Impedance vs Frequency

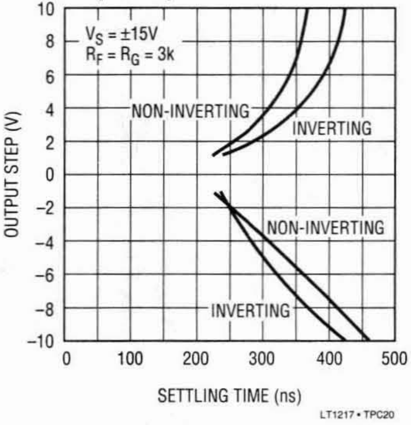


TYPICAL PERFORMANCE CHARACTERISTICS

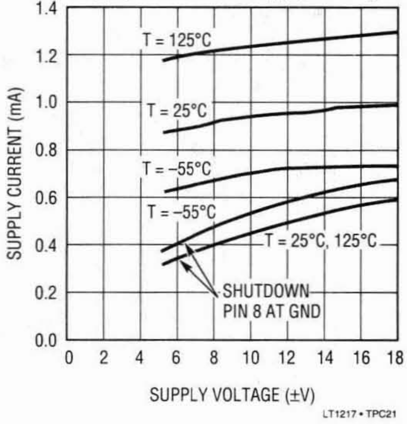
Settling Time to 10mV vs Output Step



Settling Time to 1mV vs Output Step



Supply Current vs Supply Voltage



APPLICATIONS INFORMATION

Current Feedback Basics

The small signal bandwidth of the LT1217, like all current feedback amplifiers, isn't a straight inverse function of the closed loop gain. This is because the feedback resistors determine the amount of current driving the amplifier's internal compensation capacitor. In fact, the amplifier's feedback resistor (R_F) from output to inverting input works with internal junction capacitances of the LT1217 to set the closed loop bandwidth.

Even though the gain set resistor (R_G) from inverting input to ground works with R_F to set the voltage gain just like it does in a voltage feedback op amp, the closed loop bandwidth does not change. This is because the equivalent gain bandwidth product of the current feedback amplifier is set by the Thevenin equivalent resistance at the inverting input and the internal compensation capacitor. By keeping R_F constant and changing the gain with R_G, the Thevenin resistance changes by the same amount as the change in gain. As a result, the net closed loop bandwidth of the LT1217 remains the same for various closed loop gains.

The curve on the first page shows the LT1217 voltage gain versus frequency while driving 100Ω, for five gain settings from 1 to 100. The feedback resistor is a constant 3k and the gain resistor is varied from infinity to 30Ω. Second order effects reduce the bandwidth somewhat at the higher gain settings.

Feedback Resistor Selection

The small signal bandwidth of the LT1217 is set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed loop gain and load resistor. The characteristic curves of bandwidth versus supply voltage are done with a heavy load (100Ω) and a light load (1kΩ) to show the effect of loading. These graphs also show the family of curves that result from various values of the feedback resistor. These curves use a solid line when the response has less than 0.5dB of peaking and a dashed line when the response has 0.5dB to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

At a gain of two, on ±15V supplies with a 3kΩ feedback resistor, the bandwidth into a light load is 13.5MHz with a little peaking, but into a heavy load the bandwidth is 10MHz with no peaking. At very high closed loop gains, the bandwidth is limited by the gain bandwidth product of about 100MHz. The curves show that the bandwidth at a closed loop gain of 100 is about 1MHz.

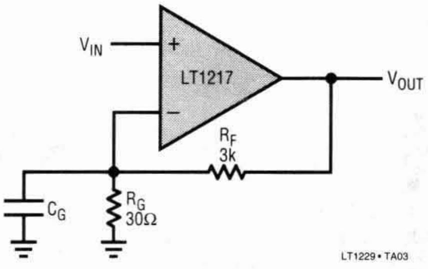
Capacitance on the Inverting Input

Current feedback amplifiers want resistive feedback from the output to the inverting input for stable operation. Take

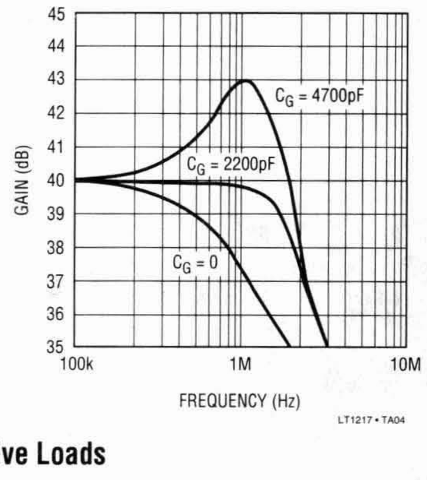
APPLICATIONS INFORMATION

care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response), but it does not degrade the stability of the amplifier. The amount of capacitance that is necessary to cause peaking is a function of the closed loop gain taken.

The higher the gain, the more capacitance is required to cause peaking. We can add capacitance from the inverting input to ground to increase the bandwidth in high gain applications. For example, in this gain of 100 application, the bandwidth can be increased from 1MHz to 2MHz by adding a 2200pF capacitor.



Boosting Bandwidth of High Gain Amplifier with Capacitance on Inverting Input



Capacitive Loads

The LT1217 can be isolated from capacitive loads with a small resistor (10Ω to 20Ω) or it can drive the capacitive load directly if the feedback resistor is increased. Both techniques lower the amplifier's bandwidth about the same amount. The advantage of resistive isolation is that the bandwidth is only reduced when the capacitive load is present. The disadvantage of resistor isolation is that resistive loading causes gain errors. Because the DC accuracy is not degraded with resistive loading, the desired way of driving capacitive loads, such as flash converters, is to increase the feedback resistor. The Maximum Capacitive Load versus Feedback Resistor curve shows the value of feedback resistor and capacitive load that gives 5dB of peaking. For less peaking, use a larger feedback resistor.

Power Supplies

The LT1217 may be operated with single or split supplies as low as ±4.5V (9V total) to as high as ±18V (36V total). It is not necessary to use equal value split supplies, however, the offset voltage will degrade about 350μV per volt of mismatch. The internal compensation capacitor decreases with increasing supply voltage. The –3dB Bandwidth versus Supply Voltage curves show how this affects the bandwidth for various feedback resistors. Generally, the bandwidth at ±5V supplies is about half the value it is at ±15V supplies for a given feedback resistor.

The LT1217 is very stable even with minimal supply bypassing, however, the transient response will suffer if the supply rings. It is recommended for good slew rate and settling time that 4.7μF tantalum capacitors be placed within 0.5 inches of the supply pins.

Input Range

The non-inverting input of the LT1217 looks like a 100MΩ resistor in parallel with a 3pF capacitor until the common mode range is exceeded. The input impedance drops somewhat and the input current rises to about 10μA when the input comes too close to the supplies. Eventually, when the input exceeds the supply by one diode drop, the base collector junction of the input transistor forward biases and the input current rises dramatically. The input current should be limited to 10mA when exceeding the supplies. The amplifier will recover quickly when the input is returned to its normal common mode range unless the input was over 500mV beyond the supplies, then it will take an extra 100ns.

APPLICATIONS INFORMATION

Offset Adjust

Output offset voltage is equal to the input offset voltage times the gain plus the inverting input bias current times the feedback resistor. The LT1217 output offset voltage can be nulled by pulling approximately 30µA from pin 1 or 5. The easy way to do this is to use a 100kΩ pot between pin 1 and 5 with a 430kΩ resistor from the wiper to ground for 15V supply applications. Use a 110k resistor when operating on a 5V supply.

Shutdown

Pin 8 activates a shutdown control function. Pulling more than 50µA from pin 8 drops the supply current to less than 350µA, and puts the output into a high impedance state. The easy way to force shutdown is to ground pin 8, using an open collector (drain) logic stage. An internal resistor limits current, allowing direct interfacing with no additional parts. When pin 8 is open, the LT1217 operates normally.

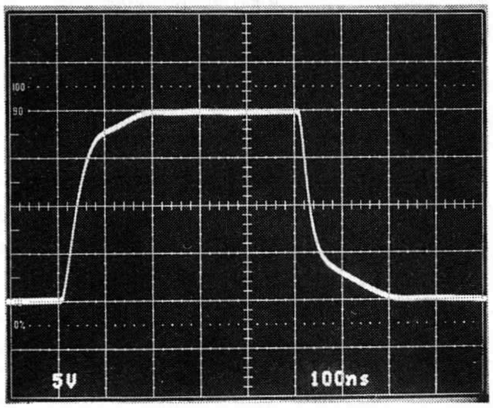
Slew Rate

The slew rate of a current feedback amplifier is not independent of the amplifier gain configuration the way it is in a traditional op amp. This is because the input stage and the output stage both have slew rate limitations. Inverting amplifiers do not slew the input and are therefore limited only by the output stage. High gain, non-inverting amplifiers are similar. The input stage slew rate of the LT1217 is about 50V/µs before it becomes non-linear and is enhanced by the normally reverse biased emitters on the input transistors. The output slew rate depends on the size of the feedback resistors. The output slew rate is about 850V/µs with a 3k feedback resistor and drops proportionally for larger values. The photos show the LT1217 with a 20V peak-to-peak output swing for three different gain configurations.

Settling Time

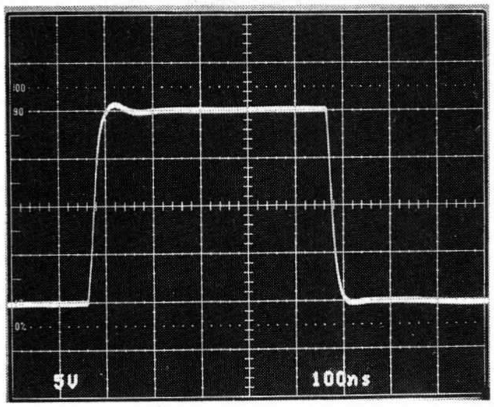
The characteristic curves show that the LT1217 settles to within 10mV of final value in less than 300ns for any output step up to 10V. Settling to 1mV of final value takes less than 500ns.

Large Signal Response, $A_V = 2$, $R_F = R_G = 3k$, Slew Rate $\simeq$ 500V/µs



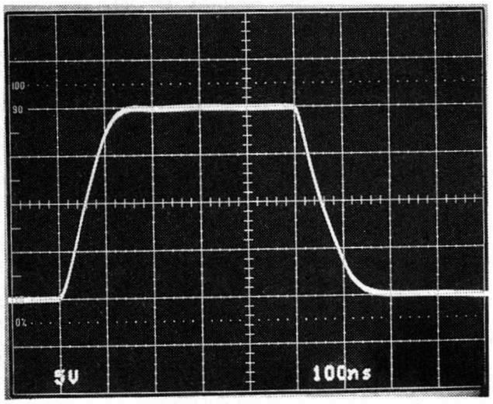
LT1217 • TA05

Large Signal Response, $A_V = -2$, $R_F = 3k$, $R_G = 1.5k$, Slew Rate $\simeq$ 850V/µs



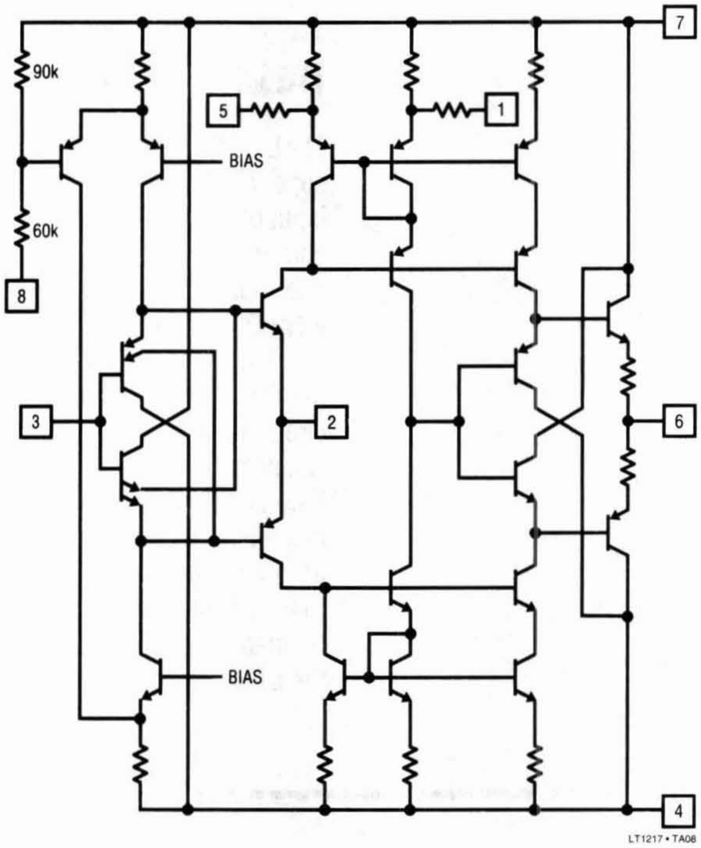
LT1217 • TA06

Large Signal Response, $A_V = 10$, $R_F = 3k$, $R_G = 330\Omega$, Slew Rate $\simeq$ 150V/µs



LT1217 • TA07

SIMPLIFIED SCHEMATIC


7
90k
5
1
BIAS
60k
8
3
2
6
BIAS
4
LT1217 • TA08

LT1220

Very High Speed Operational Amplifier

FEATURES

- 45MHz Gain Bandwidth
- 250V/μs Slew Rate
- 20,000 Minimum DC Gain
- 1mV Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- 300nA Maximum Input Offset Current
- 90ns Settling Time to 0.1%
- Drives All Capacitive Loads

APPLICATIONS

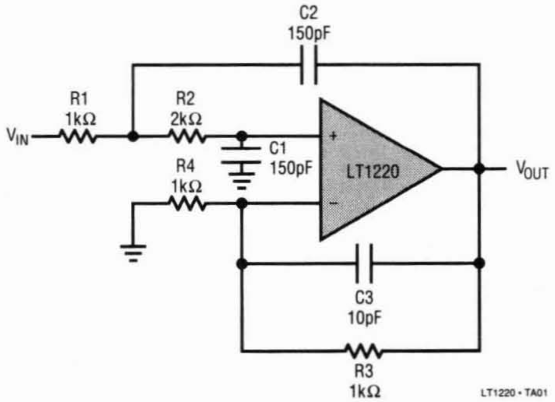
- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- 8, 10,12-Bit Data Acquisition Systems

DESCRIPTION

The LT1220 is a very high speed operational amplifier with superior DC performance. The LT1220 features reduced input offset voltage, lower input bias currents, and higher gain than devices with comparable bandwidth and slew rate. The circuit is a single gain stage that includes proprietary DC gain enhancement circuitry to obtain precision with high speed. The high gain and fast settling time make the circuit an ideal choice for data acquisition systems. The circuit is also capable of driving large capacitive loads which makes it useful in buffer or cable driver applications. This is the first of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing. For gains of four or greater the decompensated LT1221 can be used for greater bandwidth. Likewise, for gains of 10 or greater the LT1222 can be used.

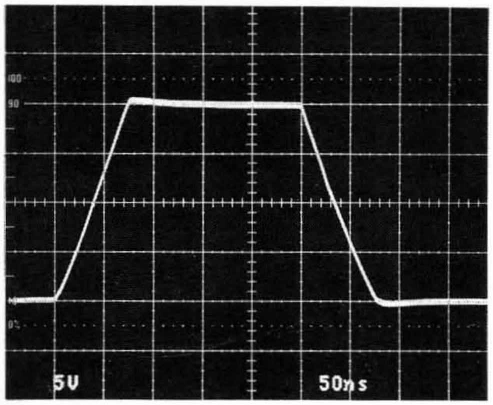
TYPICAL APPLICATION

2nd Order Low Pass Filter
f_0 = 700kHz



LT1220 • TA01

Inverter Pulse Response

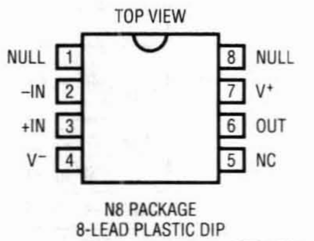


LTC1220 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Current .... ±25mA
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range
LT1220C .... 0°C to 70°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW NULL 1 –IN 2 +IN 3 V⁻ 4 8 NULL 7 V⁺ 6 OUT 5 NC N8 PACKAGE 8-LEAD PLASTIC DIP LT1220 • POI01	LT1220CN8

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $T_A = 25°C$, $R_L = 1k\Omega$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	1.0	mV
I_{OS}	Input Offset Current			100	300	nA
I_B	Input Bias Current			100	300	nA
e_n	Input Noise Voltage	f = 10kHz		17		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz		3		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$	24	45		MΩ
	Input Resistance	Differential		150		kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range +		12	14		V
	Input Voltage Range –			−13	−12	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$	92	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	86	94		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	20	50		V/mV
$V_{OUT}+$	Output Swing+	$R_L = 500\Omega$	12.0	13.0		V
$V_{OUT}-$	Output Swing–	$R_L = 500\Omega$		−13.0	−12.0	V
I_{OUT}	Output Current	$V_{OUT} = \pm 12V$	24	40		mA
SR	Slew Rate	$A_{VCL} = -2$, (Note 3)	200	250		V/μs
	Full Power Bandwidth	10V Peak, (Note 4)		4		MHz
GBW	Gain Bandwidth	f = 1MHz		45		MHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +1$, 10% to 90%, 0.1V		4		ns
	Overshoot	$A_{VCL} = +1$, 0.1V		25		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		4		ns
t_s	Settling Time	10V Step, 0.1%		90		ns
	Differential Gain	f = 3.58MHz		1.7		%
	Differential Phase	f = 3.58MHz		2.9		Deg.
R_O	Output Resistance	$A_{VCL} = +1$, f = 1MHz		2.6		Ω
I_S	Supply Current			8	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $0°C \le T_A \le 70°C$, $R_L = 1k\Omega$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	3.5	mV
	Input V_{OS} Drift			20		µV/°C
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			100	400	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	92	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	86	94		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	20	50		V/mV
$V_{OUT}+$	Output Swing+	$R_L = 500\Omega$	12.0	13.0		V
$V_{OUT}-$	Output Swing−	$R_L = 500\Omega$		−13.0	−12.0	V
I_{OUT}	Output Current	$V_{OUT} = \pm12V$	24	40		mA
SR	Slew Rate	$A_{VCL} = -2$, (Note 3)	180	250		V/µs
I_S	Supply Current			8	11	mA

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

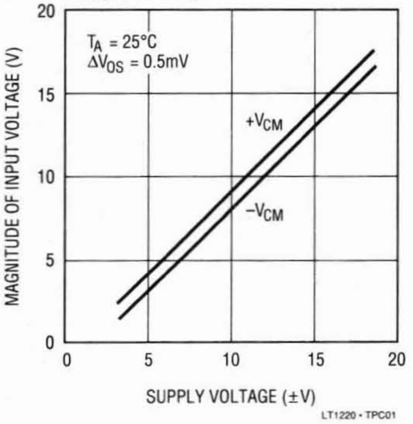
Note 2: Input offset voltage is tested with automatic test equipment in <1 second.

Note 3: Slew rate is measured between ±10V on the output with ±6V on the input and a gain of −2.

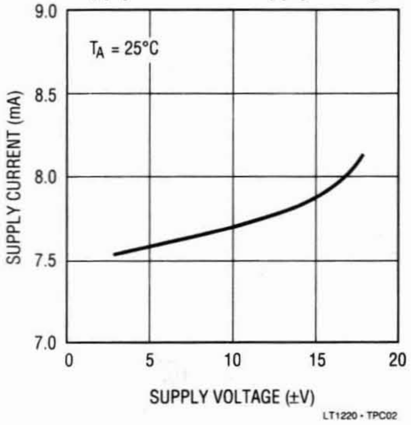
Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

TYPICAL PERFORMANCE CHARACTERISTICS

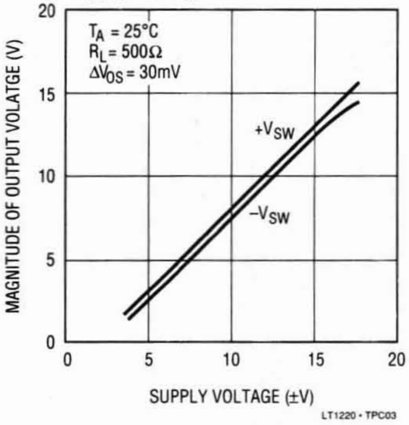
Input Common Mode Range vs Supply Voltage



Supply Current vs Supply Voltage

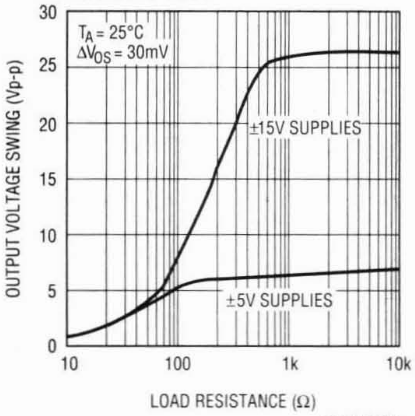


Output Voltage Swing vs Supply Voltage



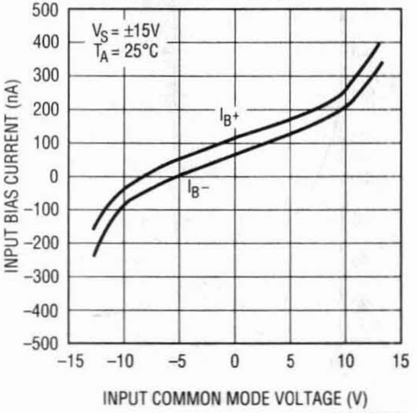
TYPICAL PERFORMANCE CHARACTERISTICS

Output Voltage Swing vs Resistive Load



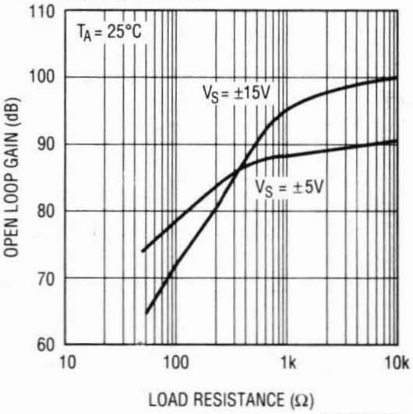
LT1220 • TPC04

Input Bias Current vs Input Common Mode Voltage



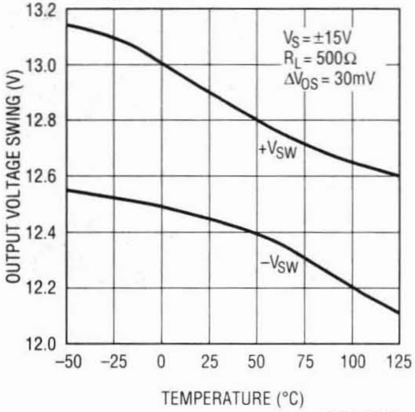
LT1220 • TPC05

Open Loop Gain vs Resistive Load



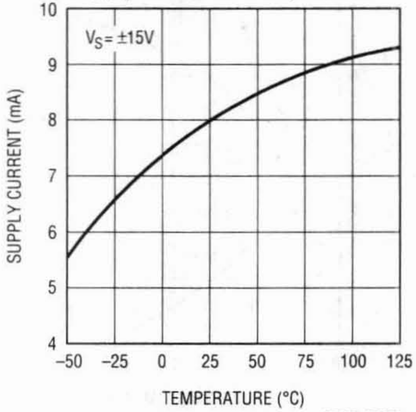
LT1220 • TPC06

Output Voltage Swing vs Temperature



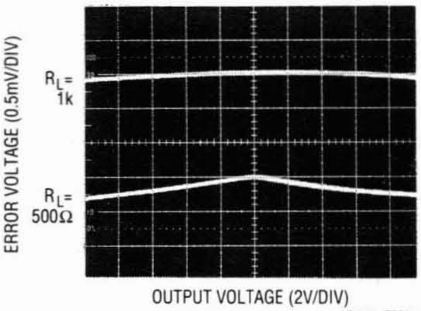
LT1220 • TPC07

Supply Current vs Temperature



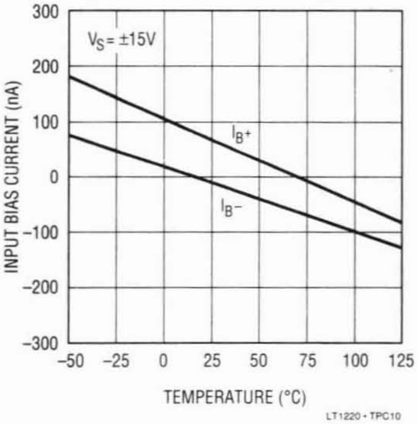
LT1220 • TPC08

Gain



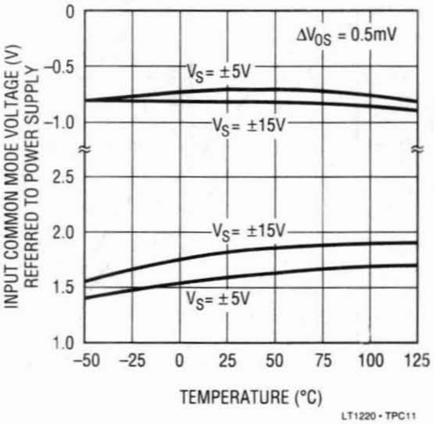
LT1220 • TPC09

Input Bias Current vs Temperature



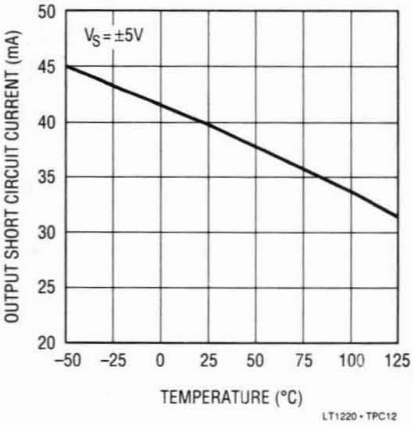
LT1220 • TPC10

Input Common Mode Voltage vs Temperature



LT1220 • TPC11

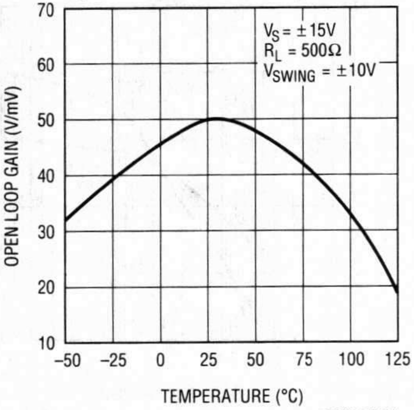
Output Short Circuit Current vs Temperature



LT1220 • TPC12

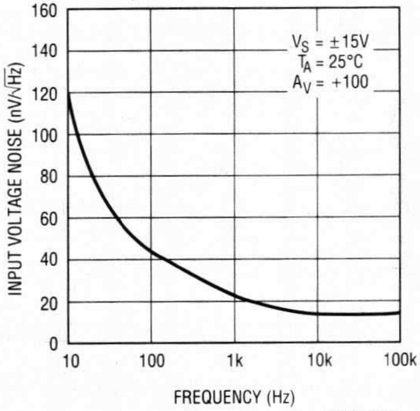
TYPICAL PERFORMANCE CHARACTERISTICS

Open Loop Gain vs Temperature



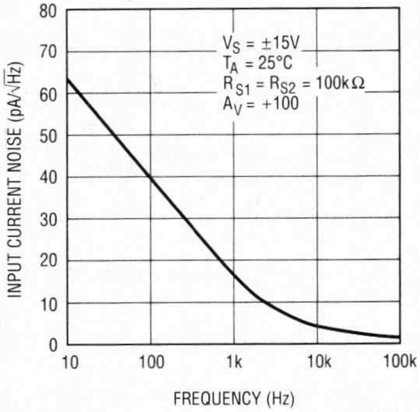
LT1220 • TPC13

Input Voltage Noise Spectral Density



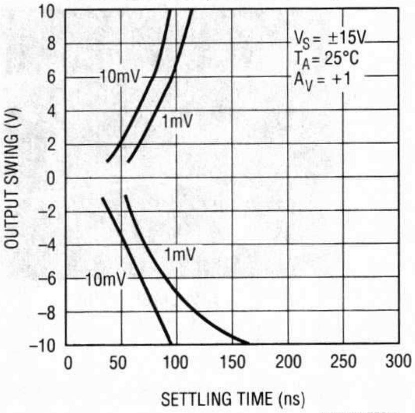
LT1220 • TPC14

Input Current Noise Spectral Density



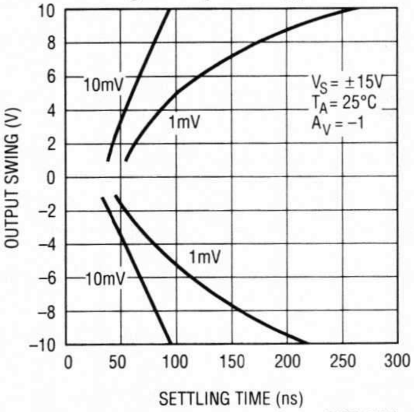
LT1220 • TPC15

Output Swing and Error vs Settling Time (Non-Inverting)



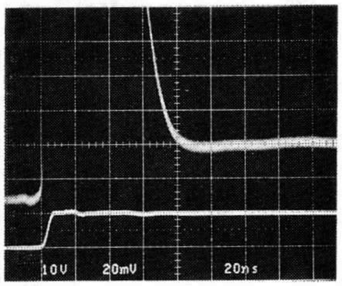
LT1220 • TPC16

Output Swing and Error vs Settling Time (Inverting)



LT1220 • TPC17

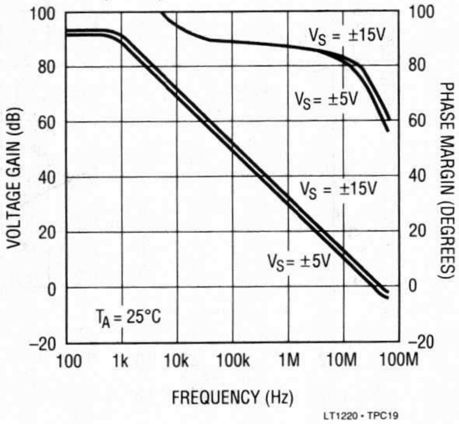
Settling Time to 0.1%



10V STEP, A_V = −1

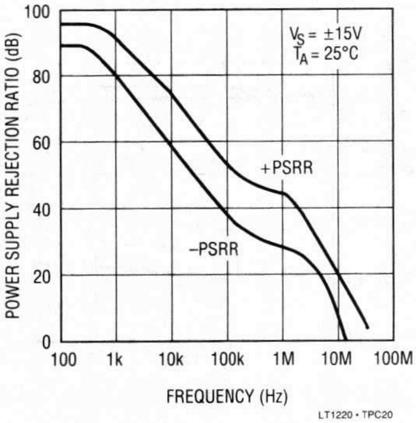
LT1220 • TPC18

Voltage Gain and Phase vs Frequency



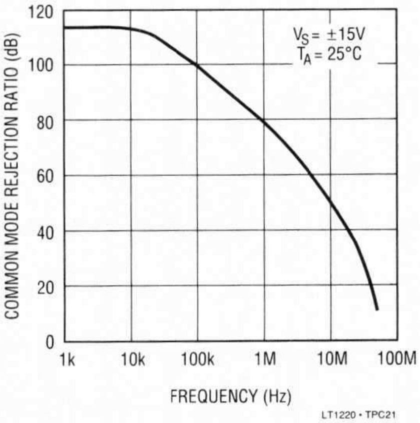
LT1220 • TPC19

Power Supply Rejection Ratio vs Frequency



LT1220 • TPC20

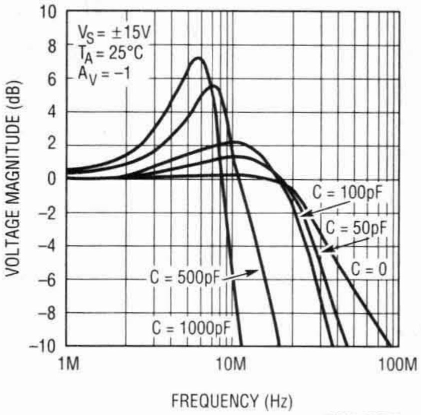
Common Mode Rejection Ratio vs Frequency



LT1220 • TPC21

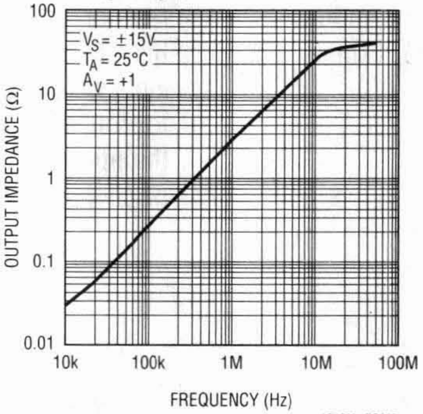
TYPICAL PERFORMANCE CHARACTERISTICS

Frequency Response vs Capacitive Load



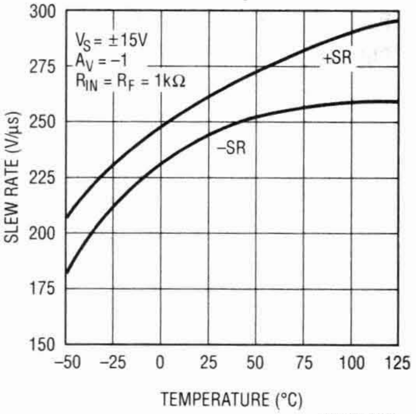
LT1220 • TPC22

Closed Loop Output Impedance vs Frequency



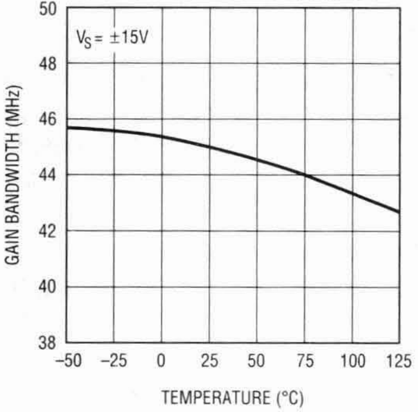
LT1220 • TPC23

Slew Rate vs Temperature



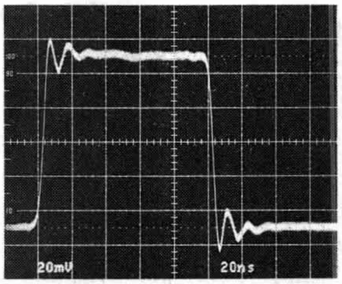
LT1220 • TPC24

Gain Bandwidth vs Temperature



LT1220 • TPC25

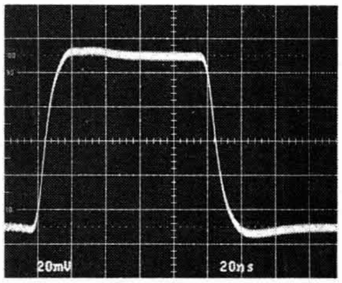
Small Signal



A_V = +1

LT1220 • TPC26

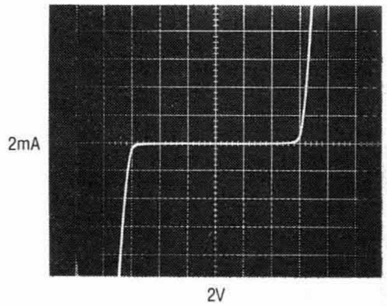
Small Signal



A_V = −1

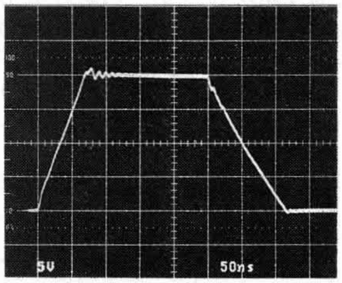
LT1220 • TPC27

Input Voltage Clamps, Pin 2 to 3



LT1220 • TPC28

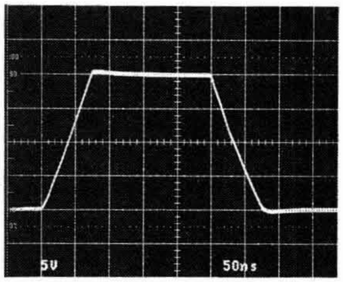
Large Signal



A_V = +1

LT1220 • TPC29

Large Signal



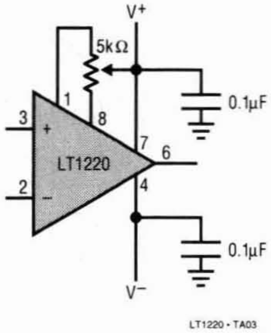
A_V = −1

LT1220 • TPC30

APPLICATIONS INFORMATION

The LT1220 may be inserted directly into HA2505/15/25, HA2541, HA2544, AD841, AD847, and LM6361 applications, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1220 is shown below.

Offset Nulling



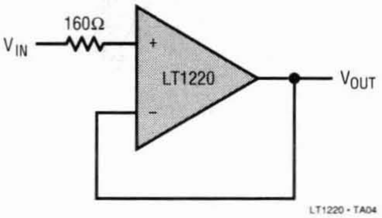
Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01μF to 0.1μF), and use of low ESR bypass capacitors for high drive current applications (typically 1μF to 10μF tantalum). Sockets should be avoided when maximum frequency performance is required, although low-profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. Feedback resistor values greater than 5kΩ are not recommended because a pole is formed with the input capacitance which can cause peaking. If feedback resistors greater than 5kΩ are used, a parallel capacitor of 5pF-10pF should be used to cancel the input pole and optimize dynamic performance.

Input Considerations

Bias current cancellation circuitry is employed on the inputs of the LT1220 so that the input bias current and input offset current have identical specifications. For this reason, matching the impedance on the inputs to reduce bias current errors is not needed. The input pins are protected by zener diode clamps which limit the maximum differential input voltage to about 6V. The effect of the clamps can be seen in high slew applications, especially in unity gain. For unity gain configurations, an optional series resistor to the non-inverting input can be used to reduce the differential input current. An example would be if the input were at +10V and the output unintentionally shorted to ground. For this case, a 160Ω series resistor would limit the input current to 25mA as the non-inverting input would be clamped at +6V.

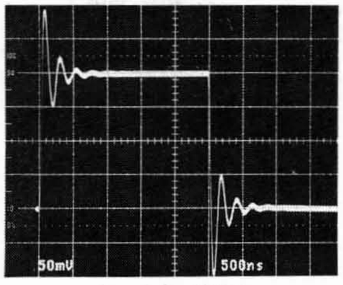
Input Current Limiting



Capacitive Loading

The LT1220 is stable with all capacitive loads. This is accomplished by sensing the load-induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases both the bandwidth and phase margin decrease. There will be peaking in the frequency response as shown in the curve of Frequency Response vs Capacitive Load. The small signal transient response will have more overshoot as shown in the photo of an inverter loaded with 1000pF. The output slew rate will be limited by the output short circuit current as seen in the photo of the large signal response of an inverter loaded with 10,000pF. The LT1220 can drive coaxial cable directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output and also at the end of the cable.

Small Signal Capacitive Loading

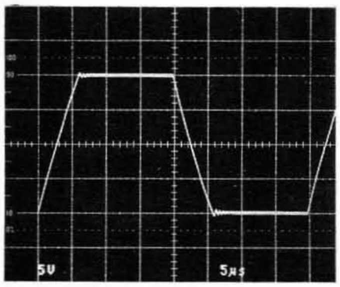


$A_V = -1$, $C_L = 1000pF$

LT1220 • TA05

APPLICATIONS INFORMATION

Large Signal Capacitive Loading



$A_V = -1$, $C_L = 10,000pF$

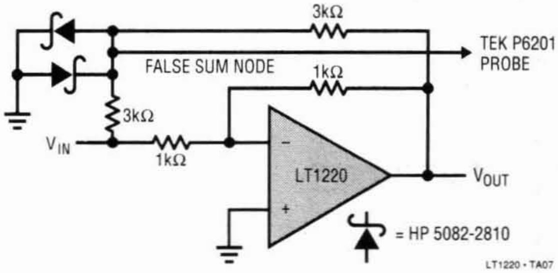
LT1220 • TA06

Settling Time

The LT1220 is a single gain stage topology and has outstanding settling characteristics. Settling time to 0.1% for a 10V step is straightforward to measure using a false sum node and an inverter configuration. Note that the voltage measured at the sum node is 1/2 the difference between the input and output voltage, so the false sum node must settle to 5mV for the output to be within 10mV. A photo showing the results of this method is shown in the typical performance curves.

The 0.01% settling time measurements were made with a fixture whose design was based on "Take the Guesswork Out of Settling Time Measurements," EDN, September 19, 1985. The LT1220 has an input referred settling tail of approximately 0.5mV with a time constant of 1µs for a 10V output step. Since an inverting gain of 1 has a noise gain of 2, the settling time to 1mV at the output is therefore longer than for a unity gain configuration. This is reflected in the settling time curves.

0.1% Settling Time Measurement

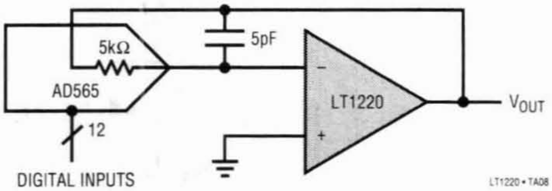


LT1220 • TA07

DAC Current to Voltage Amplifier

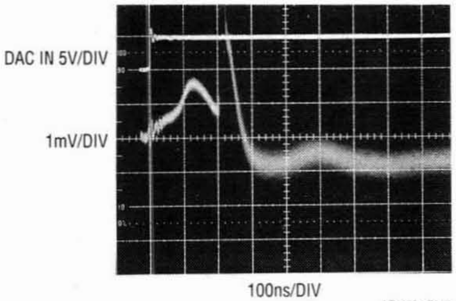
The high gain, low offset voltage, low input bias current, and fast settling of the LT1220 make it particularly useful as an I to V converter for current output DACs. A typical application is shown wth an AD565, 12-bit, 2mA full-scale output current DAC. The 5kΩ feedback resistor around the LT1220 is internal to the DAC and gives a 10V full-scale output voltage. A 5pF capacitor in parallel with the feedback resistor compensates for the DAC output capacitance and improves settling. The output of the LT1220 settles to 1/2 LSB (1.2mV) in less than 300ns. The measurement of the DAC + LT1220 combined settling involved creating a false sum node between the output of the LT1220 and a reference voltage (–10V for settling to +10V). The settling at the false sum node was then measured to 1mV. This is a difficult measurement because the node is normally clamped at several hundred millivolts and any method used to measure the node must have outstanding overdrive recovery. One method used was a sampling oscilloscope. Another method used was the previously described fixture used for 0.01% settling. A final method was a variation of a method used in AN-10 that employs a sampling switch and a variable delay. The delay allows looking at the settling waveform when it is close to 1mV and therefore does not overdrive the gain stage which follows. All three methods agreed within better than 10%. A full description of the techniques used to measure the settling time is given in AN-47, "High Speed Amplifier Techniques."

12-Bit DAC Buffer (10V Full-Scale Output)



LT1220 • TA08

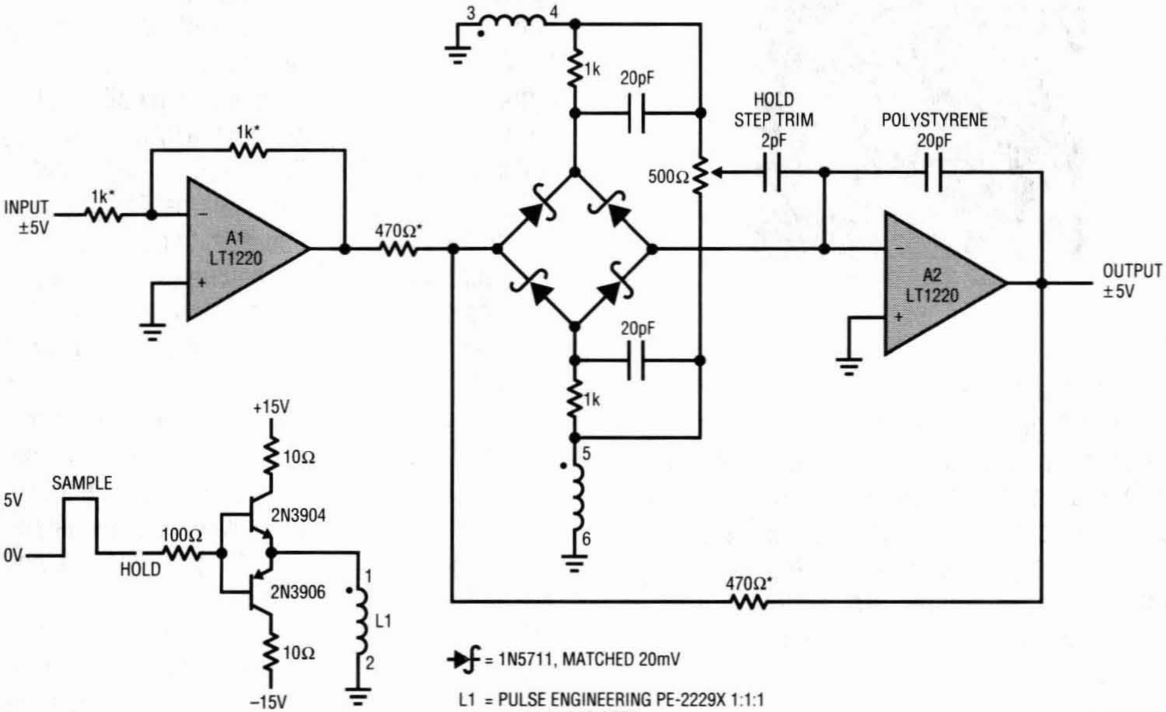
1/2 LSB Settling for 10V Output Step



LT1220 • TA09

TYPICAL APPLICATIONS

Sample and Hold, 8-Bit, 100ns


3
4
1k
20pF
HOLD
STEP TRIM
2pF
POLYSTYRENE
20pF
1k*
INPUT
±5V
1k*
A1
LT1220
470Ω*
500Ω
A2
LT1220
OUTPUT
±5V
20pF
+15V
1k
10Ω
5
5V
SAMPLE
2N3904
0V
100Ω
HOLD
6
2N3906
1
L1
10Ω
2
–15V
470Ω*

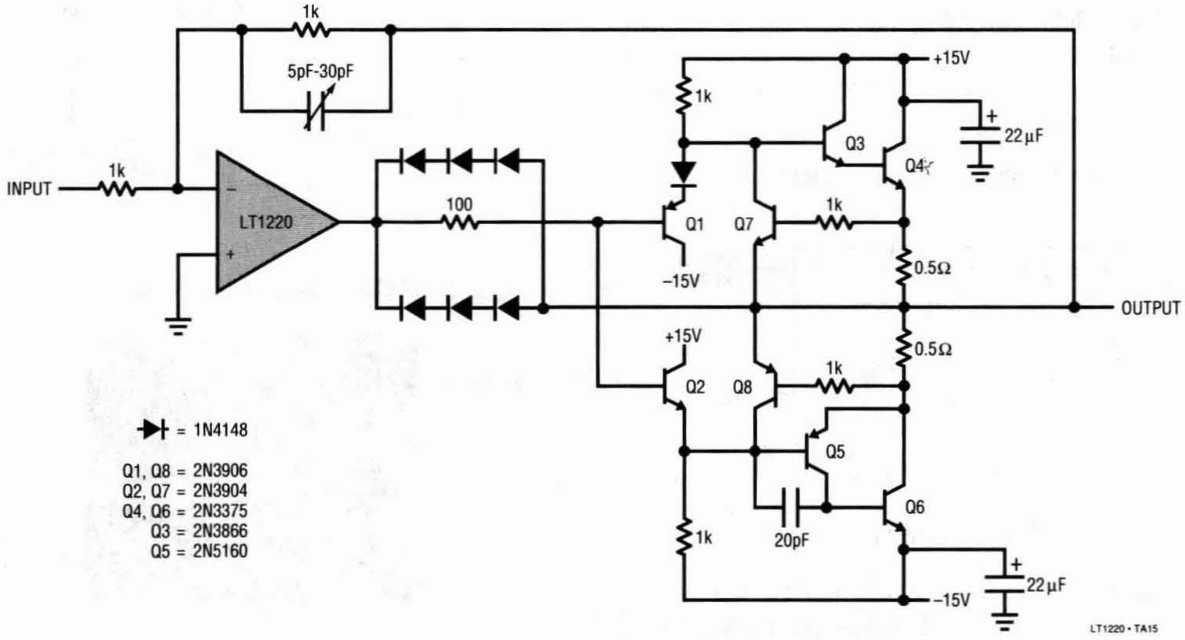
= 1N5711, MATCHED 20mV

L1 = PULSE ENGINEERING PE-2229X 1:1:1

* = 1% FILM RESISTOR

LT1220 • TA10

1A Current Buffer


1k
5pF-30pF
+15V
1k
22µF
Q3
Q4
INPUT
1k
LT1220
100
Q1
Q7
1k
0.5Ω
–15V
OUTPUT
+15V
0.5Ω
Q2
Q8
1k
Q5
Q6
1k
20pF
22µF
–15V

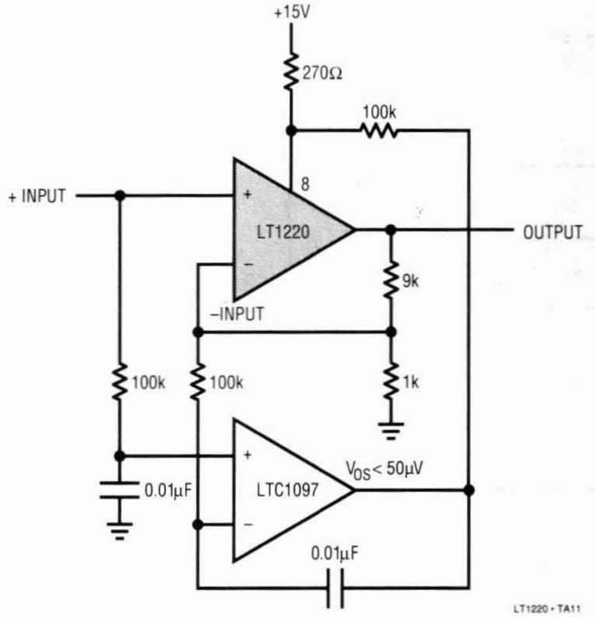
= 1N4148

Q1, Q8 = 2N3906
Q2, Q7 = 2N3904
Q4, Q6 = 2N3375
Q3 = 2N3866
Q5 = 2N5160

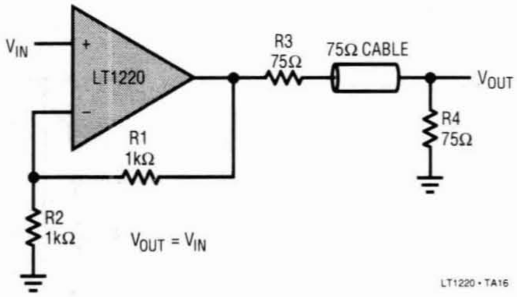
LT1220 • TA15

TYPICAL APPLICATIONS

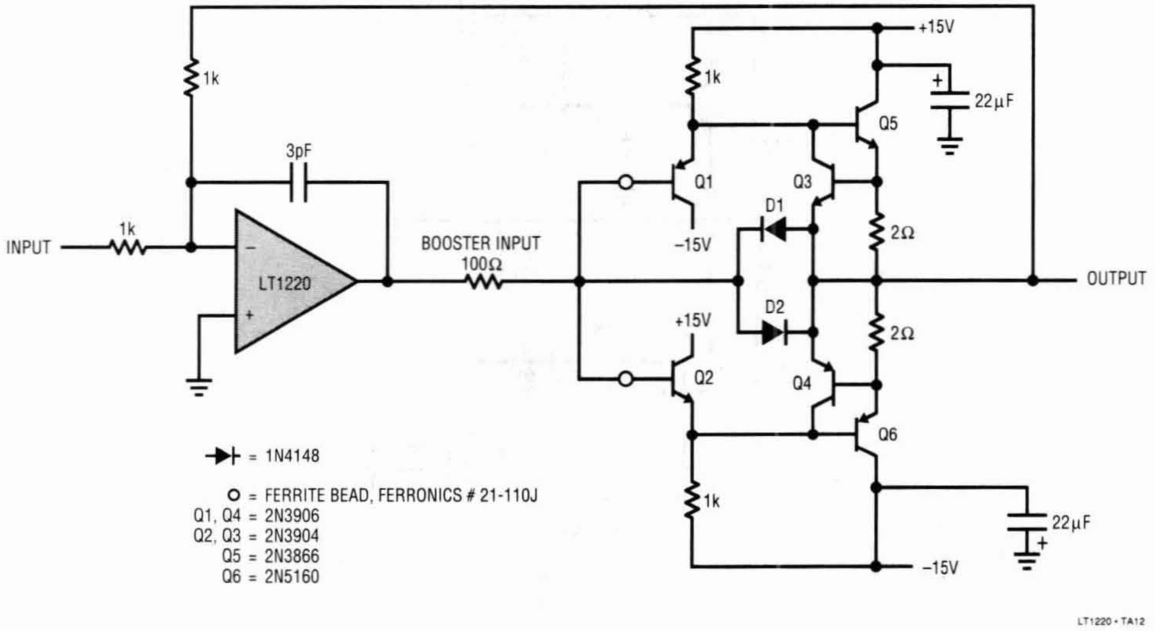
V_{OS} Nulling Loop


+15V
270Ω
100k
8
+ INPUT
LT1220
OUTPUT
9k
–INPUT
100k
100k
1k
LTC1097
V_{OS} < 50µV
0.01µF
0.01µF
LT1220 • TA11

Doubly Terminated Cable Driver

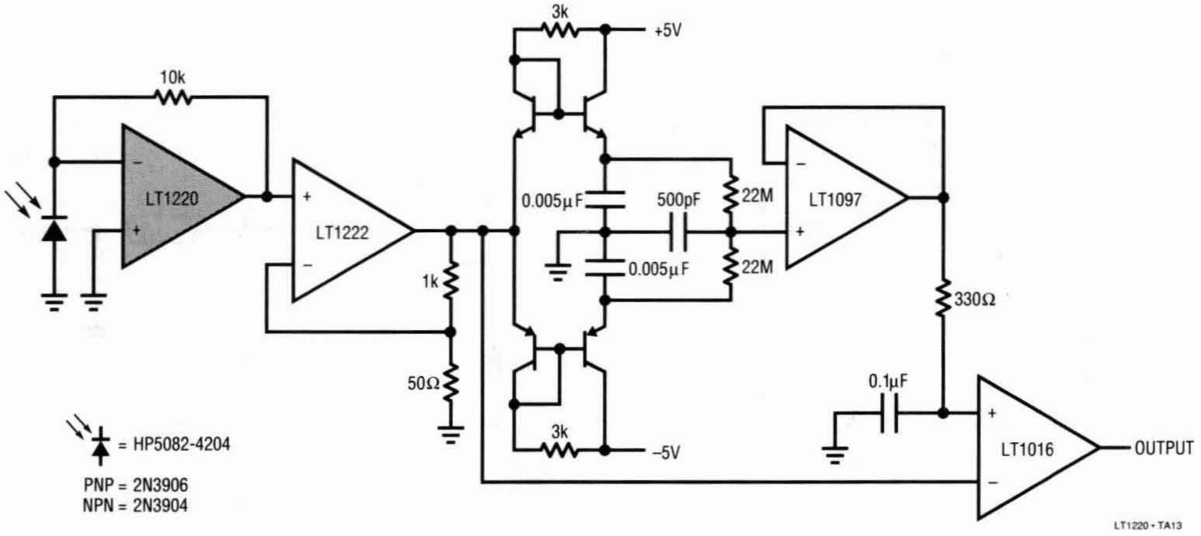

V_{IN}
LT1220
R3
75Ω
75Ω CABLE
V_{OUT}
R4
75Ω
R1
1kΩ
R2
1kΩ
$V_{OUT} = V_{IN}$
LT1220 • TA16

200mA Current Buffer

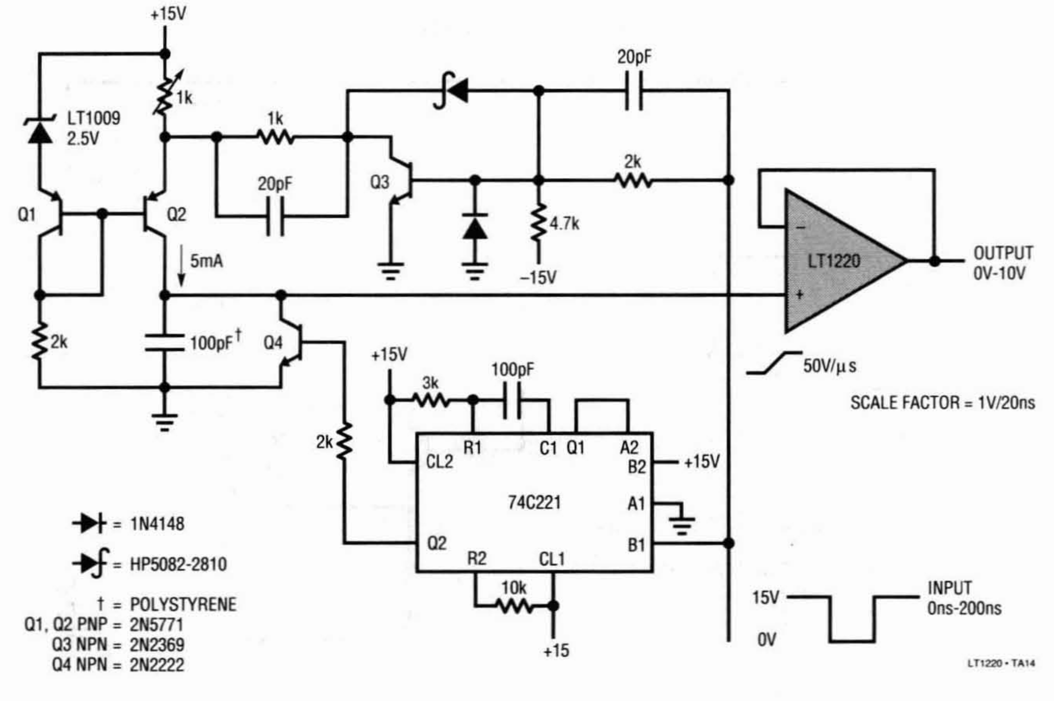

+15V
1k
1k
22µF
Q5
3pF
Q1
Q3
D1
INPUT
1k
LT1220
BOOSTER INPUT
100Ω
–15V
2Ω
OUTPUT
D2
+15V
2Ω
Q2
Q4
Q6
= 1N4148
○ = FERRITE BEAD, FERRONICS # 21-110J
Q1, Q4 = 2N3906
Q2, Q3 = 2N3904
Q5 = 2N3866
Q6 = 2N5160
1k
22µF
–15V
LT1220 • TA12

TYPICAL APPLICATIONS

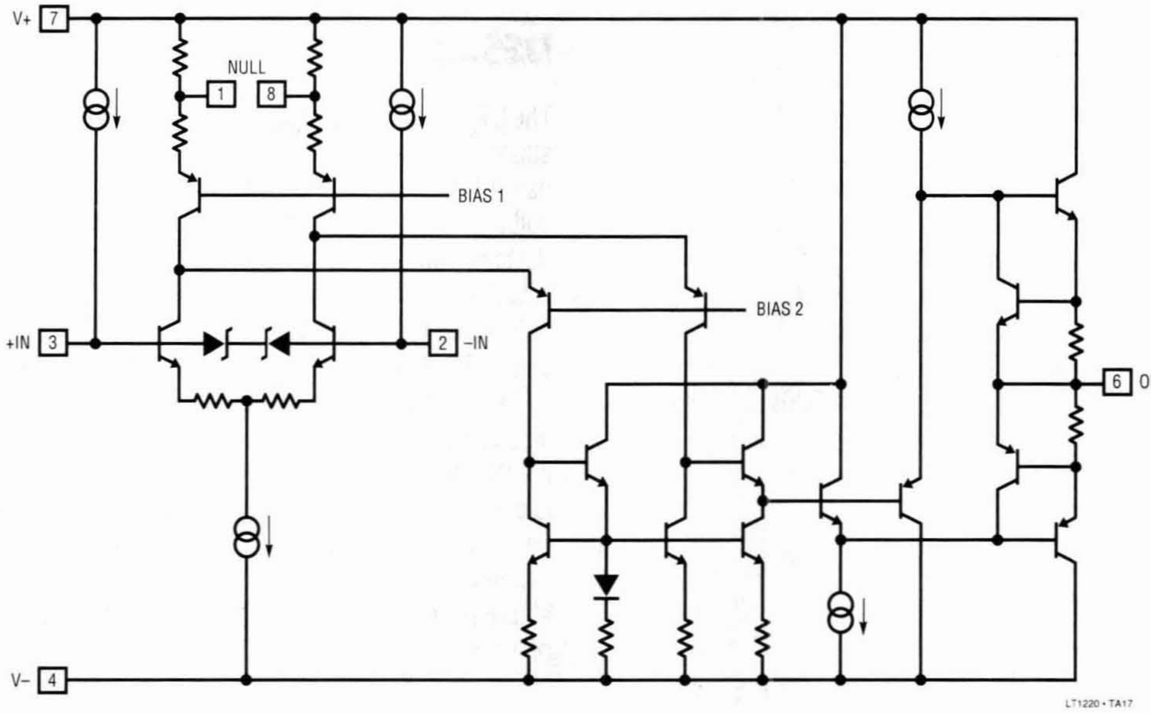
Photodiode Amplifier with Adaptive Threshold


10k
LT1220
LT1222
1k
50Ω
3k
+5V
0.005µF
500pF
22M
0.005µF
22M
3k
–5V
LT1097
330Ω
0.1µF
LT1016
OUTPUT
= HP5082-4204
PNP = 2N3906
NPN = 2N3904
LT1220 • TA13

Pulse Width Measurement


+15V
LT1009
2.5V
1k
1k
20pF
20pF
Q3
2k
4.7k
–15V
Q1
Q2
5mA
2k
100pF†
Q4
LT1220
OUTPUT
0V-10V
50V/µs
SCALE FACTOR = 1V/20ns
+15V
3k
100pF
R1
C1
Q1
A2
B2
+15V
CL2
74C221
A1
2k
Q2
R2
CL1
B1
10k
+15
15V
0V
INPUT
0ns-200ns
= 1N4148
= HP5082-2810
† = POLYSTYRENE
Q1, Q2 PNP = 2N5771
Q3 NPN = 2N2369
Q4 NPN = 2N2222
LT1220 • TA14

SIMPLIFIED SCHEMATIC


V+ 7
NULL
1
8
BIAS 1
BIAS 2
+IN 3
2 –IN
6 OUT
V– 4
LT1220 • TA17

LINEAR TECHNOLOGY

LT1221

Very High Speed Operational Amplifier

FEATURES

- Gain of +4 Stable
- 150MHz Gain Bandwidth
- 250V/μs Slew Rate
- 50,000 Minimum DC Gain
- 1mV Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- 300nA Maximum Input Offset Current
- 6nV/√Hz Input Noise Voltage
- 12V Minimum Output Swing into 500Ω
- 90ns Settling Time to 0.1%
- Drives All Capacitive Loads

APPLICATIONS

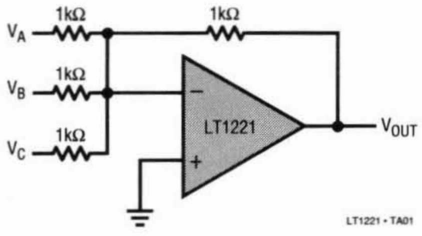
- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- 8, 10, 12-Bit Data Acquisition Systems

DESCRIPTION

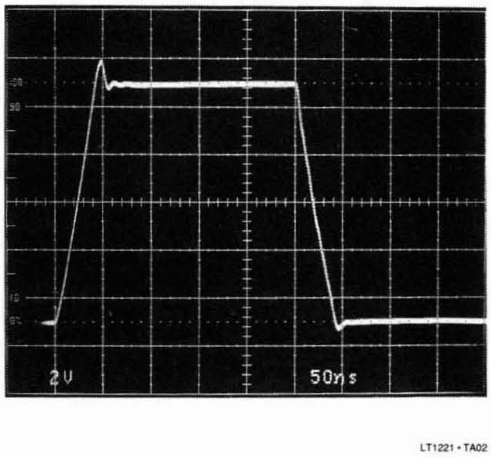
The LT1221 is a very high speed operational amplifier with superior DC performance. The LT1221 is stable in a noise gain of four or greater. It features reduced input offset voltage, lower input bias currents, and higher DC gain than devices with comparable bandwidth and slew rate. The circuit is a single gain stage that includes proprietary DC gain enhancement circuitry to obtain precision with high speed. The high gain and fast settling time make the circuit an ideal choice for data acquisition systems. The circuit is also capable of driving large capacitive loads which make it useful in buffer or cable driver applications. The LT1221 is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing. For unity gain stable applications the LT1220 can be used, and for gains of 10 or greater the LT1222 can be used.

TYPICAL APPLICATION

Summing Amplifier



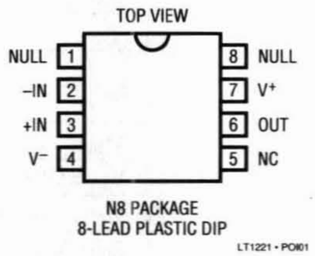
Summing Amplifier Pulse Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Current .... ±25mA
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range
LT1221C .... 0°C to 70°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

LT1221 • POI01

ORDER PART NUMBER
LT1221CN8

ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, $T_A = 25°C$, $R_L = 1k\Omega$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	1.0	mV
I_{OS}	Input Offset Current			100	300	nA
I_B	Input Bias Current			100	300	nA
e_n	Input Noise Voltage	f = 10kHz		6		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz		2		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{CM} = \pm12V$	24	45		MΩ
	Input Resistance	Differential		80		kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range +		12	14		V
	Input Voltage Range –			–13	–12	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	92	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	86	94		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	50	100		V/mV
V_{OUT+}	Output Swing +	$R_L = 500\Omega$	12.0	13.0		V
V_{OUT-}	Output Swing –	$R_L = 500\Omega$		–13.0	–12.0	V
SR	Slew Rate	(Note 3)	200	250		V/μs
	Full Power Bandwidth	10V Peak (Note 4)		4		MHz
GBW	Gain Bandwidth	f = 1MHz		150		MHz
t_r, t_f	Rise Time	$A_{VCL} = +4$, 10%-90%, 0.1V		5		ns
	Overshoot	$A_{VCL} = +4$, 0.1V		20		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V		5		ns
t_s	Settling Time	10V Step, 0.1%		90		ns
	Differential Gain	f = 3.58MHz, $R_L = 150\Omega$		1.0		%
	Differential Phase	f = 3.58MHz, $R_L = 150\Omega$		2.0		Deg.
R_O	Output Resistance	$A_{VCL} = +4$, f = 1MHz		2.5		Ω
I_S	Supply Current			8	10.5	mA

ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, T_A = 0°C-70°C, $R_L = 1k\Omega$, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	2.0	mV
	Input V_{OS} Drift			15		µV/°C
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			100	400	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	92	114		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	86	94		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	50	100		V/mV
V_{OUT+}	Output Swing +	$R_L = 500\Omega$	12.0	13.0		V
V_{OUT-}	Output Swing −	$R_L = 500\Omega$		−13.0	−12.0	V
SR	Slew Rate	(Note 3)	180	250		V/µs
I_S	Supply Current			8	11	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

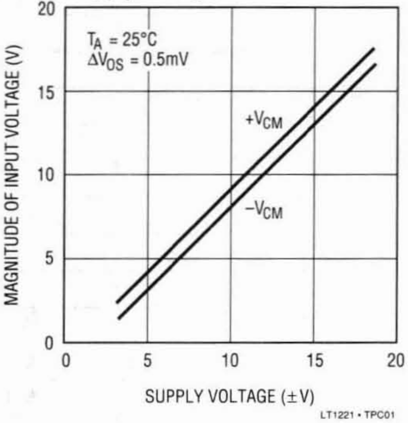
Note 2: Input Offset Voltage is tested with automated test equipment in less than one second.

Note 3: Slew rate is measured between ±10V on an output swing of ±12V.

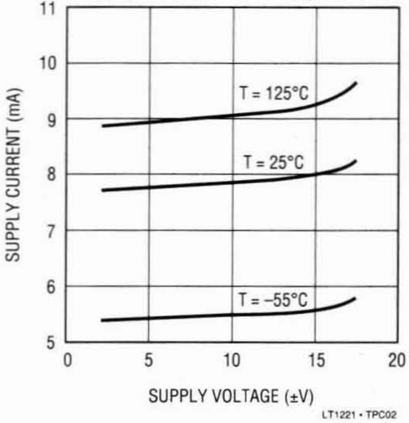
Note 4: Full power bandwidth = $SR/2\pi V_{PEAK}$.

TYPICAL PERFORMANCE CHARACTERISTICS

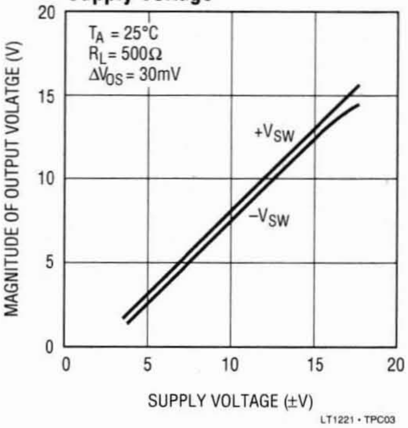
Input Common Mode Range vs Supply Voltage



Supply Current vs Supply Voltage and Temperature

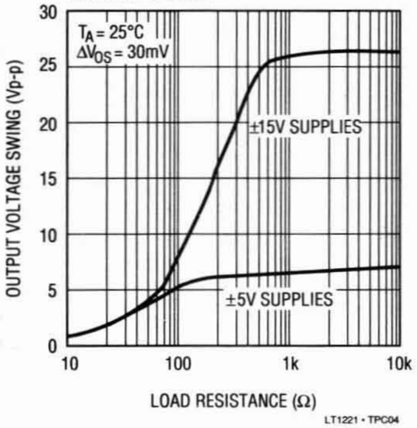


Output Voltage Swing vs Supply Voltage

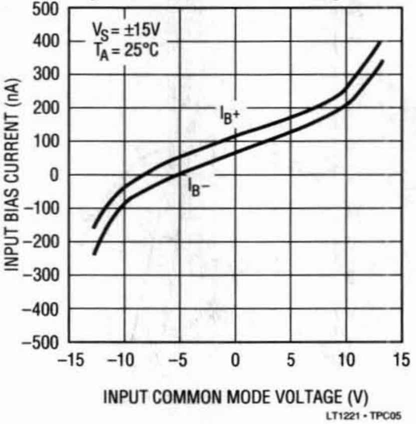


TYPICAL PERFORMANCE CHARACTERISTICS

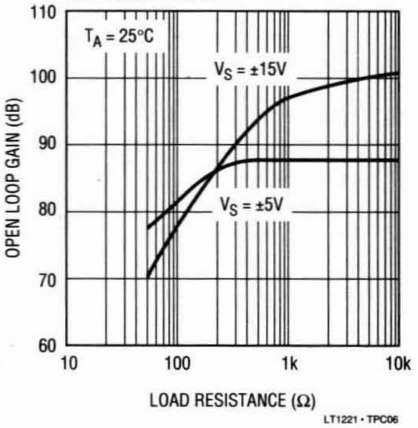
Output Voltage Swing vs Resistive Load



Input Bias Current vs Input Common Mode Voltage

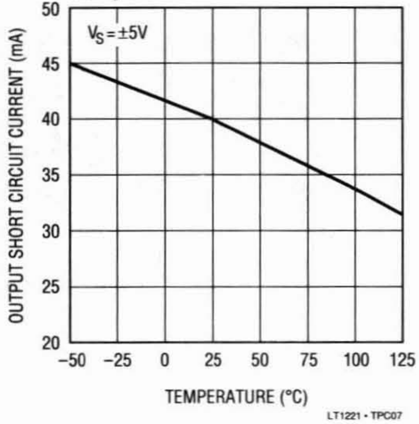


Open Loop Gain vs Resistive Load

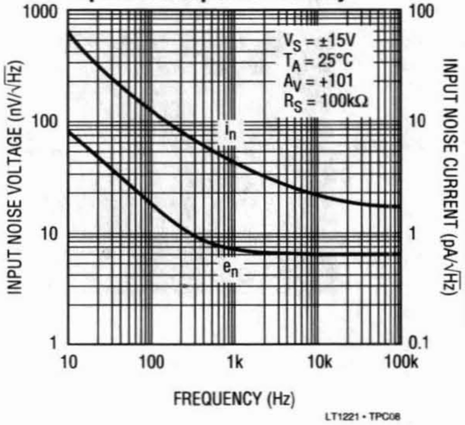


2

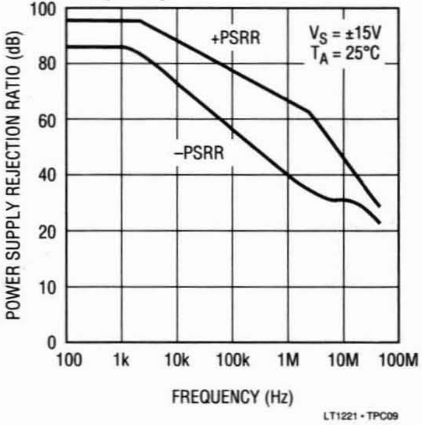
Output Short Circuit Current vs Temperature



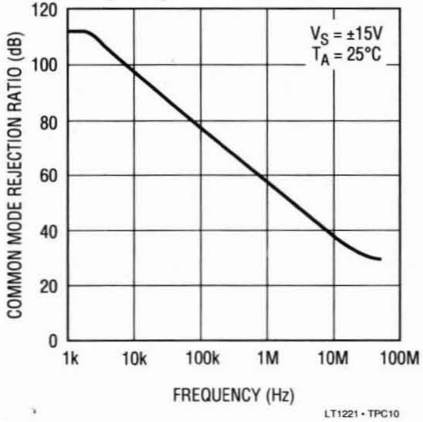
Input Noise Spectral Density



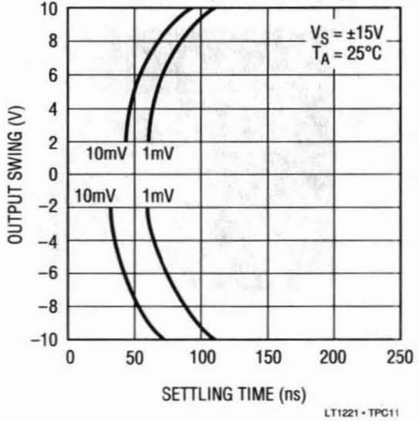
Power Supply Rejection Ratio vs Frequency



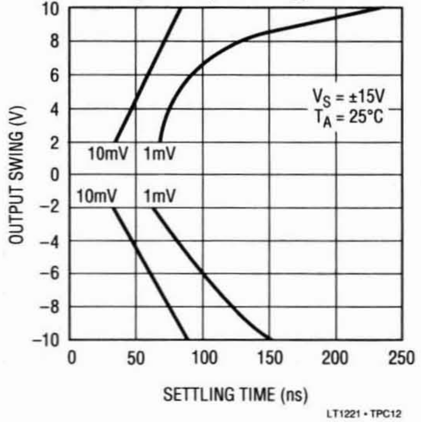
Common Mode Rejection Ratio vs Frequency



Output Swing and Error vs Settling Time (Non-Inverting)

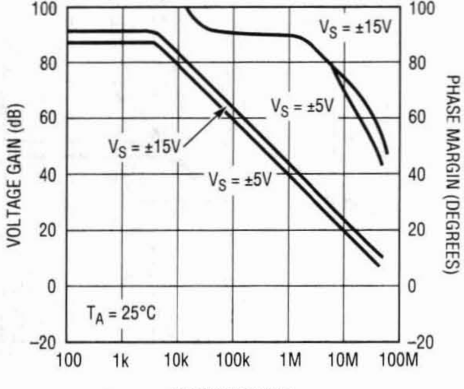


Output Swing and Error vs Settling Time (Inverting)



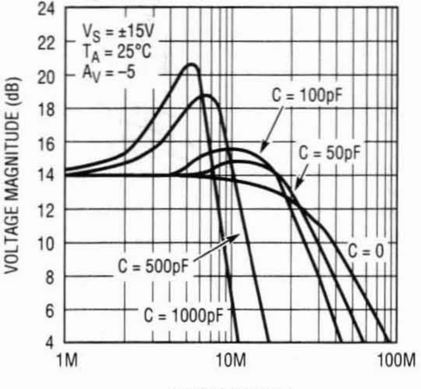
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain and Phase vs Frequency



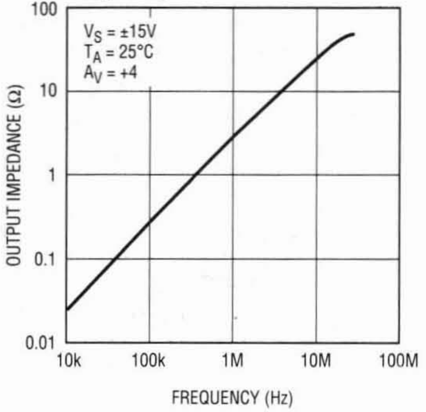
LT1221 • TPC13

Frequency Response vs Capacitive Load



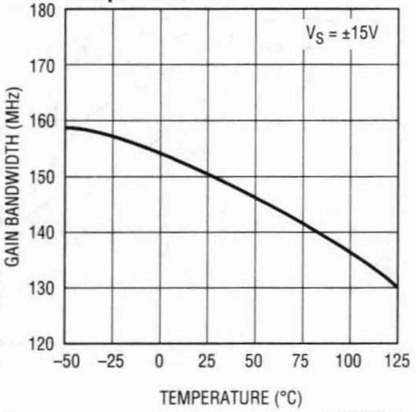
LT1221 • TPC14

Closed Loop Output Impedance vs Frequency



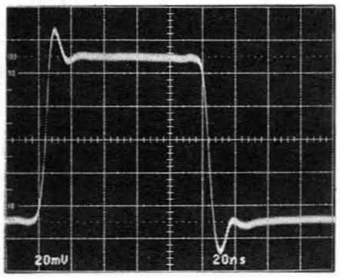
LT1221 • TPC15

Gain Bandwidth vs Temperature



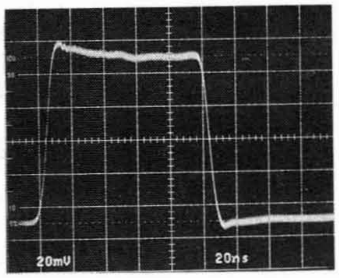
LT1221 • TPC16

Small Signal A_V = +4



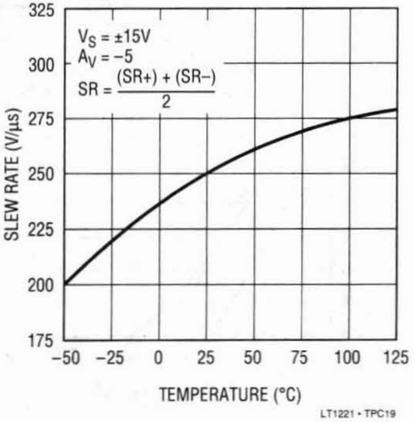
LT1221 • TPC17

Small Signal A_V = –4



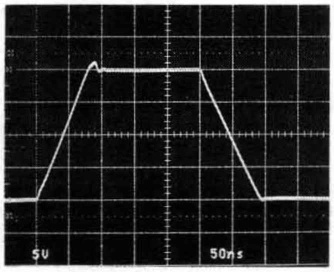
LT1221 • TPC18

Slew Rate vs Temperature



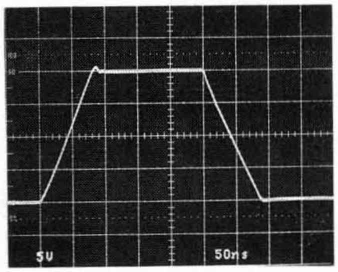
LT1221 • TPC19

Large Signal A_V = +4



LT1221 • TPC20

Large Signal A_V = –4

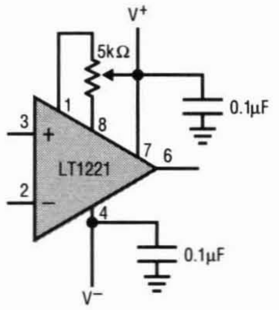


LT1221 • TPC21

APPLICATIONS INFORMATION

The LT1221 is stable in noise gains of four or greater and may be inserted directly into HA2541, HA2544, AD847, EL2020 and LM6361 applications, provided that the nulling circuitry is removed and the amplifier configuration has a high enough noise gain. The suggested nulling circuit for the LT1221 is shown below.

Offset Nulling



LT1221 • TA03

Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF), and use of low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low-profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

Feedback resistor values greater than 5kΩ are not recommended because a pole is formed with the input capacitance which can cause peaking.

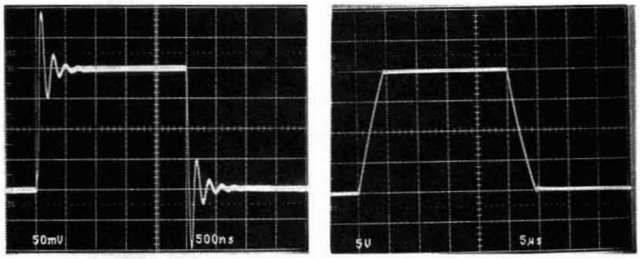
Input Considerations

Bias current cancellation circuitry is employed on the inputs of the LT1221 so the input bias current and input offset current have identical specifications. For this reason, matching the impedance on the inputs to reduce bias current errors is not necessary. The input pins are protected by zener diode clamps which limit the maximum differential input voltage to about 6V. The effect of the clamps can be seen in high slew applications, especially in non-inverting configurations.

Capacitive Loading

The LT1221 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases both the bandwidth and phase margin decrease. There will be peaking in the frequency domain as shown in the curve Frequency Response vs Capacitive Load. The small signal transient response will have more overshoot as shown in the photo $A_V = -4$ loaded with 1000pF. The large signal response for $A_V = +4$ with a 10,000pF load shows the output slew rate being limited by the short circuit current.

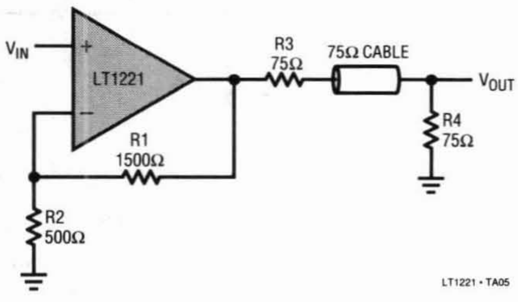
$A_V = -4$, $C_L = 1000pF$ **$A_V = +4$, $C_L = 10,000pF$**



LT1221 • TA04

The LT1221 can drive coaxial cable directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

Cable Driving



LT1221 • TA05

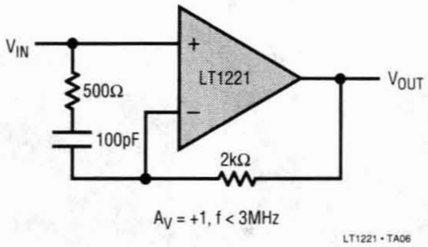
APPLICATIONS INFORMATION

Compensation

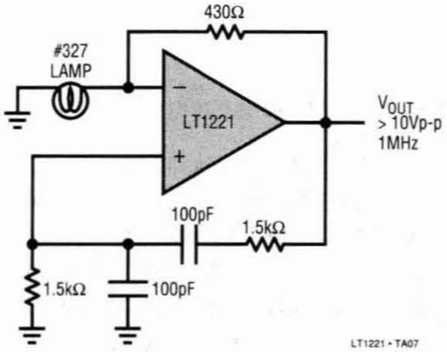
The LT1221 has a typical gain bandwidth product of 150MHz which allows it to have wide bandwidth in high gain configurations (i.e., in a gain of 10, it will have a bandwidth of about 15MHz). The amplifier is stable in a noise gain of four so the ratio of the output signal to the inverting input must be 1/4 or less. Straightforward gain configurations of +4 or –3 are stable, but there are a few configurations that allow the amplifier to be stable for lower signal gains (the noise gain, however, remains four or more). One example is the summing amplifier on the first page. Each input signal has a gain of –1 to the output, but it is easily seen that this configuration is equivalent to a gain of –3 as far as the amplifier is concerned. Another circuit is shown below with a DC gain of one, but an AC gain of +5. The break frequency of the RC combination across the amplifier inputs should be approximately a factor of 10 less than the gain bandwidth of the amplifier divided by the high frequency gain (in this case 1/10 of 150MHz/5 or 3MHz).

TYPICAL APPLICATIONS

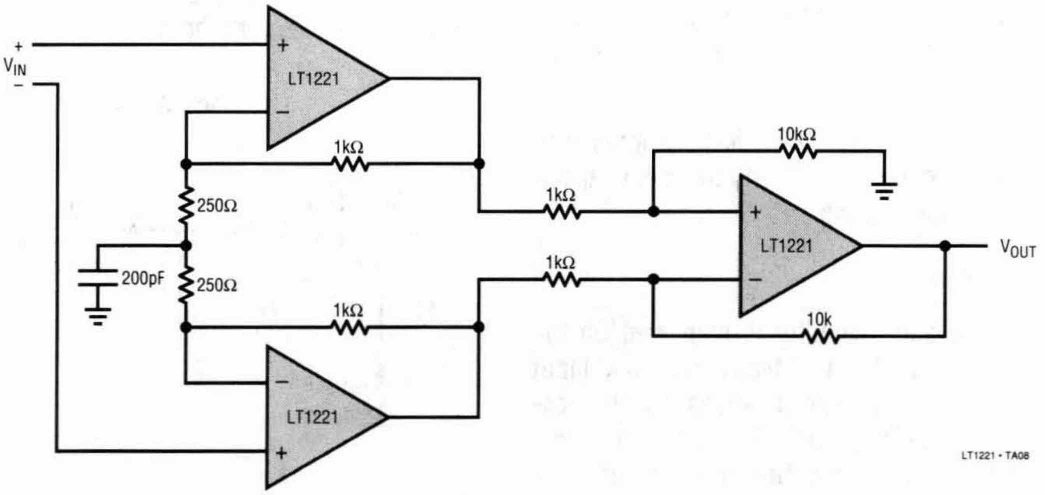
Lag Compensation


V_IN
500Ω
100pF
+
–
LT1221
V_OUT
2kΩ
A_V = +1, f < 3MHz
LT1221 • TA06

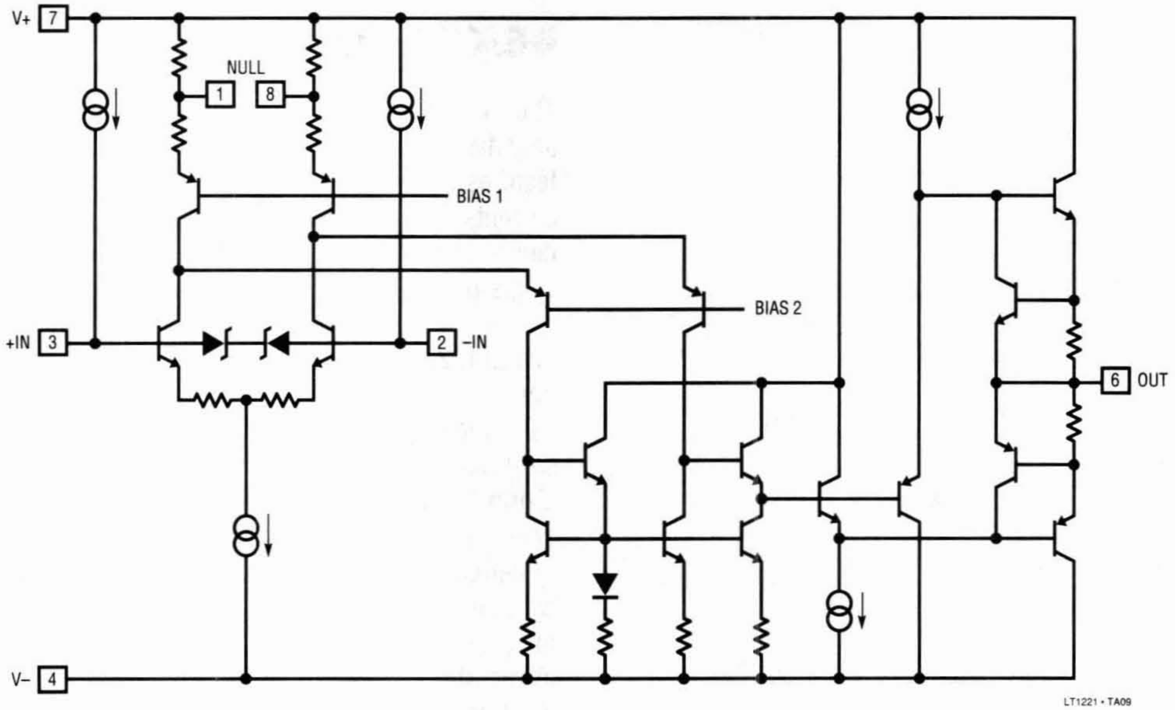
Wien Bridge Oscillator


430Ω
#327
LAMP
–
+
LT1221
V_OUT
> 10Vp-p
1MHz
100pF
1.5kΩ
1.5kΩ
100pF
LT1221 • TA07

20MHz, $A_V = 50$ Instrumentation Amplifier


+
V_IN
–
LT1221
1kΩ
250Ω
200pF
250Ω
1kΩ
LT1221
1kΩ
1kΩ
10kΩ
LT1221
V_OUT
10k
LT1221 • TA08

SIMPLIFIED SCHEMATIC


V+ 7
NULL
1
8
BIAS 1
BIAS 2
+IN 3
2 –IN
6 OUT
V– 4
LT1221 • TA09

LT1222

Low Noise, Very High Speed Operational Amplifier

FEATURES

- Gain of +10 Stable Uncompensated
- External Compensation Pin
- 500MHz Gain Bandwidth
- 200V/µs Slew Rate
- 3nV/√Hz Input Noise Voltage
- 100,000 Minimum DC Gain
- 1mV Maximum Input Offset Voltage
- 300nA Maximum Input Bias Current
- 300nA Maximum Input Offset Current
- 12V Minimum Output Swing into 500Ω
- 90ns Settling Time to 0.1%
- Drives All Capacitive Loads

APPLICATIONS

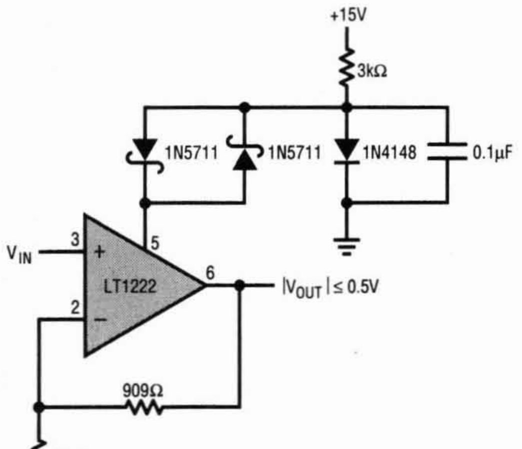
- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- 8, 10, 12-Bit Data Acquisition Systems

DESCRIPTION

The LT1222 is a low noise, very high speed operational amplifier with superior DC performance. The LT1222 features reduced input offset voltage, lower input bias currents, lower noise and higher DC gain than devices with comparable bandwidth and slew rate. The circuit is a single gain stage that includes proprietary DC gain enhancement circuitry to obtain precision with high speed. The LT1222 is stable in gains of +10 without compensation, but the part can be externally compensated for lower closed-loop gain at the expense of lower bandwidth and slew rate. The compensation node can also be used to clamp the output swing. The high gain and fast settling time make the circuit an ideal choice for data acquisition systems. The circuit is also capable of driving large capacitive loads which make it useful in buffer or cable driver applications. The part is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing. For unity gain stable applications the LT1220 can be used, and for gains of four or greater the LT1221 can be used.

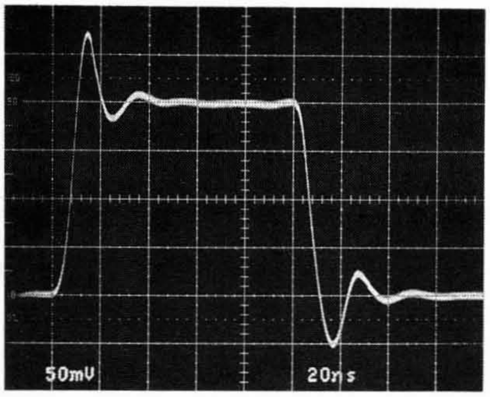
TYPICAL APPLICATION

$A_V = +10$ with Output Clamping



LT1222 • TA01

$A_V = -1$, $C_C = 30pF$ Pulse Response

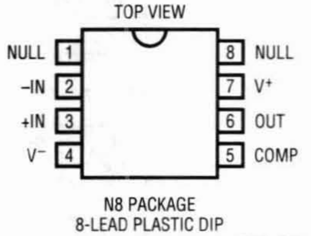


LT1222 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Current .... ±25mA
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range
LT1222C .... 0°C to 70°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

LT1222 • POI01

ORDER PART NUMBER
LT1222CN8

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, $R_L = 1k\Omega$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.3	1.0	mV
I_{OS}	Input Offset Current			100	300	nA
I_B	Input Bias Current			100	300	nA
e_n	Input Noise Voltage	f = 10kHz		3		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz		2		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$	24	45		MΩ
	Input Resistance	Differential		12		kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range +		12	14		V
	Input Voltage Range –			–13	–12	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12V$	100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	98	110		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	100	200		V/mV
V_{OUT+}	Output Swing +	$R_L = 500\Omega$	12.0	13.0		V
V_{OUT-}	Output Swing –	$R_L = 500\Omega$		–13.0	–12.0	V
SR	Slew Rate	$A_{VCL} = -10$ (Note 3)	150	200		V/µs
	Full Power Bandwidth	10V Peak (Note 4)		3.2		MHz
GBW	Gain Bandwidth	f = 1MHz		500		MHz
t_r, t_f	Rise Time	$A_{VCL} = +10$, 10%-90%, 0.1V		5		ns
	Overshoot	$A_{VCL} = +10$, 0.1V		35		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V		6.5		ns
t_s	Settling Time	10V Step, 0.1%		90		ns
	Differential Gain	f = 3.58MHz, $R_L = 150\Omega$		1.0		%
	Differential Phase	f = 3.58MHz, $R_L = 150\Omega$		2.1		Deg.
R_O	Output Resistance	$A_{VCL} = +10$, f = 1MHz		2.5		Ω
I_S	Supply Current			8	10.5	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 0°C$-$70°C$, $R_L = 1k\Omega$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	1.5	mV
	Input V_{OS} Drift			10		μV/°C
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			100	400	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm12V$	100	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	98	110		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	100	200		V/mV
V_{OUT+}	Output Swing +	$R_L = 500\Omega$	12.0	13.0		V
V_{OUT-}	Output Swing –	$R_L = 500\Omega$		–13.0	–12.0	V
SR	Slew Rate	$A_{VCL} = -10$ (Note 3)	150	200		V/μs
I_S	Supply Current			8	11	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

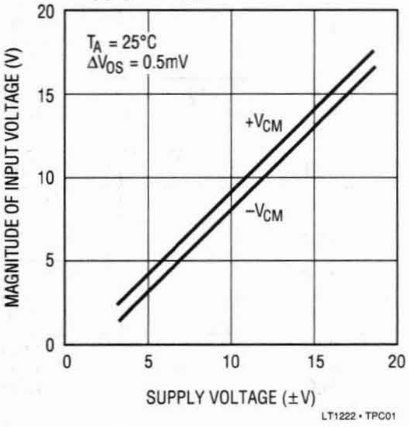
Note 2: Input offset voltage is tested with automated test equipment in less than one second.

Note 3: Slew rate is guaranteed by measuring the slew currents at the compensation pin.

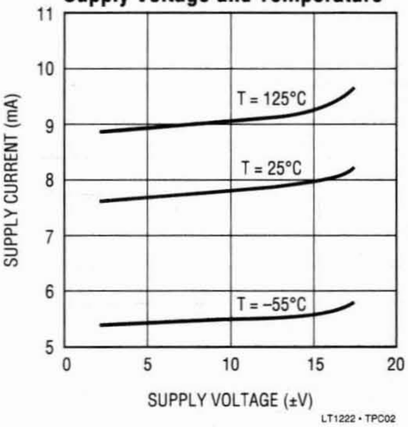
Note 4: Full power bandwidth = $SR/2\pi V_{PEAK}$.

TYPICAL PERFORMANCE CHARACTERISTICS

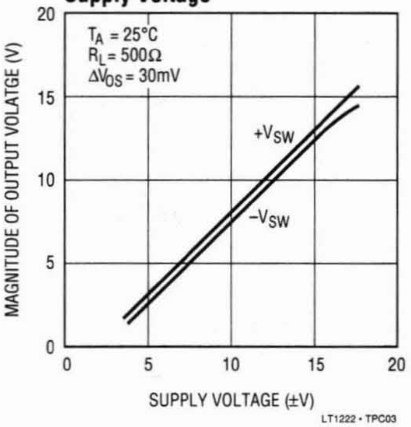
Input Common Mode Range vs Supply Voltage



Supply Current vs Supply Voltage and Temperature

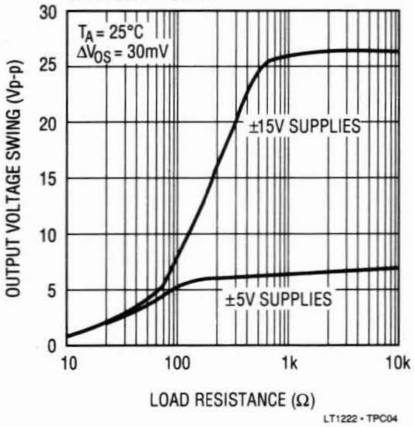


Output Voltage Swing vs Supply Voltage

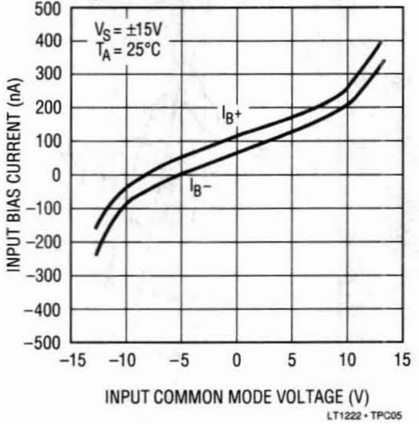


TYPICAL PERFORMANCE CHARACTERISTICS

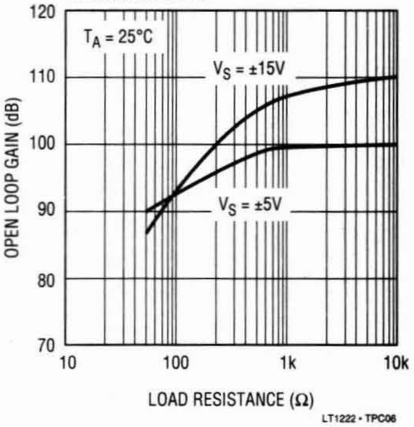
Output Voltage Swing vs Resistive Load



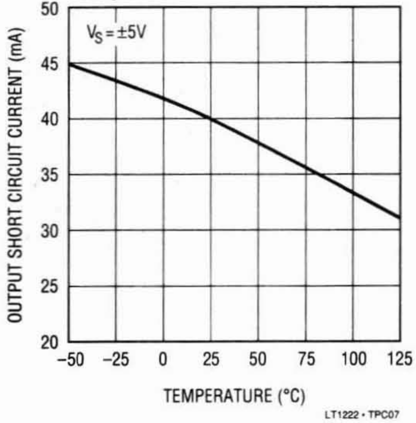
Input Bias Current vs Input Common Mode Voltage



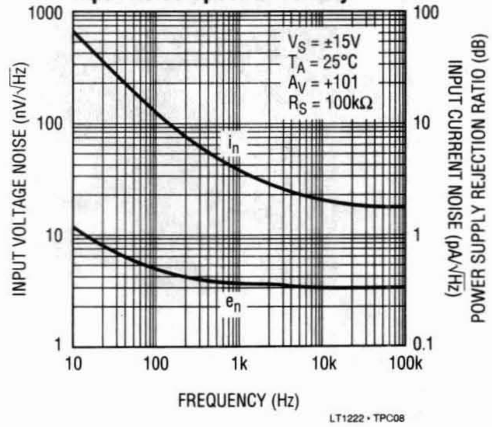
Open Loop Gain vs Resistive Load



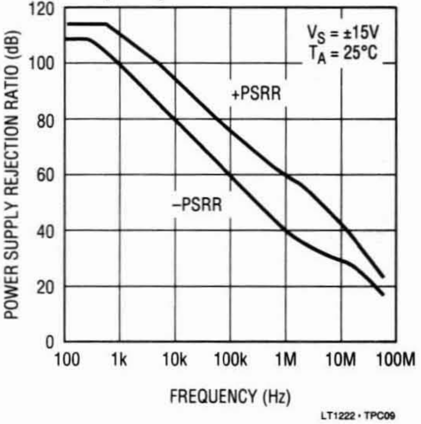
Output Short Circuit Current vs Temperature



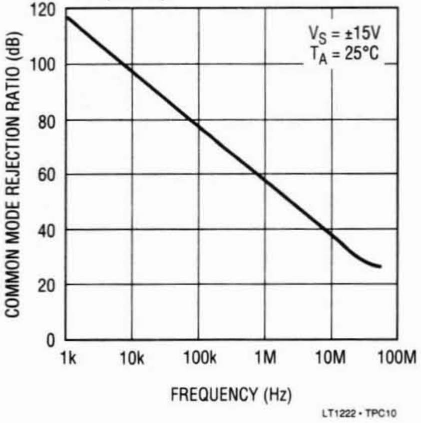
Input Noise Spectral Density



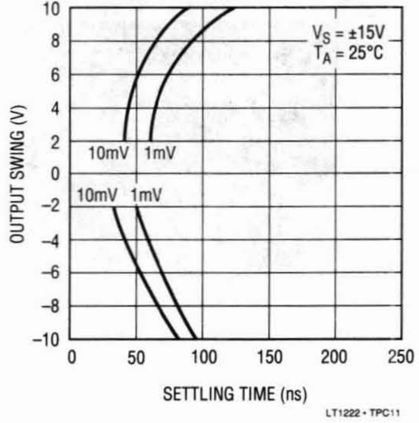
Power Supply Rejection Ratio vs Frequency



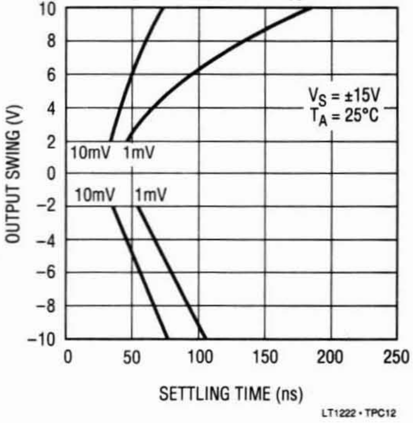
Common Mode Rejection Ratio vs Frequency



Output Swing and Error vs Settling Time (Non-Inverting)

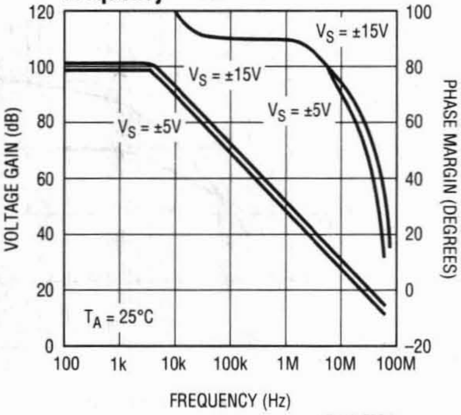


Output Swing and Error vs Settling Time (Inverting)



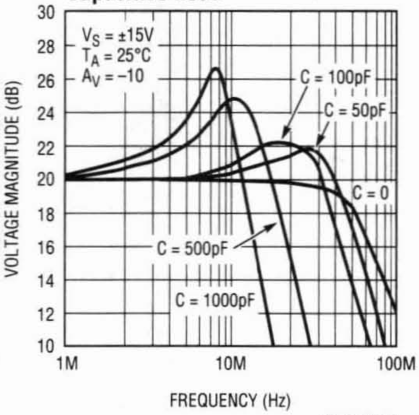
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Gain and Phase vs Frequency



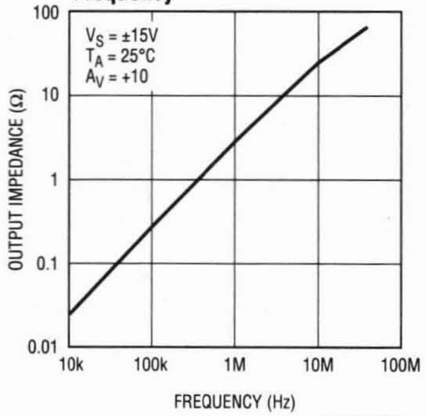
LT1222 • TPC13

Frequency Response vs Capacitive Load



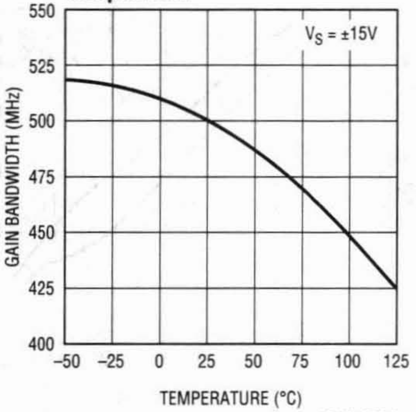
LT1222 • TPC14

Closed Loop Output Impedance vs Frequency



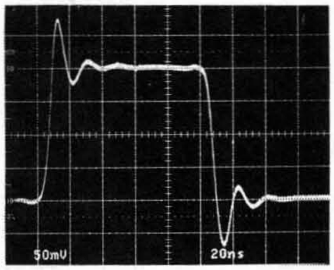
LT1222 • TPC15

Gain Bandwidth vs Temperature



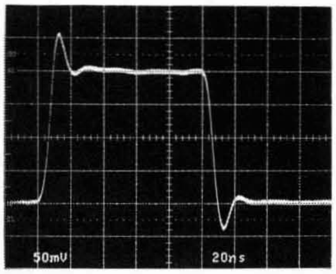
LT1222 • TPC16

Small Signal
A_V = +10



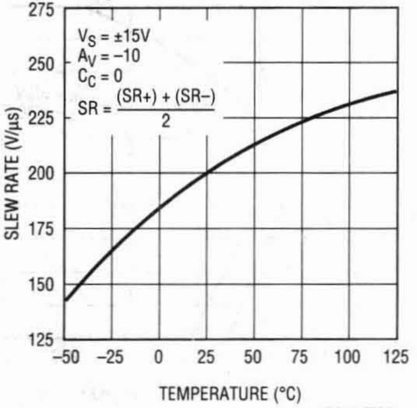
LT1222 • TPC17

Small Signal
A_V = −10



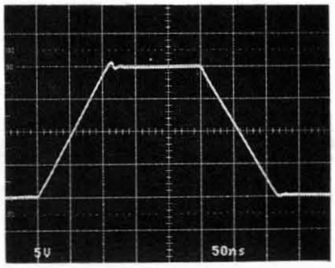
LT1222 • TPC18

Slew Rate vs Temperature



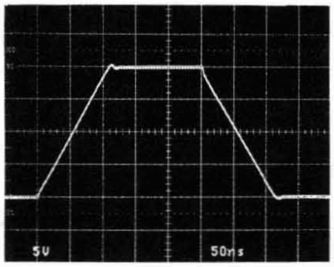
LT1222 • TPC19

Large Signal
A_V = +10



LT1222 • TPC20

Large Signal
A_V = −10

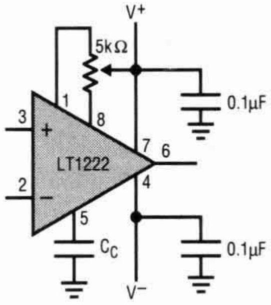


LT1222 • TPC21

APPLICATIONS INFORMATION

The LT1222 is stable without external compensation in noise gains of 10 or greater and may be inserted directly into HA2541, HA2544, AD847, EL2020 and LM6361 applications, provided that the nulling circuitry is removed and the amplifier configuration has a high enough noise gain. The suggested nulling circuit for the LT1222 is shown below.

Offset Nulling and Compensation



LT1222 • TA03

Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01μF to 0.1μF), and use of low ESR bypass capacitors for high drive current applications (typically 1μF to 10μF tantalum). Sockets should be avoided when maximum frequency performance is required, although low-profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

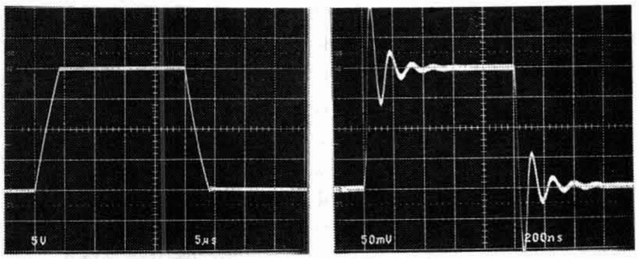
Feedback resistor values greater than 5kΩ are not recommended because a pole is formed with the input capacitance which can cause peaking.

Input Considerations

Bias current cancellation circuitry is employed on the inputs of the LT1222 so the input bias current and input offset current have identical specifications. For this reason, matching the impedance on the inputs to reduce bias current errors is not necessary. The input pins are protected by zener diode clamps which limit the maximum differential input voltage to about 6V. The effect of the clamps can be seen in high slew applications, especially in non-inverting configurations.

Capacitive Loading

The LT1222 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases both the bandwidth and phase margin decrease. There will be peaking in the frequency domain as shown in the curve Frequency Response vs Capacitive Load. The small signal transient response will have more overshoot as shown in the photo $A_V = -10$ loaded with 1000pF. The large signal response for $A_V = +10$ with a 10,000pF load shows the output slew rate being limited by the short circuit current.



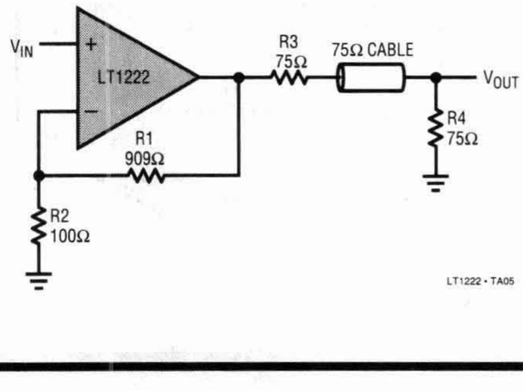
$A_V = -10$, $C_L = 1000pF$

$A_V = +10$, $C_L = 10,000pF$

LT1222 • TA04

The LT1222 can drive coaxial cable directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

Cable Driving



LT1222 • TA05

APPLICATIONS INFORMATION

Compensation

The LT1222 has a typical gain bandwidth product of 500MHz which allows it to have wide bandwidth in high gain configurations (i.e., in a gain of 100, it will have a bandwidth of 5MHz). For added flexibility the amplifier frequency response may be adjusted by adding capacitance from pin 5 to ground. A compensation capacitor may be used to reduce overshoot, to allow the amplifier to be used in lower noise gain configurations, or simply to reduce bandwidth. The table below shows gain and compensation capacitor versus –3dB bandwidth, maximum peaking in the frequency domain, and small signal overshoot.

A_V	C_C	f_{-3dB}	Mp	OS
–1	30pF	79MHz	4.5dB	35%
–1	50pF	70MHz	0.5dB	10%
–1	82pF	44MHz	0	0
–1	150pF	11MHz	0	0
+5	5pF	92MHz	7.3dB	55%
+5	10pF	82MHz	2.2dB	25%
+5	20pF	46MHz	0.1dB	5%
+5	30pF	24MHz	0	0
+5	50pF	11MHz	0	0
+10	0	90MHz	4.3dB	35%
+10	5pF	55MHz	0.1dB	5%
+10	10pF	26MHz	0	0
+10	20pF	12MHz	0	0
+20	0	40MHz	0.1dB	5%
+20	5pF	17MHz	0	0
+20	10pF	10MHz	0	0

For frequencies less than or equal to 10MHz the frequency response of the amplifier is approximately :

$$f = \frac{1}{2\pi \bullet 53\Omega \bullet (C_C + 6pF)} \bullet \frac{1}{\text{Noise Gain}}$$

Adjusting the bandwidth also affects the slew rate of the amplifier as follows:

$$SR = (1.2mA)/(C_C + 6pF)$$

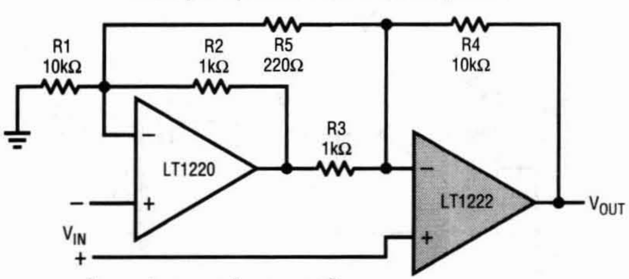
An example would be a gain of –10 (noise gain of 11) and C_C = 20pF which has about 10.5MHz bandwidth and 46V/µs slew rate. It should be noted that the LT1222 is not stable in A_V = +1 unless C_C = 100pF and 200pF is placed on the output (f = 25MHz, slew rate = 11V/µs). In any application, to reduce peaking, increase gain or add more compensation capacitance.

Output Clamping

Access to the internal compensation node at pin 5 also allows the output swing of the LT1222 to be clamped. An example is shown on the front page of the data sheet. The compensation node is approximately one diode drop above the output and can source or sink about 1.2mA. Back-to-back Schottky diodes clamp pin 5 to a diode drop above ground so the output is clamped to ±0.5V (the drop of the Schottkys at 1.2mA). The diode reference is bypassed for good AC response. This circuit is particularly useful for amplifying the voltage at false sum nodes used in settling time measurements.

TYPICAL APPLICATIONS

Two Op Amp Instrumentation Amplifier

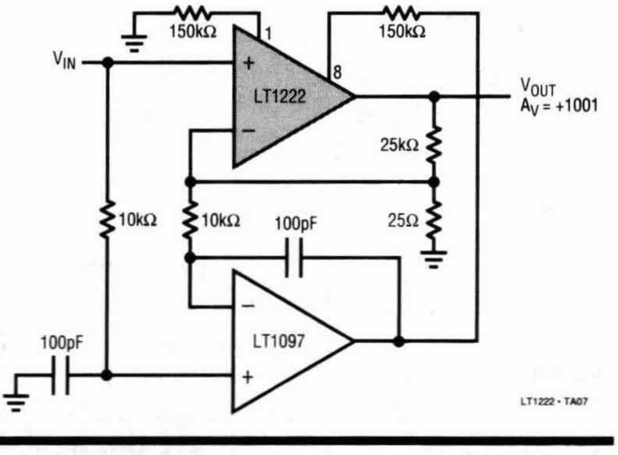


$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 102$$

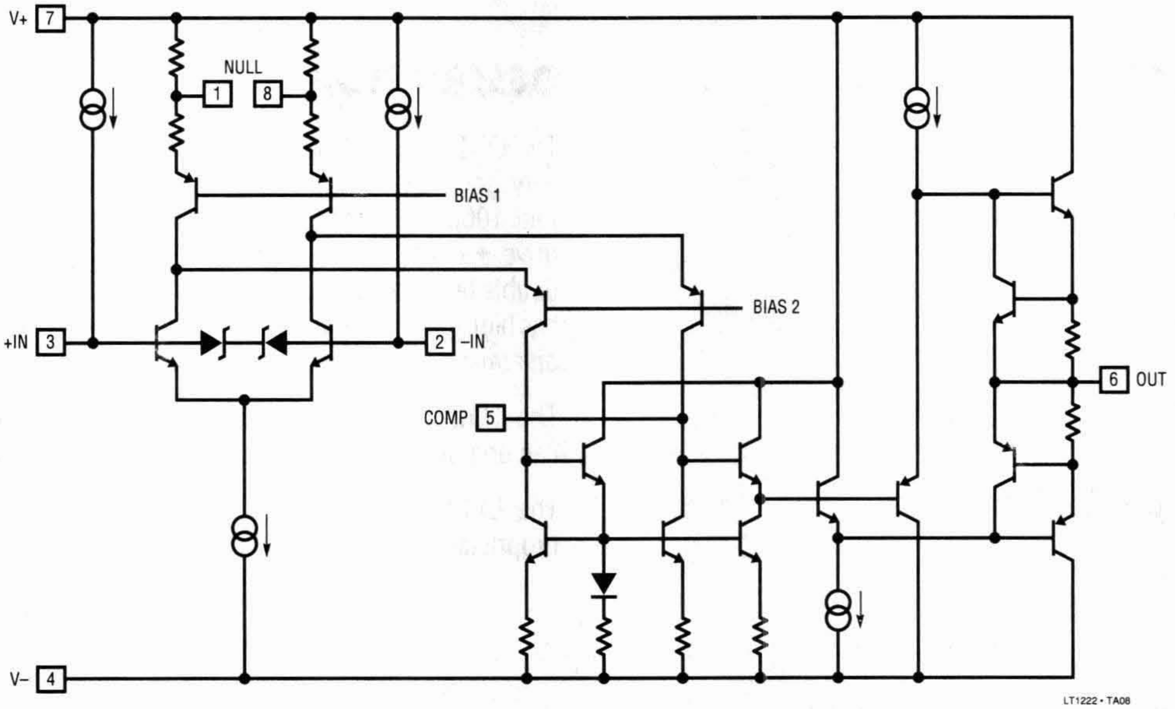
TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION
BW = 3MHz

LT1222 • TA06

V_{OS} Null Loop



SIMPLIFIED SCHEMATIC


V+ 7
NULL
1
8
BIAS 1
+IN 3
2 –IN
BIAS 2
COMP 5
6 OUT
V– 4
LT1222 • TA08

LT1223

100MHz Current Feedback Amplifier

FEATURES

- 100MHz Bandwidth at $A_V = 1$
- 1000V/µs Slew Rate
- Wide Supply Range, ±5V to ±15V
- 1mV Input Offset Voltage
- 1µA Input Bias Current
- 5MΩ Input Resistance
- 75ns Settling Time to 0.1%
- 50mA Output Current
- 6mA Quiescent Current

APPLICATIONS

- Video Amplifiers
- Buffers
- IF and RF Amplification
- Cable Drivers
- 8, 10, 12-Bit Data Acquisition Systems

DESCRIPTION

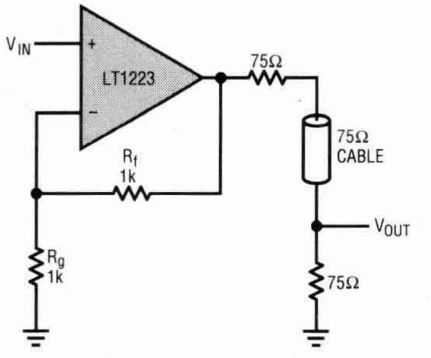
The LT1223 is a 100MHz current feedback amplifier with very good DC characteristics. The LT1223's high slew rate, 1000V/µs, wide supply range, ±15V, and large output drive, ±50mA, make it ideal for driving analog signals over double terminated cables. The current feedback amplifier has high gain bandwidth at high gains, unlike conventional op amps.

The LT1223 comes in the industry standard pinout and can upgrade the performance of many older products.

The LT1223 is manufactured on Linear Technology's proprietary complementary bipolar process.

TYPICAL APPLICATION

Video Cable Driver

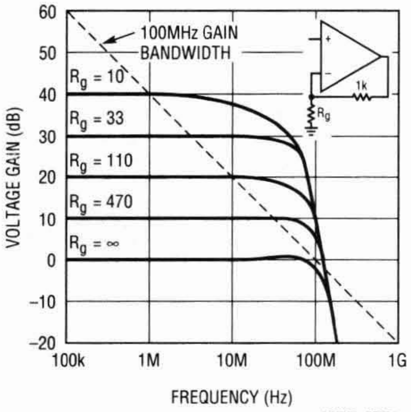


$A_V = 1 + \frac{R_f}{R_g}$

AT AMPLIFIER OUTPUT.
6dB LESS AT V_{OUT}.

LT1223 • TA02

Voltage Gain vs Frequency

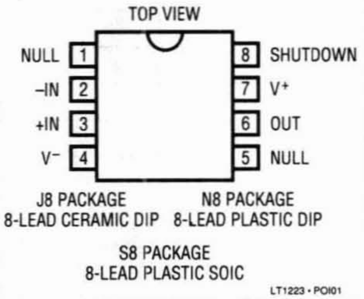


LT1223 • TPC01

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ....±18V
Differential Input Voltage..±5V
Input Voltage ....Equal to Supply Voltage
Output Short Circuit Duration (Note 1) ....Continuous
Operating Temperature Range
LT1223M ....−55°C to 125°C
LT1223C ....0°C to 70°C
Storage Temperature Range ....−65°C to 150°C
Junction Temperature Plastic Package ....150°C
Junction Temperature Ceramic Package.........175°C
Lead Temperature (Soldering, 10 sec.).................300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1223MJ8 LT1223CJ8 LT1223CN8 LT1223CS8
S8 PART MARKING
1223

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1223M/C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$		±1	±3	mV
$I_{IN}+$	Non-Inverting Input Current	$V_{CM} = 0V$		±1	±3	µA
$I_{IN}-$	Inverting Input Current	$V_{CM} = 0V$		±1	±3	µA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1k, $R_G = 10\Omega$		3.3		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Noise Current Density	f = 1kHz, R_F = 1k, $R_G = 10\Omega$		2.2		$\text{pA}/\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{IN} = \pm10V$	1	10		MΩ
C_{IN}	Input Capacitance			1.5		pF
	Input Voltage Range		±10	±12		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm10V$	56	63		dB
	Inverting Input Current Common Mode Rejection	$V_{CM} = \pm10V$		30	100	nA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm4.5V$ to $\pm18V$	68	80		dB
	Non-Inverting Input Current Power Supply Rejection	$V_S = \pm4.5V$ to $\pm18V$		12	100	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm4.5V$ to $\pm18V$		60	500	nA/V
A_V	Large Signal Voltage Gain	$R_{LOAD} = 400\Omega$, $V_{OUT} = \pm10V$	70	89		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}-$	$R_{LOAD} = 400\Omega$, $V_{OUT} = \pm10V$	1.5	5		MΩ
V_{OUT}	Maximum Output Voltage Swing	$R_{LOAD} = 200\Omega$	±10	±12		V
I_{OUT}	Maximum Output Current	$R_{LOAD} = 200\Omega$	50	60		mA
SR	Slew Rate	R_F = 1.5k, R_G = 1.5k, (Note 2)	800	1300		V/µs
BW	Bandwidth	R_F = 1k, R_G = 1k, V_{OUT} = 100mV		100		MHz
t_r	Rise Time	R_F = 1.5k, R_G = 1.5k, V_{OUT} = 1V		6.0		ns
t_{PD}	Propagation Delay	R_F = 1.5k, R_G = 1.5k, V_{OUT} = 1V		6.0		ns
	Overshoot	R_F = 1.5k, R_G = 1.5k, V_{OUT} = 1V		5		%
t_s	Settling Time, 0.1%	R_F = 1k, R_G = 1k, V_{OUT} = 10V		75		ns
	Differential Gain	R_F = 1k, R_G = 1k, $R_L = 150\Omega$		0.02		%
	Differential Phase	R_F = 1k, R_G = 1k, $R_L = 150\Omega$		0.12		Deg.
R_{OUT}	Open Loop Output Resistance	$V_{OUT} = 0$, $I_{OUT} = 0$		35		Ω
I_S	Supply Current	$V_{IN} = 0V$		6	10	mA
	Supply Current, Shutdown	Pin 8 Current = 200µA		2	4	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $0°C \le T_A \le 70°C$, unless otherwise noted.

					LT1223C		
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$	●		±1	±3	mV
$I_{IN}+$	Non-Inverting Input Current	$V_{CM} = 0V$	●		±1	±3	μA
$I_{IN}-$	Inverting Input Current	$V_{CM} = 0V$	●		±1	±3	μA
R_{IN}	Input Resistance	$V_{IN} = \pm 10V$	●	1	10		MΩ
	Input Voltage Range		●	±10	±12		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	56	63		dB
	Inverting Input Current Common Mode Rejection	$V_{CM} = \pm 10V$	●		30	100	nA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 18V$	●	68	80		dB
	Non-Inverting Input Current Power Supply Rejection	$V_S = \pm 4.5V$ to $\pm 18V$	●		12	100	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm 4.5V$ to $\pm 18V$	●		60	500	nA/V
A_V	Large Signal Voltage Gain	$R_{LOAD} = 400\Omega$, $V_{OUT} = \pm 10V$	●	70	89		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}-$	$R_{LOAD} = 400\Omega$, $V_{OUT} = \pm 10V$	●	1.5	5		MΩ
V_{OUT}	Maximum Output Voltage Swing	$R_{LOAD} = 200\Omega$	●	±10	±12		V
I_{OUT}	Maximum Output Current	$R_{LOAD} = 200\Omega$	●	50	60		mA
I_S	Supply Current	$V_{IN} = 0V$	●		6	10	mA
	Supply Current, Shutdown	Pin 8 Current = 200μA	●		2	4	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $V_{CM} = 0V$, $-55°C \le T_A \le 125°C$, unless otherwise noted.

					LT1223M		
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$	●		±1	±5	mV
$I_{IN}+$	Non-Inverting Input Current	$V_{CM} = 0V$	●		±1	±5	μA
$I_{IN}-$	Inverting Input Current	$V_{CM} = 0V$	●		±1	±10	μA
R_{IN}	Input Resistance	$V_{IN} = \pm 10V$	●	1	10		MΩ
	Input Voltage Range		●	±10	±12		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	●	56	63		dB
	Inverting Input Current Common Mode Rejection	$V_{CM} = \pm 10V$	●		30	100	nA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4.5V$ to $\pm 15V$	●	68	80		dB
	Non-Inverting Input Current Power Supply Rejection	$V_S = \pm 4.5V$ to $\pm 15V$	●		12	200	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm 4.5V$ to $\pm 15V$	●		60	500	nA/V
A_V	Large Signal Voltage Gain	$R_{LOAD} = 400\Omega$, $V_{OUT} = \pm 10V$	●	70	89		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}-$	$R_{LOAD} = 400\Omega$, $V_{OUT} = \pm 10V$	●	1.5	5		MΩ
V_{OUT}	Maximum Output Voltage Swing	$R_{LOAD} = 200\Omega$	●	±7	±12		V
I_{OUT}	Maximum Output Current	$R_{LOAD} = 200\Omega$	●	35	60		mA
I_S	Supply Current	$V_{IN} = 0V$	●		6	10	mA
	Supply Current, Shutdown	Pin 8 Current = 200μA	●		2	4	mA

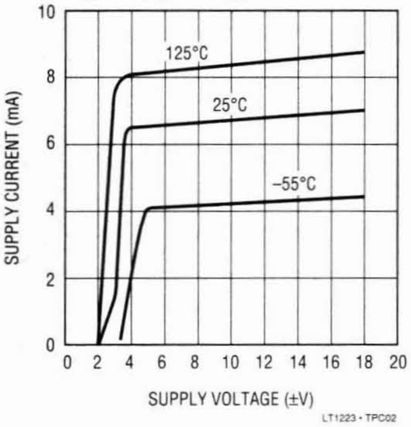
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: A heat sink may be required.

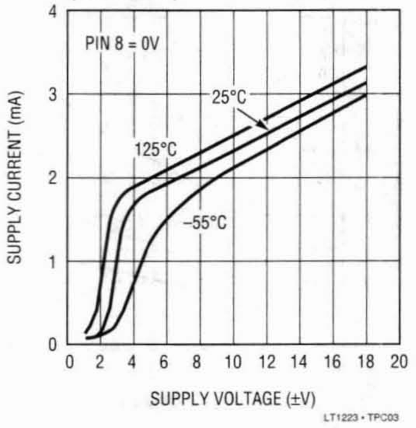
Note 2: Non-inverting operation, $V_{OUT} = \pm 10V$, measured at ±5V.

TYPICAL PERFORMANCE CHARACTERISTICS

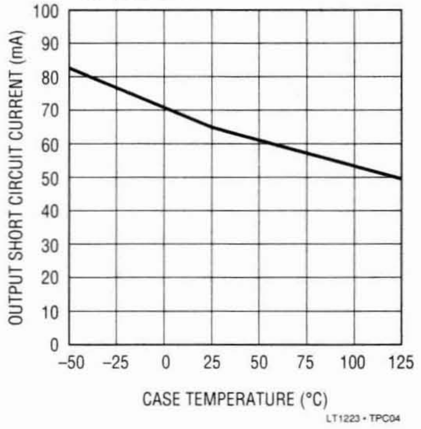
Supply Current vs Supply Voltage, $V_{IN} = 0$ (Operating)



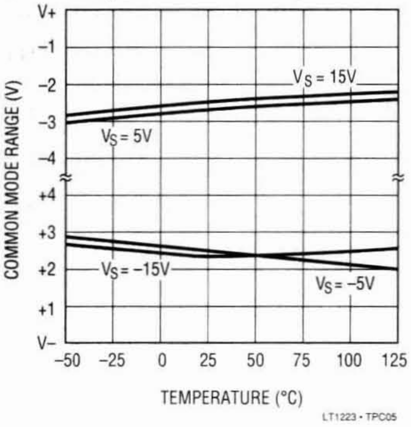
Supply Current vs Supply Voltage (Shutdown)



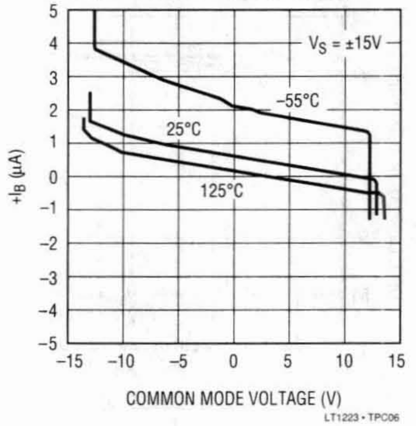
Output Short Circuit Current vs Temperature



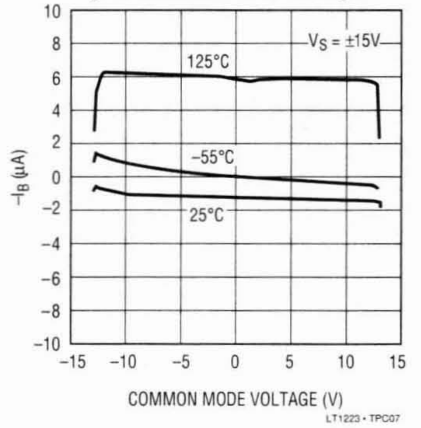
Input Common Mode Limit vs Temperature



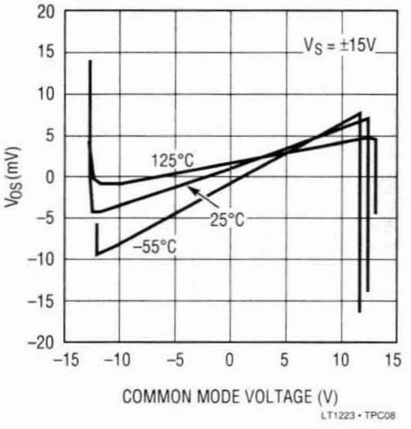
$+I_B$ vs Common Mode Voltage



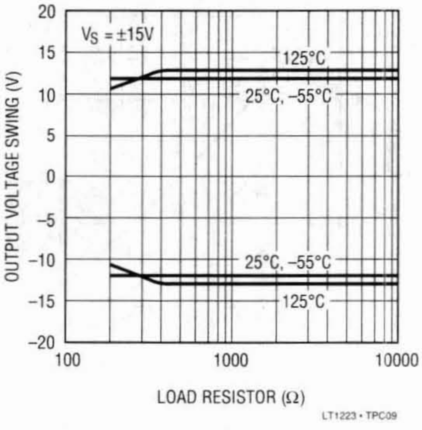
$-I_B$ vs Common Mode Voltage



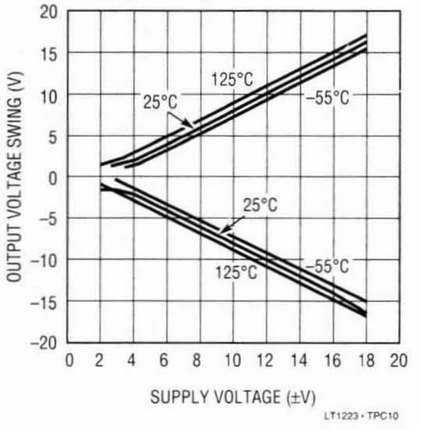
V_{OS} vs Common Mode Voltage



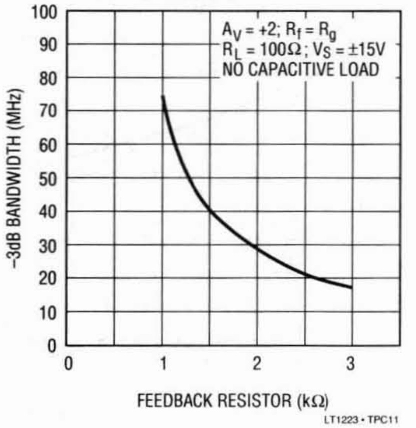
Output Voltage Swing vs Load Resistor

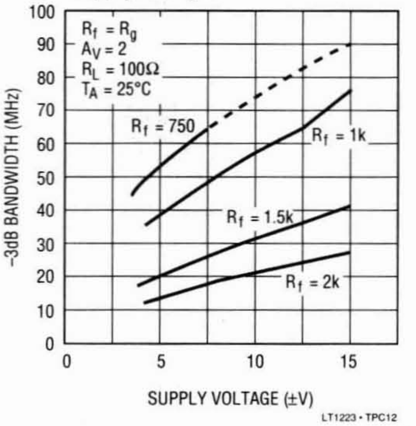


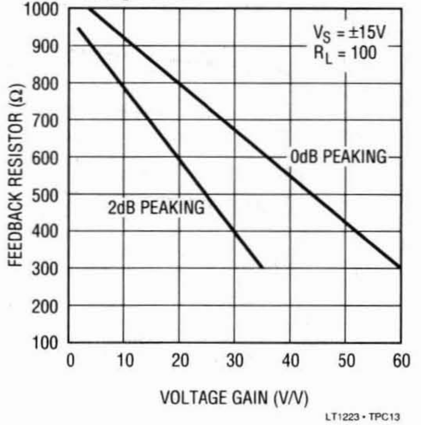
Output Voltage Swing vs Supply Voltage

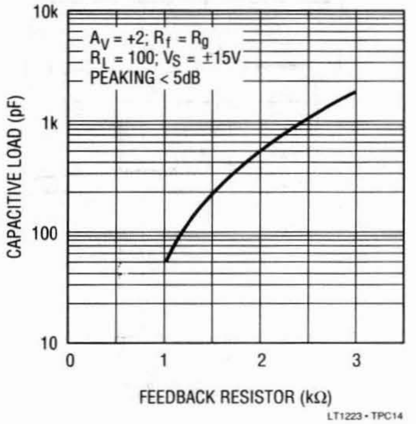


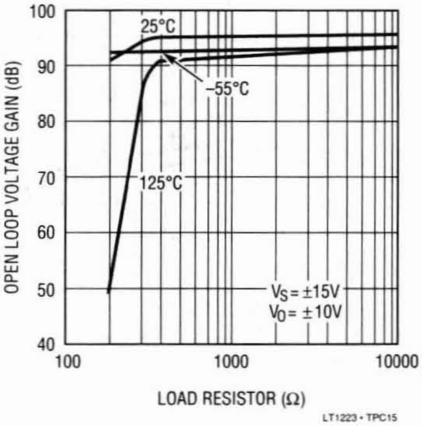
TYPICAL PERFORMANCE CHARACTERISTICS

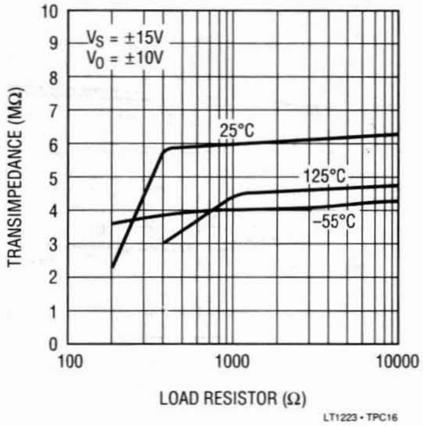

−3dB Bandwidth vs Feedback Resistor

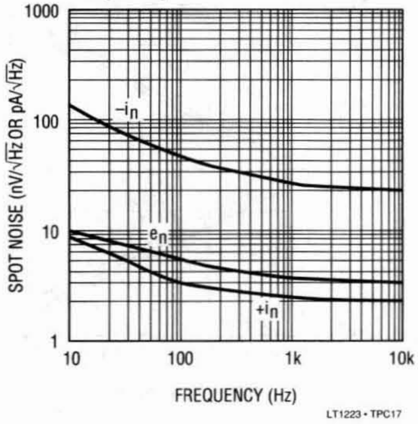

−3dB Bandwidth vs Supply Voltage

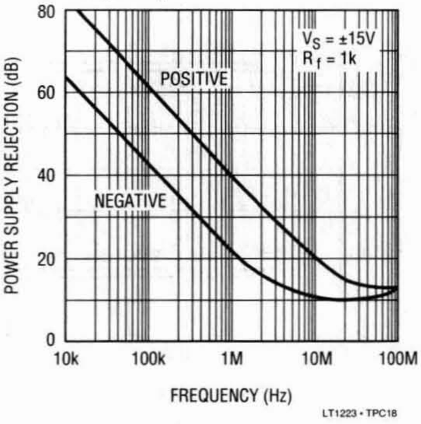

Minimum Feedback Resistor vs Voltage Gain

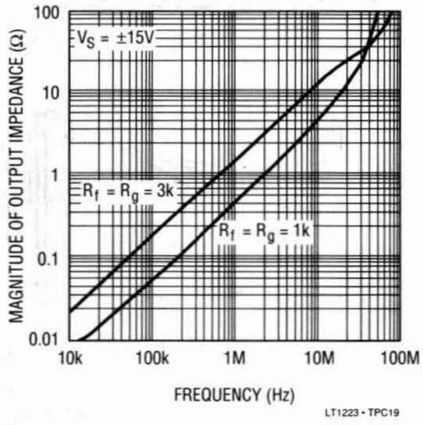

Maximum Capacitive Load vs Feedback Resistor


Open Loop Voltage Gain vs Load Resistor


Transimpedance vs Load Resistor

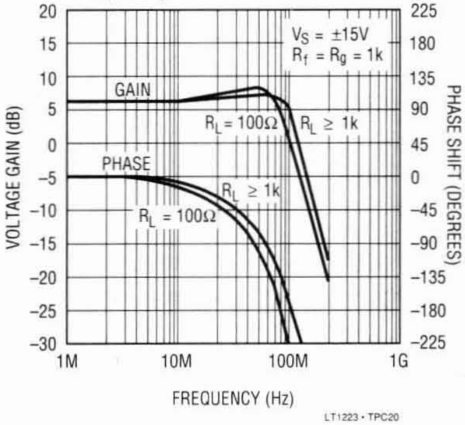

Spot Noise Voltage and Current vs Frequency


Power Supply Rejection vs Frequency

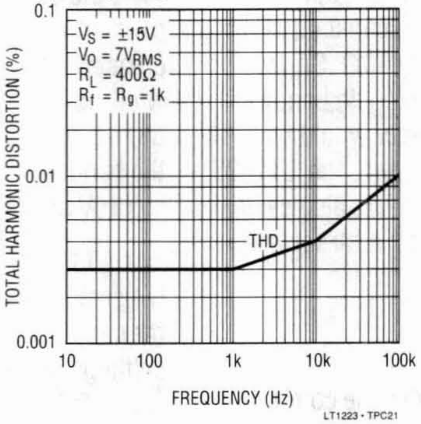

Output Impedance vs Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

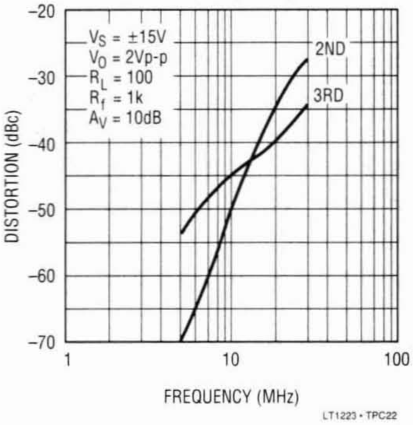
Voltage Gain and Phase vs Frequency



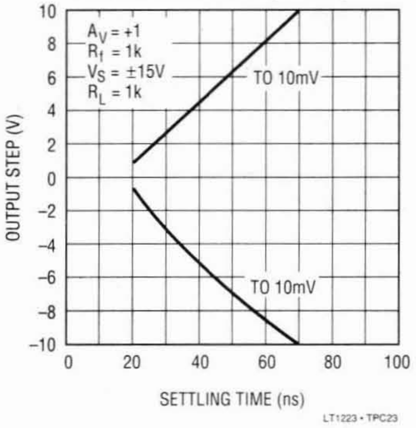
Total Harmonic Distortion vs Frequency



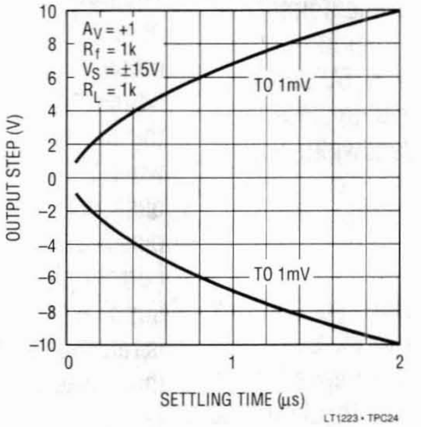
2nd and 3rd Harmonic Distortion vs Frequency



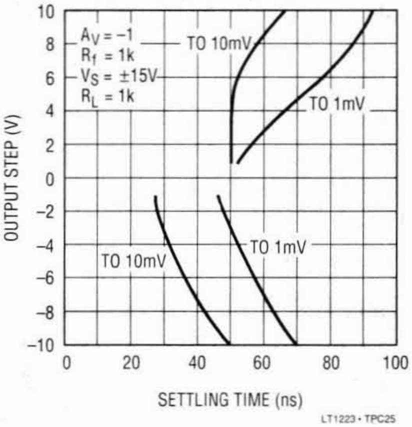
Non-Inverting Amplifier Settling Time to 10mV vs Output Step



Non-Inverting Amplifier Settling Time to 1mV vs Output Step



Inverting Amplifier Settling Time vs Output Step



APPLICATIONS INFORMATION

Current Feedback Basics

The small signal bandwidth of the LT1223, like all current feedback amplifiers, isn't a straight inverse function of the closed loop gain. This is because the feedback resistors determine the amount of current driving the amplifier's internal compensation capacitor. In fact, the amplifier's feedback resistor (R_f) from output to inverting input works with internal junction capacitances of the LT1223 to set the closed loop bandwidth.

Even though the gain set resistor (R_g) from inverting input to ground works with R_f to set the voltage gain just like it does in a voltage feedback op amp, the closed loop bandwidth does not change. This is because the equivalent gain bandwidth product of the current feedback amplifier is set by the Thevenin equivalent resistance at the inverting input and the internal compensation capacitor. By keeping R_f constant and changing the gain with R_g, the Thevenin resistance changes by the same amount as the change in gain. As a result, the net closed loop bandwidth of the LT1223 remains the same for various closed loop gains.

APPLICATIONS INFORMATION

The curve on the first page shows the LT1223 voltage gain versus frequency while driving 100Ω, for five gain settings from 1 to 100. The feedback resistor is a constant 1k and the gain resistor is varied from infinity to 10Ω. Shown for comparison is a plot of the fixed 100MHz gain bandwidth limitation that a voltage feedback amplifier would have. It is obvious that for gains greater than one, the LT1223 provides 3 to 20 times more bandwidth. It is also evident that second order effects reduce the bandwidth somewhat at the higher gain settings.

Feedback Resistor Selection

Because the feedback resistor determines the compensation of the LT1223, bandwidth and transient response can be optimized for almost every application. To increase the bandwidth when using higher gains, the feedback resistor (and gain resistor) can be reduced from the nominal 1k value. The Minimum Feedback Resistor versus Voltage Gain curve shows the values to use for ±15V supplies. Larger feedback resistors can also be used to slow down the LT1223 as shown in the –3dB Bandwidth versus Feedback Resistor curve.

Capacitive Loads

The LT1223 can be isolated from capacitive loads with a small resistor (10Ω to 20Ω) or it can drive the capacitive load directly if the feedback resistor is increased. Both techniques lower the amplifier's bandwidth about the same amount. The advantage of resistive isolation is that the bandwidth is only reduced when the capacitive load is present. The disadvantage of resistor isolation is that resistive loading causes gain errors. Because the DC accuracy is not degraded with resistive loading, the desired way of driving capacitive loads, such as flash converters, is to increase the feedback resistor. The Maximum Capacitive Load versus Feedback Resistor curve shows the value of feedback resistor and capacitive load that gives 5dB of peaking. For less peaking, use a larger feedback resistor.

Power Supplies

The LT1223 may be operated with single or split supplies as low as ±4V (8V total) to as high as ±18V (36V total). It is not necessary to use equal value split supplies, however, the offset voltage will degrade about 350μV per volt of mismatch. The internal compensation capacitor decreases with increasing supply voltage. The –3dB Bandwidth versus Supply Voltage curve shows how this affects the bandwidth for various feedback resistors. Generally, the bandwidth at ±5V supplies is about half the value it is at ±15V supplies for a given feedback resistor.

The LT1223 is very stable even with minimal supply bypassing, however, the transient response will suffer if the supply rings. It is recommended for good slew rate and settling time that 4.7μF tantalum capacitors be placed within 0.5 inches of the supply pins.

Input Range

The non-inverting input of the LT1223 looks like a 10M resistor in parallel with a 3pF capacitor until the common mode range is exceeded. The input impedance drops somewhat and the input current rises to about 10μA when the input comes too close to the supplies. Eventually, when the input exceeds the supply by one diode drop, the base collector junction of the input transistor forward biases and the input current rises dramatically. The input current should be limited to 10mA when exceeding the supplies. The amplifier will recover quickly when the input is returned to its normal common mode range unless the input was over 500mV beyond the supplies, then it will take an extra 100ns.

Offset Adjust

Output offset voltage is equal to the input offset voltage times the gain plus the inverting input bias current times the feedback resistor. For low gain applications (3 or less) a 10kΩ pot connected to pins 1 and 5 with wiper to V^+ will trim the inverting input current (±10μA) to null the output; it does not change the offset voltage very much. If the LT1223 is used in a high gain application, where input offset voltage is the dominate error, it can be nulled by pulling approximately 100μA from pin 1 or 5. The easy way to do this is to use a 10kΩ pot between pin 1 and 5 with a 150kΩ resistor from the wiper to ground for 15V supply applications. Use a 47k resistor when operating on a 5V supply.

APPLICATIONS INFORMATION

Shutdown

Pin 8 activates a shutdown control function. Pulling more than 200μA from pin 8 drops the supply current to less than 3mA, and puts the output into a high impedance state. The easy way to force shutdown is to ground pin 8, using an open collector (drain) logic stage. An internal resistor limits current, allowing direct interfacing with no additional parts. When pin 8 is open, the LT1223 operates normally.

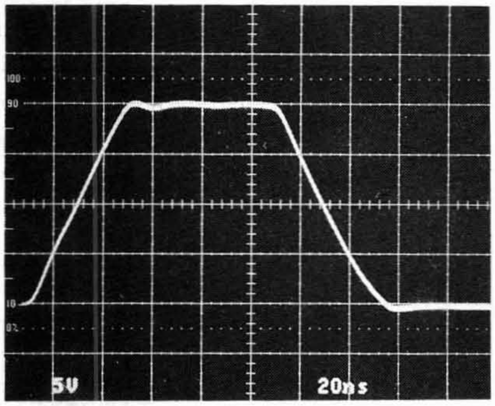
Slew Rate

The slew rate of a current feedback amplifier is not independent of the amplifier gain configuration the way it is in a traditional op amp. This is because the input stage and the output stage both have slew rate limitations. Inverting amplifiers do not slew the input and are therefore limited only by the output stage. High gain, non-inverting amplifiers are similar. The input stage slew rate of the LT1223 is about 350V/μs before it becomes non-linear and is enhanced by the normally reverse biased emitters on the input transistors. The output slew rate depends on the size of the feedback resistors. The peak output slew rate is about 2000V/μs with a 1k feedback resistor and drops proportionally for larger values. At an output slew rate of 1000V/μs or more, the transistors in the "mirror circuits" will begin to saturate due to the large feedback currents. This causes the output to have slew induced overshoot and is somewhat unusual looking; it is in no way harmful or dangerous to the device. The photos show the LT1223 in a non-inverting gain of three (R_f = 1k, R_g = 500Ω) with a 20V peak-to-peak output slewing at 500V/μs, 1000V/μs and 2000V/μs.

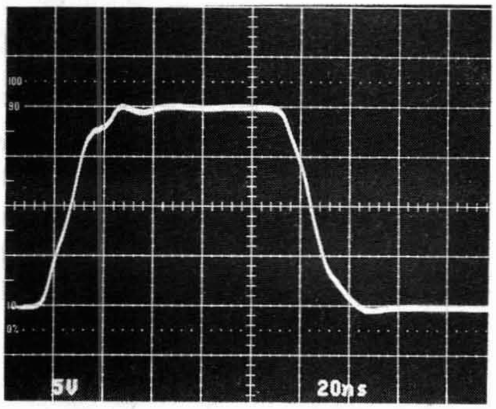
Settling Time

The Inverting Amplifier Settling Time versus Output Step curve shows that the LT1223 will settle to within 1mV of final value in less than 100ns for all output changes of 10V or less. When operated as an inverting amplifier there is less than 500μV of thermal settling in the amplifier. However, when operating the LT1223 as a non-inverting amplifier, there is an additional thermal settling component that is about 200μV for every volt of input common mode change. So a non-inverting gain of one amplifier will

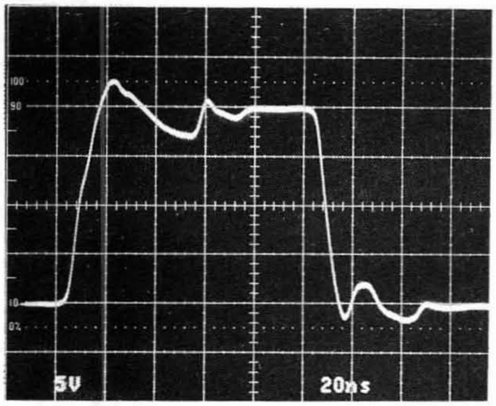
Output Slew Rate of 500V/μs



Output Slew Rate of 1000V/μs



Output Slew Rate at 2000V/μs Shows Aberrations (See Text)

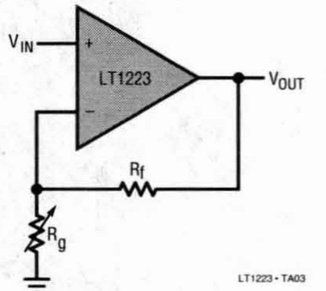


APPLICATIONS INFORMATION

have about 2.5mV thermal tail on a 10V step. Unfortunately, reducing the input signal and increasing the gain always results in a thermal tail of about the same amount for a given output step. For this reason we show separate graphs of 10mV and 1mV non-inverting amplifier settling times. Just as the bandwidth of the LT1223 is fairly constant for various closed loop gains, the settling time remains constant as well.

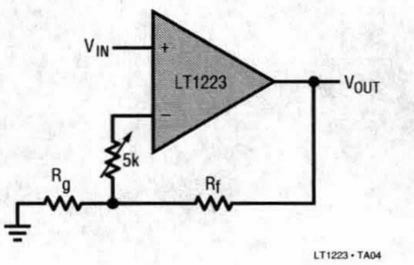
Adjustable Gain Amplifier

To make a variable gain amplifier with the LT1223, vary the value of R_g. The implementation of R_g can be a pot, a light controlled resistor, a FET, or any other low capacitance variable resistor. The value of R_f should not be varied to change the gain. If R_f is changed, then the bandwidth will be reduced at maximum gain and the circuit will oscillate when R_f is very small.



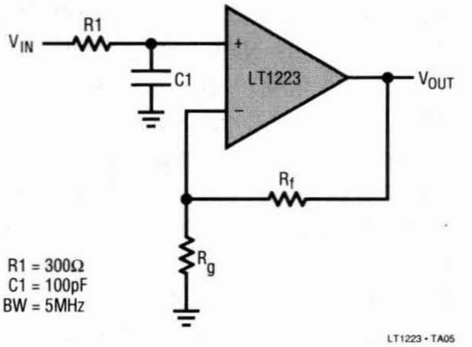
Adjustable Bandwidth Amplifier

Because the resistance at the inverting input determines the bandwidth of the LT1223, an adjustable bandwidth circuit can be made easily. The gain is set as before with R_f and R_g; the bandwidth is maximum when the variable resistor is at a minimum.



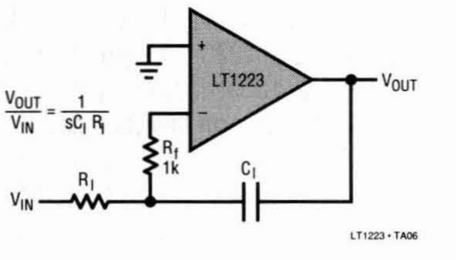
Accurate Bandwidth Limiting The LT1223

It is very common to limit the bandwidth of an op amp by putting a small capacitor in parallel with R_f. DO NOT PUT A SMALL CAPACITOR FROM THE INVERTING INPUT OF A CURRENT FEEDBACK AMPLIFIER TO ANYWHERE ELSE, ESPECIALLY NOT TO THE OUTPUT. The capacitor on the inverting input will cause peaking or oscillations. If you need to limit the bandwidth of a current feedback amplifier, use a resistor and capacitor at the non-inverting input (R1 & C1). This technique will also cancel (to a degree) the peaking caused by stray capacitance at the inverting input. Unfortunately, this will not limit the output noise the way it does for the op amp.



Current Feedback Amplifier Integrator

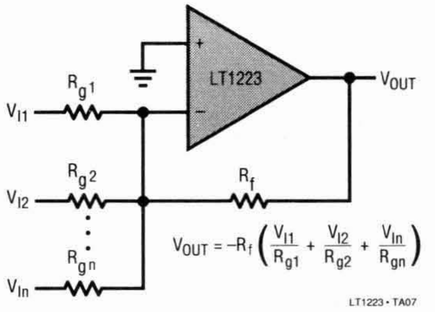
Since we remember that the inverting input wants to see a resistor, we can add one to the standard integrator circuit. This generates a new summing node where we can apply capacitive feedback. The LT1223 integrator has excellent large signal capability and accurate phase shift at high frequencies.



APPLICATIONS INFORMATION

Summing Amplifier (DC Accurate)

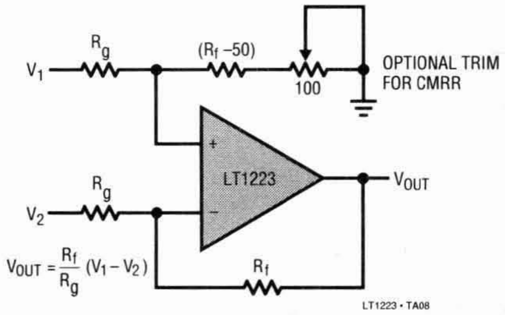
The summing amplifier is easily made by adding additional inputs to the basic inverting amplifier configuration. The LT1223 has no I_{OS} spec because there is no correlation between the two input bias currents. Therefore, we will not improve the DC accuracy of the inverting amplifier by putting in the extra resistor in the non-inverting input.



LT1223
+
–
VOUT
Rg1
VI1
Rg2
VI2
Rf
Rgn
VIn
$V_{OUT} = -R_f\left(\frac{V_{I1}}{R_{g1}} + \frac{V_{I2}}{R_{g2}} + \frac{V_{In}}{R_{gn}}\right)$
LT1223 • TA07

Difference Amplifier

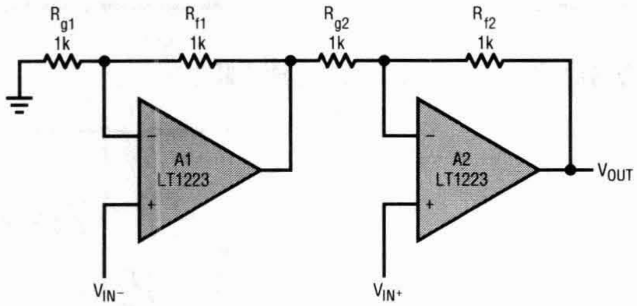
The LT1223 difference amplifier delivers excellent performance if the source impedance is very low. This is because the common mode input resistance is only equal to $R_f + R_g$.



V1
Rg
(Rf –50)
100
OPTIONAL TRIM FOR CMRR
+
LT1223
–
VOUT
V2
Rg
$V_{OUT} = \frac{R_f}{R_g}(V_1 - V_2)$
Rf
LT1223 • TA08

Video Instrumentation Amplifier

This instrumentation amplifier uses two LT1223s to increase the input resistance to well over 1MΩ. This makes an excellent "loop through" or cable sensing amplifier if the inverting input (A1) senses the shield and the non-inverting input (A2) senses the center conductor. Since this amplifier does not load the cable (take care to minimize stray capacitance) and it rejects common mode hum and noise, several amplifiers can sense the signal with only one termination at the end of the cable. The design equations are simple. Just select the gain you need (it should be two or more) and the value of the feedback resistor (typically 1k) and calculate R_{g1} and R_{g2}. The gain can be tweaked with R_{g2} and the CMRR with R_{g1} if needed. The bandwidth of the non-inverting input signal is not reduced by the presence of the other amplifier, however, the inverting input signal bandwidth is reduced since it passes two amplifiers. The CMRR is good at high frequencies because the bandwidth of the amplifiers are about the same even though they do not necessarily operate at the same gain.



Rg1
1k
Rf1
1k
Rg2
1k
Rf2
1k
–
A1
LT1223
+
–
A2
LT1223
+
VOUT
VIN–
VIN+

$V_{OUT} = G\,(V_{IN+} - V_{IN-})$

$R_{f1} = R_{f2};\ R_{g1} = (G - 1)\,R_{f2};\ R_{g2} = \frac{R_{f2}}{G - 1}$

TRIM GAIN (G) WITH R_{g2}; TRIM CMRR WITH R_{g1}

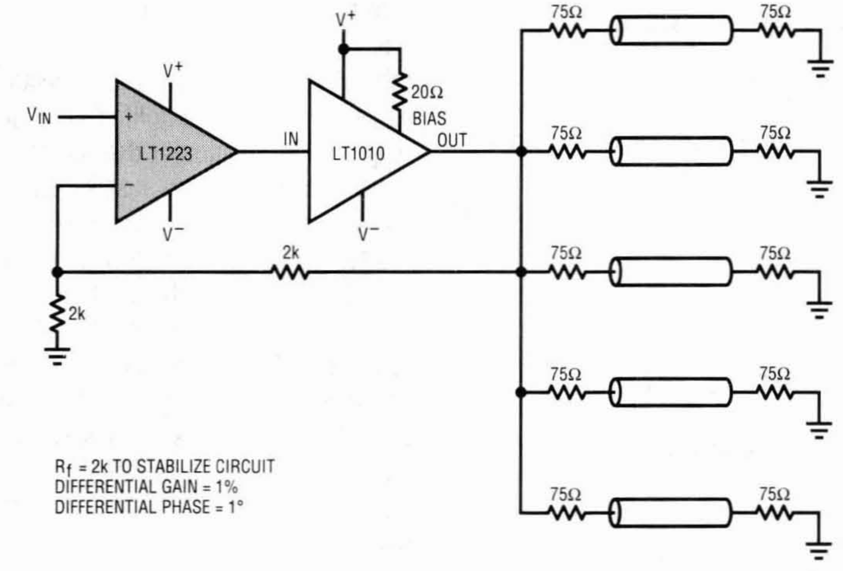
LT1223 • TA09

Cable Driver

The cable driver circuit is shown on the front page. When driving a cable it is important to properly terminate both ends if even modest high frequency performance is required. The additional advantage of this is that it isolates the capacitive load of the cable from the amplifier so it can operate at maximum bandwidth.

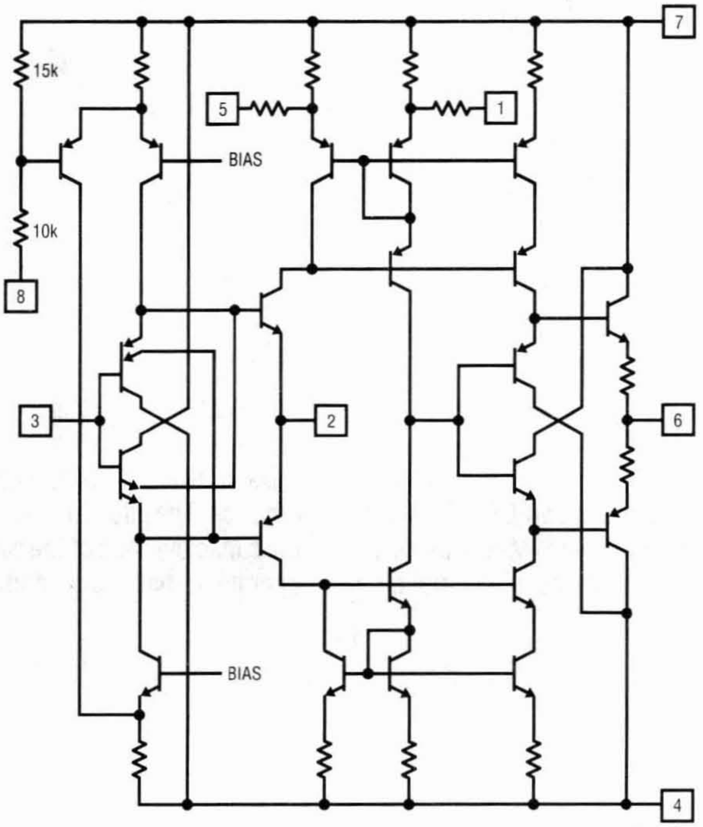
TYPICAL APPLICATION

150mA Output Current Video Amp


VIN
LT1223
V+
V−
IN
LT1010
V+
20Ω
BIAS
OUT
V−
2k
2k
75Ω
75Ω
LT1223 • TA10

R_f = 2k TO STABILIZE CIRCUIT
DIFFERENTIAL GAIN = 1%
DIFFERENTIAL PHASE = 1°

SIMPLIFIED SCHEMATIC


7
15k
5
1
BIAS
10k
8
3
2
6
BIAS
4
LT1223 • TA01

LINEAR TECHNOLOGY

LT1224

Very High Speed Operational Amplifier

FEATURES

- Unity Gain Stable
- 45MHz Gain Bandwidth
- 400V/μs Slew Rate
- 7V/mV DC Gain, $R_L = 500\Omega$
- 2mV Input Offset Voltage
- ±12V Output Swing into 500Ω
- Wide Supply Range ±5V to ±15V
- 7mA Supply Current
- 90ns Settling Time to 0.1%, 10V Step
- Drives All Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

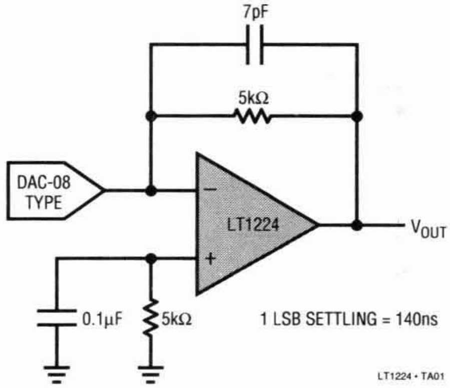
DESCRIPTION

The LT1224 is a very high speed operational amplifier with excellent DC performance. The LT1224 features reduced input offset voltage and higher DC gain than devices with comparable bandwidth and slew rate. The circuit is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. The output is capable of driving a 500Ω load to ±12V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The circuit is also capable of driving large capacitive loads which makes it useful in buffer or cable driver applications.

The LT1224 is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

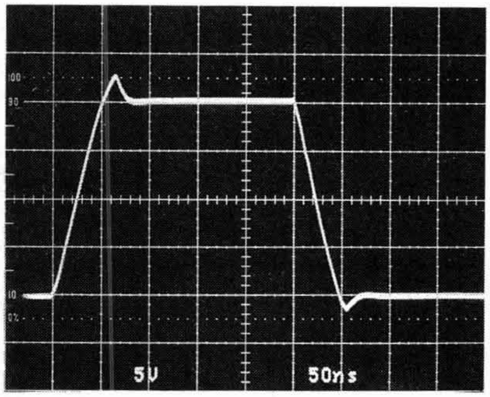
TYPICAL APPLICATION

DAC Current to Voltage Converter



LT1224 • TA01

Inverter Pulse Response

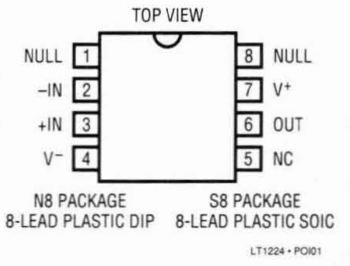


LT1224 • TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage .... ±6V
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range
LT1224C .... 0°C to 70°C
Maximum Junction Temperature
Plastic Package .... 150°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1224CN8 LT1224CS8
S8 PART MARKING
1224

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $R_L = 1k\Omega$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	2.0	mV
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			4	8	μA
e_n	Input Noise Voltage	f = 10kHz		22		nV/√Hz
i_n	Input Noise Current	f = 10kHz		1.5		pA/√Hz
R_{IN}	Input Resistance	$V_{CM} = \pm12V$	24	40		MΩ
	Input Resistance	Differential		250		kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range +		12	14		V
	Input Voltage Range –			−13	−12	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm12V$	86	100		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	75	84		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm10V$, $R_L = 500\Omega$	3.3	7		V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$	12.0	13.3		±V
I_{OUT}	Output Current	$V_{OUT} = \pm12V$	24	40		mA
SR	Slew Rate	$A_{VCL} = -2$, (Note 3)	250	400		V/μs
	Full Power Bandwidth	10V Peak, (Note 4)		6.4		MHz
GBW	Gain Bandwidth	f = 1MHz		45		MHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +1$, 10%-90%, 0.1V		5		ns
	Overshoot	$A_{VCL} = +1$, 0.1V		30		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		5		ns
t_s	Settling Time	10V Step, 0.1%		90		ns
	Differential Gain	f = 3.58MHz, $R_L = 150\Omega$		1.0		%
	Differential Phase	f = 3.58MHz, $R_L = 150\Omega$		2.4		Deg
R_O	Output Resistance	$A_{VCL} = +1$, f = 1MHz		2.5		Ω
I_S	Supply Current			7	9	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm5V$, $T_A = 25°C$, $R_L = 1k\Omega$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		1.0	4.0	mV
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			4	8	μA
	Input Voltage Range +		2.5	4		V
	Input Voltage Range –			–3	–2.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm2.5V$	86	98		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	2.5	7		V/mV
	Large Signal Voltage Gain	$V_{OUT} = \pm2.5V$, $R_L = 150\Omega$		3		V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$	3.0	3.7		±V
	Output Swing	$R_L = 150\Omega$	3.0	3.3		±V
I_{OUT}	Output Current	$V_{OUT} = \pm3V$	20	40		mA
SR	Slew Rate	$A_{VCL} = -2$, (Note 3)		250		V/μs
	Full Power Bandwidth	3V Peak, (Note 4)		13.3		MHz
GBW	Gain Bandwidth	f = 1MHz		34		MHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +1$, 10%-90%, 0.1V		7		ns
	Overshoot	$A_{VCL} = +1$, 0.1V		20		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		7		ns
t_s	Settling Time	–2.5V to 2.5V, 0.1%		90		ns
I_S	Supply Current			7	9	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $R_L = 1k\Omega$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm15V$, (Note 2)		1	4	mV
	Input Offset Voltage	$V_S = \pm5V$, (Note 2)		2	5	mV
	Input V_{OS} Drift			25		μV/°C
I_{OS}	Input Offset Current	$V_S = \pm15V$ and $V_S = \pm5V$		100	600	nA
I_B	Input Bias Current	$V_S = \pm15V$ and $V_S = \pm5V$		4	9	μA
CMRR	Common-Mode Rejection Ratio	$V_S = \pm15V$, $V_{CM} = \pm12V$ and $V_S = \pm5V$, $V_{CM} = \pm2.5V$	83	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	73	84		dB
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 500\Omega$	2.5	7		V/mV
	Large Signal Voltage Gain	$V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	2.0	7		V/mV
V_{OUT}	Output Swing	$V_S = \pm15V$, $R_L = 500\Omega$	12.0	13.3		±V
	Output Swing	$V_S = \pm5V$, $R_L = 500\Omega$ or 150Ω	3.0	3.3		±V
I_{OUT}	Output Current	$V_S = \pm15V$, $V_{OUT} = \pm12V$	24	40		mA
	Output Current	$V_S = \pm5V$, $V_{OUT} = \pm3V$	20	40		mA
SR	Slew Rate	$V_S = \pm15V$, $A_{VCL} = -2$, (Note 3)	250	400		V/μs
I_S	Supply Current	$V_S = \pm15V$ and $V_S = \pm5V$		7	10.5	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

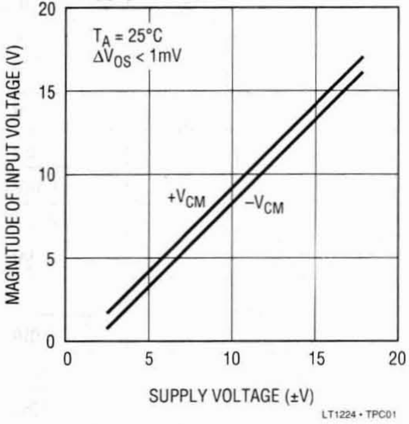
Note 2: Input offset voltage is tested with automated test equipment in <1 second.

Note 3: Slew rate is measured in a gain of –2 between ±10V on the output with ±6V on the input for ±15V supplies and ±2V on the output with ±1.75V on the input for ±5V supplies.

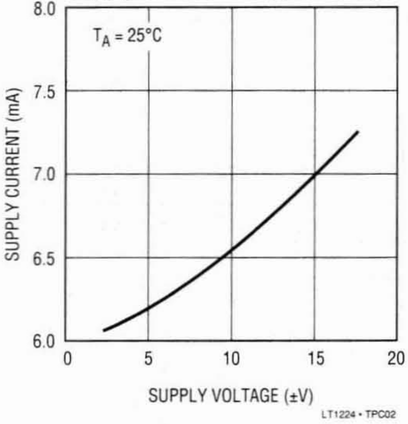
Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi Vp$.

TYPICAL PERFORMANCE CHARACTERISTICS

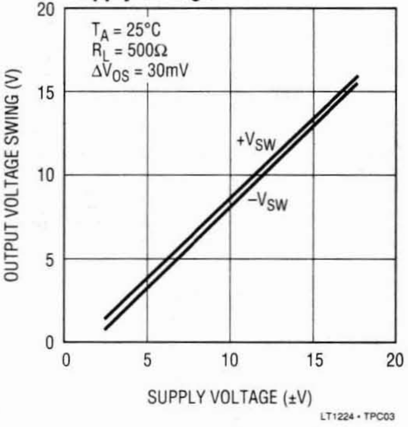
Input Common Mode Range vs Supply Voltage



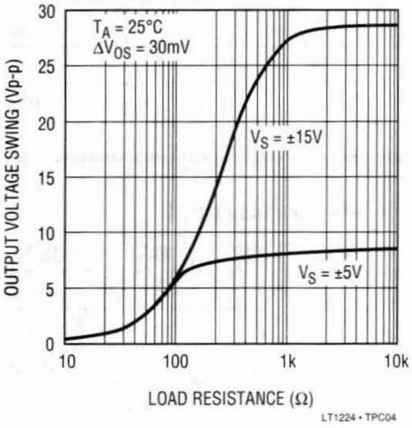
Supply Current vs Supply Voltage



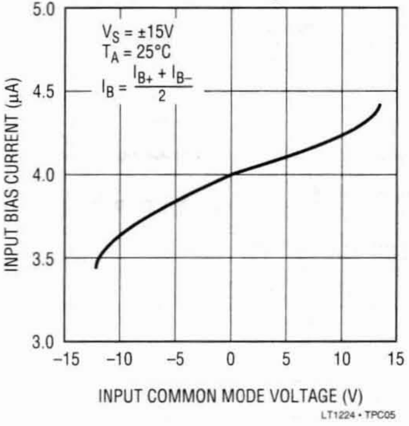
Output Voltage Swing vs Supply Voltage



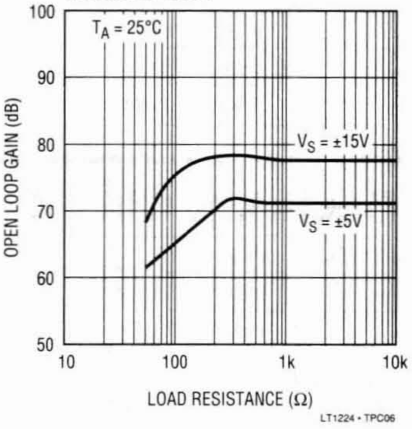
Output Voltage Swing vs Resistive Load



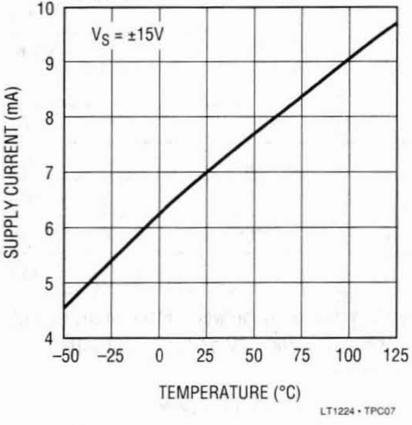
Input Bias Current vs Input Common Mode Voltage



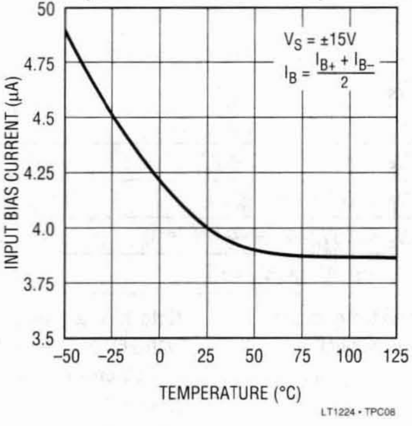
Open Loop Gain vs Resistive Load



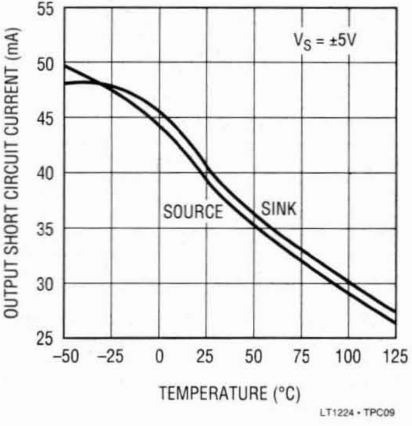
Supply Current vs Temperature



Input Bias Current vs Temperature

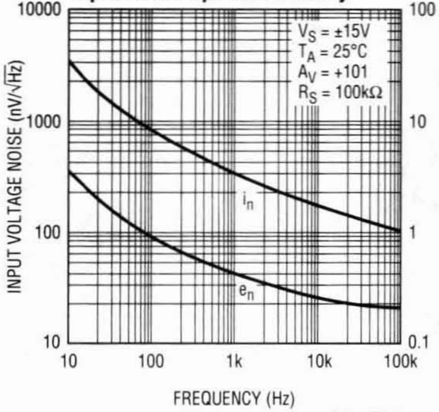


Output Short Circuit Current vs Temperature



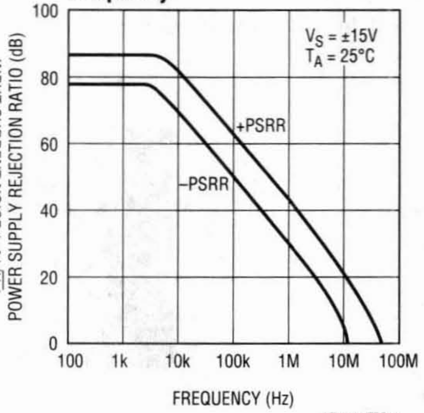
TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise Spectral Density



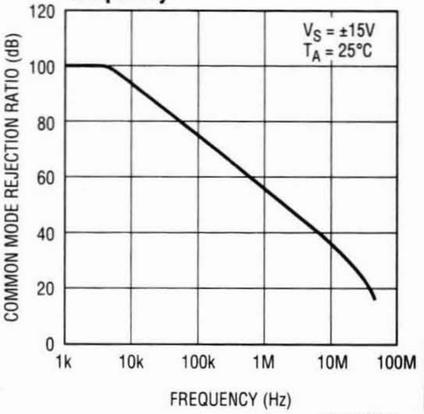
LT1224 • TPC10

Power Supply Rejection Ratio vs Frequency



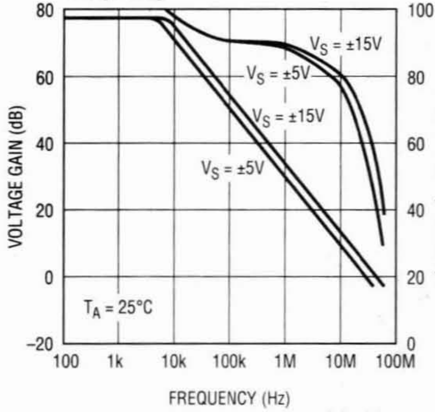
LT1224 • TPC11

Common Mode Rejection Ratio vs Frequency



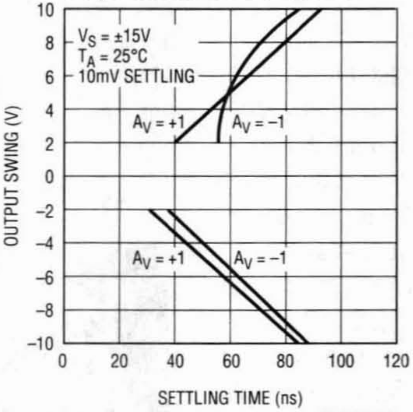
LT1224 • TPC12

Voltage Gain and Phase vs Frequency



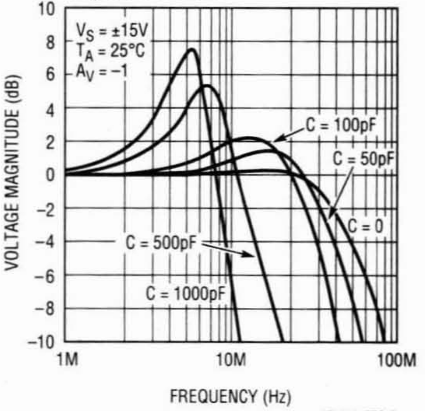
LT1224 • TPC14

Output Swing vs Settling Time



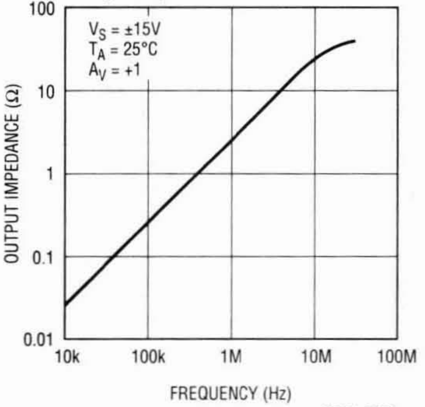
LT1224 • TPC13

Frequency Response vs Capacitive Load



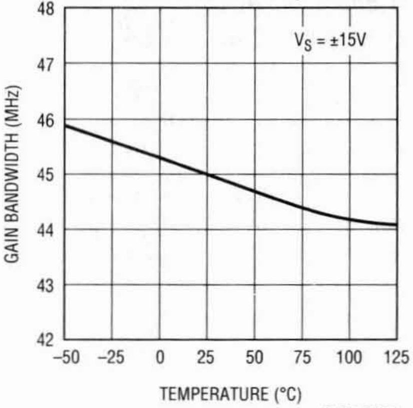
LT1224 • TPC15

Closed Loop Output Impedance vs Frequency



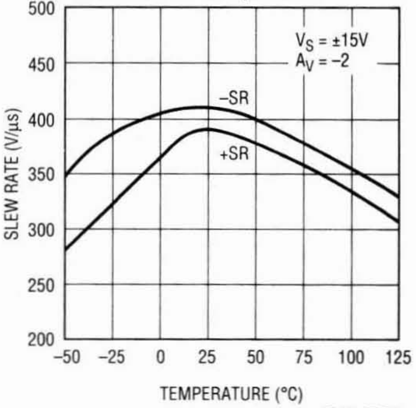
LT1224 • TPC16

Gain Bandwidth vs Temperature



LT1224 • TPC17

Slew Rate vs Temperature

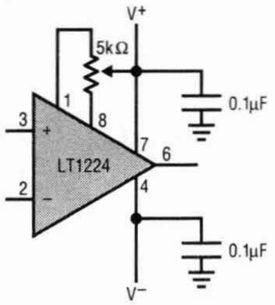


LT1224 • TPC18

APPLICATIONS INFORMATION

The LT1224 may be inserted directly into HA2541, HA2544, AD847, EL2020 and LM6361 applications, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1224 is shown below.

Offset Nulling



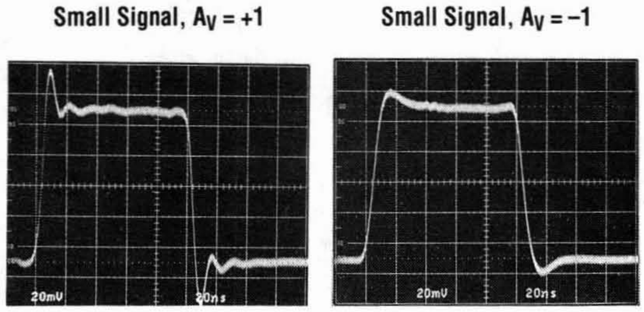
LT1224 • TA03

Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01μF to 0.1μF), and use of low ESR bypass capacitors for high drive current applications (typically 1μF to 10μF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. Feedback resistor values greater than 5kΩ are not recommended because a pole is formed with the input capacitance which can cause peaking. If feedback resistors greater than 5kΩ are used, a parallel capacitor of 5pF to 10pF should be used to cancel the input pole and optimize dynamic performance.

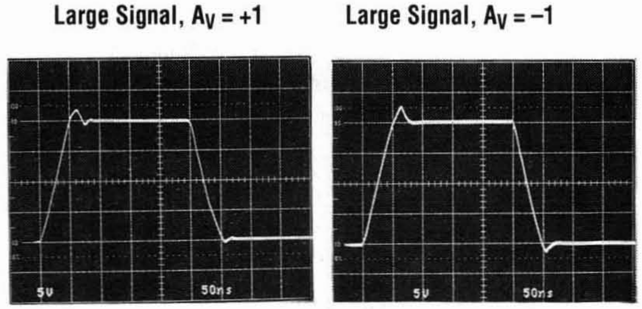
Transient Response

The LT1224 gain bandwidth is 45MHz when measured at f = 1MHz. The actual frequency response in unity gain is considerably higher than 45MHz due to peaking caused by a second pole beyond the unity gain crossover. This is reflected in the 50° phase margin and shows up as overshoot in the unity gain small signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of one response.


Small Signal, $A_V = +1$ **Small Signal, $A_V = -1$**

LT1224 • TA04

The large signal responses in both inverting and non-inverting gain show symmetrical slewing characteristics. Normally the non-inverting response has a much faster rising edge than falling edge due to the rapid change in input common mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1224 so that the non-inverting slew rate response is balanced.


Large Signal, $A_V = +1$ **Large Signal, $A_V = -1$**

LT1224 • TA05

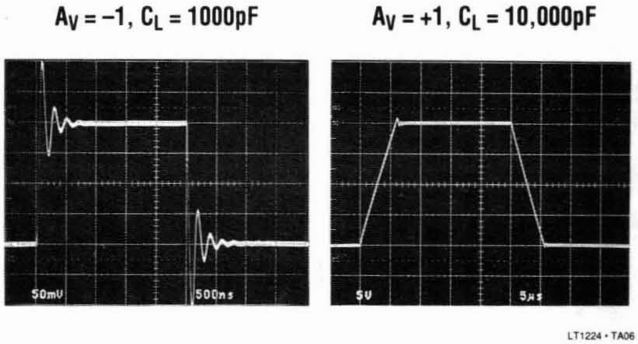
Input Considerations

Resistors in series with the inputs are recommended for the LT1224 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in non-inverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

APPLICATIONS INFORMATION

Capacitive Loading

The LT1224 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. The photo of the small signal response with 1000pF load shows 50% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited by the short circuit current.

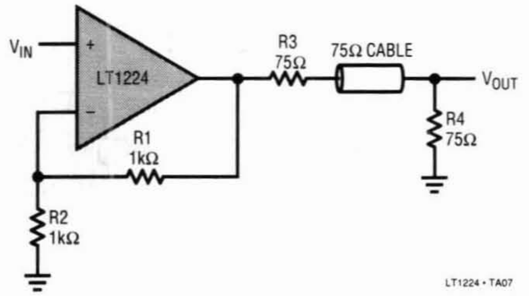


$A_V = -1$, $C_L = 1000pF$

$A_V = +1$, $C_L = 10,000pF$

The LT1224 can drive coaxial cable directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

Cable Driving



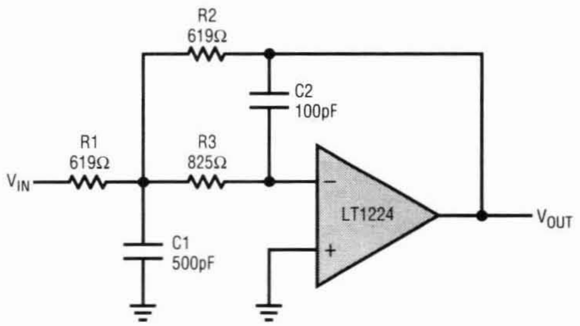
VIN
+
–
LT1224
R3
75Ω
75Ω CABLE
VOUT
R4
75Ω
R1
1kΩ
R2
1kΩ
LT1224 • TA07

DAC Current to Voltage Converter

The wide bandwidth, high slew rate and fast settling time of the LT1224 make it well suited for current to voltage conversion after current output D/A converters. A typical application is shown on page one with a DAC-08 type converter with a full-scale output of 2mA. A compensation capacitor is used across the feedback resistor to null the pole at the inverting input caused by the DAC output capacitance. The combination of the LT1224 and DAC settles to 40mV in 140ns for both a 0V to 10V step and for a 10V to 0V step.

TYPICAL APPLICATIONS

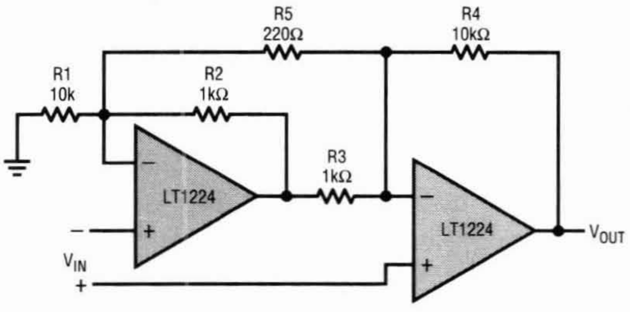
1MHz, 2nd Order Butterworth Filter



R2
619Ω
C2
100pF
R1
619Ω
R3
825Ω
VIN
–
+
LT1224
VOUT
C1
500pF
LT1224 • TA08

–38dB AT 10MHz
SMALL SIGNAL OVERSHOOT = 10%

Two Op Amp Instrumentation Amplifier

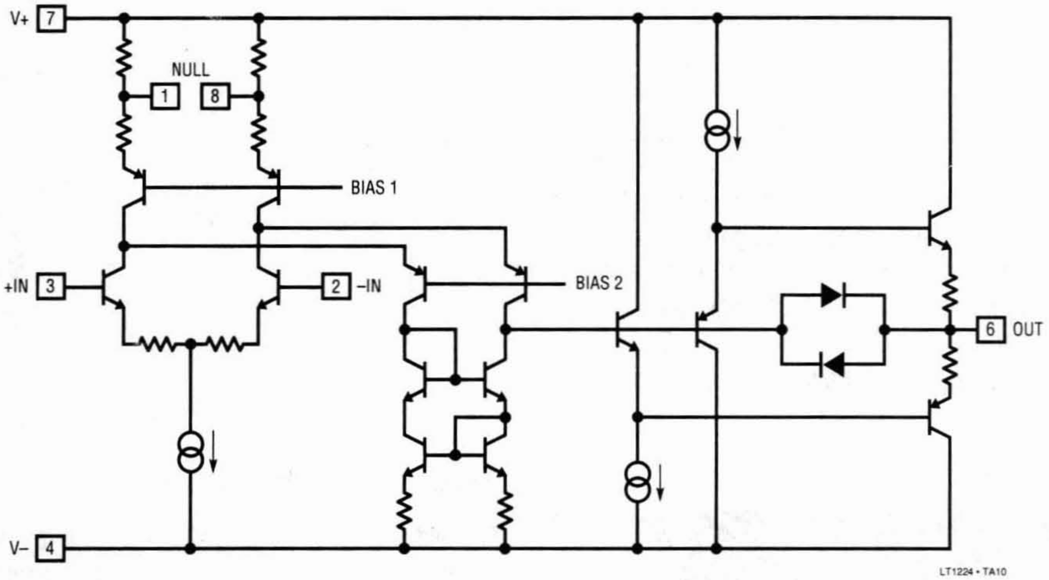


R5
220Ω
R4
10kΩ
R1
10k
R2
1kΩ
R3
1kΩ
–
+
LT1224
LT1224
VIN
–
+
VOUT
LT1224 • TA09

$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 102$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON MODE REJECTION
BW = 430kHz

SIMPLIFIED SCHEMATIC


V+ 7
NULL
1
8
BIAS 1
+IN 3
2 –IN
BIAS 2
6 OUT
V– 4
LT1224 • TA10

LT1225

Very High Speed Operational Amplifier

FEATURES

- Gain of 5 Stable
- 150MHz Gain Bandwidth
- 400V/μs Slew Rate
- 20V/mV DC Gain, $R_L = 500\Omega$
- 1mV Maximum Input Offset Voltage
- ±12V Minimum Output Swing into 500Ω
- Wide Supply Range ±2.5V to ±15V
- 7mA Supply Current
- 90ns Settling Time to 0.1%, 10V Step
- Drives All Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

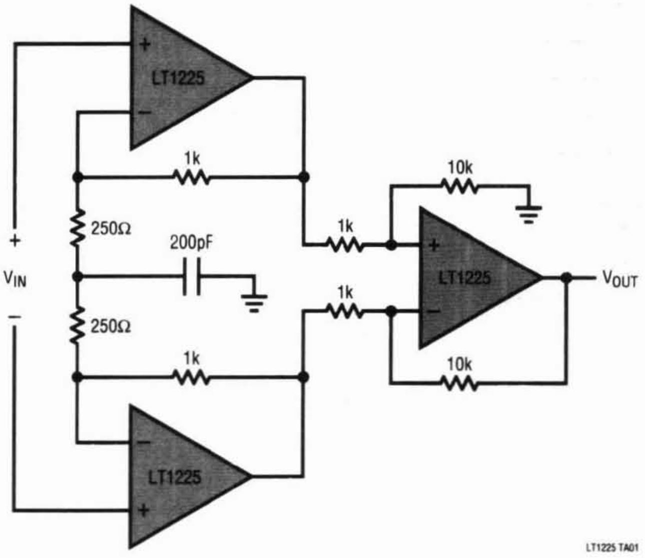
DESCRIPTION

The LT1225 is a very high speed operational amplifier with excellent DC performance. The LT1225 features reduced input offset voltage and higher DC gain than devices with comparable bandwidth and slew rate. The circuit is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. The output is capable of driving a 500Ω load to ±12V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The circuit is also capable of driving large capacitive loads which makes it useful in buffer or cable driver applications.

The LT1225 is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

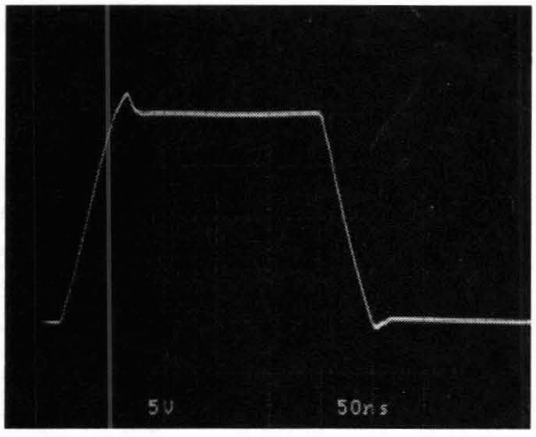
TYPICAL APPLICATION

20MHz, $A_V = 50$ Instrumentation Amplifier



LT1225 TA01

Gain of +5 Pulse Response

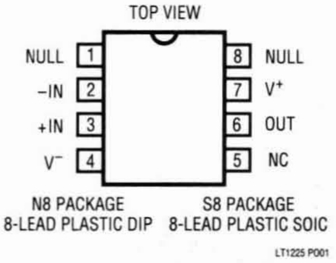


LT1225 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-)	36V
Differential Input Voltage	±6V
Input Voltage	$\pm V_S$
Output Short Circuit Duration (Note 1)	Indefinite
Operating Temperature Range	
LT1225C	0°C to 70°C
Maximum Junction Temperature	
Plastic Package	150°C
Storage Temperature Range	– 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

ORDER PART NUMBER
LT1225CN8 LT1225CS8
S8 PART MARKING
1225

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = 25°C, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.5	1.0	mV
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			4	8	μA
e_n	Input Noise Voltage	f = 10kHz		7.5		nV/√Hz
i_n	Input Noise Current	f = 10kHz		1.5		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = ±12V Differential	24	40 70		MΩ kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range +		12	14		V
	Input Voltage Range –			–13	–12	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V	94	115		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	86	95		dB
A_{VOL}	Large Signal Voltage Gain	V_{OUT} = ±10V, R_L = 500Ω	12.5	20		V/mV
V_{OUT}	Output Swing	R_L = 500Ω	12.0	13.3		±V
I_{OUT}	Output Current	V_{OUT} = ±12V	24	40		mA
SR	Slew Rate	(Note 3)	250	400		V/μs
	Full Power Bandwidth	10V Peak, (Note 4)		6.4		MHz
GBW	Gain Bandwidth	f = 1MHz		150		MHz
t_r, t_f	Rise Time, Fall Time	A_{VCL} = +5, 10% to 90%, 0.1V		7		ns
	Overshoot	A_{VCL} = +5, 0.1V		20		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		7		ns
t_s	Settling Time	10V Step, 0.1%, A_V = –5		90		ns
	Differential Gain	f = 3.58MHz, A_V = +5, R_L = 150Ω		1.0		%
	Differential Phase	f = 3.58MHz, A_V = +5, R_L = 150Ω		1.7		Deg
R_O	Output Resistance	A_{VCL} = +5, f = 1MHz		4.5		Ω
I_S	Supply Current			7	9	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm5V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		1.0	2.0	mV
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			4	8	µA
	Input Voltage Range +		2.5	4		V
	Input Voltage Range –			−3	−2.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm2.5V$	94	115		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm2.5V$, $R_L = 500\Omega$ $V_{OUT} = \pm2.5V$, $R_L = 150\Omega$	10	15 13		V/mV V/mV
V_{OUT}	Output Voltage	$R_L = 500\Omega$ $R_L = 150\Omega$	3.0 3.0	3.7 3.3		±V ±V
I_{OUT}	Output Current	$V_{OUT} = \pm3V$	20	40		mA
SR	Slew Rate	(Note 3)		250		V/µs
	Full Power Bandwidth	3V Peak, (Note 4)		13.3		MHz
GBW	Gain Bandwidth	f = 1MHz		100		MHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +5$, 10% to 90%, 0.1V		9		ns
	Overshoot	$A_{VCL} = +5$, 0.1V		10		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		9		ns
t_s	Settling Time	−2.5V to 2.5V, 0.1%, $A_V = -4$		70		ns
I_S	Supply Current			7	9	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm15V$, (Note 2) $V_S = \pm5V$, (Note 2)		0.5 1.0	1.5 2.5	mV mV
	Input V_{OS} Drift			10		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm15V$ and $V_S = \pm5V$		100	600	nA
I_B	Input Bias Current	$V_S = \pm15V$ and $V_S = \pm5V$		4	9	µA
CMRR	Common-Mode Rejection Ratio	$V_S = \pm15V$, $V_{CM} = \pm12V$ and $V_S = \pm5V$, $V_{CM} = \pm2.5V$	93	115		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	85	95		dB
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 500\Omega$ $V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 500\Omega$	10 8	12.5 10		V/mV V/mV
V_{OUT}	Output Swing	$V_S = \pm15V$, $R_L = 500\Omega$ $V_S = \pm5V$, $R_L = 500\Omega$ or 150Ω	12.0 3.0	13.3 3.3		±V ±V
I_{OUT}	Output Current	$V_S = \pm15V$, $V_{OUT} = \pm12V$ $V_S = \pm5V$, $V_{OUT} = \pm3V$	24 20	40 40		mA mA
SR	Slew Rate	$V_S = \pm15V$, (Note 3)	250	400		V/µs
I_S	Supply Current	$V_S = \pm15V$ and $V_S = \pm5V$		7	10.5	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

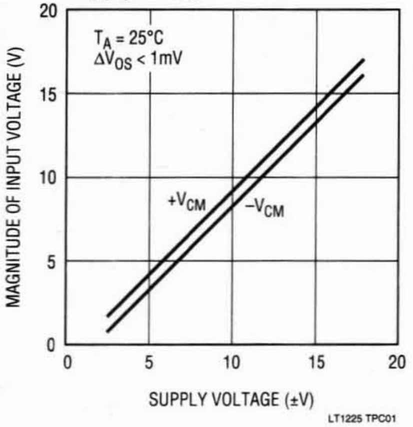
Note 2: Input offset voltage is tested with automated test equipment in <1 second.

Note 3: Slew rate is measured between ±10V on an output swing of ±12V on ±15V supplies, and ±2V on an output swing of ±3.5V on ±5V supplies.

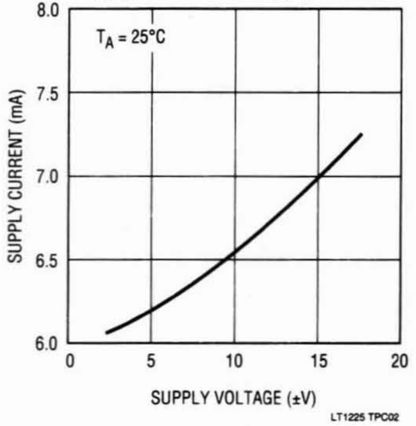
Note 4: Full power bandwidth is calculated from the slew rate measurement: FPBW = SR/2πVp.

TYPICAL PERFORMANCE CHARACTERISTICS

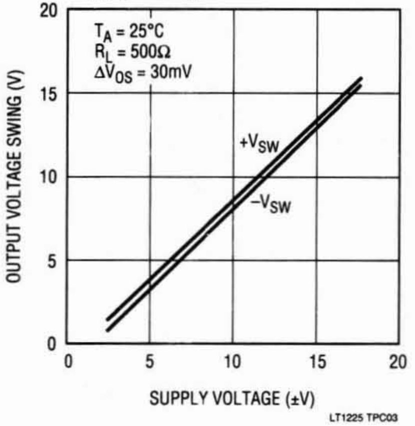
Input Common Mode Range vs Supply Voltage



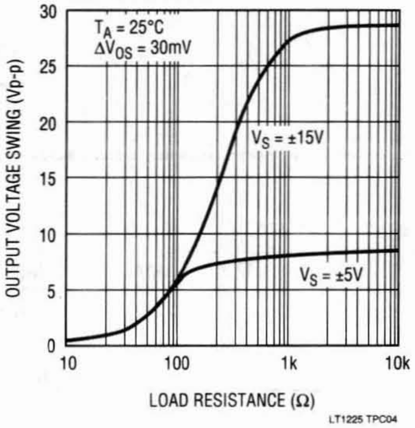
Supply Current vs Supply Voltage



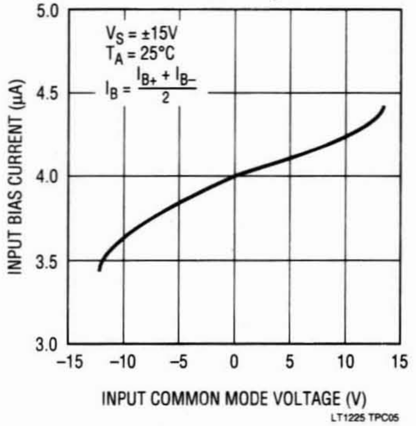
Output Voltage Swing vs Supply Voltage



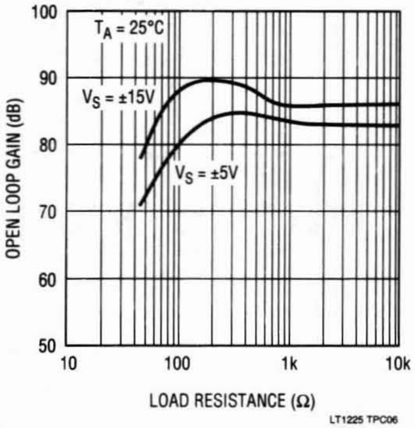
Output Voltage Swing vs Resistive Load



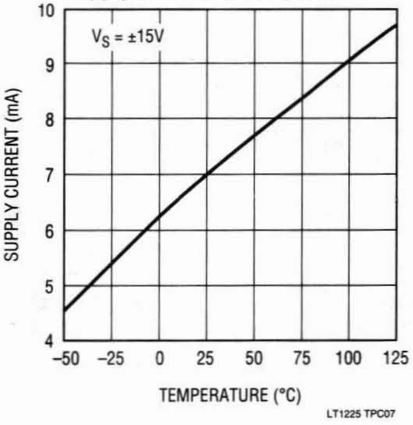
Input Bias Current vs Input Common Mode Voltage



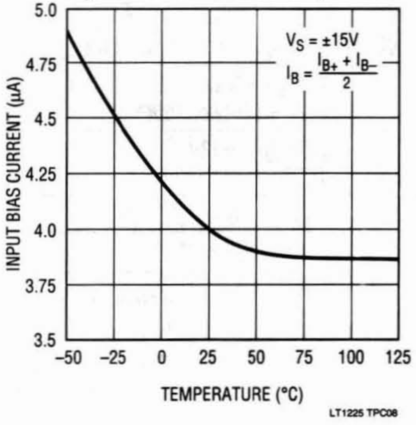
Open Loop Gain vs Resistive Load



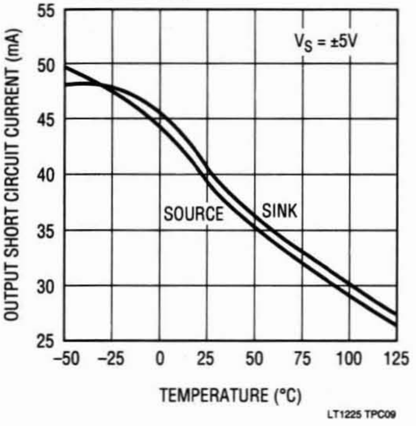
Supply Current vs Temperature



Input Bias Current vs Temperature

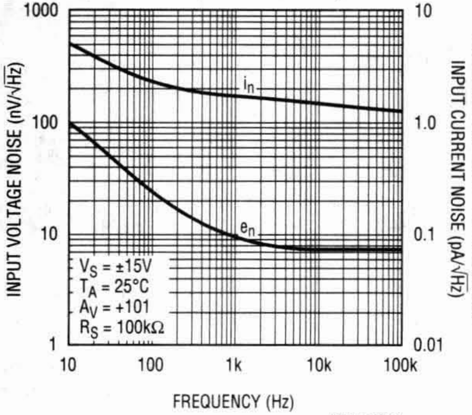


Output Short Circuit Current vs Temperature



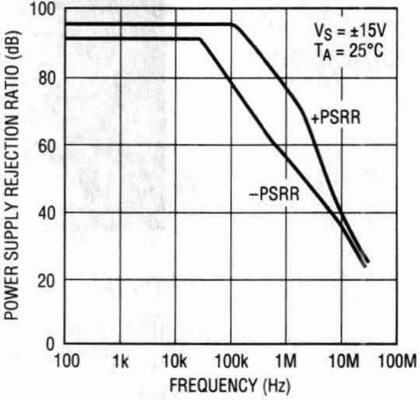
TYPICAL PERFORMANCE CHARACTERISTICS

Input Noise Spectral Density



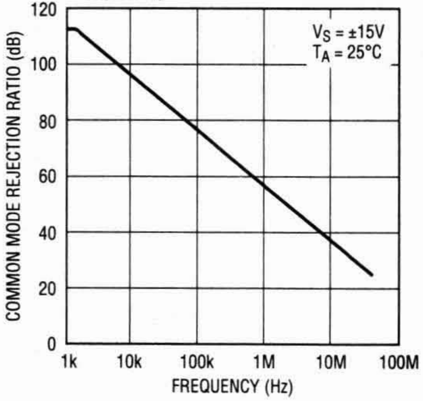
LT1225 TPC10

Power Supply Rejection Ratio vs Frequency



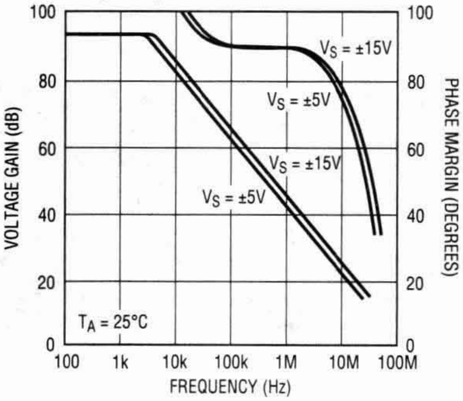
LT1225 TPC11

Common Mode Rejection Ratio vs Frequency



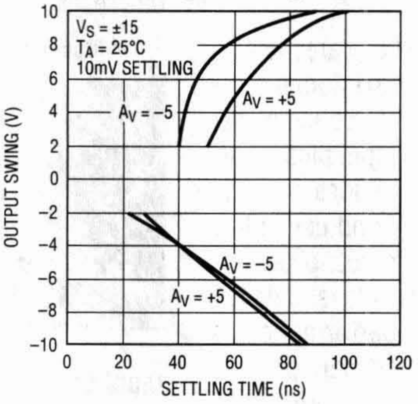
LTXXXX • TPCXX

Voltage Gain and Phase vs Frequency



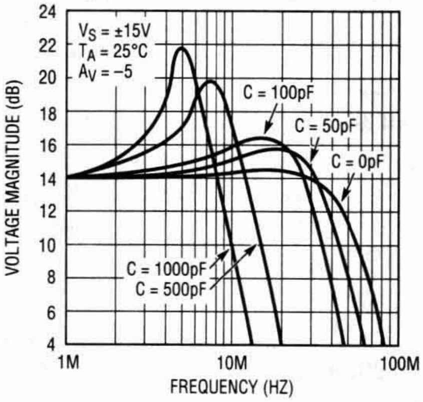
LT1225 TPC13

Output Swing vs Settling Time



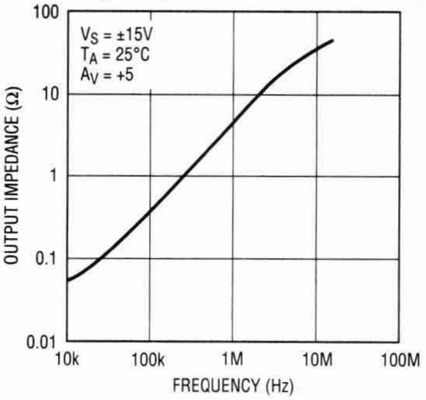
LTC1225 TPC14

Frequency Response vs Capacitive Load



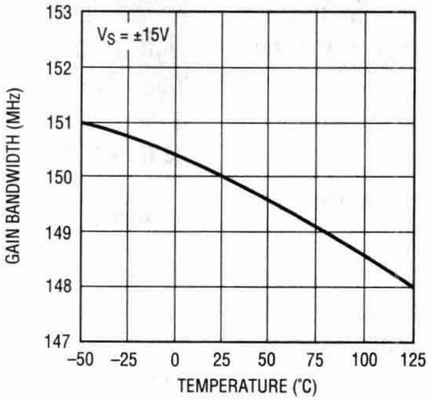
LT1225 TPC15

Closed Loop Output Impedance vs Frequency



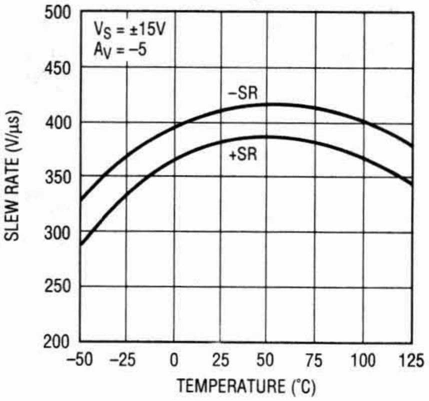
LT1225 TPC16

Gain Bandwidth vs Temperature



LT1225 TPC17

Slew Rate vs Temperature

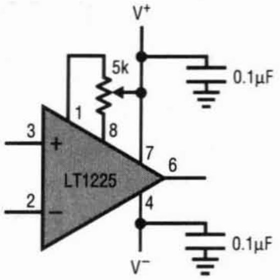


LT1225 TPC18

APPLICATIONS INFORMATION

The LT1225 may be inserted directly into HA2541, HA2544, AD847, EL2020 and LM6361 applications, provided that the amplifier configuration is a noise gain of 5 or greater, and the nulling circuitry is removed. The suggested nulling circuit for the LT1225 is shown below.

Offset Nulling



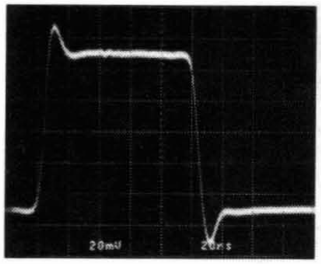
Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF), and use of low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. Feedback resistor values greater than 5kΩ are not recommended because a pole is formed with the input capacitance which can cause peaking. If feedback resistors greater than 5k are used, a parallel capacitor of 5pF to 10pF should be used to cancel the input pole and optimize dynamic performance.

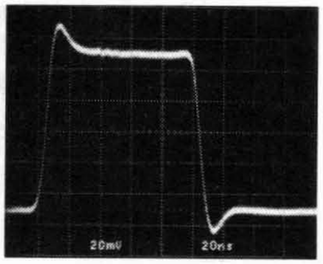
Transient Response

The LT1225 gain bandwidth is 150MHz when measured at 1MHz. The actual frequency response in gain of +5 is considerably higher than 30MHz due to peaking caused by a second pole beyond the gain of 5 crossover point. This is reflected in the small signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of 5 response.

Small Signal, $A_V = +5$

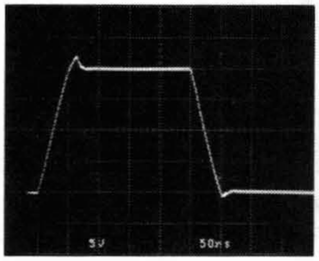


Small Signal, $A_V = -5$

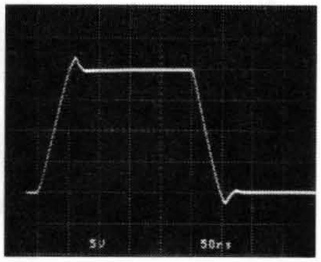


The large signal response in both inverting and noninverting gain shows symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge than falling edge due to the rapid change in input common mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1225 so that the noninverting slew rate response is balanced.

Large Signal, $A_V = +5$



Large Signal, $A_V = -5$



Input Considerations

Resistors in series with the inputs are recommended for the LT1225 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

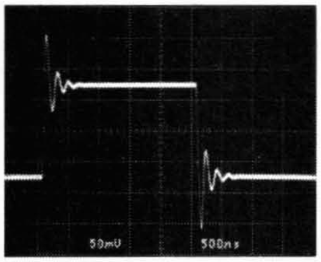
Capacitive Loading

The LT1225 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency

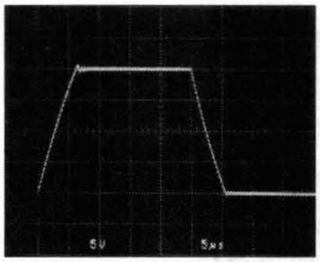
APPLICATIONS INFORMATION

domain and in the transient response. The photo of the small signal response with 1000pF load shows 50% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited by the short circuit current.

$A_V = -5$, $C_L = 1000pF$



$A_V = +5$, $C_L = 10,000pF$



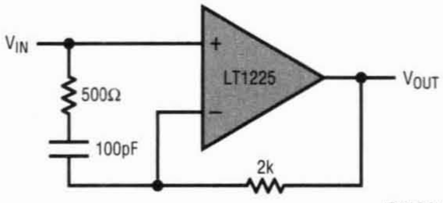
The LT1225 can drive coaxial cable directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

Compensation

The LT1225 has a typical gain bandwidth product of 150MHz which allows it to have wide bandwidth in high gain configurations (i.e., in a gain of 10 it will have a bandwidth of about 15MHz). The amplifier is stable in a noise gain of 5 so the ratio of the output signal to the inverting input must be 1/5 or less. Straightforward gain configurations of +5 or −4 are stable, but there are a few configurations that allow the amplifier to be stable for lower signal gains (the noise gain, however, remains 5 or more). One example is the summing amplifier shown in the typical applications section below. Each input signal has a gain of $-R_F/R_{IN}$ to the output, but it is easily seen that this configuration is equivalent to a gain of −4 as far as the amplifier is concerned. Lag compensation can also be used to give a low frequency gain less than 5 with a high frequency gain of 5 or greater. The example below has a DC gain of one, but an AC gain of +5. The break frequency of the RC combination across the amplifier inputs should be approximately a factor of 10 less than the gain bandwidth of the amplifier divided by the high frequency gain (in this case 1/10 of 150MHz/5 or 3MHz).

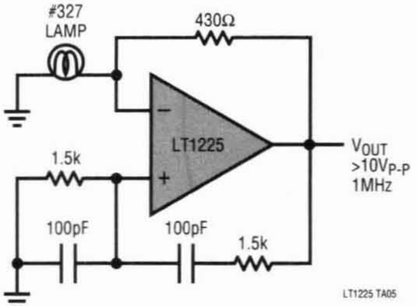
TYPICAL APPLICATIONS

Lag Compensation

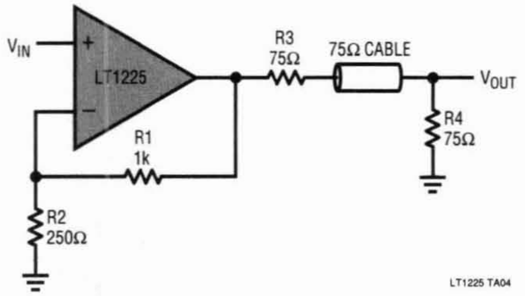

V_{IN}
500Ω
100pF
LT1225
+
−
2k
V_{OUT}
LT1225 TA03

$A_V = +1$, $f < 3MHz$

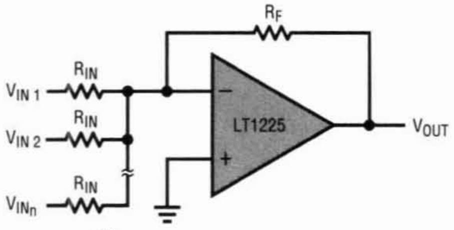
Wein Bridge Oscillator


#327
LAMP
430Ω
LT1225
−
+
1.5k
100pF
100pF
1.5k
V_{OUT}
$>10V_{P-P}$
1MHz
LT1225 TA05

Cable Driving

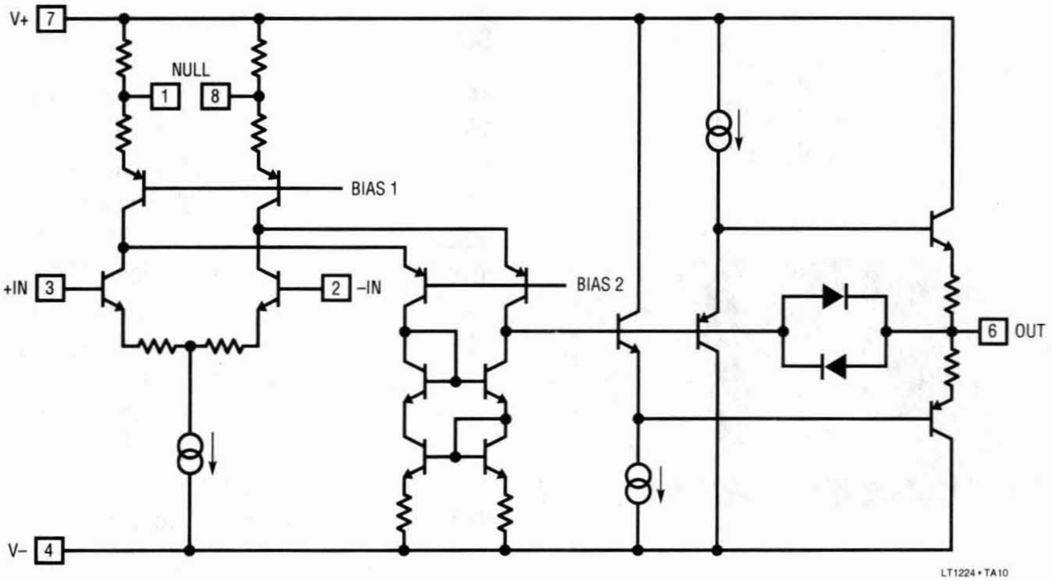

V_{IN}
+
−
LT1225
R3
75Ω
75Ω CABLE
V_{OUT}
R4
75Ω
R1
1k
R2
250Ω
LT1225 TA04

Summing Amplifier


R_F
R_{IN}
$V_{IN 1}$
R_{IN}
$V_{IN 2}$
R_{IN}
V_{IN_n}
LT1225
−
+
V_{OUT}
LT1225 TA06

$R_{IN} = \frac{nR_F}{4}$

SIMPLIFIED SCHEMATIC


V+ 7
NULL
1
8
BIAS 1
+IN 3
2 –IN
BIAS 2
6 OUT
V– 4
LT1224 • TA10

LT1226

Low Noise Very High Speed Operational Amplifier

FEATURES

- Gain of 25 Stable
- 1GHz Gain Bandwidth
- 400V/µs Slew Rate
- 2.6nV/$\sqrt{\text{Hz}}$ Input Noise Voltage
- 50V/mV Minimum DC Gain, R_L = 500Ω
- 1mV Maximum Input Offset Voltage
- ±12V Minimum Output Swing into 500Ω
- Wide Supply Range ±2.5V to ±15V
- 7mA Supply Current
- 100ns Settling Time to 0.1%, 10V Step
- Drives All Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

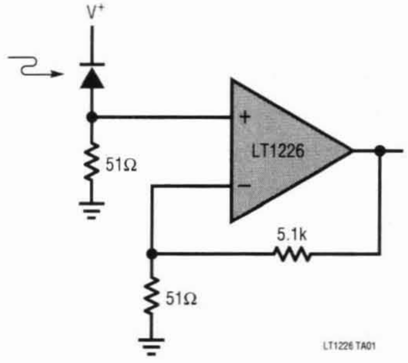
DESCRIPTION

The LT1226 is a low noise, very high speed operational amplifier with excellent DC performance. The LT1226 features low input offset voltage and high DC gain. The circuit is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. The output is capable of driving a 500Ω load to ±12V with ±15V supplies and a 150Ω load to ±3V on ±5V supplies. The circuit is also capable of driving large capacitive loads which makes it useful in buffer or cable driver applications.

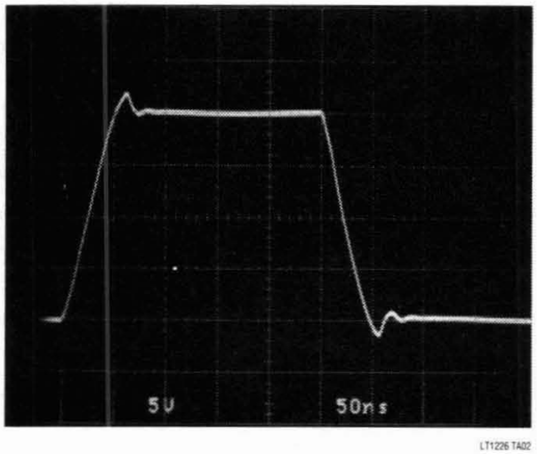
The LT1226 is a member of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

TYPICAL APPLICATION

Photodiode Preamplifier, A_V = 5.1kΩ, BW = 15MHz



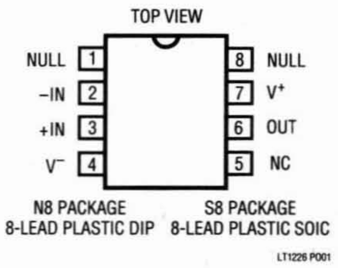
Gain of +25 Pulse Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage .... ±6V
Input Voltage .... $\pm V_S$
Output Short Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range
LT1226C .... 0°C to 70°C
Maximum Junction Temperature
Plastic Package .... 150°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1226CN8 LT1226CS8
S8 PART MARKING
1226

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		0.3	1.0	mV
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			4	8	μA
e_n	Input Noise Voltage	f = 10kHz		2.6		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz		1.5		$pA/\sqrt{Hz}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$ Differential	24	40 15		MΩ kΩ
C_{IN}	Input Capacitance			2		pF
	Input Voltage Range +		12	14		V
	Input Voltage Range –			–13	–12	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$	94	103		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	94	110		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	50	150		V/mV
V_{OUT}	Output Swing	$R_L = 500\Omega$	12.0	13.3		±V
I_{OUT}	Output Current	$V_{OUT} = \pm 12V$	24	40		mA
SR	Slew Rate	(Note 3)	250	400		V/μs
	Full Power Bandwidth	10V Peak, (Note 4)		6.4		MHz
GBW	Gain Bandwidth	f = 1MHz		1		GHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +25$, 10% to 90%, 0.1V		5.5		ns
	Overshoot	$A_{VCL} = +25$, 0.1V		35		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		5.5		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -25$		100		ns
	Differential Gain	f = 3.58MHz, $A_V = +25$, $R_L = 150\Omega$		0.7		%
	Differential Phase	f = 3.58MHz, $A_V = +25$, $R_L = 150\Omega$		0.6		Deg
R_O	Output Resistance	$A_{VCL} = +25$, f = 1MHz		3.1		Ω
I_S	Supply Current			7	9	mA

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, $T_A = 25°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	(Note 2)		1.0	1.4	mV
I_{OS}	Input Offset Current			100	400	nA
I_B	Input Bias Current			4	8	µA
	Input Voltage Range +		2.5	4		V
	Input Voltage Range –			−3	−2.5	V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 2.5V$	94	103		dB
A_{VOL}	Large Signal Voltage Gain	$V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$ $V_{OUT} = \pm 2.5V$, $R_L = 150\Omega$	50	100 75		V/mV V/mV
V_{OUT}	Output Voltage	$R_L = 500\Omega$ $R_L = 150\Omega$	3.0 3.0	3.7 3.3		±V ±V
I_{OUT}	Output Current	$V_{OUT} = \pm 3V$	20	40		mA
SR	Slew Rate	(Note 3)		250		V/µs
	Full Power Bandwidth	3V Peak, (Note 4)		13.3		MHz
GBW	Gain Bandwidth	f = 1MHz		700		MHz
t_r, t_f	Rise Time, Fall Time	$A_{VCL} = +25$, 10% to 90%, 0.1V		8		ns
	Overshoot	$A_{VCL} = +25$, 0.1V		25		%
	Propagation Delay	50% V_{IN} to 50% V_{OUT}		8		ns
t_s	Settling Time	−2.5V to 2.5V, 0.1%, $A_V = -24$		60		ns
I_S	Supply Current			7	9	mA

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm 15V$, (Note 2) $V_S = \pm\ 5V$, (Note 2)		0.3 1.0	1.3 1.8	mV mV
	Input V_{OS} Drift			6		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm 15V$ and $V_S = \pm 5V$		100	600	nA
I_B	Input Bias Current	$V_S = \pm 15V$ and $V_S = \pm 5V$		4	9	µA
CMRR	Common-Mode Rejection Ratio	$V_S = \pm 15V$, $V_{CM} = \pm 12V$ and $V_S = \pm 5V$, $V_{CM} = \pm 2.5V$	92	103		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	92	110		dB
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 500\Omega$ $V_S = \pm 5V$, $V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$	35 35	150 100		V/mV V/mV
V_{OUT}	Output Swing	$V_S = \pm 15V$, $R_L = 500\Omega$ $V_S = \pm 5V$, $R_L = 500\Omega$ or 150Ω	12.0 3.0	13.3 3.3		±V ±V
I_{OUT}	Output Current	$V_S = \pm 15V$, $V_{OUT} = \pm 12V$ $V_S = \pm 5V$, $V_{OUT} = \pm 3V$	24 20	40 40		mA mA
SR	Slew Rate	$V_S = \pm 15V$, (Note 3)	250	400		V/µs
I_S	Supply Current	$V_S = \pm 15V$ and $V_S = \pm 5V$		7	10.5	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

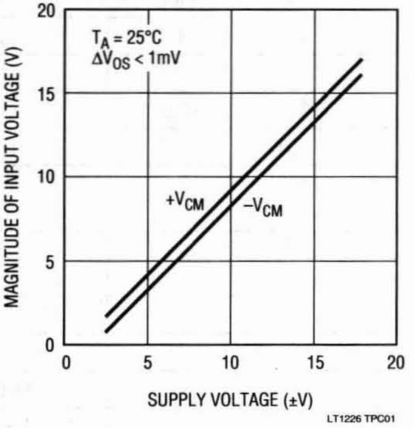
Note 2: Input offset voltage is tested with automated test equipment in <1 second.

Note 3: Slew rate is measured between ±10V on an output swing of ±12V on ±15V supplies, and ±2V on an output swing of ±3.5V on ±5V supplies.

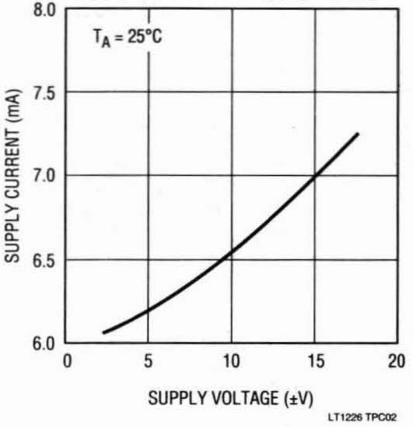
Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi Vp$.

TYPICAL PERFORMANCE CHARACTERISTICS

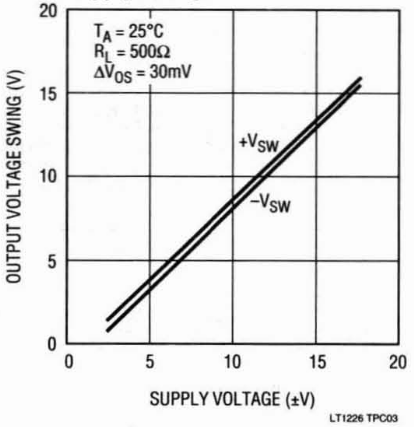
Input Common Mode Range vs Supply Voltage



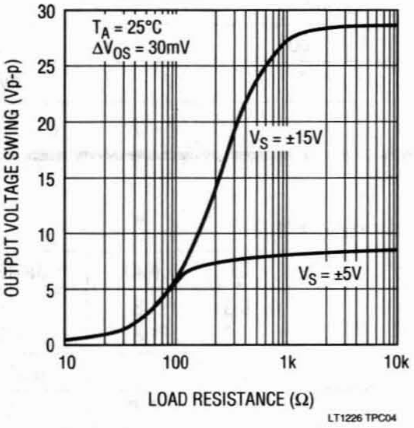
Supply Current vs Supply Voltage



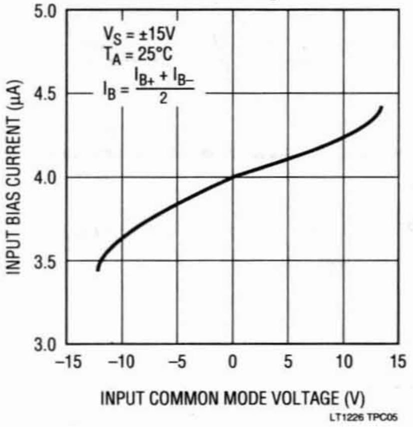
Output Voltage Swing vs Supply Voltage



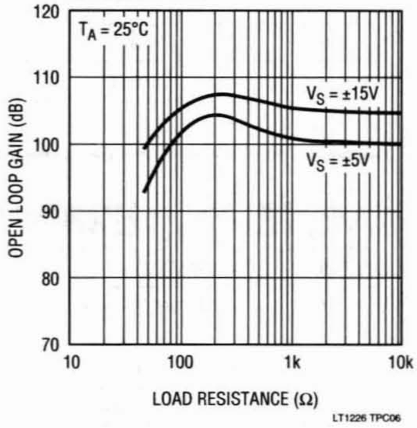
Output Voltage Swing vs Resistive Load



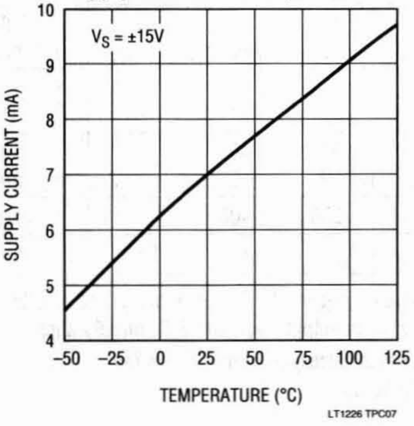
Input Bias Current vs Input Common Mode Voltage



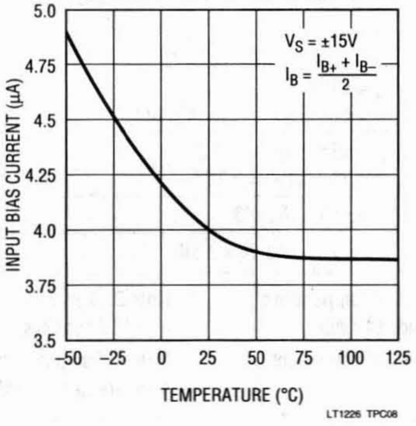
Open Loop Gain vs Resistive Load



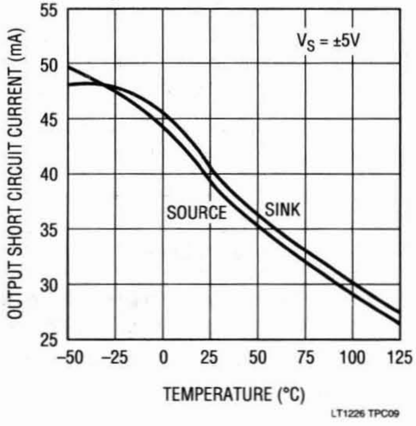
Supply Current vs Temperature



Input Bias Current vs Temperature

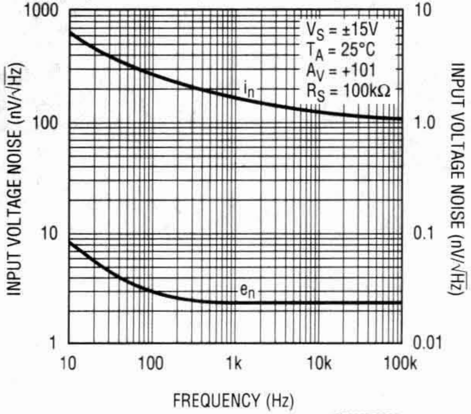


Output Short Circuit Current vs Temperature

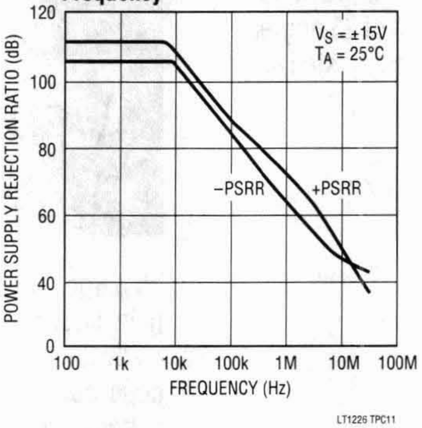


TYPICAL PERFORMANCE CHARACTERISTICS

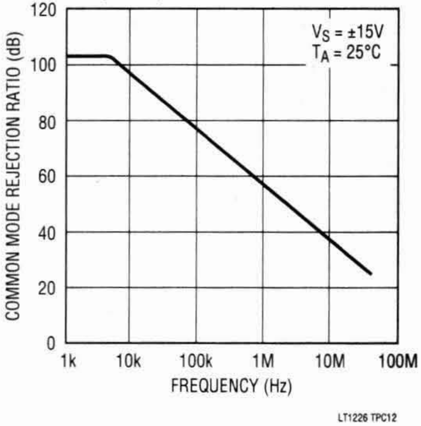
Input Noise Spectral Density



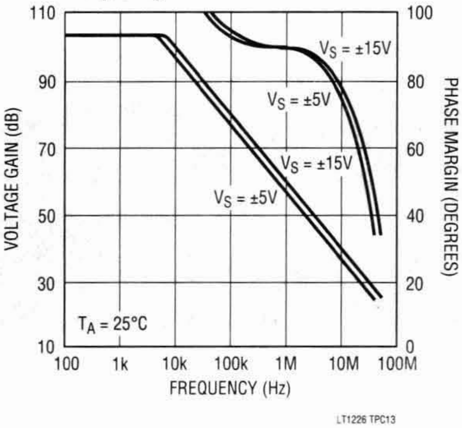
Power Supply Rejection Ratio vs Frequency



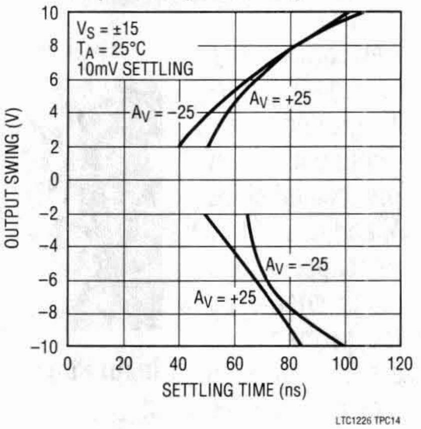
Common Mode Rejection Ratio vs Frequency



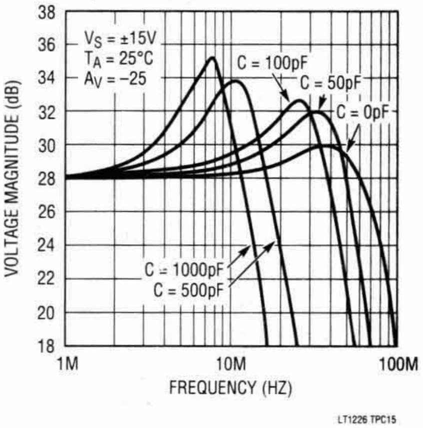
Voltage Gain and Phase vs Frequency



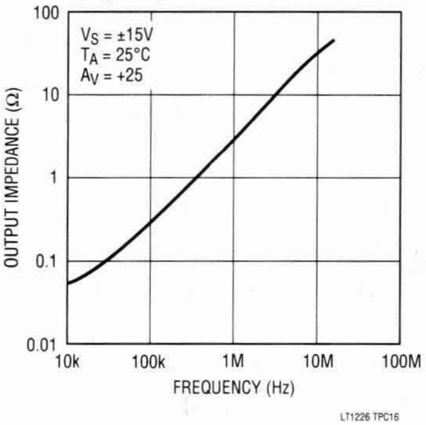
Output Swing vs Settling Time



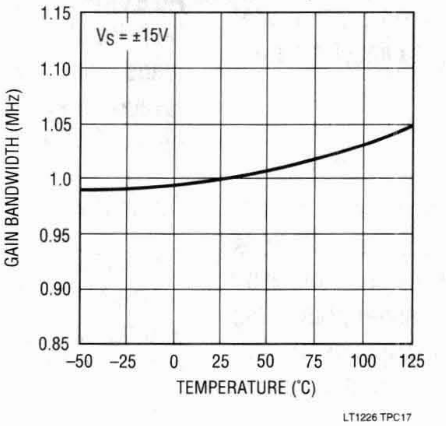
Frequency Response vs Capacitive Load



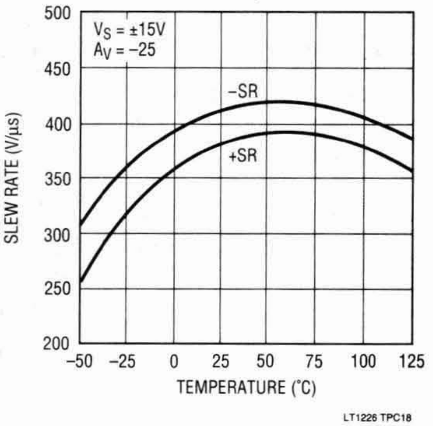
Closed Loop Output Impedance vs Frequency



Gain Bandwidth vs Temperature



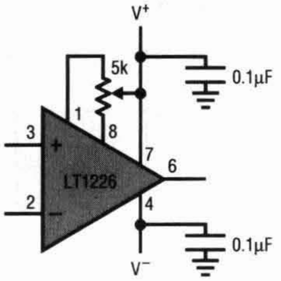
Slew Rate vs Temperature



APPLICATIONS INFORMATION

The LT1226 may be inserted directly into HA2541, HA2544, AD847, EL2020 and LM6361 applications, provided that the amplifier configuration is a noise gain of 25 or greater, and the nulling circuitry is removed. The suggested nulling circuit for the LT1226 is shown below.

Offset Nulling



LT1226 AI01

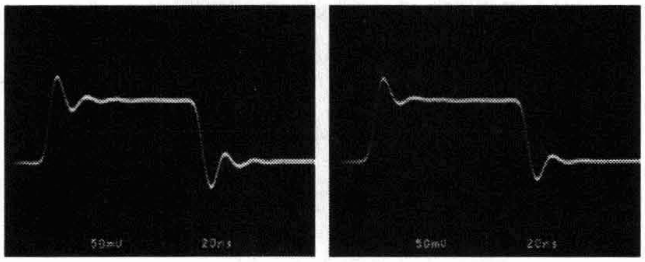
Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF), and use of low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. Feedback resistors greater than 5kΩ are not recommended because a pole is formed with the input capacitance which can cause peaking. If feedback resistors greater than 5kΩ are used, a parallel capacitor of 5pF to 10pF should be used to cancel the input pole and optimize dynamic performance.

Transient Response

The LT1226 gain bandwidth is 1GHz when measured at 1MHz. The actual frequency response in a gain of +25 is considerably higher than 40MHz due to peaking caused by a second pole beyond the gain of 25 crossover point. This is reflected in the small signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of 25 response.

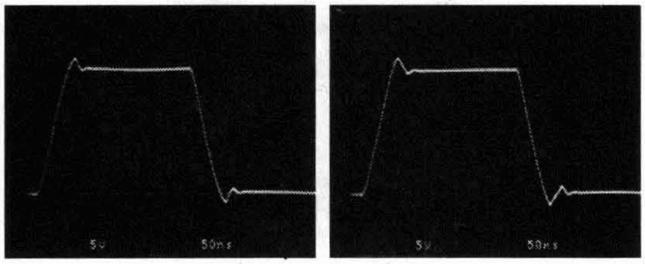
Small Signal, A_V = +25 **Small Signal, A_V = –25**



LT1226 AI02

The large signal response in both inverting and noninverting gain shows symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge due to the rapid change in input common mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1226 so that the falling edge slew rate is enhanced which balances the noninverting slew rate response.

Large Signal, A_V = +25 **Large Signal, A_V = –25**



LT1226 AI03

Input Considerations

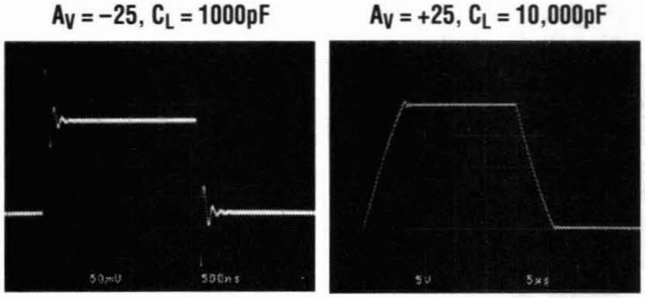
Resistors in series with the inputs are recommended for the LT1226 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

Capacitive Loading

The LT1226 is stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency

APPLICATIONS INFORMATION

domain and in the transient response. The photo of the small signal response with 1000pF load shows 55% peaking. The large signal response with a 10,000pF load shows the output slew rate being limited by the short circuit current.



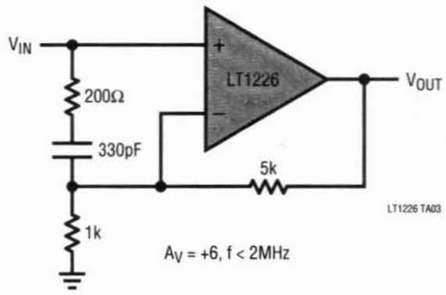
The LT1226 can drive coaxial cable directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output.

Compensation

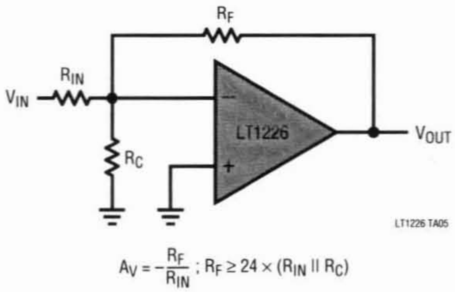
The LT1226 has a typical gain bandwidth product of 1GHz which allows it to have wide bandwidth in high gain configurations (i.e., in a gain of 1000 it will have a bandwidth of about 1MHz). The amplifier is stable in a noise gain of 25 so the ratio of the output signal to the inverting input must be 1/25 or less. Straightforward gain configurations of +25 or −24 are stable, but there are a few configurations that allow the amplifier to be stable for lower signal gains (the noise gain, however, remains 25 or more). One example is the inverting amplifier shown in the typical applications sections below. The input signal has a gain of $-R_F/R_{IN}$ to the output, but it is easily seen that this configuration is equivalent to a gain of −24 as far as the amplifier is concerned. Lag compensation can also be used to give a low frequency gain less than 25 with a high frequency gain of 25 or greater. The example below has a DC gain of 6, but an AC gain of +31. The break frequency of the RC combination across the amplifier inputs should be at least a factor of 10 less than the gain bandwidth of the amplifier divided by the high frequency gain (in this case 1/10 of 1GHz/31 or 3MHz).

TYPICAL APPLICATIONS

Lag Compensation

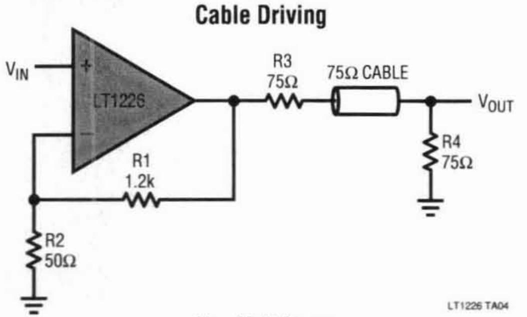

V_{IN}
+
−
LT1226
V_{OUT}
200Ω
330pF
5k
1k
$A_V = +6$, f < 2MHz
LT1226 TA03

Compensation for Lower Closed-Loop Gains

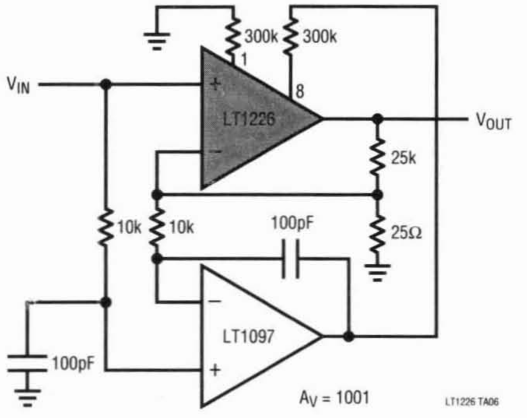

R_F
R_{IN}
V_{IN}
−
+
LT1226
V_{OUT}
R_C
LT1226 TA05

$A_V = -\frac{R_F}{R_{IN}}$; $R_F \ge 24 \times (R_{IN} \parallel R_C)$

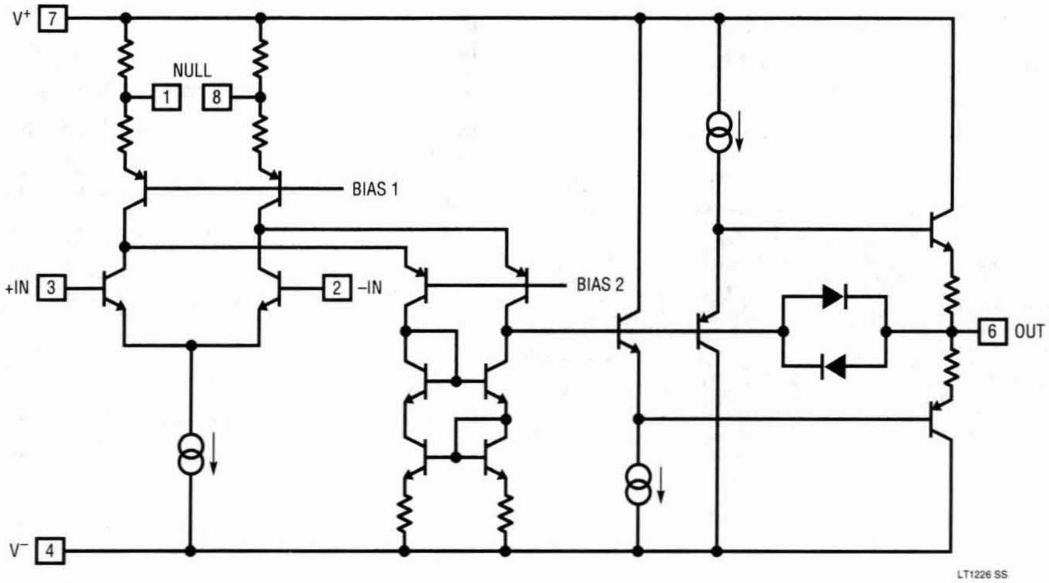
Cable Driving


V_{IN}
+
−
LT1226
R3
75Ω
75Ω CABLE
V_{OUT}
R4
75Ω
R1
1.2k
R2
50Ω
LT1226 TA04

V_{OS} Null Loop


300k
300k
1
8
V_{IN}
+
−
LT1226
V_{OUT}
25k
10k
10k
100pF
25Ω
−
+
LT1097
100pF
$A_V = 1001$
LT1226 TA06

SIMPLIFIED SCHEMATIC


V⁺ 7
NULL
1
8
BIAS 1
+IN 3
2 –IN
BIAS 2
6 OUT
V⁻ 4
LT1226 SS

LINEAR TECHNOLOGY

LT1228

100MHz Current Feedback Amplifier with DC Gain Control

FEATURES

- Very Fast Transconductance Amplifier
  - 75MHz Bandwidth
  - $g_m = 10 \times I_{SET}$
  - Low THD, 0.2% @ $30mV_{RMS}$ Input
  - Wide I_{SET} Range, 1µA to 1mA
- Very Fast Current Feedback Amplifier
  - 100MHz Bandwidth
  - 1000V/µs Slew Rate
  - 30mA Output Drive Current
  - 0.04% Differential Gain
  - 0.1° Differential Phase
  - High Input Impedance, 25MΩ, 6pF
- Wide Supply Range, ±2V to ±15V
- Inputs Common Mode to Within 1.5V of Supplies
- Outputs Swing Within 0.8V of Supplies
- 7mA Supply Current

APPLICATIONS

- Video DC Restore (Clamp) Circuits
- Video Differential Input Amplifiers
- Video Keyer/Fader Amplifiers
- AGC Amplifiers
- Tunable Filters
- Oscillators

DESCRIPTION

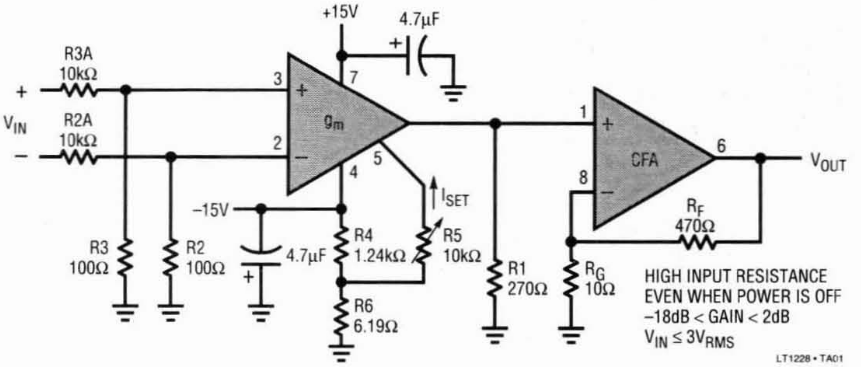
The LT1228 makes it easy to electronically control the gain of signals from DC to video frequencies. The LT1228 implements gain control with a transconductance amplifier (voltage to current) whose gain is proportional to an externally controlled current. A resistor is typically used to convert the output current to a voltage, which is then amplified with a current feedback amplifier. The LT1228 combines both amplifiers into an 8-pin package, and operates on any supply voltage from 4V (±2V) to 30V (±15V). A complete differential input, gain controlled amplifier can be implemented with the LT1228 and just a few resistors.

The LT1228 transconductance amplifier has a high impedance differential input and a current source output with wide output voltage compliance. The transconductance, g_m, is set by the current that flows into pin 5, I_{SET}. The small signal g_m is equal to ten times the value of I_{SET} and this relationship holds over several decades of set current. The voltage at pin 5 is two diode drops above the negative supply, pin 4.

The LT1228 current feedback amplifier has very high input impedance and therefore it is an excellent buffer for the output of the transconductance amplifier. The current feedback amplifier maintains its wide bandwidth over a wide range of voltage gains making it easy to interface the transconductance amplifier output to other circuitry. The current feedback amplifier is designed to drive low impedance loads, such as cables, with excellent linearity at high frequencies.

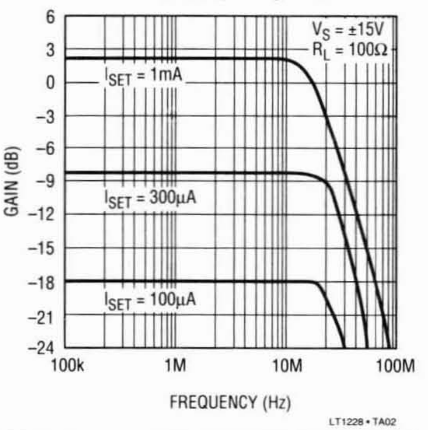
TYPICAL APPLICATION

Differential Input Variable Gain Amp



HIGH INPUT RESISTANCE
EVEN WHEN POWER IS OFF
$-18dB < GAIN < 2dB$
$V_{IN} \le 3V_{RMS}$

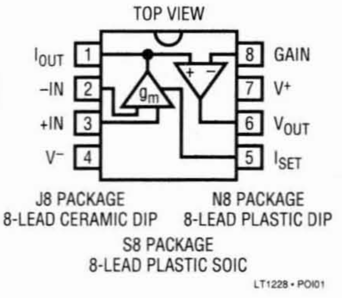
Frequency Response



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ....±18V
Input Current, Pins 1, 2, 3, 5, & 8 ....±15mA
Output Short Circuit Duration (Note 1) ....Continuous
Operating Temperature Range
  LT1228C ....0°C to 70°C
  LT1228M ....−55°C to 125°C
Storage Temperature Range ....−65°C to 150°C
Junction Temperature
  Plastic Package ....150°C
  Ceramic Package ....175°C
Lead Temperature (Soldering, 10 sec.) ....300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1228MJ8 LT1228CJ8 LT1228CN8 LT1228CS8
S8 PART MARKING
1228

ELECTRICAL CHARACTERISTICS

Current Feedback Amplifier

Pins 1, 6, & 8. ±5V ≤ V_S ≤ ±15V, I_{SET} = 0µA, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$T_A = 25°C$			±3	±10	mV
			●			±15	mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{IN+}	Non-Inverting Input Current	$T_A = 25°C$			±0.3	±3	µA
			●			±10	µA
I_{IN-}	Inverting Input Current	$T_A = 25°C$			±10	±65	µA
			●			±100	µA
e_n	Input Noise Voltage Density	f = 1kHz, $R_F = 1kΩ$, $R_G = 10Ω$, $R_S = 0Ω$			6		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz, $R_F = 1kΩ$, $R_G = 10Ω$, $R_S = 10kΩ$			1.4		pA/√Hz
R_{IN}	Input Resistance	$V_{IN} = ±13V$, $V_S = ±15V$	●	2	25		MΩ
		$V_{IN} = ±3V$, $V_S = ±5V$	●	2	25		MΩ
C_{IN}	Input Capacitance (Note 2)	$V_S = ±5V$			6		pF
	Input Voltage Range	$V_S = ±15V$, $T_A = 25°C$		±13	±13.5		V
			●	±12			V
		$V_S = ±5V$, $T_A = 25°C$		±3	±3.5		V
			●	±2			V
CMRR	Common Mode Rejection Ratio	$V_S = ±15V$, $V_{CM} = ±13V$, $T_A = 25°C$		55	69		dB
		$V_S = ±15V$, $V_{CM} = ±12V$	●	55			dB
		$V_S = ±5V$, $V_{CM} = ±3V$, $T_A = 25°C$		55	69		dB
		$V_S = ±5V$, $V_{CM} = ±2V$	●	55			dB
	Inverting Input Current Common Mode Rejection	$V_S = ±15V$, $V_{CM} = ±13V$, $T_A = 25°C$			2.5	10	µA/V
		$V_S = ±15V$, $V_{CM} = ±12V$	●			10	µA/V
		$V_S = ±5V$, $V_{CM} = ±3V$, $T_A = 25°C$			2.5	10	µA/V
		$V_S = ±5V$, $V_{CM} = ±2V$	●			10	µA/V
PSRR	Power Supply Rejection Ratio	$V_S = ±2V$ to $±15V$, $T_A = 25°C$		60	80		dB
		$V_S = ±3V$ to $±15V$	●	60			dB
	Non-Inverting Input Current Power Supply Rejection	$V_S = ±2V$ to $±15V$, $T_A = 25°C$			10	50	nA/V
		$V_S = ±3V$ to $±15V$	●			50	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = ±2V$ to $±15V$, $T_A = 25°C$			0.1	5	µA/V
		$V_S = ±3V$ to $±15V$	●			5	µA/V

ELECTRICAL CHARACTERISTICS Current Feedback Amplifier

Pins 1, 6, & 8. $\pm5V \le V_S \le \pm15V$, $I_{SET} = 0\mu A$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_V	Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_{LOAD} = 1k\Omega$	●	55	65		dB
		$V_S = \pm5V$, $V_{OUT} = \pm2V$, $R_{LOAD} = 150\Omega$	●	55	65		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN}-$	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_{LOAD} = 1k\Omega$	●	100	200		kΩ
		$V_S = \pm5V$, $V_{OUT} = \pm2V$, $R_{LOAD} = 150\Omega$	●	100	200		kΩ
V_{OUT}	Maximum Output Voltage Swing	$V_S = \pm15V$, $R_{LOAD} = 400\Omega$, $T_A = 25°C$		±12	±13.5		V
			●	±10			V
		$V_S = \pm5V$, $R_{LOAD} = 150\Omega$, $T_A = 25°C$		±3	±3.7		V
			●	±2.5			V
I_{OUT}	Maximum Output Current	$R_{LOAD} = 0\Omega$, $T_A = 25°C$		30	65	125	mA
			●	25		125	mA
I_S	Supply Current	$V_{OUT} = 0V$, $I_{SET} = 0V$	●		6	11	mA
SR	Slew Rate (Notes 3 and 5)	$T_A = 25°C$		300	500		V/µs
SR	Slew Rate	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 400\Omega$			3500		V/µs
t_r	Rise Time (Notes 4 and 5)	$T_A = 25°C$			10	20	ns
BW	Small Signal Bandwidth	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 100\Omega$			100		MHz
t_r	Small Signal Rise Time	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 100\Omega$			3.5		ns
	Propagation Delay	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 100\Omega$			3.5		ns
	Small Signal Overshoot	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 100\Omega$			15		%
t_s	Settling Time	0.1%, $V_{OUT} = 10V$, $R_F = 1k\Omega$, $R_G = 1k\Omega$, $R_L = 1k\Omega$			45		ns
	Differential Gain (Note 6)	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 1k\Omega$			0.01		%
	Differential Phase (Note 6)	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 1k\Omega$			0.01		Deg.
	Differential Gain (Note 6)	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 150\Omega$			0.04		%
	Differential Phase (Note 6)	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 150\Omega$			0.1		Deg.

ELECTRICAL CHARACTERISTICS Transconductance Amplifier

Pins 1, 2, 3, & 5. $\pm5V \le V_S \le \pm15V$, $I_{SET} = 100\mu A$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$I_{SET} = 1mA$, $T_A = 25°C$			0.5	5	mV
			●			10	mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$			40	200	nA
			●			500	nA
I_B	Input Bias Current	$T_A = 25°C$			0.4	1	µA
			●			5	µA
e_n	Input Noise Voltage Density	f = 1kHz			20		nV/√Hz
R_{IN}	Input Resistance-Differential Mode	$V_{IN} \approx \pm30mV$	●	30	200		kΩ
	Input Resistance-Common Mode	$V_S = \pm15V$, $V_{CM} = \pm12V$	●	50	1000		MΩ
		$V_S = \pm5V$, $V_{CM} = \pm2V$	●	50	1000		MΩ
C_{IN}	Input Capacitance				3		pF
	Input Voltage Range	$V_S = \pm15V$, $T_A = 25°C$		±13	±14		V
		$V_S = \pm15V$	●	±12			V
		$V_S = \pm5V$, $T_A = 25°C$		±3	±4		V
		$V_S = \pm5V$	●	±2			V

ELECTRICAL CHARACTERISTICS Transconductance Amplifier

Pins 1, 2, 3, & 5. ±5V ≤ V_S ≤ ±15V, I_{SET} = 100µA, V_{CM} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR	Common Mode Rejection Ratio	V_S = ±15V, V_{CM} = ±13V, T_A = 25°C		60	100		dB
		V_S = ±15V, V_{CM} = ±12V	●	60			dB
		V_S = ±5V, V_{CM} = ±3V, T_A = 25°C		60	100		dB
		V_S = ±5V, V_{CM} = ±2V	●	60			dB
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±15V, T_A = 25°C		60	100		dB
		V_S = ±3V to ±15V	●	60			dB
g_m	Transconductance	I_{SET} = 100µA, I_{OUT} = ±30µA, T_A = 25°C		0.75	1.00	1.25	µA/mV
	Transconductance Drift		●		−0.33		%/°C
I_{OUT}	Maximum Output Current	I_{SET} = 100µA	●	70	100	130	µA
I_{OL}	Output Leakage Current	I_{SET} = 0µA (+I_{IN} of CFA), T_A = 25°C			0.3	3	µA
			●			10	µA
V_{OUT}	Maximum Output Voltage Swing	V_S = ±15V , R1 = ∞	●	±13	±14		V
		V_S = ±5V , R1 = ∞	●	±3	±4		V
R_O	Output Resistance	V_S = ±15V, V_{OUT} = ±13V	●	2	8		MΩ
		V_S = ±5V, V_{OUT} = ±3V	●	2	8		MΩ
	Output Capacitance (Note 2)	V_S = ±5V			6		pF
I_S	Supply Current, Both Amps	I_{SET} = 1mA	●		9	15	mA
THD	Total Harmonic Distortion	V_{IN} = 30mV_{RMS} at 1kHz, R1 = 100kΩ			0.2		%
BW	Small Signal Bandwidth	R1 = 50Ω, I_{SET} = 500µA			80		MHz
t_r	Small Signal Rise Time	R1 = 50Ω, I_{SET} = 500µA, 10%-90%			5		ns
	Propagation Delay	R1 = 50Ω, I_{SET} = 500µA, 50%-50%			5		ns

The ● denotes specifications which apply over the operating temperature range.

Note 1: A heatsink may be required depending on the power supply voltage.

Note 2: This is the total capacitance at pin 1. It includes the input capacitance of the current feedback amplifier and the output capacitance of the transconductance amplifier.

Note 3: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with R_F = 1kΩ, R_G = 110Ω and R_L = 400Ω. The slew rate is much higher when the input is overdriven, see the applications section.

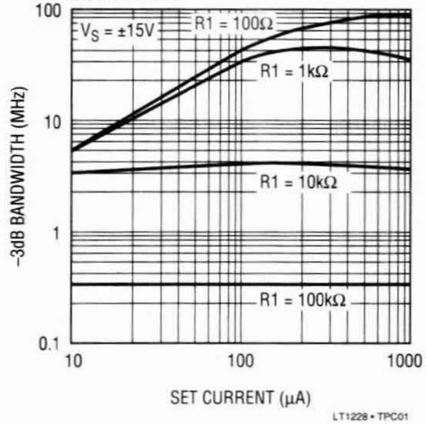
Note 4: Rise time is measured from 10% to 90% on a ±500mV output signal while operating on ±15V supplies with R_F = 1kΩ, R_G = 110Ω and R_L = 100Ω. This condition is not the fastest possible, however, it does guarantee the internal capacitances are correct and it makes automatic testing practical.

Note 5: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

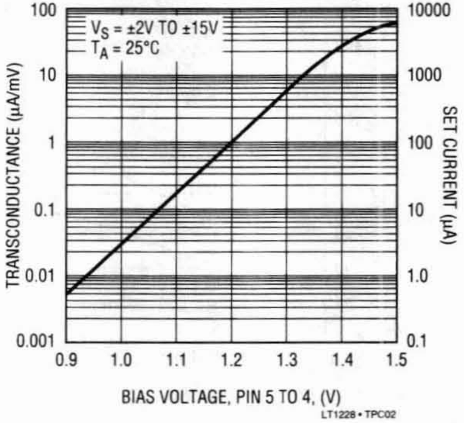
Note 6: NTSC composite video with an output level of 2V.

TYPICAL PERFORMANCE CHARACTERISTICS Transconductance Amplifier, Pins 1, 2, 3 & 5

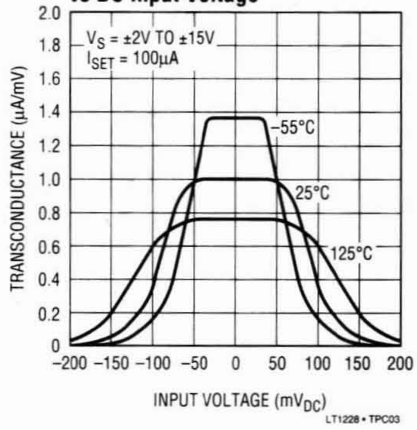
Small Signal Bandwidth vs Set Current



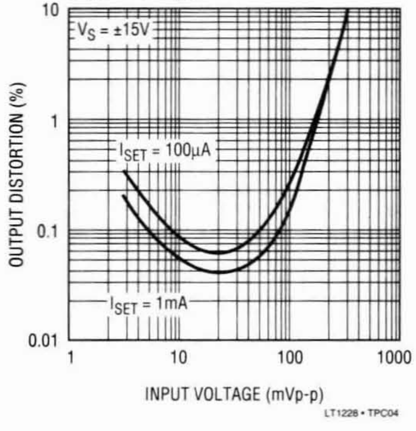
Small Signal Transconductance and Set Current vs Bias Voltage



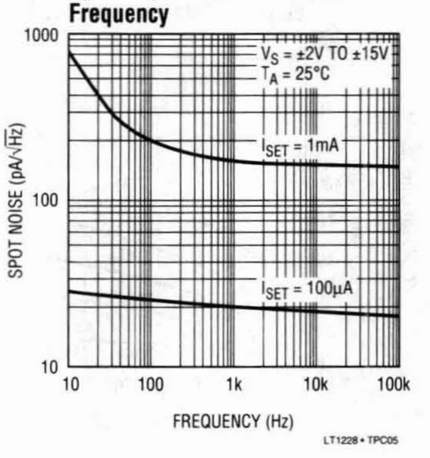
Small Signal Transconductance vs DC Input Voltage



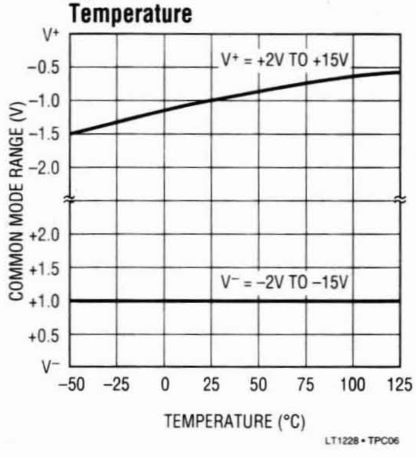
Total Harmonic Distortion vs Input Voltage



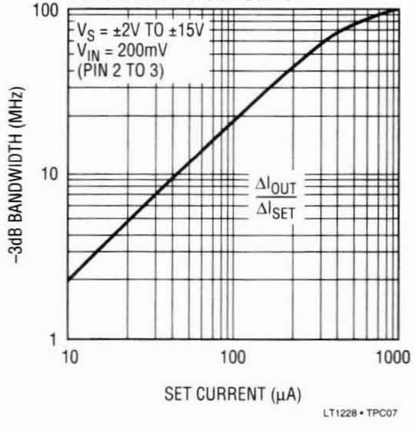
Spot Output Noise Current vs Frequency



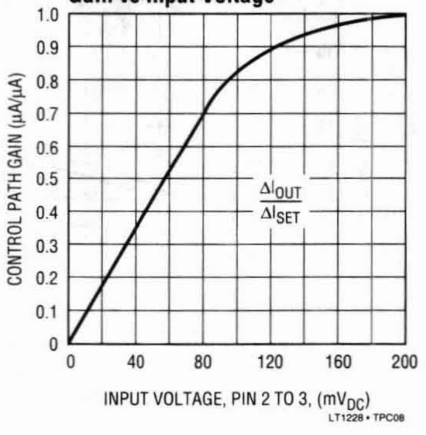
Input Common Mode Limit vs Temperature



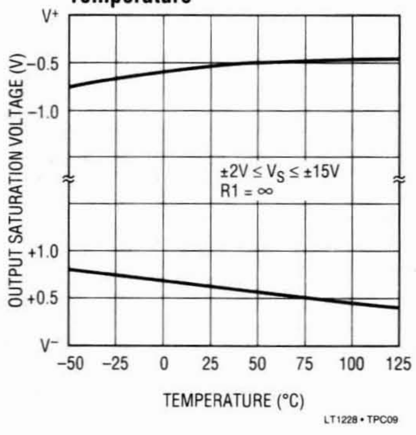
Small Signal Control Path Bandwidth vs Set Current



Small Signal Control Path Gain vs Input Voltage

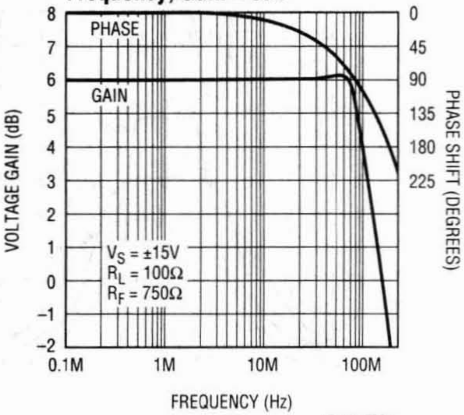


Output Saturation Voltage vs Temperature



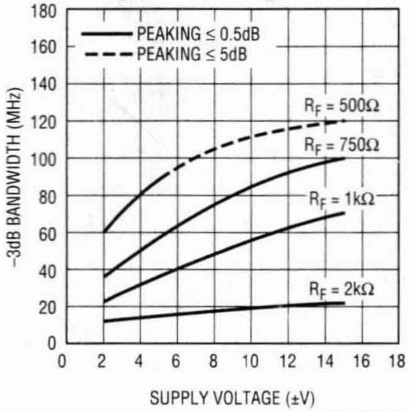
TYPICAL PERFORMANCE CHARACTERISTICS Current Feedback Amplifier, Pins 1, 6 & 8

Voltage Gain and Phase vs Frequency, Gain = 6dB



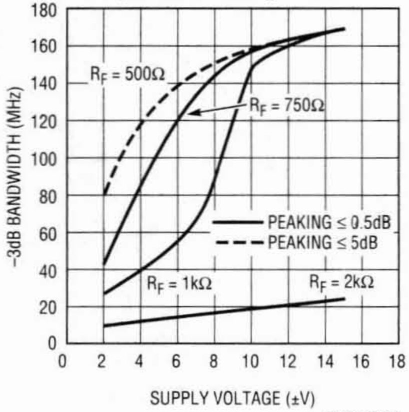
LT1228 • TPC10

–3dB Bandwidth vs Supply Voltage, Gain = 2, $R_L = 100\Omega$



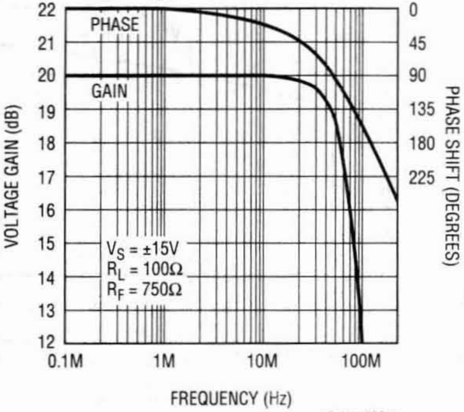
LT1228 • TPC11

–3dB Bandwidth vs Supply Voltage, Gain = 2, $R_L = 1k\Omega$



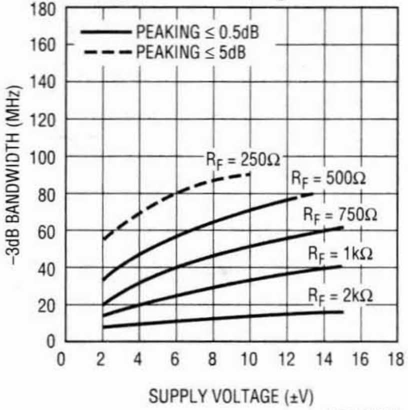
LT1228 • TPC12

Voltage Gain and Phase vs Frequency, Gain = 20dB



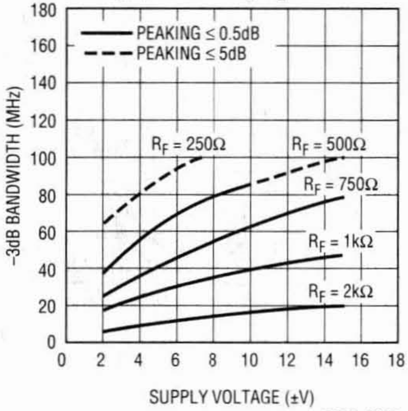
LT1228 • TPC13

–3dB Bandwidth vs Supply Voltage, Gain = 10, $R_L = 100\Omega$



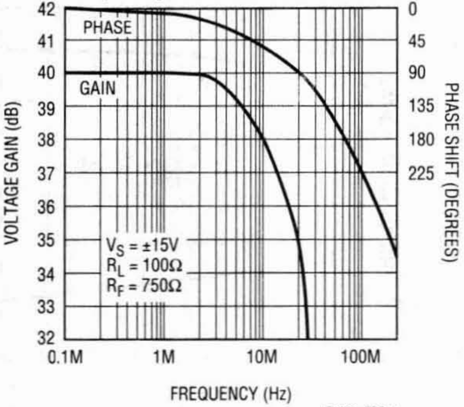
LT1228 • TPC14

–3dB Bandwidth vs Supply Voltage, Gain = 10, $R_L = 1k\Omega$



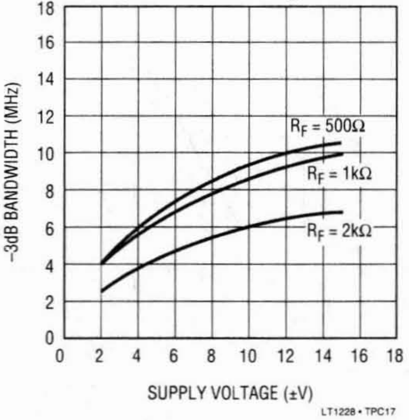
LT1228 • TPC15

Voltage Gain and Phase vs Frequency, Gain = 40dB



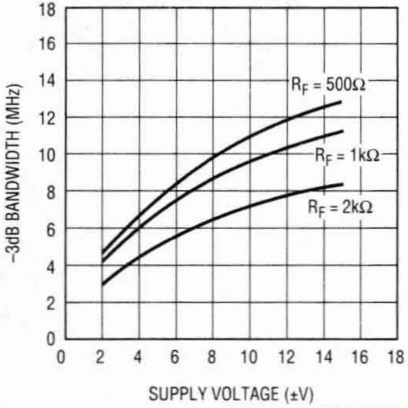
LT1228 • TPC16

–3dB Bandwidth vs Supply Voltage, Gain = 100, $R_L = 100\Omega$



LT1228 • TPC17

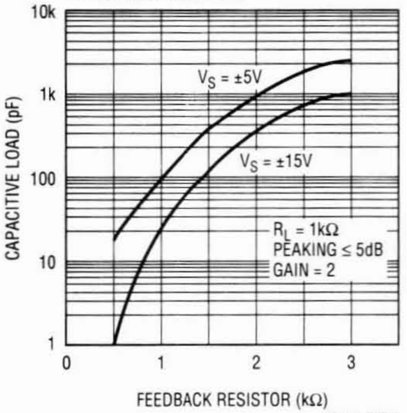
–3dB Bandwidth vs Supply Voltage, Gain = 100, $R_L = 1k\Omega$



LT1228 • TPC18

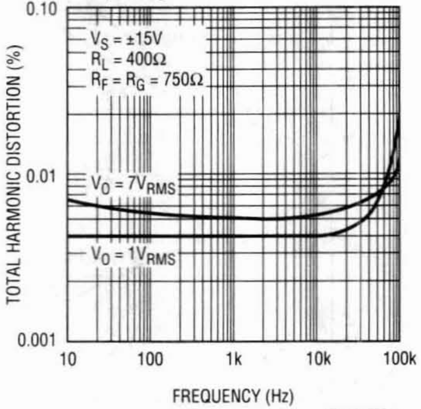
TYPICAL PERFORMANCE CHARACTERISTICS Current Feedback Amplifier, Pins 1, 6 & 8

Maximum Capacitive Load vs Feedback Resistor



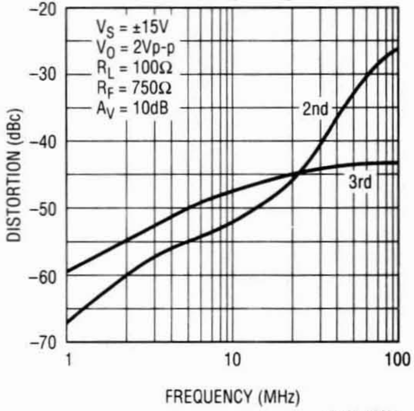
LT1228 • TPC19

Total Harmonic Distortion vs Frequency



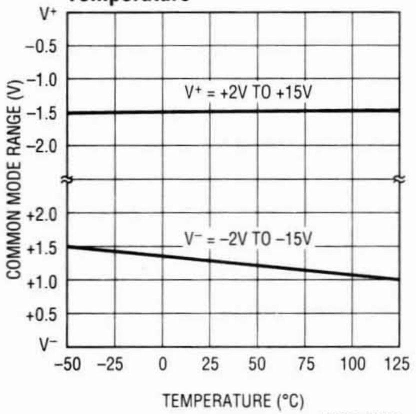
LT1228 • TPC20

2nd and 3rd Harmonic Distortion vs Frequency



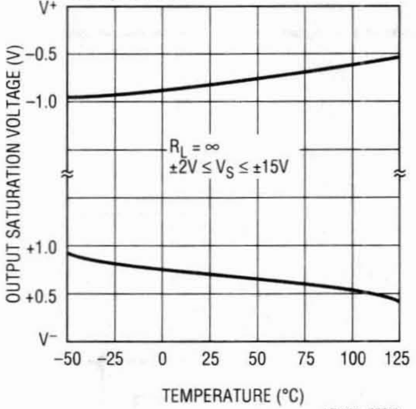
LT1228 • TPC21

Input Common Mode Limit vs Temperature



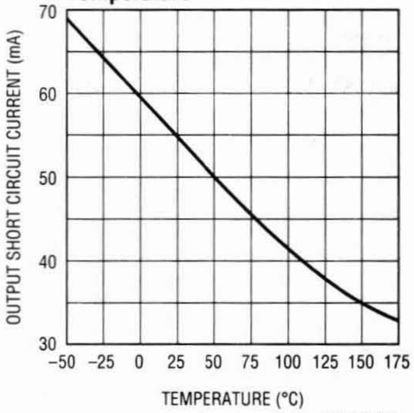
LT1228 • TPC22

Output Saturation Voltage vs Temperature



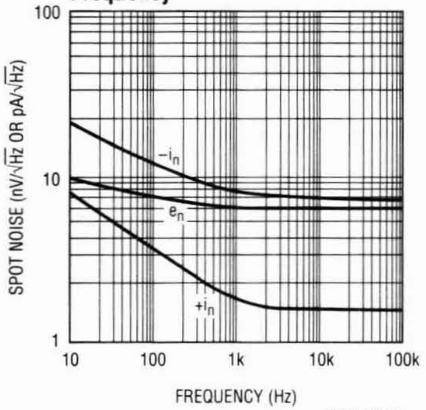
LT1228 • TPC23

Output Short Circuit Current vs Temperature



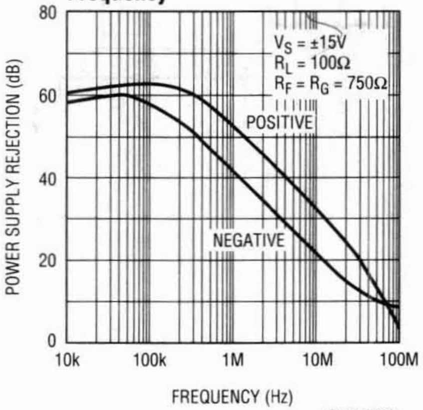
LT1228 • TPC24

Spot Noise Voltage and Current vs Frequency



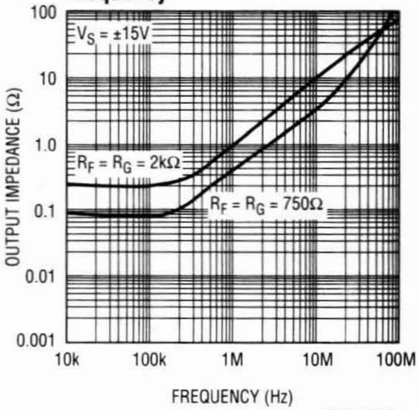
LT1228 • TPC25

Power Supply Rejection vs Frequency



LT1228 • TPC26

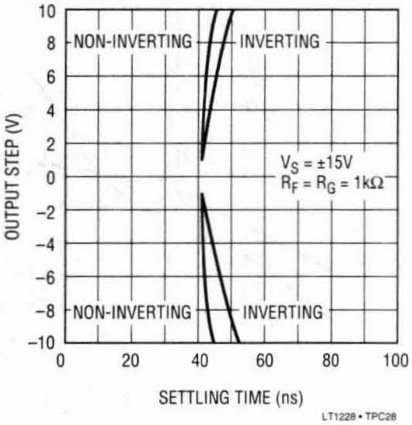
Output Impedance vs Frequency



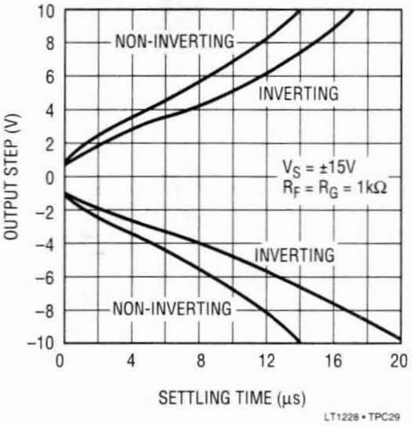
LT1228 • TPC27

TYPICAL PERFORMANCE CHARACTERISTICS Current Feedback Amplifier, Pins 1, 6 & 8

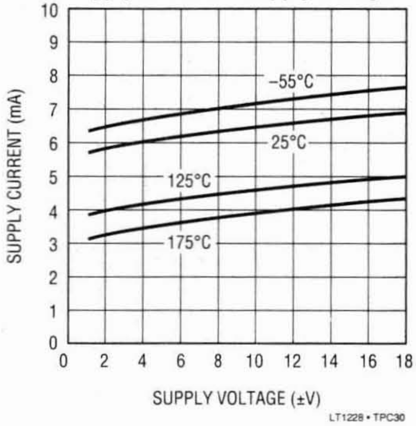
Settling Time to 10mV vs Output Step



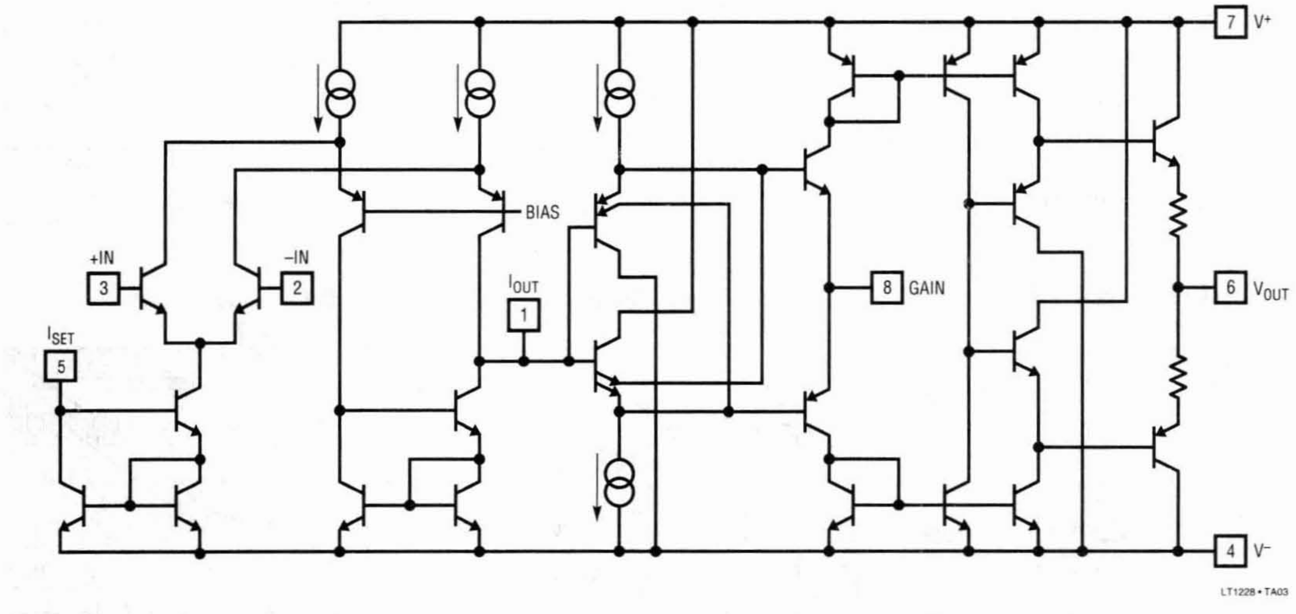
Settling Time to 1mV vs Output Step



Supply Current vs Supply Voltage



SIMPLIFIED SCHEMATIC


7 V+
BIAS
+IN
3
−IN
2
I_{OUT}
1
I_{SET}
5
8 GAIN
6 V_{OUT}
4 V−
LT1228 • TA03

APPLICATIONS INFORMATION

The LT1228 contains two amplifiers, a transconductance amplifier (voltage to current) and a current feedback amplifier (voltage to voltage). The gain of the transconductance amplifier is proportional to the current that is externally programmed into pin 5. Both amplifiers are designed to operate on almost any available supply voltage from 4V (±2V) to 30V (±15V). The output of the transconductance amplifier is connected to the non-inverting input of the current feedback amplifier so that both fit into an eight pin package.

TRANSCONDUCTANCE AMPLIFIER

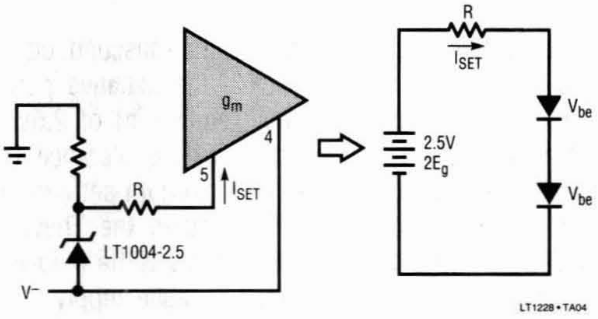
The LT1228 transconductance amplifier has a high impedance differential input (pins 2 and 3) and a current source output (pin 1) with wide output voltage compliance. The voltage to current gain or transconductance (g_m) is set by the current that flows into pin 5, I_{SET}. The voltage at pin 5 is two forward biased diode drops above the negative supply, pin 4. Therefore the voltage at pin 5 (with respect to V–) is about 1.2V and changes with the log of the set current (120mV/decade), see the characteristic curves. The temperature coefficient of this voltage is about –4mV/°C (–3300ppm/°C) and the temperature coefficient of the logging characteristic is +3300ppm/°C. It is important that the current into pin 5 be limited to less than 15mA. THE LT1228 WILL BE DESTROYED IF PIN 5 IS SHORTED TO GROUND OR TO THE POSITIVE SUPPLY. A limiting resistor (2kΩ or so) should be used to prevent more than 15mA from flowing into pin 5.

The small signal transconductance (g_m) is equal to ten times the value of I_{SET} (in mA/mV) and this relationship holds over many decades of set current (see the characteristic curves). The transconductance is inversely proportional to absolute temperature (–3300ppm/°C). The input stage of the transconductance amplifier has been designed to operate with much larger signals than is possible with an ordinary diff-amp. The transconductance of the input stage varies much less than 1% for differential input signals over a ±30 mV range (see the characteristic curve Small Signal Transconductance vs DC Input Voltage).

Resistance Controlled Gain

If the set current is to be set or varied with a resistor or potentiometer it is possible to use the negative temperature coefficient at pin 5 (with respect to pin 4) to compensate for the negative temperature coefficient of the transconductance. The easiest way is to use an LT1004-2.5, a 2.5V reference diode, as shown below:

Temperature Compensation of gm with a 2.5V Reference



The current flowing into pin 5 has a positive temperature coefficient that cancels the negative coefficient of the transconductance. The following derivation shows why a 2.5V reference results in zero gain change with temperature:

$$\text{Since } g_m = \frac{q}{kT} \times \frac{I_{SET}}{3.87} = 10 \times I_{SET}$$

$$\text{and } V_{be} = E_g - \frac{akT}{q} \text{ where } a = \ln\left(\frac{cT^n}{Ic}\right) \approx 19.4 \text{ at } 27^\circ C$$

$$(c = 0.001, n = 3, Ic = 100\mu A)$$

E_g is about 1.25V so the 2.5V reference is $2E_g$. Solving the loop for the set current gives:

$$I_{SET} = \frac{2E_g - 2\left(E_g - \frac{akT}{q}\right)}{R} \text{ or } I_{SET} = \frac{2akT}{Rq}$$

APPLICATIONS INFORMATION

Substituting into the equation for transconductance gives:

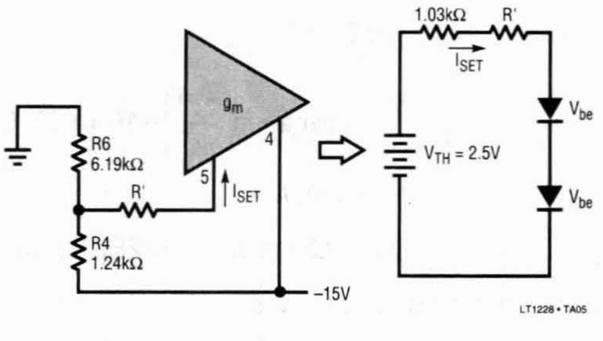
$$g_m = \frac{a}{1.94R} = \frac{10}{R}$$

The temperature variation in the term "a" can be ignored since it is much less than that of the term "T" in the equation for V_{be}. Using a 2.5V source this way will maintain the gain constant within 1% over the full temperature range of –55°C to +125°C. If the 2.5V source is off by 10%, the gain will vary only about ±6% over the same temperature range.

We can also temperature compensate the transconductance without using a 2.5V reference if the negative power supply is regulated. A Thevenin equivalent of 2.5V is generated from two resistors to replace the reference. The two resistors also determine the maximum set current, approximately $1.1V/R_{TH}$. By rearranging the Thevenin equations to solve for R4 and R6 we get the following equations in terms of R_{TH} and the negative supply, V_{EE}.

$$R4 = \frac{R_{TH}}{\left(1 - \frac{2.5V}{V_{EE}}\right)} \text{ and } R6 = \frac{R_{TH}V_{EE}}{2.5V}$$

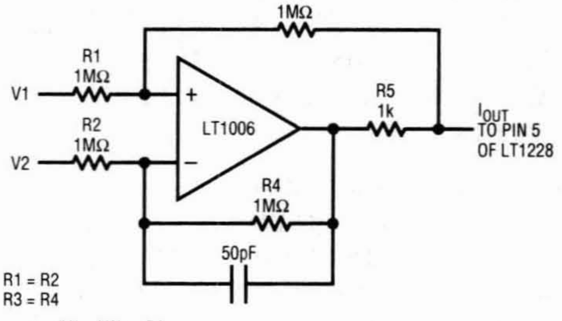
Temperature Compensation of gm with a Thevenin Voltage



Voltage Controlled Gain

To use a voltage to control the gain of the transconductance amplifier requires converting the voltage into a current that flows into pin 5. Because the voltage at pin 5 is two diode drops above the negative supply, a single resistor from the control voltage source to pin 5 will suffice in many applications. The control voltage is referenced to the negative supply and has an offset of about 900mV. The conversion will be monotonic, but the linearity is determined by the change in the voltage at pin 5 (120mV per decade of current). The characteristic is very repeatable since the voltage at pin 5 will vary less than ±5% from part to part. The voltage at pin 5 also has a negative temperature coefficient as described in the previous section. When the gain of several LT1228s are to be varied together, the current can be split equally by using equal value resistors to each pin 5.

For more accurate (and linear) control, a voltage to current converter circuit using one op amp can be used. The following circuit has several advantages. The input no longer has to be referenced to the negative supply and the input can be either polarity (or differential). This circuit works on both single and split supplies since the input voltage and the pin 5 voltage are independent of each other. The temperature coefficient of the output current is set by R5.



R1 = R2
R3 = R4

$$I_{OUT} = \frac{(V1 - V2)}{R5} \times \frac{R3}{R1} = 1mA/V$$

Digital control of the transconductance amplifier gain is done by converting the output of a DAC to a current flowing into pin 5. Unfortunately most current output DACs sink rather than source current and do not have output

APPLICATIONS INFORMATION

compliance compatible with pin 5 of the LT1228. Therefore, the easiest way to digitally control the set current is to use a voltage output DAC and a voltage to current circuit. The previous voltage to current converter will take the output of any voltage output DAC and drive pin 5 with a proportional current. The R, 2R CMOS multiplying DACs operating in the voltage switching mode work well on both single and split supplies with the above circuit.

Logarithmic control is often easier to use than linear control. A simple circuit that doubles the set current for each additional volt of input is shown in the voltage controlled state variable filter application near the end of this data sheet.

Transconductance Amplifier Frequency Response

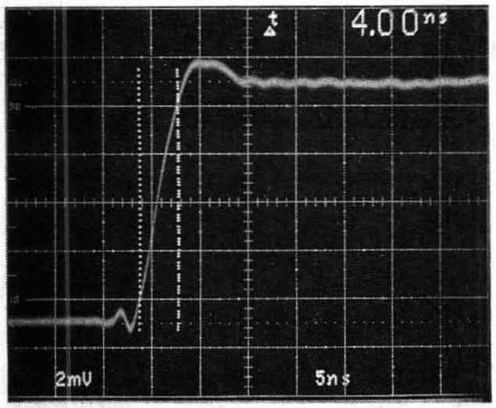
The bandwidth of the transconductance amplifier is a function of the set current as shown in the characteristic curves. At set currents below 100µA, the bandwidth is approximately:

$$-3\text{dB bandwidth} = 3 \times 10^{11}\ I_{SET}$$

The peak bandwidth is about 80MHz at 500µA. When a resistor is used to convert the output current to a voltage, the capacitance at the output forms a pole with the resistor. The best case output capacitance is about 5pF with ±15V supplies and 6pF with ±5V supplies. You must add any PC board or socket capacitance to these values to get the total output capacitance. When using a 1kΩ resistor at the output of the transconductance amp, the output capacitance limits the bandwidth to about 25MHz.

The output slew rate of the transconductance amplifier is the set current divided by the output capacitance, which is 6pF plus board and socket capacitance. For example with the set current at 1mA, the slew rate would be over 100V/µs.

Transconductance Amp Small Signal Response
I_{SET} = 500µA, R1 = 50Ω



LT1228 • TA06

CURRENT FEEDBACK AMPLIFIER

The LT1228 current feedback amplifier has very high non-inverting input impedance and is therefore an excellent buffer for the output of the transconductance amplifier. The non-inverting input is at pin 1, the inverting input at pin 8 and the output at pin 6. The current feedback amplifier maintains its wide bandwidth for almost all voltage gains making it easy to interface the output levels of the transconductance amplifier to other circuitry. The current feedback amplifier is designed to drive low impedance loads such as cables with excellent linearity at high frequencies.

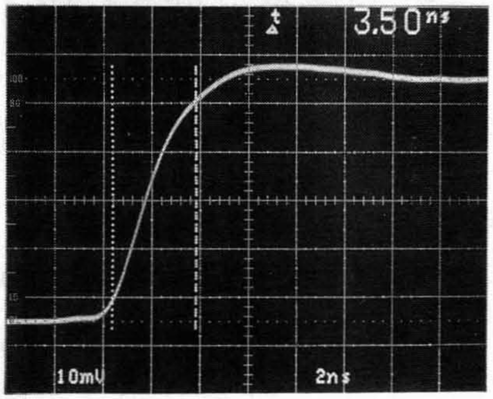
Feedback Resistor Selection

The small signal bandwidth of the LT1228 current feedback amplifier is set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed loop gain and load resistor. The characteristic curves of bandwidth versus supply voltage are done with a heavy load (100Ω) and a light load (1kΩ) to show the effect of loading. These graphs also

APPLICATIONS INFORMATION

show the family of curves that result from various values of the feedback resistor. These curves use a solid line when the response has less than 0.5dB of peaking and a dashed line for the response with 0.5dB to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

Current Feedback Amp Small Signal Response
$V_S = \pm15V$, $R_F = R_G = 750\Omega$, $R_L = 100\Omega$

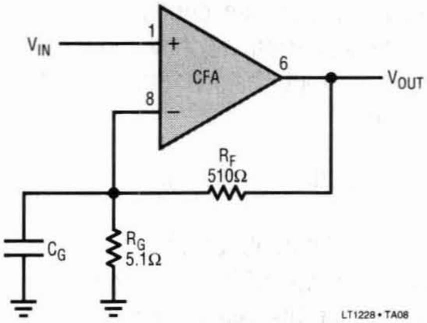


LT1228 • TA07

At a gain of two, on ±15V supplies with a 750Ω feedback resistor, the bandwidth into a light load is over 160MHz without peaking, but into a heavy load the bandwidth reduces to 100MHz. The loading has so much effect because there is a mild resonance in the output stage that enhances the bandwidth at light loads but has its Q reduced by the heavy load. This enhancement is only useful at low gain settings, at a gain of ten it does not boost the bandwidth. At unity gain, the enhancement is so effective the value of the feedback resistor has very little effect on the bandwidth. At very high closed loop gains, the bandwidth is limited by the gain bandwidth product of about 1GHz. The curves show that the bandwidth at a closed loop gain of 100 is 10MHz, only one tenth what it is at a gain of two.

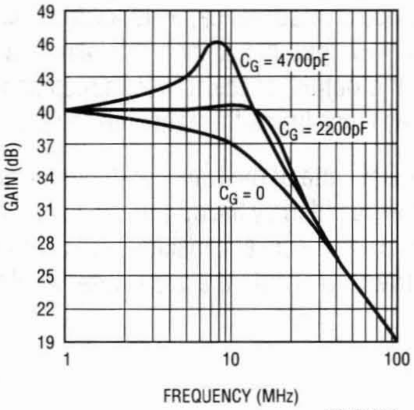
Capacitance on the Inverting Input

Current feedback amplifiers want resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and over shoot in the transient response), but it does not degrade the stability of the amplifier. The amount of capacitance that is necessary to cause peaking is a function of the closed loop gain taken. The higher the gain, the more capacitance is required to cause peaking. For example, in a gain of 100 application, the bandwidth can be increased from 10MHz to 17MHz by adding a 2200pF capacitor, as shown below. C_G must have very low series resistance, such as silver mica.



LT1228 • TA08

Boosting Bandwidth of High Gain Amplifier with Capacitance On Inverting Input



LT1228 • TA09

APPLICATIONS INFORMATION

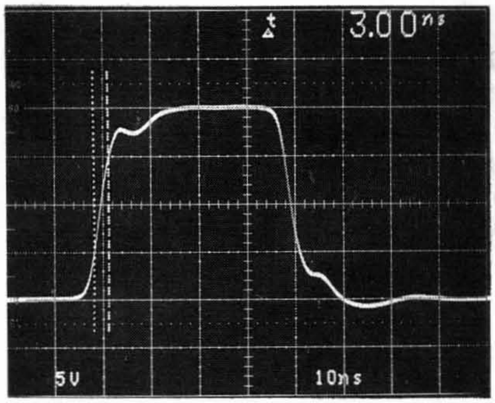
Capacitive Loads

The LT1228 current feedback amplifier can drive capacitive loads directly when the proper value of feedback resistor is used. The graph of Maximum Capacitive Load vs Feedback Resistor should be used to select the appropriate value. The value shown is for 5dB peaking when driving a 1kΩ load, at a gain of 2. This is a worst case condition, the amplifier is more stable at higher gains, and driving heavier loads. Alternatively, a small resistor (10Ω to 20Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present and the disadvantage that the gain is a function of the load resistance.

Slew Rate

The slew rate of the current feedback amplifier is not independent of the amplifier gain configuration the way it is in a traditional op amp. This is because the input stage and the output stage both have slew rate limitations. The input stage of the LT1228 current feedback amplifier slews at about 100V/μs before it becomes non-linear. Faster input signals will turn on the normally reverse biased emitters on the input transistors and enhance the slew rate significantly. This enhanced slew rate can be as much as 3500V/μs!

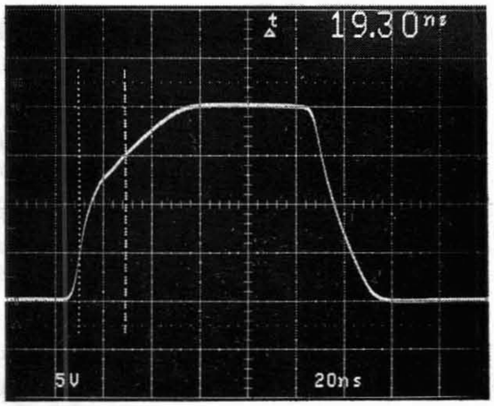
Current Feedback Amp Large Signal Response
$V_S = \pm15V$, $R_F = R_G = 750\Omega$ Slew Rate Enhanced



LT1228 • TA10

The output slew rate is set by the value of the feedback resistors and the internal capacitance. At a gain of ten with a 1kΩ feedback resistor and ±15V supplies, the output slew rate is typically +500V/μs and –850V/μs. There is no input stage enhancement because of the high gain. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced.

Current Feedback Amp Large Signal Response
$V_S = \pm15V$, $R_F = 1k$, $R_G = 110\Omega$, $R_L = 400\Omega$



LT1228 • TA11

Settling Time

The characteristic curves show that the LT1228 current feedback amplifier settles to within 10mV of final value in 40ns to 55ns for any output step less than 10V. The curve of settling to 1mV of final value shows that there is a slower thermal contribution up to 20μs. The thermal settling component comes from the output and the input stage. The output contributes just under 1mV/V of output change and the input contributes 300μV/V of input change. Fortunately the input thermal tends to cancel the output thermal. For this reason the non-inverting gain of two configuration settles faster than the inverting gain of one.

APPLICATIONS INFORMATION

Power Supplies

The LT1228 amplifiers will operate from single or split supplies from ±2V (4V total) to ±18V (36V total). It is not necessary to use equal value split supplies, however the offset voltage and inverting input bias current of the current feedback amplifier will degrade. The offset voltage changes about 350μV/V of supply mismatch, the inverting bias current changes about 2.5μA/V of supply mismatch.

Power Dissipation

The worst case amplifier power dissipation is the total of the quiescent current times the total power supply voltage plus the power in the IC due to the load. The quiescent supply current of the LT1228 transconductance amplifier is equal to 3.5 times the set current at all temperatures. The quiescent supply current of the LT1228 current feedback amplifier has a strong negative temperature coefficient and at 150°C is less than 7mA, typically only 4.5mA. The power in the IC due to the load is a function of the output voltage, the supply voltage and load resistance. The worst case occurs when the output voltage is at half supply, if it can go that far, or its maximum value if it cannot reach half supply.

For example, let's calculate the worst case power dissipation in a variable gain video cable driver operating on ±12V supplies that delivers a maximum of 2V into 150Ω. The maximum set current is 1mA.

$$P_D = 2V_S\left(I_{SMAX} + 3.5I_{SET}\right) + \left(V_S - V_{OMAX}\right)\frac{V_{OMAX}}{R_L}$$

$$P_D = 2 \times 12V \times \left[7mA + \left(3.5 \times 1mA\right)\right] + \left(12V - 2V\right)\frac{2V}{150\Omega}$$

$$= 0.252 + 0.133 = 0.385W$$

The total power dissipation times the thermal resistance of the package gives the temperature rise of the die above ambient. The above example in SO8 surface mount package (thermal resistance is 150°C/W) gives:

$$\text{Temperature Rise} = P_D\theta_{JA} = 0.385W \times 150°C/W$$
$$= 57.75°C$$

Therefore the maximum junction temperature is 70°C + 57.75°C or 127.75°C, well under the absolute maximum junction temperature for plastic packages of 150°C.

TYPICAL APPLICATIONS

Basic Gain Control

The basic gain controlled amplifier is shown on the front page of the data sheet. The gain is directly proportional to the set current. The signal passes through three stages from the input to the output.

First the input signal is attenuated to match the dynamic range of the transconductance amplifier. The attenuator should reduce the signal down to less than 100mV peak. The characteristic curves can be used to estimate how much distortion there will be at maximum input signal. For single ended inputs eliminate R2A or R3A.

The signal is then amplified by the transconductance amplifier (g_m) and referred to ground. The voltage gain of the transconductance amplifier is:

$$g_m \times R1 = 10 \times I_{SET} \times R1$$

Lastly the signal is buffered and amplified by the current feedback amplifier (CFA). The voltage gain of the current feedback amplifier is:

$$1 + \frac{R_F}{R_G}$$

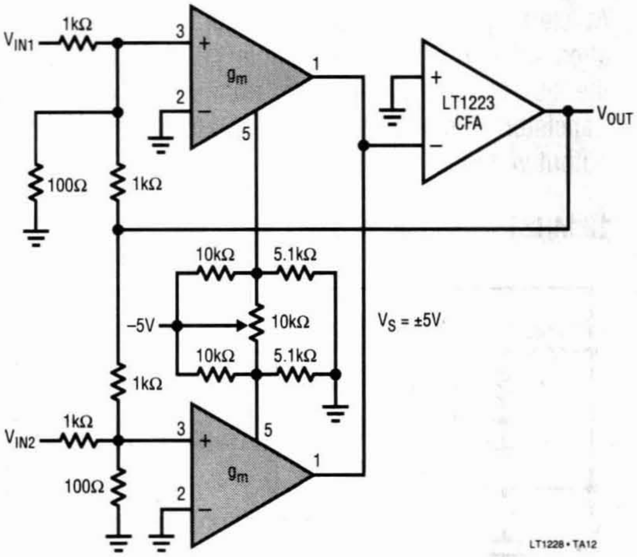
The overall gain of the gain controlled amplifier is the product of all three stages:

$$A_V = \left(\frac{R3}{R3 + R3A}\right) \times 10 \times I_{SET} \times R1 \times \left(1 + \frac{R_F}{R_G}\right)$$

More than one output can be summed into R1 because the output of the transconductance amplifier is a current. This is the simplest way to make a video mixer.

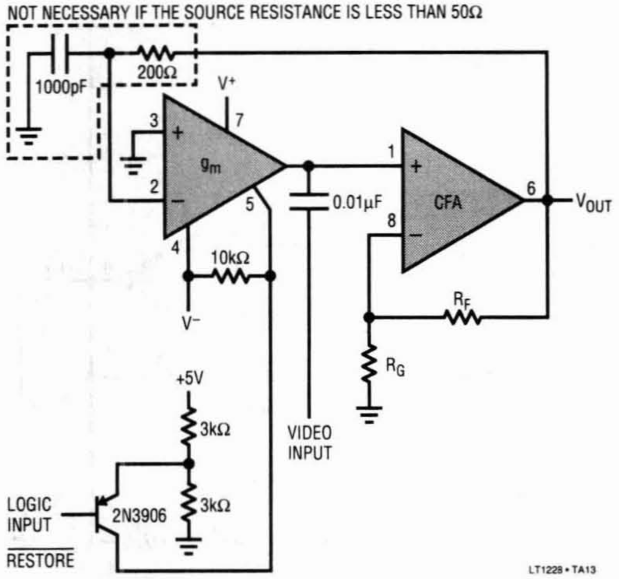
TYPICAL APPLICATIONS

Video Fader


V_IN1
1kΩ
3
+
gm
2
–
1
5
+
LT1223
CFA
–
V_OUT
100Ω
1kΩ
10kΩ
5.1kΩ
–5V
10kΩ
V_S = ±5V
10kΩ
5.1kΩ
1kΩ
V_IN2
1kΩ
3
5
gm
1
100Ω
2
LT1228 • TA12

The video fader uses the transconductance amplifiers from two LT1228s in the feedback loop of another current feedback amplifier, the LT1223. The amount of signal from each input at the output is set by the ratio of the set currents of the two LT1228s, not by their absolute value. The bandwidth of the current feedback amplifier is inversely proportional to the set current in this configuration. Therefore, the set currents remain high over most of the pot's range, keeping the bandwidth over 15MHz even when the signal is attenuated 20dB. The pot is set up to completely turn off one LT1228 at each end of the rotation.

Video DC Restore (Clamp) Circuit


NOT NECESSARY IF THE SOURCE RESISTANCE IS LESS THAN 50Ω
1000pF
200Ω
V+
3
7
+
gm
2
–
5
4
10kΩ
V–
0.01µF
1
+
CFA
6
8
–
V_OUT
R_F
R_G
+5V
3kΩ
VIDEO INPUT
LOGIC INPUT
RESTORE
2N3906
3kΩ
LT1228 • TA13

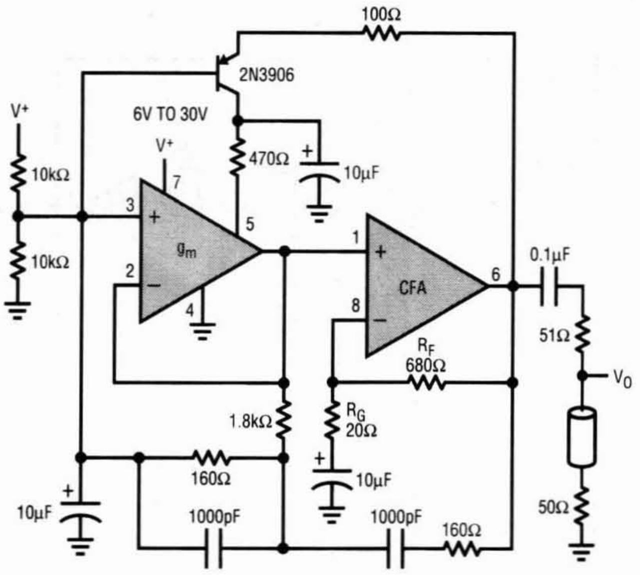
The video restore (clamp) circuit restores the black level of the composite video to zero volts at the beginning of every line. This is necessary because AC coupled video changes DC level as a function of the average brightness of the picture. DC restoration also rejects low frequency noise such as hum.

The circuit has two inputs: composite video and a logic signal. The logic signal is high except during the back porch time right after the horizontal sync pulse. While the logic is high, the PNP is off and I_{SET} is zero. With I_{SET} equal to zero the feedback to pin 2 has no affect. The video input drives the non-inverting input of the current feedback amplifier whose gain is set by R_F and R_G. When the logic signal is low, the PNP turns on and I_{SET} goes to about 1mA. Then the transconductance amplifier charges the capacitor to force the output to match the voltage at pin 3, in this case zero volts.

This circuit can be modified so that the video is DC coupled by operating the amplifier in an inverting configuration. Just ground the video input shown and connect R_G to the video input instead of to ground.

TYPICAL APPLICATIONS

Single Supply Wien Bridge Oscillator



f = 1MHz
V_O = +6dBm (450mV_{RMS})
2nd HARMONIC = −38dBc
3rd HARMONIC = −54 dBc
FOR +5V OPERATION SHORT OUT 100Ω RESISTOR

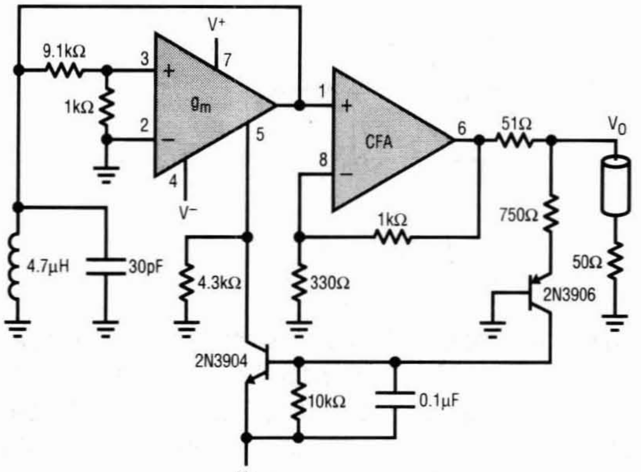
LT1228 • TA14

In this application the LT1228 is biased for operation from a single supply. An artificial signal ground at half supply voltage is generated with two 10kΩ resistors and bypassed with a capacitor. A capacitor is used in series with R_G to set the DC gain of the current feedback amplifier to unity.

The transconductance amplifier is used as a variable resistor to control gain. A variable resistor is formed by driving the inverting input and connecting the output back to it. The equivalent resistor value is the inverse of the g_m. This works with the 1.8kΩ resistor to make a variable attenuator. The 1MHz oscillation frequency is set by the Wien bridge network made up of two 1000pF capacitors and two 160Ω resistors.

For clean sine wave oscillation, the circuit needs a net gain of one around the loop. The current feedback amplifier has a gain of 34 to keep the voltage at the transconductance amplifier input low. The Wien bridge has an attenuation of 3 at resonance; therefore the attenuation of the 1.8kΩ resistor and the transconductance amplifier must be about 11, resulting in a set current of about 600μA at oscillation. At start up there is no set current and therefore no attenuation for a net gain of about 11 around the loop. As the output oscillation builds up it turns on the PNP transistor which generates the set current to regulate the output voltage.

12 MHz Negative Resistance LC Oscillator



V_O = +10dB
AT V_S = ±5V ALL HARMONICS 40dB DOWN
AT V_S = ±12V ALL HARMONICS 50dB DOWN

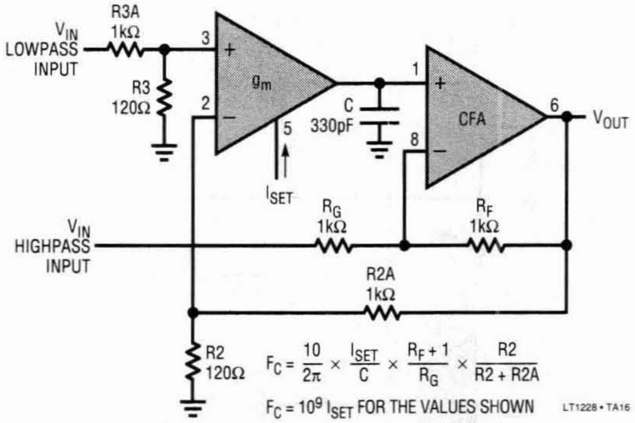
LT1228 • TA15

This oscillator uses the transconductance amplifier as a negative resistor to cause oscillation. A negative resistor results when the positive input of the transconductance amplifier is driven and the output is returned to it. In this example a voltage divider is used to lower the signal level at the positive input for less distortion. The negative resistor will not DC bias correctly unless the output of the transconductance amplifier drives a very low resistance. Here it sees an inductor to ground so the gain at DC is zero. The oscillator needs negative resistance to start and that is provided by the 4.3kΩ resistor to pin 5. As the output level rises it turns on the PNP transistor and in turn the NPN which steals current from the transconductance amplifier bias input.

TYPICAL APPLICATIONS

Filters

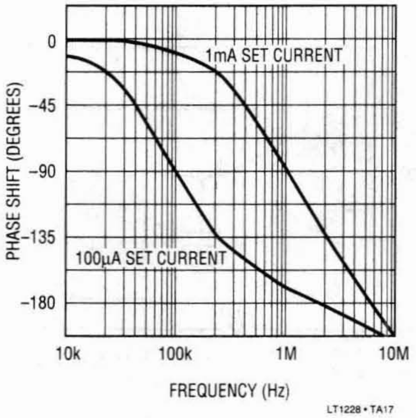
Single Pole Low/High/Allpass Filter



$$F_C = \frac{10}{2\pi} \times \frac{I_{SET}}{C} \times \frac{R_F + 1}{R_G} \times \frac{R2}{R2 + R2A}$$

$F_C = 10^9 I_{SET}$ FOR THE VALUES SHOWN

Allpass Filter Phase Response

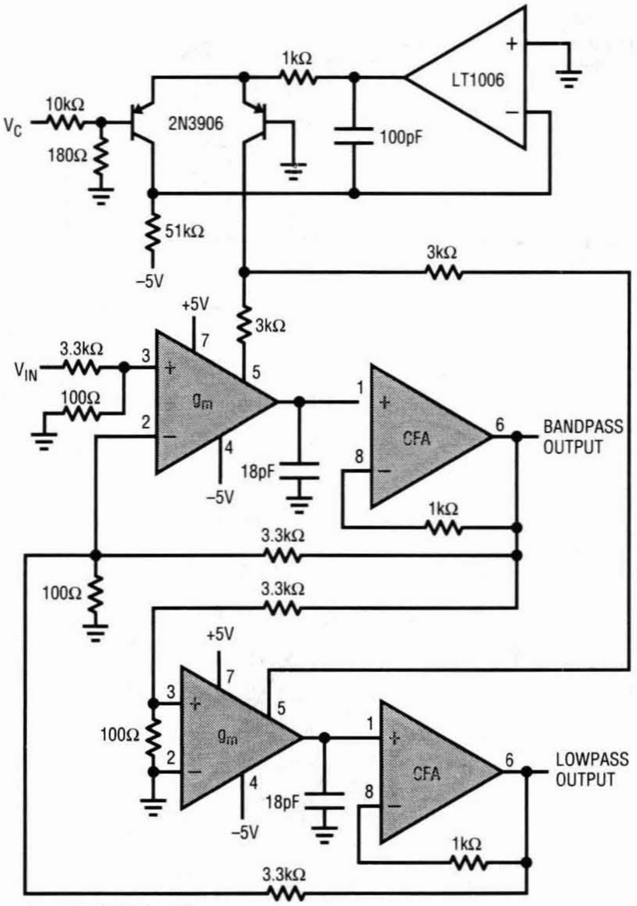


Using the variable transconductance of the LT1228 to make variable filters is easy and predictable. The most straight forward way is to make an integrator by putting a capacitor at the output of the transconductance amp and buffering it with the current feedback amplifier. Because the input bias current of the current feedback amplifier must be supplied by the transconductance amplifier, the set current should not be operated below 10μA. This limits the filters to about a 100:1 tuning range.

The Single Pole circuit realizes a single pole filter with a corner frequency (f_C) proportional to the set current. The values shown give a 100kHz corner frequency for 100μA set current. The circuit has two inputs, a lowpass filter input and a highpass filter input. To make a lowpass filter, ground the highpass input and drive the lowpass input. Conversely for a highpass filter, ground the lowpass input and drive the highpass input. If both inputs are driven, the result is an allpass filter or phase shifter. The allpass has flat amplitude response and 0° phase shift at low frequencies, going to −180° at high frequencies. The allpass filter has −90° phase shift at the corner frequency.

TYPICAL APPLICATIONS

Voltage Controlled State Variable Filter


10kΩ
V_C
180Ω
2N3906
1kΩ
100pF
LT1006
+
–
51kΩ
–5V
3kΩ
+5V
3kΩ
7
3.3kΩ
V_{IN}
100Ω
3
2
+
–
g_m
5
4
–5V
18pF
1
CFA
8
6
BANDPASS OUTPUT
1kΩ
3.3kΩ
100Ω
3.3kΩ
+5V
7
3
100Ω
2
g_m
5
4
–5V
18pF
1
CFA
8
6
LOWPASS OUTPUT
1kΩ
3.3kΩ

f_0 = 100kHz AT V_C = 0V
f_0 = 200kHz AT V_C = 1V
f_0 = 400kHz AT V_C = 2V
f_0 = 800kHz AT V_C = 3V
f_0 = 1.6MHz AT V_C = 4V

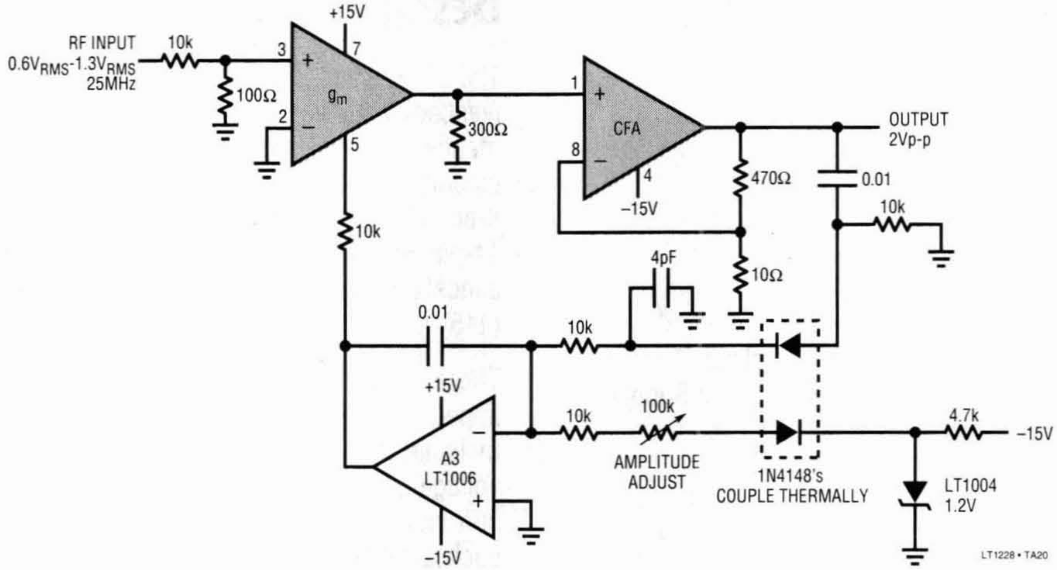
LT1228 • TA18

The state variable filter has both lowpass and bandpass outputs. Each LT1228 is configured as a variable integrator whose frequency is set by the attenuators, the capacitors and the set current. Because the integrators have both positive and negative inputs, the additional op amp normally required is not needed. The input attenuators set the circuit up to handle $3V_{PP}$ signals.

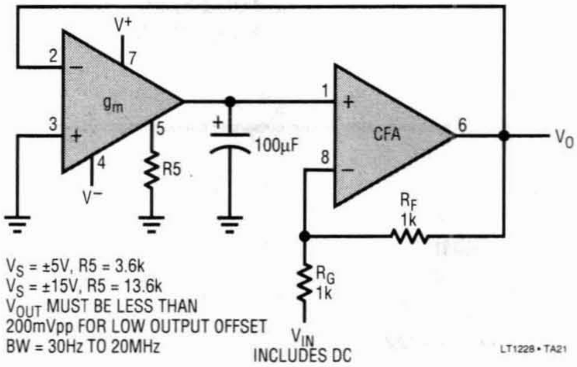
The set current is generated with a simple circuit that gives logarithmic voltage to current control. The two PNP transistors should be a matched pair in the same package for best accuracy. If discrete transistors are used, the 51kΩ resistor should be trimmed to give proper frequency response with V_C equal zero. The circuit generates 100μA for V_C equal zero volts and doubles the current for every additional volt. The two 3kΩ resistors divide the current between the two LT1228s. Therefore the set current of each amplifier goes from 50μA to 800μA for a control voltage of 0V to 4V. The resulting filter is at 100kHz for V_C equal zero, and changes it one octave/V of control input.

TYPICAL APPLICATIONS

RF AGC Amp (Leveling Loop)

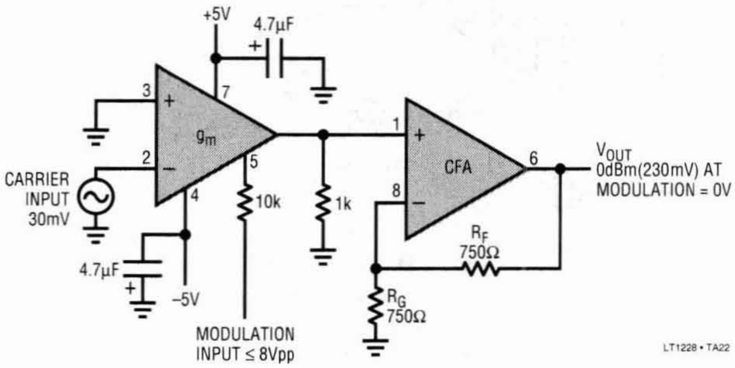

RF INPUT
0.6V$_{RMS}$-1.3V$_{RMS}$
25MHz
10k
100Ω
+15V
3
7
2
5
g$_m$
300Ω
1
8
4
CFA
−15V
OUTPUT
2Vp-p
470Ω
0.01
10k
10Ω
4pF
10k
0.01
10k
+15V
A3
LT1006
−15V
10k
100k
AMPLITUDE
ADJUST
1N4148's
COUPLE THERMALLY
4.7k
−15V
LT1004
1.2V
LT1228 • TA20

Inverting Amplifier with DC Output Less Than 5mV


V+
2
7
3
4
V−
g$_m$
5
R5
100μF
1
8
CFA
6
V$_O$
R$_F$
1k
R$_G$
1k
V$_{IN}$
INCLUDES DC
LT1228 • TA21

V$_S$ = ±5V, R5 = 3.6k
V$_S$ = ±15V, R5 = 13.6k
V$_{OUT}$ MUST BE LESS THAN
200mVpp FOR LOW OUTPUT OFFSET
BW = 30Hz TO 20MHz

Amplitude Modulator


+5V
4.7μF
3
7
2
g$_m$
5
4
CARRIER
INPUT
30mV
4.7μF
−5V
10k
1k
1
8
CFA
6
R$_F$
750Ω
R$_G$
750Ω
MODULATION
INPUT ≤ 8Vpp
LT1228 • TA22

V$_{OUT}$
0dBm(230mV) AT
MODULATION = 0V

LINEAR TECHNOLOGY

LT1229/LT1230

Dual and Quad 100MHz Current Feedback Amplifiers

FEATURES

- 100MHz Bandwidth
- 1000V/μs Slew Rate
- Low Cost
- 30mA Output Drive Current
- 0.04% Differential Gain
- 0.1° Differential Phase
- High Input Impedance, 25MΩ, 3pF
- Wide Supply Range, ±2V to ±15V
- Low Supply Current, 6mA Per Amplifier
- Inputs Common Mode to Within 1.5V of Supplies
- Outputs Swing Within 0.8V of Supplies

APPLICATIONS

- Video Instrumentation Amplifiers
- Cable Drivers
- RGB Amplifiers
- Test Equipment Amplifiers

DESCRIPTION

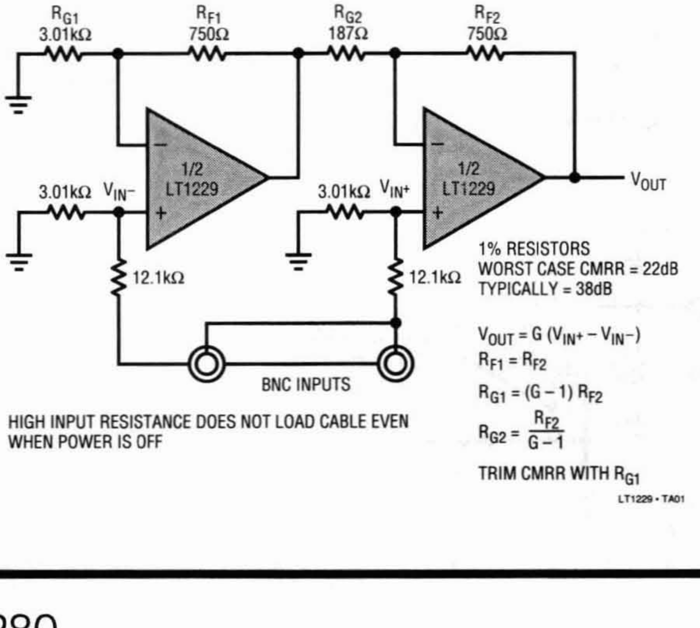
The LT1229 and LT1230 dual and quad 100MHz current feedback amplifiers are designed for maximum performance in small packages. Using industry standard pinouts, the dual is available in the 8-pin miniDIP and the 8-pin SO package while the quad is in the 14-pin DIP and 14-pin SO. The amplifiers are designed to operate on almost any available supply voltage from 4V (±2V) to 30V (±15V).

These current feedback amplifiers have very high input impedance and make excellent buffer amplifiers. They maintain their wide bandwidth for almost all closed loop voltage gains. The amplifiers drive over 30mA of output current and are optimized to drive low impedance loads, such as cables, with excellent linearity at high frequencies.

The LT1229 and LT1230 are manufactured on Linear Technology's proprietary complementary bipolar process. For a single amplifier like these see the LT1227 and for better DC accuracy see the LT1223.

TYPICAL APPLICATION

Video Loop Through Amplifier



1% RESISTORS
WORST CASE CMRR = 22dB
TYPICALLY = 38dB

$V_{OUT} = G\,(V_{IN^+} - V_{IN^-})$

$R_{F1} = R_{F2}$

$R_{G1} = (G - 1)\,R_{F2}$

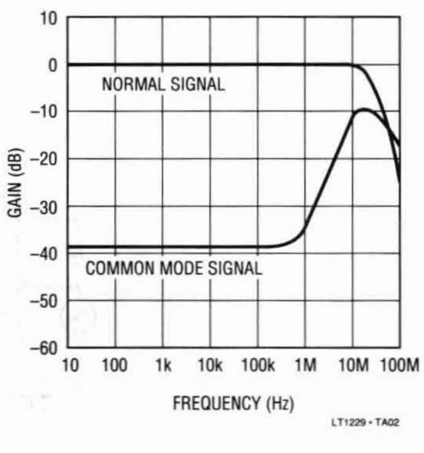
$R_{G2} = \frac{R_{F2}}{G - 1}$

TRIM CMRR WITH R_{G1}

HIGH INPUT RESISTANCE DOES NOT LOAD CABLE EVEN WHEN POWER IS OFF

LT1229 • TA01

Loop Through Amplifier Frequency Response

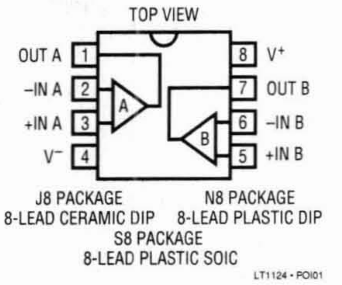


LT1229 • TA02

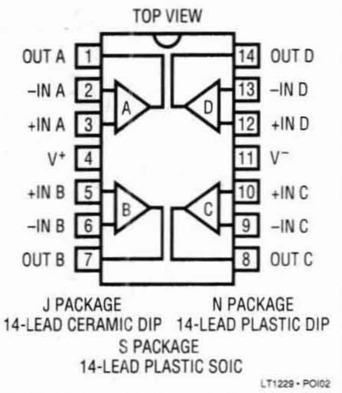
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Current	±15mA
Output Short Circuit Duration (Note 1)	Continuous
Operating Temperature Range	
LT1229C, LT1230C	0°C to 70°C
LT1229M, LT1230M	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature	
Plastic Package	150°C
Ceramic Package	175°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION


TOP VIEW
OUT A 1
−IN A 2
+IN A 3
V⁻ 4
8 V⁺
7 OUT B
6 −IN B
5 +IN B
A
B
J8 PACKAGE 8-LEAD CERAMIC DIP
N8 PACKAGE 8-LEAD PLASTIC DIP
S8 PACKAGE 8-LEAD PLASTIC SOIC
LT1124 • POI01

ORDER PART NUMBER
LT1229MJ8 LT1229CJ8 LT1229CN8 LT1229CS8
S8 PART MARKING
1229


TOP VIEW
OUT A 1
−IN A 2
+IN A 3
V⁺ 4
+IN B 5
−IN B 6
OUT B 7
14 OUT D
13 −IN D
12 +IN D
11 V⁻
10 +IN C
9 −IN C
8 OUT C
A
B
C
D
J PACKAGE 14-LEAD CERAMIC DIP
N PACKAGE 14-LEAD PLASTIC DIP
S PACKAGE 14-LEAD PLASTIC SOIC
LT1229 • POI02

ORDER PART NUMBER
LT1230MJ LT1230CJ LT1230CN LT1230CS

ELECTRICAL CHARACTERISTICS

Each Amplifier, V_{CM} = 0V, ±5V ≤ V_S = ±15V, pulse tested unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			±3	±10	mV
			●			±15	mV
	Input Offset Voltage Drift		●		10		μV/°C
I_{IN+}	Non-Inverting Input Current	T_A = 25°C			±0.3	±3	μA
			●			±10	μA
I_{IN-}	Inverting Input Current	T_A = 25°C			±10	±50	μA
			●			±100	μA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1kΩ, R_G = 10Ω, R_S = 0Ω			6		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz, R_F = 1kΩ, R_G = 10Ω, R_S = 10kΩ			1.4		pA/√Hz
R_{IN}	Input Resistance	V_{IN} = ±13V, V_S = ±15V	●	2	25		MΩ
		V_{IN} = ±3V, V_S = ±5V	●	2	25		MΩ
C_{IN}	Input Capacitance				3		pF
	Input Voltage Range	V_S = ±15V, T_A = 25°C		±13	±13.5		V
			●	±12			V
		V_S = ±5V, T_A = 25°C		±3	±3.5		V
			●	±2			V
CMRR	Common Mode Rejection Ratio	V_S = ±15V, V_{CM} = ±13V, T_A = 25°C		55	69		dB
		V_S = ±15V, V_{CM} = ±12V	●	55			dB
		V_S = ±5V, V_{CM} = ±3V, T_A = 25°C		55	69		dB
		V_S = ±5V, V_{CM} = ±2V	●	55			dB

ELECTRICAL CHARACTERISTICS

Each Amplifier, V_{CM} = 0V, ±5V ≤ V_S = ±15V, pulse tested unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Inverting Input Current Common Mode Rejection	$V_S = \pm15V$, $V_{CM} = \pm13V$, $T_A = 25°C$			2.5	10	µA/V
		$V_S = \pm15V$, $V_{CM} = \pm12V$	●			10	µA/V
		$V_S = \pm5V$, $V_{CM} = \pm3V$, $T_A = 25°C$			2.5	10	µA/V
		$V_S = \pm5V$, $V_{CM} = \pm2V$	●			10	µA/V
PSRR	Power Supply Rejection Ratio	$V_S = \pm2V$ to $\pm15V$, $T_A = 25°C$		60	80		dB
		$V_S = \pm3V$ to $\pm15V$	●	60			dB
	Non-Inverting Input Current Power Supply Rejection	$V_S = \pm2V$ to $\pm15V$, $T_A = 25°C$			10	50	nA/V
		$V_S = \pm3V$ to $\pm15V$	●			50	nA/V
	Inverting Input Current Power Supply Rejection	$V_S = \pm2V$ to $\pm15V$, $T_A = 25°C$			0.1	5	µA/V
		$V_S = \pm3V$ to $\pm15V$	●			5	µA/V
A_V	Large Signal Voltage Gain, (Note 2)	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 1k\Omega$	●	55	65		dB
		$V_S = \pm5V$, $V_{OUT} = \pm2V$, $R_L = 150\Omega$	●	55	65		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN-}$, (Note 2)	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 1k\Omega$	●	100	200		kΩ
		$V_S = \pm5V$, $V_{OUT} = \pm2V$, $R_L = 150\Omega$	●	100	200		kΩ
V_{OUT}	Maximum Output Voltage Swing, (Note 2)	$V_S = \pm15V$, $R_L = 400\Omega$, $T_A = 25°C$		±12	±13.5		V
			●	±10			V
		$V_S = \pm5V$, $R_L = 150\Omega$, $T_A = 25°C$		±3	±3.7		V
			●	±2.5			V
I_{OUT}	Maximum Output Current	$R_L = 0\Omega$, $T_A = 25°C$		30	65	125	mA
I_s	Supply Current, (Note 3)	$V_{OUT} = 0V$, Each Amplifier, $T_A = 25°C$			6	9.5	mA
			●			11	mA
SR	Slew Rate, (Notes 4 and 6)	$T_A = 25°C$		300	700		V/µs
SR	Slew Rate	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 400\Omega$			2500		V/µs
t_r	Rise Time, (Notes 5 and 6)	$T_A = 25°C$			10	20	ns
BW	Small Signal Bandwidth	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 100\Omega$			100		MHz
t_r	Small Signal Rise Time	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 100\Omega$			3.5		ns
	Propagation Delay	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 100\Omega$			3.5		ns
	Small Signal Overshoot	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 100\Omega$			15		%
t_s	Settling Time	0.1%, $V_{OUT} = 10V$, $R_F = 1k\Omega$, $R_G = 1k\Omega$, $R_L = 1k\Omega$			45		ns
	Differential Gain, (Note 7)	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 1k\Omega$			0.01		%
	Differential Phase, (Note 7)	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 1k\Omega$			0.01		Deg.
	Differential Gain, (Note 7)	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 150\Omega$			0.04		%
	Differential Phase, (Note 7)	$V_S = \pm15V$, $R_F = 750\Omega$, $R_G = 750\Omega$, $R_L = 150\Omega$			0.1		Deg.

The ● denotes specifications which apply over the operating temperature range.

Note 1: A heatsink may be required depending on the power supply voltage and how many amplifiers are shorted.

Note 2: The power tests done on ±15V supplies are done on only one amplifier at a time to prevent excessive junction temperatures when testing at maximum operating temperature.

Note 3: The supply current of the LT1229, LT1230 has a negative temperature coefficient. For more information see the application information section.

Note 4: Slew rate is measured at ±5V on a ±10V output signal while operating on ±15V supplies with $R_F = 1k\Omega$, $R_G = 110\Omega$ and $R_L = 400\Omega$. The slew rate is much higher when the input is overdriven and when the amplifier is operated inverting, see the applications section.

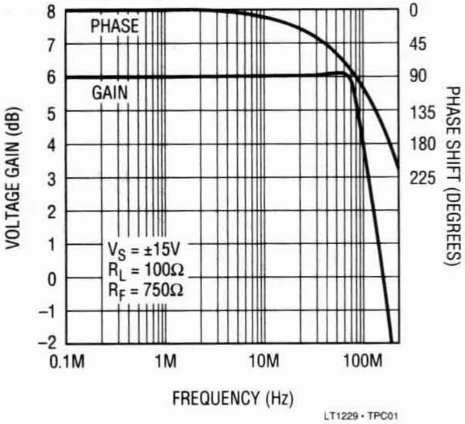
Note 5: Rise time is measured from 10% to 90% on a ±500mV output signal while operating on ±15V supplies with $R_F = 1k\Omega$, $R_G = 110\Omega$ and $R_L = 100\Omega$. This condition is not the fastest possible, however, it does guarantee the internal capacitances are correct and it makes automatic testing practical.

Note 6: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

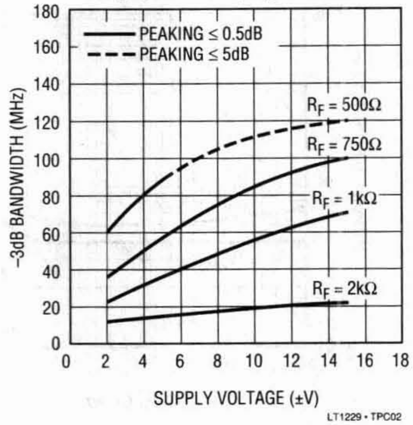
Note 7: NTSC composite video with an output level of 2Vp.

TYPICAL PERFORMANCE CHARACTERISTICS

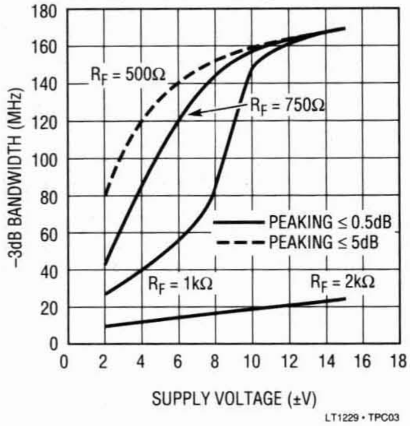
Voltage Gain and Phase vs Frequency, Gain = 6dB



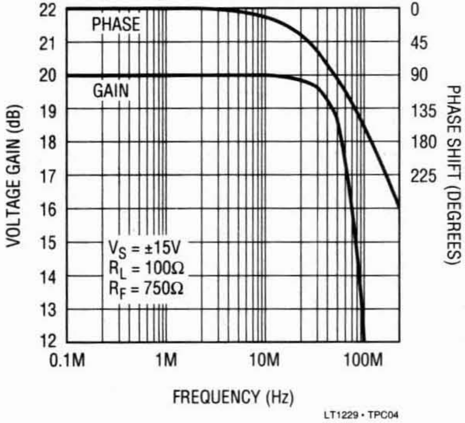
–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 100Ω



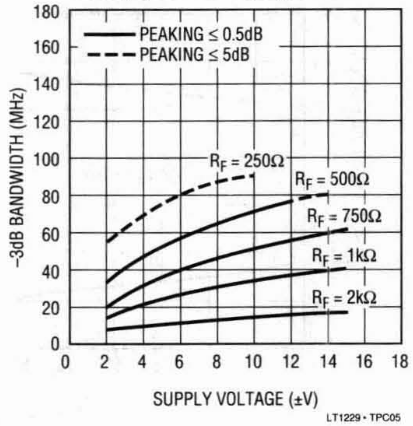
–3dB Bandwidth vs Supply Voltage, Gain = 2, R_L = 1kΩ



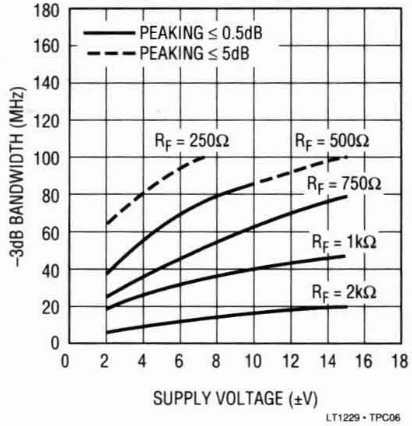
Voltage Gain and Phase vs Frequency, Gain = 20dB



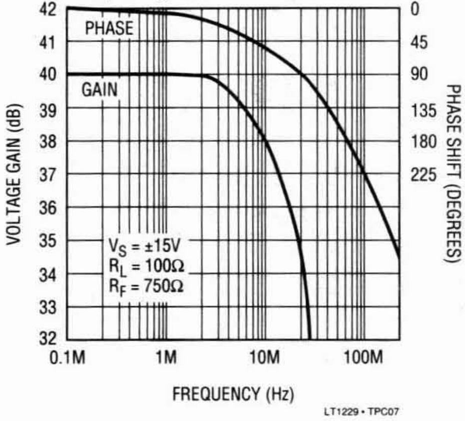
–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 100Ω



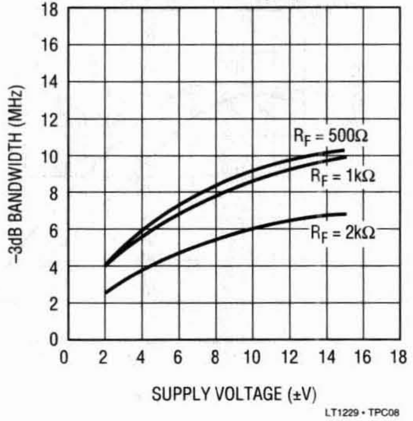
–3dB Bandwidth vs Supply Voltage, Gain = 10, R_L = 1kΩ



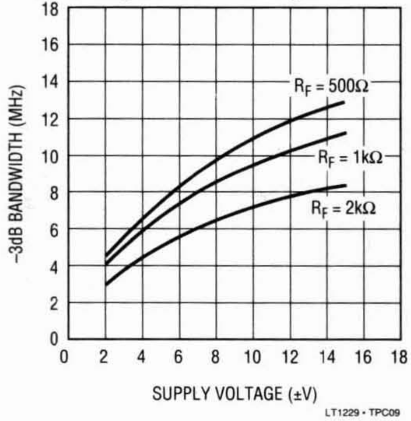
Voltage Gain and Phase vs Frequency, Gain = 40dB



–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 100Ω

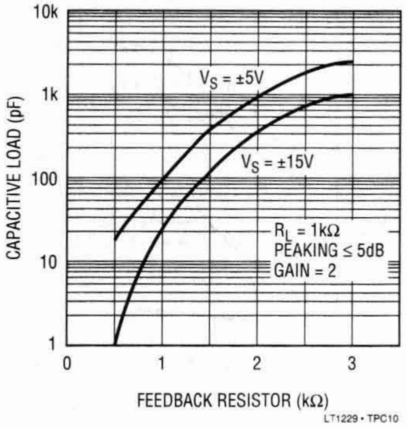


–3dB Bandwidth vs Supply Voltage, Gain = 100, R_L = 1kΩ

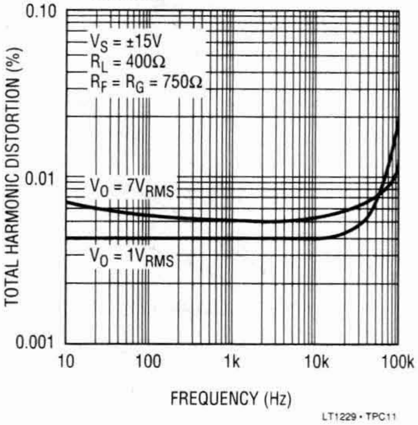


TYPICAL PERFORMANCE CHARACTERISTICS

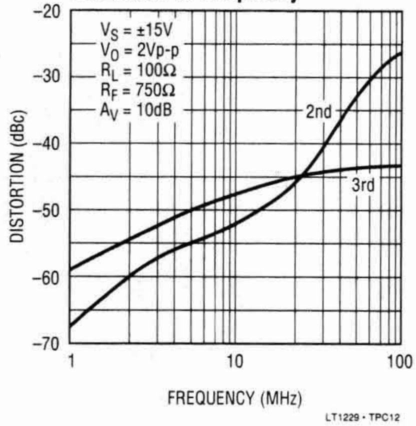
Maximum Capacitance Load vs Feedback Resistor



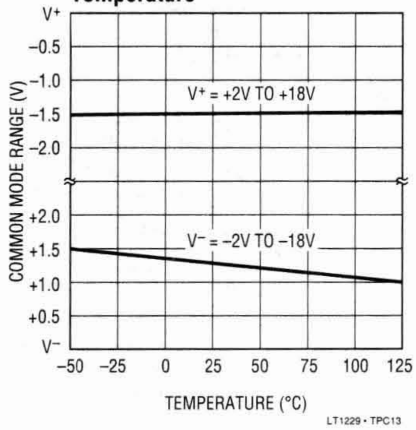
Total Harmonic Distortion vs Frequency



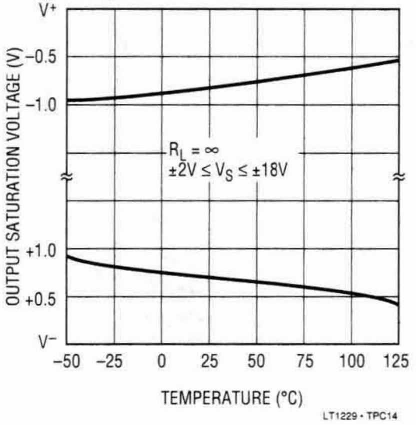
2nd and 3rd Harmonic Distortion vs Frequency



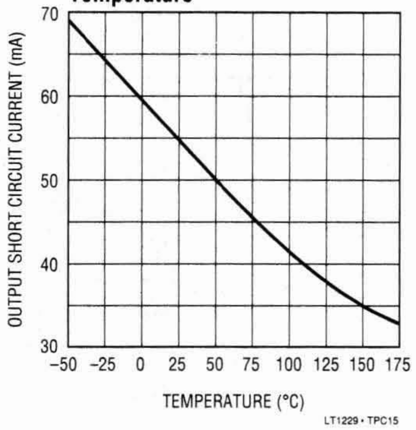
Input Common Mode Limit vs Temperature



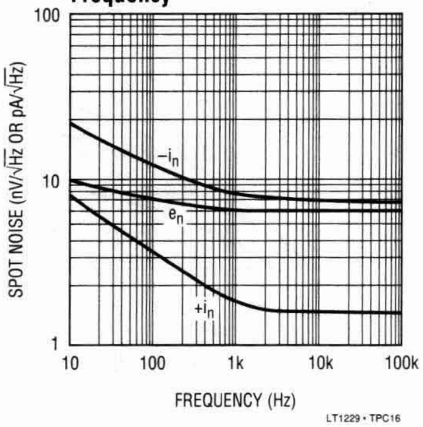
Output Saturation Voltage vs Temperature



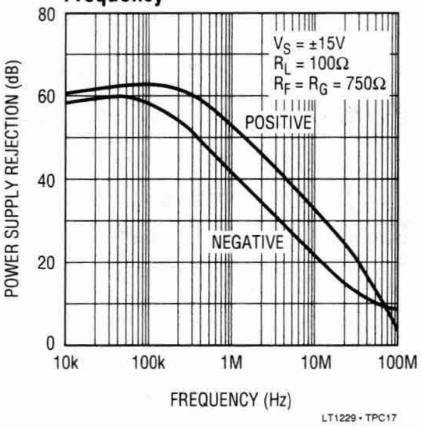
Output Short Circuit Current vs Temperature



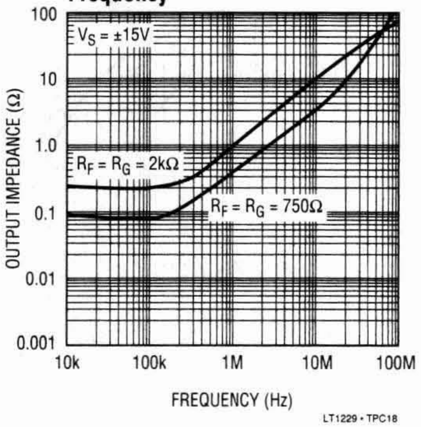
Spot Noise Voltage and Current vs Frequency



Power Supply Rejection vs Frequency

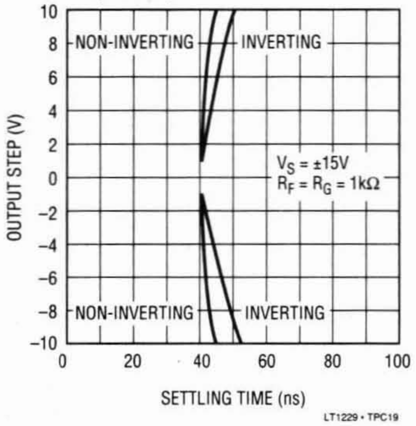


Output Impedance vs Frequency

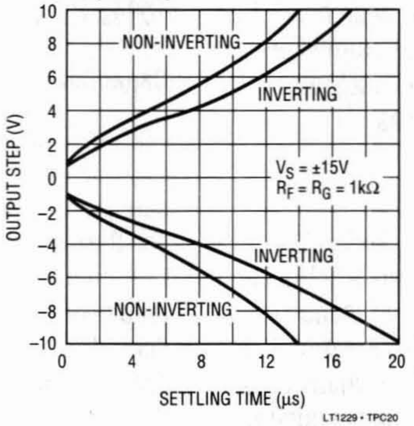


TYPICAL PERFORMANCE CHARACTERISTICS

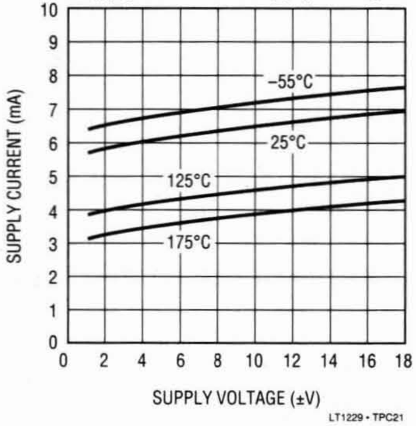
Settling Time to 10mV vs Output Step



Settling Time to 1mV vs Output Step

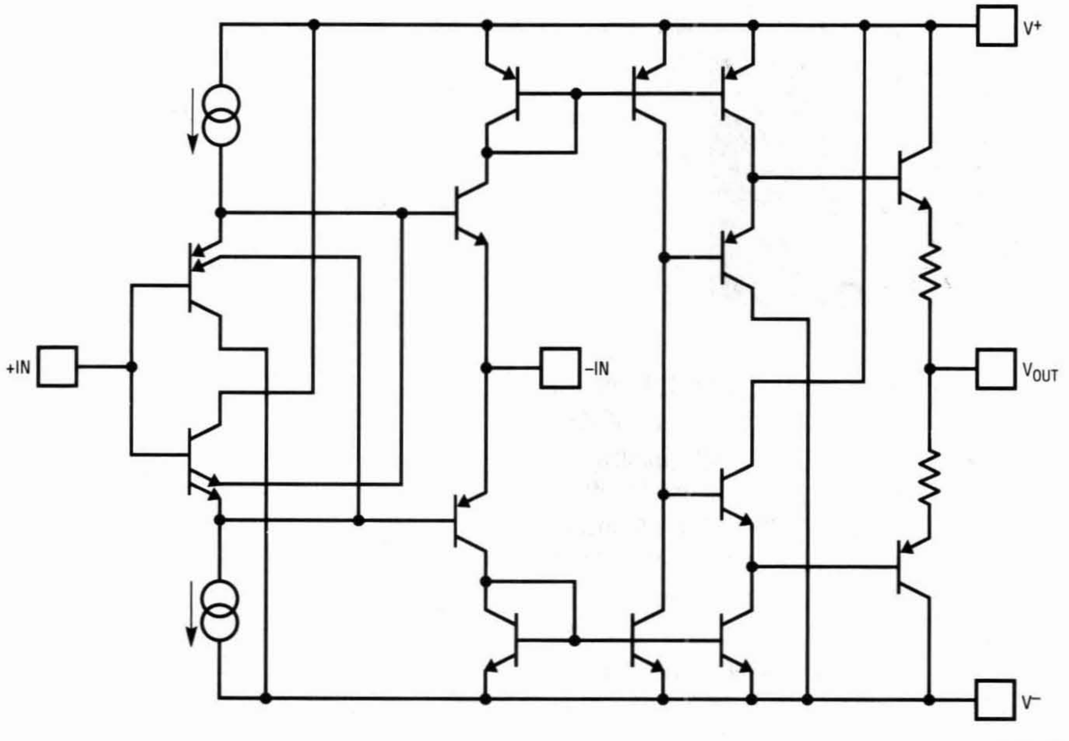


Supply Current vs Supply Voltage



SIMPLIFIED SCHEMATIC

One Amplifier



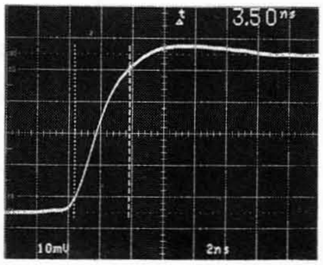
APPLICATIONS INFORMATION

The LT1229 and LT1230 are very fast dual and quad current feedback amplifiers. Because they are current feedback amplifiers, they maintain their wide bandwidth over a wide range of voltage gains. These amplifiers are designed to drive low impedance loads such as cables with excellent linearity at high frequencies.

Feedback Resistor Selection

The small signal bandwidth of the LT1229/LT1230 is set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed loop gain and load resistor. The characteristic curves of bandwidth versus supply voltage are done with a heavy load (100Ω) and a light load (1kΩ) to show the effect of loading. These graphs also show the family of curves that result from various values of the feedback resistor. These curves use a solid line when the response has less than 0.5dB of peaking and a dashed line when the response has 0.5dB to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

Small Signal Rise Time with $R_F = R_G = 750\Omega$, $V_S = \pm15V$, and $R_L = 100\Omega$

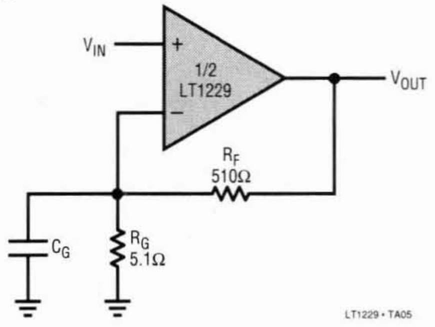


LT1229 • TA04

At a gain of two, on ±15V supplies with a 750Ω feedback resistor, the bandwidth into a light load is over 160MHz without peaking, but into a heavy load the bandwidth reduces to 100MHz. The loading has so much effect because there is a mild resonance in the output stage that enhances the bandwidth at light loads but has its Q reduced by the heavy load. This enhancement is only useful at low gain settings; at a gain of ten it does not boost the bandwidth. At unity gain, the enhancement is so effective the value of the feedback resistor has very little effect. At very high closed loop gains, the bandwidth is limited by the gain bandwidth product of about 1GHz. The curves show that the bandwidth at a closed loop gain of 100 is 10MHz, only one tenth what it is at a gain of two.

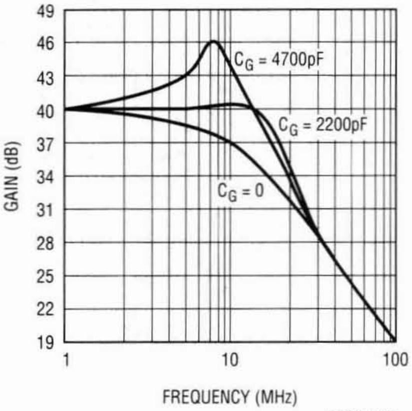
Capacitance on the Inverting Input

Current feedback amplifiers want resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and overshoot in the transient response), but it does not degrade the stability of the amplifier. The amount of capacitance that is necessary to cause peaking is a function of the closed loop gain taken. The higher the gain, the more capacitance is required to cause peaking. We can add capacitance from the inverting input to ground to increase the bandwidth in high gain applications. For example, in this gain of 100 application, the bandwidth can be increased from 10MHz to 17MHz by adding a 2200pF capacitor.



LT1229 • TA05

Boosting Bandwidth of High Gain Amplifier with Capacitance on Inverting Input



LT1229 • TA06

APPLICATIONS INFORMATION

Capacitive Loads

The LT1229/LT1230 can drive capacitive loads directly when the proper value of feedback resistor is used. The graph Maximum Capacitive Load vs Feedback Resistor should be used to select the appropriate value. The value shown is for 5dB peaking when driving a 1kΩ load at a gain of 2. This is a worst case condition; the amplifier is more stable at higher gains and driving heavier loads. Alternatively, a small resistor (10Ω to 20Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present, and the disadvantage that the gain is a function of the load resistance.

Power Supplies

The LT1229 and LT1230 amplifiers will operate from single or split supplies from ±2V (4V total) to ±15V (30V total). It is not necessary to use equal value split supplies, however, the offset voltage and inverting input bias current will change. The offset voltage changes about 350μV per volt of supply mismatch, the inverting bias current changes about 2.5μA per volt of supply mismatch.

Power Dissipation

The LT1229/LT1230 amplifiers combine high speed and large output current drive into very small packages. Because these amplifiers work over a very wide supply range, it is possible to exceed the maximum junction temperature under certain conditions. To ensure that the LT1229/LT1230 remain within their absolute maximum ratings, we must calculate the worst case power dissipation, define the maximum ambient temperature, select the appropriate package and then calculate the maximum junction temperature.

The worst case amplifier power dissipation is the total of the quiescent current times the total power supply voltage plus the power in the IC due to the load. The quiescent supply current of the LT1229/LT1230 has a strong negative temperature coefficient. The supply current of each amplifier at 150°C is less than 7mA and typically is only 4.5mA. The power in the IC due to the load is a function of the output voltage, the supply voltage and load resistance. The worst case occurs when the output voltage is at half supply, if it can go that far, or its maximum value if it cannot reach half supply.

For example, let's calculate the worst case power dissipation in a video cable driver operating on ±12V supplies that delivers a maximum of 2V into 150Ω.

$$Pd_{MAX} = 2V_S I_{SMAX} + \left(V_S - V_{OMAX}\right)\frac{V_{OMAX}}{R_L}$$

$$Pd_{MAX} = 2 \times 12V \times 7mA + \left(12V - 2V\right) \times \frac{2V}{150\Omega}$$

$$= 0.168 + 0.133 = 0.301W \text{ per Amp}$$

Now if that is the dual LT1229, the total power in the package is twice that, or 0.602W. We now must calculate how much the die temperature will rise above the ambient. The total power dissipation times the thermal resistance of the package gives the amount of temperature rise. For the above example, if we use the SO8 surface mount package, the thermal resistance is 150°C/W junction to ambient in still air.

$$\text{Temperature Rise} = P_{dMAX} R_{\theta JA} = 0.602W \times 150°C/W$$
$$= 90.3°C$$

The maximum junction temperature allowed in the plastic package is 150°C. Therefore, the maximum ambient allowed is the maximum junction temperature less the temperature rise.

$$\text{Maximum Ambient} = 150°C - 90.3°C = 59.7°C$$

Note that this is less than the maximum of 70°C that is specified in the absolute maximum data listing. If we must use this package at the maximum ambient we must lower the supply voltage or reduce the output swing.

As a guideline to help in the selection of the LT1229/LT1230 the following table describes the maximum supply voltage that can be used with each part in cable driving applications.

APPLICATIONS INFORMATION

Assumptions:

1. The maximum ambient is 70°C for the commercial parts (C suffix) and 125°C for the full temperature parts (M suffix).
2. The load is a double terminated video cable, 150Ω.
3. The maximum output voltage is 2V (peak or DC).
4. The thermal resistance of each package:

J8 is 100°C/W	J is 80°/W
N8 is 100°C/W	N is 70°/W
S8 is 150°C/W	S is 110°/W

Maximum Supply Voltage for 75Ω Cable Driving Applications at Maximum Ambient Temperature

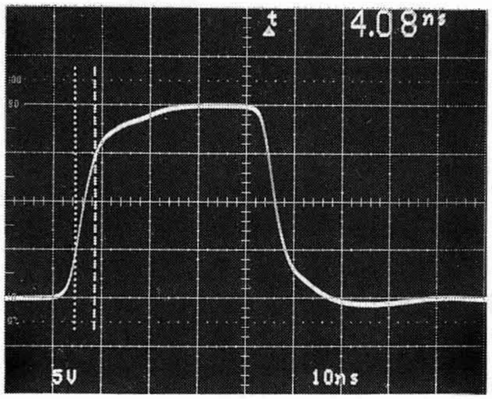
PART	PACKAGE	MAX POWER AT T_A	MAX SUPPLY
LT1229MJ8	Ceramic DIP	0.500W @ 125°C	Vs < ±10.1
LT1229CJ8	Ceramic DIP	1.050W @ 70°C	Vs < ±18.0
LT1229CN8	Plastic DIP	0.800W @ 70°C	Vs < ±15.6
LT1229CS8	Plastic S08	0.533W @ 70°C	Vs < ±10.6
LT1230MJ	Ceramic DIP	0.625W @ 125°C	Vs < ±6.6
LT1230CJ	Ceramic DIP	1.313W @ 70°C	Vs < ±13.0
LT1230CN	Plastic DIP	1.143W @ 70°C	Vs < ±11.4
LT1230CS	Plastic S014	0.727W @ 70°C	Vs < ±7.6

Slew Rate

The slew rate of a current feedback amplifier is not independent of the amplifier gain the way it is in a traditional op amp. This is because the input stage and the output stage both have slew rate limitations. The input stage of the LT1229/LT1230 amplifiers slew at about 100V/μs before they become non-linear. Faster input signals will turn on the normally reverse biased emitters on the input transistors and enhance the slew rate significantly. This enhanced slew rate can be as much as 2500V/μs.

The output slew rate is set by the value of the feedback resistors and the internal capacitance. At a gain of ten with a 1kΩ feedback resistor and ±15V supplies, the output slew rate is typically +700V/μs and −1000V/μs. There is no input stage enhancement because of the high gain.

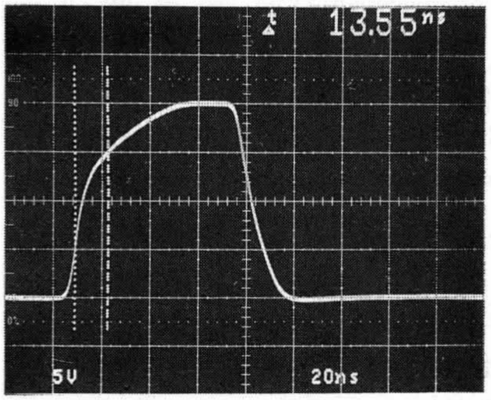
Large Signal Response, $A_V = 2$, $R_F = R_G = 750\Omega$



LT1229 • TA07

Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced.

Large Signal Response, $A_V = 10$, $R_F = 1k$, $R_G = 110\Omega$



LT1229 • TA08

Settling Time

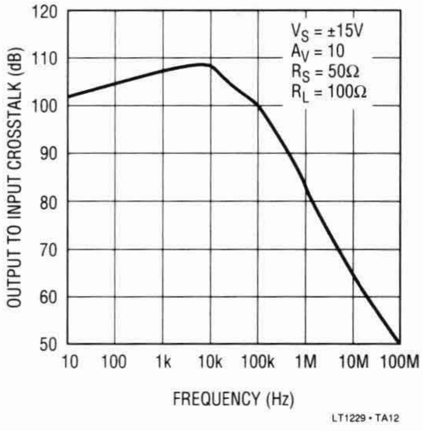
The characteristic curves show that the LT1229/LT1230 amplifiers settle to within 10mV of final value in 40ns to 55ns for any output step up to 10V. The curve of settling to 1mV of final value shows that there is a slower thermal contribution up to 20μs. The thermal settling component comes from the output and the input stage. The output contributes just under 1mV per volt of output change and the input contributes 300μV per volt of input change. Fortunately, the input thermal tends to cancel the output thermal. For this reason the non-inverting gain of two configurations settles faster than the inverting gain of one.

APPLICATIONS INFORMATION

Crosstalk and Cascaded Amplifiers

The amplifiers in the LT1229 and LT1230 do not share any common circuitry. The only thing the amplifiers share is the supplies. As a result, the crosstalk between amplifiers is very low. In a good breadboard or with a good PC board layout the crosstalk from the output of one amplifier to the input of another will be over 100dB down, up to 100kHz and 65dB down at 10MHz. The following curve shows the crosstalk from the output of one amplifier to the input of another.

Amplifier Crosstalk vs Frequency



The high frequency crosstalk between amplifiers is caused by magnetic coupling between the internal wire bonds that connect the IC chip to the package lead frame. The amount of crosstalk is inversely proportional to the load resistor the amplifier is driving, with no load (just the feedback resistor) the crosstalk improves 18dB. The curve shows the crosstalk of the LT1229 amplifier B output (pin 7) to the input of amplifier A. The crosstalk from amplifier A's output (pin 1) to amplifier B is about 10dB better. The crosstalk between all of the LT1230 amplifiers is as shown. The LT1230 amplifiers that are separated by the supplies are a few dB better.

When cascading amplifiers the crosstalk will limit the amount of high frequency gain that is available because the crosstalk signal is out of phase with the input signal. This will often show up as unusual frequency response. For example: cascading the two amplifiers in the LT1229, each set up with 20dB of gain and a –3dB bandwidth of 65MHz into 100Ω will result in 40dB of gain, BUT the response will start to drop at about 10MHz and then flatten out from 20MHz to 30MHz at about 0.5dB down. This is due to the crosstalk back to the input of the first amplifier.

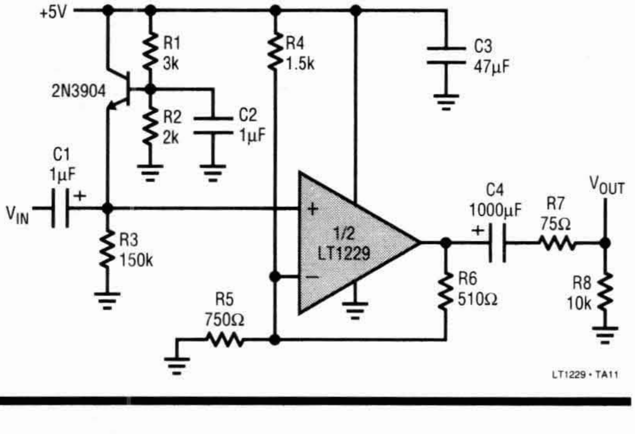
For best results when cascading amplifiers use the LT1229 and drive amplifier B and follow it with amplifier A.

TYPICAL APPLICATIONS

Single +5V Supply Cable Driver for Composite Video

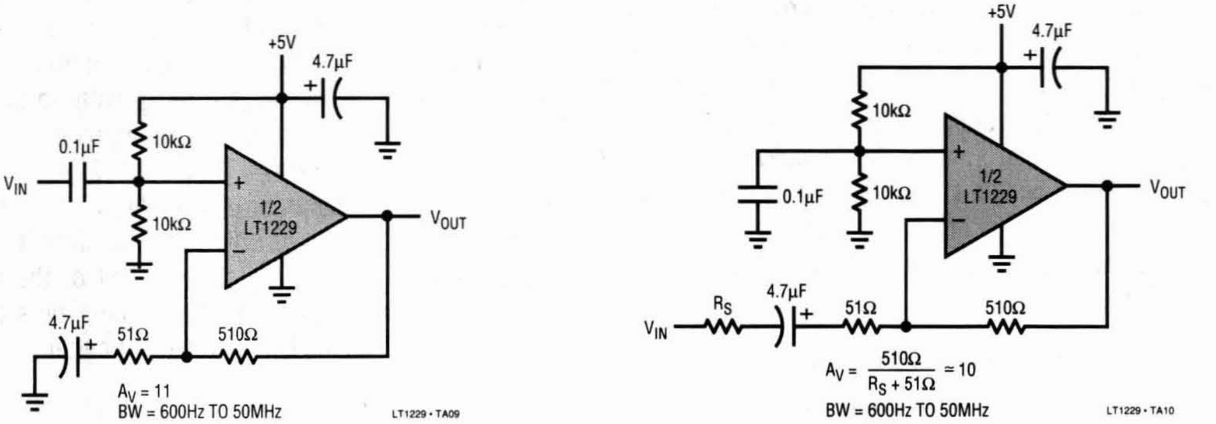
This circuit amplifies standard 1V peak composite video input (1.4Vp-p) by two and drives an AC coupled doubly terminated cable. In order for the output to swing 2.8Vp-p on a single 5V supply, it must be biased accurately. The average DC level of the composite input is a function of the luminance signal. This will cause problems if we AC couple the input signal into the amplifier because a rapid change in luminance will drive the output into the rails. To prevent this we must establish the DC level at the input and operate the amplifier with DC gain.

The transistor's base is biased by R1 and R2 at 2V. The emitter of the transistor clamps the non-inverting input of the amplifier to 1.4V at the most negative part of the input (the sync pulses). R4, R5 and R6 set the amplifier up with a gain of two and bias the output so the bottom of the sync pulses are at 1.1V. The maximum input then drives the output to 3.9V.



TYPICAL APPLICATIONS

Single Supply AC Coupled Amplifiers



Non-Inverting

Inverting

+5V
4.7μF
0.1μF
10kΩ
10kΩ
V_{IN}
1/2 LT1229
V_{OUT}
4.7μF
51Ω
510Ω
+5V
4.7μF
10kΩ
10kΩ
0.1μF
1/2 LT1229
V_{OUT}
R_S
4.7μF
51Ω
510Ω
V_{IN}

$A_V = 11$
BW = 600Hz TO 50MHz

LT1229 • TA09

$A_V = \frac{510\Omega}{R_S + 51\Omega} \approx 10$
BW = 600Hz TO 50MHz

LT1229 • TA10

SECTION 2—AMPLIFIERS

ZERO DRIFT OPERATIONAL AMPLIFIERS

LTC1047, Dual Micropower Zero Drift Operational Amplifier with Internal Capacitors **2-292**
LTC1049, Low Power Zero Drift Operational Amplifier with Internal Capacitors **2-299**
LTC1051/LTC1053, Dual/Quad Precision Zero Drift Operational Amplifiers with Internal Capacitors **2-306**
LTC1150, ±15V Zero Drift Operational Amplifier with Internal Capacitors **2-321**
LTC1151, Dual ±15V Zero Drift Operational Amplifier with Internal Capacitors **13-56**
LTC1250, Very Low Noise Zero Drift Bridge Amplifier **13-80**

LINEAR TECHNOLOGY

LTC1047

Dual Micropower Chopper Stabilized Operational Amplifier with Internal Capacitors

FEATURES

- **No External Components Required**
- Supply Current 80μA
- **Maximum Offset Voltage 10μV**
- **Maximum Offset Voltage Drift 50nV/°C**
- Minimum CMRR 110dB
- Minimum PSRR 110dB
- Single Supply Operation 4.75V to 16V
- Common Mode Range Includes GND
- Output Swings to GND
- Typical Overload Recovery Time 70ms
- Pin Compatible with Industry Standard Dual Op Amps

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Battery Powered Instrumentation
- Strain Gauge Amplifiers
- Remote Located Sensors

DESCRIPTION

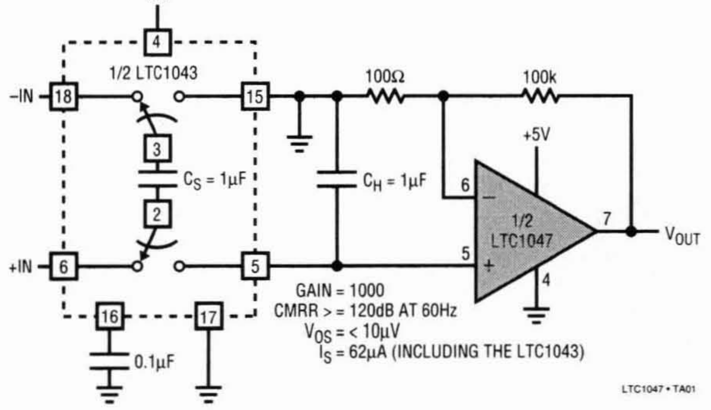
The LTC1047 is a micropower, high performance dual chopper stabilized operational amplifier. The sample-and-hold capacitors usually required by other chopper amplifiers are integrated on-chip, minimizing the need for external components.

The LTC1047 has a typical offset voltage of 3μV, drift of 10nV/°C, input noise voltage typically 3.5μVp-p, and typical voltage gain of 150dB. The common mode rejection is 110dB minimum, with minimum power supply rejection of 110dB. The LTC1047 also offers 0.2V/μs slew rate and a gain bandwidth product of 200kHz. Overload recovery time from saturation is 70ms, four times faster than chopper amplifiers with external capacitors.

The LTC1047 is available in a standard plastic 8-pin DIP as well as a 16-pin SOL package. The LTC1047 is a plug-in replacement for most dual op amps with improved DC performance and substantial power savings.

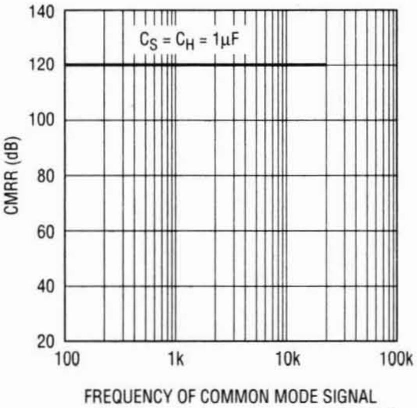
TYPICAL APPLICATION

Micropower Single Supply Instrumentation Amplifier



LTC1047 • TA01

CMRR vs Frequency

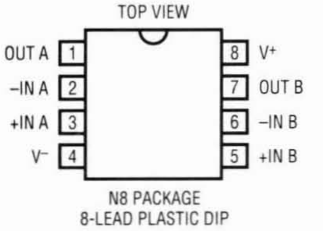


LTC1047 • TPC01

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16V
Input Voltage (Note 2) .... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short Circuit Duration .... Indefinite
Storage Temperature Range .... – 65°C to 150°C
Operating Temperature Range
LTC1047C .... 0°C to 70°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

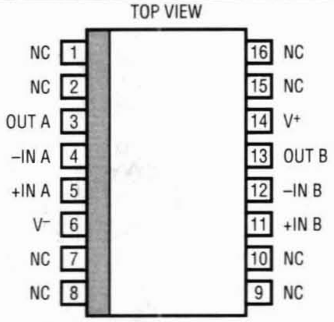
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

LTC1047 • POI01

ORDER PART NUMBER
LTC1047CN8



S PACKAGE
16-LEAD PLASTIC SOL

LTC1047 • POI02

ORDER PART NUMBER
LTC1047CS

ELECTRICAL CHARACTERISTICS $V_S = \pm5V$, T_A = Operating Temperature Range, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	T_A = 25°C (Note 3)			±3	±10	µV
Average Input Offset Voltage Drift	(Note 3)	●		±0.01	±0.05	µV/°C
Long Term Offset Drift				100		nV/rt mo.
Input Bias Current	T_A = 25°C			±5	±30	pA
		●			±300	pA
Input Offset Current	T_A = 25°C			±10	±60	pA
		●			±150	pA
Input Noise Voltage	0.1Hz to 10Hz			3.5		µVp-p
	0.1Hz to 1Hz			0.8		µVp-p
Input Noise Current	f = 10Hz (Note 4)			1.5		fA/rtHz
Common Mode Rejection Ratio	$V_{CM} = V^-$ to +2.7V, T_A = 25°C		110	130		dB
		●	105			dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±8V	●	105	122		dB
Large Signal Voltage Gain	R_L = 100k, V_{OUT} = ±4V	●	120	150		dB
Maximum Output Voltage Swing	R_L = 10k			+4.3/–4.8		V
	R_L = 100k	●	+4.8/–4.9	±4.95		V
Slew Rate	R_L = 100k, C_L = 50pF			0.2		V/µs
Gain Bandwidth Product				200		kHz
Supply Current/Amplifier	No Load, 25°C ≤ T_A ≤ 70°C			60	150	µA
	No Load, 0°C ≤ T_A ≤ 25°C			80	275	µA
Internal Sampling Frequency	T_A = 25°C			680		Hz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

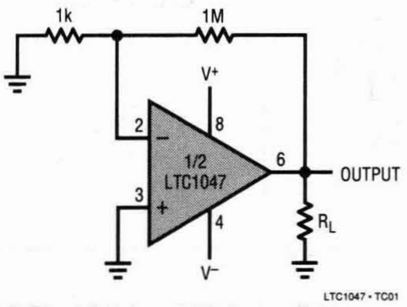
Note 2: Connecting any terminal to voltages greater than V+ or less than V– may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1047.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurements of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

Note 4: Current Noise is calculated from the formula: $I_n = \sqrt{(2q \bullet I_B)}$ where $q = 1.6 \times 10^{-19}$ Coulomb.

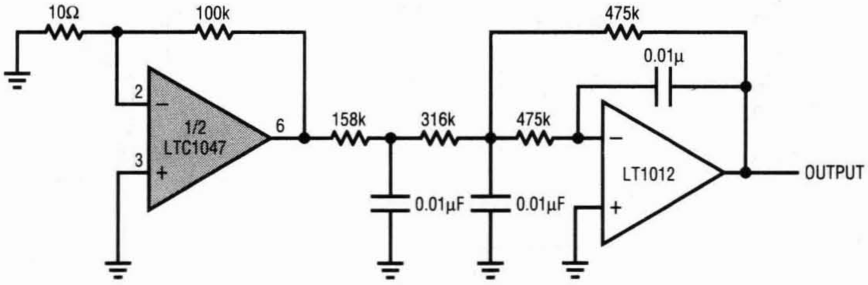
TEST CIRCUITS

Electrical Characteristics Test Circuit



LTC1047 • TC01

DC-10Hz Noise Test Circuit

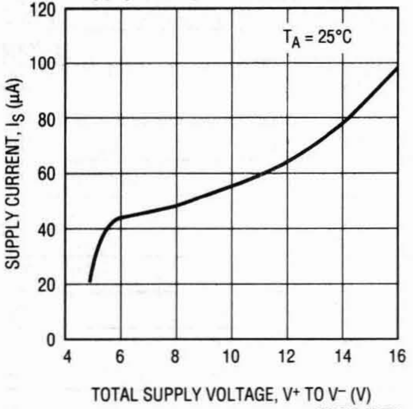


FOR 1Hz NOISE BANDWIDTH, INCREASE ALL CAPACITORS BY A FACTOR OF 10.

LTC1047 • TC02

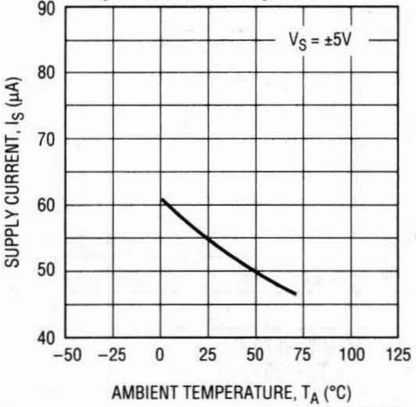
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage Per Amplifier



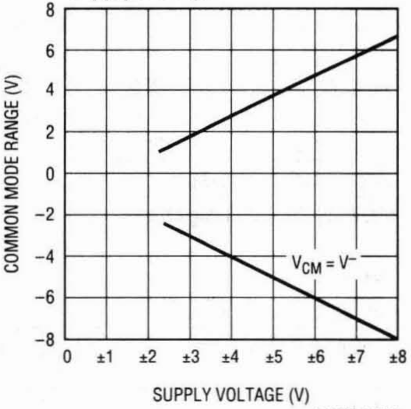
LTC1047 • TPC02

Supply Current vs Temperature Per Amplifier



LTC1047 • TPC03

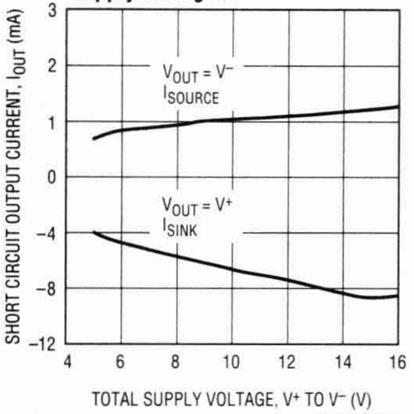
Common Mode Input Range vs Supply Voltage



LTC1047 • TPC04

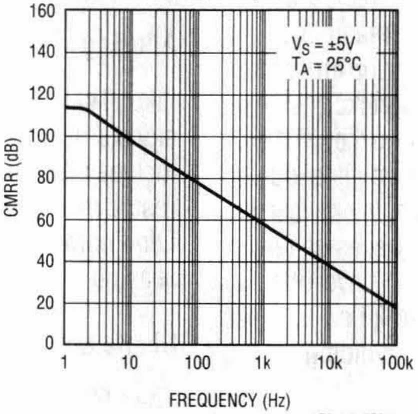
TYPICAL PERFORMANCE CHARACTERISTICS

Output Short Circuit Current vs Supply Voltage



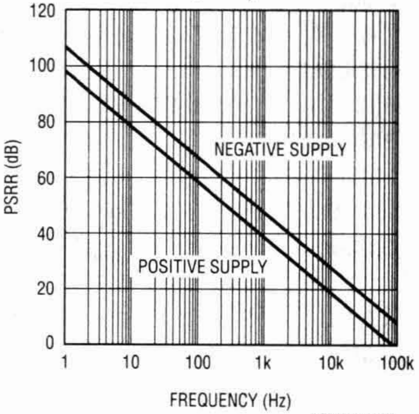
LTC1047 • TPC05

CMRR vs Frequency



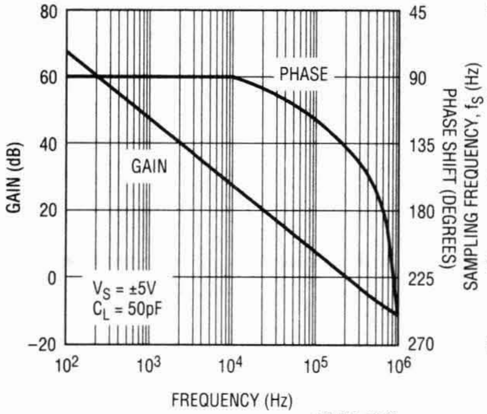
LTC1047 • TPC06

PSRR vs Frequency



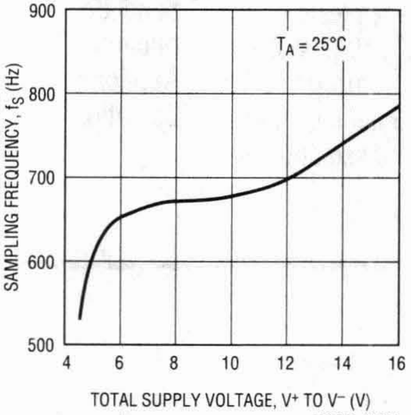
LTC1047 • TPC07

Gain, Phase vs Frequency, ±5V



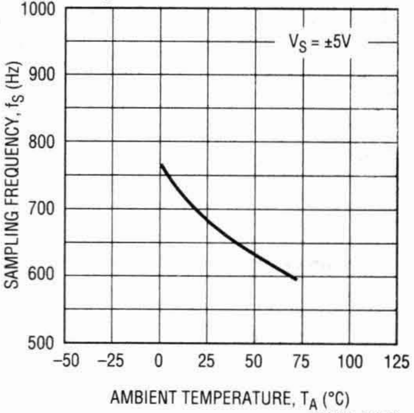
LTC1047 • TPC08

Sampling Frequency vs Supply Voltage



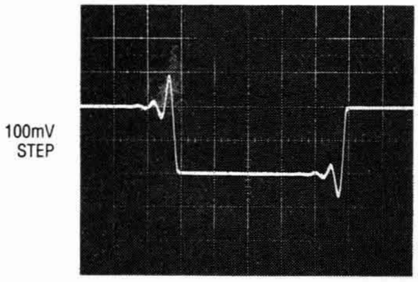
LTC1047 • TPC09

Sampling Frequency vs Temperature



LTC1047 • TPC10

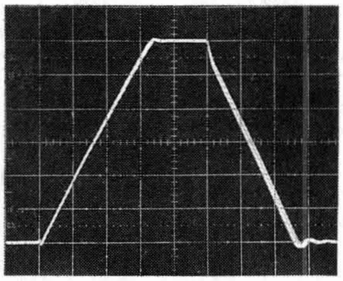
Small Signal Transient Response



$A_V = +1$, $R_L = 100k$, $C_L = 50pF$, $V_S = ±5V$
HORIZONTAL = 10μs/DIV

LTC1047 • TPC11

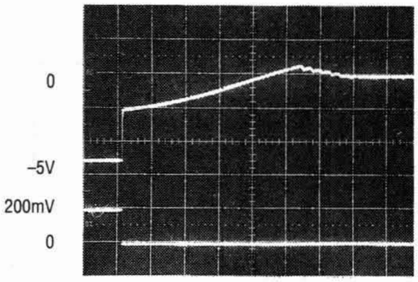
Large Signal Transient Response



$A_V = +1$, $R_L = 100k$, $C_L = 50pF$, $V_S = ±5V$
HORIZONTAL = 10μs/DIV

LTC1047 • TPC12

Overload Recovery



$A_V = −100$, $V_S = ±5V$
HORIZONTAL = 10ms/DIV

LTC1047 • TPC13

APPLICATIONS INFORMATION

Input Considerations

Frequently circuits built with parts as precise as the LTC1047 show errors at the output far greater than the designer expects. Rarely is the problem the op amp; more often the surrounding circuitry is causing errors several orders of magnitude greater than those due to the LTC1047. Such obscure effects as leakage between pins due to residual solder flux and thermocouple effects between the tin/lead solder and the copper PC board traces can overwhelm the pA-level bias currents and the μV-level offset of the LTC1047. For a more complete description of these types of problems (and some advice on avoiding them), see the LTC1051/53 data sheet.

Input Capacitance

The LTC1047 has approximately 12pF of capacitance at each input pin. This will react with large series resistors to form a pole at the input, degrading the LTC1047's phase margin. The problem is especially common with micropower parts like the LTC1047 because high value resistors are often used to minimize power dissipation. As a rule of thumb, bypass feedback resistors larger than 7k with a 20pF capacitor to minimize this effect.

Aliasing

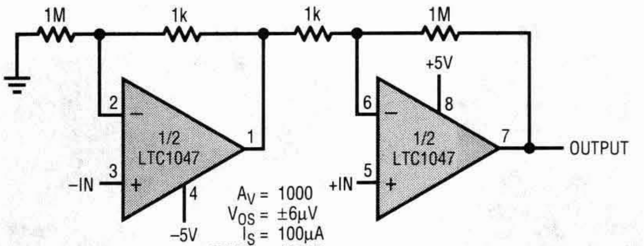
Like all sampled data systems, the LTC1047 will alias input signals near its internal sampling frequency. The design includes internal circuitry to minimize this effect; as a result, most applications do not exhibit aliasing problems. For a complete discussion of the correction circuitry and aliasing behavior, refer to the LTC1051/53 data sheet.

Single Supply Operation

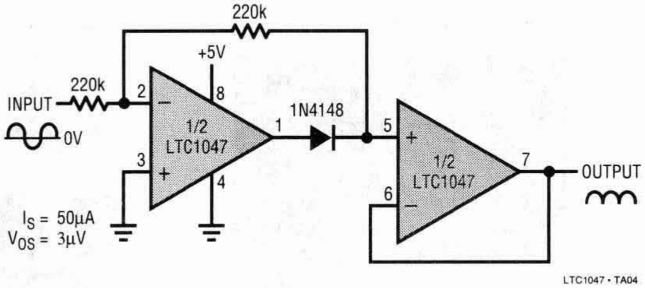
The LTC1047 is compatible with all single supply applications. It has an input common mode range which includes V–, and an output which will swing within millivolts of the negative power supply. The LTC1047 is guaranteed functional down to 4.75V total supply, allowing it to run from minimum TTL voltage all the way up to 16V. See the Typical Applications section for examples of single supply operation.

TYPICAL APPLICATIONS

Low Offset, Low Drift Instrumentation Amplifier

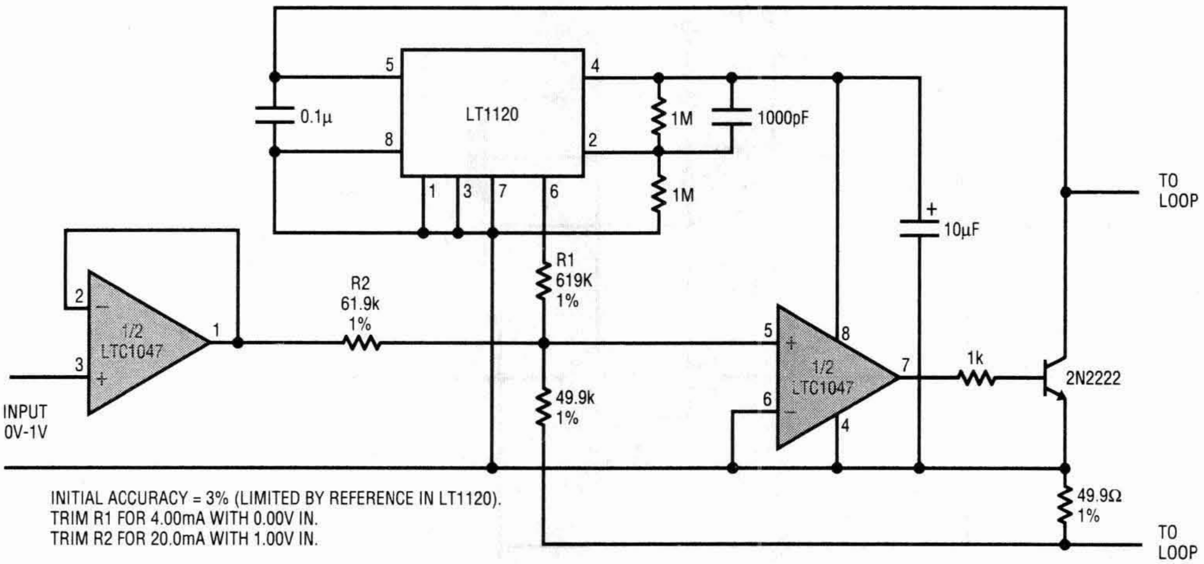


Precise DC Full Wave Rectifier (Absolute Value Circuit)



TYPICAL APPLICATIONS

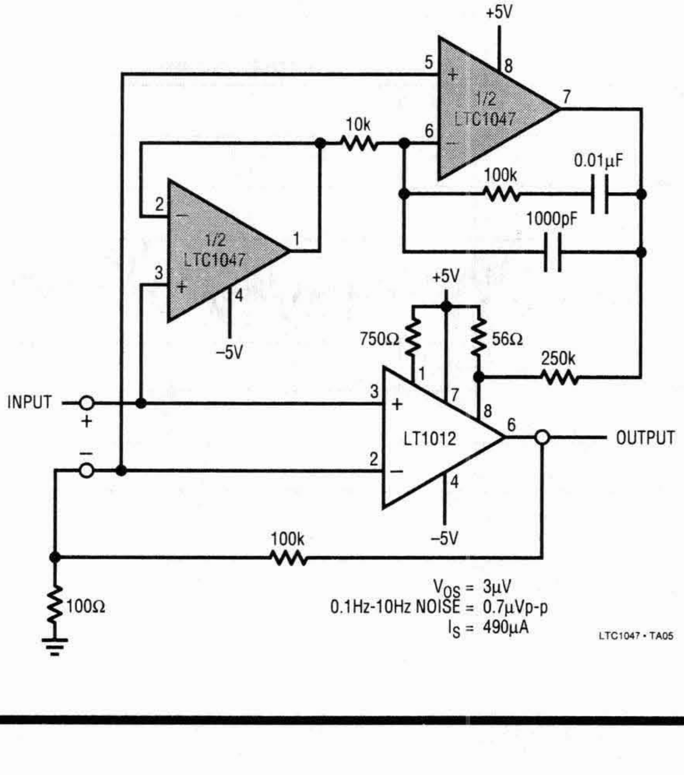
4-20mA Transducer Amplifier


LT1120
5
4
8
2
1
3
7
6
0.1μ
1M
1000pF
1M
+
10μF
TO LOOP
2
–
3
+
1/2 LTC1047
1
INPUT 0V-1V
R2 61.9k 1%
R1 619K 1%
49.9k 1%
5
+
6
–
1/2 LTC1047
8
4
7
1k
2N2222
49.9Ω 1%
TO LOOP

INITIAL ACCURACY = 3% (LIMITED BY REFERENCE IN LT1120).
TRIM R1 FOR 4.00mA WITH 0.00V IN.
TRIM R2 FOR 20.0mA WITH 1.00V IN.

LTC1047 • TA03

Low Noise, Low Drift Composite Amplifier

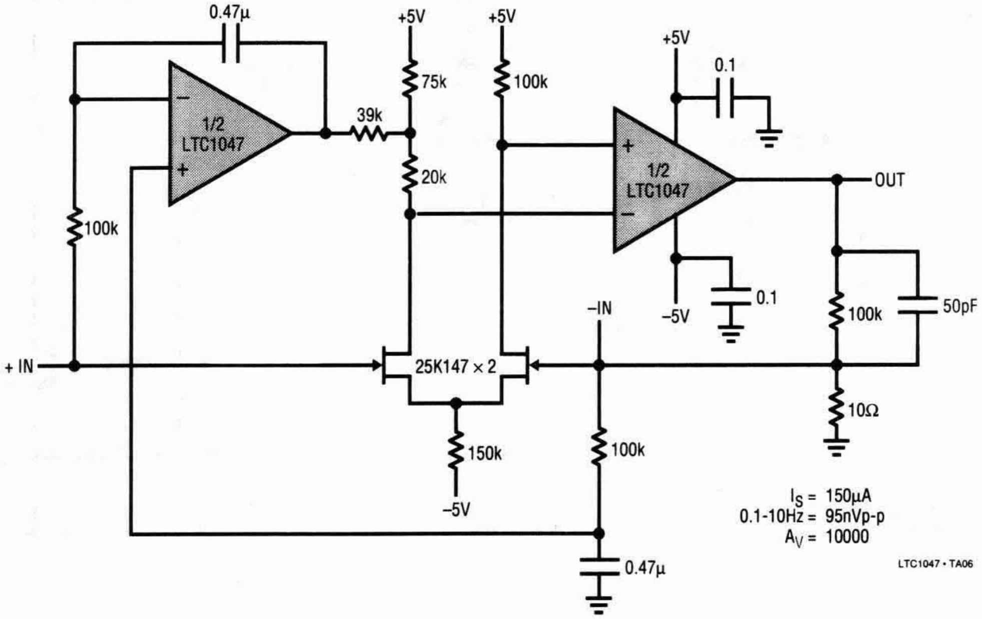

+5V
5
+
8
1/2 LTC1047
7
6
–
10k
0.01μF
100k
1000pF
2
–
1/2 LTC1047
1
3
+
4
–5V
+5V
750Ω
56Ω
250k
1
7
3
+
8
LT1012
6
2
–
4
–5V
INPUT
+
–
OUTPUT
100k
100Ω

V_{OS} = 3μV
0.1Hz-10Hz NOISE = 0.7μVp-p
I_S = 490μA

LTC1047 • TA05

TYPICAL APPLICATIONS

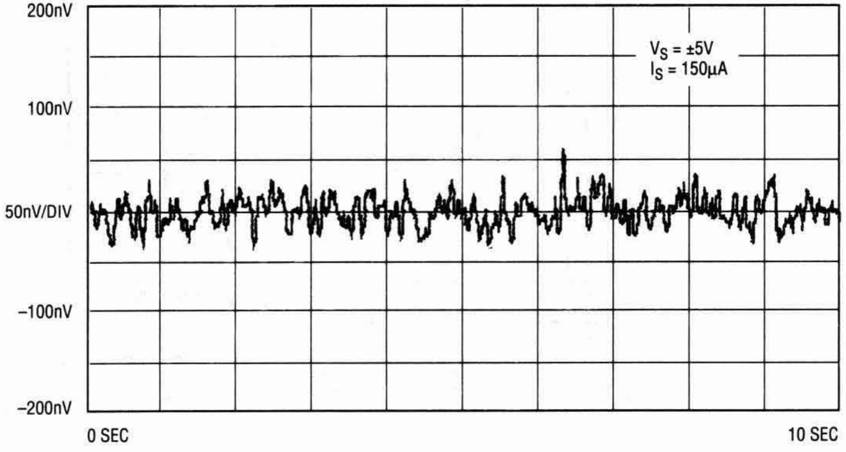
Ultra Low Noise Micropower Chopper


0.47µ
+5V
+5V
+5V
0.1
75k
100k
39k
1/2 LTC1047
20k
1/2 LTC1047
OUT
100k
0.1
–5V
–IN
100k
50pF
+ IN
25K147 × 2
10Ω
150k
100k
–5V
0.47µ

I_S = 150µA
0.1-10Hz = 95nVp-p
A_V = 10000

LTC1047 • TA06

0.1Hz-10Hz NOISE (INPUT REFERRED)



LTC1047 • TA07

LINEAR TECHNOLOGY

LTC1049

Low Power Chopper Stabilized Operational Amplifier with Internal Capacitors

FEATURES

- Low Supply Current 200µA
- No External Components Required
- Maximum Offset Voltage 10µV
- Maximum Offset Voltage Drift 0.1µV/°C
- Single Supply Operation 4.75V to 16V
- Input Common Mode Range Includes Ground
- Output Swings to Ground
- Typical Overload Recovery Time 6ms

APPLICATIONS

- 4mA-20mA Current Loops
- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

The LTC1049 is a high performance, low power chopper stabilized operational amplifier. The two sample-and-hold capacitors usually required externally by other chopper stabilized amplifiers are integrated on the chip. Further, the LTC1049 offers superior DC and AC performance with a nominal supply current of only 200µA.

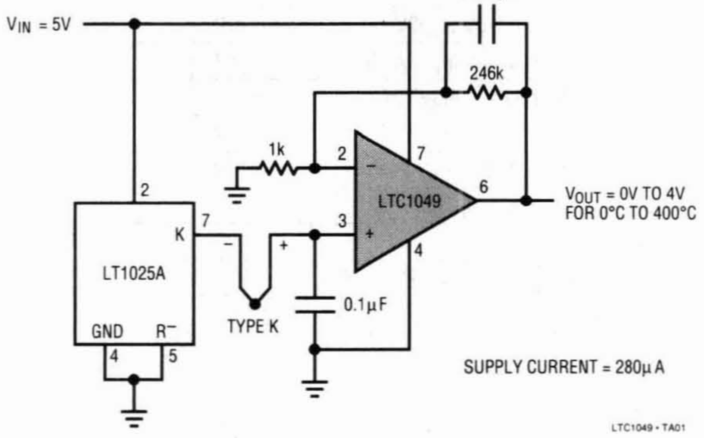
The LTC1049 has a typical offset voltage of 0.5µV, with drift of 0.01µV/°C, 0.1Hz to 10Hz input noise voltage of 3µVp-p and typical voltage gain of 160dB. The slew rate is 0.8V/µs with a gain bandwidth product of 0.8MHz.

Overload recovery time from a saturation condition is 6ms, a significant improvement over chopper amplifiers using external capacitors.

The LTC1049 is available in a standard 8-pin metal can, plastic and ceramic dual in line packages as well as an 8-pin SO package. The LTC1049 can be a plug-in replacement for most standard op amps with improved DC performance and substantial power savings.

TYPICAL APPLICATION

Single Supply Thermocouple Amplifier

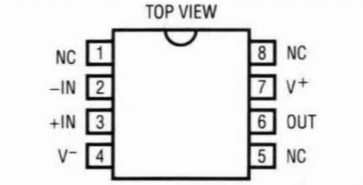


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage (Note 2) .... ($V^+ + 0.3V$) to ($V^- - 0.3V$)
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
LTC1049C .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

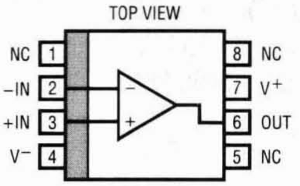


J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

ORDER PART NUMBER

LTC1049CJ8
LTC1049CN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

LTC1049CS8

S8 PART MARKING

1049

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, T_A = operating temperature range, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1049C MIN	TYP	MAX	UNITS
Input Offset Voltage	T_A=25°C(Note 3)			±2	±10	μV
Average Input Offset Drift	(Note 3)	●		±0.02	±0.1	μV/°C
Long Term Offset Voltage Drift				50		nV/√mo
Input Offset Current	T_A= 25°C			±30	±100	pA
		●			±150	
Input Bias Current	T_A= 25°C			±15	±50	pA
		●			±150	
Input Noise Voltage	0.1Hz to 10Hz			3.0		μVp-p
	0.1Hz to 1Hz			1.0		
Input Noise Current	f=10Hz (Note 4)			2.0		fA/√Hz
Common Mode Rejection Ratio	V_{CM}= V^- to 2.7V	●	110	130		dB
Power Supply Rejection Ratio	V_S= ±2.375V to ±8V	●	110	130		dB
Large Signal Voltage Gain	R_L=100kΩ,V_{OUT}= ±4.9V	●	130	160		dB
Maximum Output Voltage Swing	R_L=10kΩ T_A=25°C			−4.9/+4.2		V
		●	−4.6/+3.2			
	R_L=100kΩ	●	±4.9	±4.97		
Slew Rate	R_L=10kΩ, C_L=50pF			0.8		V/μs
Gain Bandwidth Product				0.8		MHz
Supply Current	No Load T_A=25°C			200	300	μA
		●			450	
Internal Sampling Frequency				700		Hz

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1049.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

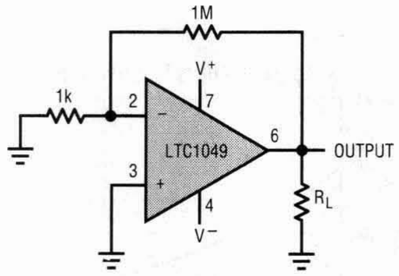
Note 4: Current Noise is calculated from the formula:

$$I_N = \sqrt{(2q \bullet 1b)}$$

where $q = 1.6 \times 10^{-19}$ Coulomb.

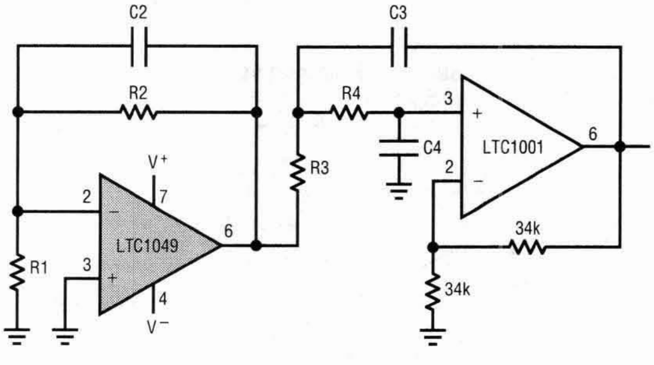
TEST CIRCUITS

Electrical Characteristics Test Circuit



LTC1049 • TC01

DC to 10Hz and DC to 1Hz Noise Test Circuit

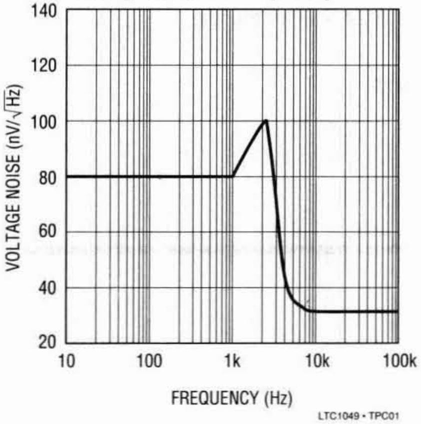


BANDWIDTH	R1	R2	R3	R4	C2	C3	C4
10Hz	16.2Ω	162k	16.2k	16.2Ω	0.1μF	1.0μF	1.0μF
1Hz	16.2Ω	162k	162k	162k	1.0μF	1.0μF	1.0μF

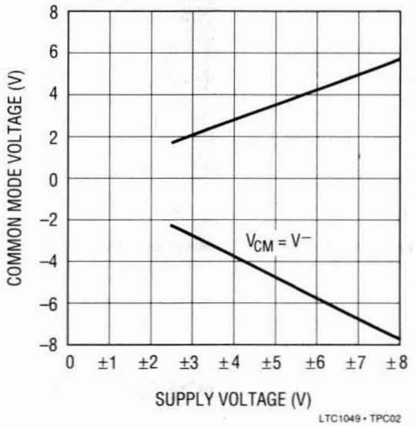
LTC1049 • TC02

TYPICAL PERFORMANCE CHARACTERISTICS

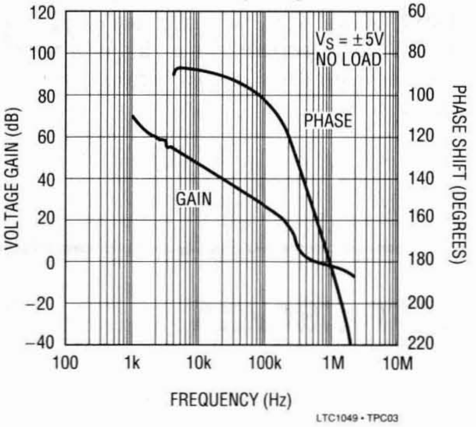
Voltage Noise vs Frequency



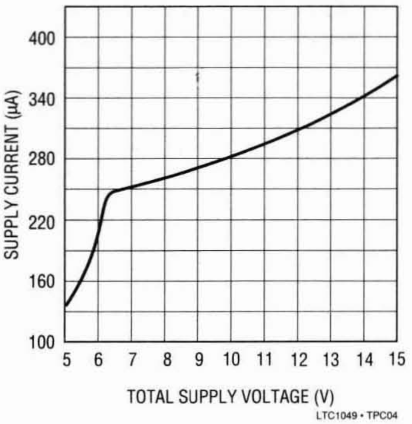
Common Mode Input Range vs Supply Voltage



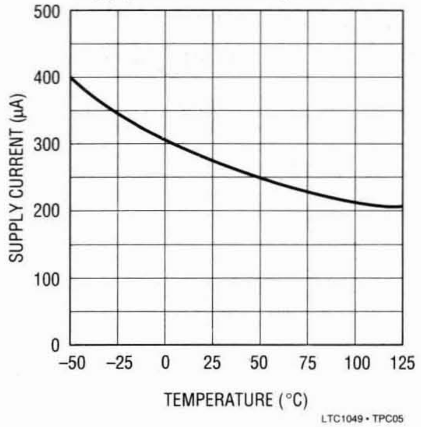
Gain/Phase vs Frequency



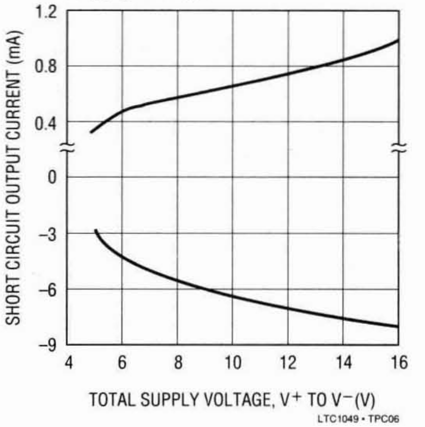
Supply Current vs Supply Voltage



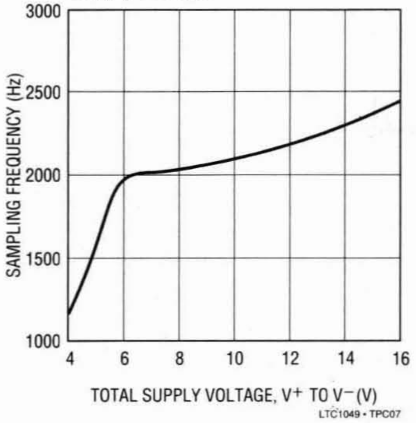
Supply Current vs Temperature



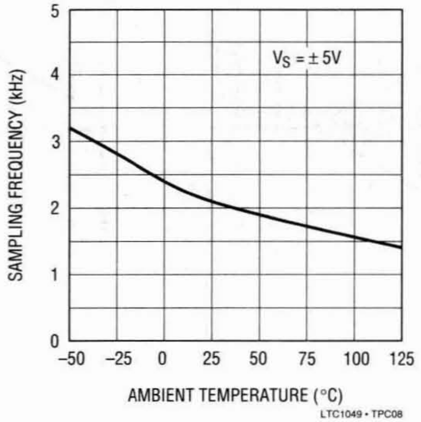
Output Short Circuit Current vs Supply Voltage



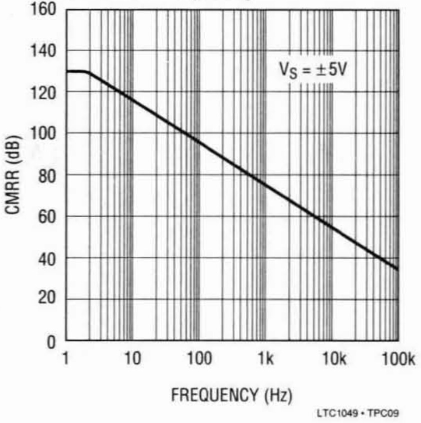
Sampling Frequency vs Supply Voltage



Sampling Frequency vs Temperature

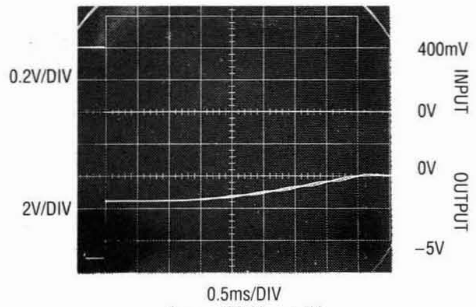


CMRR vs Frequency



TYPICAL PERFORMANCE CHARACTERISTICS

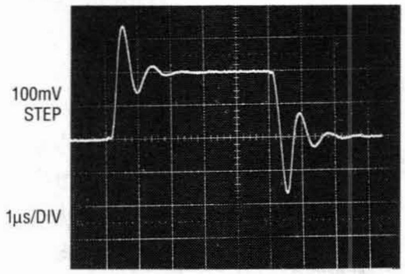
Overload Recovery



$A_V = -100$, $V_S = \pm 5V$

LTC1049 • TPC10

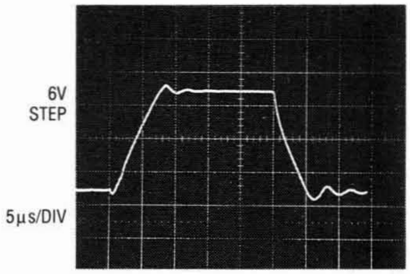
Small Signal Transient Response



$A_V = +1$, $R_L = 10k$, $C_L = 50pF$, $V_S = \pm 5V$

LTC1049 • TPC11

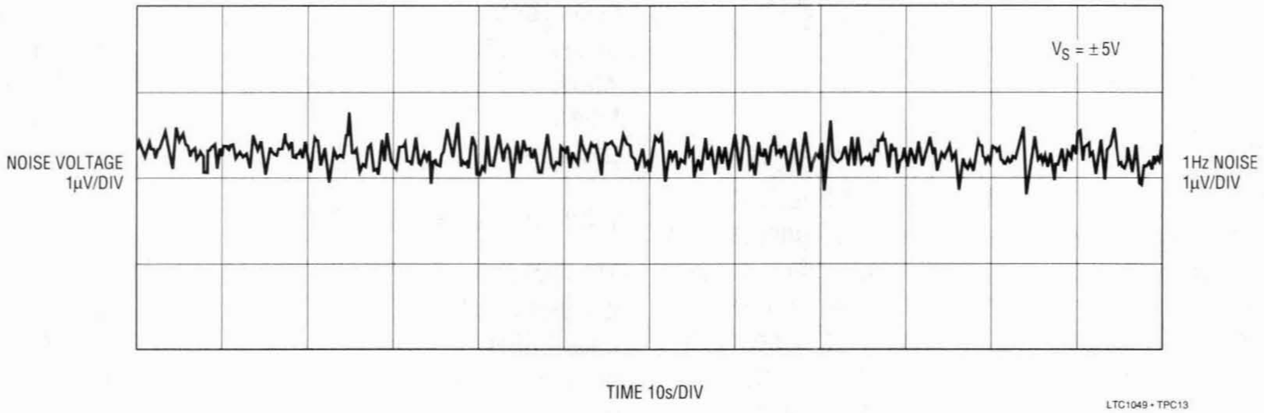
Large Signal Transient Response



$A_V = +1$, $R_L = 10k$, $C_L = 50pF$, $V_S = \pm 5V$

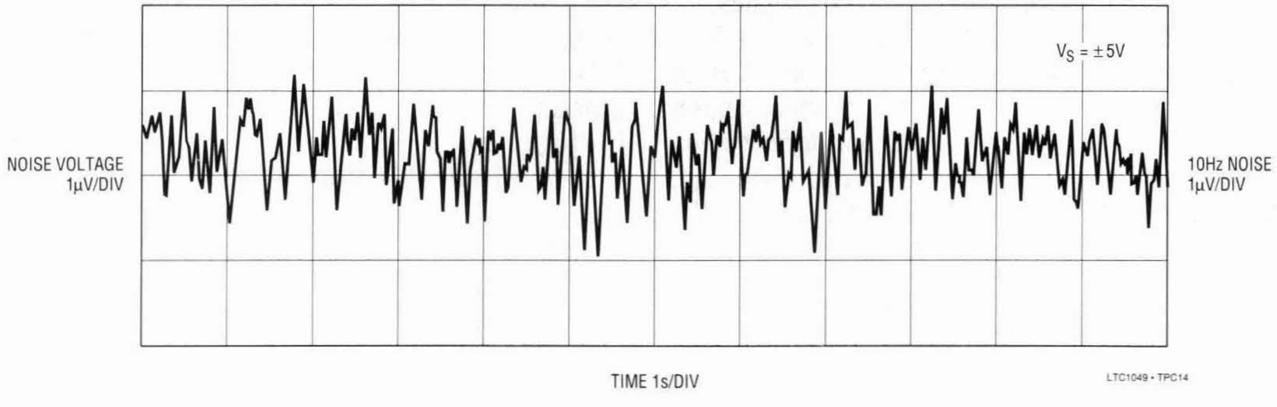
LTC1049 • TPC12

LTC1049 DC to 1Hz Noise



LTC1049 • TPC13

LTC1049 DC to 10Hz Noise



LTC1049 • TPC14

APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1049, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary — particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Microvolts

Thermocouple effects must be considered if the LTC1049's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C — twice the maximum drift specification of the LTC1049. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35µV/°C — 300 times the maximum drift specification of the LTC1049.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches, and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

PACKAGE-INDUCED OFFSET VOLTAGE

Package-induced thermal EMF effects are another important source of errors. It arises at the copper/kovar junctions formed when wire or printed circuit traces contact a package lead. Like all the previously mentioned thermal EMF effects, it is outside the LTC1049's offset nulling loop and cannot be cancelled. The input offset voltage specification of the LTC1049 is actually set by the package-induced warm-up drift rather than by the circuit itself. The thermal time constant ranges from 0.5 to 3 minutes, depending on package type.

LOW SUPPLY OPERATION

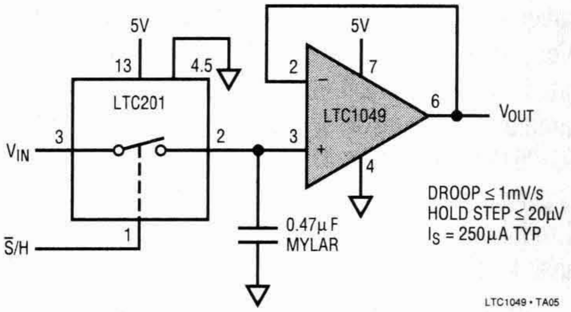
The minimum supply for proper operation of the LTC1049 is typically below 4.0V (±2.0V). In single supply applications, PSRR is guaranteed down to 4.7V (±2.35V) to ensure proper operation down to the minimum TTL specified voltage of 4.75V.

PIN COMPATIBILITY

The LTC1049 is pin compatible with the 8-pin versions of 7650, 7652 and other chopper-stabilized amplifiers. The 7650 and 7652 require the use of two external capacitors connected to pin 1 and 8 which are not needed for the LTC1049. Pins 1, 5, and 8 of the LTC1049 are not connected internally; thus the LTC1049 can be a direct plug in for the 7650 and 7652 even if the two capacitors are left on the circuit board.

TYPICAL APPLICATIONS

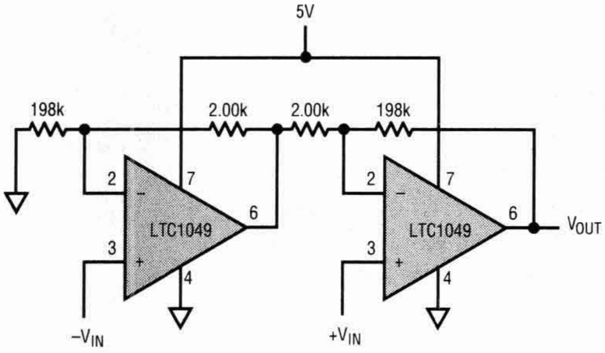
Low Power, Low Hold Step Sample and Hold


5V
13
4.5
LTC201
V_{IN}
3
2
1
$\overline{S}$/H
0.47µF
MYLAR
5V
2
7
3
LTC1049
6
4
V_{OUT}

DROOP ≤ 1mV/s
HOLD STEP ≤ 20µV
I_S = 250µA TYP

LTC1049 • TA05

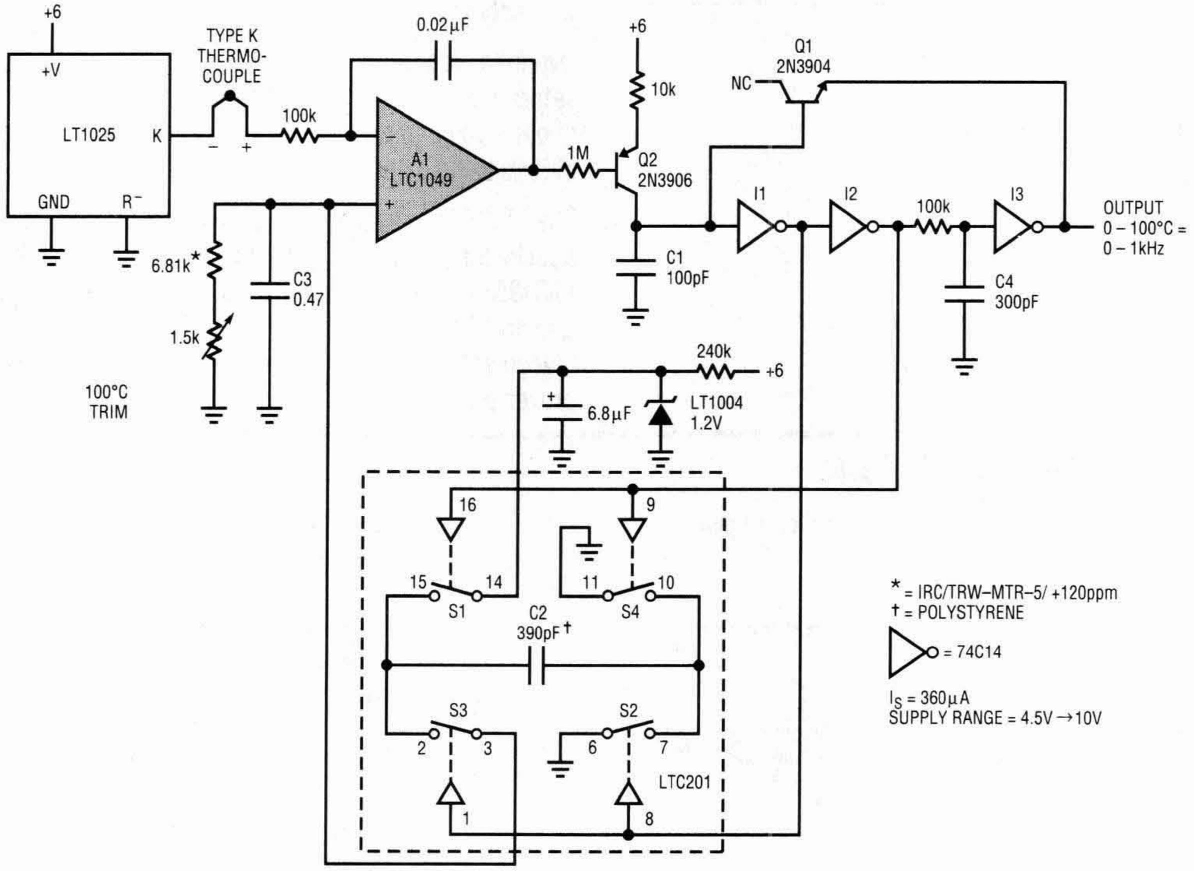
Low Power, Single Supply, Low Offset Instrumentation Amp


5V
198k
2.00k
2.00k
198k
2
7
3
LTC1049
6
4
$-V_{IN}$
2
7
3
LTC1049
6
4
$+V_{IN}$
V_{OUT}

GAIN = 100
I_S = 400µA
CMRR ≥ 60dB, WITH 0.1% RESISTORS (RESISTOR LIMITED)

LTC1049 • TA06

Thermocouple Based Temperature to Frequency Converter


+6
+V
LT1025
K
GND
R⁻
TYPE K
THERMO-
COUPLE
−
+
100k
0.02µF
A1
LTC1049
6.81k*
1.5k
100°C
TRIM
C3
0.47
+6
10k
1M
Q2
2N3906
C1
100pF
NC
Q1
2N3904
I1
I2
100k
I3
C4
300pF
OUTPUT
0 – 100°C =
0 – 1kHz
240k
+6
6.8µF
LT1004
1.2V
16
9
15
14
S1
11
10
S4
C2
390pF†
S3
S2
2
3
6
7
1
8
LTC201

* = IRC/TRW–MTR–5/ +120ppm
† = POLYSTYRENE
▷○ = 74C14
I_S = 360µA
SUPPLY RANGE = 4.5V → 10V

LTC1049 • TA07

LTC1051/LTC1053

Dual/Quad Precision Chopper Stabilized Operational Amplifiers With Internal Capacitors

FEATURES

- Dual/Quad Low Cost Precision Op Amp
- No External Components Required
- Maximum Offset Voltage 5μV
- Maximum Offset Voltage Drift 0.05μV/°C
- Low Noise 1.5$\mu V_{p\text{-}p}$ (0.1Hz to 10Hz)
- Minimum Voltage Gain, 120dB
- Minimum PSRR, 120dB
- Minimum CMRR, 114dB
- Low Supply Current 1mA/Op Amp
- Single Supply Operation 4.75V to 16V
- Input Common Mode Range Includes Ground
- Output Swings to Ground
- Typical Overload Recovery Time 3ms
- Pin Compatible with Industry Standard Dual and Quad Op Amps

APPLICATIONS

- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition
- DC Accurate R, C Active Filters

DESCRIPTION

The LTC1051/LTC1053 is a high performance, low cost dual/quad chopper stabilized operational amplifier. The unique achievement of the LTC1051/LTC1053 is that it integrates on chip the sample-and-hold capacitors usually required externally by other chopper amplifiers. Further, the LTC1051/LTC1053 offers better combined overall DC and AC performance than is available from other chopper stabilized amplifiers with or without internal sample/hold capacitors

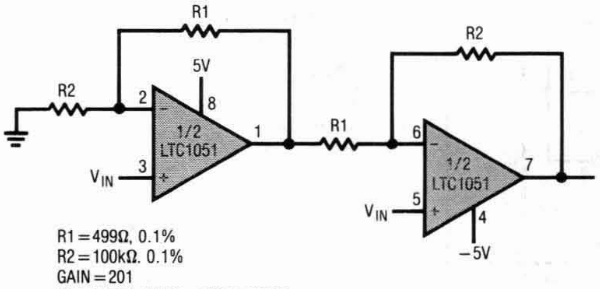
The LTC1051/LTC1053 has an offset voltage of 0.5μV, drift of 0.01μV/°C, DC to 10Hz, input noise voltage typically 1.5$\mu V_{p\text{-}p}$ and typical voltage gain of 140dB. The slew rate of 4V/μs and gain bandwidth product of 2.5MHz are achieved with only 1mA of supply current per op amp.

Overload recovery times from positive and negative saturation conditions are 1.5ms and 3ms respectively, about a 100 or more times improvement over chopper amplifiers using external capacitors.

The LTC1051 is available in standard plastic and ceramic dual in line packages as well as a 16-pin SOL package. The LTC1053 is available in a standard 14-pin plastic package and an 18-pin SOIC. The LTC1051/LTC1053 is a plug in replacement for most standard dual/quad op amps with improved performance.

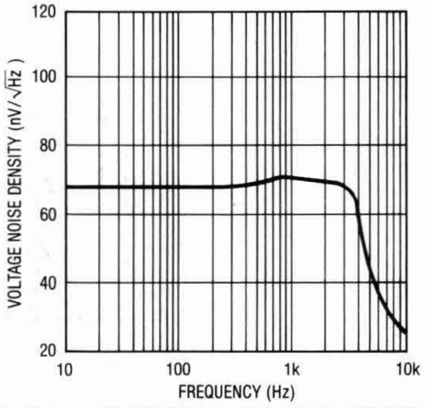
TYPICAL APPLICATION

High Performance Low Cost Instrumentation Amplifier



R1 = 499Ω, 0.1%
R2 = 100kΩ. 0.1%
GAIN = 201
MEASURED CMRR ~ 120dB AT DC
MEASURED INPUT V_{OS} 3μV
MEASURED INPUT NOISE 2μVp-p (DC − 10Hz)

LTC1051 Noise Spectrum

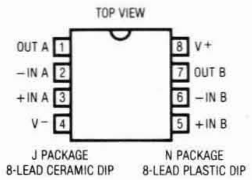
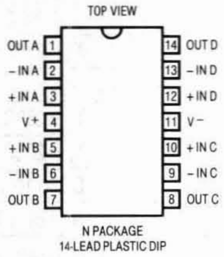
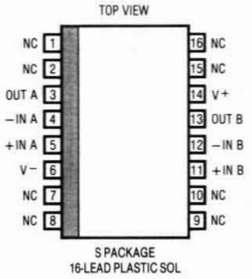
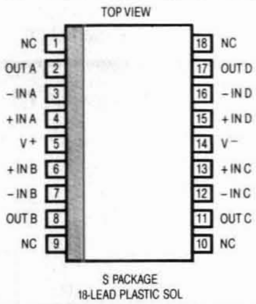


ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V−) 16.5V
Input Voltage ....(V+ + 0.3V) to (V− − 0.3V)
Output Short Circuit Duration .... Indefinite

Operating Temperature Range
LTC1051M, LTC1051AM .... −55°C to 125°C
LTC1051C/LTC1053C, LTC1051AC .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
 TOP VIEW OUT A 1 −IN A 2 +IN A 3 V− 4 8 V+ 7 OUT B 6 −IN B 5 +IN B J PACKAGE 8-LEAD CERAMIC DIP N PACKAGE 8-LEAD PLASTIC DIP	LTC1051MJ8 LTC1051CJ8 LTC1051CN8 LTC1051AMJ8 LTC1051ACJ8 LTC1051ACN8	 TOP VIEW OUT A 1 −IN A 2 +IN A 3 V+ 4 +IN B 5 −IN B 6 OUT B 7 14 OUT D 13 −IN D 12 +IN D 11 V− 10 +IN C 9 −IN C 8 OUT C N PACKAGE 14-LEAD PLASTIC DIP	LTC1053CN
 TOP VIEW NC 1 NC 2 OUT A 3 −IN A 4 +IN A 5 V− 6 NC 7 NC 8 16 NC 15 NC 14 V+ 13 OUT B 12 −IN B 11 +IN B 10 NC 9 NC S PACKAGE 16-LEAD PLASTIC SOL	LTC1051CS LTC1051ACS	 TOP VIEW NC 1 OUT A 2 −IN A 3 +IN A 4 V+ 5 +IN B 6 −IN B 7 OUT B 8 NC 9 18 NC 17 OUT D 16 −IN D 15 +IN D 14 V− 13 +IN C 12 −IN C 11 OUT C 10 NC S PACKAGE 18-LEAD PLASTIC SOL	LTC1053CS

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, T_A = operating temperature range unless otherwise specified.

			LTC1051/LTC1053			LTC1051A			
PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$			±0.5	±5		±0.5	±5	μV
Average Input Offset Drift		●		±0.0	±0.05		±0.0	±0.05	μV/°C
Long Term Offset Drift				50			50		nV/√Mo
Input Bias Current	$T_A = 25°C$			±15	±65		±15	±50	pA
LTC1051C/LTC1053C		●			±135			±100	pA
LTC1051M		●			±450			±300	pA
Input Offset Current (All Grades)	$T_A = 25°C$			±30	±125		±30	±100	pA
		●			±175			±150	pA
Input Noise Voltage (Note 1)	$R_S = 100\Omega$, DC to 10Hz			1.5			1.5	2	μV_{p-p}
	$R_S = 100\Omega$, DC to 1Hz			0.4			0.4		μV_{p-p}
Input Noise Current	f = 10Hz			2.2			2.2		fA/√Hz
Common Mode Rejection Ratio, CMRR	$V_{CM} = V-$ to $+2.7V$, $T_A = 25°C$		106	130		114	130		dB
		●	100			110			dB
Differential CMRR LTC1051, LTC1053 (Note 2)	$V_{CM} = V^-$ to $+2.7V$, $T_A = 25°C$		112			112			dB
Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 8V$	●	116	140		120	140		dB
Large Signal Voltage Gain	$R_L = 10k\Omega$, $V_{OUT} = \pm 4V$	●	116	160		120	160		dB
Maximum Output Voltage Swing	$R_L = 10k\Omega$	●	±4.5	±4.85		±4.7	±4.85		V
	$R_L = 100k\Omega$		±4.5	±4.95			±4.95		V
Slew Rate	$R_L = 10k\Omega$, $C_L = 50pF$			4			4		V/μs

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, T_A = operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS		LTC1051A/LTC1051/LTC1053 MIN	 TYP	 MAX	UNITS
Gain Bandwidth Product				2.5		MHz
Supply Current/Op Amp	No Load, $T_A = 25°C$			1	2	mA
		●			2.5	mA
Internal Sampling Frequency				3		kHz

V_S = 5V, GND, T_A = operating temperature range unless otherwise specified.

PARAMETER	CONDITIONS		LTC1051A/LTC1051/LTC1053 MIN	 TYP	 MAX	UNITS
Input Offset Voltage	$T_A = 25°C$			±0.5	±5	µV
Input Offset Drift				±0.01	±0.05	µV/°C
Input Bias Current	$T_A = 25°C$			±10	±50	pA
Input Offset Current	$T_A = 25°C$			±20	±80	pA
Input Noise Voltage	DC to 10Hz			1.8		$µV_{P-P}$
Supply Current/Op Amp	No Load, $T_A = 25°C$	●			1.5	mA

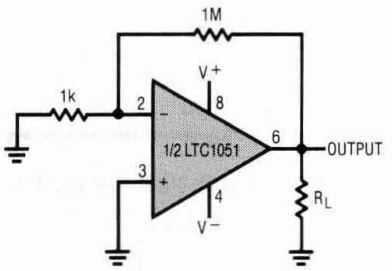
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: For guaranteed noise specification contact LTC marketing.

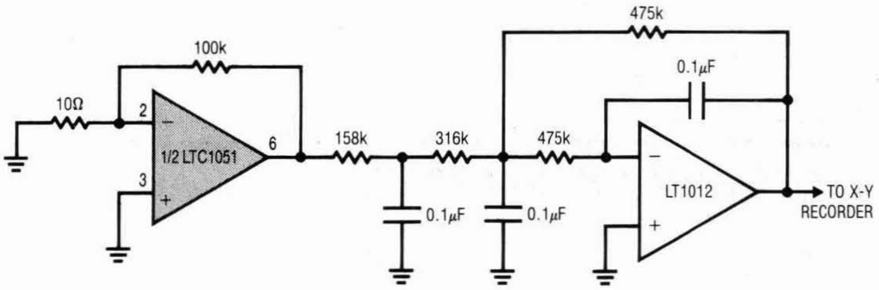
Note 2: Differential CMRR for the LTC1053 is measured between amplifiers A and D, and amplifiers B and C.

TEST CIRCUITS

Electrical Characteristics Test Circuit



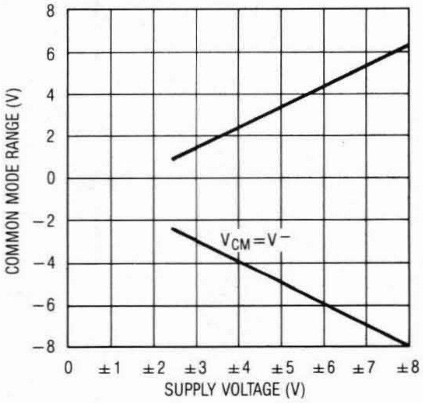
DC-10Hz Noise Test Circuit



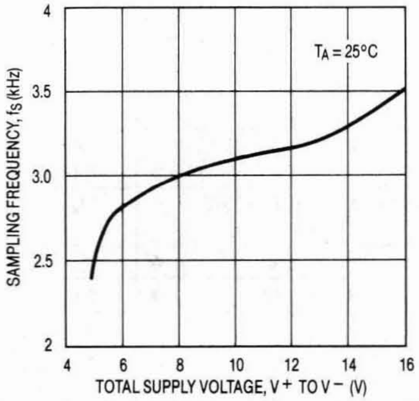
FOR 1Hz NOISE BW INCREASE ALL THE CAPACITORS BY A FACTOR OF 10.

TYPICAL PERFORMANCE CHARACTERISTICS

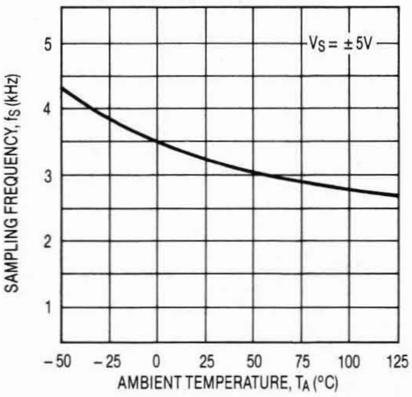
Common Mode Input Range vs Supply Voltage



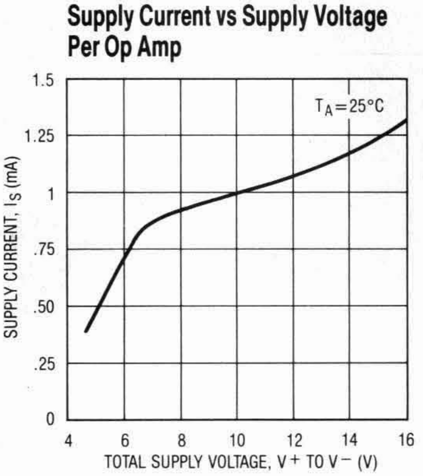
Sampling Frequency vs Supply Voltage

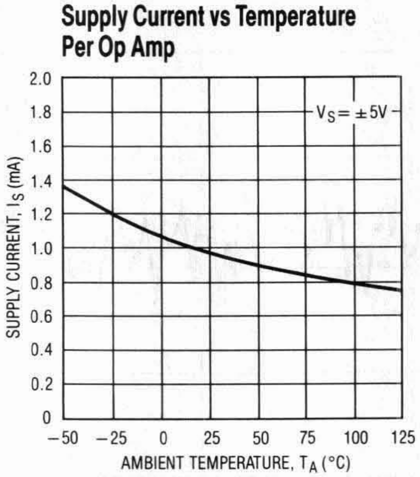


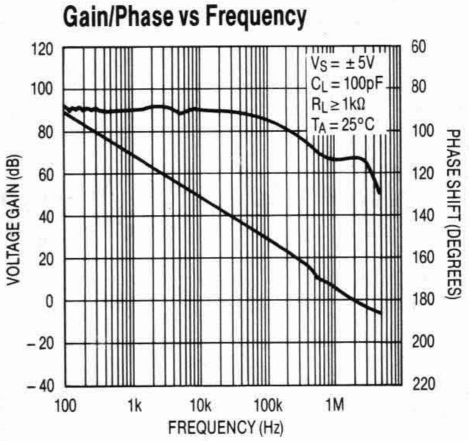
Sampling Frequency vs Temperature

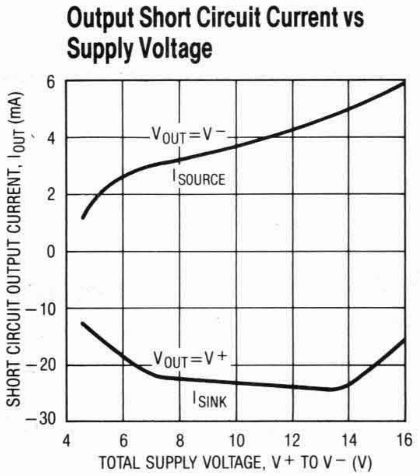


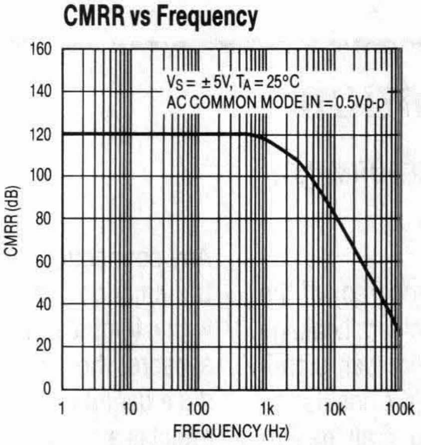
TYPICAL PERFORMANCE CHARACTERISTICS

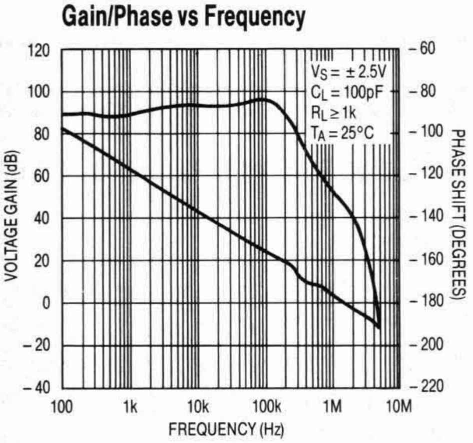

Supply Current vs Supply Voltage Per Op Amp

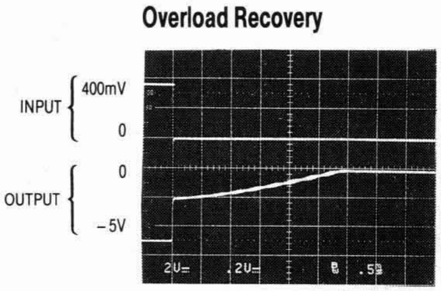

Supply Current vs Temperature Per Op Amp


Gain/Phase vs Frequency

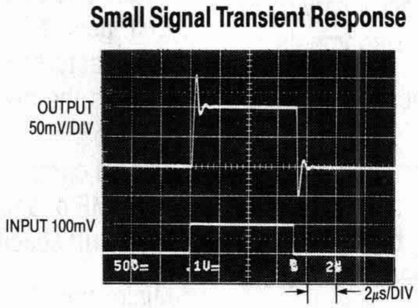

Output Short Circuit Current vs Supply Voltage


CMRR vs Frequency

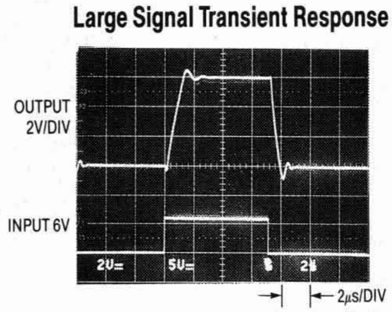

Gain/Phase vs Frequency


Overload Recovery

$A_V = -100$, $V_S = \pm 5V$


Small Signal Transient Response

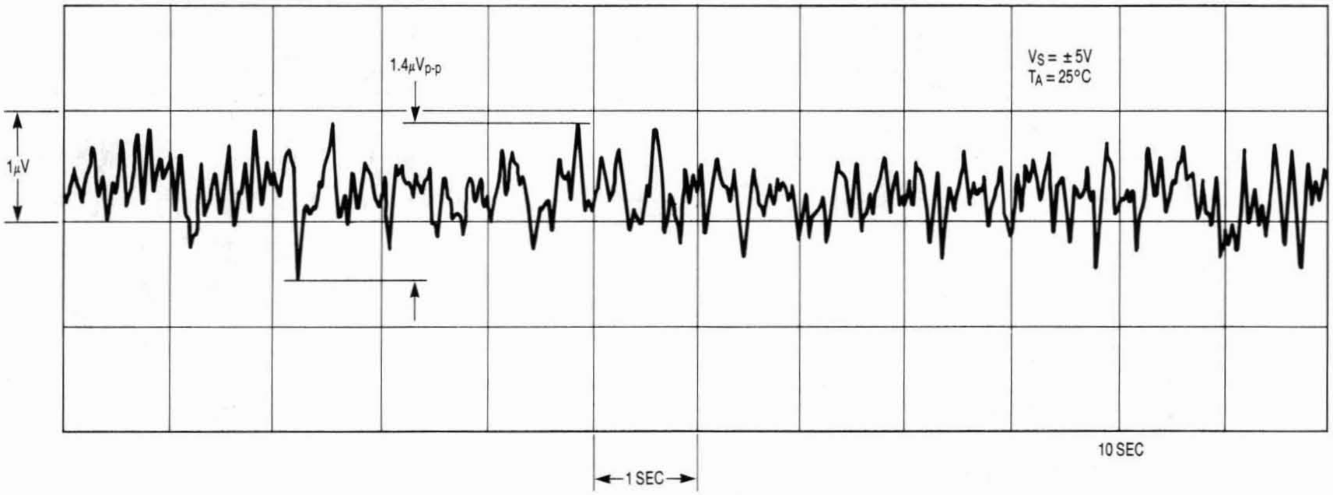
$A_V = +1$, $R_L = 10k$, $C_L = 100pF$
$V_S = \pm 5V$, $T_A = 25°C$


Large Signal Transient Response

$A_V = +1$, $R_L = 10k$, $C_L = 100pF$
$V_S = \pm 5V$, $T_A = 25°C$

TYPICAL PERFORMANCE CHARACTERISTICS

LTC1051/LTC1053 DC to 10Hz Noise



APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1051/LTC1053, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary — particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Microvolts

Thermocouple effects must be considered if the LTC1051/LTC1053's ultra low drift op amps are to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C — 4 times the maximum drift specification of the LTC1051/LTC1053. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35μV/°C — 700 times the maximum drift specification of the LTC1051/LTC1053.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of juctions in the amplifier's input signal path. Avoid connectors, sockets, switches and relays where possible. In instances where this is not possible, attempt

APPLICATIONS INFORMATION

to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The termal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

Table 1. Resistor Thermal EMF

Resistor Type	Thermal EMF/°C Gradient
Tin Oxide	~mV/°C
Carbon Composition	~450μV/°C
Metal Film	~20μV/°C
Wire Wound	
Evenohm	~2μV/°C
Manganin	~2μV/°C

INPUT BIAS CURRENT, CLOCK FEEDTHROUGH

At ambient temperatures below 60°C, the input bias current of the LTC1051/LTC1053 op amps is dominated by the small amount of charge injection occurring during the sampling and holding of the op amps input offset voltage. The average value of the resulting current pulses is 10pA to 15pA with sign convention shown in Figure 1.

As the ambient temperature rises, the leakage current of the input protection devices increases, while the charge injection component of the bias current, for all practical purposes, stays constant. At elevated temperatures (above 85°C) the leakage current dominates and the bias current of both inputs assumes the same sign.

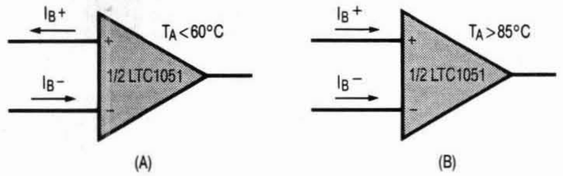


Figure 1. LTC1051 Bias Current

The charge injection at the op amp input pins will cause small output spikes. This phenomenon is often referred to as "clock feedthrough" and it can be easily observed when the closed loop gain exceeds 10V/V, Figure 2. The magnitude of the clock feedthrough is temperature independent but it increases when the closed loop gain goes up, when the source resistance increases, and when the gain setting resistors increase, Figure 2A, 2B. It is important to note that the output small spikes are centered at 0V level and they do not add to the output offset error budget. For instance, with $R_S = 1M\Omega$, the typical output offset voltage of Figure 2C is $V_{OS(OUT)} \approx 10^8 \times I_B^+ + 101V_{OS}(in)$. A 10pA bias current will yield an output of 1mV ± 100μV. The output clock feedthrough can be attenuated by lowering the value of the gain setting resistors, i.e. R2 = 10k, R1 = 100Ω, instead of (100k, 1k; Figure 2).

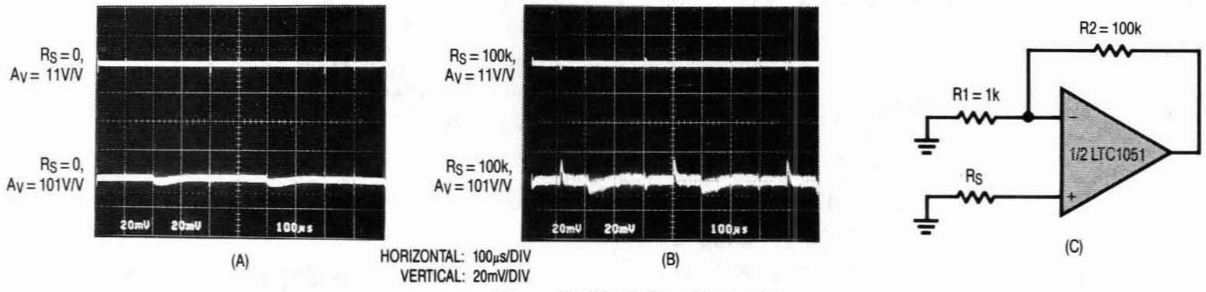


Figure 2. Clock Feedthrough

APPLICATIONS INFORMATION

Clock feedthrough can also be attenuated by adding a capacitor across the feedback resistor to limit the circuit bandwidth below the internal sampling frequency, Figure 3.

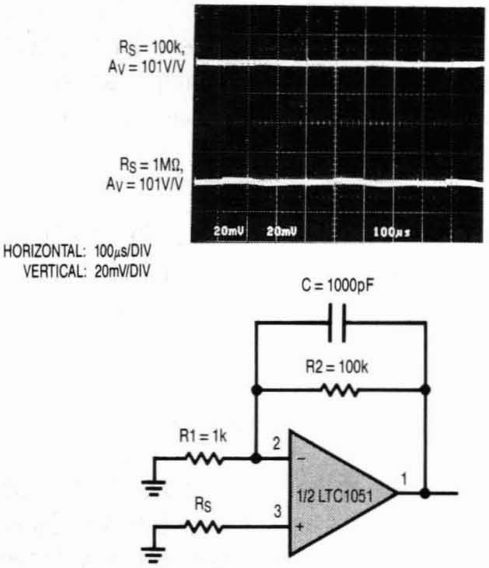


Figure 3. Adding a Feedback Capacitor to Eliminate Clock Feedthrough

INPUT CAPACITANCE

The input capacitance of the LTC1051/LTC1053 op amps is approximately 12pF. When the LTC1051/LTC1053 op amps are used with feedback factors approaching unity, the feedback resistor value should not exceed 7kΩ for industrial temperature range and 5kΩ for military temperature range. If a higher feedback resistor value is required, a feedback capacitor of 20pF should be placed across the feedback resistor. Note that the most common circuits with feedback factors approaching unity are unity gain followers and instrumentation amplifier front ends, Figure 4.

LTC1051/LTC1053 AS AC AMPLIFIERS

Although initially chopper stabilized op amps were designed to minimize DC offsets and offset drifts, the LTC1051/LTC1053 family, on top of its outstanding DC characteristics, presents efficient AC performance. For instance, at single +5V supply, each op amp typically consumes 0.5mA and still provides 1.8MHz gain bandwidth product and 3V/µs slew rate. This, combined with almost distortionless swing to the supply rails, Figure 8, makes the LTC1051/LTC1053 op amps nearly general purpose. To further expand this idea, the "aliasing" phenomenon, which could occur under AC conditions, should be described and properly evaluated.

ALIASING

The LTC1051/LTC1053 are equipped with internal circuitry to minimize aliasing. Aliasing, no matter how small, occurs when the input signal approaches and exceeds the internal clock frequency. Aliasing is caused by the sampled data nature of the chopper op amps. A generalized study of this phenomenon is beyond the scope of a datasheet, however, a set of rules of thumb can answer many questions.

1. Alias signals can be generally defined as output AC signals at a frequency of $nf_{CLK} \pm mf_{IN}$. The nf_{CLK} term is the internal sampling frequency of the chopper stabilized op amps, and its harmonics, mf_{IN} is the frequency of the input signal and its harmonics, if any.
2. If we arbitrarily accept that "aliasing" occurs when output alias signals reach an amplitude of 0.01% or more of the output signal, then: The approximate minimum frequency of an AC input signal which will cause aliasing is equal to the internal clock frequency multiplied by the square root of the op amp feedback factor. For instance, with closed loop gain of −10, the feedback factor is 1/11, and if $f_{CLK} = 2.6kHz$, alias signals can be detected when the frequency of the input signal exceeds 750Hz to 800Hz, Figure 5A.

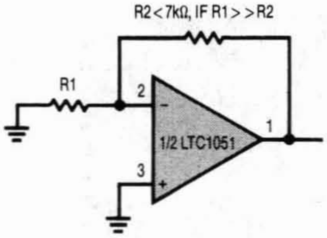


Figure 4. Operating the LTC1051 with Feedback Factors Approaching Unity

APPLICATIONS INFORMATION

3. The number of alias signals increases when the input signal frequency increases, Figure 5B.

4. When the frequency, f_{IN}, of the input signal is less than f_{CLOCK}, the alias signal(s) amplitude(s) directly scale with the amplitude of the incoming signal. The output "signal to alias ratio" cannot be increased by just boosting the input signal amplitude. However, when the input AC signal frequency well exceeds the clock frequency, the amplitude of the alias signals does not directly scale with the input amplitude. The "signal to alias ratio" increases when the output swings closely to the rails, Figures 5B, 7. It is important to note that the LTC1051/LTC1053 op amps under light loads ($R_L \geq 10k\Omega$) swing closely to the supply rails without generating harmonic distortion, Figure 8.

5. For unity gain inverting configuration, all the alias frequencies are 80dB to 84dB down from the output signal, Figures 6A, 6B. Combined with excellent THD under wide swing, the LTC1051/LTC1053 op amps make efficient unity gain inverters.

   For gain higher than −1, the "signal to alias" ratio decreases at an approximate rate of −6dB per decade of closed loop gain Figure 8.

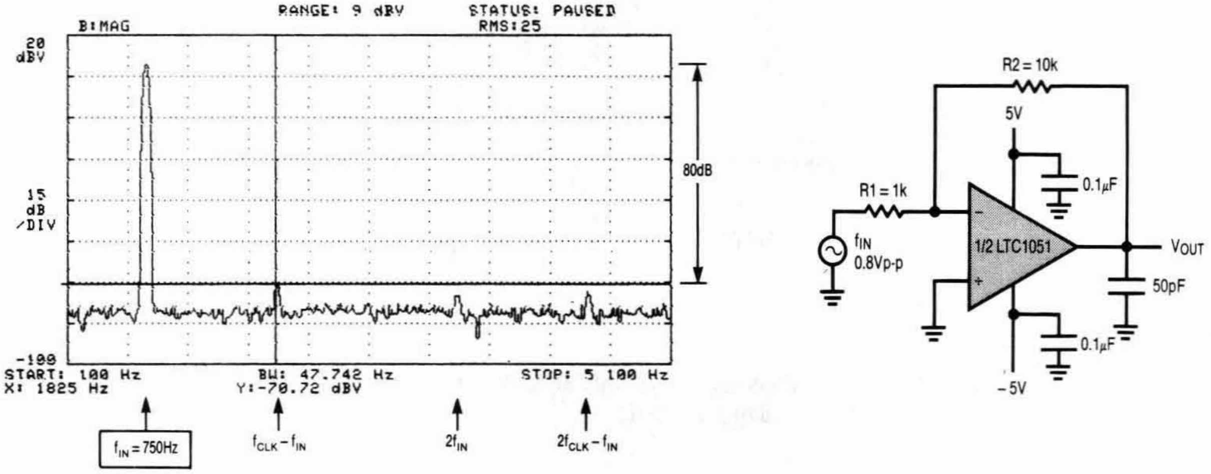


Figure 5A. Output Voltage Spectrum of 1/2 LTC1051 Operating as an Inverting Amplifier with Gain of 10, and Amplifying a 750Hz, 800mV Input AC Signal.

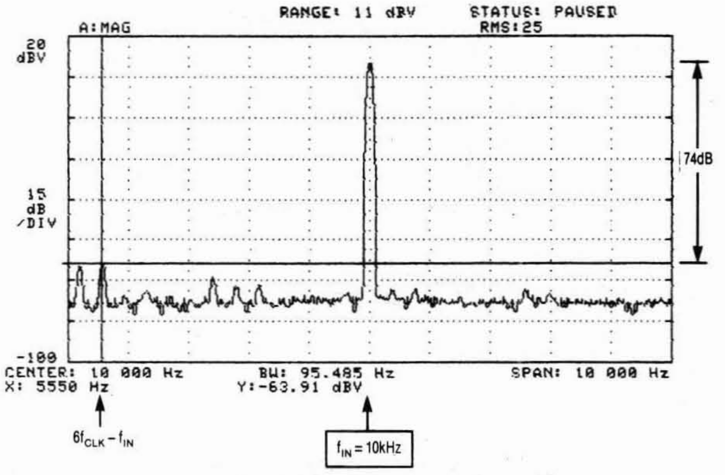


Figure 5B. Same as Figure 5A, but the AC Input Signal is 900mV, 10kHz

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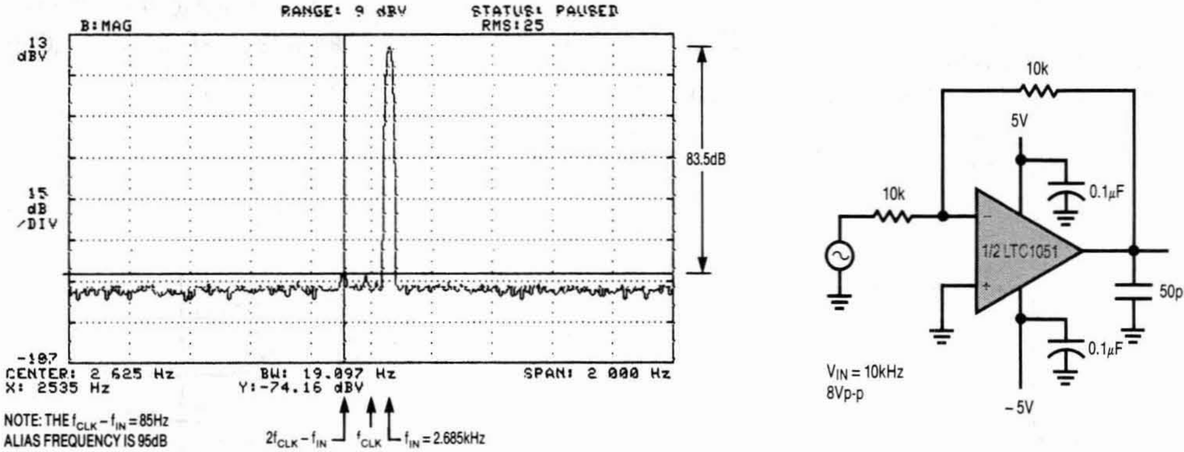
6. For closed loop gains of − 10 or higher, the "signal to alias" ratio degrades when the value of the feedback gain setting resistor increases beyond 50kΩ. For instance, the 68dB value of Figure 7, decreases to 56dB if a (1kΩ, 100kΩ) resistor set will be used to set the gain of − 100.

7. When the LTC1051/LTC1053 are used as non-inverting amplifiers all the previous approximate rules of thumb apply with the following exceptions: When the closed loop gain is + 10(V/V) and below, the "signal to alias" ratio is 1dB to 3dB less than the inverting case. When the closed loop gain is 100(V/V) the degradation can be up to 9dB, especially when the input signal is much higher than the clock frequency (i.e. f_{IN} = 10kHz).

8. The signal/alias ratio performance improves when the op amp has bandlimited loop gain.



NOTE: THE $f_{CLK} - f_{IN}$ = 85Hz ALIAS FREQUENCY IS 95dB DOWN FROM THE OUTPUT LEVEL

Figure 6A. Output Voltage Spectrum of 1/2 LTC1051 Operating as a Unity Gain Inverting Amplifier. $V_S = \pm 5V$, R_L = 10k, C_L = 50pF, V_{IN} = 8Vp-p, 2.685kHz.

ALL ALIAS FREQUENCY 80dB TO 84dB DOWN FROM OUTPUT

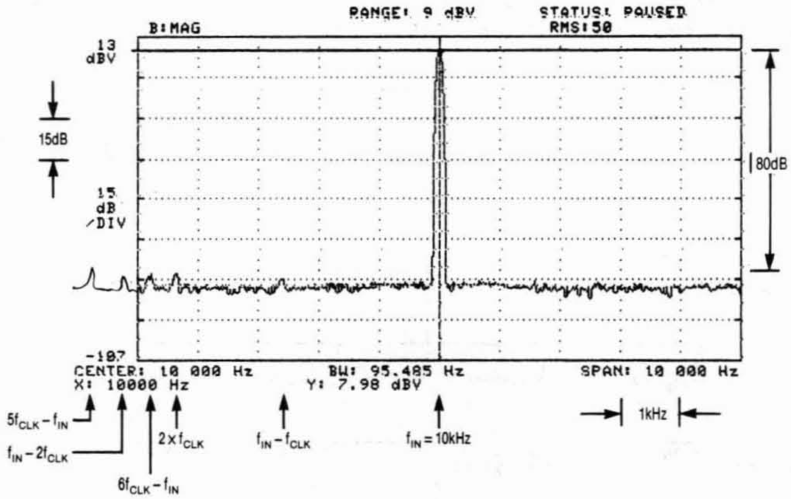


Figure 6B. Output Voltage Spectrum of 1/2 LTC1051, Operating as a Unity Gain Inverting Amplifier. $V_S = \pm 5V$, R_L = 10k, C_L = 50pF, V_{IN} = 8Vp-p, 10kHz.

APPLICATIONS INFORMATION

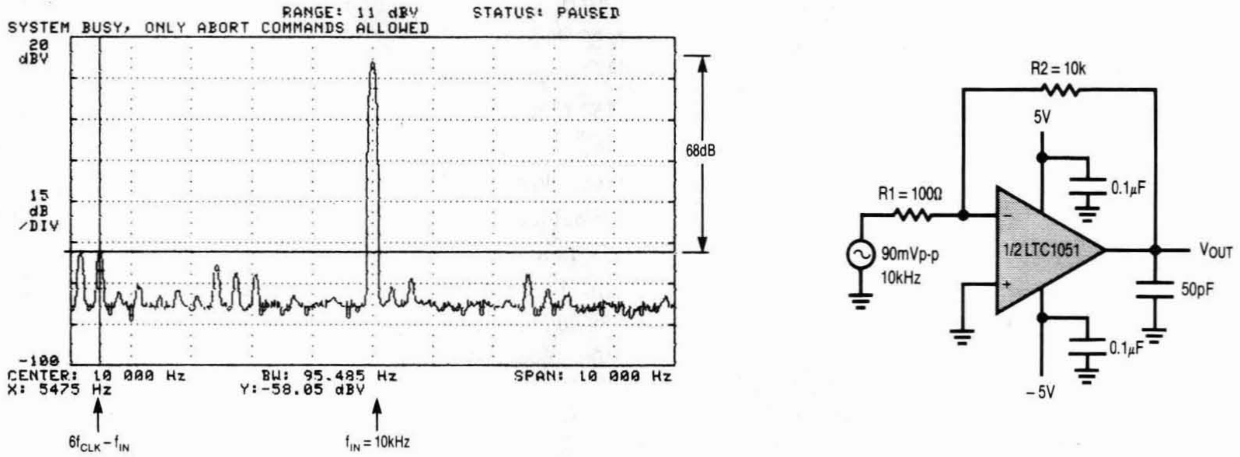


Figure 7. Output Voltage Spectrum of 1/2 LTC1051 Operating as an Inverting Amplifier with a Gain of – 100 and Amplifying a 90mVp-p, 10kHz Input Signal. With a 9Vp-p Output Swing the Measured 2nd Harmonic (20kHz) was 75 Down from the 10kHz Input Signal.

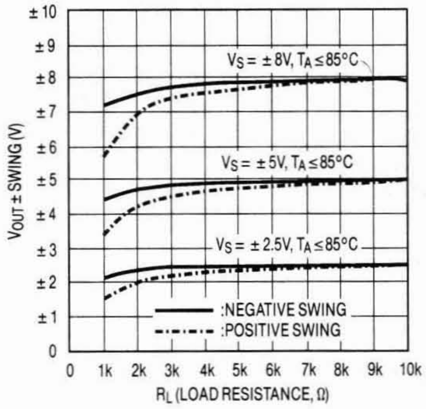


Figure 8. Output Voltage Swing vs Load

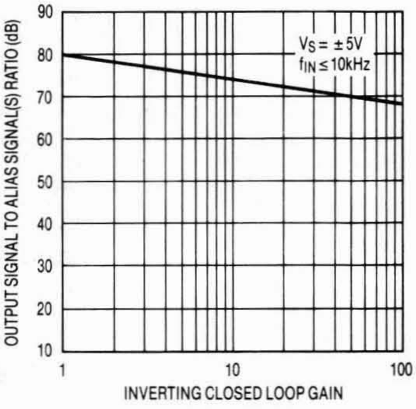
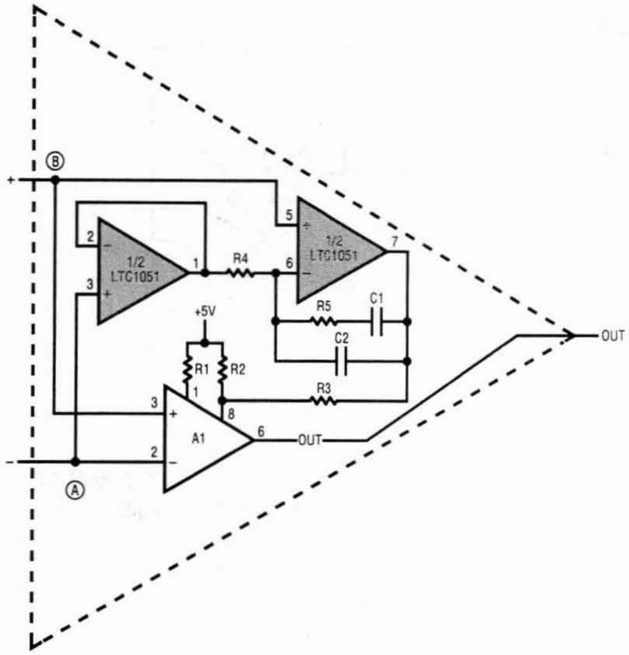


Figure 9. Signal to Alias Ratio vs Closed Loop Gain

APPLICATION CIRCUITS

Obtaining Ultra-Low V_{OS} Drift and Low Noise



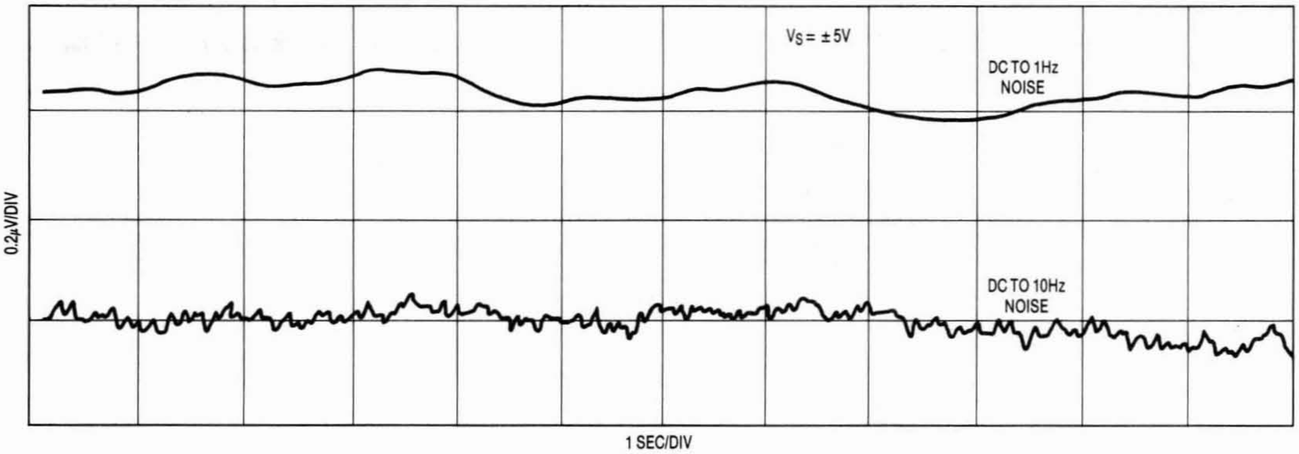
The dual chopper op amp buffers the inputs of A, and corrects its offset voltage and offset voltage drift. With the shown R,C values, the power up warm up time is typically 20s. The step response of the composite amplifier does not present settling tails. The LT1007 should be used when extremely low noise, V_{OS} and V_{OS} drift are sought when the input source resistance is low. (For instance a 350Ω strain gauge bridge.) The LT1012 or equivalent should be used when low bias current (100pA) is also required in conjunction with DC to 10Hz low noise, and low V_{OS} and V_{OS} drift. The measured typical input offset voltages were less than 2μV.

A1	R1	R2	R3	R4	R5	C1	C2	$\bar{e}_{OUT}$ (DC – 1Hz)**	$\bar{e}_{OUT}$ (DC – 10Hz)**
LT1007	3k	2k	340k	10k	100k	0.01μF	0.001μF	0.1μVp-p	0.15μVp-p
LT1012*	750Ω	57Ω	250k	10k	100k	0.01μF	0.001μF	0.3μVp-p	0.4μVp-p

*Interchange connections Ⓐ and Ⓑ.

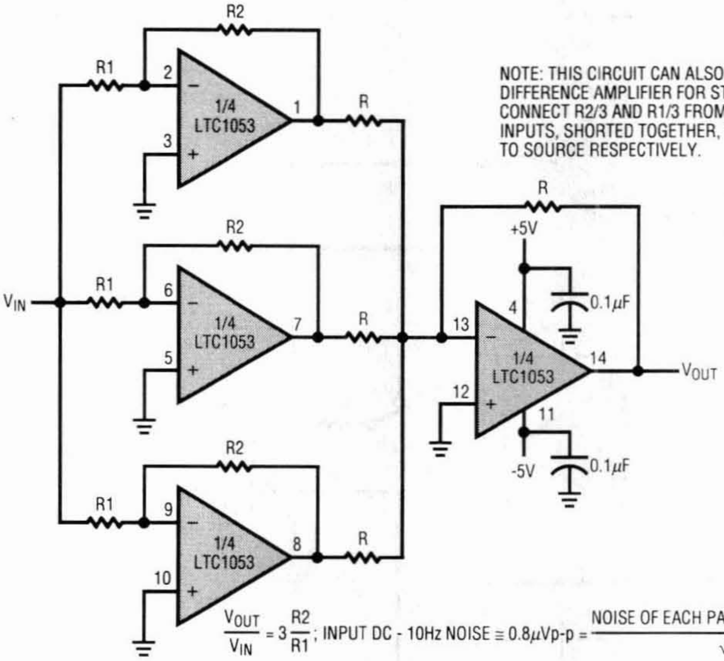
**Noise measured in a 10 sec. window. Peak-to-peak noise was also measured for 10 continuous minutes: With the LT1007 op amp the recorded noise was 0.2μVp-p for both DC-1Hz and DC-10Hz.

LTC1051/LT1007 Peak-to-Peak Noise



APPLICATION CIRCUITS

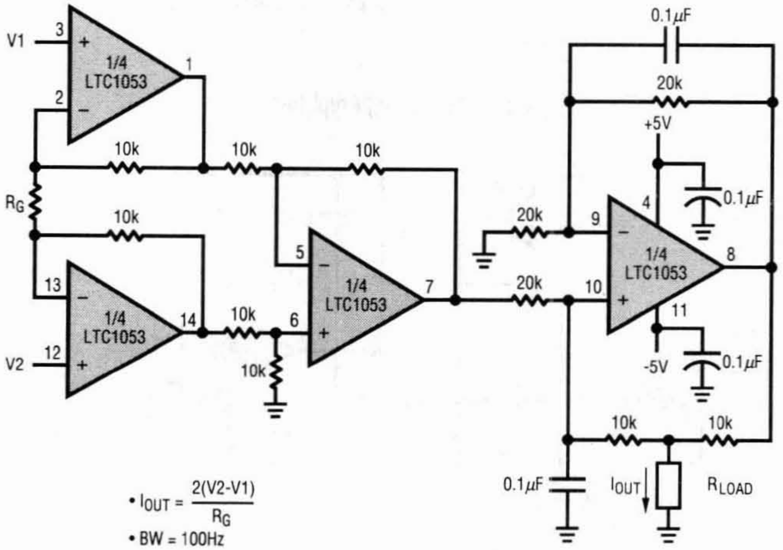
Paralleling Choppers to Improve Noise


R2
R1
2
3
1/4
LTC1053
1
R
R2
R1
6
5
1/4
LTC1053
7
R
R2
R1
9
10
1/4
LTC1053
8
R
V_{IN}
R
+5V
4
0.1µF
13
12
1/4
LTC1053
14
V_{OUT}
11
-5V
0.1µF

NOTE: THIS CIRCUIT CAN ALSO BE USED AS A DIFFERENCE AMPLIFIER FOR STRAIN GAUGES. CONNECT R2/3 AND R1/3 FROM NON-INVERTING INPUTS, SHORTED TOGETHER, TO GROUND AND TO SOURCE RESPECTIVELY.

$\frac{V_{OUT}}{V_{IN}} = 3\frac{R2}{R1}$; INPUT DC - 10Hz NOISE $\cong 0.8\mu Vp\text{-}p = \frac{\text{NOISE OF EACH PARALLELED OP AMP}}{\sqrt{3}}$

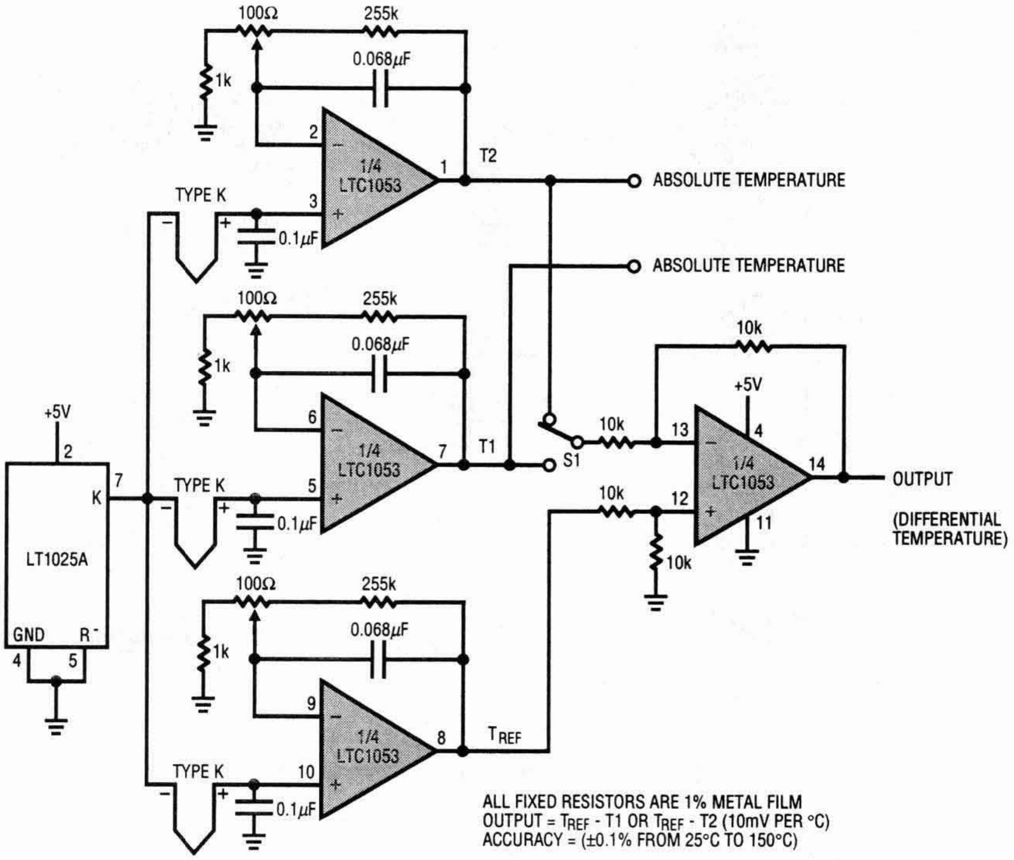
Differential Voltage to Current Converter


V1
3
2
1/4
LTC1053
1
10k
10k
10k
R_G
10k
13
12
V2
1/4
LTC1053
14
10k
6
10k
5
1/4
LTC1053
7
0.1µF
20k
+5V
4
0.1µF
20k
9
20k
10
1/4
LTC1053
8
11
-5V
0.1µF
10k
10k
0.1µF
I_{OUT}
R_{LOAD}

- $I_{OUT} = \frac{2(V2-V1)}{R_G}$
- BW = 100Hz
- I_{OUT} MAX. = 1mA

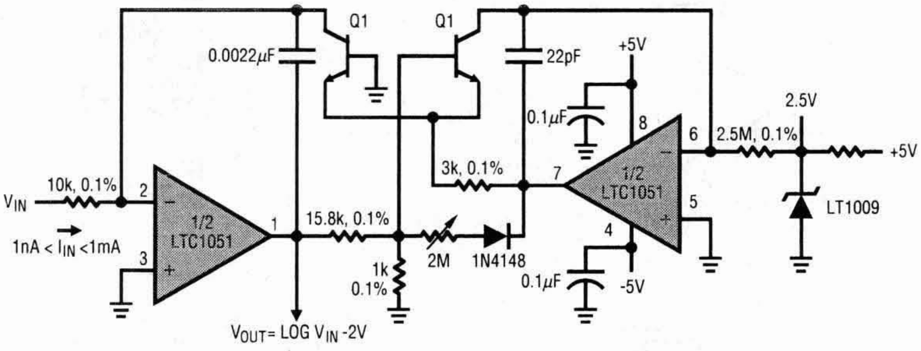
APPLICATION CIRCUITS

Multiplexed Differential Thermometer


100Ω
255k
0.068μF
1k
2
3
1
1/4 LTC1053
T2
TYPE K
0.1μF
ABSOLUTE TEMPERATURE
ABSOLUTE TEMPERATURE
10k
+5V
6
5
7
T1
S1
13
4
14
12
11
OUTPUT
(DIFFERENTIAL TEMPERATURE)
LT1025A
K
GND
R⁻
4
5
9
10
8
T_REF

ALL FIXED RESISTORS ARE 1% METAL FILM
OUTPUT = T_{REF} - T1 OR T_{REF} - T2 (10mV PER °C)
ACCURACY = (±0.1% FROM 25°C TO 150°C)

Six Decade Log Amplifier

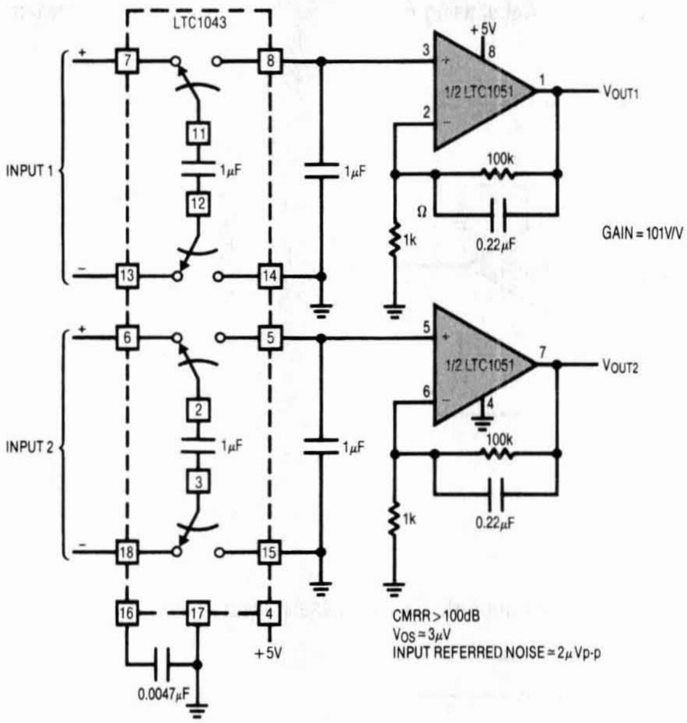

Q1
Q1
0.0022μF
22pF
+5V
2.5V
0.1μF
8
6
2.5M, 0.1%
+5V
3k, 0.1%
7
1/2 LTC1051
5
LT1009
V_IN
10k, 0.1%
2
1nA < I_IN <1mA
3
1
15.8k, 0.1%
1k 0.1%
2M
1N4148
4
0.1μF
-5V

V_{OUT}= LOG V_{IN} -2V

Q1: TEL LAB TYPE Q81
ADJUST 2M POR. FOR NON-LINEARITIES

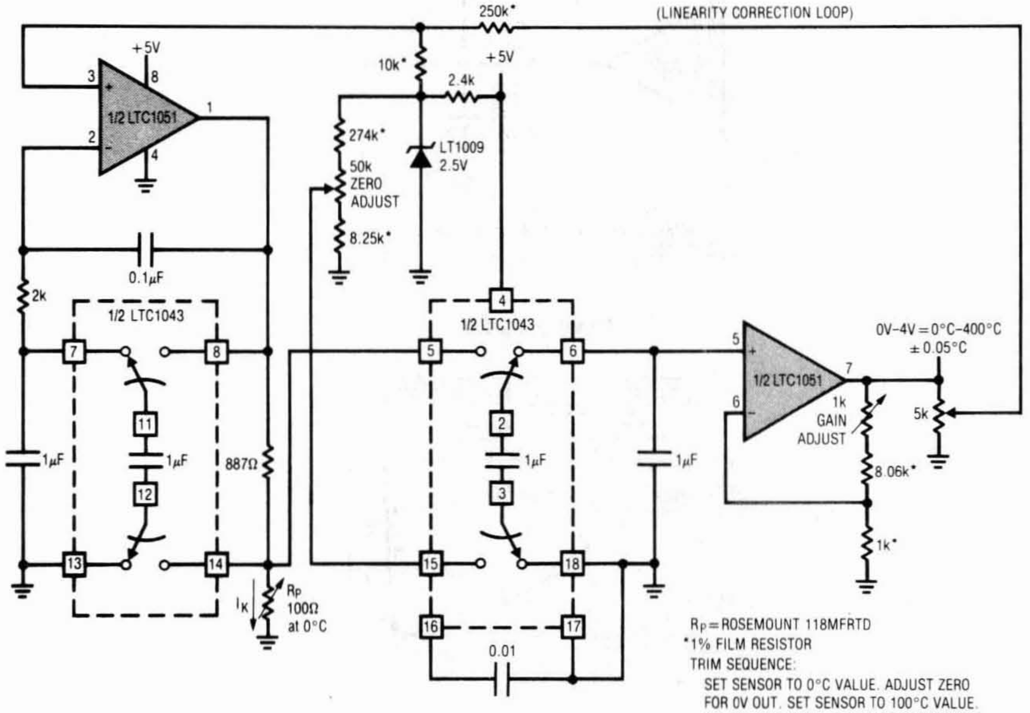
APPLICATION CIRCUITS

Dual Instrumentation Amplifier


LTC1043
INPUT 1
INPUT 2
+
−
7
8
11
12
13
14
6
5
2
3
18
15
16
17
4
1µF
0.0047µF
+5V
3
2
8
1
1/2 LTC1051
VOUT1
100k
1k
0.22µF
GAIN = 101V/V
5
6
7
4
1/2 LTC1051
VOUT2
100k
1k
0.22µF

CMRR > 100dB
$V_{OS} = 3\mu V$
INPUT REFERRED NOISE ≈ 2µVp-p

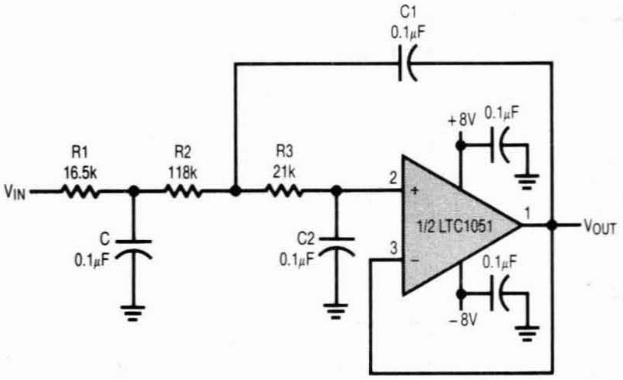
Linearized Platinum Signal Conditioner


250k*
(LINEARITY CORRECTION LOOP)
+5V
3
2
8
4
1
1/2 LTC1051
10k*
2.4k
+5V
274k*
50k
ZERO
ADJUST
8.25k*
LT1009
2.5V
0.1µF
2k
1/2 LTC1043
7
8
11
12
13
14
1µF
887Ω
Rp
100Ω
at 0°C
IK
4
1/2 LTC1043
5
6
2
3
15
18
16
17
0.01
1µF
5
6
7
1/2 LTC1051
0V–4V = 0°C–400°C
± 0.05°C
1k
GAIN
ADJUST
5k
8.06k*
1k*

R_P = ROSEMOUNT 118MFRTD
*1% FILM RESISTOR
TRIM SEQUENCE:
SET SENSOR TO 0°C VALUE. ADJUST ZERO FOR 0V OUT. SET SENSOR TO 100°C VALUE. ADJUST GAIN FOR 1,000V OUT. SET SENSOR TO 400°C VALUE. ADJUST LINEARITY FOR 4.000V OUT. REPEAT AS REQUIRED. FOR MORE INFORMATION REFER TO AN3.

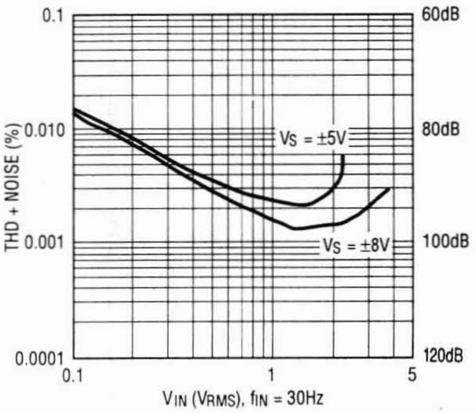
APPLICATION CIRCUITS

DC Accurate, 3rd Order, 100Hz, Butterworth Antialiasing Filter

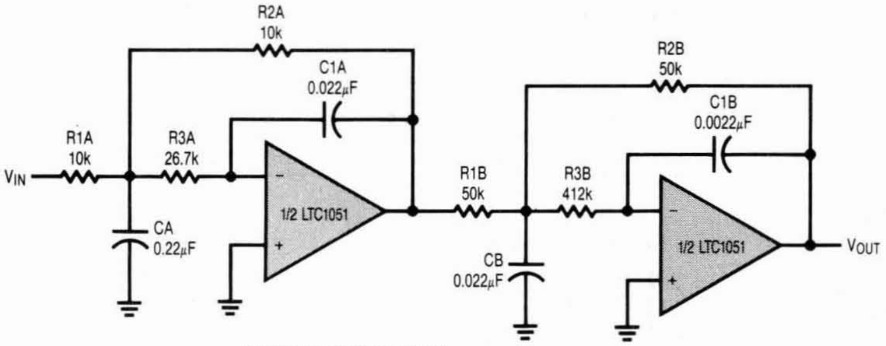

C1
0.1μF
+8V
0.1μF
R1
16.5k
R2
118k
R3
21k
VIN
2
+
1
VOUT
1/2 LTC1051
C
0.1μF
C2
0.1μF
3
−
0.1μF
−8V

WIDEBAND NOISE $9\mu V_{RMS}$
THD + NOISE ≈ 0.0012%, $1V_{RMS} < V_{IN} < 2V_{RMS}$, $V_S = \pm 8V$
V_{OS} (OUT) < $5\mu V$

Dynamic Range

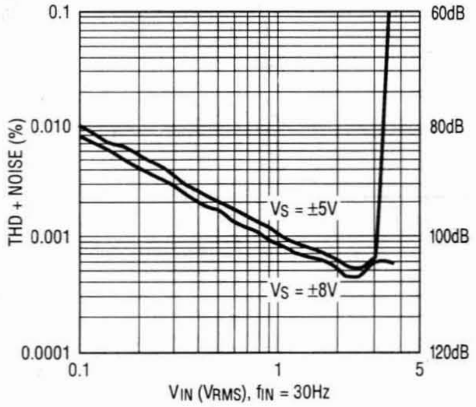


DC Accurate, 18-Bit 4th Order Antialiasing Bessel (Linear Phase), 100Hz, Lowpass Filter


R2A
10k
C1A
0.022μF
R1A
10k
R3A
26.7k
VIN
CA
0.22μF
−
+
1/2 LTC1051
R1B
50k
CB
0.022μF
R2B
50k
C1B
0.0022μF
R3B
412k
−
+
1/2 LTC1051
VOUT

WIDEBAND RMS NOISE $4.5\mu V_{RMS}$
THD + NOISE ≈ 0.0005% (= 106dB DYN. RANGE), $2V_{RMS} \leq V_{IN} \leq 3V_{RMS}$
V_{OS} OUT < $10\mu V$

Dynamic Range



LINEAR TECHNOLOGY

LTC1150

±15V Chopper Stabilized Operational Amplifier with Internal Capacitors

FEATURES

- High Voltage Operation, ±18V
- No External Components Required
- Maximum Offset Voltage 5μV
- Maximum Offset Voltage Drift 0.05μV/°C
- Low Noise 1.8μVp-p (0.1Hz to 10Hz)
- Minimum Voltage Gain 140dB
- Minimum PSRR 120dB
- Minimum CMRR 120dB
- Low Supply Current 0.8mA
- Single Supply Operation 4.75V to 36V
- Input Common Mode Range Includes Ground
- 200μA Supply Current with Pin 1 Grounded
- Typical Overload Recovery Time 20ms

APPLICATIONS

- Strain Gauge Amplifiers
- Electronic Scales
- Medical Instrumentation
- Thermocouple Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

The LTC1150 is a high-voltage, high-performance chopper stabilized operational amplifier. The two sample-and-hold capacitors usually required externally by other chopper amplifiers are integrated on-chip. Further, LTC's proprietary high-voltage CMOS structures allow the LTC1150 to operate at up to 36V total supply voltage.

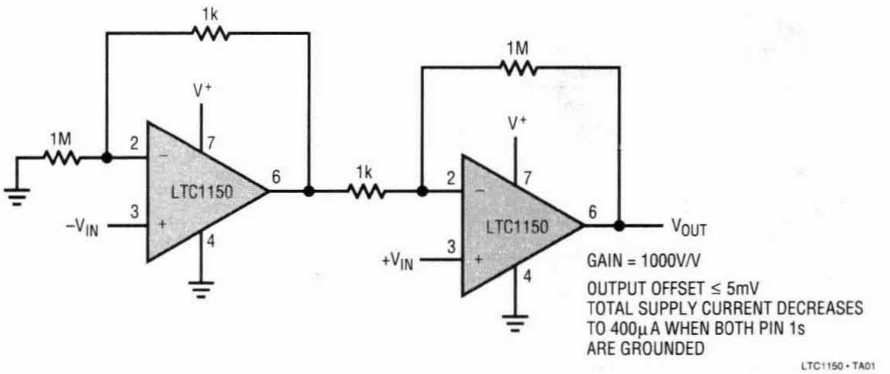
The LTC1150 has an offset voltage of 0.5μV, drift of 0.01μV/°C, 0.1Hz to 10Hz input noise voltage of 1.8μVp-p and a typical voltage gain of 180dB. The slew rate of 3V/μs and a gain bandwidth product of 2.5MHz are achieved with 0.8mA of supply current. Overload recovery times from positive and negative saturation conditions are 3ms and 20ms, respectively.

For applications demanding low power consumption, pin 1 can be used to program the supply current. Pin 5 is an optional AC-coupled clock input, useful for synchronization.

The LTC1150 is available in a standard 8-lead metal can, plastic and ceramic dual in line packages, as well as an 8-lead SO8 package. The LTC1150 can be a plug-in replacement for most standard bipolar op amps with significant improvement in DC performance.

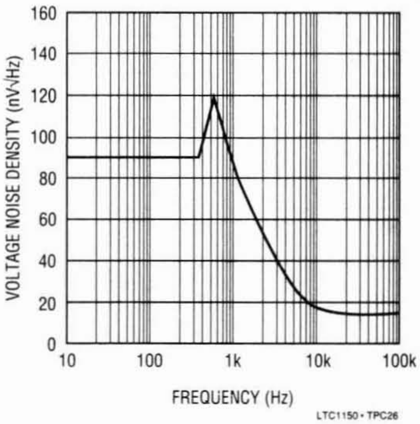
TYPICAL APPLICATION

Single Supply Instrumentation Amplifier



GAIN = 1000V/V
OUTPUT OFFSET ≤ 5mV
TOTAL SUPPLY CURRENT DECREASES TO 400μA WHEN BOTH PIN 1s ARE GROUNDED

Noise Spectrum

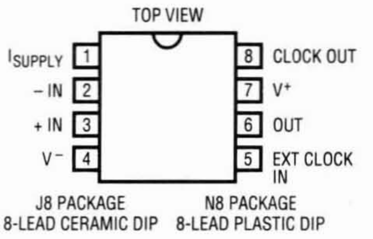


ABSOLUTE MAXIMUM RATINGS

(Note 1)

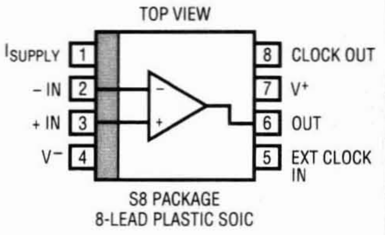
Total Supply Voltage (V^+ to V^-) 36V
Input Voltage (Note 2) .... (V^+ + 0.3V) to (V^- − 0.3V)
Output Short Circuit Duration .... Indefinite
Burn-In Voltage 36V
Operating Temperature Range
LTC1150M .... −55°C to 125°C
LTC1150C .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP



S8 PACKAGE
8-LEAD PLASTIC SOIC

ORDER PART NUMBER
LTC1150MJ8 LTC1150CJ8 LTC1150CN8
LTC1150CS8
S8 PART MARKING
1150

ELECTRICAL CHARACTERISTICS

V_S = ±15V, Pin 1 = Open, T_A = Operating Temperature Range, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1150M MIN	LTC1150M TYP	LTC1150M MAX	LTC1150C MIN	LTC1150C TYP	LTC1150C MAX	UNITS
Input Offset Voltage	T_A = 25°C (Note 3)			± 0.5	± 5		± 0.5	± 5	μV
Average Input Offset Drift	(Note 3)	●		± 0.01	± 0.05		± 0.01	± 0.05	μV/°C
Long Term Offset Voltage Drift				50			50		nV/√mo
Input Offset Current	T_A = 25°C			± 20	± 60		± 20	± 200	pA
		●			± 1.5			± 0.5	nA
Input Bias Current	T_A = 25°C			± 10	± 50		± 10	± 100	pA
		●			± 2.5			± 0.5	nA
Input Noise Voltage	R_S = 100Ω, 0.1Hz to 10Hz, TC2			1.8			1.8		μVp-p
	R_S = 100Ω, 0.1Hz to 1Hz, TC2			0.6			0.6		
Input Noise Current	f = 10Hz (Note 4)			1.8			1.8		fA/√Hz
Common-Mode Rejection Ratio	V_{CM} = V^- to 12V	●	110	130		110	130		dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±16V	●	120	145		120	145		dB
Large Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = ±10V	●	140	180		140	180		dB
Maximum Output Voltage Swing	R_L = 10kΩ T_A = 25°C		± 13.5	± 14.5		± 13.5	± 14.5		V
	R_L = 10kΩ	●	+ 10.5/ − 13.5			+ 10.5/ − 13.5			
	R_L = 100kΩ			± 14.95			± 14.95		
Slew Rate	R_L = 10kΩ, C_L = 50pF			3			3		V/μs
Gain Bandwidth Product				2.5			2.5		MHz
Supply Current	No Load T_A = 25°C			0.8	1.0		0.8	1.5	mA
	No Load, Pin 1 = V^- T_A = 25°C			0.2			0.2		
	No Load	●			1.5			2	
Internal Sampling Frequency				550			550		Hz

ELECTRICAL CHARACTERISTICS

V_S = 5V, Pin 1 = Open, T_A = Operating Temperature Range, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1150M MIN	LTC1150M TYP	LTC1150M MAX	LTC1150C MIN	LTC1150C TYP	LTC1150C MAX	UNITS
Input Offset Voltage	T_A = 25°C (Note 3)			±0.5	±5		±0.05	±5	μV
Average Input Offset Drift	(Note 3)	●		±0.01	±0.05		±0.01	±0.05	μV/°C
Long Term Offset Voltage Drift				50			50		nV/√mo
Input Offset Current	T_A = 25°C			±10	±30		±10	±60	pA
		●			±100			±100	
Input Bias Current	T_A = 25°C			±5	±15		±5	±30	pA
		●			±400			±100	
Input Noise Voltage	R_S = 100Ω, 0.1Hz to 10Hz, TC2			2.0			2.0		μVp-p
	R_S = 100Ω, 0.1Hz to 1Hz, TC2			0.7			0.7		
Input Noise Current	f = 10Hz (Note 4)			1.3			1.3		fA/√Hz
Common-Mode Rejection Ratio	V_{CM} = 0V to 2.7V	●	110			110			dB
Power Supply Rejection Ratio	V_S = ±2.375V to ±16V	●	130	145		125	145		dB
Large Signal Voltage Gain	R_L = 10kΩ, V_{OUT} = 0.3V to 4.5V	●	130	180		130	180		dB
Maximum Output Voltage Swing	R_L = 10kΩ			0.15 – 4.85			0.15 – 4.85		V
	R_L = 100kΩ			0.02 – 4.97			0.02 – 4.97		
Slew Rate	R_L = 10kΩ, C_L = 50pF			1.5			1.5		V/μs
Gain Bandwidth Product				1.8			1.8		MHz
Supply Current	No Load T_A = 25°C			0.4	1		0.4	1	mA
		●			1.5			1.5	
Internal Sampling Frequency				300			300		Hz

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1150.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high-speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

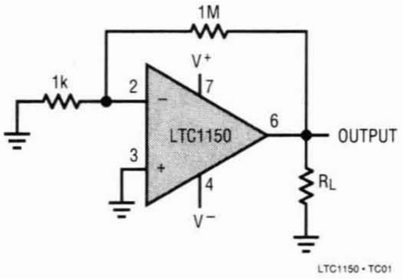
Note 4: Current Noise is calculated from the formula:

$I_N = \sqrt{(2q \bullet I_b)}$

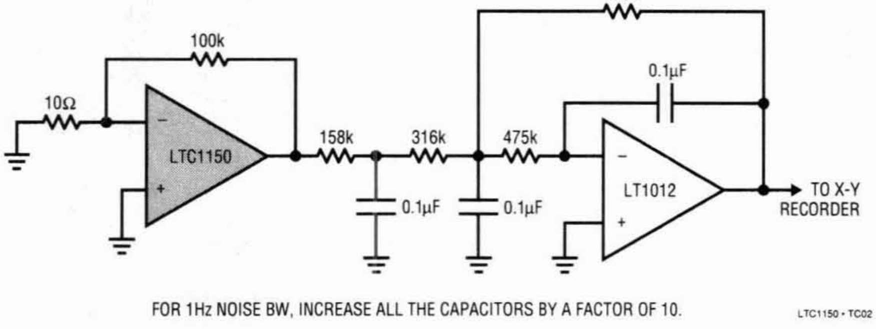
where $q = 1.6 \times 10^{-19}$ Coulomb.

TEST CIRCUITS

Offset Voltage Test Circuit



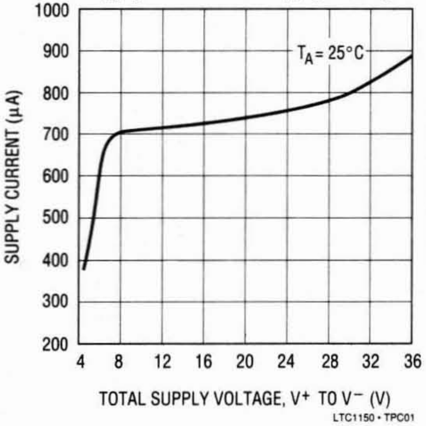
DC-10Hz Noise Test Circuit



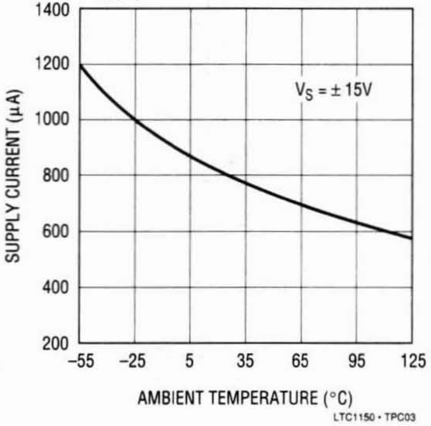
FOR 1Hz NOISE BW, INCREASE ALL THE CAPACITORS BY A FACTOR OF 10.

TYPICAL PERFORMANCE CHARACTERISTICS

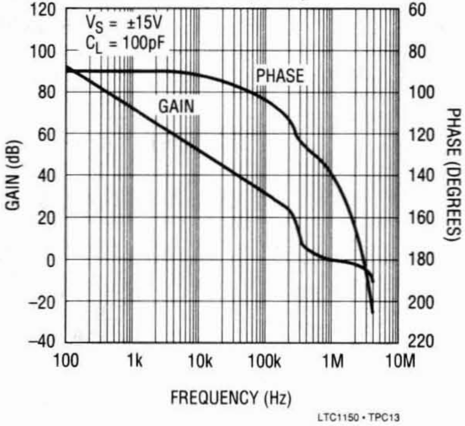
Supply Current vs Supply Voltage



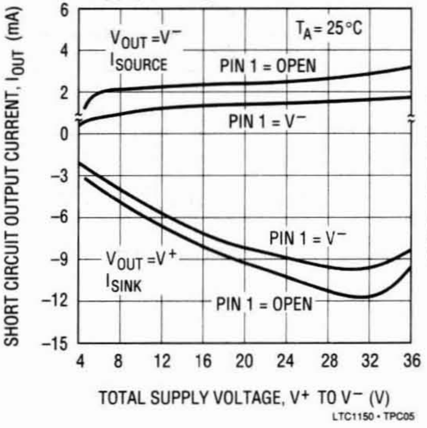
Supply Current vs Temperature



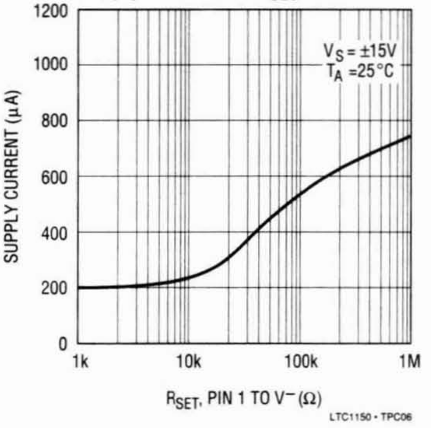
Gain/Phase vs Frequency



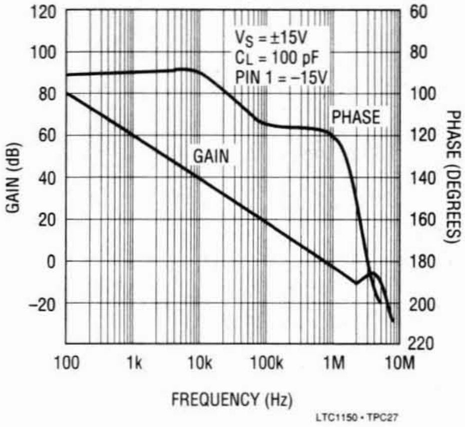
Output Short Circuit Current vs Supply Voltage



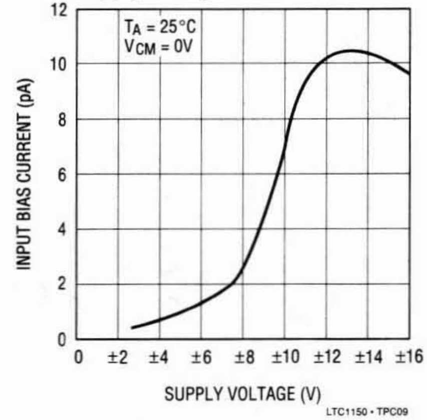
Supply Current vs R_{SET}



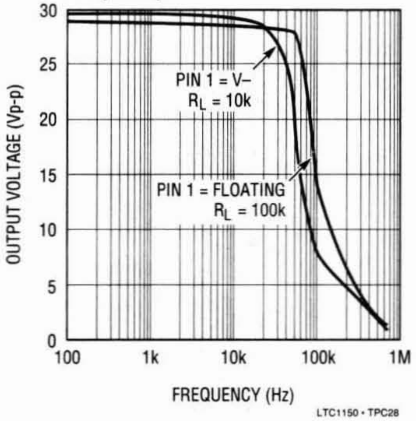
Gain/Phase vs Frequency



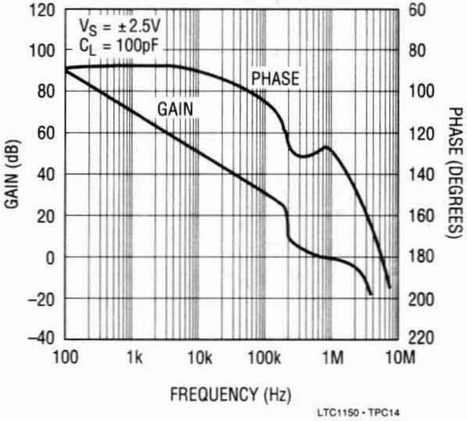
Input Bias Current vs Supply Voltage



Undistorted Output Swing vs Frequency

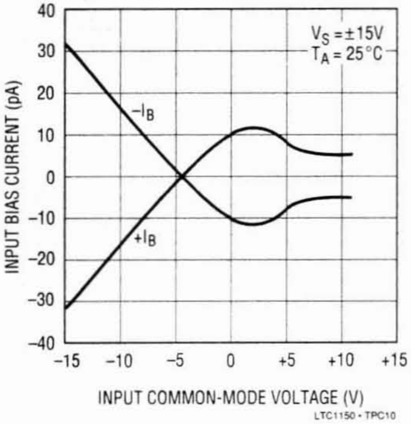


Gain/Phase vs Frequency

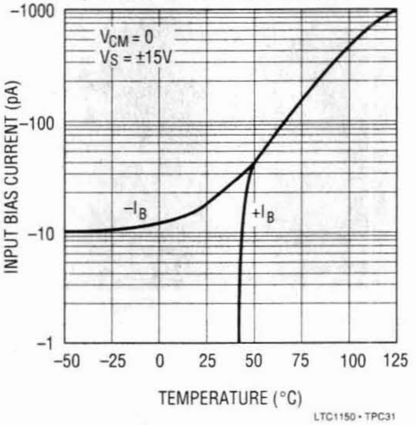


TYPICAL PERFORMANCE CHARACTERISTICS

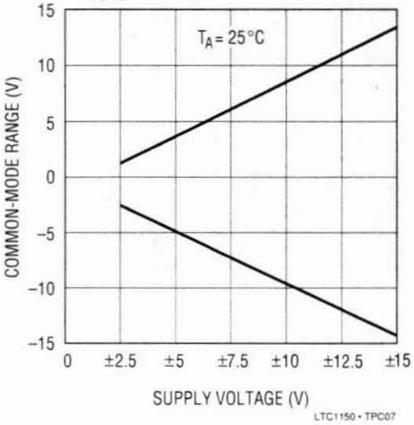
Input Bias Current vs Input Common-Mode Voltage



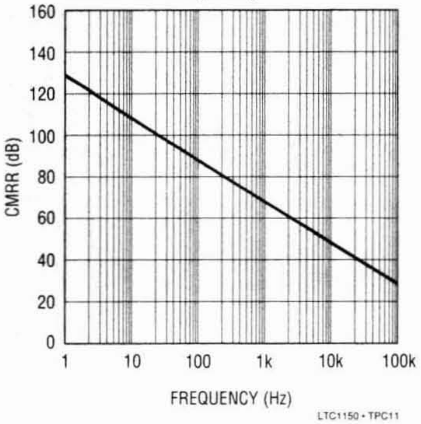
Input Bias Current vs Temperature



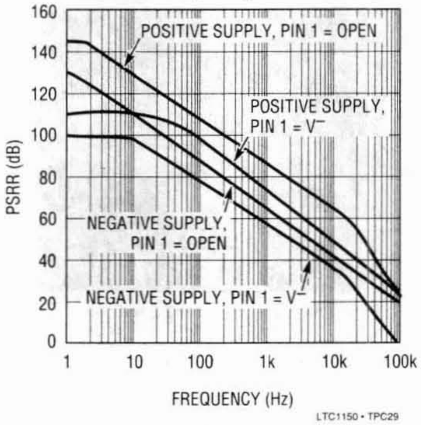
Common-Mode Input Range vs Supply Voltage



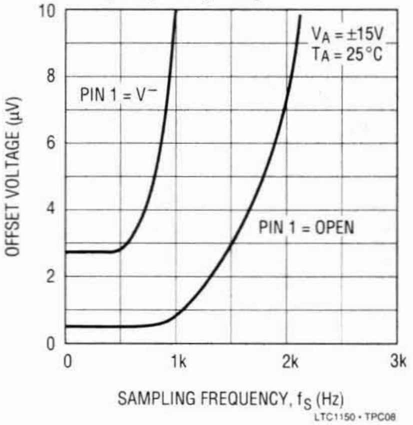
CMRR vs Frequency



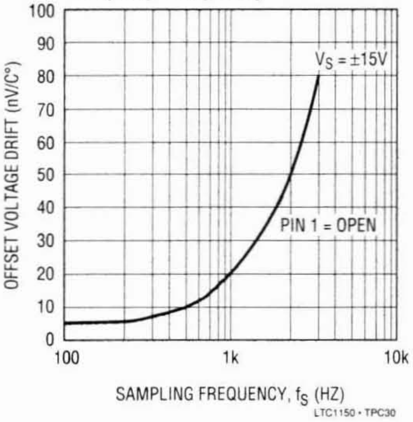
PSRR vs Frequency



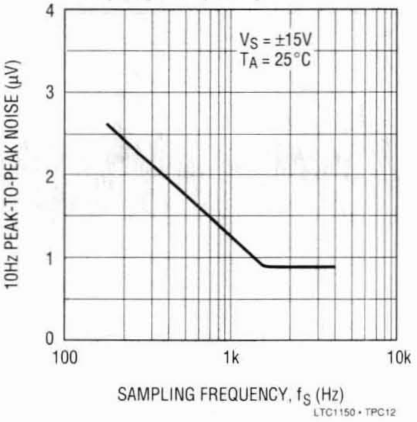
Offset Voltage vs Sampling Frequency



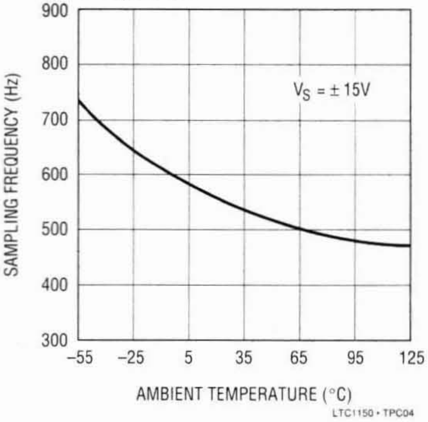
Offset Voltage Drift vs Sampling Frequency



10Hz p-p Noise vs Sampling Frequency

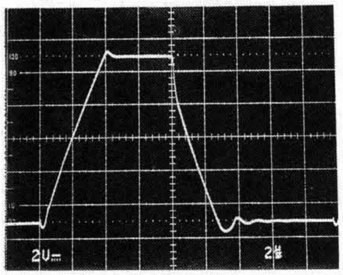


Sampling Frequency vs Temperature



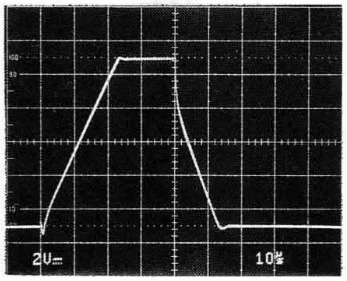
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Transient Response



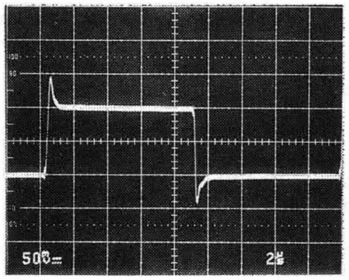
$V_S = \pm15V$, $A_V = 1$, $C_L = 100pF$, $R_L = 10k\Omega$
LTC1150 • TPC15

Large Signal Transient Response, Pin 1 = V^-



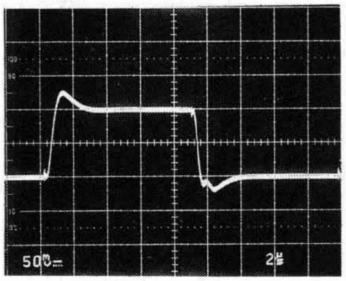
$V_S = \pm15V$, $A_V = 1$, $C_L = 100pF$, PIN 1 = V^-
LTC1150 • TPC16

Small Signal Transient Response



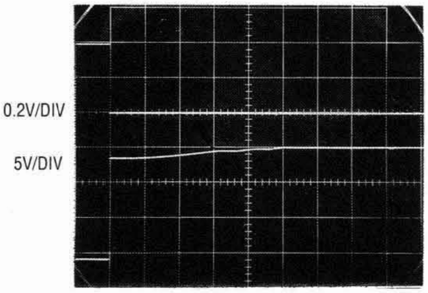
$V_S = \pm15V$, $A_V = 1$, $C_L = 100pF$, $R_L = 10k\Omega$
LTC1150 • TPC17

Small Signal Transient Response, Pin 1 = V^-



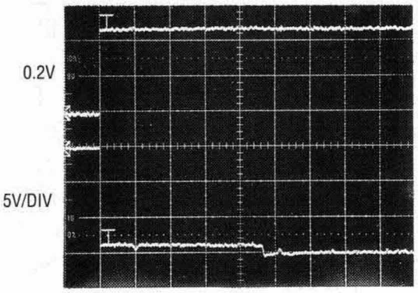
$V_S = \pm15V$, $A_V = 1$, $C_L = 100pF$, $R_L = 10k\Omega$,
PIN 1 = V^-
LTC1150 • TPC18

Overload Recovery from Negative Saturation



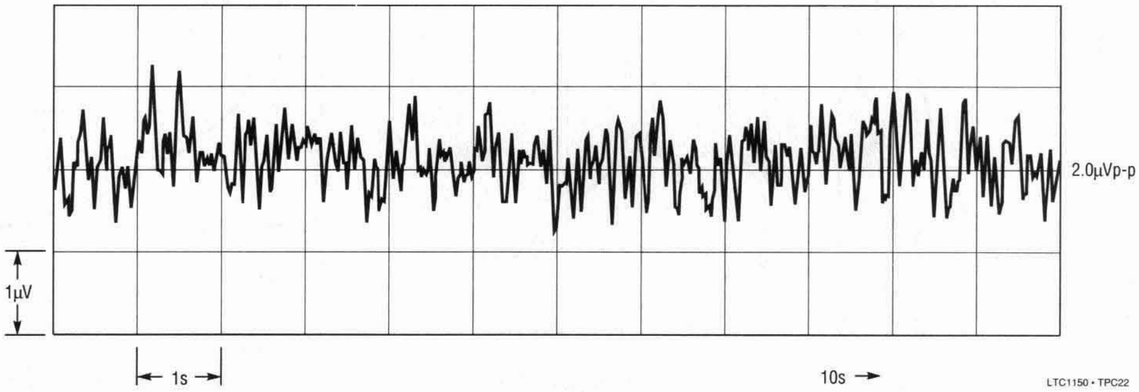
$V_S = \pm15V$, $A_V = -100$, 2ms/DIV
LTC1150 • TPC21

Overload Recovery from Positive Saturation



$V_S = \pm15V$, $A_V = -100$, 2ms/DIV
LTC1150 • TPC33

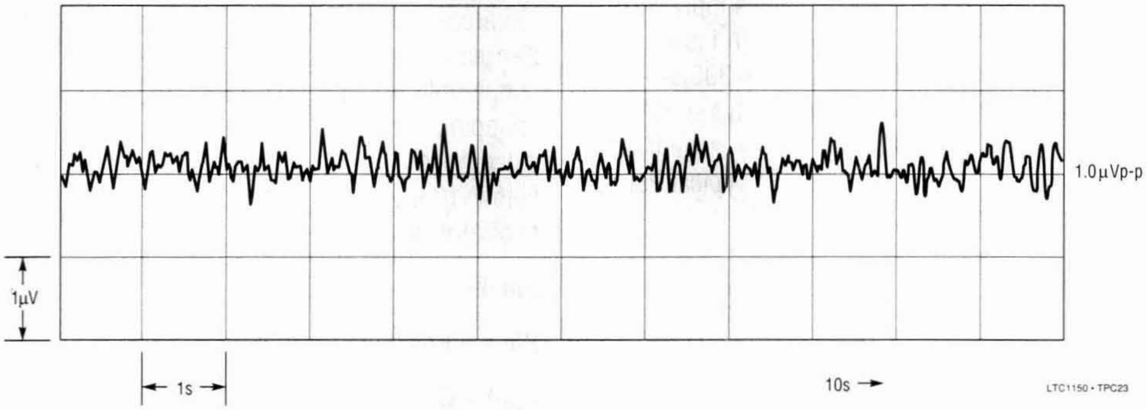
0.1Hz-10Hz Noise, V = ±15V, $T_A = 25°C$, Internal Clock



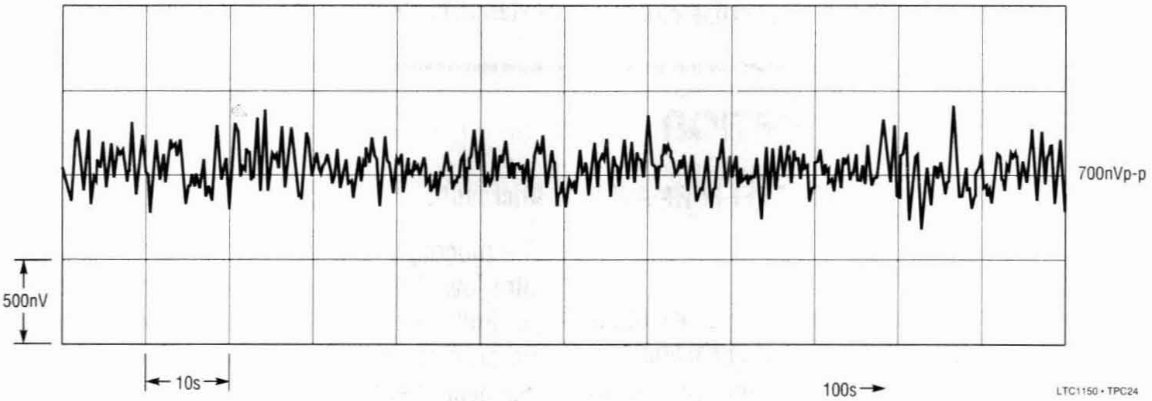
LTC1150 • TPC22

TYPICAL PERFORMANCE CHARACTERISTICS

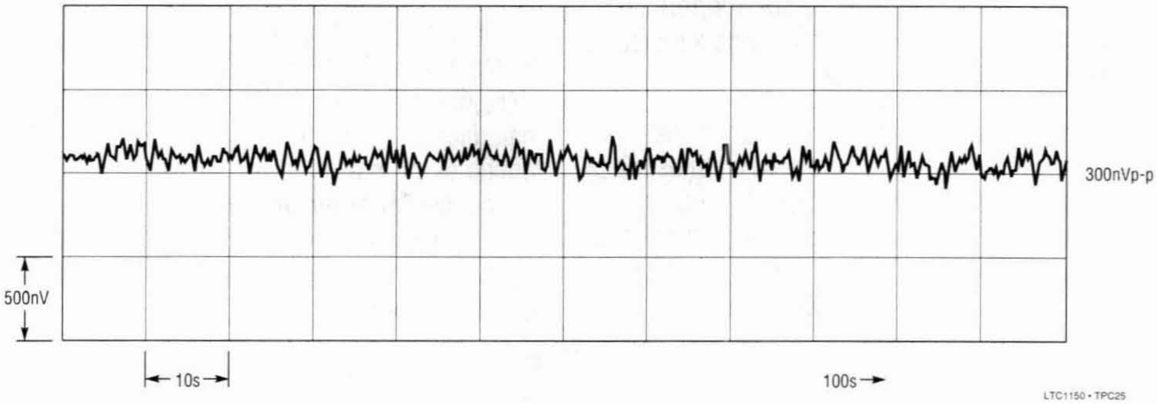
0.1Hz-10Hz Noise, V = ±15V, T_A = 25°C, f_S = 1800Hz



0.1Hz-1Hz Noise, V = ±15V, T_A = 25°C, Internal Clock



0.1Hz-1Hz Noise, V = ±15V, T_A = 25°C, f_S = 1800Hz



PIN DESCRIPTIONS

1) 8-Pin Packages

Pin 1– Supply Current Programming. The supply current can be programmed through pin 1. When pin 1 is left open or tied to $+V_S$, the supply current defaults to 800μA. Tying a resistor between pin 1 and pin 4, the negative supply pin, will reduce the supply current. The supply current, as a function of the resistor value, is shown in Typical Performance Characteristics.

Pin 2 – Inverting Input.

Pin 3 – Non-Inverting Input.

Pin 4 – Negative Supply.

Pin 5 – Optional External Clock Input. The LTC1150 has an internal oscillator to control the circuit operation of the amplifier if pin 5 is left open or biased at any DC voltage in the supply voltage range. When an external clock is desirable it can be applied to pin 5. The applied clock is AC-coupled to the internal circuitry to simplified interface requirements. The amplitude of clock input signal needs to be greater than 2V and the voltage level has to be within the supply voltage range. Duty cycle is not critical. The internal chopping frequency is the external clock frequency divided by four. When frequency of the external clock falls below 100Hz (internal chopping at 25Hz), the internal oscillator takes over and the circuit chops at 550Hz.

Pin 6 – Output.

Pin 7 – Positive Supply.

Pin 8 – Clock Output. The signal coming out of this pin is at the internal oscillator frequency of about 2.2kHz (four times the chopping frequency) and has voltage levels at $V_H = +V_S$ and $V_L = V_S - 4.6V$. If the circuit is driven by an external clock, pin 8 is pulled up to $+V_S$.

APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1150, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary– particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Microvolts

Thermocouple effects must be considered if the LTC1150's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect if a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C — four times the maximum drift specification of the LTC1150. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35μV/°C — 700 times the maximum drift specification of the LTC1150.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and

APPLICATIONS INFORMATION

component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches, and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 1 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

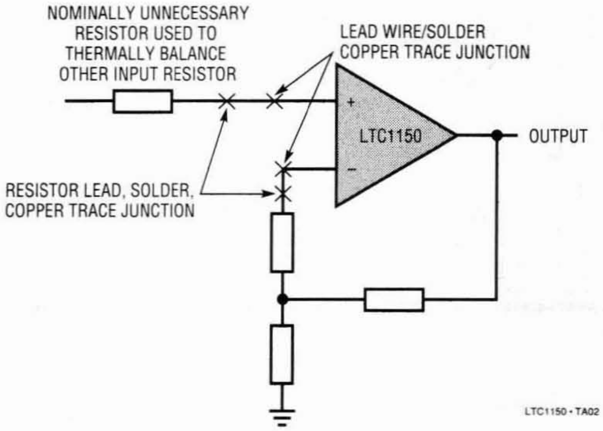

NOMINALLY UNNECESSARY RESISTOR USED TO THERMALLY BALANCE OTHER INPUT RESISTOR
LEAD WIRE/SOLDER COPPER TRACE JUNCTION
+
LTC1150
–
OUTPUT
RESISTOR LEAD, SOLDER, COPPER TRACE JUNCTION
LTC1150 • TA02

Figure 1. Extra Resistors Cancel Thermal EMF

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally-balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

Table 1. Resistor Thermal EMF

Resistor Type	Thermal EMF/°C Gradient
Tin Oxide	~mV/°C
Carbon Composition	~450μV/°C
Metal Film	~20μV/°C
Wire Wound	
Evenohm	~2μV/°C
Manganin	~2μV/°C

PACKAGE-INDUCED OFFSET VOLTAGE

Package-induced thermal EMF effects are another important source of errors. It arises at the copper/kovar junctions formed when wire or printed circuit traces contact a package lead. Like all the previously mentioned thermal EMF effects, it is outside the LTC1150's offset nulling loop and cannot be cancelled. Metal can H packages exhibit the worst warm-up drift. The input offset voltage specification of the LTC1150 is actually set by the package-induced warm-up drift rather than by the circuit itself. The thermal time constant ranges from 0.5 to 3 minutes, depending on package type.

ALIASING

Like all sampled data systems, the LTC1150 exhibits aliasing behavior at input frequencies near the sampling frequency. The LTC1150 includes a high-frequency correction loop which minimizes this effect; as a result, aliasing is not a problem for most applications.

For a complete discussion of the correction circuitry and aliasing behavior, please refer to the LTC1051/53 data sheet.

SYNCHRONIZATION OF MULTIPLE LTC1150's

When synchronization of several LTC1150's is required, one of the LTC1150's can be used to provide the "master" clock to control over 100 "slave" LTC1150's. The master clock, coming from pin 8 of the master LTC1150, can directly drive pin 5 of the slaves. Note that pin 8 of the slave LTC1150's will be pulled up to $+V_S$.

If all the LTC1150's are to be synchronized with an external clock, then the external clock should drive pin 5 of all the LTC1150's.

APPLICATIONS INFORMATION

LEVEL SHIFTING THE CLOCK

Level shifting is needed if the clock output of the LTC1150 in ±15V operation must interface to regular +5V logic circuits. Figures 2 and 3 show some typical level shifting circuits.

When operated from a single +5V or ±5V supplies, the LTC1150 clock output at pin 8 can interface to TTL or CMOS inputs directly.

LOW SUPPLY OPERATION

The minimum supply for proper operation of the LTC1150 is typically below 4.0V (±2.0V). In single supply applications, PSRR is guaranteed down to 4.7V (±2.35V) to ensure proper operation down to the minimum TTL specified voltage of 4.75V.

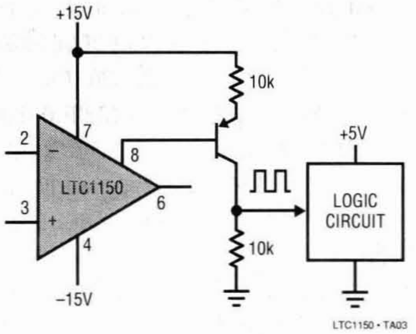

+15V
10k
2
7
8
LTC1150
3
6
4
-15V
10k
+5V
LOGIC CIRCUIT
LTC1150 • TA03

Figure 2. Output Level Shift (Option 1)

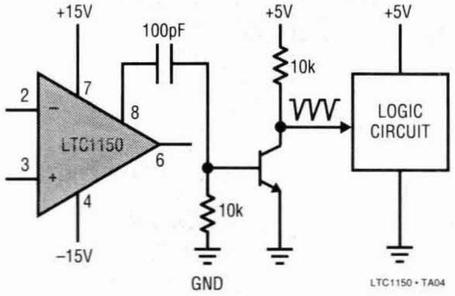
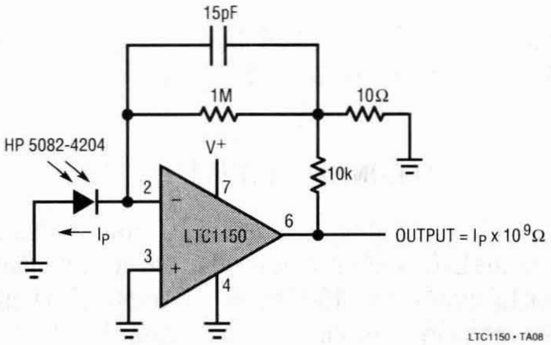

+15V
100pF
+5V
+5V
10k
2
7
8
LTC1150
LOGIC CIRCUIT
3
6
4
10k
-15V
GND
LTC1150 • TA04

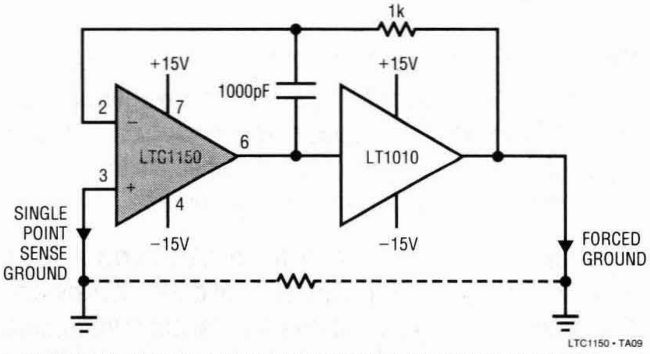
Figure 3. Output Level Shift (Option 2)

TYPICAL APPLICATIONS

Low Level Photodectector


15pF
1M
10Ω
HP 5082-4204
V+
10k
2
7
6
I_P
LTC1150
3
4
OUTPUT = I_P x 10^9Ω
LTC1150 • TA08

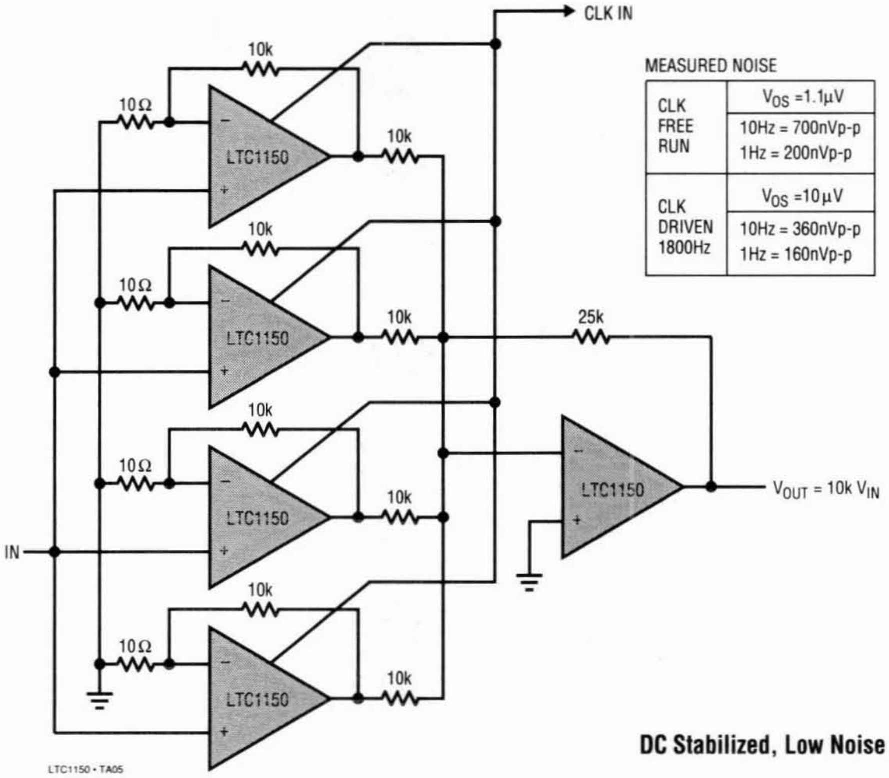
Ground Force Reference


1k
+15V
+15V
1000pF
2
7
6
LTC1150
LT1010
3
4
SINGLE POINT SENSE GROUND
-15V
-15V
FORCED GROUND
LTC1150 • TA09

APPLICATION: TO FORCE TWO GROUND POINTS IN A SYSTEM WITHIN 5μV.

TYPICAL APPLICATIONS

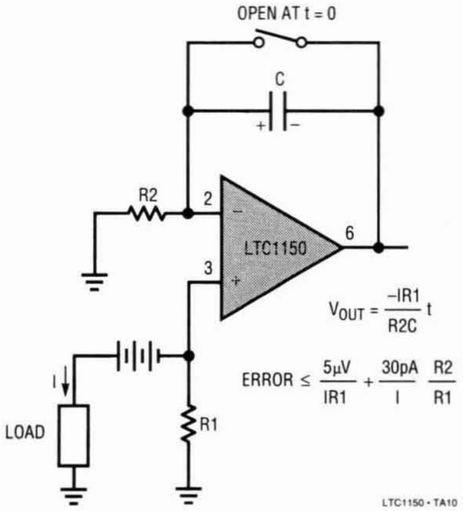
Paralleling to Improve Noise


CLK IN
10k
10Ω
LTC1150
10k
25k
IN
V_{OUT} = 10k V_{IN}
LTC1150 • TA05

MEASURED NOISE

CLK FREE RUN	V_{OS} = 1.1µV
	10Hz = 700nVp-p 1Hz = 200nVp-p
CLK DRIVEN 1800Hz	V_{OS} = 10µV
	10Hz = 360nVp-p 1Hz = 160nVp-p

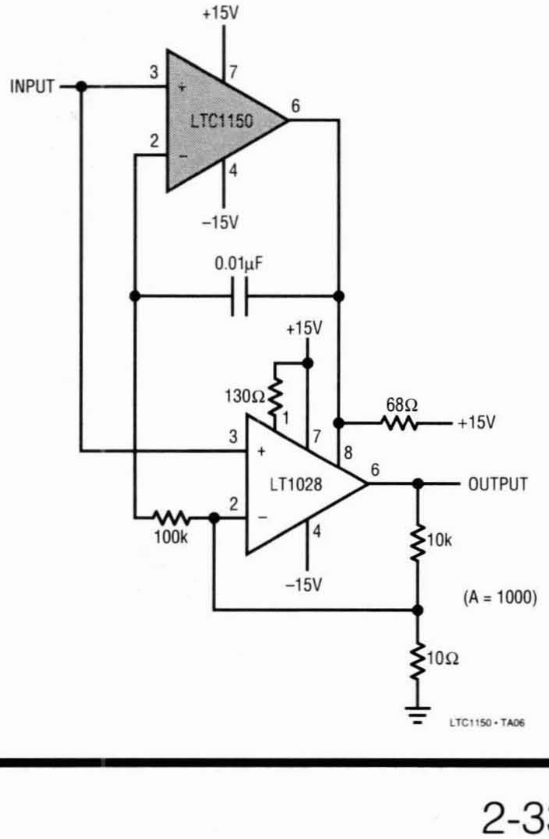
Battery Discharge Monitor


OPEN AT t = 0
C
+
−
R2
2
3
6
LTC1150
I
LOAD
R1
LTC1150 • TA10

$$V_{OUT} = \frac{-IR1}{R2C}t$$

$$ERROR \le \frac{5\mu V}{IR1} + \frac{30pA}{I}\frac{R2}{R1}$$

DC Stabilized, Low Noise Amplifier


+15V
INPUT
3
7
6
2
4
LTC1150
−15V
0.01µF
+15V
130Ω
1
7
8
68Ω
+15V
3
+
LT1028
6
OUTPUT
2
−
100k
4
−15V
10k
(A = 1000)
10Ω
LTC1150 • TA06

NOTES

SECTION 3—INSTRUMENTATION AMPLIFIERS

SECTION 3—INSTRUMENTATION AMPLIFIERS

INDEX 3-2
SELECTION GUIDE 3-3

PROPRIETARY PRODUCTS

LTC1100, Precision, Zero Drift Instrumentation Amplifier 3-4
LT1101, Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain = 10 or 100) 3-11
LT1102, High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100) 3-23
LT1193, Video Difference Amplifier, Adjustable Gain 2-159
LT1194, Video Difference Amplifier, Gain of 10 2-171

Instrumentation Amps

Micropower Single Supply

LT1101

	AM/AI/AC	M/I/C	S
Fixed Gains Available	10, 100	10, 100	10, 100
Max Gain Error	0.040%	0.060%	0.060%
Max Gain Non-Linearity	7ppm	8ppm	8ppm
Max V_{OS}	160μV	220μV	250μV
Max I_{OS}	0.6nA	0.9nA	0.9nA
Max I_B	8nA	10nA	10nA
Max Supply Current	105μA	120μA	120μA
Min CMRR	95dB	92dB	92dB
Min Supply Voltage	2.3V	2.3V	2.3V
Max Output Swing	3.5V/0.001V	3.5V/0.001V	3.5V/0.001V
Packages Available	H, J8/N8/H, J8, N8	H, J8/N8/H, J8, N8	S

Fast JFET Input

LT1102

	AM/AC	M/I/C
Fixed Gains Available	10, 100	10, 100
Min Slew Rate	21V/μs	18V/μs
Max Settling Time to 0.01%	6.5μs	6.5μs
Min Gain Bandwidth Product	20MHz	17MHz
Max Gain Error	0.05%	0.07%
Max Gain Non-Linearity	14ppm	18ppm
Max Offset Voltage	600μV	900μV
Max Bias Current	40pA	60pA
Min CMRR	84dB	82dB
Max Supply Current	5.0mA	5.6mA
Packages Available	H/H, N8	H, J8/N8/H, J8, N8

Low Offset, Low Drift

LTC1100

	C (–40°C to 85°C)	CS (–40°C to 85°C)
Fixed Gains Available	100	10,100
Max Gain Error	0.075%	0.075%
Max Gain Non-Linearity	20ppm	20ppm
Max V_{OS}	10μV	10μV
Max V_{OS} Drift with Temperature	0.01μV/°C	0.01μV/°C
Typ 0.1Hz to 10Hz Input Noise Voltage	1.9μVp-p	1.9μVp-p
Max I_B	65pA	65pA
Min CMRR	90dB	90dB
Max Supply Current	3.8mA	3.8mA
Packages Available	N8	S

LINEAR TECHNOLOGY

LTC1100

Precision, Chopper Stabilized Instrumentation Amplifier

FEATURES

- Offset Voltage 10µV Max
- Offset Voltage Drift 50nV/°C Max
- Bias Current 50pA Max
- Offset Current 50pA Max
- Gain Non-Linearity 8ppm Max
- Gain Error ±0.05% Max
- CMRR 104dB
- 0.1Hz-10Hz Noise 2µVp-p
- Single 5V Supply Operation
- 8-Pin MiniDIP

APPLICATIONS

- Thermocouple Amplifiers
- Strain Gauge Amplifiers
- Differential to Single Ended Converters

DESCRIPTION

The LTC1100 is a high precision instrumentation amplifier using chopper stabilization techniques to achieve outstanding DC performance. The input DC offset is typically 1µV while the DC offset drift is typically 10nV/°C; a very low bias current of 50pA is also achieved.

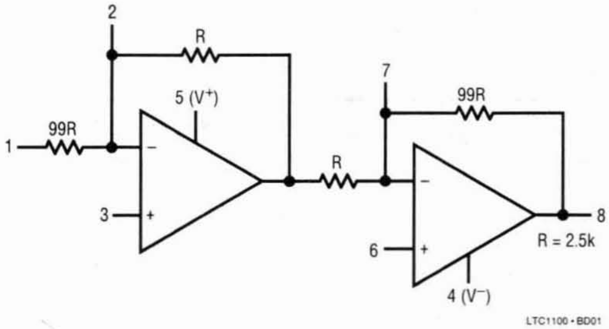
The LTC1100 is self contained; that is, it achieves a differential gain of 100 without any external gain setting resistor or trim pot. The gain linearity is 8ppm and the gain drift is 4ppm/°C. The LTC1100 operates from a single 5V supply up to ±8V. The output typically swings 300mV from its power supply rails with a 10k load.

An optional external capacitor can be added from pin 7 to pin 8 to tailor the device's 18kHz bandwidth and to eliminate any unwanted noise pickup.

The LTC1100 is also offered in a 16-pin surface mount package with selectable gains of 10 or 100.

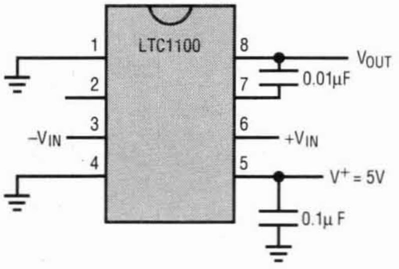
The LTC1100 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

BLOCK DIAGRAM



TYPICAL APPLICATION

Single 5V Supply, DC Instrumentation Amplifier



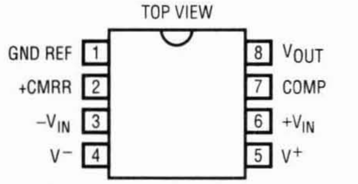
$V_{OUT} = 100\ (+V_{IN} - -V_{IN})$

LTC1100 • TA01

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range
LTC1100M/AM .... −55°C to 125°C
LTC1100C/AC .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C
Total Supply Voltage (V^+ to V^-) 18V
Input Voltage .... (V^+ + 0.3V) to (V^- − 0.3V)
Output Short Circuit Duration .... Indefinite

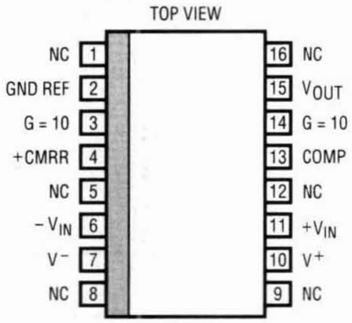
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

J8 PACKAGE
8-LEAD CERAMIC DIP

ORDER PART NUMBER
LTC1100ACN/ACJ LTC1100CN/CJ LTC1100AMJ LTC1100MJ



S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER
LTC1100ACS LTC1100CS

ELECTRICAL CHARACTERISTICS $V_S=\pm5V$, $R_L=10k$, $C_C=1000pF$, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1100ACN/ACJ MIN	LTC1100ACN/ACJ TYP	LTC1100ACN/ACJ MAX	LTC1100CN/CJ MIN	LTC1100CN/CJ TYP	LTC1100CN/CJ MAX	UNITS
Gain Error	$T_A = 25°C$			0.01	0.05		0.01	0.075	±%
		●			0.1			0.15	
Gain Non-Linearity	$T_A = 25°C$			3	8		3	20	ppm
		●		12	30		12	60	
Input Offset Voltage	(Note 1)			±1	±10		±1	±10	μV
Input Offset Voltage Drift	(Note 1)	●		±5	±100		±5	±100	nV/°C
Input Noise Voltage	DC to 10Hz, $T_A = 25°C$			1.9			1.9		μVp-p
Input Bias Current	$T_A = 25°C$			2.5	50		2.5	65	pA
		●			120			135	
Input Offset Current		●		10	50		10	65	pA
Common Mode Rejection Ratio	$V_{CM} = +2.3V$ to $-4.7V$ (Note 2)	●	104	115		90	110		dB
Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm8V$	●	120			105			dB
Output Voltage Swing	$R_L = 2k\Omega$, $V_S = \pm8V$	●	−7.2		6.2	−7.2		6.2	V
	$R_L = 10k\Omega$, $V_S = \pm8V$	●	−7.7		7.5	−7.7		7.5	
Supply Current	$T_A = 25°C$			2.4	2.8		2.4	3.3	mA
		●		3.4	4		3.4	4.5	
Internal Sampling Frequency	$T_A = 25°C$			2.8			2.8		kHz
Bandwidth	$T_A = 25°C$			18			18		kHz

ELECTRICAL CHARACTERISTICS

$V_S = \pm5V$, $R_L = 10k$, $C_C = 1000pF$, unless otherwise specified.

			LTC1100AMJ			LTC1100MJ			
PARAMETER	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Gain Error	$T_A = 25°C$			0.01	0.05		0.01	0.075	±%
		●			0.11			0.15	
Gain Non-Linearity	$T_A = 25°C$			3	8		3	20	ppm
		●			40			65	
Input Offset Voltage	(Note 1)			±1	±10		±1	±10	μV
Input Offset Voltage Drift	(Note 1)	●		±5	±100		±5	±100	nV/°C
Input Noise Voltage	DC to 10Hz, $T_A = 25°C$			1.9			1.9		μVp-p
Input Bias Current	$T_A = 25°C$			5	50		5	65	pA
		●			300			450	
Input Offset Current		●			80			120	pA
Common Mode Rejection Ratio	$V_{CM} = -4.7V$ to $+2.3V$	●	100			90			dB
Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm8V$	●	115			95			dB
Output Voltage Swing	$R_L = 10k\Omega$, $V_S = \pm8V$	●	−7.4		7.4	−7.4		7.4	V
	$R_L = 2k\Omega$, $V_S = \pm8V$	●	−7.0		6.0	−7.0		6.0	
Supply Current	$T_A = 25°C$			2.4			2.4	3.3	mA
		●			4.2			4.6	
Internal Sampling Frequency	$T_A = 25°C$			2.8			2.8		kHz
Bandwidth	$T_A = 25°C$			18			18		kHz

ELECTRICAL CHARACTERISTICS

$V_S = \pm5V$, $R_L = 10k$, $C_C = 1000pF$, unless otherwise specified.

			LTC1100ACS			LTC1100CS			
PARAMETER	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Gain Error	$T_A = 25°C$, $A_V = 100$			0.01	0.05		0.01	0.075	±%
	$A_V = 100$	●			0.1			0.15	
	$A_V = 10$			0.01	0.04		0.01	0.06	
	$A_V = 10$	●			0.1			0.15	
Gain Non-Linearity	$T_A = 25°C$, $A_V = 100$			3	8		3	20	ppm
	$A_V = 100$	●		12	30		12	60	
	$A_V = 10$			1	8		1	10	
	$A_V = 10$	●			25			40	
Input Offset Voltage	(Note 1)			±1	±10		±1	±10	μV
Input Offset Voltage Drift	(Note 1)	●		±5	±100		±5	±100	nV/°C
Input Noise Voltage	DC to 10Hz, $T_A = 25°C$			1.9			1.9		μVp-p
Input Bias Current	$T_A = 25°C$			2.5	50		2.5	65	pA
		●			120			135	
Input Offset Current		●		10	50		10	65	pA
Common Mode Rejection Ratio	$V_{CM} = -4.7V$ to $+2.3V$,								
	$A_V = 100$	●	104	115		90	110		dB
	$A_V = 10$	●	95			85			
Power Supply Rejection Ratio	$V_S = \pm2.375V$ to $\pm8V$	●	120			105			dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $R_L = 10k$, $C_C = 1000pF$, unless otherwise specified.

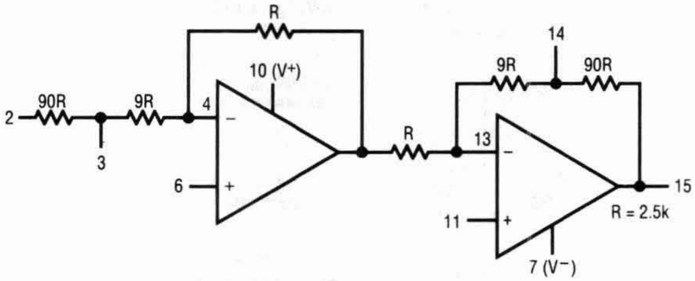
PARAMETER		CONDITIONS		LTC1100ACS MIN	LTC1100ACS TYP	LTC1100ACS MAX	LTC1100CS MIN	LTC1100CS TYP	LTC1100CS MAX	UNITS
Output Voltage Swing		$R_L = 10k\Omega$, $V_S = \pm 8V$	●	−7.2		6.2	−7.2		6.2	V
		$R_L = 2k\Omega$, $V_S = \pm 8V$	●	−7.7		7.5	−7.7		7.5	
Supply Current		$T_A = 25°C$			2.4	2.8		2.4	3.3	mA
			●		3.4	4		3.4	4.5	
Internal Sampling Frequency		$T_A = 25°C$			2.8			2.8		kHz
Bandwidth	G = 100	$T_A = 25°C$			18			18		kHz
	G = 10				180			180		

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

Note 2: See Applications Information, Single Supply Operation.

LTC1100CS BLOCK DIAGRAM

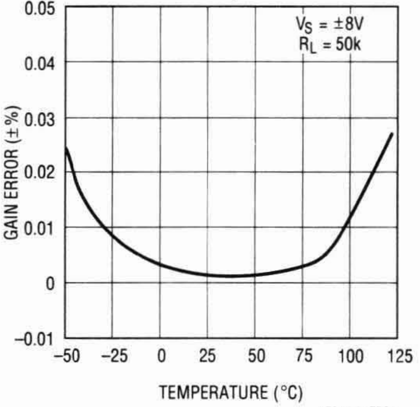


NOTE: FOR A VOLTAGE GAIN OF 10V/V SHORT PIN 2 TO 3, AND PIN 14 TO 15.

LTC1100 • BD02

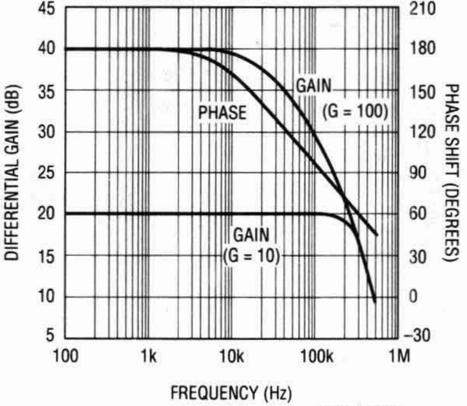
TYPICAL PERFORMANCE CHARACTERISTICS

Gain Error vs Temperature



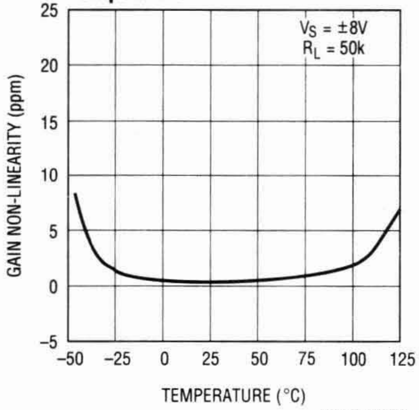
LTC1100 • TPC01

Gain, Phase vs Frequency



LTC1100 • TPC03

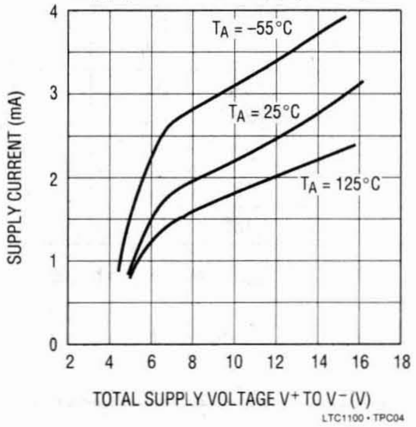
Gain Non-Linearity vs Temperature



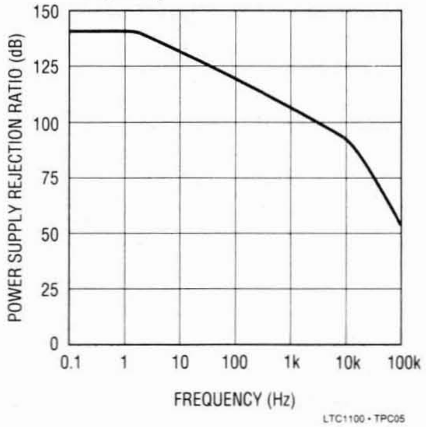
LTC1100 • TPC02

TYPICAL PERFORMANCE CHARACTERISTICS

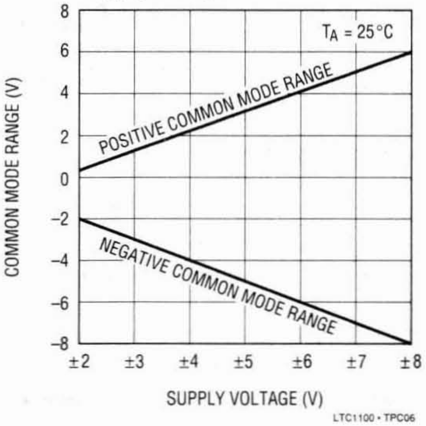
Supply Current vs Supply Voltage



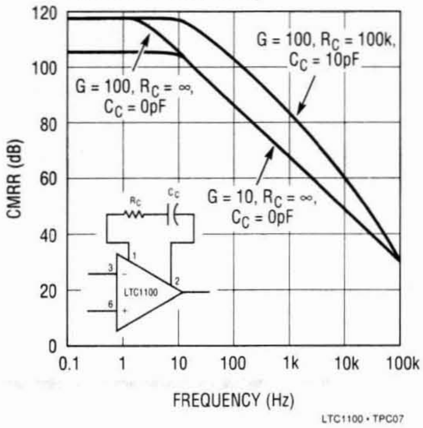
Power Supply Rejection Ratio vs Frequency



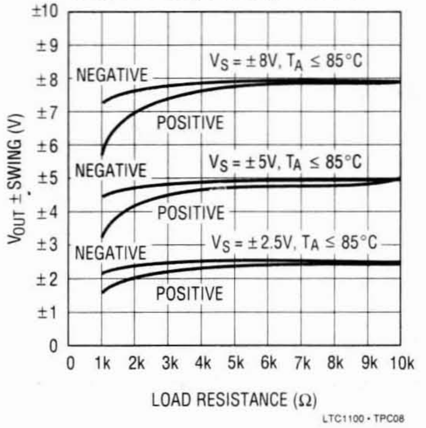
Common Mode Range vs Supply Voltage



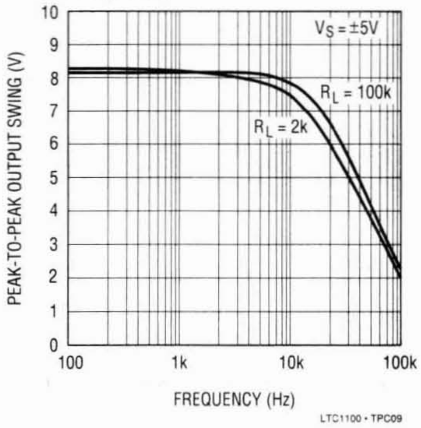
CMRR vs Frequency



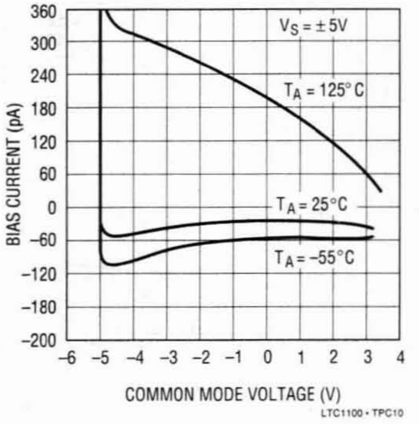
Output Voltage Swing vs Load



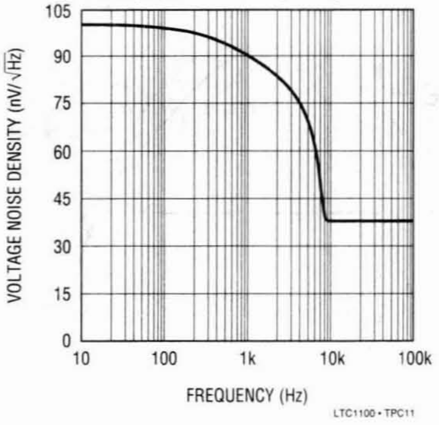
Undistorted Output Swing vs Frequency



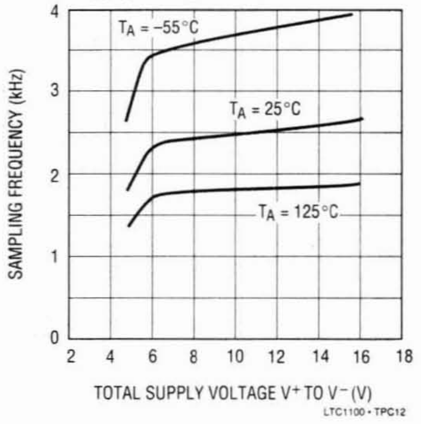
Bias Current vs Common Mode Voltage



Voltage Noise vs Frequency

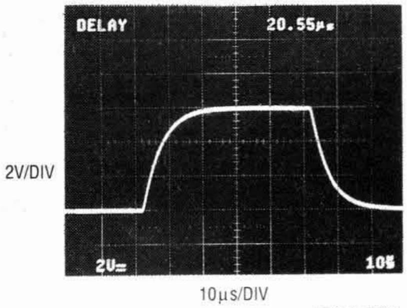


Internal Sampling Frequency vs Supply Voltage



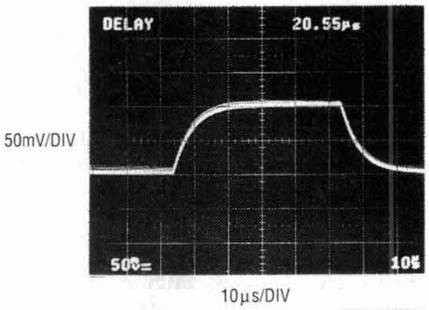
TYPICAL PERFORMANCE CHARACTERISTICS

Large Signal Transient Response
G=100, $V_S=\pm5V$



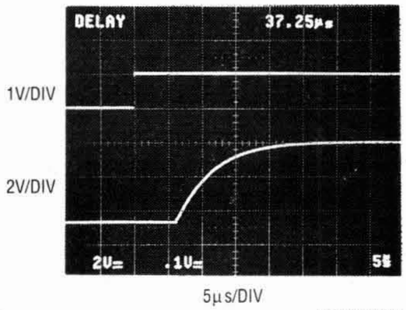
LTC1100 • TPC13

Small Signal Transient Response
G=100, $V_S=\pm5V$



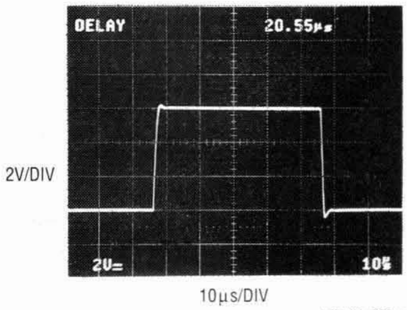
LTC1100 • TPC14

Overload Recovery
G=100, $V_S=\pm5V$



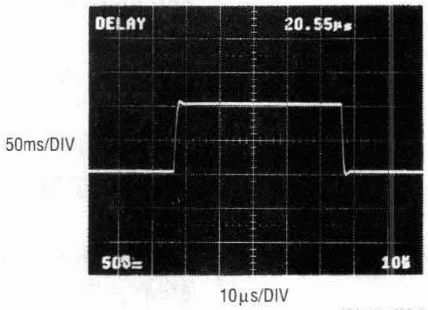
LTC1100 • TPC15

Large Signal Transient Response
G=10 (LTC1100CS Only), $V_S=\pm5V$



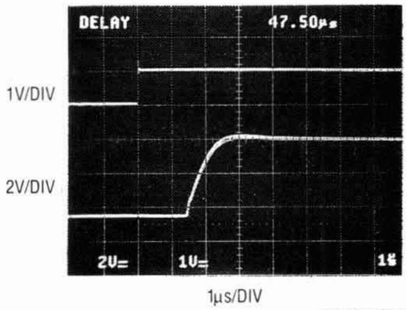
LTC1100 • TPC16

Small Signal Transient Response
G=10 (LTC1100CS Only), $V_S=\pm5V$



LTC1100 • TPC17

Overload Recovery
G=10 (LTC1100CS Only), $V_S=\pm5V$



LTC1100 • TPC18

PIN DESCRIPTION

8-Pin DIP (16-Pin SO)

Pin 1 (2) GND REF – Connect to system ground. This sets the zero reference for the internal op amps.

Pin 2 (4) +CMRR – This pin tailors the gain of the internal amplifiers to maximize AC CMRR. For applications which emphasize CMRR requirements, connect a 100k resistor and a 10pF capacitor in series from +CMRR to ground. See the Applications section.

Pin 3 (6) $-V_{IN}$ – Inverting Input.

Pin 4 (7) V^- – Negative Supply.

Pin 5 (10) V^+ – Positive Supply.

Pin 6 (11) $+V_{IN}$ – Non-Inverting Input.

Pin 7 (13) COMP – This pin reduces the bandwidth of the internal amplifiers for applications at or near DC. Clock feedthru from the internal sampling clock can also be suppressed by using the COMP pin. The standard compensation circuit is a capacitor from COMP to V_{OUT}, sized to provide an RC pole with the internal 247k resistor (22.5k for LTC1100CS in gain-of-10 mode). See the Applications section.

Pin 8 (15) V_{OUT} – Signal Output.

16-Pin SO Package Only

(3) G=10 – Short to pin (2) for gain of 10. Leave disconnected for gain of 100.

(14) G=10 – Short to pin (15) for gain of 10. Leave disconnected for gain of 100.

NOTE: *Both* pins must be shorted or open to provide correct gain.

(1),(5),(8),(9),(12),(16) NC – No internal connection.

APPLICATIONS INFORMATION

Common Mode Rejection

Due to very precise matching of the internal resistors, no trims are required to obtain a DC CMRR of better than 100dB. However, things change as frequency rises. The inverting amplifier is in a gain of 1.01 (1.1 for gain of 10), while the non-inverting amplifier is in a gain of 99 (9 for gain of 10). As frequency rises, the higher gain amplifier hits its gain-bandwidth limit long before the low gain amplifier, degrading CMRR. The solution is straightforward — slow down the inverting amplifier to match the non-inverting amp. Figure 1 shows the recommended circuit. The problem is less pronounced in the LTC1100CS in gain-of-10 mode; no CMRR trims are necessary.

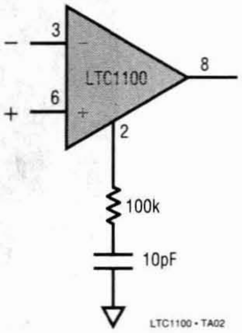


Figure 1. Improving AC CMRR

Overcompensation

Many instrumentation amplifier applications process DC or low frequency signals only; consequently the 18kHz (180kHz for G=10) bandwidth of the LTC1100 can be reduced to minimize system errors or reduce transmitted clock noise by using the COMP pin. A feedback cap from COMP to V_{OUT} will react with the 247k internal resistor (22.5k for G=10) to limit the bandwidth, as in Figure 2.

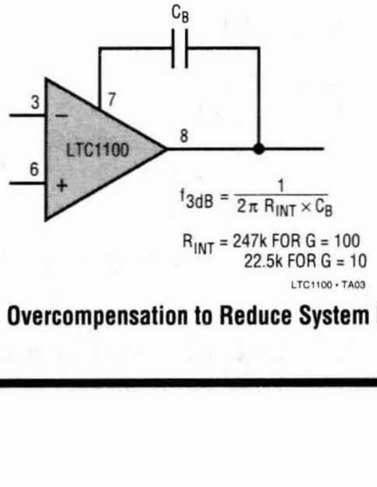

C_B
3
–
7
LTC1100
8
6
+
$f_{3dB} = \frac{1}{2\pi R_{INT} \times C_B}$
R_{INT} = 247k FOR G = 100
22.5k FOR G = 10
LTC1100 • TA03

Figure 2. Overcompensation to Reduce System Bandwidth

Aliasing

The LTC1100 is a chopper stabilized instrumentation amplifier; like all sampled systems it exhibits aliasing behavior for input frequencies at or near the internal sampling frequency. The LTC1100 incorporates specialized anti-aliasing circuitry which typically attenuates aliasing products by ≥60dB; however, extremely sensitive systems may still have to take precautions to avoid aliasing errors. For more information, see the LTC1051/1053 data sheet.

Single Supply Operation

The LTC1100 will operate on a single 5V supply, and the common mode range of the internal op amps includes ground; single supply operation is limited only by the output swing of the op amps. The internal inverting amplifier has a negative saturation limit of 5mV typically, setting the minimum common mode limit at 5mV/1.01 (or 1.1 for gain of 10). The inputs can be biased above ground as shown in Figure 3. Low cost biasing components can be used since any errors appear as a common mode term and are rejected.

The minimum differential input voltage is limited by the swing of the output op amp. Lightly loaded, it will swing down to 5mV, allowing differential input voltages as low as 50µV (450µV for gain of 10). Single supply operation limits the LTC1100 to positive differential inputs only; negative inputs will give a saturated zero output.

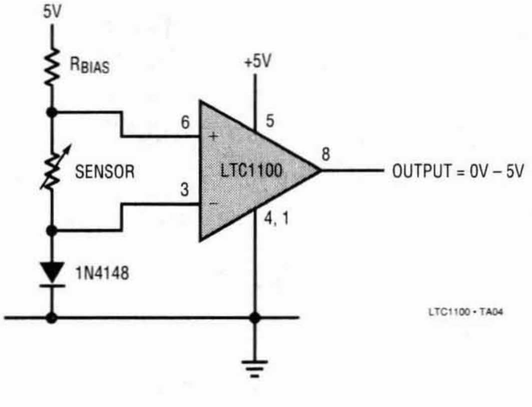


Figure 3.

Precision, Micropower, Single Supply Instrumentation Amplifier (Fixed Gain =10 or 100)

FEATURES

■ Gain Error	0.04% Max
■ Gain Non-Linearity	0.0008% (8ppm) Max
■ Gain Drift	4ppm/°C Max
■ Supply Current	105µA Max
■ Offset Voltage	160µV Max
■ Offset Voltage Drift	0.4µV/°C Typ
■ Offset Current	600pA Max
■ CMRR, G = 100	100dB Min
■ 0.1Hz to 10Hz Noise	0.9µVp-p Typ 2.3pAp-p Typ
■ Gain Bandwidth Product	250kHz Min
■ Single or Dual Supply Operation	
■ Surface Mount Package Available	

APPLICATIONS

- Differential Signal Amplification in Presence of Common-Mode Voltage
- Micropower Bridge Transducer Amplifier
  - Thermocouples
  - Strain Gauges
  - Thermistors
- Differential Voltage to Current Converter
- Transformer Coupled Amplifier
- 4mA-20mA Bridge Transmitter

DESCRIPTION

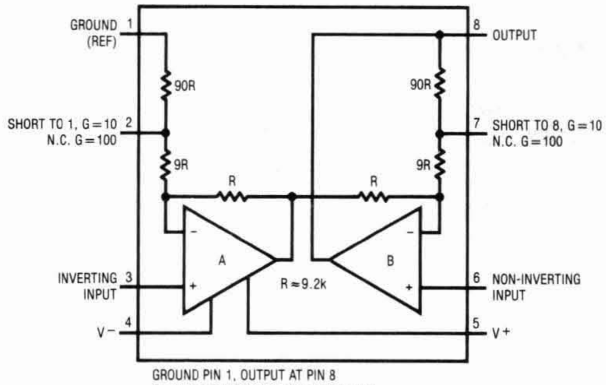
The LT1101 establishes the following milestones:
(1) It is the first micropower instrumentation amplifier,
(2) It is the first single supply instrumentation amplifier,
(3) It is the first instrumentation amplifier to feature fixed gains of 10 and/or 100 in low cost, space-saving 8-lead packages.

The LT1101 is completely self-contained: no external gain setting resistor is required. The LT1101 combines its micropower operation (75µA supply current) with a gain error of 0.008%, gain linearity of 3ppm, gain drift of 1ppm/°C. The output is guaranteed to drive a 2k load to ±10V with excellent gain accuracy.

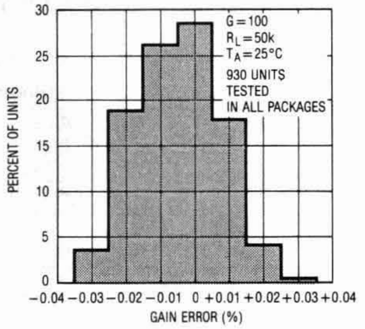
Other precision specifications are also outstanding: 50µV input offset voltage, 130pA input offset current, and low drift (0.4µV/°C and 0.7pA/°C). In addition, unlike other instrumentation amplifiers, there is no output offset voltage contribution to total error.

A full set of specifications are provided with ±15V dual supplies and for single 5V supply operation. The LT1101 can be operated from a single lithium cell or two Ni-Cad batteries. Battery voltage can drop as low as 1.8V, yet the LT1101 still maintains its gain accuracy. In single supply applications, both input and output voltages swing to within a few millivolts of ground. The output sinks current while swinging to ground — no external, power consuming pull down resistors are needed.

BLOCK DIAGRAM



GROUND PIN 1, OUTPUT AT PIN 8
G = 100: NO ADDITIONAL CONNECTIONS
G = 10: SHORT PIN 2 TO PIN 1, SHORT PIN 7 TO PIN 8

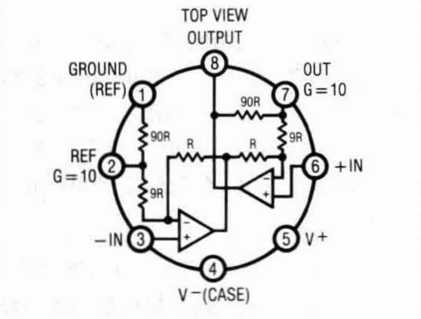

Gain Error Distribution

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±22V
Differential Input Voltage .... ±36V
Input Voltage .... Equal to Positive Supply Voltage
.... 10V Below Negative Supply Voltage
Output Short Circuit Duration .... Indefinite
Lead Temperature (Soldering, 10 sec.) .... 300°C

Operating Temperature Range
LT1101AM/LT1101M .... –55°C to 125°C
LT1101AI/LT1101I .... –40°C to 85°C
LT1101AC/LT1101C/LT1101S .... 0°C to 70°C
Storage Temperature Range
All Grades .... –65°C to 150°C

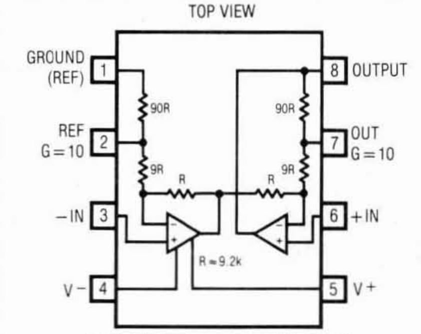
PACKAGE/ORDER INFORMATION


TOP VIEW
OUTPUT
8
GROUND
(REF)
1
OUT
G = 10
7
90R
90R
9R
9R
R
R
REF
G = 10
2
6
+IN
–IN
3
5
V+
4
V–(CASE)

H PACKAGE
8-LEAD TO-5 METAL CAN

ORDER PART NUMBER

LT1101AMH
LT1101MH
LT1101ACH
LT1101CH

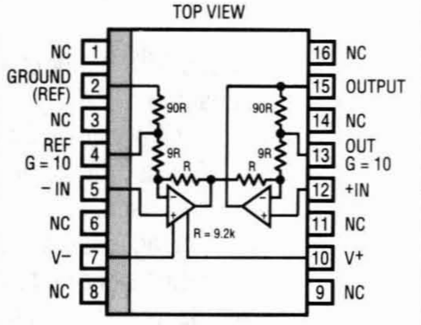

TOP VIEW
GROUND
(REF)
1
8
OUTPUT
90R
90R
REF
G = 10
2
7
OUT
G = 10
9R
9R
R
R
–IN
3
6
+IN
R = 9.2k
V–
4
5
V+

N PACKAGE
8-LEAD PLASTIC DIP

J PACKAGE
8-LEAD CERAMIC DIP

ORDER PART NUMBER

LT1101AIN8
LT1101IN8
LT1101ACN8
LT1101CN8
LT1101AMJ8
LT1101MJ8
LT1101ACJ8
LT1101CJ8


TOP VIEW
NC
1
16
NC
GROUND
(REF)
2
15
OUTPUT
NC
3
14
NC
90R
90R
REF
G = 10
4
13
OUT
G = 10
9R
9R
R
R
–IN
5
12
+IN
NC
6
11
NC
R = 9.2k
V–
7
10
V+
NC
8
9
NC

S PACKAGE
16-LEAD PLASTIC SOL

LT1101S

ELECTRICAL CHARACTERISTICS

$V_S = 5V, 0V, V_{CM} = 0.1V, V_{REF(PIN\ 1)} = 0.1V, G = 10$ or $100, T_A = 25°C$, unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS	LT1101AM/AI/AC MIN	LT1101AM/AI/AC TYP	LT1101AM/AI/AC MAX	LT1101M/I/C/S MIN	LT1101M/I/C/S TYP	LT1101M/I/C/S MAX	UNITS
G_E	Gain Error	$G = 100, V_O = 0.1V$ to $3.5V, R_L = 50k$		0.010	0.050		0.011	0.075	%
		$G = 10, V_O = 0.1V$ to $3.5V, R_L = 50k$		0.009	0.040		0.010	0.060	%
G_{NL}	Gain Non-Linearity	$G = 100, R_L = 50k$		20	60		20	75	ppm
		$G = 10, R_L = 50k$ (Note 1)		3	7		3	8	ppm
V_{OS}	Input Offset Voltage			50	160		60	220	μV
		LT1101S					250	600	μV
I_{OS}	Input Offset Current			0.13	0.60		0.15	0.90	nA
I_B	Input Bias Current			6	8		6	10	nA
I_S	Supply Current			75	105		78	120	μA

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, $V_{REF(PIN\ 1)}$ = 0.1V, G = 10 or 100, T_A = 25°C, unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS	LT1101AM/AI/AC MIN	TYP	MAX	LT1101M/I/C/S MIN	TYP	MAX	UNITS
CMRR	Common-Mode Rejection Ratio	1k Source Imbalance							
		G = 100, V_{CM} = 0.07V to 3.4V	95	106		92	105		dB
		G = 10, V_{CM} = 0.07V to 3.1V	84	100		82	99		dB
	Minimum Supply Voltage	(Note 4)		1.8	2.3		1.8	2.3	V
V_O	Maximum Output Voltage Swing	Output High, 50k to GND	4.1	4.3		4.1	4.3		V
		Output High, 2k to GND	3.5	3.9		3.5	3.9		V
		Output Low, V_{REF} = 0, No Load		3.3	6		3.3	6	mV
		Output Low, V_{REF} = 0, 2k to GND		0.5	1		0.5	1	mV
		Output Low, V_{REF} = 0, I_{SINK} = 100µA		90	130		90	130	mV
BW	Bandwidth	G = 100 (Note 1)	2.0	3.0		2.0	3.0		kHz
		G = 10 (Note 1)	22	33		22	33		kHz
SR	Slew Rate	(Note 1)	0.04	0.07		0.04	0.07		V/µs

ELECTRICAL CHARACTERISTICS

V_S = ± 15V, V_{CM} = 0V, T_A = 25°C, Gain = 10 or 100, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1101AM/AI/AC MIN	TYP	MAX	LT1101M/I/C/S MIN	TYP	MAX	UNITS
G_E	Gain Error	G = 100, V_O = ± 10V, R_L = 50k		0.008	0.040		0.009	0.060	%
		G = 100, V_O = ± 10V, R_L = 2k		0.011	0.055		0.012	0.070	%
		G = 10, V_O = ± 10V, R_L = 50k or 2k		0.008	0.040		0.009	0.060	%
G_{NL}	Gain Non-Linearity	G = 100, R_L = 50k		7	16		8	20	ppm
		G = 100, R_L = 2k		24	45		25	60	ppm
		G = 10, R_L = 50k or 2k		3	8		3	9	ppm
V_{OS}	Input Offset Voltage			50	160		60	220	µV
		LT1101S					250	600	µV
I_{OS}	Input Offset Current			0.13	0.60		0.15	0.90	nA
I_B	Input Bias Current			6	8		6	10	nA
	Input Resistance								
	Common-Mode	(Note 1)	4	7		3	7		GΩ
	Differential Mode	(Note 1)	7	12		5	12		GΩ
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.9	1.8		0.9		µVp-p
	Input Noise Voltage Density	f_o = 10Hz (Note 2)		45	64		45		nV/√Hz
		f_o = 1000Hz (Note 2)		43	54		43		nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		2.3	4.0		2.3		pAp-p
	Input Noise Current Density	f_o = 10Hz (Note 2)		0.06	0.10		0.06		pA/√Hz
		f_o = 1000Hz		0.02			0.02		pA/√Hz
	Input Voltage Range	G = 100	+13.0	+13.8		+13.0	+13.8		V
			−14.4	−14.7		−14.4	−14.7		V
		G = 10	+11.5	+12.5		+11.5	+12.5		V
			−13.0	−13.3		−13.0	−13.3		V
CMRR	Common-Mode Rejection Ratio	1k Source Imbalance							
		G = 100, Over CM Range	100	112		98	112		dB
		G = 10, Over CM Range	84	100		82	99		dB
PSRR	Power Supply Rejection Ratio	V_S = + 2.2V, − 0.1V to ± 18V	102	114		100	114		dB
I_S	Supply Current			92	130		94	150	µA
V_O	Maximum Output Voltage Swing	R_L = 50k	± 13.0	± 14.2		± 13.0	± 14.2		V
		R_L = 2k	± 11.0	± 13.2		± 11.0	± 13.2		V
BW	Bandwidth	G = 100 (Note 1)	2.3	3.5		2.3	3.5		kHz
		G = 10 (Note 1)	25	37		25	37		kHz
SR	Slew Rate		0.06	0.10		0.06	0.10		V/µs

Note 1: This parameter is not tested. It is guaranteed by design and by inference from other tests.

Note 2: This parameter is tested on a sample basis only.

Note 3: These test conditions are equivalent to V_S = 4.9V, − 0.1V, V_{CM} = 0V, $V_{REF(PIN\ 1)}$ = 0V.

Note 4: Minimum supply voltage is guaranteed by the power supply rejection test. The LT1101 actually works at 1.8V supply with minimal degradation in performance.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $-55°C \leq T_A \leq 125°C$ for AM/M grades, $-40°C \leq T_A \leq 85°C$ for AI/I grades, unless otherwise noted.

				LT1101AM/AI			LT1101M/I		
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
G_E	Gain Error	$G = 100$, $V_O = \pm 10V$, $R_L = 50k$		0.024	0.070		0.026	0.100	%
		$G = 100$, $V_O = \pm 10V$, $R_L = 5k$		0.030	0.100		0.035	0.130	%
		$G = 10$, $V_O = \pm 10V$, $R_L = 50k$ or $5k$		0.015	0.070		0.018	0.100	%
TCG_E	Gain Error Drift (Note 1)	$G = 100$, $R_L = 50k$		2	4		2	5	ppm/°C
		$G = 100$, $R_L = 5k$		2	7		2	8	ppm/°C
		$G = 10$, $R_L = 50k$ or $5k$		1	4		1	5	ppm/°C
G_{NL}	Gain Non-Linearity	$G = 100$, $R_L = 50k$		24	70		26	90	ppm
		$G = 100$, $R_L = 5k$		70	300		75	500	ppm
		$G = 10$, $R_L = 50k$		4	13		5	15	ppm
		$G = 10$, $R_L = 5k$		10	40		12	60	ppm
V_{OS}	Input Offset Voltage			90	350		110	500	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 1)		0.4	2.0		0.5	2.8	μV/°C
I_{OS}	Input Offset Current			0.16	0.80		0.19	1.30	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 1)		0.5	4.0		0.8	7.0	pA/°C
I_B	Input Bias Current			7	10		7	12	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 1)		10	25		10	30	pA/°C
CMRR	Common-Mode Rejection Ratio	$G = 100$, $V_{CM} = -14.4V$ to $13V$	96	111		94	111		dB
		$G = 10$, $V_{CM} = -13V$ to $11.5V$	80	99		78	98		dB
PSRR	Power Supply Rejection Ratio	$V_S = +3.0, -0.1V$ to $\pm 18V$	98	110		94	110		dB
I_S	Supply Current			105	165		108	190	μA
V_O	Maximum Output Voltage Swing	$R_L = 50k$	±12.5	±14.0		±12.5	±14.0		V
		$R_L = 5k$	±11.0	±13.5		±11.0	±13.5		V

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $0°C \leq T_A \leq 70°C$, unless otherwise noted.

				LT1101AC			LT1101C/S		
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
G_E	Gain Error	$G = 100$, $V_O = \pm 10V$, $R_L = 50k$		0.012	0.055		0.014	0.080	%
		$G = 100$, $V_O = \pm 10V$, $R_L = 2k$		0.018	0.085		0.020	0.100	%
		$G = 10$, $V_O = \pm 10V$, $R_L = 50k$ or $2k$		0.009	0.055		0.010	0.080	%
TCG_E	Gain Error Drift (Note 1)	$G = 100$, $R_L = 50k$		1	4		1	5	ppm/°C
		$G = 100$, $R_L = 2k$		2	7		2	9	ppm/°C
		$G = 10$, $R_L = 50k$ or $2k$		1	4		1	5	ppm/°C
G_{NL}	Gain Non-Linearity	$G = 100$, $R_L = 50k$		9	25		10	35	ppm
		$G = 100$, $R_L = 2k$		33	75		36	100	ppm
		$G = 10$, $R_L = 50k$ or $2k$		4	10		4	11	ppm
V_{OS}	Input Offset Voltage			70	250		85	350	μV
		LT1101S					300	800	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 1)		0.4	2.0		0.5	2.8	μV/°C
		LT1101S					1.2	4.5	μV/°C
I_{OS}	Input Offset Current			0.14	0.70		0.17	1.10	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 1)		0.5	4.0		0.8	7.0	pA/°C
I_B	Input Bias Current			6	9		6	11	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 1)		10	25		10	30	pA/°C
CMRR	Common-Mode Rejection Ratio	$G = 100$, $V_{CM} = -14.4V$ to $13V$	98	112		96	112		dB
		$G = 10$, $V_{CM} = -13V$ to $11.5V$	82	100		80	99		dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.5, -0.1V$ to $\pm 18V$	100	112		97	112		dB
I_S	Supply Current			98	148		100	170	μA
V_O	Maximum Output Voltage Swing	$R_L = 50k$	±12.5	±14.1		±12.5	±14.1		V
		$R_L = 2k$	±10.5	±13.0		±10.5	±13.0		V

ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, $V_{REF(PIN\ 1)}$ = 0.1V, Gain = 10 or 100, – 55°C ≤ T_A ≤ 125°C for AM/M grades, – 40°C ≤ T_A ≤ 85°C for AI/I grades, unless otherwise noted.

			LT1101AM/AI			LT1101M/I			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
G_E	Gain Error	G = 100, V_O = 0.1V to 3.5V, R_L = 50k G = 10, V_{CM} = 0.15, R_L = 50k		0.026 0.011	0.080 0.070		0.028 0.014	0.120 0.100	% %
TCG_E	Gain Error Drift	R_L = 50k (Note 1)		1	4		1	5	ppm/°C
G_{NL}	Gain Non-Linearity	G = 100, R_L = 50k G = 10, R_L = 50k (Note 1)		45 4	110 13		48 5	140 15	ppm ppm
V_{OS}	Input Offset Voltage			90	350		110	500	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 1)		0.4	2.0		0.5	2.8	μV/°C
I_{OS}	Input Offset Current			0.16	0.80		0.19	1.30	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 1)		0.5	4.0		0.8	7.0	pA/°C
I_B	Input Bias Current			7	10		7	12	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 1)		10	25		10	30	pA/°C
CMRR	Common-Mode Rejection Ratio	G = 100, V_{CM} = 0.1V to 3.2V G = 10, V_{CM} = 0.1V to 2.9V, V_{REF} = 0.15V	91 80	105 98		88 77	104 97		dB dB
I_S	Supply Current			88	135		92	160	μA
V_O	Maximum Output Voltage Swing	Output High, 50k to GND Output High, 2k to GND Output Low, V_{REF} = 0, No Load Output Low, V_{REF} = 0, 2k to GND Output Low, V_{REF} = 0, I_{SINK} = 100μA	3.8 3.0	4.1 3.7 4.5 0.7 125	 8 1.5 170	3.8 3.0	4.1 3.7 4.5 0.7 125	 8 1.5 170	V V mV mV mV

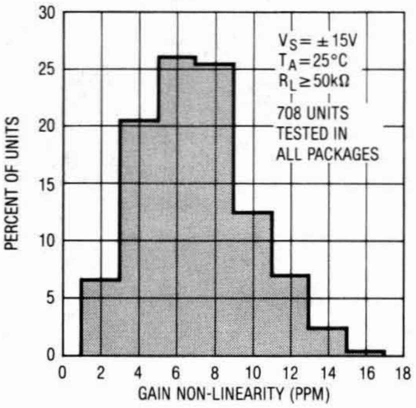
ELECTRICAL CHARACTERISTICS

V_S = 5V, 0V, V_{CM} = 0.1V, $V_{REF(PIN\ 1)}$ = 0.1V, Gain = 10 or 100, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

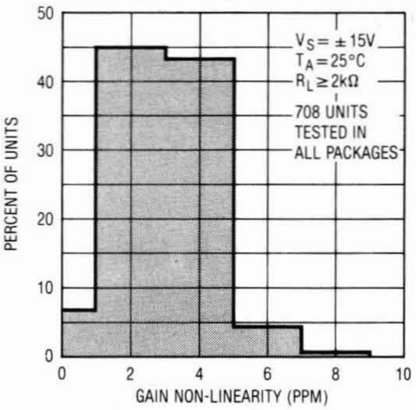
			LT1101AC			LT1101C/S			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
G_E	Gain Error	G = 100, V_O = 0.1V to 3.5V, R_L = 50k G = 10, V_{CM} = 0.15V, R_L = 50k		0.017 0.010	0.065 0.060		0.018 0.012	0.095 0.080	% %
TCG_E	Gain Error Drift	R_L = 50k (Note 1)		1	4		1	5	ppm/°C
G_{NL}	Gain Non-Linearity	G = 100, R_L = 50k G = 10, R_L = 50k (Note 1)		25 4	80 10		25 4	100 11	ppm ppm
V_{OS}	Input Offset Voltage	 LT1101S		70	250		85 300	350 800	μV μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 1) LT1101S		0.4	2.0		0.5 1.2	2.8 4.5	μV/°C μV/°C
I_{OS}	Input Offset Current			0.14	0.70		0.17	1.10	nA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 1)		0.5	4.0		0.8	7.0	pA/°C
I_B	Input Bias Current			6	9		6	11	nA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 1)		10	25		10	30	pA/°C
CMRR	Common-Mode Rejection Ratio	G = 100, V_{CM} = 0.07V to 3.3V G = 10, V_{CM} = 0.07V to 3.0V, V_{REF} = 0.15V	93 82	105 99		90 80	104 98		dB dB
I_S	Supply Current			80	120		85	145	μA
V_O	Maximum Output Voltage Swing	Output High, 50k to GND Output High, 2k to GND Output Low, V_{REF} = 0, No Load Output Low, V_{REF} = 0, 2k to GND Output Low, V_{REF} = 0, I_{SINK} = 100μA	4.0 3.3	4.2 3.8 4 0.6 100	 7 1.2 150	4.0 3.3	4.2 3.8 4 0.6 100	 7 1.2 150	V V mV mV mV

TYPICAL PERFORMANCE CHARACTERISTICS

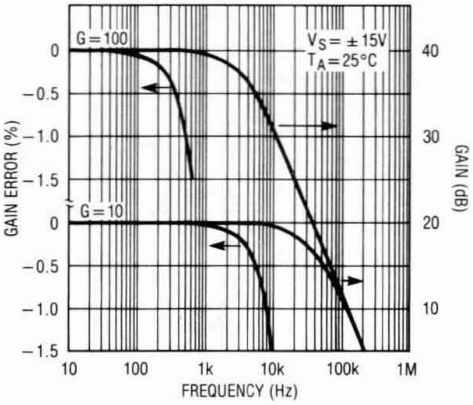
Gain = 100 Non-Linearity Distribution



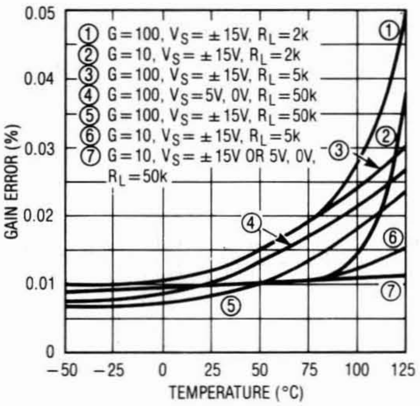
Gain = 10 Non-Linearity Distribution



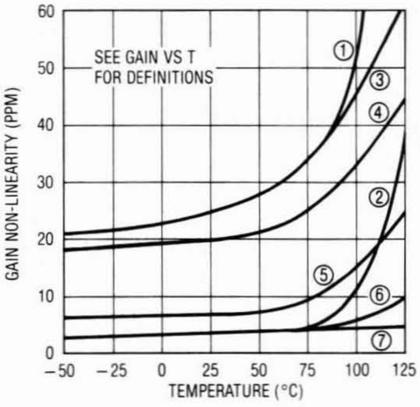
Gain vs Frequency



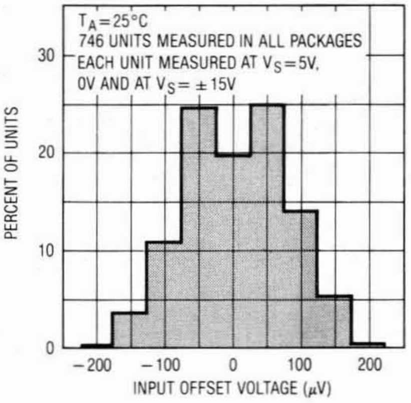
Gain Error Over Temperature



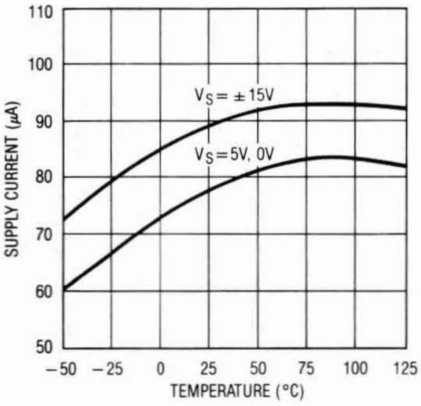
Gain Non-Linearity Over Temperature



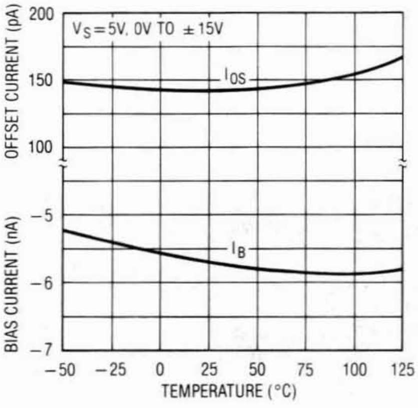
Input Offset Voltage Distribution



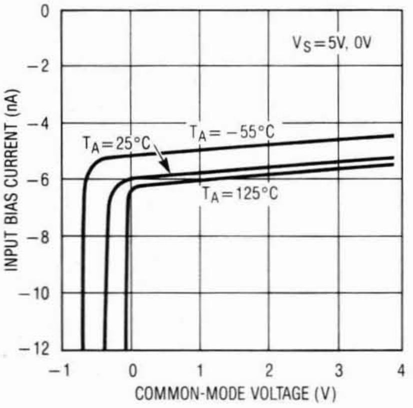
Supply Current vs Temperature



Input Bias and Offset Currents vs Temperature

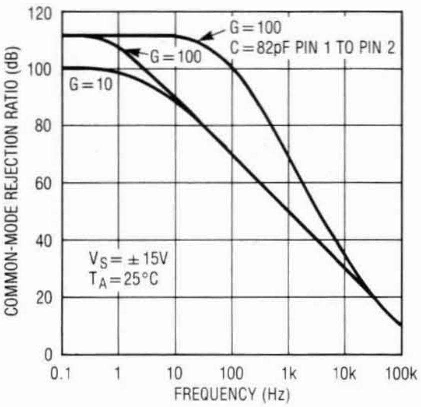


Input Bias Current vs Common-Mode Voltage

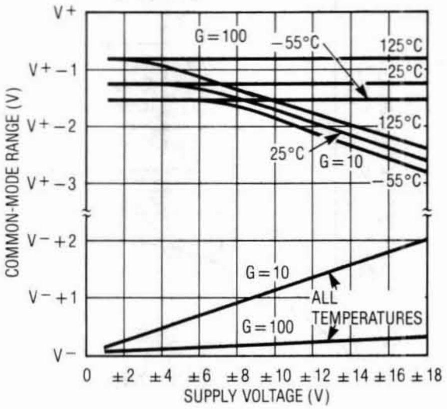


TYPICAL PERFORMANCE CHARACTERISTICS

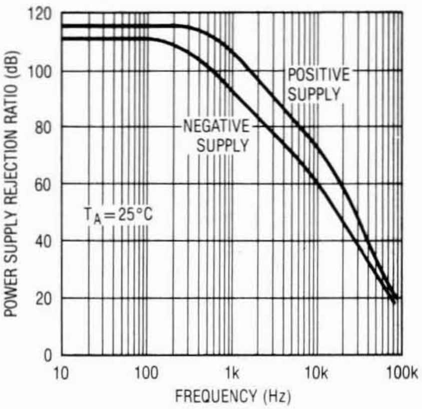
Common-Mode Rejection Ratio vs Frequency



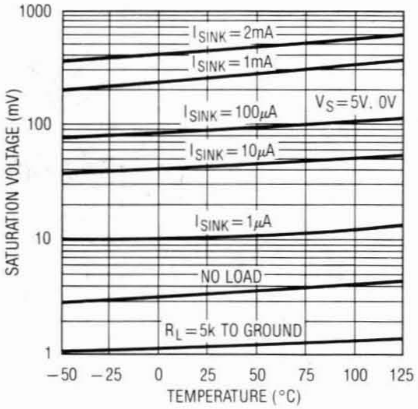
Common-Mode Range vs Supply Voltage



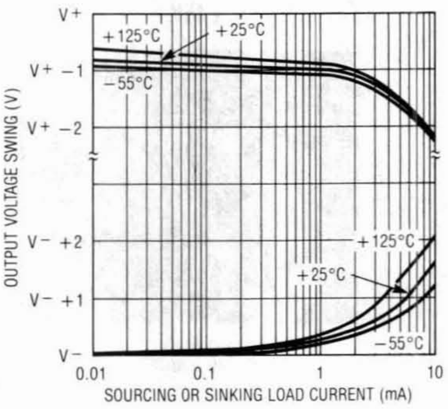
Power Supply Rejection Ratio vs Frequency



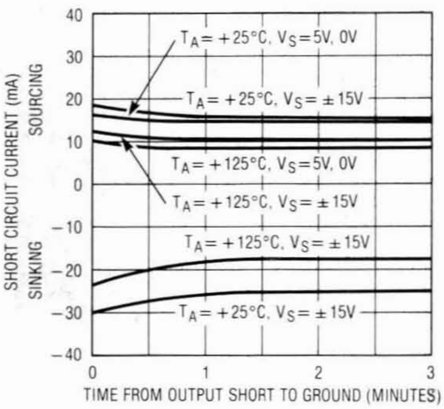
Output Saturation vs Temperature vs Sink Current



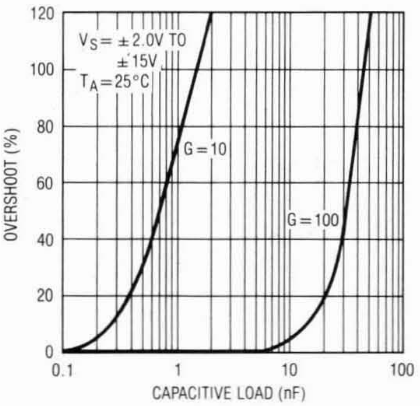
Output Voltage Swing vs Load Current



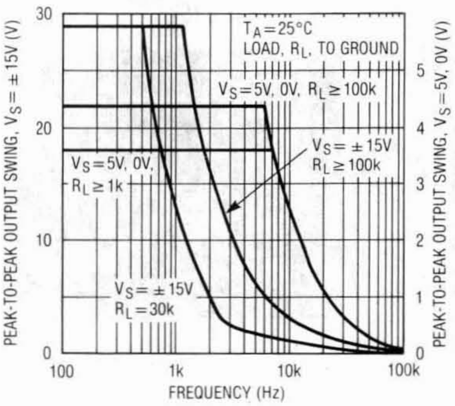
Short Circuit Current vs Time



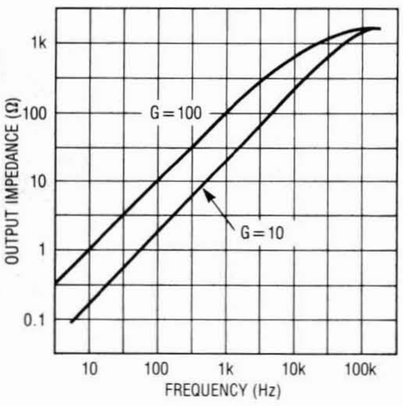
Capacitive Load Handling



Undistorted Output Swing vs Frequency

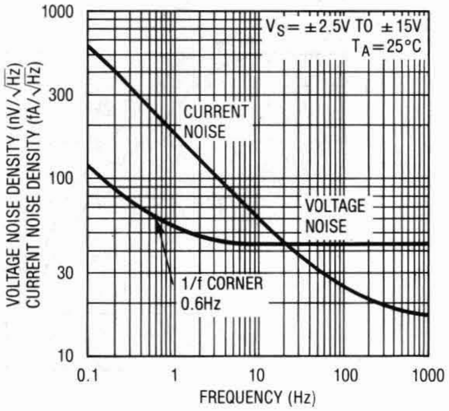


Output Impedance vs Frequency

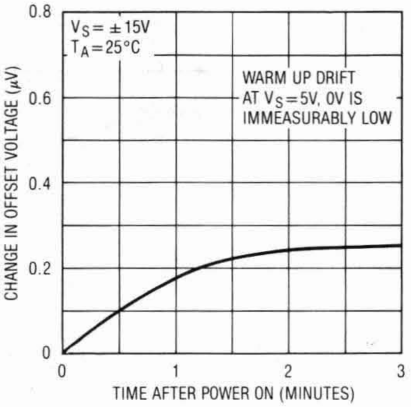


TYPICAL PERFORMANCE CHARACTERISTICS

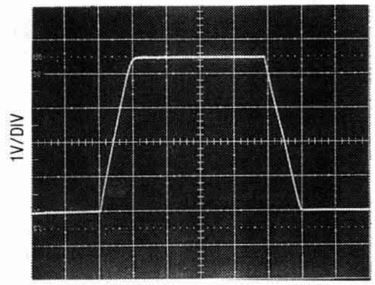
Noise Spectrum



Warm-Up Drift

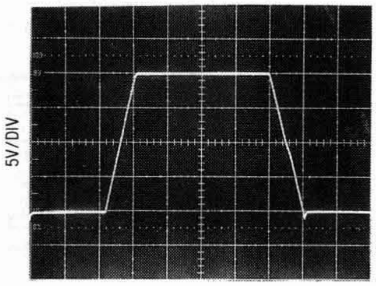


Large Signal Transient Response
G = 10, V_S = 5V, 0V



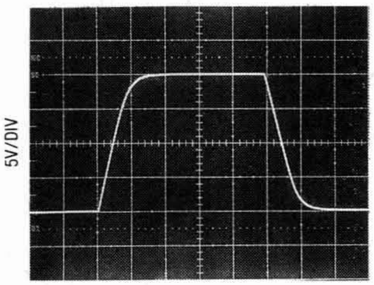
50µs/DIV
OUTPUT FROM 0V TO 4.5V, NO LOAD

Large Signal Transient Response
G = 10, V_S = ±15V



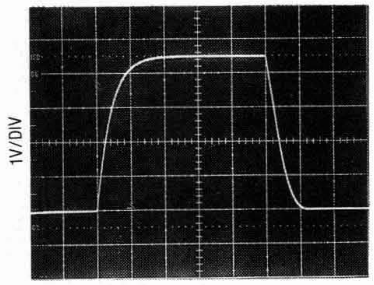
200µs/DIV
NO LOAD

Large Signal Transient Response
G = 100, V_S = ±15V



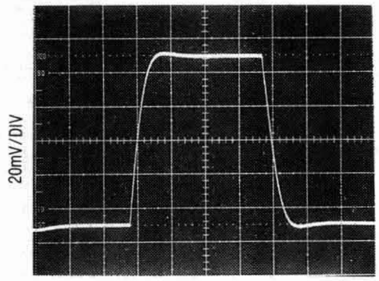
200µs/DIV
NO LOAD

Large Signal Transient Response
G = 100, V_S = 5V, 0V



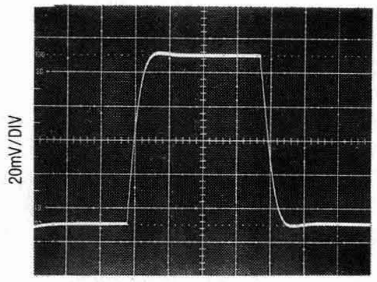
100µs/DIV
OUTPUT FROM 0V TO 4.5V, NO LOAD

Small Signal Transient Response
G = 10, V_S = 5V, 0V



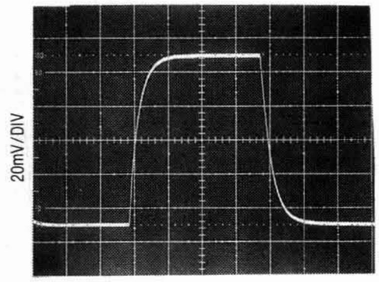
20µs/DIV
OUTPUT FROM 0.05V TO 0.15V, NO LOAD

Small Signal Transient Response
G = 10, V_S = ±15V



20µs/DIV

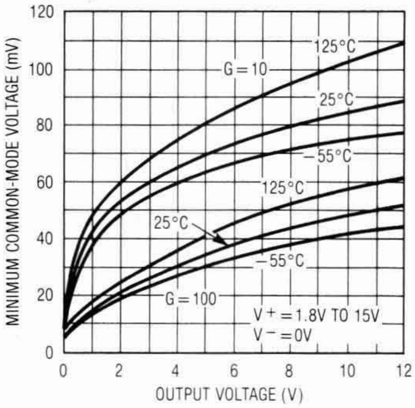
Small Signal Transient Response
G = 100, V_S = 5V, 0V



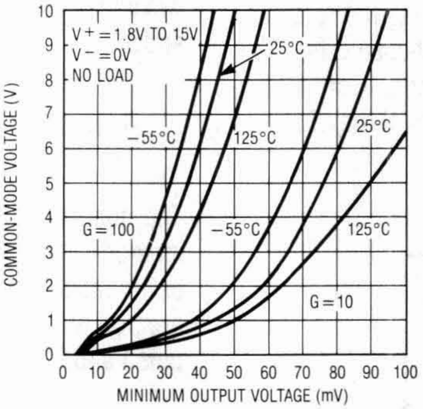
200µs/DIV
OUTPUT FROM 0.05V TO 0.15V, NO LOAD
(RESPONSE WITH V_S = ±15V, G = 100 IS IDENTICAL)

TYPICAL PERFORMANCE CHARACTERISTICS

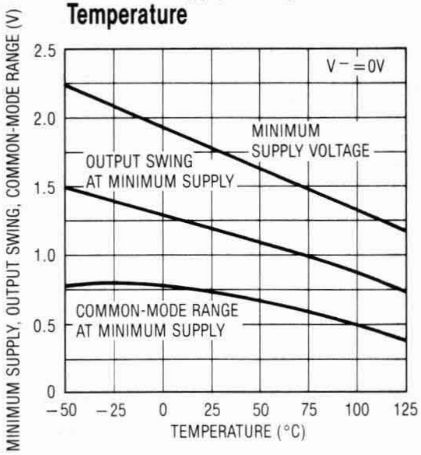
Single Supply: Minimum Common-Mode Voltage vs Output Voltage



Single Supply: Minimum Output Voltage vs Common-Mode Voltage



Minimum Supply Voltage vs Temperature



APPLICATIONS INFORMATION

Single Supply Applications

The LT1101 is the first instrumentation amplifier which is fully specified for single supply operation, i.e. when the negative supply is 0V. Both the input common-mode range and the output swing are within a few millivolts of ground.

Probably the most common application for instrumentation amplifiers is amplifying a differential signal from a transducer or sensor resistance bridge. All competitive instrumentation amplifiers have a minimum required common-mode voltage which is 3V to 5V above the negative supply. This means that the voltage across the bridge has to be 6V to 10V or dual supplies have to be used, i.e. micropower, single battery usage is not attainable on competitive devices.

The minimum output voltage obtainable on the LT1101 is a function of the input common-mode voltage. When the common-mode voltage is high and the output is low, current will flow from the output of amplifier A into the output of amplifier B. See the Minimum Output Voltage vs Common-Mode Voltage plot.

Similarly, the Minimum Common-Mode Voltage vs Output Voltage plot specifies the expected common-mode range. When the output is high and input common-mode is low, the output of amplifier A has to sink current coming from the output of amplifier B. Since amplifier A is effectively in unity gain, its input is limited by its output.

Common-Mode Rejection vs Frequency

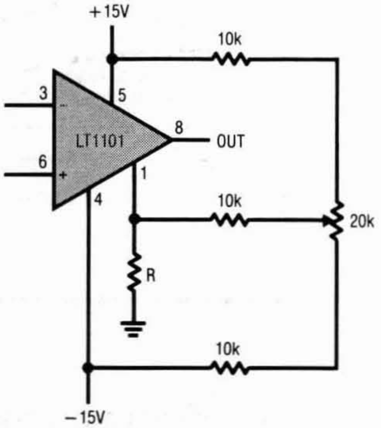
The common-mode rejection ratio (CMRR) of the LT1101 starts to roll off at a relatively low frequency. However, as shown on the CMRR vs Frequency plot, CMRR can be enhanced significantly by connecting an 82pF capacitor between pins 1 and 2. This improvement is only available in the gain 100 configuration, and it is in excess of 30dB at 60Hz.

Offset Nulling

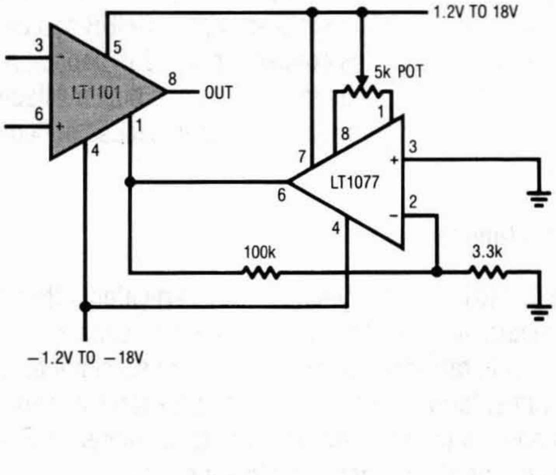
The LT1101 is not equipped with dedicated offset null terminals. In many bridge transducer or sensor applications, calibrating the bridge simultaneously eliminates the instrumentation amplifier's offset as a source of error. For example, in the Micropower Remote Temperature Sensor Application shown, one adjustment removes the offset errors due to the temperature sensor, voltage reference and the LT1101.

APPLICATIONS INFORMATION

A simple resistive offset adjust procedure is shown below. If R = 5Ω for G = 10, and R = 50Ω for G = 100 then the effect of R on gain error is approximately 0.006%. Unfortunately, about 450μA has to flow through R to bias the reference terminal (pin 1) and to null out the worst-case offset voltage. The total current through the resistor network can exceed 1mA, and the micropower advantage of the LT1101 is lost.



Another offset adjust scheme uses the LT1077 micropower op amp to drive the reference pin 1. Gain error and common-mode rejection are unaffected, the total current increase is 45μA. The offset of the LT1077 is trimmed and amplified to match and cancel the offset voltage of the LT1101. Output offset null range is ±25mV.



Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors (= R_X) between pins 1 and 2 and pins 7 and 8.

$$\text{Gain} = 10 + \frac{R_X}{R + R_X/90}$$

The nominal value of R is 9.2kΩ. The usefulness of this method is limited by the fact that R is not controlled to better than ±10% absolute accuracy in production. However, on any specific unit 90R can be measured between pins 1 and 2.

Input Protection

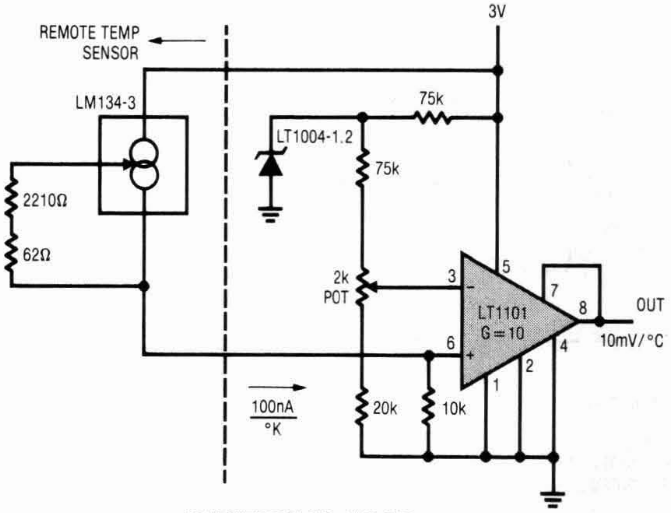
Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1101 employs PNP input transistors, consequently the differential input voltage can be ±30V (with ±15V supplies, ±36V with ±18V supplies) without an increase in input bias current. Competitive instrumentation amplifiers have NPN inputs which are protected by back to back diodes. When the differential input voltage exceeds ±1.3V on these competitive devices, input current increases to the milliampere level; more than ±10V differential voltage can cause permanent damage.

When the LT1101's inputs are pulled above the positive supply, the inputs will clamp a diode voltage above the positive supply. No damage will occur if the input current is limited to 20mA.

500Ω resistors in series with the inputs protect the LT1101 when the inputs are pulled as much as 10V below the negative supply.

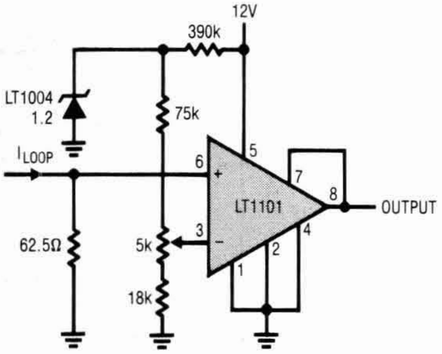
APPLICATIONS INFORMATION

Micropower, Battery Operated, Remote Temperature Sensor


3V
REMOTE TEMP SENSOR
LM134-3
75k
LT1004-1.2
75k
2210Ω
62Ω
2k POT
3
5
7
8
OUT
LT1101 G = 10
6
4
10mV/°C
2
1
100nA / °K
20k
10k

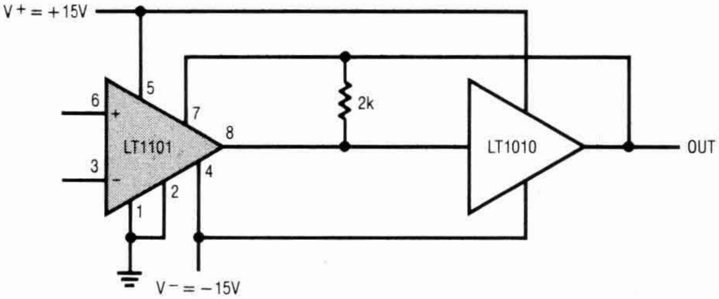
TRIM OUTPUT TO 250mV AT 25°C
TEMPERATURE RANGE = 2.5°C TO 150°C
ACCURACY = ±0.5°C

4mA to 20mA Loop Receiver


12V
390k
LT1004 1.2
75k
I_{LOOP}
6
5
7
8
LT1101
OUTPUT
62.5Ω
5k
3
4
2
1
18k

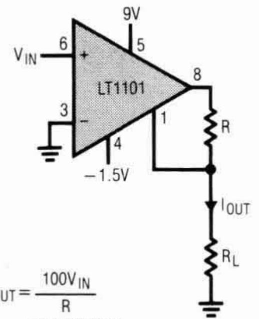
4mA TO 20mA IN → 0V TO 10V OUT
TRIM OUTPUT TO 5V AT 12mA IN

Instrumentation Amplifier with ±150mA Output Current


V+ = +15V
6
5
7
8
LT1101
3
4
2
1
2k
LT1010
OUT
V− = −15V

GAIN = 10, DEGRADED BY 0.01% DUE TO LT1010
OUTPUT = ±10V INTO 75Ω (TO 1.5kHz)
DRIVES ANY CAPACITIVE LOAD
SINGLE SUPPLY APPLICATION (V+ = 5V, V− = 0V):
$V_{OUT\ MIN} = 120mV$, $V_{OUT\ MAX} = 3.4V$

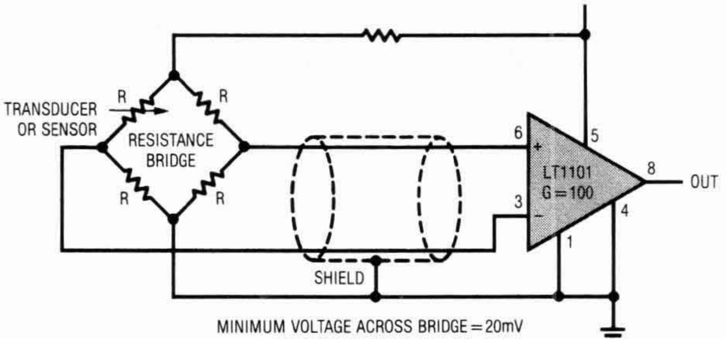
Voltage Controlled Current Source


9V
V_{IN}
6
5
8
LT1101
3
1
R
4
−1.5V
I_{OUT}
R_L

$$I_{OUT} = \frac{100V_{IN}}{R}$$

$I_{OUT} = 0mA$ TO 5mA
VOLTAGE COMPLIANCE = 6.4V
(R ≤ 200Ω)

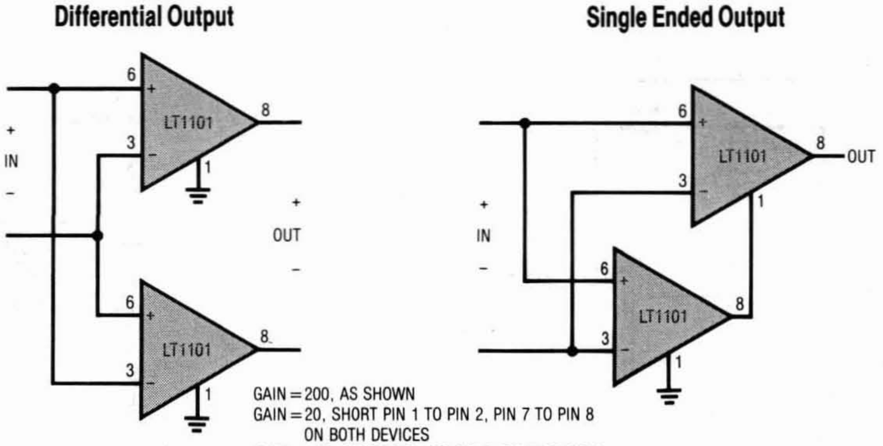
Differential Voltage Amplification from a Resistance Bridge


V+
TRANSDUCER OR SENSOR
R
R
RESISTANCE BRIDGE
R
R
6
5
LT1101 G = 100
8
OUT
3
4
1
SHIELD

MINIMUM VOLTAGE ACROSS BRIDGE = 20mV
MINIMUM SUPPLY VOLTAGE = 1.8V

APPLICATIONS INFORMATION

Gain = 20, 110 or 200 Instrumentation Amplifiers



Differential Output

Single Ended Output

6
3
8
1
LT1101
+
IN
–
+
OUT
–
6
3
8
1
LT1101
6
3
8
1
LT1101
OUT
+
IN
–
6
3
8
1
LT1101

GAIN = 200, AS SHOWN
GAIN = 20, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8
ON BOTH DEVICES
GAIN = 110, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8
ON ONE DEVICE, NOT ON THE OTHER
INPUT REFERRED NOISE IS REDUCED BY $\sqrt{2}$ (G = 200 OR 20)

High Speed, Precision, JFET Input Instrumentation Amplifier (Fixed Gain = 10 or 100)

FEATURES

■ Slew Rate	30V/µs
■ Gain-Bandwidth Product	35MHz
■ Settling Time (0.01%)	3µs
■ Overdrive Recovery	0.4µs
■ Gain Error	0.05% Max
■ Gain Drift	5ppm/°C
■ Gain Non-Linearity	16ppm Max
■ Offset Voltage (Input + Output)	600µV Max
– Drift with Temperature	2.5µV/°C
■ Input Bias Current	40pA Max
■ Input Offset Current	40pA Max
– Drift with Temperature (to 70°C)	0.5pA/°C

APPLICATIONS

- Fast Settling Analog Signal Processing
- Multiplexed Input Data Acquisition Systems
- High Source Impedance Signal Amplification from High Resistance Bridges, Capacitance Sensors, Photodetector Sensors
- Bridge Amplifier with <1Hz Lowpass Filtering

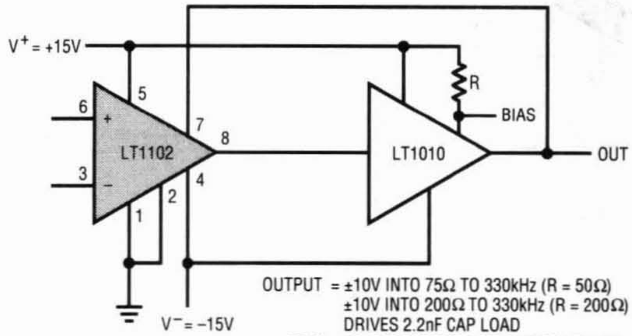
DESCRIPTION

The LT1102 is the first fast FET input instrumentation amplifier offered in the low cost, space saving 8-pin packages. Fixed gains of 10 and 100 are provided with excellent gain accuracy (0.01%) and non-linearity (3ppm). No external gain setting resistor is required.

Slew rate, settling time, gain-bandwidth product, overdrive recovery time are all improved compared to competitive high speed instrumentation amplifiers.

Industry best speed performance is combined with impressive precision specifications: less than 10pA input bias and offset currents, 200µV offset voltage. Unlike other FET input instrumentation amplifiers, on the LT1102 there is no output offset voltage contribution to total error, and input bias currents do not double with every 10°C rise in temperature. Indeed, at 70°C ambient temperature the input bias current is only 50pA.

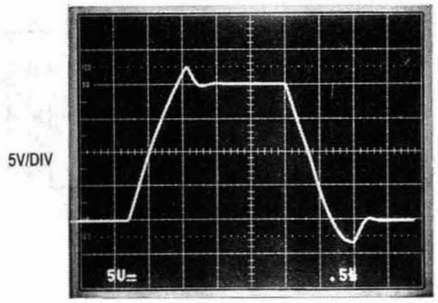
Wideband Instrumentation Amplifier with ±150mA Output Current



OUTPUT = ±10V INTO 75Ω TO 330kHz (R = 50Ω)
±10V INTO 200Ω TO 330kHz (R = 200Ω)
DRIVES 2.2nF CAP LOAD
GAIN = 10, DEGRADED 0.01% DUE TO LT1010

LT1102 • TA01

Slew Rate

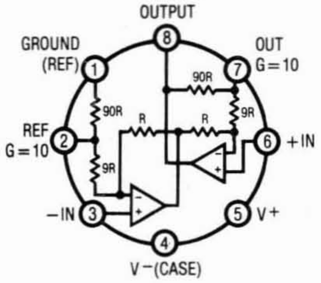
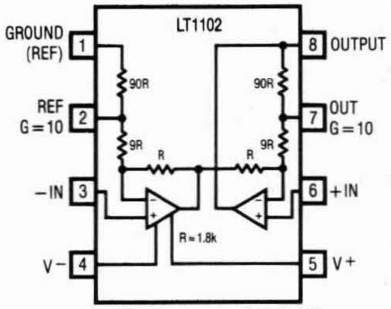


G = 10 0.5µs/DIV

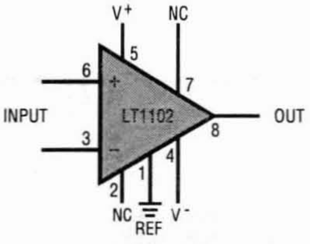
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 20V
Differential Input Voltage	± 40V
Input Voltage	± 20V
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1102AM/LT1102M	– 55°C to 125°C
LT1102I	– 40°C to 85°C
LT1102AC/LT1102C	0°C to 70°C
Storage Temperature Range	
All Grades	– 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

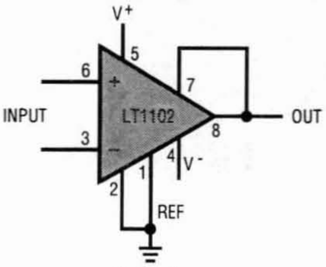
PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
TOP VIEW  H PACKAGE 8-LEAD TO-5 METAL CAN	LT1102AMH LT1102MH LT1102ACH LT1102CH
TOP VIEW  J PACKAGE 8-LEAD CERAMIC DIP N PACKAGE 8-LEAD PLASTIC DIP	LT1102IN8 LT1102ACN8 LT1102CN8 LT1102MJ8 LT1102CJ8

Basic Connections

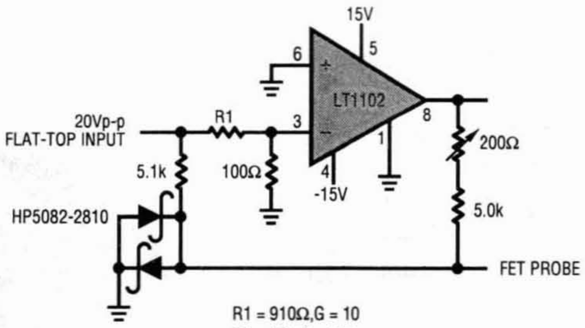

V+
NC
5
7
6
INPUT
3
LT1102
8
OUT
1
4
2
NC
REF
V-

GAIN = 100


V+
5
7
6
INPUT
3
LT1102
8
OUT
4
V-
1
2
REF

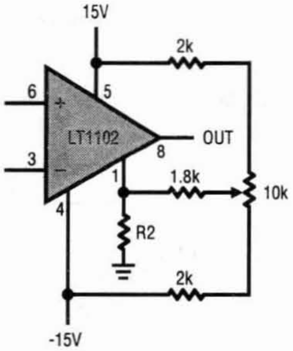
GAIN = 10

Settling Time Test Circuit


15V
6
5
LT1102
8
3
1
4
-15V
20Vp-p
FLAT-TOP INPUT
R1
5.1k
100Ω
200Ω
5.0k
HP5082-2810
FET PROBE

R1 = 910Ω, G = 10
R1 = 10k, G = 100

Offset Nulling


15V
2k
6
5
LT1102
OUT
3
8
1
1.8k
10k
4
R2
2k
-15V

R2 = 3.3Ω, G = 10
R2 = 30Ω, G = 100
NULL RANGE = ±1mV
GAIN DEGRADATION ≈ 0.018%

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, $T_A = 25°C$, Gain = 10 or 100, unless otherwise noted.

			LT1102AM/AC			LT1102M/I/C			
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
G_E	Gain Error	$V_O = \pm 10V$, $R_L = 50k$ or 2k		0.010	0.050		0.012	0.070	%
G_{NL}	Gain Non-Linearity	$G = 100$, $R_L = 50k$		3	14		4	18	ppm
		$G = 100$, $R_L = 2k$		8	20		8	25	ppm
		$G = 10$, $R_L = 50k$ or 2k		7	16		7	30	ppm
V_{OS}	Input Offset Voltage			180	600		200	900	μV
I_{OS}	Input Offset Current			3	40		4	60	pA
I_B	Input Bias Current			±3	±40		±4	±60	pA
	Input Resistance Common-Mode	$V_{CM} = -11V$ to 8V		10^{12}			10^{12}		Ω
		$V_{CM} = 8V$ to 11V		10^{11}			10^{11}		Ω
	Differential Mode			10^{12}			10^{12}		Ω
e_n	Input Noise Voltage	0.1Hz to 10Hz		2.8			2.8		μVp-p
	Input Noise Voltage Density	$f_o = 10Hz$		37			37		nV/√Hz
		$f_o = 1000Hz$ (Note 1)		19	30		20		nV/√Hz
	Input Noise Current Density	$f_o = 1000Hz$, 10Hz (Note 2)		1.5	4		2	5	fA/√Hz
	Input Voltage Range		±10.5	±11.5		±10.5	±11.5		V
CMRR	Common-Mode Rejection Ratio	1k Source Imbalance, $V_{CM} = \pm 10.5V$	84	98		82	97		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 9V$ to $\pm 18V$	88	102		86	101		dB
I_S	Supply Current			3.3	5.0		3.4	5.6	mA
V_O	Maximum Output Voltage Swing	$R_L = 50k$	±13.0	±13.5		±13.0	±13.5		V
		$R_L = 2k$	±12.0	±13.0		±12.0	±13.0		V
BW	Bandwidth	G = 100 (Note 3)	120	220		100	220		kHz
		G = 10 (Note 3)	2.0	3.5		1.7	3.5		MHz
SR	Slew Rate	$G = 100$, $V_{IN} = \pm 0.13V$, $V_O = \pm 5V$	12	17		10	17		V/μs
		$G = 10$, $V_{IN} = \pm 1V$, $V_O = \pm 5V$	21	30		18	30		V/μs
	Overdrive Recovery	50% Overdrive (Note 4)		400			400		ns
	Settling Time	$V_O = 20V$ Step (Note 3)							
		G = 10 to 0.05%		1.8	4.0		1.8	4.0	μs
		G = 10 to 0.01%		3.0	6.5		3.0	6.5	μs
		G = 100 to 0.05%		7	13		7	13	μs
		G = 100 to 0.01%		9	18		9	18	μs

Note 1: This parameter is tested on a sample basis only.

Note 2: Current noise is calculated from the formula:
$i_n = (2qI_b)^{1/2}$
where $q = 1.6 \times 10^{-19}$ coulomb. The noise of source resistors up to 1GΩ swamps the contribution of current noise.

Note 3: This parameter is not tested. It is guaranteed by design and by inference from the slew rate measurement.

Note 4: Overdrive recovery is defined as the time delay from the removal of an input overdrive to the output's return from saturation to linear operation. 50% overdrive equals $V_{IN} = \pm 2V$ (G = 10) or $V_{IN} = \pm 200mV$ (G = 100).

Note 5: This parameter is not tested. It is guaranteed by design and by inference from other tests.

ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $-55°C \le T_A \le 125°C$ for AM/M grades, $-40°C \le T_A \le 85°C$ for I grades, unless otherwise noted.

				LT1102AM			LT1102M/I		
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
G_E	Gain Error	$G = 100, V_O = \pm 10V, R_L = 50k$ or 2k		0.10	0.25		0.10	0.30	%
		$G = 10, V_O = \pm 10V, R_L = 50k$ or 2k		0.05	0.12		0.06	0.15	%
TCG_E	Gain Error Drift (Note 5)	$G = 100, R_L = 50k$ or 2k		9	20		10	25	ppm/°C
		$G = 10, R_L = 50k$ or 2k		5	10		6	14	ppm/°C
G_{NL}	Gain Non-Linearity	$G = 100, R_L = 50k$		20	70		24	90	ppm
		$G = 100, R_L = 2k$		28	85		32	110	ppm
		$G = 10, R_L = 50k$ or 2k		9	20		9	24	ppm
V_{OS}	Input Offset Voltage			300	1400		400	2000	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)		2	8		3	12	μV/°C
I_{OS}	Input Offset Current			0.3	4		0.4	6	nA
I_B	Input Bias Current			±2	±10		±2.5	±15	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	82	97		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	86	100		84	99		dB
I_S	Supply Current	$T_A = 125°C$		2.5			2.5		mA
V_O	Maximum Output Voltage Swing	$R_L = 50k$	±12.5	±13.2		±12.5	±13.2		V
		$R_L = 2k$	±12.0	±12.6		±12.0	±12.6		V

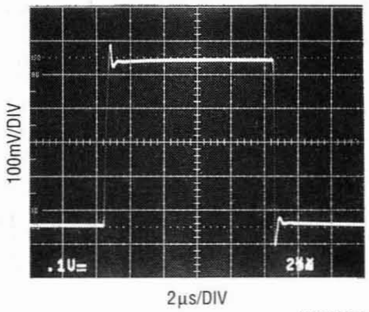
ELECTRICAL CHARACTERISTICS

$V_S = \pm 15V$, $V_{CM} = 0V$, Gain = 10 or 100, $0°C \le T_A \le 70°C$, unless otherwise noted.

				LT1102AC			LT1102C		
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
G_E	Gain Error	$G = 100, V_O = \pm 10V, R_L = 50k$ or 2k		0.04	0.11		0.05	0.14	%
		$G = 10, V_O = \pm 10V, R_L = 50k$ or 2k		0.03	0.09		0.04	0.12	%
TCG_E	Gain Error Drift (Note 5)	$G = 100, R_L = 50k$ or 2k		8	18		9	22	ppm/°C
		$G = 10, R_L = 50k$ or 2k		5	10		6	14	ppm/°C
G_{NL}	Gain Non-Linearity	$G = 100, R_L = 50k$		8	30		9	40	ppm
		$G = 100, R_L = 2k$		11	36		12	48	ppm
		$G = 10, R_L = 50k$ or 2k		8	18		8	22	ppm
V_{OS}	Input Offset Voltage			230	1000		280	1400	μV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	(Note 5)		2	8		3	12	μV/°C
I_{OS}	Input Offset Current			10	150		15	220	pA
$\Delta I_{OS}/\Delta T$	Input Offset Current Drift	(Note 5)		0.5	3		0.5	4	pA/°C
I_B	Input Bias Current			±40	±300		±50	±400	pA
$\Delta I_B/\Delta T$	Input Bias Current Drift	(Note 5)		1	4		1	6	pA/°C
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 10.3V$	83	98		81	97		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	87	101		85	100		dB
I_S	Supply Current	$T_A = 70°C$		2.8			2.9		mA
V_O	Maximum Output Voltage Swing	$R_L = 50k$	±12.8	±13.4		±12.8	±13.4		V
		$R_L = 2k$	±12.0	±12.8		±12.0	±12.8		V

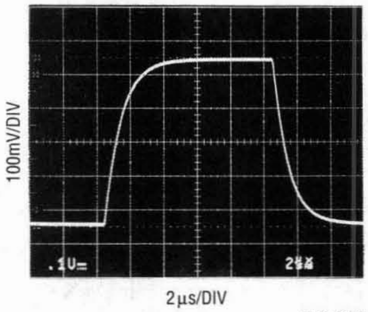
TYPICAL PERFORMANCE CHARACTERISTICS

Small Signal Response, G = 10 (Input = 50mV Pulse)



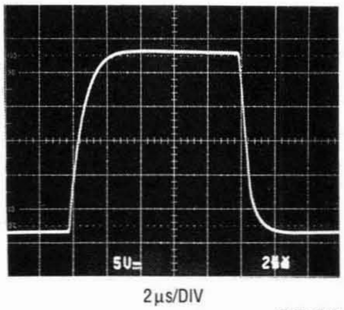
LT1102 • TPC01

Small Signal Response, G = 100 (Input = 5mV Pulse)



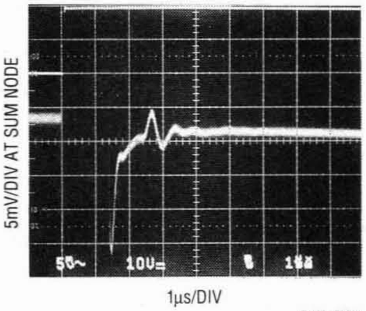
LT1102 • TPC02

Slew Rate, G = 100 (Input = ±130mV Pulse)



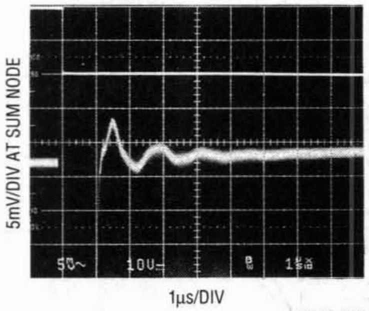
LT1102 • TPC03

Settling Time, G = 10 (Input From –10V to +10V)



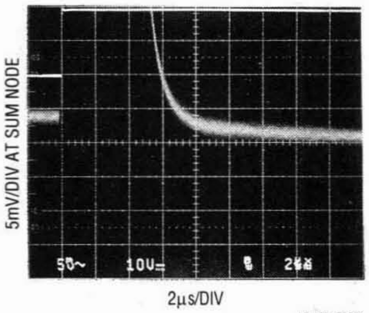
LT1102 • TPC04

Settling Time, G = 10 (Input From +10V to –10V)



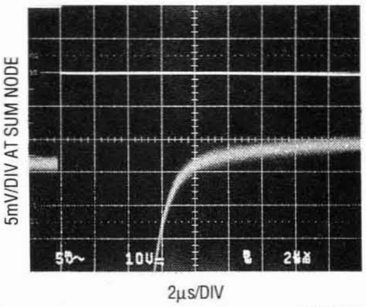
LT1102 • TPC05

Settling Time, G = 100 (Input From –10V to +10V)



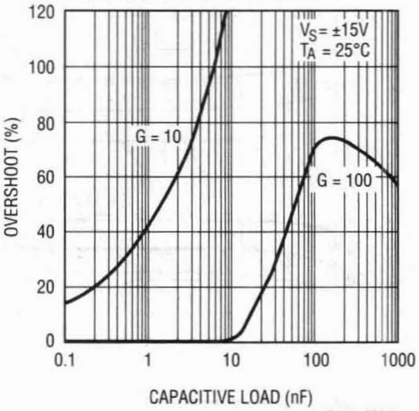
LT1102 • TPC06

Settling Time, G = 100 (Input From +10V to –10V)



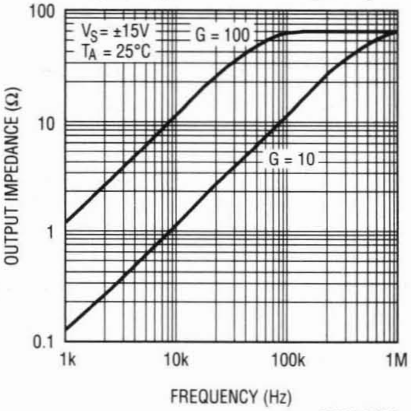
LT1102 • TPC07

Capacitive Load Handling



LT1102 • TPC08

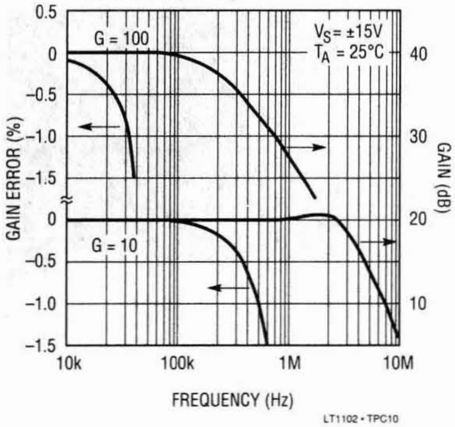
Output Impedance vs Frequency



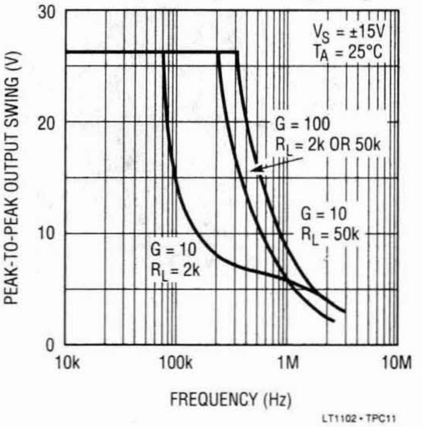
LT1102 • TPC09

TYPICAL PERFORMANCE CHARACTERISTICS

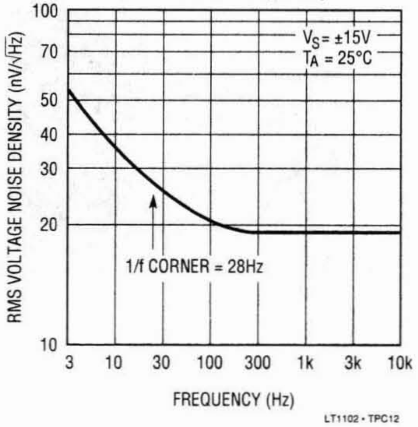
Gain vs Frequency



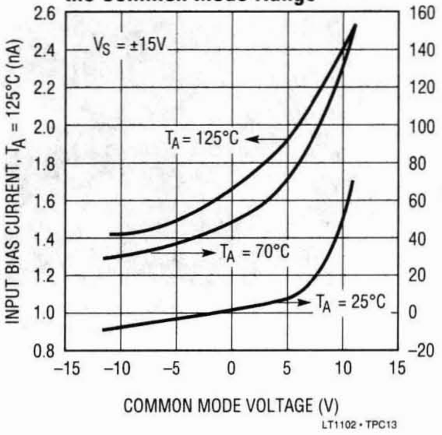
Undistorted Output vs Frequency



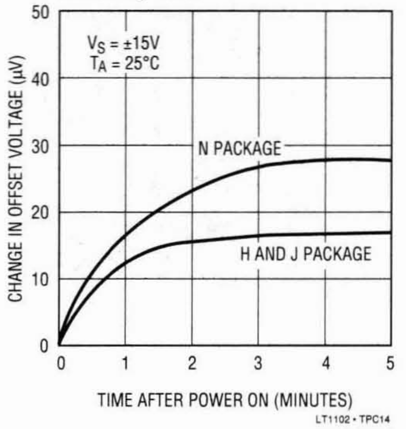
Voltage Noise vs Frequency



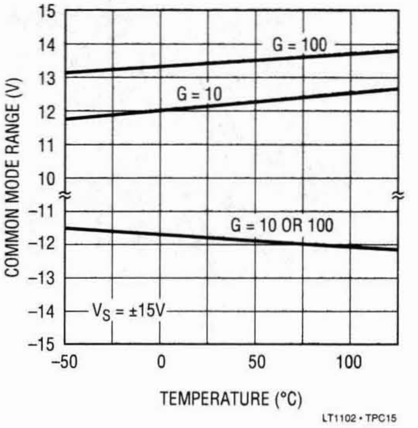
Input Bias Current Over the Common Mode Range



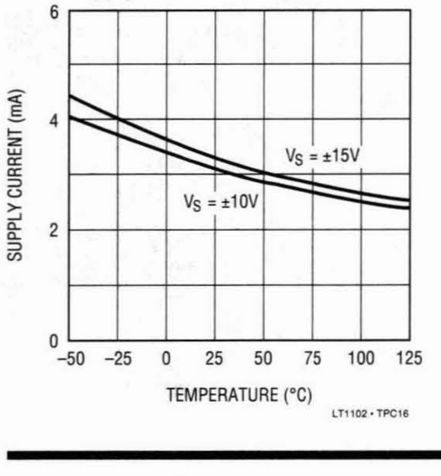
Warm-Up Drift



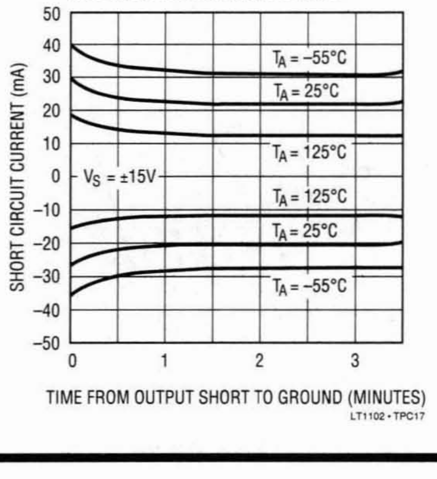
Common Mode Range vs Temperature



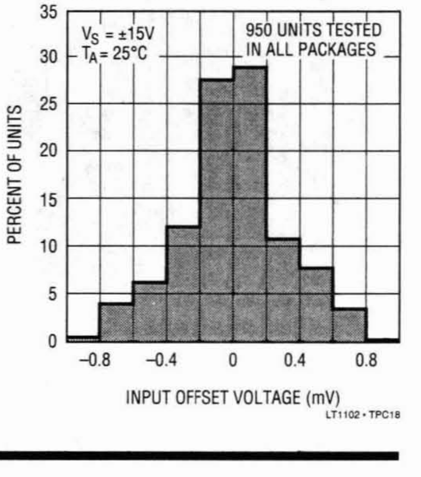
Supply Current vs Temperature



Short Circuit Current vs Time

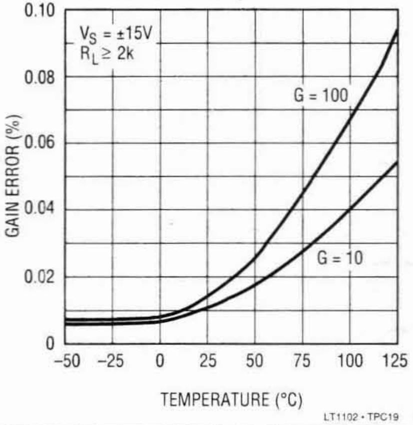


Distribution of Offset Voltage

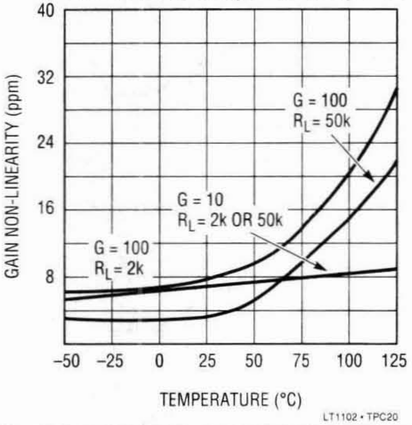


TYPICAL PERFORMANCE CHARACTERISTICS

Gain Error vs Temperature



Gain Non-Linearity Over Temperature



APPLICATIONS INFORMATION

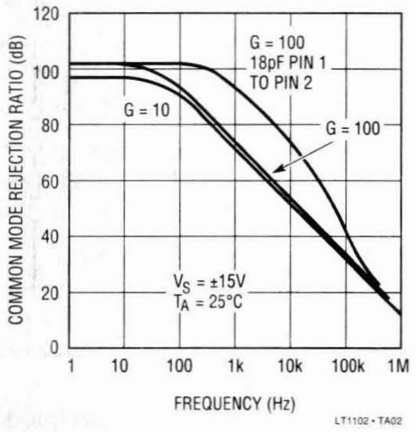
In the two op amp instrumentation amplifier configuration, the first amplifier is basically in unity gain, and the second amplifier provides all the voltage gain. In the LT1102 the second amplifier is decompensated for gain of 10 stability, therefore high slew rate and bandwidth are achieved. Common mode rejection versus frequency is also optimized in the G = 10 mode, because the bandwidths of the two op amps are similar. When G = 100 this statement is no longer true. However, by connecting an 18pF capacitor between pins 1 and 2, a common mode AC gain is created to cancel the inherent roll-off. From 200Hz to 30kHz CMRR versus frequency is improved by an order of magnitude.

Input Protection

Instrumentation amplifiers are often used in harsh environments where overload conditions can occur. The LT1102 employs FET input transistors, consequently the differential input voltage can be ±30V (with ±15V supplies, ±36V with ±18V supplies) Some competitive instrumentation amplifiers have NPN inputs which are protected by back to back diodes. When the differential input voltage exceeds ±1.3V on these competitive devices, input current increases to milliampere level; more than ±10V differential voltage can cause permanent damage.

When the LT1102 inputs are pulled below the negative supply or above the positive supply, the inputs will clamp a diode voltage below or above the supplies. No damage will occur if the input current is limited to 20mA.

Common Mode Rejection Ratio vs Frequency



Gains Between 10 and 100

Gains between 10 and 100 can be achieved by connecting two equal resistors (=R_X) between pins 1 and 2 and pins 7 and 8.

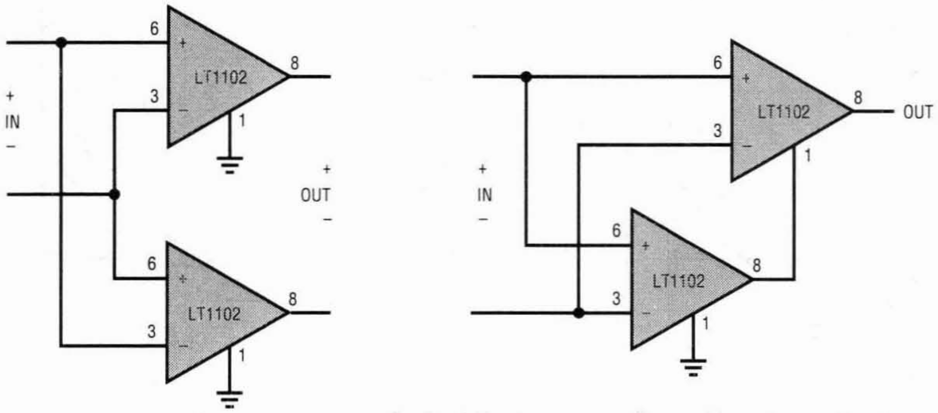
$$\text{Gain} = 10 + \frac{R_X}{R + R_X/90}$$

The nominal value of R is 1.84kΩ. The usefulness of this method is limited by the fact that R is not controlled to better than ±10% absolute accuracy is production. However, on any specific unit 90R can be measured between pins 1 and 2.

APPLICATIONS INFORMATION

Gain = 20, 110, or 200 Instrumentation Amplifiers

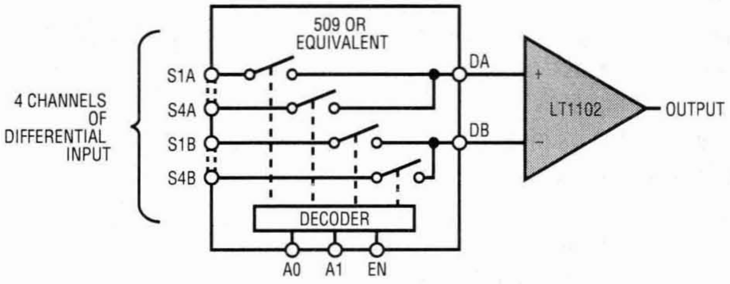
Differential Output **Single Ended Output**


6
3
8
1
LT1102
+
IN
–
+
OUT
–
6
3
8
1
LT1102
6
3
8
1
LT1102
OUT
+
IN
–
6
3
8
1
LT1102

GAIN = 200, AS SHOWN
GAIN = 20, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON BOTH DEVICES
GAIN = 110, SHORT PIN 1 TO PIN 2, PIN 7 TO PIN 8 ON ONE DEVICE, NOT ON THE OTHER
INPUT REFERRED NOISE IS REDUCED BY $\sqrt{2}$ (G = 200 OR 20)

LT1102 • TA03

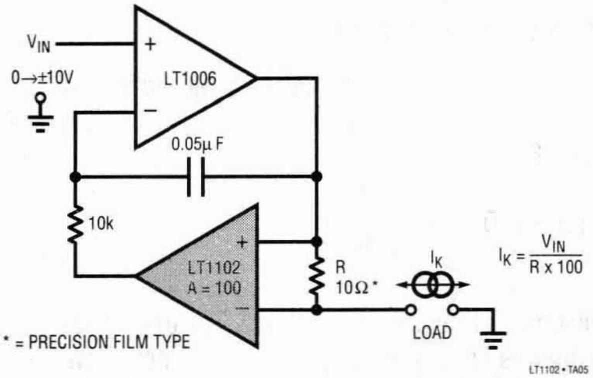
Multiplexed Input Data Acquisition


509 OR
EQUIVALENT
4 CHANNELS
OF
DIFFERENTIAL
INPUT
S1A
S4A
S1B
S4B
DA
DB
LT1102
OUTPUT
DECODER
A0
A1
EN

800kHz SIGNALS CAN BE MULTIPLEXED WITH LT1102 IN G = 10

LT1102 • TA04

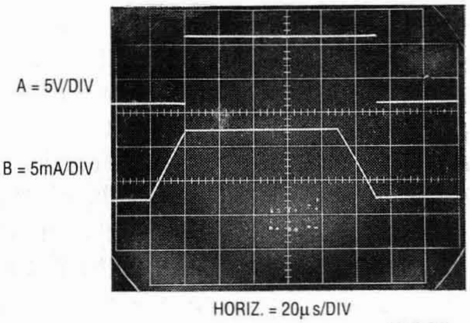
Voltage Programmable Current Source is Simple and Precise


V_{IN}
0→±10V
LT1006
0.05μF
10k
LT1102
A = 100
R
10Ω*
I_K
$I_K = \frac{V_{IN}}{R \times 100}$
LOAD

* = PRECISION FILM TYPE

LT1102 • TA05

Dynamic Response of the Current Source



LT1102 • TA06

SECTION 4—POWER PRODUCTS

SECTION 4—POWER PRODUCTS

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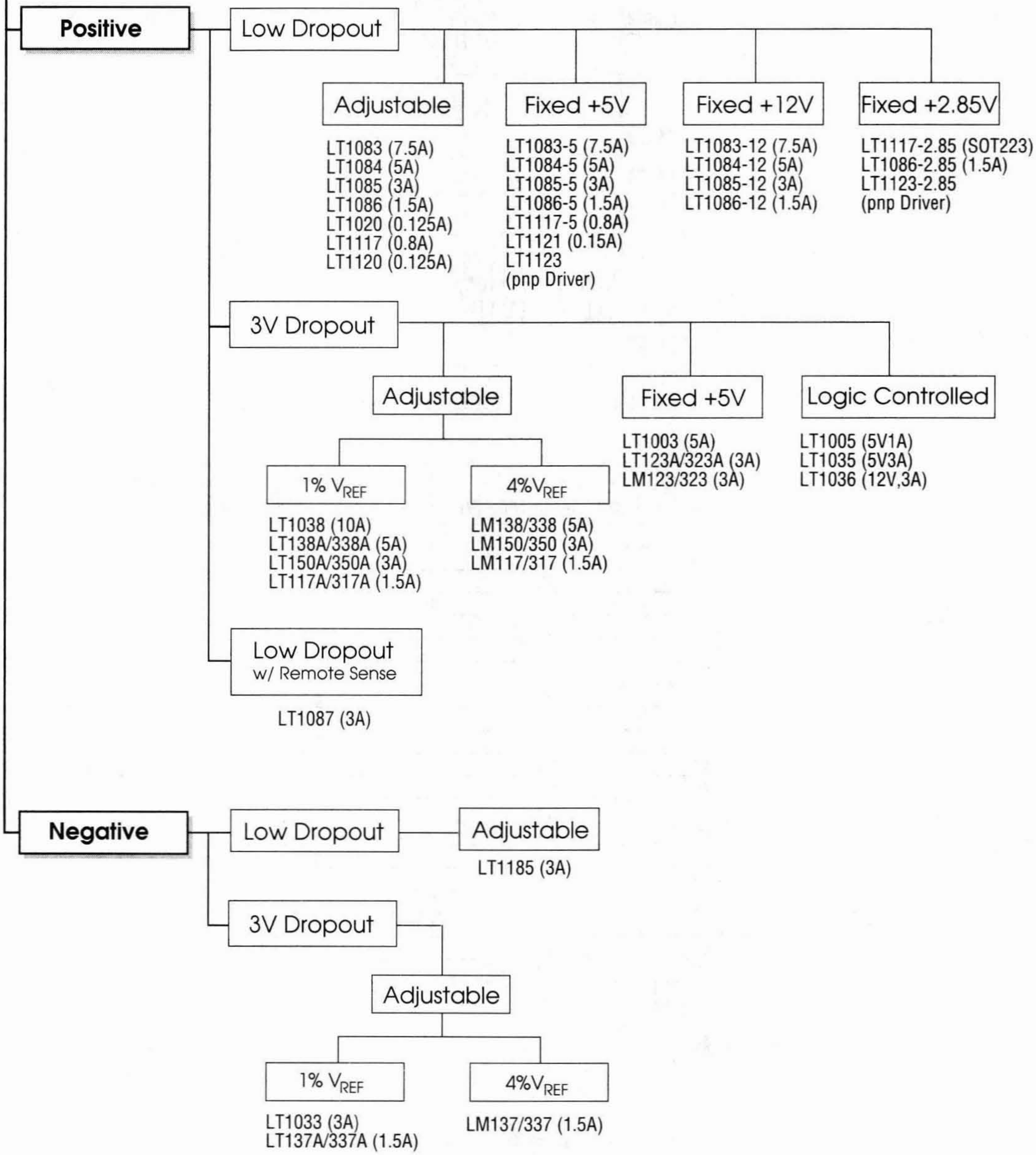
LINEAR REGULATORS



- **Positive**
  - Low Dropout
    - Adjustable
      - LT1083 (7.5A)
      - LT1084 (5A)
      - LT1085 (3A)
      - LT1086 (1.5A)
      - LT1020 (0.125A)
      - LT1117 (0.8A)
      - LT1120 (0.125A)
    - Fixed +5V
      - LT1083-5 (7.5A)
      - LT1084-5 (5A)
      - LT1085-5 (3A)
      - LT1086-5 (1.5A)
      - LT1117-5 (0.8A)
      - LT1121 (0.15A)
      - LT1123 (pnp Driver)
    - Fixed +12V
      - LT1083-12 (7.5A)
      - LT1084-12 (5A)
      - LT1085-12 (3A)
      - LT1086-12 (1.5A)
    - Fixed +2.85V
      - LT1117-2.85 (SOT223)
      - LT1086-2.85 (1.5A)
      - LT1123-2.85 (pnp Driver)
  - 3V Dropout
    - Adjustable
      - 1% V_{REF}
        - LT1038 (10A)
        - LT138A/338A (5A)
        - LT150A/350A (3A)
        - LT117A/317A (1.5A)
      - 4%V_{REF}
        - LM138/338 (5A)
        - LM150/350 (3A)
        - LM117/317 (1.5A)
    - Fixed +5V
      - LT1003 (5A)
      - LT123A/323A (3A)
      - LM123/323 (3A)
    - Logic Controlled
      - LT1005 (5V1A)
      - LT1035 (5V3A)
      - LT1036 (12V,3A)
  - Low Dropout w/ Remote Sense
    - LT1087 (3A)
- **Negative**
  - Low Dropout
    - Adjustable
      - LT1185 (3A)
  - 3V Dropout
    - Adjustable
      - 1% V_{REF}
        - LT1033 (3A)
        - LT137A/337A (1.5A)
      - 4%V_{REF}
        - LM137/337 (1.5A)

4

SWITCHING REGULATOR SELECTION GUIDE

		OPTIMIZED FOR STEP-UP OR FLYBACK CONFIGURATIONS			BOTH		OPTIMIZED FOR STEP-DOWN OR INVERTING APPLICATIONS	OFFLINE AND/OR PWM CONTROLLERS		
	OSCILLATOR FREQUENCY →	40kHz	60kHz	100kHz	20kHz	60kHz	100kHz	200kHz	500kHz	1MHz
SWITCH CURRENT	10A		LT1270A							
	8A		LT1270							
	5A	LT1070		LT1170			LT1074			
	2.5A	LT1071		LT1171						
	2A						LT1076**	LT1103		
	1.25A	LT1072		LT1172						
	1A		LT1082		LT1073* LT1173* (MICROPOWER)	LT1110* LT1111* (MICROPOWER)				
	0.5A			LT1109 (MICROPOWER)						
	EXTERNAL							LT1105	LT124x	LT1246

	INPUT VOLTAGE (V) MIN	INPUT VOLTAGE (V) MAX	MAXIMUM SWITCH VOLTAGE (V)	MAX RATED SWITCH CURRENT (A)	PACKAGES AVAILABLE
LT1070	3	40	65	5	K, T
LT1070HV	3	60	75	5	K, T
LT1071	3	40	65	2.5	K, T
LT1071HV	3	60	75	2.5	K, T
LT1072	3	40	65	1.25	K, T, N8, S8, S16
LT1072HV	3	60	75	1.25	K, T
LT1073*	1	36	50	1	N8, S8
LT1074	3	40	65	5	K, Q,T, V
LT1074HV	3	60	75	5	K, T, V
LT1076**	3	40	65	2	K, R, T, V, Y
LT1076HV	3	60	75	2	K, R, T, V, Y
LT1082	3	75	100	1	J8, N8, S, T
LT1109*	2	36	50	0.5	N8, S8, Z
LT1110*	1	15	40	1	N8, S8
LT1111*	2	36	50	1	N8, S8
LT1170	3	40	65	5	K, T
LT1170HV	3	60	75	5	K, T
LT1171	3	40	65	2.5	K, Q, T
LT1171HV	3	60	75	2.5	K, T
LT1172	3	40	65	1.25	K, T, N8, S8, S16
LT1172HV	3	60	75	1.25	K, T
LT1173*	2	36	30	1	N8, S8
LT1270A	3	30	60	10	T
LT1270	3	30	60	8	T
LT1271	3	30	60	4	T, Q

*** Fixed +5V and +12V output versions available**
**** Fixed +5V version available**

MILITARY

I_O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT*	PART NUMBER	PACKAGE TYPE	V_{IN}/ V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURE/COMMENTS
10.0	Pos Adj	LT1038MK	Steel TO-3	35	1.2 to 33	0.8% V_{OUT} Tol, Plug in Compatible with 117, 150, 138 Types
7.5	Pos Fixed	LT1083MK-5	Steel TO-3	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1083MK-12	Steel TO-3	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT1083MK	Steel TO-3	35	1.2 to 34	Low Dropout (1.2V), 1% V_{REF} Tol, Pin Compatible with 117, 150, 138 Types
5.0	Pos Fixed	LT1084MK-5	Steel TO-3	30	5	Low Dropout (1.2V), 1%V_{OUT} Tol
		LT1084MK-12	Steel TO-3	30	12	Low Dropout (1.2V), 1%V_{OUT} Tol
		LT1003MK	Steel TO-3	20	5	2% V_{OUT} Tol
	Pos Adj	LT 138AK LM138K	Steel TO-3	35	1.2 to 32	LT138A Has 1% V_{REF} Tol
		LT1084MK	Steel TO-3	35	1.2 to 34	Low Dropout (1.2V), 1% V_{REF} Tol, Pin Compatible with 117, 150, 138 Types
	Switching	LT1070MK	Steel TO-3	40	*	Self Contained 40kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1070HVMK	Steel TO-3	60	*	Self Contained 40kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1074MK	Steel TO-3	45	*	Self-Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1074HVMK	Steel TO-3	64	*	Self-Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1170MK	Steel TO-3	40	*	Self Contained 100kHz PWM and 5 Amp Switch in a 5-Pin package
3.0	Pos Fixed	LT1085MK-5	Steel TO-3	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1085MK-12	Steel TO-3	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT123AK LM123K	Steel TO-3	20	5	LT123A Has 1% V_{OUT} Tol
	Pos Adj	LT150AK LM150K	Steel TO-3	35	1.2 to 33	LT150A Has 1% V_{REF} Tol
		LT1085MK	Steel TO-3	35	1.2 to 34	Low Dropout (1.2V), 1% V_{REF} Tol, Pin Compatible with 117, 150 Types
	Neg Adj	LT1033MK	Steel TO-3	35	−1.2 to −32	2% V_{REF} Tol
	Dual Pos Fixed	LT1035MK	Steel TO-3	20	Two 5V Outputs	Logic Controlled Main Output Voltage, 75mA
	Positive	LT1036MK	Steel TO-3	30	12, 5	Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output
2.5	Switching	LT1071MK	Steel TO-3	40	*	Self Contained 40kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1071HVMK	Steel TO-3	60	*	Self Contained 40kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1171MK	Steel TO-3	40	*	Self Contained 100kHz PWM and 2.5 Amp Switch in a 5-Pin Package
2.0	Switching	LT1076MK	Steel TO-3	45	*	Self Contained 100kHz PWM and 2.0 Amp Switch in a 5-Pin Package
		LT1076HVMK	Steel TO-3	64	*	Self Contained 100kHz PWM and 2.0 Amp Switch in a 5-Pin Package
1.5	Pos Fixed	LM1086MK-5	Steel TO-3	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1086MK-12	Steel TO-3	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT1086MK	Steel TO-3	30	1.2 to 29	Low Dropout (1.2V), 1% V_{REF} Tol, Pin Compatible with 117 Types
0.5 to 1.5	Pos Adj	LT117AK LM117K	Steel TO-3	40	1.2 to 37	LT117A Has 1% V_{REF} Tol
		LT117AH LM117H	TO-39	40		
		LT1086MH	TO-39	30	1.2 to 29	Low Dropout (1.2V), 1% V_{REF} Tol, Pin Compatible with 117 Types
	Neg Adj	LT137AK LM137K	Steel TO-3	40	−1.2 to −37	LT137A Has 1% V_{REF} Tol
		LT137AH LM137H	TO-39	40		
	Pos Adj High Voltage	LT117AHVK LM117HVK	Steel TO-3	60	1.2 to 57	LT117AHV Has 1% V_{REF} Tol
		LT117AHVH LM117HVH	TO-39	60		
	Neg Adj High Voltage	LT137AHVK LM137HVK	Steel TO-3	50	−1.2 to −47	LT137AHV Has 1% V_{REF} Tol
		LT137AHVH LM137HVH	TO-39	50		
1.25	Switching	LT1072MJ8	CERDIP	40	*	Self Contained 40kHz PWM and 1.25 Amp Switch
		LT1072MK	Steel TO-3	40	*	Self Contained 40kHz PWM and 1.25 Amp Switch
		LT1072HVMK	Steel TO-3	60	*	Self Contained 40kHz PWM and 1.25 Amp Switch
		LT1172MJ8	CERDIP	40	*	Self Contained 100kHz PWM and 1.25 Amp Switch
		LT1172MK	Steel TO-3	40	*	Self Contained 100kHz PWM and 1.25 Amp Switch
1.0	Dual Pos Fixed	LT1005MK	Steel TO-3	20	Two 5V Outputs	Logic Controlled 1 Amp Main Output Voltage, 35mA Auxiliary Output
125mA	Positive	LT1020MJ	14-Pin CERDIP	36	4 to 30	Dropout Voltage = 0.5V, 40μAI_Q, Reference and Comparator
		LT1120MJ8	8-Pin CERDIP	36	4 to 30	Dropout Voltage = 0.5V, 40μAI_Q, Reference and Comparator
40mA to 100mA	Switched Capacitor	LT1026MJ8	CERDIP	10	**	Voltage Converter, 10mA Output
		LT1026MH	TO-5 Can	10	**	Voltage Converter, 10mA Output
		LTC1044MJ8	CERDIP	9.5	**	Voltage Converter, 40mA Output, 5kHz Switching Rate
		LTC1044MH	TO-5 Can	9.5	**	Voltage Converter, 40mA Output, 5kHz Switching Rate
		LT1054MJ8	CERDIP	16	††	Voltage Converter and Regulator, 100mA Output, 25kHz Switching Rate
		LT1054MH	TO-5 Can	16	††	Voltage Converter and Regulator, 100mA Output, 25kHz Switching Rate

* The I_O values for the LT1070, LT1071, LT1072, LT1073, LT1074, LT1170, LT1171, and LT1172, are switch current values. Actual output current, voltage and polarity depends on the type of switching regulator employed.

** These devices are non-regulating converters.

†† The available output voltage range is dependent upon the mode.

NOTE: See page 4-3 for DESC cross reference numbers.

POWER SUPPLY PRODUCTS SELECTION GUIDE

COMMERCIAL

I_O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT*	PART NUMBER	PACKAGE TYPE	V_{IN}/ V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURE/COMMENTS
10.0	Pos Adj	LT1038CK	Steel TO-3	35	1.2 to 33	2% V_{OUT} Tol, Plug In Compatible with 317, 350, 338 Types
	Switching	LT1270ACT	TO-220	30	*	Self Contained 60kHz PWM and 10 Amp Switch in a 5-Pin Package
8.0	Switching	LT1270CT	TO-220	30	*	Self Contained 60kHz PWM and 8 Amp Switch in a 5-Pin Package
7.5	Pos Fixed	LT1083CK-5	Steel TO-3	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1083CP-5	Plastic TO-3P	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1083CK-12	Steel TO-3	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1083CP-12	Plastic TO-3P	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT1083CK	Steel TO-3	30	1.2 to 29	Low Dropout (1.2V), Pin Compatible with 317, 350, 338 Types
		LT 1083CP	Plastic TO-3P	30	1.2 to 29	Low Dropout (1.2V), Pin Compatible with 317, 350, 338 Types
5.0	Pos Fixed	LT1003CK	Steel TO-3	20	5	2% V_{OUT} Tol
		LT1003CP	Plastic TO-3P	20	5	2% V_{OUT} Tol
		LT1084CK-5	Steel TO-3	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1084CP-5	Plastic TO-3P	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1084CK-12	Steel TO-3	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1084CP-12	Plastic TO-3P	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT338AK LM338K	Steel TO-3	35	1.2 to 32	LT338A Has 1% V_{REF} Tol
		LT338AP LM338P	Plastic TO-3P	35	1.2 to 32	LT338A Has 1% V_{REF} Tol
		LT1084CK	Steel TO-3	30	1.2 to 29	Low Dropout (1.2V), Pin Compatible with 317, 350, 338 Types
		LT1084CP	Plastic TO-3P	30	1.2 to 29	Low Dropout (1.2V), Pin Compatible with 317, 350, 338 Types
		LT1087CT	TO-220	30	1.2 to 29	Low Dropout (1.2V) with Kelvin Sense
	Switching	LT1070CK	Steel TO-3	40	*	Self Contained 40kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1070CT	TO-220	40	*	Self Contained 40kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1070HVCK	Steel TO-3	60	*	Self Contained 40kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1070HVCT	TO-220	60	*	Self Contained 40kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1074CK	Steel TO-3	45	*	Self Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1074CT	TO-220	45	*	Self Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1074CV	11 Lead SIP	45	*	Self Contained 100kHz PWM and 5A Switch in a 11-Pin Power SIP Pkg
		LT1074HVCK	Steel TO-3	64	*	Self Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1074HVCT	TO-220	64	*	Self Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1074HVCV	11 Lead SIP	64	*	Self Contained 100kHz PWM and 5A Switch in a 11-Pin Power SIP Pkg
		LT1170CK	Steel TO-3	40	*	Self Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1170CT	TO-220	40	*	Self Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
		LT1170HVCT	TO-220	60	*	Self Contained 100kHz PWM and 5 Amp Switch in a 5-Pin Package
4.0	Switching	LT1271CQ	Plastic DD	30	*	Self Contained 60kHz PWM and 4 Amp Switch in 5-Pin Surface Mt Pkg
		LT1271CT	TO-220	30	*	Self Contained 60kHz PWM and 4 Amp Switch in 5-Pin Surface Mt Pkg
3.0	Pos Fixed	LT323AK LM323K	Steel TO-3	20	5	LT323A Has 1% V_{OUT} Tol
		LT323AT	TO-220	20	5	LT323A Has 1% V_{OUT} Tol
		LT1085CK-5	Steel TO-3	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1085CT-5	TO-220	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1085CK-12	Steel TO-3	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1085CT-12	TO-220	30	12	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT350AK LM350K	Steel TO-3	35	1.2 to 33	LT350A Has 1% V_{REF} Tol
		LT350AT LM350T	TO-220	35	1.2 to 33	LT350A Has 1% V_{REF} Tol
		LT350AP LM350P	Plastic TO-3P	35	1.2 to 33	LT350A Has 1% V_{REF} Tol
		LT1085CK	Steel TO-3	30	1.2 to 29	Low Dropout (1.2V), Pin Compatible with 317, 350 Types
		LT1085CT	TO-220	30	1.2 to 29	Low Dropout (1.2V), Pin Compatible with 317, 350 Types
	Neg Adj	LT1033CK	Steel TO-3	35	−1.2 to −32	2% V_{REF} Tol
		LT1033CP	Plastic TO-3P	35	−1.2 to −32	2% V_{REF} Tol
		LT1033CT	TO-220	35	−1.2 to −32	2% V_{REF} Tol
		LT1185CT	TO-220	35	−2.5 to −25	Low Dropout (0.75V) with Prog Current Limit and Shutdown
	Dual Pos Fixed	LT1035CK	Steel TO-3	20	Two 5V Outputs	Logic Controlled Main Output Voltage, 75mA Auxiliary Output
		LT1035CT	TO-220	20	Two 5V Outputs	Logic Controlled Main Output Voltage, 75mA Auxiliary Output
	Positive	LT1036CK	Steel TO-3	30	12, 5	Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output
		LT1036CT	TO-220	30	12, 5	Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output

* The I_O values for the LT1070, LT1071, LT1072, LT1073, LT1074, LT1082, LT1109, LT1110, LT1111, LT1170, LT1171, LT1172, and LT1173 are switch current values. Actual output current, voltage and polarity depends on the type of switching regulator employed.

COMMERCIAL

I_O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT*	PART NUMBER	PACKAGE TYPE	V_{IN}/ V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURE/COMMENTS
2.5	Switching	LT1071CK	Steel TO-3	40	*	Self Contained 40kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1071CT	TO-220	40	*	Self Contained 40kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1071HVCK	Steel TO-3	60	*	Self Contained 40kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1071HVCT	TO-220	60	*	Self Contained 40kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1171CK	Steel TO-3	40	*	Self Contained 100kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1171CT	TO-220	40	*	Self Contained 100kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1171HVCT	TO-220	60	*	Self Contained 100kHz PWM and 2.5 Amp Switch in a 5-Pin Package
		LT1171CQ	Plastic DD	40	*	Self Contained 100kHz PWM and 2.5 Amp Switch in a 5-Pin Surface Mount Package
2.0	Switching	LT1076CK	Steel TO-3	45	*	Self Contained 100kHz PWM and 2 Amp Switch in a 5-Pin Package
		LT1076CT	TO-220	45	*	
		LT1076HVCK	Steel TO-3	64	*	
		LT1076HVCT	TO-220	64	*	
		LT1076CY-5	7-Lead TO-220	45	5	100kHz PWM and 2 Amp Switch in a 7-Pin Package with Shutdown and Fixed 5V Output
		LT1076HVCY-5	7-Lead TO-220	64	5	
		LT1076CR-5	Plastic DD	45	5	Self Contained 100kHz PWM and 2 Amp Switch in a 7-Pin Surface Mount Package
		LT1076CV	11 Lead SIP	45	*	Self Contained 100kHz PWM and 2 Amp Switch in a 11-Pin Power SIP Package
		LT1076HVCV	11 Lead SIP	64	*	
		LT1103CV	11 Lead SIP	30	*	Designed for AC Line Powered Applications, Minimum External Components Required for 75W Isolated Power Supply
		LT1103CY	7-Lead TO-220	30	*	
1.5	Pos Fixed	LT1086CT-2.85	TO-220	30	2.85	Intended for SCSI-2 Active Termination
0.5 to 1.5	Pos Fixed	LT1086CK-5	Steel TO-3	30	5	Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1086CT-5	TO-220	30	5	
		LT1086CK-12	Steel TO-3	30	12	
		LT1086CT-12	TO-220	30	12	
	Pos Adj	LT317AK LM317K	Steel TO-3	40	1.2 to 37	LT317A Has 1% V_{REF} Tol
		LT317AH LM317H	TO-39	40	1.2 to 37	
		LT317AT LM317T	TO-220	40	1.2 to 37	
		LT1086CK	Steel TO-3	30	1.2 to 29	Low Dropout (1.2V),1% V_{REF} Tol Pin Compatible with 317 Types
		LT1086CT	TO-220	30	1.2 to 29	
		LT1086CH	TO-39	30	1.2 to 29	
		LT1086CM	Plastic DD	30	1.2 to 29	Low Dropout (1.2V), 1% V_{REF} Tol 3-Pin Surface Mount Package
	Neg Adj	LT337AK LM337K	Steel TO-3	40	−1.2 to −37	LT337A Has 1% V_{REF} Tol
		LT337AH LM337H	TO-39	40	−1.2 to −37	
		LT337AT LM337H	TO-220	40	−1.2 to −37	
	Pos Adj High Voltage	LT317AHVK LM317HVK	Steel TO-3	60	1.2 to 57	LT317HV Has 1% V_{REF} Tol
		LT317AHVH LM317HVH	TO-39	60	1.2 to 57	
	Neg Adj High Voltage	LT337AHVK LM337HVK	Steel TO-3	50	−1.2 to −47	LT337HV Has 1% V_{REF} Tol
		LT337AHVH LM337HVH	TO-39	50	−1.2 to −47	
1.25	Switching	LT1072CK	Steel TO-3	40	*	Self Contained 40kHz PWM and 1.25 Amp Switch in a 5-Pin Package
		LT1072CT	TO-220	40	*	
		LT1072HVCK	Steel TO-3	60	*	
		LT1072HVCT	TO-220	60	*	
		LT1072CJ8	8-Pin CERDIP	40	*	Self Contained 40kHz PWM and 1.25 Amp Switch
		LT1072CN8	8-Pin Plastic DIP	40	*	
		LT1072CS	16-Pin Plastic SOL	40	*	
		LT1172CK	Steel TO-3	40	*	Self Contained 100kHz PWM and 1.25 Amp Switch in a 5-Pin Package
		LT1172CT	TO-220	40	*	
		LT1172HVCT	TO-220	60	*	
		LT1172CJ8	8-Pin CERDIP	40	*	Self Contained 100kHz PWM and 1.25 Amp Switch
		LT1172CN8	8-Pin Plastic DIP	40	*	
		LT1172CS	16-Pin Plastic SOL	40	*	
1.0	Dual Pos Fixed	LT1005CK	Steel TO-3	20	Two 5V Outputs	Logic Controlled Main Output Voltage
		LT1005CT	TO-220	20	Two 5V Outputs	

* The I_O values for the LT1070, LT1071, LT1072, LT1073, LT1074, LT1082, LT1109, LT1110, LT1111, LT1170, LT1171, LT1172, and LT1173 are switch current values. Actual output current, voltage and polarity depends on the type of switching regulator employed.

POWER SUPPLY PRODUCTS SELECTION GUIDE

COMMERCIAL

I_O OUTPUT CURRENT (AMPS)*	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/ V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURE/COMMENTS
1.0	Switching	LT1073CN8	8-Pin Plastic DIP	15	Adjustable	Micropower Switching Regulator Works Down to 1V Input. Requires Only 3 External Components (-5, -12 Versions)
		LT1073CS8	8-Pin Plastic SOIC	15	Adjustable	
		LT1073CN8-5	8-Pin Plastic DIP	15	5	
		LT1073CS8-5	8-Pin Plastic SOIC	15	5	
		LT1073CN8-12	8-Pin Plastic DIP	15	12	
		LT1073CS8-12	8-Pin Plastic SOIC	15	12	
		LT1082CT	TO-220	75	*	60kHz PWM and 1 Amp Switch in a 5-Pin Package
		LT1109CZ-5	3-Pin TO-92	36	5	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions). Optimized for $V_{IN} \geq 2V$. Available in 3-Pin TO-92 Package. N8/S8 Versions Also Offer Shutdown Feature. 12V version ideal for flash memory Vpp pulse generation from 5V or 3V
		LT1109CZ-12	3-Pin TO-92	36	12	
		LT1109CN8-5	8-Pin Plastic DIP	36	5	
		LT1109CS8-12	8-Pin Plastic SOIC	36	5	
		LT1109CN8-5	8-Pin Plastic DIP	36	12	
		LT1109CS8-12	8-Pin Plastic SOIC	36	12	
		LT1110CN8	8-Pin Plastic DIP	15	Adjustable	Micropower Switching Regulator Works Down to 1V Input. Requires Only 3 External Components (-5, -12 Versions). 60kHz Oscillator Allows Use of Surface Mount Inductors
		LT1110CS8	8-Pin Plastic SOIC	15	Adjustable	
		LT1110CN8-5	8-Pin Plastic DIP	15	5	
		LT1110CS8-5	8-Pin Plastic SOIC	15	5	
		LT1110CN8-12	8-Pin Plastic DIP	15	12	
		LT1110CS8-12	8-Pin Plastic SOIC	15	12	
		LT1111CN8	8-Pin Plastic DIP	36	Adjustable	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions). Optimized for $V_{IN} \geq 2V$. 70kHz Oscillator Allows Use of Surface Mount Inductors
		LT1111CS8	8-Pin Plastic SOIC	36	Adjustable	
		LT1111CN8-5	8-Pin Plastic DIP	36	5	
		LT1111CS8-5	8-Pin Plastic SOIC	36	5	
		LT1111CN8-12	8-Pin Plastic DIP	36	12	
		LT1111CS8-12	8-Pin Plastic SOIC	36	12	
		LT1173CN8	8-Pin Plastic DIP	36	Adjustable	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions). Optimized for $V_{IN} \geq 2V$
		LT1173CS8	8-Pin Plastic SOIC	36	Adjustable	
		LT1173CN8-5	8-Pin Plastic DIP	36	5	
		LT1173CS8-5	8-Pin Plastic SOIC	36	5	
		LT1173CN8-12	8-Pin Plastic DIP	36	12	
		LT1173CS8-12	8-Pin Plastic SOIC	36	12	
800mA	Pos Fixed	LT1117-2.85	3-Pin SOT-223	12	2.85	Active SCSI-2 Terminator, SOT-223 Package
		LT1117-5	3-Pin SOT-223	10	5	5V Low Dropout Regulator, SOT-223 Package
		LT1117	3-Pin SOT-223	15	Adjustable	Adjustable Low Dropout Regulator, SOT-223 Package
125mA	Pos Adj	LT1020CJ	14-Pin CERDIP	36	4 to 30	Dropout Voltage = 0.4V, 40μA I_Q, Reference and Comparator
		LT1020CN	14-Pin Plastic	36	4 to 30	
		LT1020CS	16-Pin Plastic SOL	36	4 to 30	
		LT1120CJ8	8-Pin CERDIP	36	4 to 30	Dropout Voltage = 0.4V, 40μA I_Q, Reference, Comparator, Shutdown, 8-Pin Package
		LT1120CN8	8-Pin Plastic DIP	36	4 to 30	
		LT1120CH	8-Pin TO-5	36	4 to 30	
100mA	Pos Adj	LT1431CJ8	8-Pin CERDIP	36	2.5 to 36	0.4% Initial Tolerance, 1% Over Temperature
		LT1431CN8	8-Pin Plastic DIP	36	2.5 to 36	
		LT1431CS8	8-Pin Plastic SOIC	36	2.5 to 36	
		LT1431CZ	TO-92	36	2.5 to 36	
40mA to 100mA	Switched Capacitor	LT1026CJ8	8-Pin CERDIP	10	**	Voltage Converter, 10mA Output, $\pm 2V_{IN}$
		LT1026CN8	8-Pin Plastic DIP	10	**	
		LT1026CH	8-Pin TO-5 Can	10	**	
		LTC1044CJ8	8-Pin CERDIP	9.5	**	Voltage Converter, 40mA Output
		LTC1044CN8	8-Pin Plastic DIP	9.5	**	
		LTC1044CH	8-Pin TO-5 Can	9.5	**	
		LTC1044CS8	8-Pin Plastic SO	9.5	**	
		LTC1046CN8	8-Pin Plastic DIP	6	**	50mA Output Current, 165μA Supply Current, 35Ω Max Output Impedance
		LTC1046CS8	8-Pin Plastic SOIC	6	**	
		LT1054CJ8	8-Pin CERDIP	16	††	Voltage Converter and Regulator, 100mA Output, 25kHz Switching Rate
		LT1054CN8	8-Pin Plastic DIP	16	††	
		LT1054CH	8-Pin TO-5 Can	16	††	
		LT1054CS	16-Pin Plastic SOL	16	††	

* The I_O values for the LT1070, LT1071, LT1072, LT1073, LT1074, LT1082, LT1109, LT1110, LT1111, LT1170, LT1171, LT1172, and LT1173 are switch current values. Actual output current, voltage and polarity depends on the type of switching regulator employed.

** These devices are non-regulating converters.

†† The available output voltage range is dependent upon the mode of operation selected.

SURFACE MOUNT

I_0 OUTPUT CURRENT (AMPS)	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_0 NOMINAL REG OUTPUT VOLTAGE (V)	FEATURES/COMMENTS
4.0	Switching	LT1271CQ	Plastic DD	30	*	Self Contained 60kHz PWM and 4A Switch in a 5-Pin Surface Mount Pkg
2.5	Switching	LT1171CQ	Plastic DD	40	*	Self Contained 100kHz PWM and 2.5A Switch in a 5-Pin Surface Mount Pkg
2.0	Switching	LT1076CR-5	Plastic DD	45	*	Self Contained 100kHz PWM and 2A Switch in a 7-Pin Surface Mount Pkg
0.5 to 1.5	Pos Adj	LT1086CM	Plastic DD	30	*	Low Dropout (1.2V), 1% V_{REF} Tol 3-Pin Surface Mount Pkg
1.25	Switching	LT1072S8	8-Pin Plastic SOIC	40	*	Self Contained Power and 1.25A Switch
1.25	Switching	LT1172S8	8-Pin Plastic SOIC	40	*	Self Contained 100kHz PWM and 1.25A Switch
1.25	Switching	LT1072CS	16-Pin Plastic SOL	40	*	Self Contained Power and 1.25A Switch
1.25	Switching	LT1172CS	16-Pin Plastic SOL	40	*	Self Contained 100kHz PWM and 1.25A Switch
1.0	Switching	LT1073CS8	8-Pin Plastic SOIC	15	Adjustable	Micropower Switching Regulator Works Down to 1V Input. Requires Only 3 External Components (-5, -12 Versions)
1.0	Switching	LT1073CS8-5	8-Pin Plastic SOIC	15	5	
1.0	Switching	LT1073CS8-12	8-Pin Plastic SOIC	15	12	
1.0	Switching	LT1109CS8	8-Pin Plastic SOIC	20	Adjustable	Micropower Switching Regulator Works Down to 2V Input. Ideal for Flash Memory Vpp Generation (-12 Version)
1.0	Switching	LT1109CS8-5	8-Pin Plastic SOIC	20	5	
1.0	Switching	LT1109CS8-12	8-Pin Plastic SOIC	20	12	
1.0	Switching	LT1110CS8	8-Pin Plastic SOIC	36	Adjustable	Micropower Switching Regulator Works Down to 1V Output. Requires Only 3 External Components (-5, -12 Versions)
1.0	Switching	LT1110CS8-5	8-Pin Plastic SOIC	36	5	
1.0	Switching	LT1110CS8-12	8-Pin Plastic SOIC	36	12	
1.0	Switching	LT1111CS8	8-Pin Plastic SOIC	36	Adjustable	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions)
1.0	Switching	LT1111CS8-5	8-Pin Plastic SOIC	36	5	
1.0	Switching	LT1111CS8-12	8-Pin Plastic SOIC	36	12	
1.0	Switching	LT1173CS8	8-Pin Plastic SOIC	36	Adjustable	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions). Optimized for $V_{IN} \geq 2V$
1.0	Switching	LT1173CS8-5	8-Pin Plastic SOIC	36	5	
1.0	Switching	LT1173CS8-12	8-Pin Plastic SOIC	36	12	
800mA	Positive	LT1117CST	SOT-223	15	Adjustable	Low Dropout Adjustable Regulator, 800mA Output at 1V Dropout Voltage, SOT-223 Package
800mA	Positive	LT1117CST-2.85	SOT-223	15	2.85	
800mA	Positive	LT1117CST-5	SOT-223	15	5	
125mA	Pos Adj	LT1020CS	16-Pin Plastic SOL	36	4 to 30	Dropout Voltage = 0.4V, 40mA I_Q, Reference and Comparator
100mA	Switched Cap	LT1054CS	16-Pin Plastic SOL	16	††	Voltage Converter and Regulator, 25kHz Switching Rate
50mA	Switched Cap	LTC1046CS8	8-Pin Plastic SOIC	6	**	Lowest Loss for $V_{IN} \leq 6V$
20mA	Switched Cap	LTC1044CS8	8-Pin Plastic SOIC	9.5	**	Voltage Converter, 5kHz Switching Rate

* The I_0 values for the LT1070, LT1071, LT1072, LT1170, LT1171, and LT1172, are switch current values. Actual output current, voltage and polarity depends on the type of switching regulator employed.

** These devices are non-regulating converters.

†† The available output voltage range is dependent upon the mode of operation selected.

REGULATOR DRIVERS

BASE DRIVE CURRENT	POSITIVE OR NEGATIVE OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN} MAX (V)	V_0 NOMINAL REGULATED OUTPUT VOLTAGE (V)	FEATURE/COMMENTS
150mA	Pos Fixed	LT1123CZ	TO-92	30	5.0	Requires External PNP, 1% Output Tolerance, 600µA Quiescent Current
150mA	Pos Fixed	LT1123CS8-2.85	S08	30	2.85	

REGULATING PULSE-WIDTH MODULATORS

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LT1105	Off-Line Regulating Pulse Width Modulator	N8	Designed for AC Line Powered Applications
LT1241 Series	500kHz Regulating Pulse Width Modulators	J8, N8, S8	Improved Replacements for UC1842, 1843, 1844, 1845
LT1246	1MHz Regulating Pulse Width Modulator	J8, N8, S8	1MHz Current Mode PWM, 1.5% V_{REF}
LT1524/LT3524	Regulating Pulse Width Modulator	J, N, S	Improved SG1524, 2% V_{REF}, Guaranteed Oscillator Accuracy
LT1525A/LT3525A LT1527A/LT3527A	Regulating Pulse Width Modulator	J, N	Improved SG1525A/1527A Switching Regulator with Undervoltage Lockout, Guaranteed Long Term Stability
LT1526/LT3526	Regulating Pulse Width Modulator	J, N	Switching Regulator Control with Soft Start, Current Limit, Metering Logic, Undervoltage Lockout, Guaranteed Long Term Stability
SG1524/SG3524	Regulating Pulse Width Modulator	J, N	Industry Standard Switching Power Supply Control Circuit
SG1525A/SG3525A	Regulating Pulse Width Modulator	J, N	More Features Than 1524 Series, 100mA Source/Sink Outputs
SG1527A/SG3527A	Regulating Pulse Width Modulator	J, N	Same as SG1525A with Inverted Output Logic
LT1846/3846 LT1847/3847	Current Mode Regulating Pulse Width Modulator	J, N	Current Mode PWM with UV Lockout, Soft Start, 1% V_{REF}, 500kHz Operation, 200mA Totem Pole Outputs

SWITCHING REGULATOR CONTROLLERS

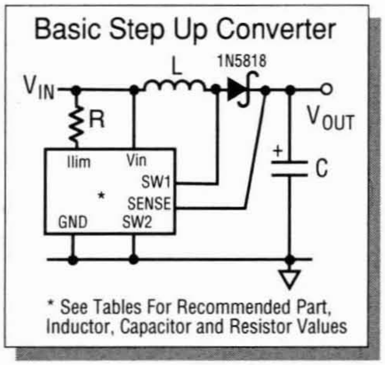
PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LT1432	Step-Down Switching Regulator Controller	N8, S8	Provides High Efficiency +5V Output Using LT1070 Series Regulator and Minimum External Parts

LTC BATTERY POWERED DC/DC CONVERSION SOLUTIONS

STEP UP FROM ONE CELL (1V)

V_{OUT}	I_{OUT}	P/N	I_Q	L	C	R	Price **	
5V	40mA	LT1073-5	95µA	82µH	100µF	0Ω	$3.15	Most Efficient
	40mA	LT1110-5	350µA	27µH	33µF	0Ω	$3.15	**Best For Surface Mount**
12V	15mA	LT1073-12	95µA	82µH	100µF	0Ω	$3.15	Most Efficient
	15mA	LT1110-12	350µA	27µH	33µF	0Ω	$3.15	**Best For Surface Mount**

•ADJUSTABLE VERSIONS ALSO AVAILABLE FOR V_{OUT} UP TO 50V



* See Tables For Recommended Part, Inductor, Capacitor and Resistor Values

STEP UP FROM TWO CELLS (2V)

V_{OUT}	I_{OUT}	P/N	I_Q	L	C	R	Price **	
5V	90mA	LT1173-5	110µA	47µH	100µF	47Ω	$2.40	Most Efficient
	90mA	LT1111-5	350µA	18µH	33µF	47Ω	$2.40	Smallest Board Space/**Best For Surface Mount**
	150mA	LT1073-5	95µA	100µH	100µF	47Ω	$3.15	More Output Current/Most Efficient
	150mA	LT1110-5	350µA	33µH	33µF	47Ω	$3.15	More Output Current/Smallest Board Space/**Best For Surface Mount**
	20mA	LT1109CZ-5	1mA	33µH	10µF	N/A	$1.90	3 Pin Package/Lowest Cost/**Best For Surface Mount (8 Lead Version)**
12V	20mA	LT1173-12	110µA	47µH	47µF	47Ω	$2.40	Most Efficient
	20mA	LT1111-12	350µA	18µH	22µF	47Ω	$2.40	Smallest Board Space/**Best For Surface Mount**
	40mA	LT1073-12	95µA	82µH	100µF	47Ω	$3.15	More Output Current/Most Efficient
	40mA	LT1110-12	350µA	27µH	33µF	0Ω	$3.15	More Output Current/Smallest Board Space/**Best For Surface Mount**
	20mA	LT1109CZ-12	350µA	20µH	4.7µF	N/A	$1.90	3 Pin Package/Lowest Cost/**Best For Surface Mount (8 Lead Version)**

• ADJUSTABLE VERSIONS ALSO AVAILABLE FOR V_{OUT} UP TO 50V

STEP UP FROM 5V TO 12V

V_{OUT}	I_{OUT}	P/N	I_Q	L	C	R	Price **	
12V	90mA	LT1173-12	110µA	120µH	100µF	0Ω	$2.40	Most Efficient
	90mA	LT1111-12	350µA	47µH	33µF	0Ω	$2.40	Smallest Board Space/**Best For Surface Mount**
	175mA	LT1073-12	95µA	180µH	100µF	0Ω	$3.15	More Output Current/Most Efficient
	175mA	LT1110-12	350µA	60µH	33µF	0Ω	$3.15	More Output Current/**Best For Surface Mount**
	60mA	LT1109CZ-12	350µA	33µH	10µF	N/A	$1.90	3 Pin Package/Lowest Cost/**Best For Surface Mount (8 Lead Version)**

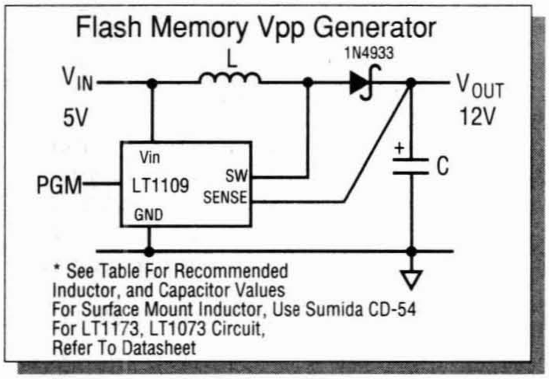
• ADJUSTABLE VERSIONS ALSO AVAILABLE FOR V_{OUT} UP TO 50V

FLASH MEMORY VPP (12V) GENERATION

Vout	I_{OUT}	P/N	I_Q	L	C	R	Price **	
12V	60mA	LT1109-12	350µA	33µH	10µF	----	$2.90	All Surface Mount
	90mA	LT1173 ADJ	110µA	120µH	100µF	47Ω	$2.40	More I_{OUT}
	120mA	LT1073 ADJ	100µA	100µH†	100µF	20Ω	$3.15	Most I_{OUT}

All Flash Memory V_{PP} Circuits Can Easily Be Made In All Surface Mount- Including Inductors- **See Other Side**

**** 100 Piece Quantity Price** † Coiltronics CTX100-4



* See Table For Recommended Inductor, and Capacitor Values
For Surface Mount Inductor, Use Sumida CD-54
For LT1173, LT1073 Circuit, Refer To Datasheet

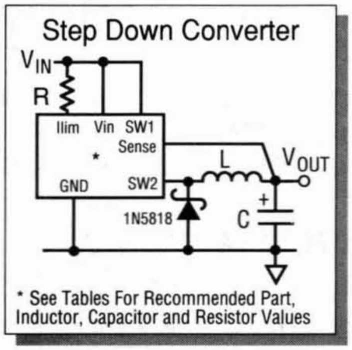
SEE OTHER SIDE FOR MORE DC/DC CONVERSION SOLUTIONS, INDUCTOR MFGRs., CAP MFGRs., DEVICE PINOUTS

LTC BATTERY POWERED DC/DC CONVERSION SOLUTIONS

STEP DOWN CONVERSION TO 5V

V_{IN}	I_{OUT}	P/N	I_Q	L	C	R	Price **	
6.5V to 12V	50mA	LT1173-5	110µA	47µH	100µF	100Ω	$2.40	Most Efficient
	50mA	LT1111-5	330µA	18µH	33µF	100Ω	$2.40	**Best For Surface Mount**
	90mA	LT1073-5	95µA	47µH	100µF	220Ω	$3.15	More Output Current/Most Efficient
	90mA	LT1110-5	330µA	15µH	33µF	220Ω	$3.15	More I_{OUT}/**Best For Surface Mount**
9V to 20V	300mA	LT1073-5	95µA	180µH	330µF	100Ω	$3.15	Most Efficient
	300mA	LT1110-5	330µA	60µH	100µF	100Ω	$3.15	**Best For Surface Mount**
12V to 20V	300mA	LT1173-5	110µA	220µH	220µF	220Ω	$2.40	Most Efficient
	300mA	LT1111-5	330µA	82µH	100µF	220Ω	$2.40	**Best For Surface Mount**
20V to 30V	300mA	LT1173-5	110µA	470µH	470µF	100Ω	$2.40	Most Efficient
	300mA	LT1111-5	330µA	180µH	220µF	100Ω	$2.40	**Best For Surface Mount**

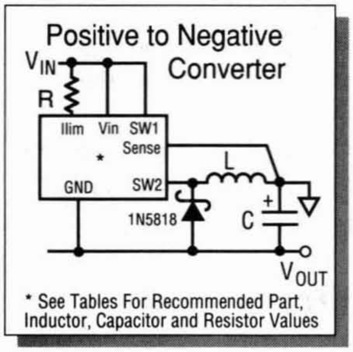
• ADJUSTABLE OUTPUT VOLTAGES UP TO 6.2V CAN BE OBTAINED WITH THE ADJUSTABLE VERSIONS OF LT1173, LT1111, LT1073 OR LT1110


Step Down Converter

* See Tables For Recommended Part, Inductor, Capacitor and Resistor Values

POSITIVE TO NEGATIVE VOLTAGE CONVERSION

V_{IN}	V_{OUT}	I_{OUT}	P/N	I_Q	L	C	R	Price **	
5V	-5V	75mA	LT1173-5	250µA	100µH	100µF	100Ω	$2.40	Most Efficient
	-5V	75mA	LT1111-5	650µA	33µH	33µF	100Ω	$2.40	**Best For Surface Mount**
	-5V	150mA	LT1073-5	220µA	180µH	470µF	100Ω	$3.15	More Output Current
	-5V	150mA	LT1110-5	650µA	68µH	150µF	100Ω	$3.15	More I_{OUT}/**Best For Surface Mount**
12V	-5V	250mA	LT1173-5	110µA	470µH	220µF	100Ω	$2.40	Most Efficient
	-5V	250mA	LT1111-5	330µA	180µH	82µF	100Ω	$2.40	**Best For Surface Mount**


Positive to Negative Converter

* See Tables For Recommended Part, Inductor, Capacitor and Resistor Values

INDUCTOR AND CAPACITOR PART NUMBERS/MANUFACTURERS

Inductor Value	Caddell-Burns P/N	Gowanda P/N	Coiltronics P/N ††
15µH	7070-15	GA10-152K	----
18µH	7070-16	GA10-182K	CTX20-1
20µH	----	----	CTX20-1
22µH	7070-17	GA10-222K	CTX20-1
27µH	7070-18	GA10-272K	----
33µH	7070-19	GA10-332K	----
47µH	7300-09	GA10-472K	CTX50-1
68µH	7300-11	GA10-682K	----
82µH	7300-12	GA10-822K	CTX82-1
100µH	7300-13	GA10-103K	CTX100-1
120µH	7300-14	GA10-123K	CTX100-1
180µH	7200-16	GA40-183K	CTX250-4
220µH	7200-17	GA40-223K	CTX250-4
470µH	7200-21	GA40-473K	----

**** 100 Piece Quantity Price** **†† Surface Mount Inductors**

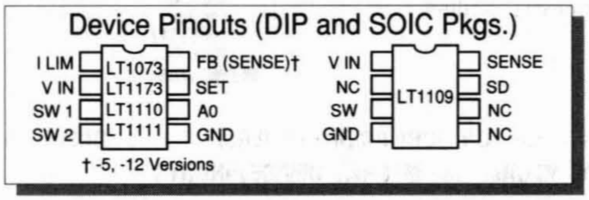
Inductor Manufacturers

Caddell-Burns	Mineola, NY, USA 11501	516-746-2310	FAX: 516-742-2416
Gowanda Elect.	Gowanda, NY, USA 14070	716-532-2234	FAX: 716-532-2702
Coiltronics Intl.	Pompano Beach, FL, USA	305-781-8900	FAX: 305-782-4163
†† Sumida	Arlington Heights, Ill, USA	708-956-0666	FAX: 708-956-0702

Capacitor Manufacturers

Best:	OS-CON Series	Sanyo Video	San Diego, CA, USA 92073	619-661-6322
Better:	PL Series	Nichicon America	Schaumberg, IL, USA 60173	708-843-7500
Good:	150D or 550D	Sprague Electric	Sanford, ME, USA 04073	207-324-4140

Device Pinouts (DIP and SOIC Pkgs.)



† -5, -12 Versions

POWER AND MOTOR CONTROL CIRCUITS

High Side Switch Drivers

LTC1155 – Dual N-Ch FET Switch Drivers w/ Short Circuit Protection

LTC1156 – Quad N-Ch FET Switch Drivers w/ Short Circuit Protection

Integrated High Side Switches

LT1188 – 1.5A HSS, Output Protected Against Inductive Kickback
Controlled Slew Rate/Low RF Noise
STATUS Line for Diagnostics
Protected Against Overtemp, Load Faults

LT1089 – 7.5A HSS, Low Loss, Only 1.5V at 7.5A
Protected Against Overtemp, Overcurrent. Low
Quiescent Current

Half Bridge N-Ch MOSFET Drivers

LT1158 – 5V to 30V Operation, Drives DC motors and Switching Power Supply N-Ch MOSFET Switch Gates, On-Chip Charge Pump, Adaptive Anti Shoot-Through, Fully Protected, 150ns Transition Times Driving 3000pF

P/N	DESCRIPTION	PACKAGE	FEATURES
LTC1155	Dual High-Side Switch Driver	N8, S8	Low Quiescent Current, Short Circuit Protection, Internal Capacitors, Drives Low-Loss N-Channel MOSFETs
LTC1156	Quad High-Side Switch Driver	N, S	Four Drivers in One Package, Low Quiescent Current, Short Circuit Protection, Internal Capacitors
LT1158	Half Bridge N-Channel MOSFET Driver	N	Drives 3000pF Loads in 150ns, Continuous Current Limit Protection, 5V to 30V Supplies

NOTES

SECTION 4—POWER PRODUCTS

INDUCTORLESS DC TO DC CONVERTERS

LTC1046, 50mA Switched Capacitor Voltage Converter 4-16

"Inductorless" +5V to –5V Converter

FEATURES

- 50mA Output Current
- Plug-In Compatible with ICL7660/LTC1044
- $R_{OUT} = 35\Omega$ Maximum
- 300μA Maximum No Load Supply Current at 5V
- Boost Pin (Pin 1) for Higher Switching Frequency
- 97% Minimum Open Circuit Voltage Conversion Efficiency
- 95% Minimum Power Conversion Efficiency
- Wide Operating Supply Voltage Range, 1.5V to 6V
- Easy to Use
- Low Cost

APPLICATIONS

- Conversion of +5V to ±5V Supplies
- Precise Voltage Division, $V_{OUT} = V_{IN}/2$
- Supply Splitter, $V_{OUT} = \pm V_S/2$

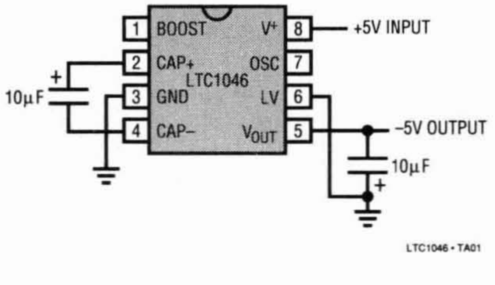
DESCRIPTION

The LTC1046 is a 50mA monolithic CMOS switched capacitor voltage converter. It plugs in for ICL7660/LTC1044 in 5V applications where more output current is needed. The device is optimized to provide high current capability for input voltages of 6V or less. It trades off operating voltage to get higher output current. The LTC1046 provides several voltage conversion functions: the input voltage can be inverted ($V_{OUT} = -V_{IN}$), divided ($V_{OUT} = V_{IN}/2$) or multiplied ($V_{OUT} = \pm nV_{IN}$).

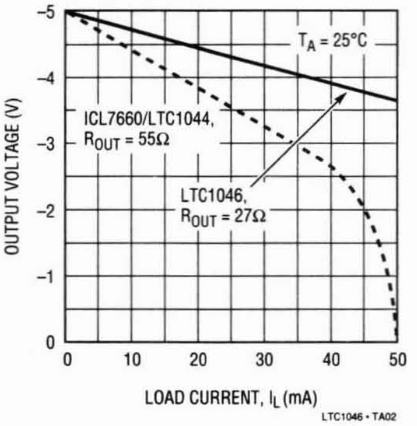
Designed to be pin-for-pin and functionally compatible with the ICL7660 and LTC1044, the LTC1046 provides 2.5 times the output drive capability.

TYPICAL APPLICATION

Generating –5V from +5V



Output Voltage vs Load Current for V+ = 5V

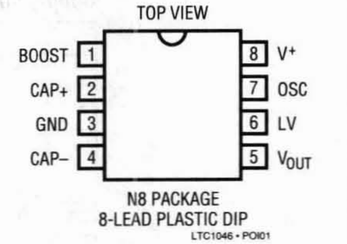


ABSOLUTE MAXIMUM RATINGS

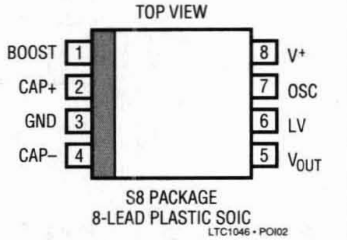
(Note 1)

Supply Voltage 6.5V
Input Voltage on Pins 1, 6 and 7
(Note 2) .... $-0.3 < V_{IN} < (V^+) + 0.3V$
Current into Pin 6 .... 20μA
Output Short Circuit Duration
($V^+ \leq 6V$) .... Continuous
Operating Temperature Range
LTC1046C .... $0°C \leq T_A \leq 70°C$
LTC1046I .... $-40°C \leq T_A \leq 85°C$
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP



S8 PACKAGE
8-LEAD PLASTIC SOIC

ORDER PART NUMBER
LTC1046IN8 LTC1046CN8
LTC1046IS8 LTC1046CS8
S8 PART MARKING
1046 1046I

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $C_{OSC} = 0pF$, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1046C			LTC1046I			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
I_S	Supply Current	$R_L = \infty$, Pins 1 and 7 No Connection			165	300		165	300	μA
		$R_L = \infty$, Pins 1 and 7 No Connection, $V^+ = 3V$			35			35		μA
V^+_L	Minimum Supply Voltage	$R_L = 5k\Omega$	●	1.5			1.5			V
V^+_H	Maximum Supply Voltage	$R_L = 5k\Omega$	●			6			6	V
R_{OUT}	Output Resistance	$V^+ = 5V$, $I_L = 50mA$ (Note 3)			27	35		27	35	Ω
			●		27	45		27	50	Ω
		$V^+ = 2V$, $I_L = 10mA$	●		60	85		60	90	Ω
f_{OSC}	Oscillator Frequency	$V^+ = 5V$ (Note 4)		20	30		20	30		kHz
		$V^+ = 2V$		4	5.5		4	5.5		kHz
P_{EFF}	Power Efficiency	$R_L = 2.4k\Omega$		95	97		95	97		%
V_{OUTEFF}	Voltage Conversion Efficiency	$R_L = \infty$		97	99.9		97	99.9		%
I_{OSC}	Oscillator Sink or Source Current	$V_{OSC} = 0V$ or V^+								
		Pin 1 = 0V	●		4.2	35		4.2	40	μA
		Pin 1 = V^+	●		15	45		15	50	μA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

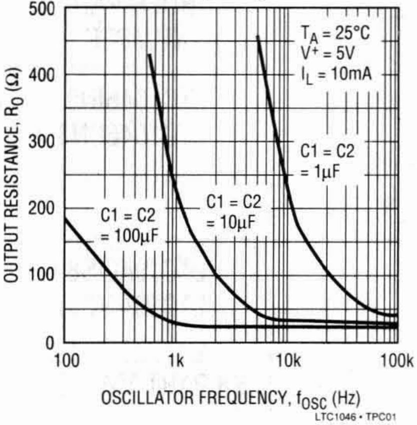
Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to power-up of the LTC1046.

Note 3: R_{OUT} is measured at $T_J = 25°C$ immediately after power-on.

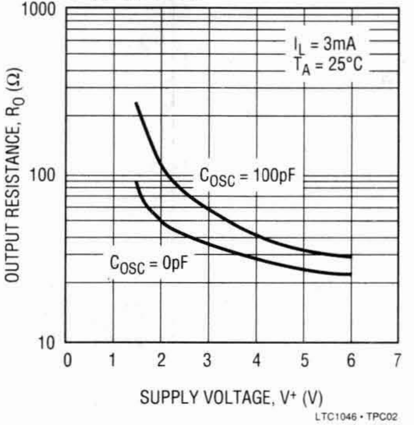
Note 4: f_{OSC} is tested with $C_{OSC} = 100pF$ to minimize the effects of test fixture capacitance loading. The 0pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit in Figure 1)

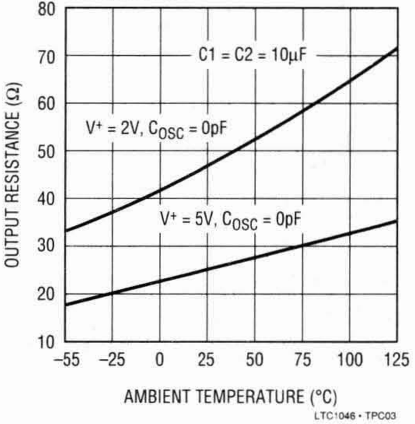
Output Resistance vs Oscillator Frequency



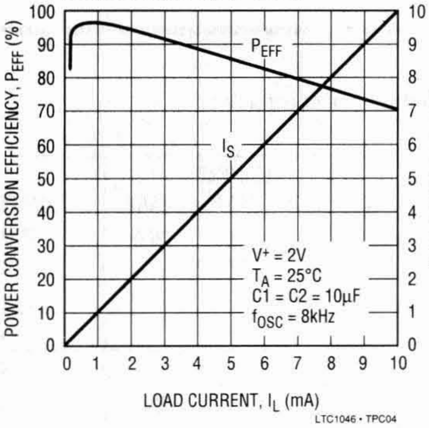
Output Resistance vs Supply Voltage



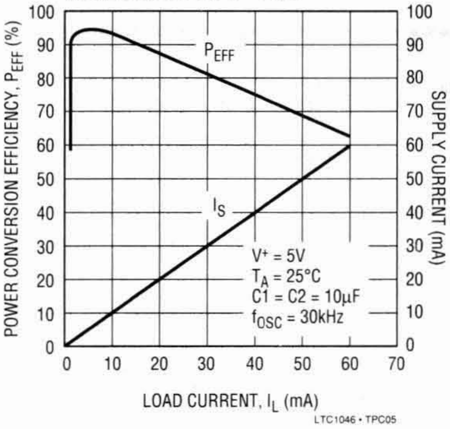
Output Resistance vs Temperature



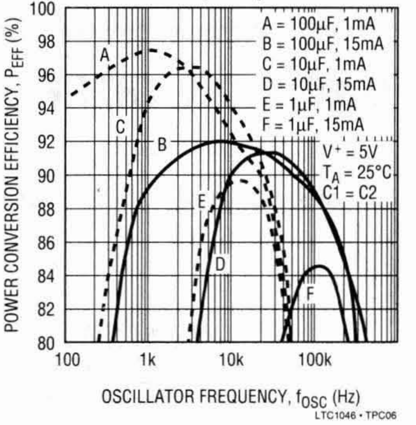
Power Conversion Efficiency vs Load Current for V$^+$ = 2V



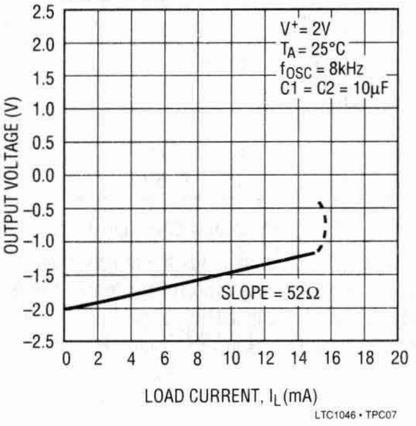
Power Conversion Efficiency vs Load Current for V$^+$ = 5V



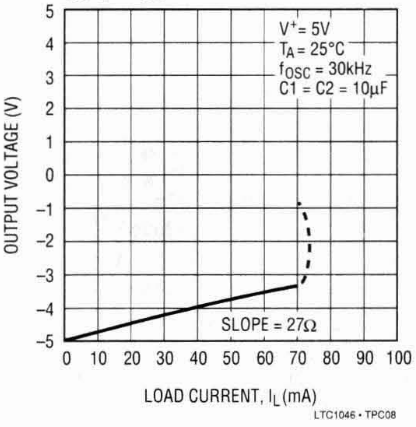
Power Conversion Efficiency vs Oscillator Frequency



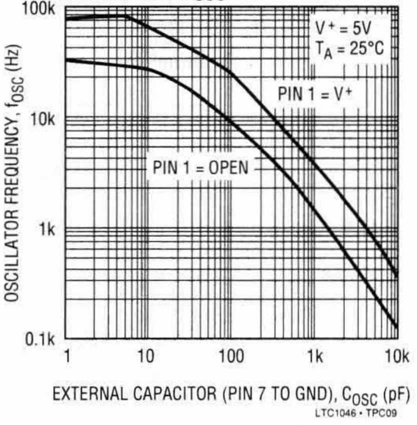
Output Voltage vs Load Current for V$^+$ = 2V



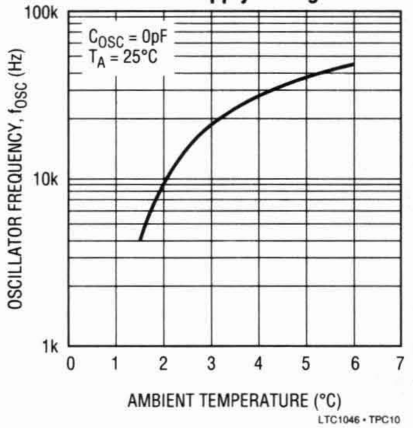
Output Voltage vs Load Current for V$^+$ = 5V

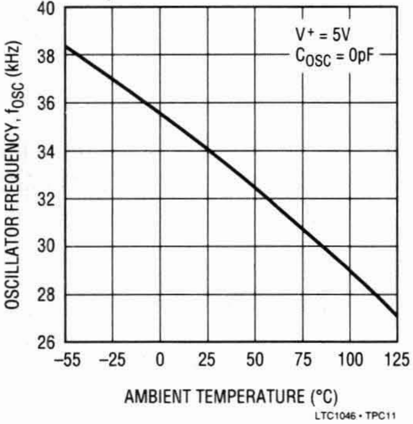


Oscillator Frequency as a Function of C$_{OSC}$



TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit in Figure 1)


Oscillator Frequency as a Function of Supply Voltage


Oscillator Frequency vs Temperature

TEST CIRCUIT

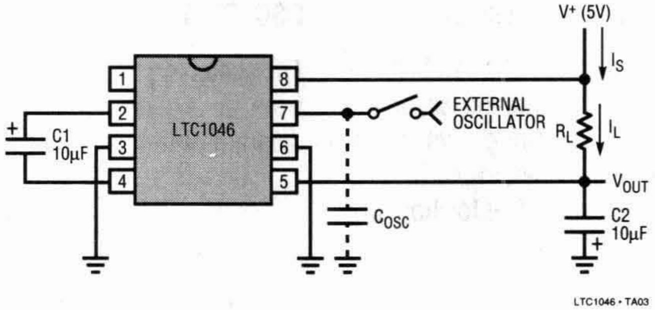

V+ (5V)
I_S
1
2
3
4
8
7
6
5
LTC1046
C1
10µF
+
EXTERNAL
OSCILLATOR
R_L
I_L
V_OUT
C_OSC
C2
10µF
+
LTC1046 • TA03

Figure 1.

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation of the LTC1046, a review of a basic switched capacitor building block is helpful.

In Figure 2, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be $q1 = C1V1$. The switch then moves to the right, discharging C1 to voltage V2. After this discharge time, the charge on C1 is $q2 = C1V2$. Note that charge has been transferred from the source, V1, to the output, V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1(V1 - V2).$$

If the switch is cycled "f" times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1(V1 - V2).$$

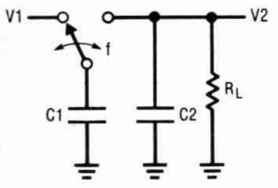

V1
V2
f
C1
C2
R_L

Figure 2. Switched Capacitor Building Block

APPLICATIONS INFORMATION

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{(1/fC1)} = \frac{V1 - V2}{R_{EQUIV}}.$$

A new variable, R_{EQUIV}, has been defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched capacitor network is as shown in Figure 3.

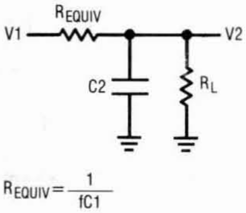


Figure 3. Switched Capacitor Equivalent Circuit

Examination of Figure 4 shows that the LTC1046 has the same switching action as the basic switched capacitor building block. With the addition of finite switch ON resistance and output voltage ripple, the simple theory, although not exact, provides an intuitive feel for how the device works.

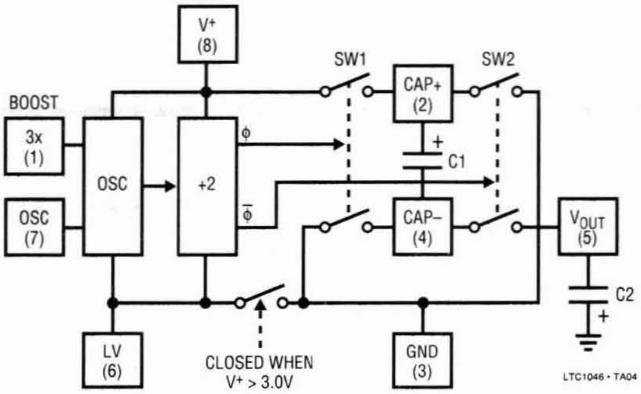


Figure 4. LTC1046 Switched Capacitor Voltage Converter Block Diagram

For example, if you examine power conversion efficiency as a function of frequency (see typical curve), this simple theory will explain how the LTC1046 behaves. The loss, and hence the efficiency, is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and power efficiency will drop. The typical curves for power efficiency versus frequency show this effect for various capacitor values.

Note also that power efficiency decreases as frequency goes up. This is caused by internal switching losses which occur due to some finite charge being lost on each switching cycle. This charge loss per unit cycle, when multiplied by the switching frequency, becomes a current loss. At high frequency this loss becomes significant and the power efficiency starts to decrease.

LV (Pin 6)

The internal logic of the LTC1046 runs between V^+ and LV (pin 6). For V^+ greater than or equal to 3V, an internal switch shorts LV to ground (pin 3). For V^+ less than 3V, the LV pin should be tied to ground. For V^+ greater than or equal to 3V, the LV pin can be tied to ground or left floating.

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered or driven from an external source. Figure 5 shows a functional diagram of the oscillator circuit.

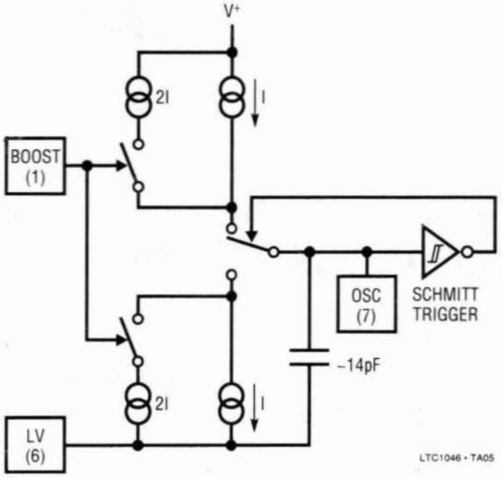


Figure 5. Oscillator

By connecting the boost pin (pin 1) to V^+, the charge and discharge current is increased and, hence, the frequency is increased by approximately three times. Increasing the frequency will decrease output impedance and ripple for higher load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the boost (pin 1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

APPLICATIONS INFORMATION

Driving the LTC1046 from an external frequency source can be easily achieved by driving pin 7 and leaving the boost pin open, as shown in Figure 6. The output current from pin 7 is small, typically 15µA, so a logic gate is capable of driving this current. The choice of using a CMOS logic gate is best because it can operate over a wide supply voltage range (3V to 15V) and has enough voltage swing to drive the internal Schmitt trigger shown in Figure 5. For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 6).

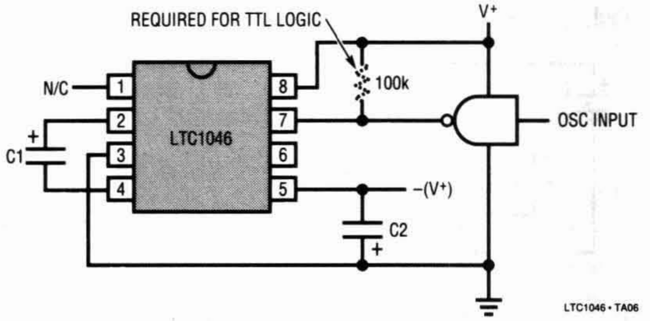


Figure 6. External Clocking

Capacitor Selection

While the exact values of C_{IN} and C_{OUT} are non-critical, good quality, low ESR capacitors such as solid tantalum are necessary to minimize voltage losses at high currents. For C_{IN} the effect of the ESR of the capacitor will be multiplied by four, due to the fact that switch currents are approximately two times higher than output current, and losses will occur on both the charge and discharge cycle. This means that using a capacitor with 1Ω of ESR for C_{IN} will have the same effect as increasing the output impedance of the LTC1046 by 4Ω. This represents a significant increase in the voltage losses. For C_{OUT} the effect of ESR is less dramatic. C_{OUT} is alternately charged and discharged at a current approximately equal to the output current, and the ESR of the capacitor will cause a step function to occur, in the output ripple, at the switch transitions. This step function will degrade the output regulation for changes in output load current, and should be avoided. Realizing that large value tantalum capacitors can be expensive, a technique that can be used is to parallel a smaller tantalum capacitor with a large aluminum electrolytic capacitor to gain both low ESR and reasonable cost. Where physical size is a concern some of the newer chip type surface mount tantalum capacitors can be used. These capacitors are normally rated at working voltages in the 10V-20V range and exhibit very low ESR (in the range of 0.1Ω).

TYPICAL APPLICATIONS

Negative Voltage Converter

Figure 7 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges without the need of any external diodes. The LV pin (pin 6) is shown grounded, but for $V^+ \geq 3V$, it may be floated, since LV is internally switched to ground (pin 3) for $V^+ \geq 3V$.

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with an 27Ω resistor. The 27Ω output impedance is composed of two terms: 1) the equivalent switched capacitor resistance (see Theory of Operation), and 2) a term related to the ON resistance of the MOS switches.

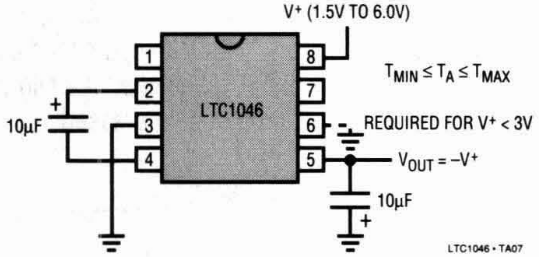


Figure 7. Negative Voltage Converter

At an oscillator frequency of 30kHz and C1 = 10µF, the first term is:

$$R_{EQUIV} = \frac{1}{\left(f_{OSC}/2\right) \times C1} =$$

$$\frac{1}{15 \times 10^3 \times 10 \times 10^{-6}} = 6.7\Omega.$$

TYPICAL APPLICATIONS

Notice that the equation for R_{EQUIV} is not an capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

The exact expression for output impedance is complex, but the dominant effect of the capacitor is clearly shown on the typical curves of output impedance and power efficiency versus frequency. For C1 = C2 = 10µF, the output impedance goes from 27Ω at f_{OSC} = 30kHz to 225Ω at f_{OSC} = 1kHz. As the 1/fC term becomes large compared to switch ON resistance term, the output resistance is determined by 1/fC only.

Voltage Doubling

Figure 8 shows a two diode, capacitive voltage doubler. With a 5V input, the output is 9.1V with no load and 8.2V with a 10mA load.

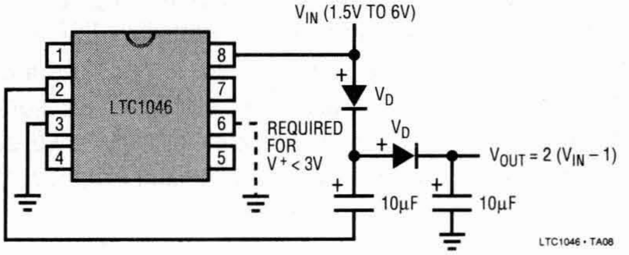

V_{IN} (1.5V TO 6V)
1
2
3
4
8
7
6
5
LTC1046
+
V_D
REQUIRED FOR $V^+ < 3V$
V_D
+
$V_{OUT} = 2 (V_{IN} - 1)$
+
10µF
+
10µF
LTC1046 • TA08

Figure 8. Voltage Doubler

Ultra-Precision Voltage Divider

An ultra-precision voltage divider is shown in Figure 9. To achieve the 0.0002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy, the load current can be increased.

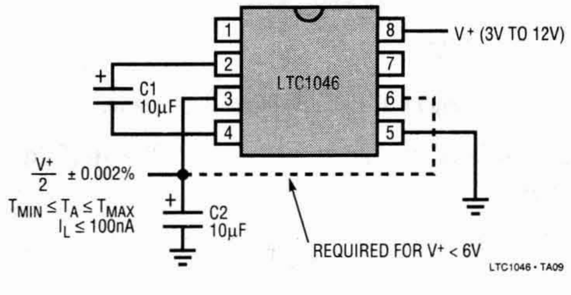

1
2
3
4
8
7
6
5
LTC1046
V^+ (3V TO 12V)
+
C1
10µF
$\frac{V^+}{2} \pm 0.002\%$
$T_{MIN} \le T_A \le T_{MAX}$
$I_L \le 100nA$
+
C2
10µF
REQUIRED FOR $V^+ < 6V$
LTC1046 • TA09

Figure 9. Ultra-Precision Voltage Divider

Battery Splitter

A common need in many systems is to obtain positive and negative supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 10 is a simple solution. It provides symmetrical positive or negative output voltages, both equal to one half the input voltage. The output voltages are both referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 is less than 6V, pin 6 should also be connected to pin 3, as shown by the dashed line.

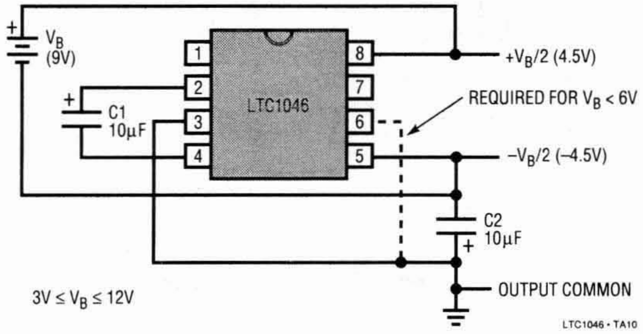

+
V_B
(9V)
1
2
3
4
8
7
6
5
LTC1046
+
C1
10µF
$+V_B/2$ (4.5V)
REQUIRED FOR $V_B < 6V$
$-V_B/2$ (–4.5V)
C2
10µF
+
OUTPUT COMMON
$3V \le V_B \le 12V$
LTC1046 • TA10

Figure 10. Battery Splitter

Paralleling for Lower Output Resistance

Additional flexibility of the LTC1046 is shown in Figures 11 and 12. Figure 11 shows two LTC1046s connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/fC1, increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Figure 12 makes use of "stacking" two LTC1046s to provide even higher voltages. In Figure 12, a negative voltage doubler or tripler can be achieved depending upon how pin 8 of the second LTC1046 is connected, as shown schematically by the switch.

TYPICAL APPLICATIONS

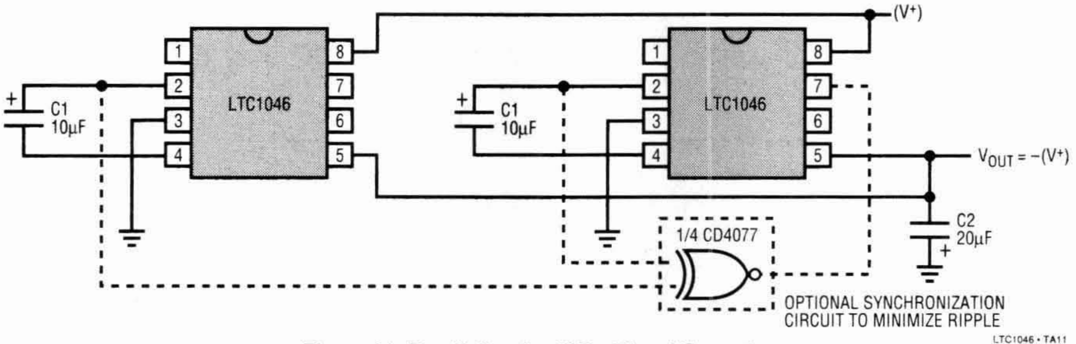

(V+)
C1
10µF
LTC1046
C1
10µF
LTC1046
V_{OUT} = −(V+)
C2
20µF
1/4 CD4077
OPTIONAL SYNCHRONIZATION
CIRCUIT TO MINIMIZE RIPPLE
LTC1046 • TA11

Figure 11. Paralleling for 100mA Load Current

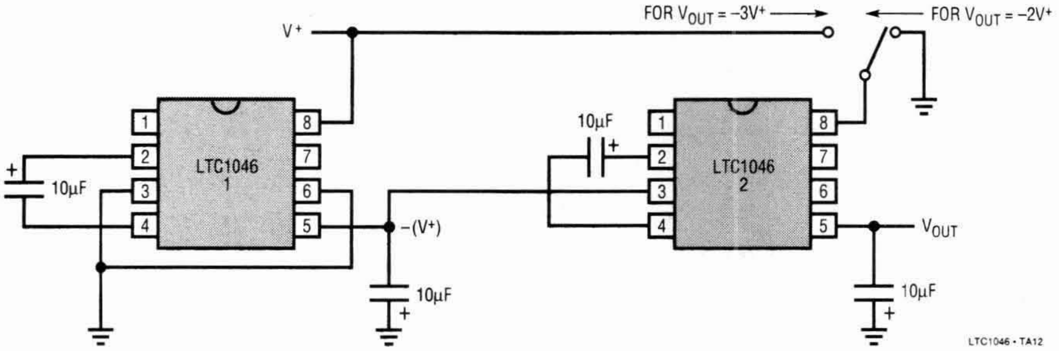

V+
FOR V_{OUT} = −3V+
FOR V_{OUT} = −2V+
10µF
LTC1046
1
−(V+)
10µF
10µF
LTC1046
2
V_{OUT}
10µF
LTC1046 • TA12

Figure 12. Stacking for Higher Voltage

NOTES

SECTION 4—POWER PRODUCTS

HIGH SIDE SWITCHES

LTC1155, Dual High Side Micropower N-Channel MOSFET Driver with Internal Charge Pump 4-26
LTC1156, Quad High Side Micropower N-Channel MOSFET Driver with Internal Charge Pump 4-41
LT1188, 1.5A High Side Switch 4-48

LTC1155

Dual High Side Micropower MOSFET Driver

FEATURES

- Fully Enhances N-Channel Power MOSFETs
- 8μA Standby Current
- 85μA ON Current
- Short Circuit Protection
- Wide Power Supply Range 4.5V to 18V
- Controlled Switching ON and OFF Times
- No External Charge Pump Components
- Replaces P-Channel High Side MOSFETs
- Compatible with Standard Logic Families
- Available in 8-Pin SO Package

APPLICATIONS

- Lap-Top Power Bus Switching
- SCSI Termination Power Switching
- Cellular Phone Power Management
- P-Channel Switch Replacement
- Relay and Solenoid Drivers
- Low Frequency Half H-Bridge
- Motor Speed and Torque Control

DESCRIPTION

The LTC1155 dual high side gate driver allows using low cost N-channel FETs for high side switching applications. An internal charge pump boosts the gate above the positive rail, fully enhancing an N-channel MOSFET with no external components. Micropower operation, with 8μA standby current and 85μA operating current, allows use in virtually all systems with maximum efficiency.

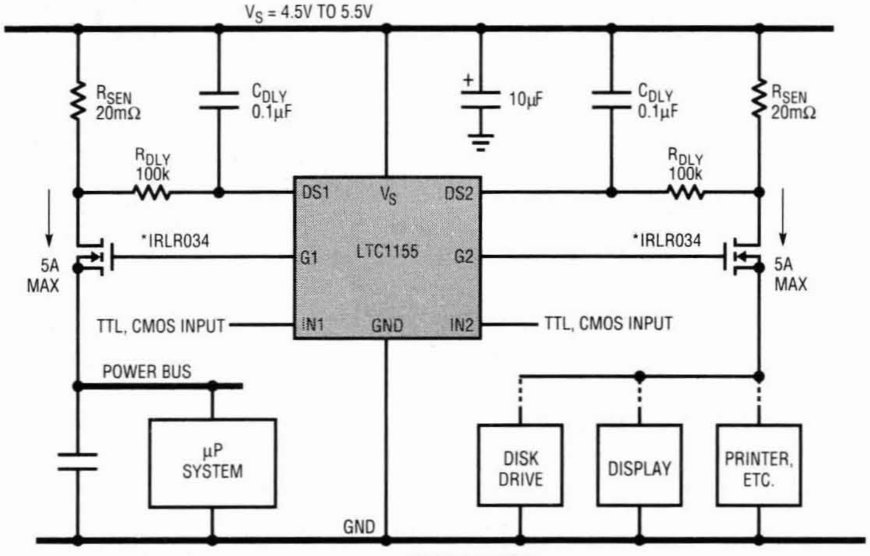
Included on-chip is over-current sensing to provide automatic shutdown in case of short circuits. A time delay can be added in series with the current sense to prevent false triggering on high in-rush loads such as capacitors and incandescent lamps.

The LTC1155 operates off of a 4.5V to 18V supply input and safely drives the gates of virtually all FETs. The LTC1155 is well suited for low voltage (battery powered) applications, particularly where micropower "sleep" operation is required.

The LTC1155 is available in both 8-pin DIP and 8-pin SO packages.

TYPICAL APPLICATION

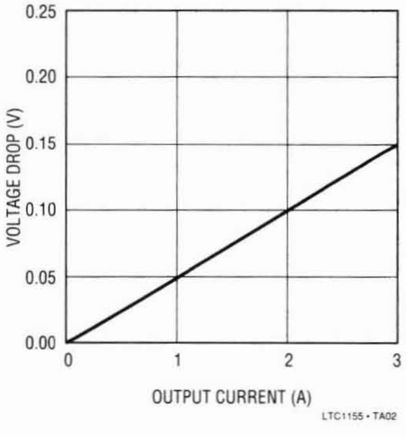
Lap-Top Computer Power Bus Switch with Short Circuit Protection



V_S = 4.5V TO 5.5V
R_{SEN} 20mΩ
C_{DLY} 0.1μF
10μF
C_{DLY} 0.1μF
R_{SEN} 20mΩ
R_{DLY} 100k
R_{DLY} 100k
DS1
V_S
DS2
*IRLR034
G1
LTC1155
G2
*IRLR034
5A MAX
5A MAX
TTL, CMOS INPUT
IN1
GND
IN2
TTL, CMOS INPUT
POWER BUS
μP SYSTEM
DISK DRIVE
DISPLAY
PRINTER, ETC.
GND
LTC1155 • TA01

*SURFACE MOUNT

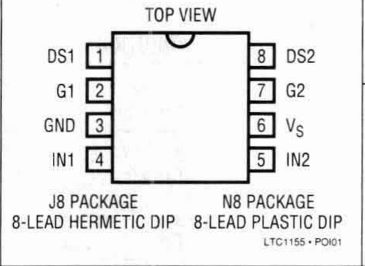
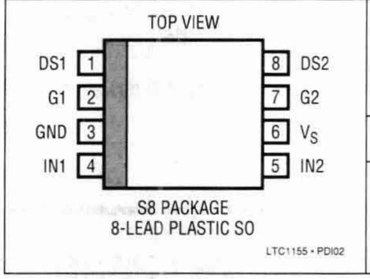
Switch Voltage Drop



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	22V
Input Voltage	(V_S +0.3V) to (GND − 0.3V)
Gate Voltage	(V_S +24V) to (GND − 0.3V)
Current (Any Pin)	50mA
Operating Temperature Range	
LTC1155M	−55°C to +125°C
LTC1155C	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature Range (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW DS1 1 G1 2 GND 3 IN1 4 8 DS2 7 G2 6 V_S 5 IN2 J8 PACKAGE 8-LEAD HERMETIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP LTC1155 • POI01	LTC1155CN8 LTC1155CJ8 LTC1155MJ8
 TOP VIEW DS1 1 G1 2 GND 3 IN1 4 8 DS2 7 G2 6 V_S 5 IN2 S8 PACKAGE 8-LEAD PLASTIC SO LTC1155 • POI02	LTC1155CS8 **S8 PART MARKING** 1155

ELECTRICAL CHARACTERISTICS V_S = 4.5V to 18V, T_A = 25°C, unless otherwise noted.

				LTC1155M			LTC1155C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_S	Supply Voltage		●	4.5		18	4.5		18	V
I_Q	Quiescent Current OFF	V_{IN} = 0V, V_S = 5V (Note 1)			8	20		8	20	µA
	Quiescent Current ON	V_S = 5V, V_{IN} = 5V (Note 2)			85	120		85	120	µA
	Quiescent Current ON	V_S = 12V, V_{IN} = 5V (Note 2)			180	400		180	400	µA
V_{INH}	Input High Voltage		●	2.0			2.0			V
V_{INL}	Input Low Voltage		●			0.8			0.8	V
I_{IN}	Input Current	0V < V_{IN} < V_S	●			±1.0			±1.0	µA
C_{IN}	Input Capacitance				5			5		pF
V_{SEN}	Drain Sense Threshold Voltage			80	100	120	80	100	120	mV
			●	75	100	125	75	100	125	mV
I_{SEN}	Drain Sense Input Current	0V < V_{SEN} < V_S				±0.1			±0.1	µA
V_{GATE}-V_S	Gate Voltage Above Supply	V_S = 5V	●	6.0	6.8	9.0	6.0	6.8	9.0	V
		V_S = 6V	●	8.0	8.5	15	8.0	8.5	15	V
		V_S = 12V	●	18	20	28	18	20	28	V
T_{ON}	Turn ON Time	V_S = 5V, C_{GATE} = 1000pF								
		Time for V_{GATE} > V_S +2V		50	160	300	50	160	300	µs
		Time for V_{GATE} > V_S +5V		200	580	1000	200	580	1000	µs
		V_S = 12V, C_{GATE} = 1000pF								
		Time for V_{GATE} > V_S +5V		50	100	200	50	100	200	µs
		Time for V_{GATE} > V_S +10V		120	250	500	120	250	500	µs

ELECTRICAL CHARACTERISTICS V_S = 4.5V to 18V, T_A = 25°C, unless otherwise noted.

				LTC1155M			LTC1155C			
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{OFF}	Turn OFF Time	V_S = 5V, C_{GATE} = 1000pF Time for V_{GATE} < 1V		10	36	60	10	36	60	µs
		V_S = 12V, C_{GATE} = 1000pF Time for V_{GATE} < 1V		10	26	60	10	26	60	µs
T_{SC}	Short Circuit Turn OFF Time	V_S = 5V, C_{GATE} = 1000pF Time for V_{GATE} < 1V		5	16	30	5	16	30	µs
		V_S = 12V, C_{GATE} = 1000pF Time for V_{GATE} < 1V		5	16	30	5	16	30	µs

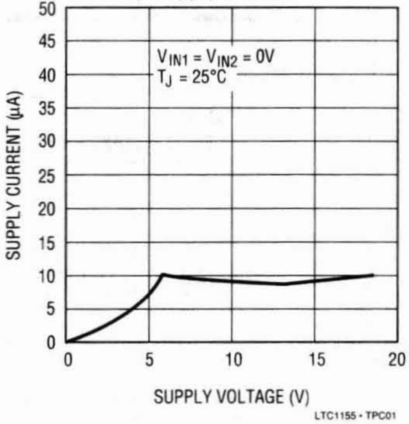
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Quiescent current OFF is for both channels in OFF condition.

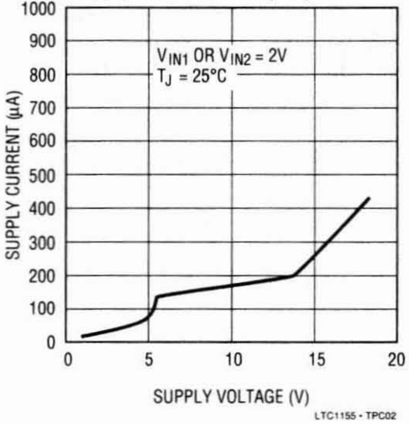
Note 2: Quiescent current ON is per driver and is measured independently.

TYPICAL PERFORMANCE CHARACTERISTICS

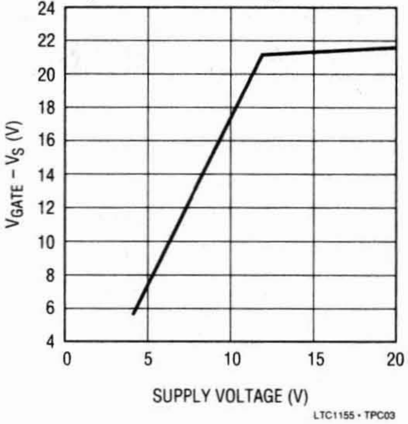
Standby Supply Current



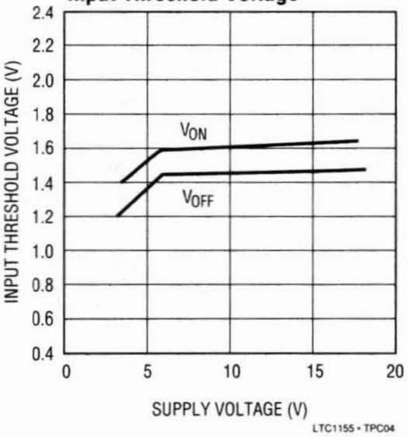
Supply Current/Side (ON)



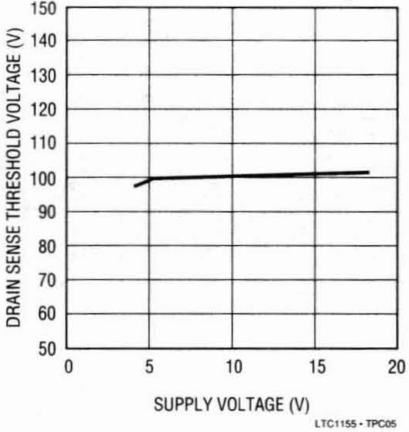
High Side Gate Voltage



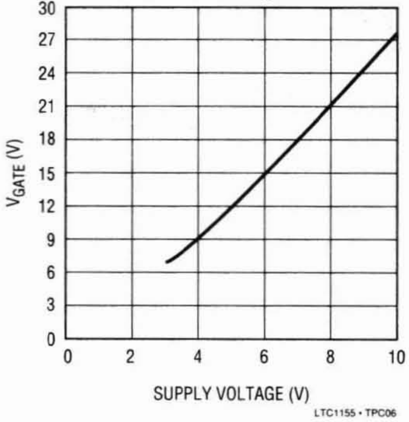
Input Threshold Voltage



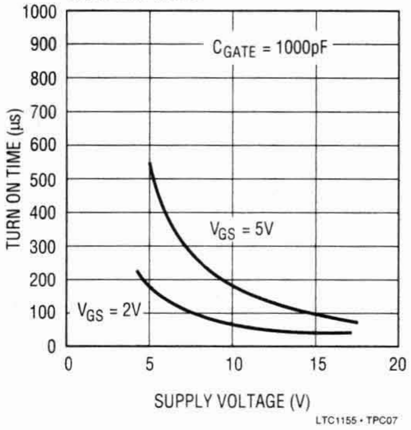
Drain Sense Threshold Voltage

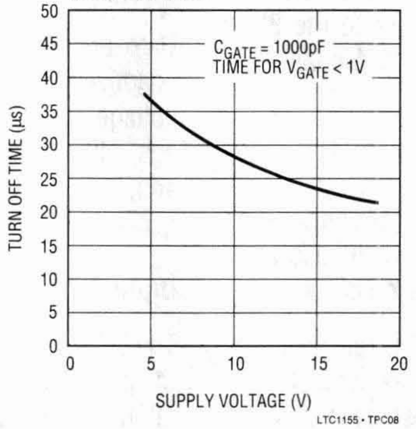


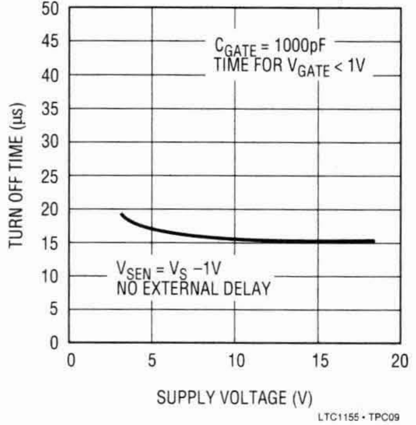
Low Side Gate Voltage

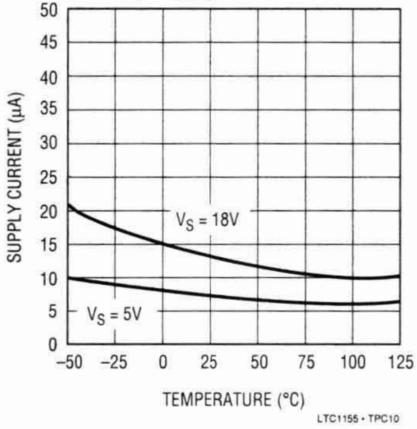


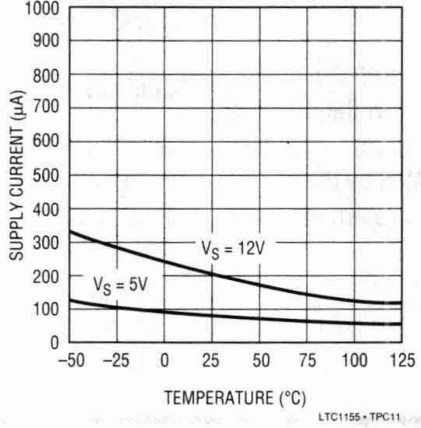
TYPICAL PERFORMANCE CHARACTERISTICS

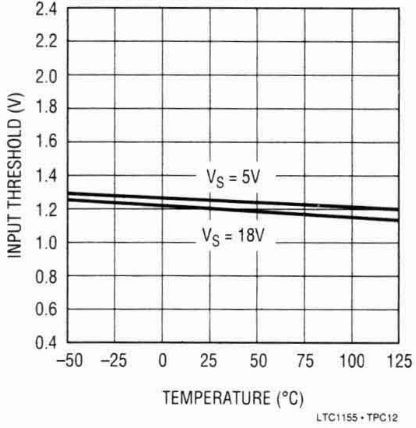

Turn ON Time


Turn OFF Time

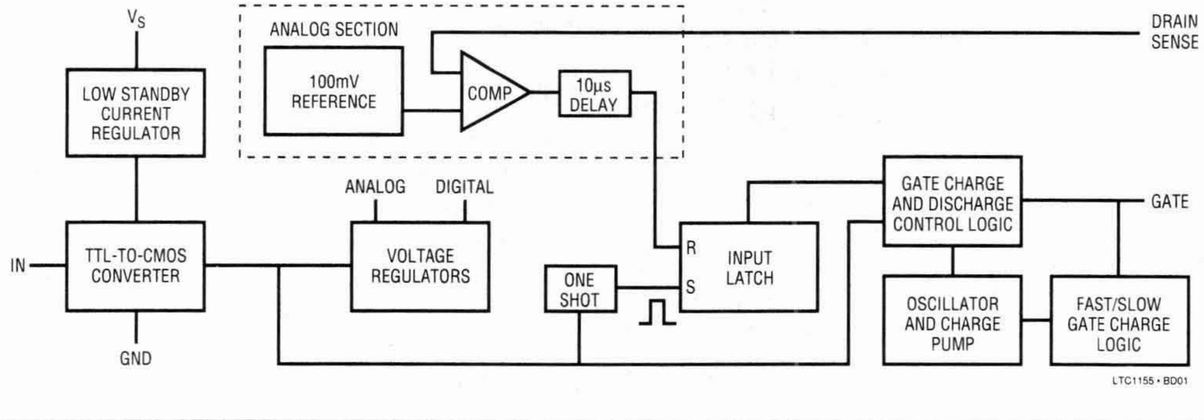

Short Circuit Turn OFF Delay Time


Standby Supply Current


Supply Current Per Side (ON)


Input ON Threshold

BLOCK DIAGRAM


V_S
LOW STANDBY CURRENT REGULATOR
ANALOG SECTION
100mV REFERENCE
COMP
10µs DELAY
DRAIN SENSE
ANALOG
DIGITAL
GATE CHARGE AND DISCHARGE CONTROL LOGIC
GATE
IN
TTL-TO-CMOS CONVERTER
VOLTAGE REGULATORS
R
S
INPUT LATCH
ONE SHOT
OSCILLATOR AND CHARGE PUMP
FAST/SLOW GATE CHARGE LOGIC
GND
LTC1155 • BD01

LTC1155 OPERATION

The LTC1155 contains two independent power MOSFET gate drivers and protection circuits (refer to the Block Diagram for details). Each half of the LTC1155 consists of the following functional blocks:

TTL and CMOS Compatible Inputs

Each driver input has been designed to accommodate a wide range of logic families. The input threshold is set at 1.3V with approximately 100mV of hysteresis.

A voltage regulator with low standby current provides continuous bias for the TTL to CMOS converters. The TTL to CMOS converter output enables the rest of the circuitry. In this way the power consumption is kept to a minimum in the standby mode.

Internal Voltage Regulation

The output of the TTL to CMOS converter drives two regulated supplies which power the low voltage CMOS logic and analog blocks. The regulator outputs are isolated from each other so that the noise generated by the charge pump logic is not coupled into the 100mV reference or the analog comparator.

Gate Charge Pump

Gate drive for the power MOSFET is produced by an adaptive charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on chip and, therefore, no external components are required to generate the gate drive.

Drain Current Sense

The LTC1155 is configured to sense the drain current of the power MOSFET in high side applications. An internal 100mV reference is compared to the drop across a sense resistor (typically 0.002Ω to 0.1Ω) in series with the drain lead. If the drop across this resistor exceeds the internal 100mV threshold, the input latch is reset and the gate is quickly discharged by a large N-channel transistor.

Controlled Gate Rise and Fall Times

When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions in normal operation. If a short circuit or current overload condition is encountered, the gate is discharged very quickly (typically a few microseconds) by a large N-channel transistor.

PIN DESCRIPTIONS

Input Pin

The LTC1155 logic input is a high impedance CMOS gate and should be grounded when not in use. These input pins have ESD protection diodes to ground and supply and, therefore, should not be forced beyond the power supply rails.

Gate Drive Pin

The gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is a relatively high impedance when driven above the rail (the equivalent of a few hundred kΩ). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin

The supply pin of the LTC1155 serves two vital purposes. The first is obvious: it powers the input, gate drive, regulation and protection circuitry. The second purpose is less obvious: it provides a Kelvin connection to the top of the two drain sense resistors for the internal 100mV reference. The supply pin should be connected directly to the power supply source as close as possible to the top of the two sense resistors.

PIN DESCRIPTIONS

The supply pin of the LTC1155 should not be forced below ground as this may result in permanent damage to the device. A 300Ω resistor should be inserted in series with the ground pin if negative supply voltages are anticipated.

Drain Sense Pin

As noted previously, the drain sense pin is compared against the supply pin voltage. If the voltage at this pin is more than 100mV below the supply pin, the input latch will be reset and the MOSFET gate will be quickly discharged. Cycle the input to reset the short circuit latch and turn the MOSFET back on.

This pin is also a high impedance CMOS gate with ESD protection and, therefore, should not be forced beyond the power supply rails. To defeat the over current protection, short the drain sense to supply.

Some loads, such as large supply capacitors, lamps or motors require high inrush currents. An RC time delay must be added between the sense resistor and the drain sense pin to ensure that the drain sense circuitry does not false trigger during start-up. This time constant can be set from a few microseconds to many seconds. However, very long delays may put the MOSFET in risk of being destroyed by a short circuit condition (see Applications Information section).

APPLICATIONS INFORMATION

Protecting the MOSFET

The MOSFET is protected against destruction by removing drive from the gate as soon as an over current condition is detected. Resistive and inductive loads can be protected with no external time delay. Large capacitive or lamp loads, however, require that the over current shutdown function be delayed long enough to start the load but short enough to ensure the safety of the MOSFET.

Example Calculations

Consider the circuit of Figure 1. A power MOSFET is driven by one side of an LTC1155 to switch a high inrush current load. The drain sense resistor is selected to limit the maximum DC current to 3.3A.

$$R_{SEN} = V_{SEN}/I_{TRIP}$$

$$= 0.1/3.3A$$

$$= 30m\Omega$$

A time delay is introduced between R_{SEN} and the drain sense pin of the LTC1155 which provides sufficient delay to start a high inrush load such as large supply capacitors.

In this example circuit, we have selected the IRLZ34 because of its low RDS_{ON} (0.05Ω with VGS = 5V). The FET drops 0.1V at 2A and, therefore, dissipates 200mW in normal operation (no heat sinking required).

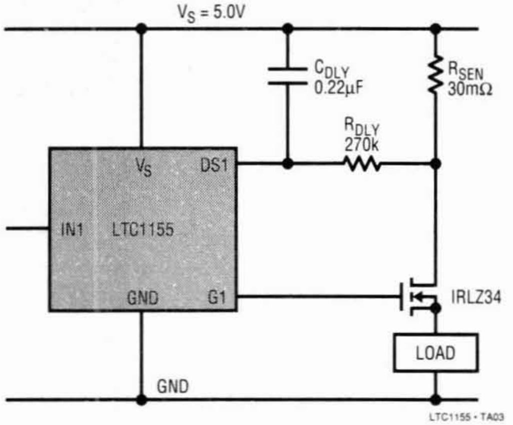


Figure 1. Adding an RC Delay

If the output is shorted to ground, the current through the FET rises rapidly and is limited by the RDS_{ON} of the FET, the drain sense resistor and the series resistance between the power supply and the FET. Series resistance in the power supply can be substantial and attributed to many sources including harness wiring, PCB traces, supply capacitor ESR, transformer resistance or battery resistance.

APPLICATIONS INFORMATION

For this example, we assume a worst case scenario; i.e. that the power supply to the power MOSFET is "hard" and provides a constant 5V regardless of the current. In this case, the current is limited by the RDS_{ON} of the MOSFET and the drain sense resistance. Therefore:

$$I_{PEAK} = V_{SUPPLY}/0.08\Omega$$
$$= 62.5A$$

The drop across the drain sense resistor under these conditions is much larger than 100mV and is equal to the drain current times the sense resistance:

$$V_{DROP} = (I_{PEAK})(R_{SEN})$$
$$= 1.88V$$

By consulting the power MOSFET data sheet SOA graph, we note that the IRLZ34 is capable of delivering 62.5A at a drain-to-source voltage of 3.12V for approximately 10ms.

An RC time constant can now be calculated which satisfies this requirement:

$$RC = \frac{-t}{\ln\left[1 - \frac{V_{SEN}}{R_{SEN} \bullet I_{MAX}}\right]}$$

$$RC = \frac{-0.01}{\ln\left[1 - \frac{0.10}{0.030 \bullet 62.5}\right]}$$

$$= -0.01/-0.054$$

$$= 182ms$$

This time constant should be viewed as a maximum safe delay time and should be reduced if the competing requirement of starting a high inrush current load is less stringent; i.e., if the inrush time period is calculated at 20ms, the RC time constant should be set at roughly two or three times this time period and not at the maximum of 182ms. A 60ms time constant would be produced with a 270k resistor and a 0.22µF capacitor (as shown in Figure 1).

Graphical Approach to Selecting R_{DLY} and C_{DLY}

Figure 2 is a graph of normalized over-current shutdown time versus normalized MOSFET current. This graph can be used instead of the above equation to calculate the RC time constant. The Y axis of the graph is normalized to one RC time constant. The X axis is normalized to the set current. (The set current is defined as the current required to develop 100mV across the drain sense resistor).

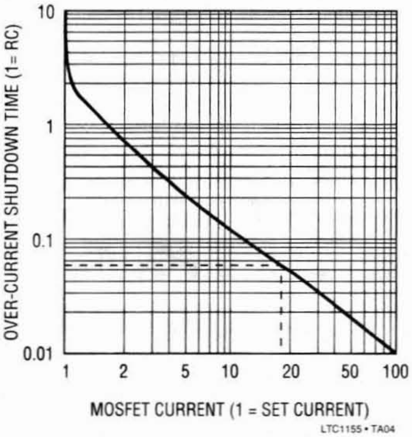


Figure 2. Shutdown Time vs MOSFET Current

Note that the shutdown time is shorter for increasing levels of MOSFET current. This ensures that the total energy dissipated by the MOSFET is always within the bounds established by the MOSFET manufacturer for safe operation.

In the example presented above, we established that the power MOSFET should not be allowed to pass 62.5A for more than 10ms. 62.5A is roughly 18 times the set current of 3.3A. By drawing a line up from 18 and reflecting it off the curve, we establish that the RC time constant should be set at 10ms divided by 0.054, or 180ms. Both methods result in the same conclusion.

Using a Speed Up Diode

A way to further reduce the amount of time that the power MOSFET is in a short circuit condition is to "bypass" the delay resistor with a small signal diode as shown in Figure 3. The diode will engage when the drop across the drain sense resistor exceeds 0.7V, providing a direct path to the sense pin and dramatically reducing the amount of time

APPLICATIONS INFORMATION

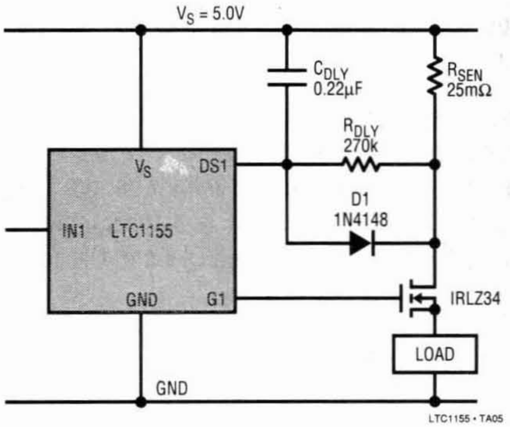


Figure 3. Using a Speed-Up Diode

the MOSFET is in an overload condition. The drain sense resistor value is selected to limit the maximum DC current to 4A. Above 28A, the delay time drops to 10µs.

Switched Supply Applications

Large inductive loads, such as solenoids, relays and motors store energy which must be directed back to either the power supply or to ground when the supply voltage is interrupted (see Figure 4). In normal operation, when the switch is turned OFF, the energy stored in the inductor is harmlessly absorbed by the MOSFET; i.e., the current flows out of the supply through the MOSFET until the inductor current fails to zero.

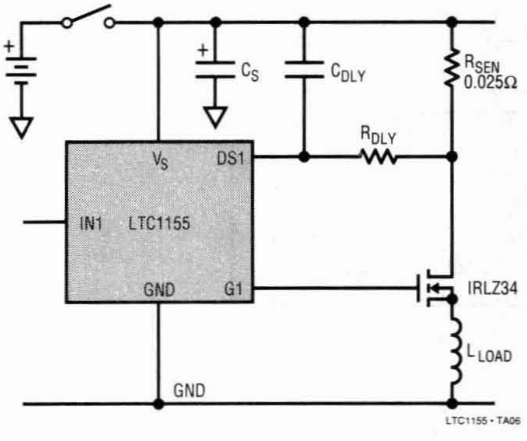


Figure 4. Switched Supply

If the MOSFET is turned ON and the power supply (battery) removed, the inductor current is delivered by the supply capacitor. The supply capacitor must be large enough to deliver the energy demanded by the discharging inductor. *If the storage capacitor is too small, the supply lead of the LTC1155 may be pulled below ground, permanently destroying the device.*

Consider the case of a load inductance of 1mH which is supporting 3A when the 6V power supply connection is interrupted. A supply capacitor of at least 250µF is required to prevent the supply lead of the LTC1155 from being pulled below ground (along with any other circuitry tied to the supply).

Any wire between the power MOSFET source and the load will add a small amount of parasitic inductance in series with the load (approximately 0.4µH/foot). Bypass the power supply lead of the LTC1155 with a minimum of 10µF to ensure that this parasitic load inductance is discharged safely, even if the load is otherwise resistive.

Large Inductive Loads

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating should be connected across the load to safely divert the stored energy.

Reverse Battery Protection

The LTC1155 can be protected against reverse battery conditions by connecting a resistor in series with the ground lead as shown in Figure 5. The resistor limits the supply current to less than 50mA with –12V applied. Since the LTC1155 draws very little current while in normal operation, the drop across the ground resistor is minimal.

The TTL or CMOS driving logic is protected against reverse battery conditions by the 100k input current limiting resistor. The addition of 100k resistance in series with the input pin will not affect the turn ON and turn OFF times which are dominated by the controlled gate charge and discharge periods.

APPLICATIONS INFORMATION

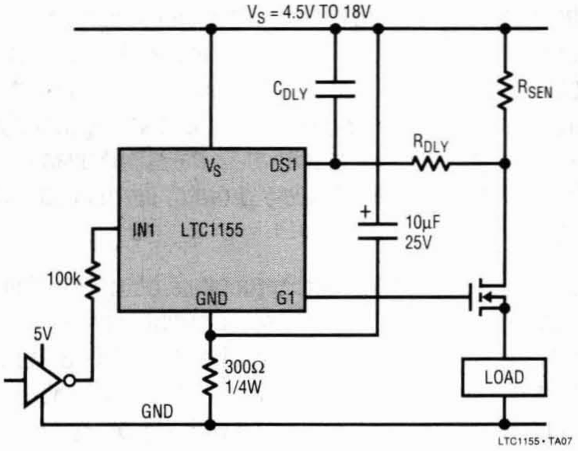

V_S = 4.5V TO 18V
C_{DLY}
R_{SEN}
R_{DLY}
V_S
DS1
IN1
LTC1155
GND
G1
10μF
25V
100k
5V
300Ω
1/4W
LOAD
GND
LTC1155 • TA07

Figure 5. Reverse Battery Protection

Over Voltage Protection

The MOSFET and load can be protected against over voltage conditions by using the circuit of Figure 6. The drain sense function is used to detect an over voltage condition and quickly discharge the power MOSFET gate. The 18V zener diode conducts when the supply voltage exceeds 18.6V and pulls the drain sense pin 0.6V below the supply pin voltage.

The supply voltage is limited to 18.6V and the gate drive is immediately removed from the MOSFET to ensure that it cannot conduct during the over voltage period. The gate of the MOSFET will be latched OFF until the supply transient is removed and the input turned OFF and ON again.

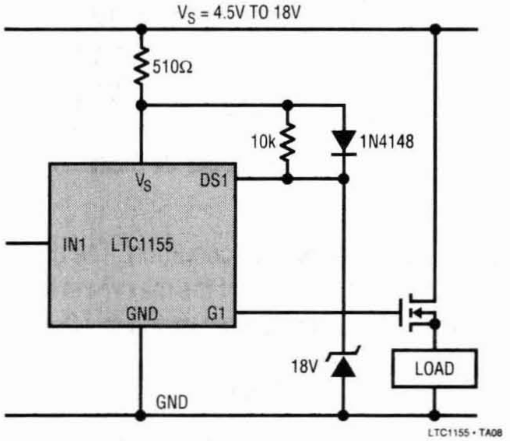
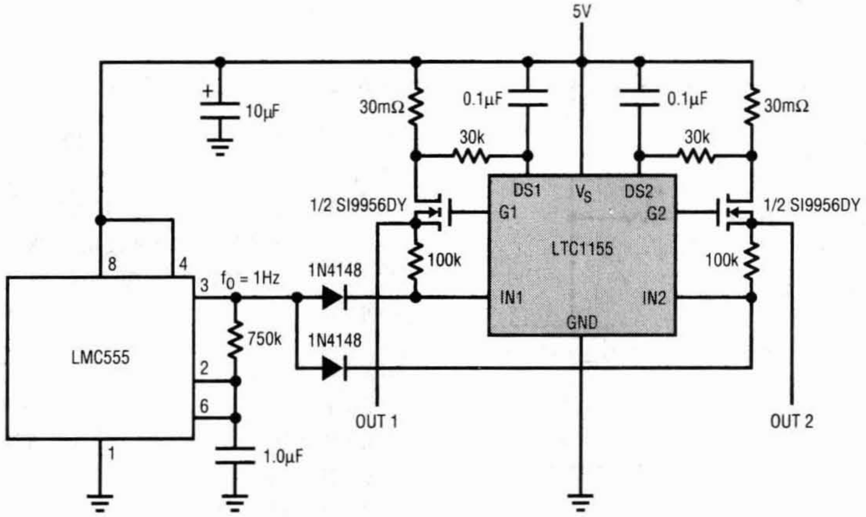

V_S = 4.5V TO 18V
510Ω
10k
1N4148
V_S
DS1
IN1
LTC1155
GND
G1
18V
LOAD
GND
LTC1155 • TA08

Figure 6. Over Voltage Shutdown and Protection

TYPICAL APPLICATIONS

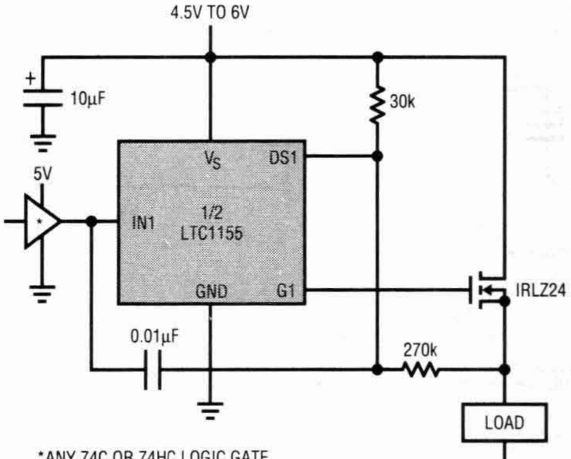
Dual 2A Auto-Reset Electronic Fuse


5V
10μF
30mΩ*
0.1μF
0.1μF
30mΩ*
30k
30k
1/2 SI9956DY
1/2 SI9956DY
DS1
V_S
DS2
G1
G2
LTC1155
IN1
IN2
GND
100k
100k
8
4
3
f_O = 1Hz
1N4148
1N4148
750k
LMC555
2
6
1
1.0μF
OUT 1
OUT 2
LTC1155 • TA09

ALL COMPONENTS SHOWN ARE SURFACE MOUNT.
*STR101G TECHNO (818) 781-1642

TYPICAL APPLICATIONS

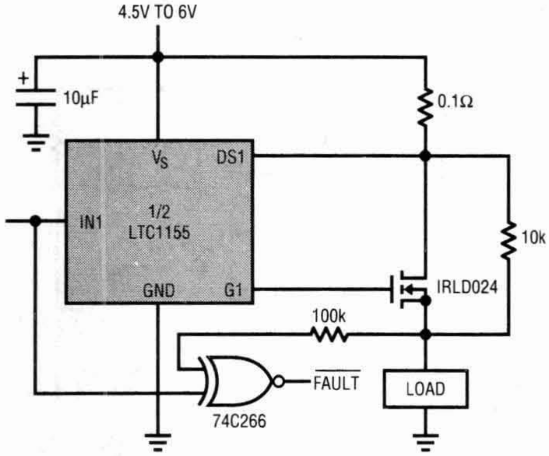
High Side Driver with V_{DS} Sense Short Circuit Shutdown


4.5V TO 6V
10μF
30k
5V
*
V_S
DS1
IN1
1/2
LTC1155
GND
G1
IRLZ24
0.01μF
270k
LOAD

*ANY 74C OR 74HC LOGIC GATE.
MOSFET SHUTS DOWN IF $V_{DS} > 1V$

LTC1155 • TA10

X-NOR Fault Detection

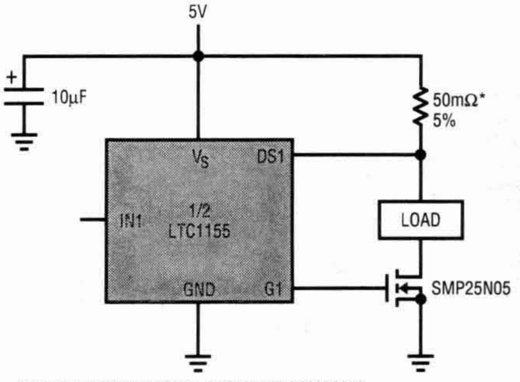

4.5V TO 6V
10μF
0.1Ω
V_S
DS1
IN1
1/2
LTC1155
GND
G1
10k
IRLD024
100k
$\overline{FAULT}$
74C266
LOAD

LTC1155 • TA11

Truth Table

IN	OUT	CONDITION	$\overline{FLT}$
0	0	Switch OFF	1
1	0	Short Circuit	0
0	1	Open Load	0
1	1	Switch ON	1

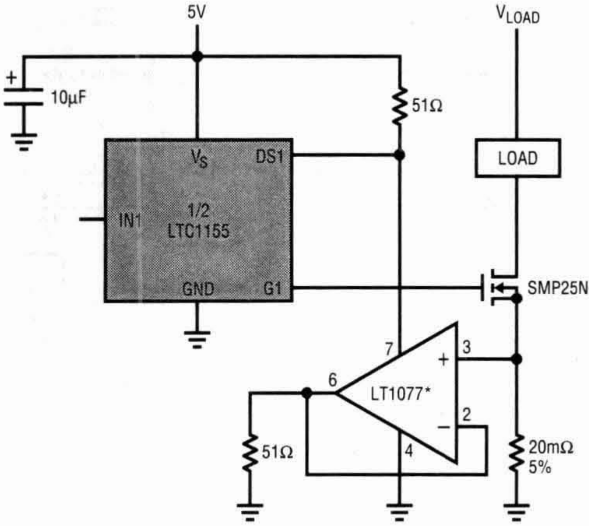
Low Side Driver with Drain End Current Sensing


5V
10μF
50mΩ*
5%
V_S
DS1
IN1
1/2
LTC1155
GND
G1
LOAD
SMP25N05

*MSM-1 INTERNATIONAL RESISTIVE COMPANY
(704) 264-8861

LTC1155 • TA12

Low Side Driver with Source End Current Sensing

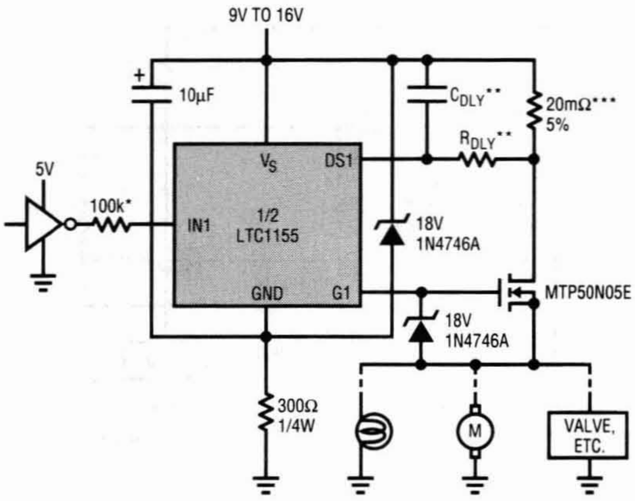

5V
V_{LOAD}
10μF
51Ω
V_S
DS1
IN1
1/2
LTC1155
GND
G1
LOAD
SMP25N05
7
3
6
LT1077*
2
4
51Ω
20mΩ
5%

*DO NOT SUBSTITUTE. MUST BE A PRECISION, SINGLE
SUPPLY, MICROPOWER OP AMP ($I_Q < 60μA$)

LTC1155 • TA13

TYPICAL APPLICATIONS

Automotive High Side Driver with Reverse Battery and High Voltage Transient Protection


9V TO 16V
+
10µF
C_{DLY}**
20mΩ***
5%
R_{DLY}**
5V
100k*
V_S
DS1
IN1
1/2
LTC1155
18V
1N4746A
GND
G1
MTP50N05E
18V
1N4746A
300Ω
1/4W
M
VALVE,
ETC.

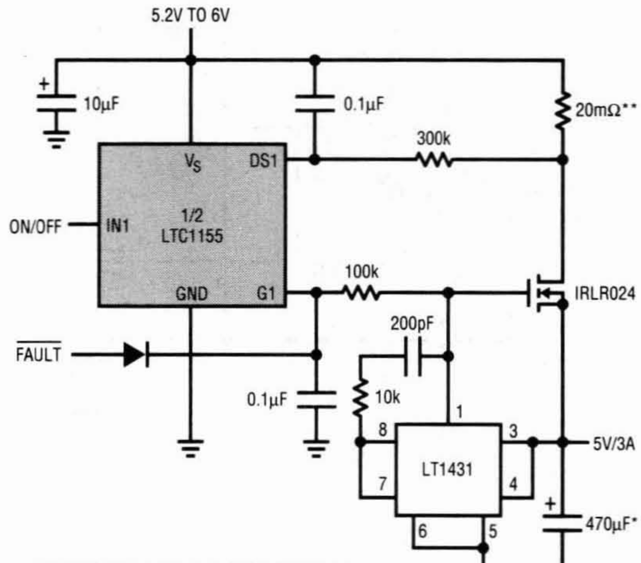
*PROTECTS TTL/CMOS GATES DURING HIGH VOLTAGE TRANSIENT OR REVERSE BATTERY

**NOT REQUIRED FOR INDUCTIVE OR RESISTIVE LOADS

***SMV ISOTEK CORPORATION (508) 673-2900

LTC1155 • TA14

5V/3A Extremely Low Voltage Drop Regulator with 10µA Standby Current and Short Circuit Protection

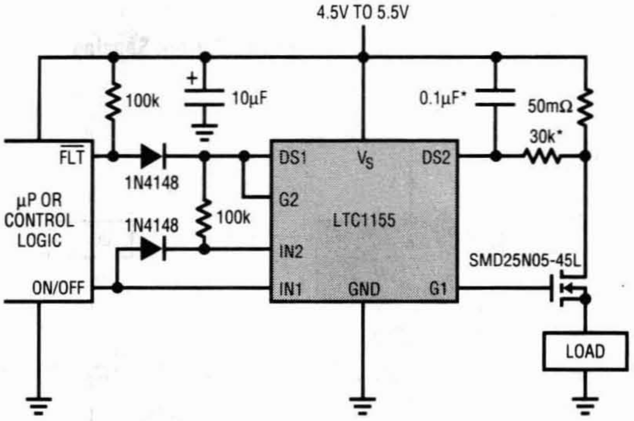

5.2V TO 6V
+
10µF
0.1µF
20mΩ**
300k
V_S
DS1
ON/OFF
IN1
1/2
LTC1155
100k
GND
G1
IRLR024
200pF
$\overline{FAULT}$
0.1µF
10k
1
8
3
5V/3A
LT1431
7
4
+
470µF*
6
5

*CAPACITOR ESR SHOULD BE LESS THAN 0.5Ω

**STR101G TECHNO (818) 781-1642

LTC1155 • TA15

Using the Second Channel for Fault Detection

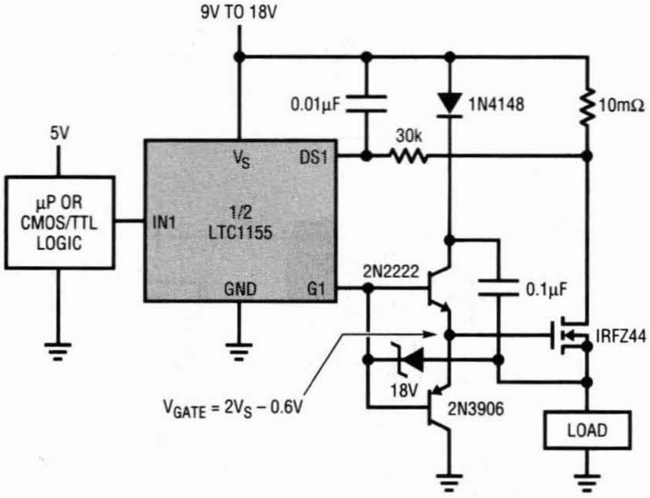

4.5V TO 5.5V
100k
+
10µF
0.1µF*
50mΩ
30k*
$\overline{FLT}$
1N4148
DS1
V_S
DS2
G2
µP OR
CONTROL
LOGIC
1N4148
100k
LTC1155
IN2
SMD25N05-45L
ON/OFF
IN1
GND
G1
LOAD

NOTE:
DRAIN SENSE 2 IS USED TO DETECT A FAULT IN CHANNEL 1. GATE 2 PULLS DOWN ON DRAIN SENSE 1 TO DISCHARGE THE MOSFET AND REPORT THE FAULT TO THE µP

*NOT REQUIRED FOR RESISTIVE OR INDUCTIVE LOADS

LTC1155 • TA16

Bootstrapped Gate Drive for (100Hz < F_0 < 10kHz)

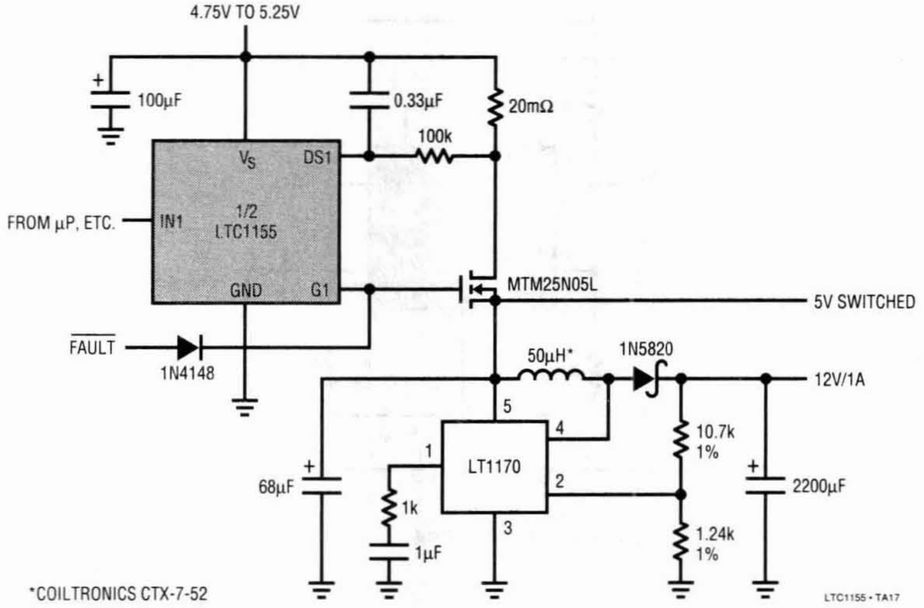

9V TO 18V
0.01µF
1N4148
10mΩ
5V
30k
V_S
DS1
µP OR
CMOS/TTL
LOGIC
IN1
1/2
LTC1155
2N2222
GND
G1
0.1µF
IRFZ44
18V
$V_{GATE} = 2V_S - 0.6V$
2N3906
LOAD

RISE AND FALL TIMES ARE βETA TIMES FASTER

LTC1155 • TA22

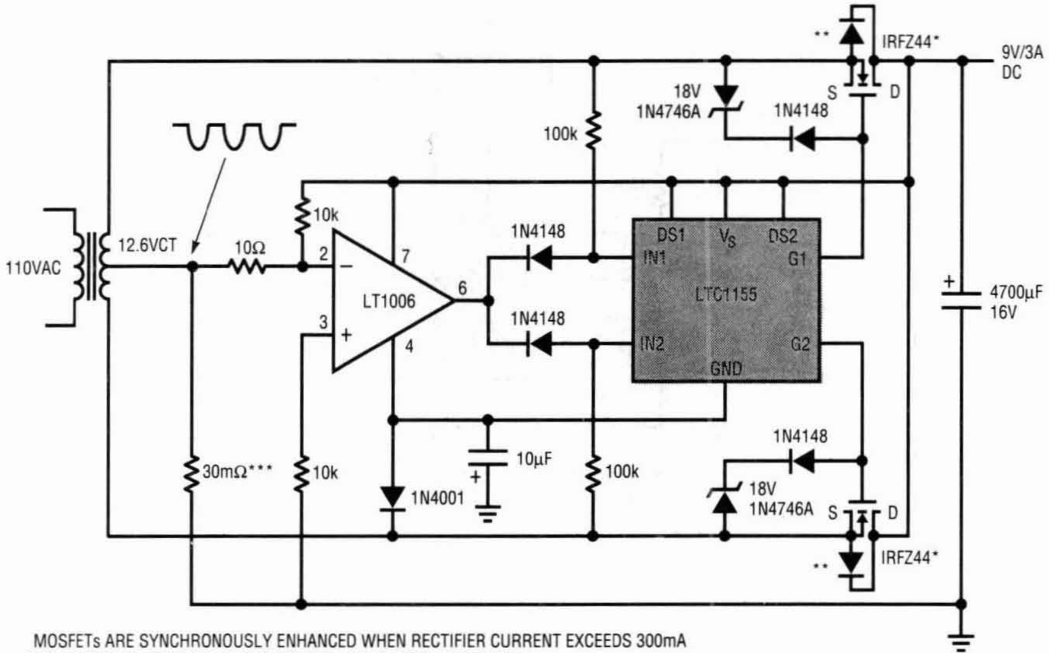
TYPICAL APPLICATIONS

Logic Controlled Boost Mode Switching Regulator with Short Circuit Protection and 8μA Standby Current


4.75V TO 5.25V
100μF
0.33μF
20mΩ
100k
V_S
DS1
FROM μP, ETC.
IN1
1/2 LTC1155
GND
G1
MTM25N05L
5V SWITCHED
FAULT
1N4148
50μH*
1N5820
12V/1A
5
4
1
LT1170
2
3
68μF
1k
1μF
10.7k 1%
1.24k 1%
2200μF
LTC1155 • TA17

*COILTRONICS CTX-7-52

High Efficiency 60Hz Full-Wave Synchronous Rectifier


**
IRFZ44*
9V/3A DC
18V 1N4746A
1N4148
S
D
100k
110VAC
12.6VCT
10Ω
10k
2
7
LT1006
6
3
4
1N4148
1N4148
DS1
V_S
DS2
IN1
G1
LTC1155
IN2
G2
GND
4700μF 16V
1N4148
30mΩ***
10k
1N4001
10μF
100k
18V 1N4746A
S
D
IRFZ44*
**
LTC1155 • TA18

MOSFETs ARE SYNCHRONOUSLY ENHANCED WHEN RECTIFIER CURRENT EXCEEDS 300mA

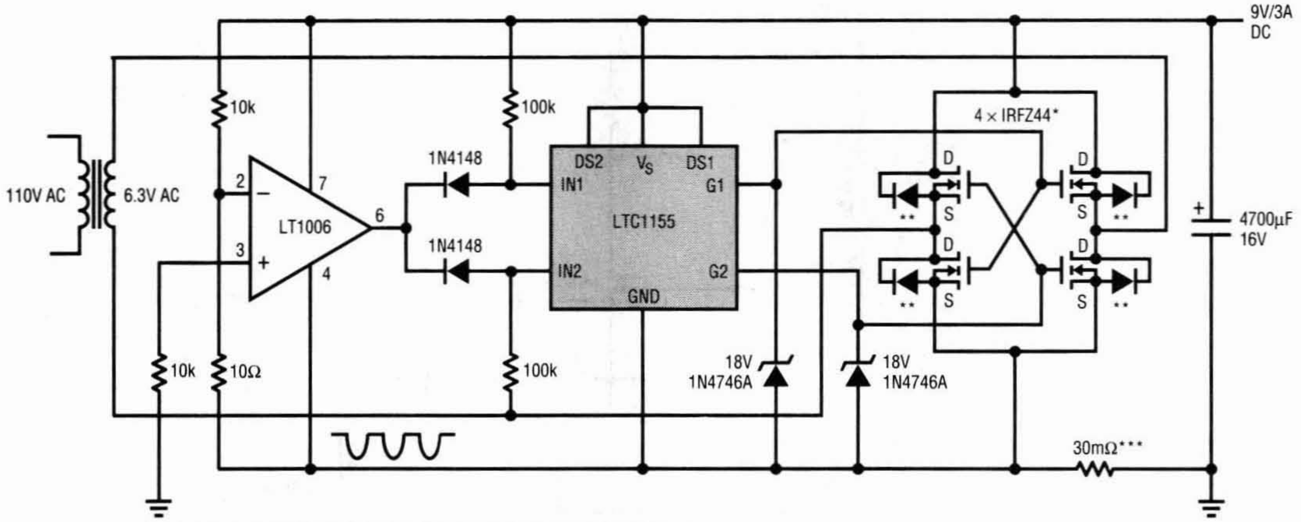
*NO HEATSINK REQUIRED. CASES (DRAINS) CAN BE TIED TOGETHER

**INTERNAL BODY DIODE OF MOSFET

***RCS02 ULTRONIX (303) 242-0810

TYPICAL APPLICATIONS

High Efficiency 60Hz Full-Wave Synchronous Rectifier


9V/3A
DC
10k
100k
4 × IRFZ44*
110V AC
6.3V AC
2
7
LT1006
6
3
4
1N4148
1N4148
DS2
V_S
DS1
IN1
G1
LTC1155
IN2
G2
GND
D
S
**
4700µF
16V
10k
10Ω
100k
18V
1N4746A
18V
1N4746A
30mΩ***

MOSFETs ARE SYNCHRONOUSLY ENHANCED WHEN RECTIFIER CURRENT EXCEEDS 300mA

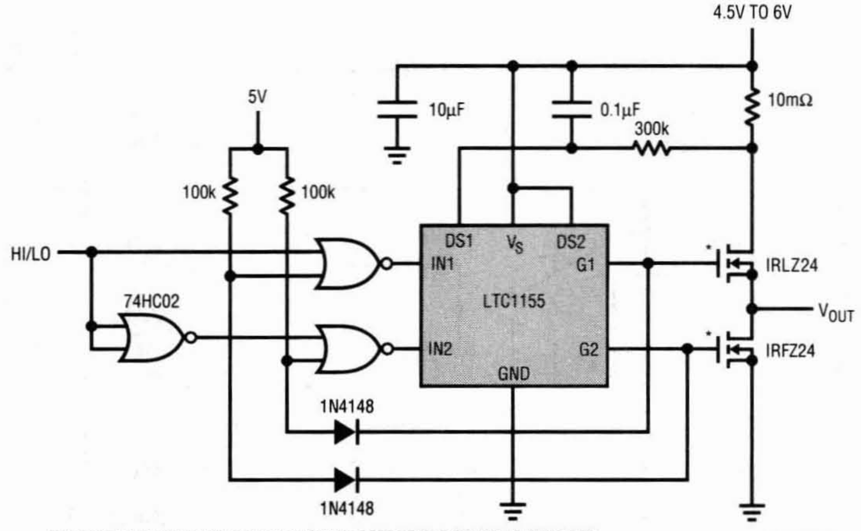
*NO HEATSINK REQUIRED

**INTERNAL BODY DIODE OF MOSFET

***RCS02 ULTRONIX (303) 242-0810

LTC1155 • TA19

Push-Pull Driver with Shoot-Through Current Lockout (F_O < 100Hz)

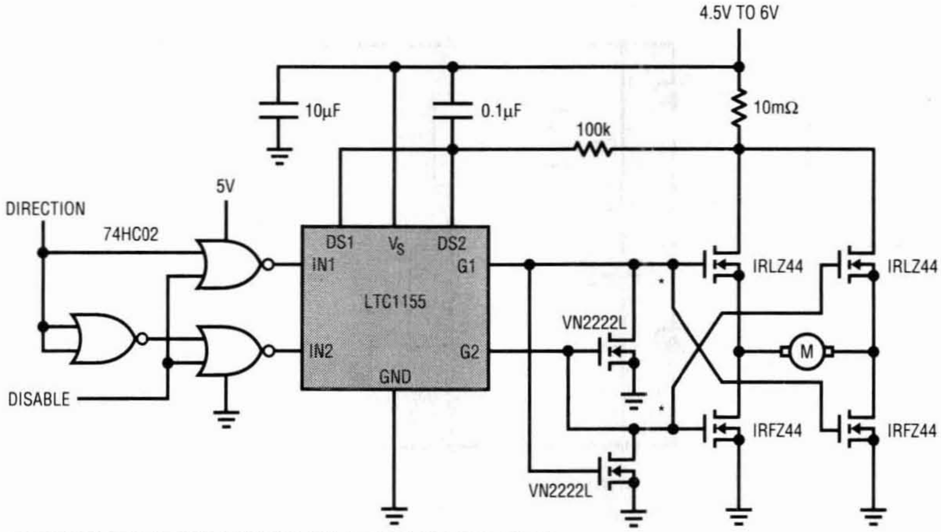

4.5V TO 6V
5V
10µF
0.1µF
10mΩ
300k
100k
100k
HI/LO
74HC02
DS1
V_S
DS2
IN1
G1
LTC1155
IN2
G2
GND
*
IRLZ24
V_{OUT}
*
IRFZ24
1N4148
1N4148

*OPPOSING GATE MUST DROP BELOW 2V BEFORE THE OTHER IS CHARGED

LTC1155 • TA20

TYPICAL APPLICATIONS

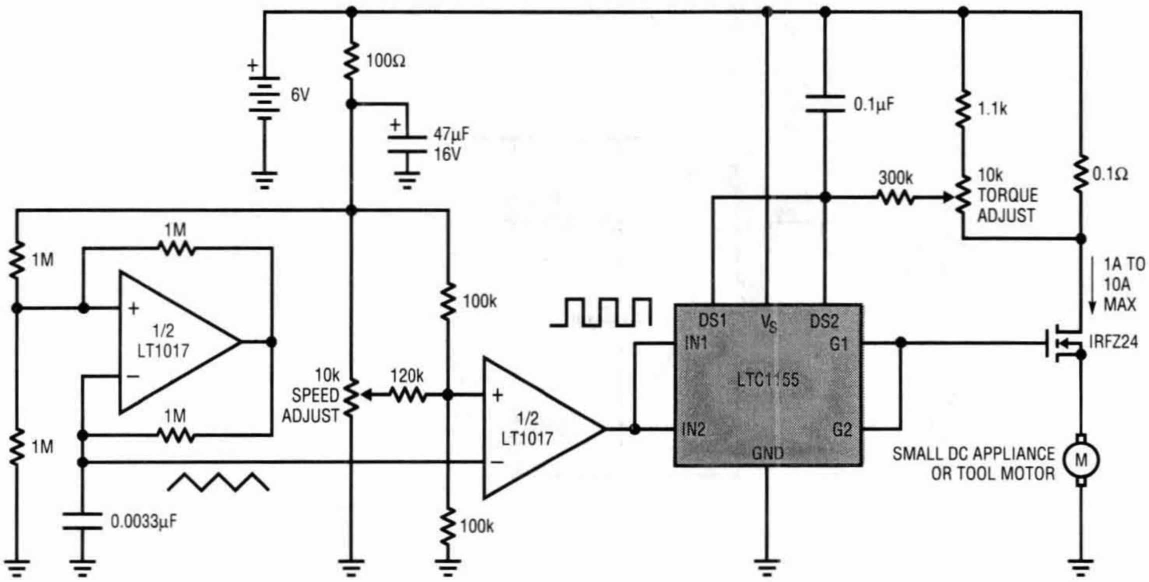
Full H-Bridge Driver with Shoot-Through Current Lockout and Stall Current Shutdown (F_O < 100Hz)


4.5V TO 6V
10μF
0.1μF
10mΩ
100k
5V
DIRECTION
74HC02
DISABLE
DS1
V_S
DS2
IN1
G1
LTC1155
IN2
G2
GND
VN2222L
VN2222L
IRLZ44
IRLZ44
IRFZ44
IRFZ44
M
*
*

*OPPOSING GATES ARE HELD OFF UNTIL OTHER GATES DROP BELOW 1.5V

LTC1155 • TA21

DC Motor Speed and Torque Control for Cordless Tools and Appliances

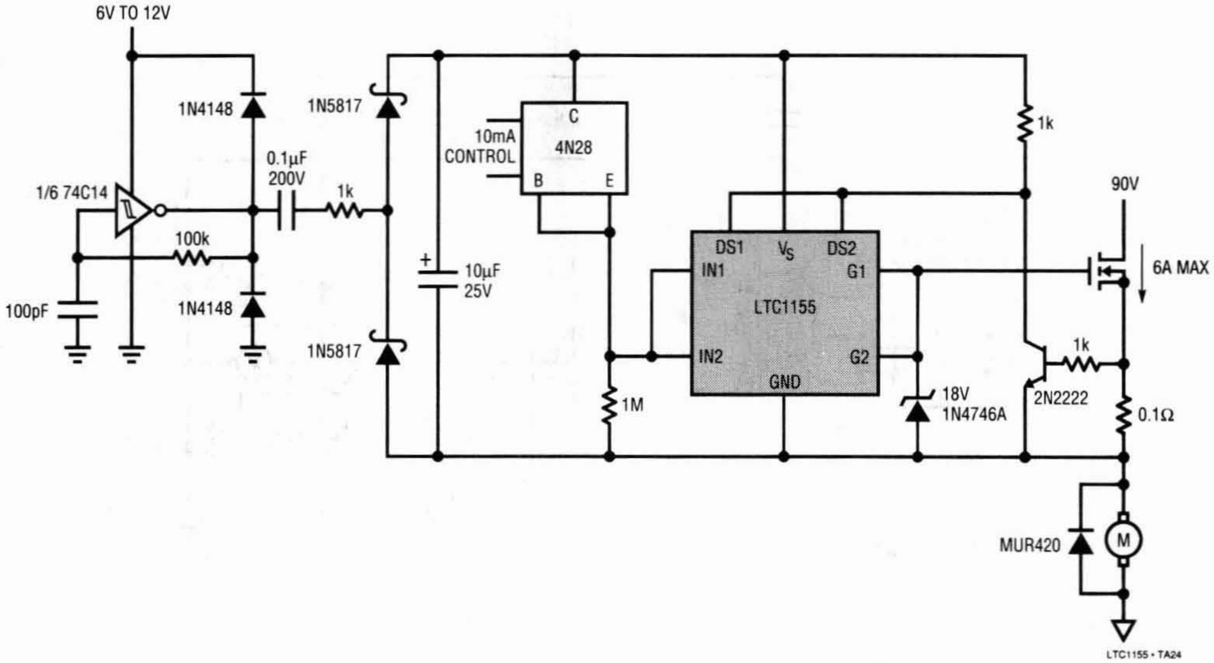

+
6V
100Ω
+
47μF
16V
0.1μF
1.1k
0.1Ω
300k
10k
TORQUE
ADJUST
1A TO
10A
MAX
1M
1M
+
1/2
LT1017
−
1M
1M
100k
10k
SPEED
ADJUST
120k
+
1/2
LT1017
−
0.0033μF
100k
DS1
V_S
DS2
IN1
G1
LTC1155
IN2
G2
GND
IRFZ24
SMALL DC APPLIANCE
OR TOOL MOTOR
M

SPEED IS PROPORTIONAL TO PULSE WIDTH. TORQUE IS PROPORTIONAL TO CURRENT

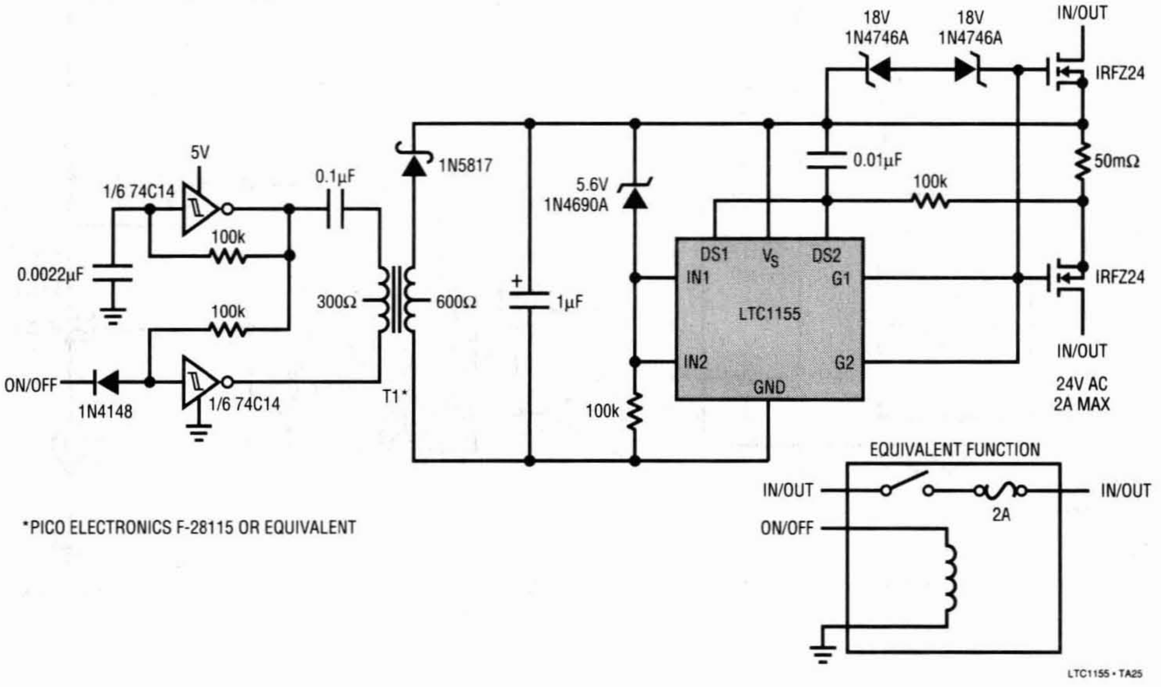
LTC1155 • TA23

TYPICAL APPLICATIONS

Isolated High Voltage High-Side Switch with Circuit Breaker


6V TO 12V
1N4148
1N5817
0.1μF
200V
1k
1/6 74C14
100k
100pF
1N4148
1N5817
+
10μF
25V
10mA
CONTROL
C
4N28
B
E
1M
DS1
V_S
DS2
IN1
G1
LTC1155
IN2
G2
GND
18V
1N4746A
1k
90V
6A MAX
1k
2N2222
0.1Ω
MUR420
M
LTC1155 • TA24

Isolated Solid State AC Relay with Circuit Breaker


18V
1N4746A
18V
1N4746A
IN/OUT
IRFZ24
5V
1/6 74C14
0.1μF
1N5817
5.6V
1N4690A
0.01μF
50mΩ
100k
100k
0.0022μF
300Ω
600Ω
+
1μF
DS1
V_S
DS2
IN1
G1
LTC1155
IN2
G2
GND
IRFZ24
100k
ON/OFF
1N4148
1/6 74C14
T1*
100k
IN/OUT
24V AC
2A MAX
EQUIVALENT FUNCTION
IN/OUT
IN/OUT
2A
ON/OFF
LTC1155 • TA25

*PICO ELECTRONICS F-28115 OR EQUIVALENT

LINEAR TECHNOLOGY

LTC1156

Quad High Side Micropower MOSFET Driver with Internal Charge Pump

FEATURES

- No External Charge Pump Components
- Fully Enhances N-Channel Power MOSFETs
- 16 Microamps Standby Current
- 95 Microamps ON Current
- Wide Power Supply Range 4.5V to 18V
- Controlled Switching ON and OFF Times
- Replaces P-Channel High Side Switches
- Compatible with Standard Logic Families
- Available in 16-pin SOL Package

APPLICATIONS

- Laptop Computer Power Switching
- SCSI Termination Power Switching
- Cellular Telephone Power Management
- P-Channel Switch Replacement
- Battery Charging and Management
- Low Frequency H-Bridge Driver
- Stepper Motor and DC Motor Control

DESCRIPTION

The LTC1156 quad High side gate driver allows using low cost N-channel FETs for high side switching applications. An internal charge pump boosts the gate drive voltage above the positive rail, fully enhancing an N-channel MOS switch with no external components. Micropower operation, with 16μA standby current and 95μA operating current, allows use in virtually all systems with maximum efficiency.

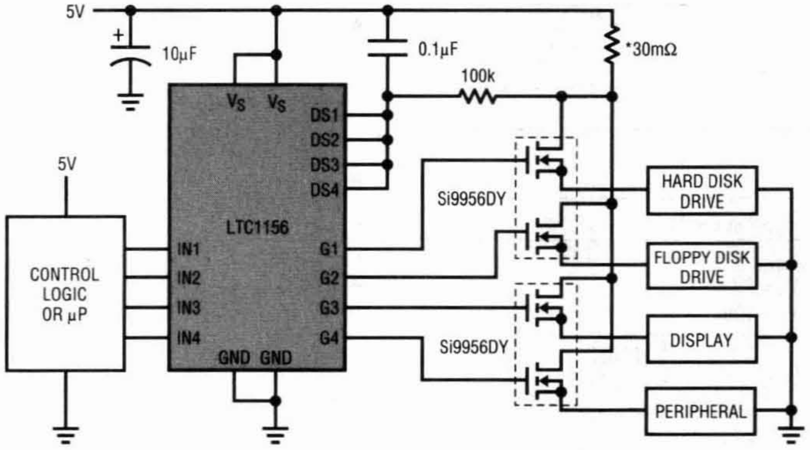
Included on chip is independent over-current sensing to provide automatic shutdown in case of short circuits. A time delay can be added to the current sense to prevent false triggering on high in-rush current loads.

The LTC1156 operates off of a 4.5V to 18V supply and is well suited for battery-powered applications, particularly where micropower "sleep" operation is required.

The LTC1156 is available in both 16-pin DIP and 16-pin SOL packages.

TYPICAL APPLICATION

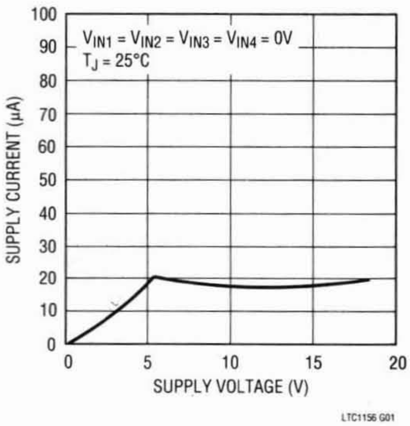
Laptop Computer Power Management



ALL COMPONENTS SHOWN ARE SURFACE MOUNT. MINIMUM PARTS COUNT SHOWN. CURRENT LIMITS CAN BE SET SEPARATELY AND TAILORED TO INDIVIDUAL LOAD CHARACTERISTICS.
* IMS026 INTERNATIONAL MANUFACTURING SERVICES, INC. (401) 683-9700

1156 TA01

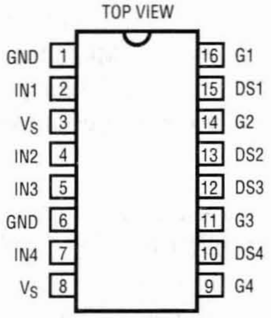
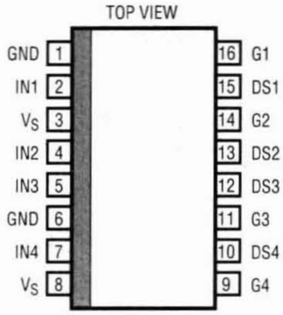
Standby Supply Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	22V
Input Voltage	$(V_S + 0.3V)$ to $(GND - 0.3V)$
Gate Voltage	$(V_S + 24V)$ to $(GND - 0.3V)$
Current (Any Pin)	50mA
Operating Temperature Range	
LTC1156C	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
 TOP VIEW GND 1 IN1 2 V_S 3 IN2 4 IN3 5 GND 6 IN4 7 V_S 8 16 G1 15 DS1 14 G2 13 DS2 12 DS3 11 G3 10 DS4 9 G4 N PACKAGE 16-LEAD PLASTIC DIP	LTC1156CN	 TOP VIEW GND 1 IN1 2 V_S 3 IN2 4 IN3 5 GND 6 IN4 7 V_S 8 16 G1 15 DS1 14 G2 13 DS2 12 DS3 11 G3 10 DS4 9 G4 S PACKAGE 16-LEAD PLASTIC SOL	LTC1156CS

ELECTRICAL CHARACTERISTICS $V_S = 4.5V$ to 18V, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_S	Supply Voltage	(Note 1)	●	4.5		18	V
I_Q	Quiescent Current OFF	$V_S = 5V$, $V_{IN} = 0V$ (Note 2)			16	40	µA
I_Q	Quiescent Current ON	$V_S = 5V$, $V_{IN} = 5V$ (Note 3)			95	125	µA
I_Q	Quiescent Current ON	$V_S = 12V$, $V_{IN} = 5V$ (Note 3)			180	400	µA
V_{INH}	Input High Voltage		●	2.0			V
V_{INL}	Input Low Voltage		●			0.8	V
I_{IN}	Input Current	$0V < V_{IN} < V_S$	●			±1.0	µA
C_{IN}	Input Capacitance				5		pF
V_{SEN}	Drain Sense Threshold Voltage			80	100	120	mV
			●	75	100	125	mV
I_{SEN}	Drain Sense Input Current	$0V < V_{SEN} < V_S$	●			±0.1	µA
$V_{GATE} - V_S$	Gate Voltage Above Supply	$V_S = 5V$	●	6.0	7.0	9.0	V
		$V_S = 6V$	●	7.5	8.3	15.0	V
		$V_S = 12V$	●	18.0	20.0	28.0	V
t_{ON}	Turn-ON Time	$V_S = 5V$, $C_{GATE} = 1000pF$					
		Time for $V_{GATE} > V_S + 2V$		50	160	300	µs
		Time for $V_{GATE} > V_S + 5V$		200	580	1000	µs
		$V_S = 12V$, $C_{GATE} = 1000pF$					
		Time for $V_{GATE} > V_S + 5V$		50	100	200	µs
		Time for $V_{GATE} > V_S + 10V$		120	250	500	µs

ELECTRICAL CHARACTERISTICS V_S = 4.5V to 18V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{OFF}	Turn-OFF Time	V_S = 5V, C_{GATE} = 1000pF Time for V_{GATE} < 1V		10	36	60	μs
		V_S = 12V, C_{GATE} = 1000pF Time for V_{GATE} < 1V		10	26	60	μs
t_{SC}	Short Circuit Turn-OFF Time	V_S = 5V, C_{GATE} = 1000pF Time for V_{GATE} < 1V		5	16	30	μs
		V_S = 12V, C_{GATE} = 1000pF Time for V_{GATE} < 1V		5	16	30	μs

The ● denotes specifications which apply over the full operating temperature range.

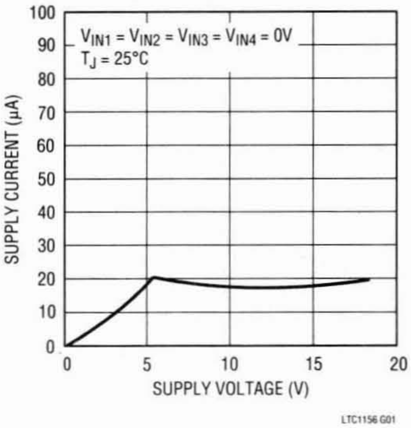
Note 1: Both V_S pins (3 and 8) must be connected together, and both ground pins (1 and 6) must be connected together.

Note 2: Quiescent current OFF is for all channels in OFF condition.

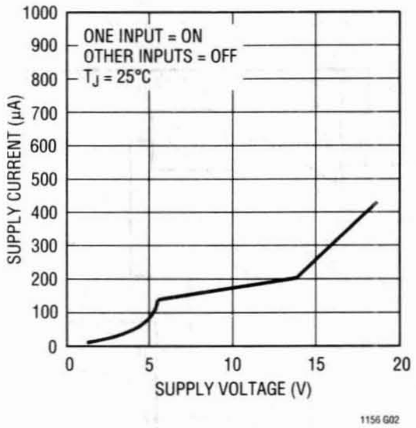
Note 3: Quiescent current ON is per driver and is measured independently.

TYPICAL PERFORMANCE CHARACTERISTICS

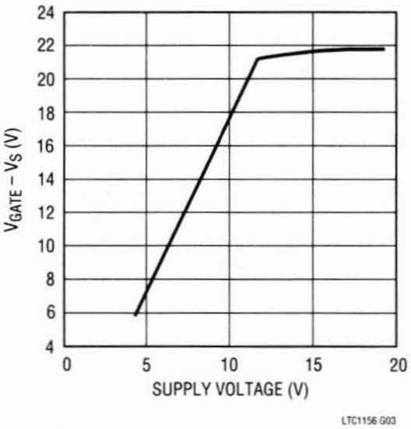
Standby Supply Current



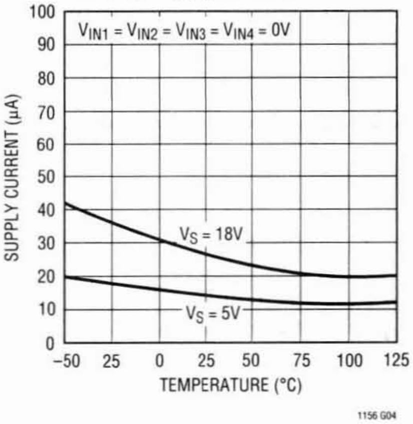
Supply Current per Channel ON



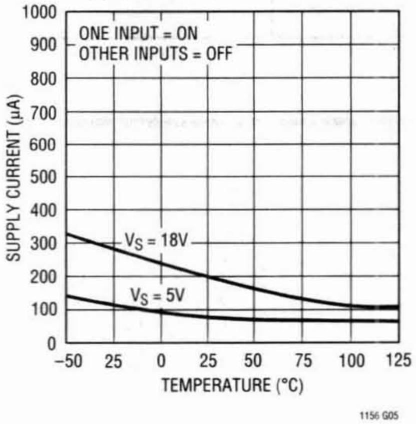
High Side Gate Voltage



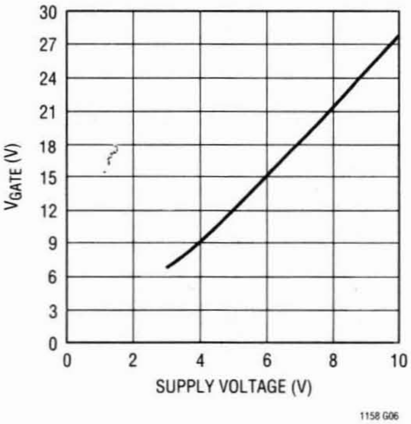
Standby Supply Current



Supply Current per Channel ON

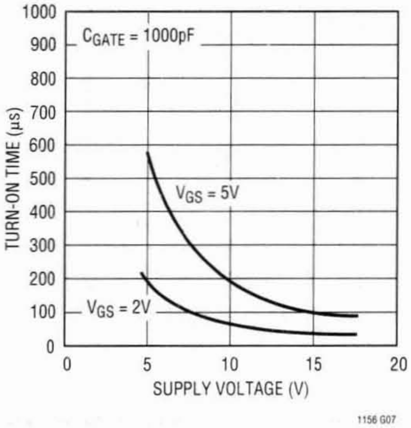


Low Side Gate Voltage

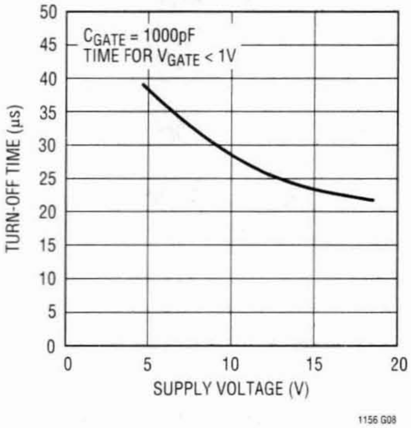


TYPICAL PERFORMANCE CHARACTERISTICS

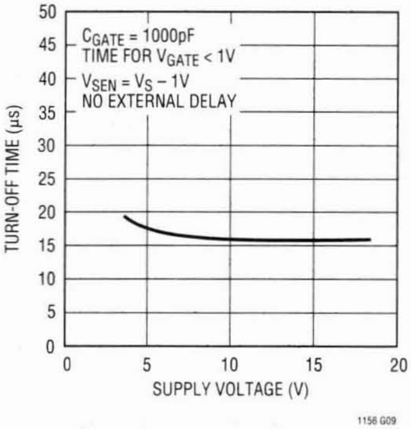
Turn-ON Time



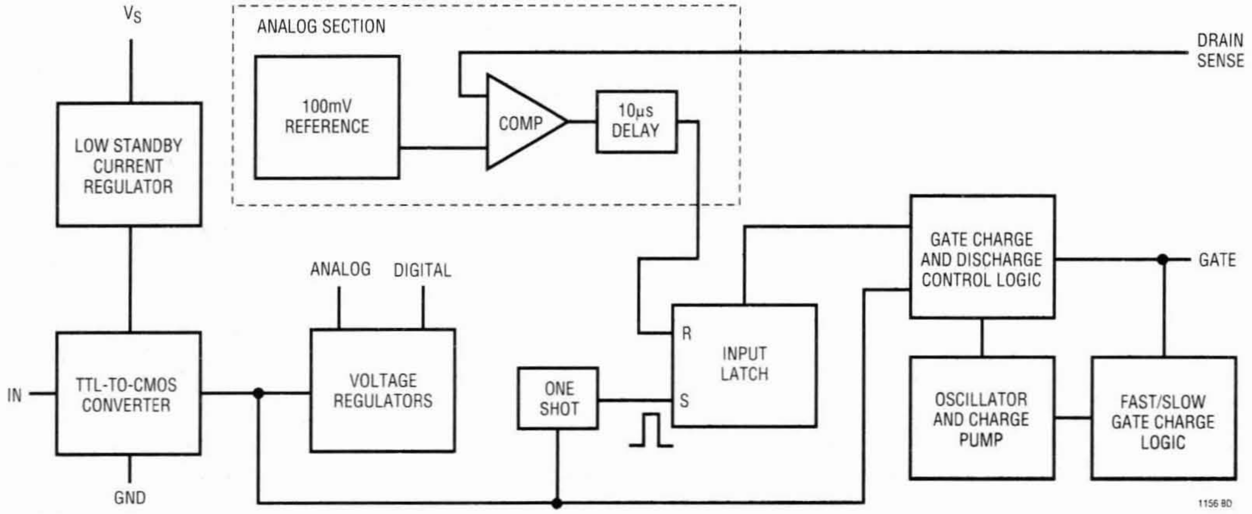
Turn-OFF Time



Short Circuit Turn-OFF Delay Time



BLOCK DIAGRAM


VS
ANALOG SECTION
DRAIN SENSE
LOW STANDBY CURRENT REGULATOR
100mV REFERENCE
COMP
10µs DELAY
GATE CHARGE AND DISCHARGE CONTROL LOGIC
GATE
ANALOG
DIGITAL
R
INPUT LATCH
S
IN
TTL-TO-CMOS CONVERTER
VOLTAGE REGULATORS
ONE SHOT
OSCILLATOR AND CHARGE PUMP
FAST/SLOW GATE CHARGE LOGIC
GND
1156 BD

OPERATION

The LTC1156 contains four independent power MOSFET gate drivers and protection circuits (refer to the Block Diagram for detail). Each section of LTC1156 consists of the following functional blocks:

TTL and CMOS Compatible Inputs

Each driver input has been designed to accommodate a wide range of logic families. The input threshold is set at 1.3V with approximately 100mV of hysteresis.

OPERATION

A voltage regulator with low standby current provides continuous bias for the TTL to CMOS converters. The TTL to CMOS converter output enables the rest of the circuitry. In this way the power consumption is kept to a minimum in the standby mode.

Internal Voltage Regulation

The output of the TTL to CMOS converter drives two regulated supplies which power the low voltage CMOS logic and analog blocks. The regulator outputs are isolated from each other so that the noise generated by the charge pump logic is not coupled into the 100mV reference or the analog comparator.

Gate Charge Pump

Gate drive for the power MOSFET is produced by an adaptive charge pump circuit which generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on chip and therefore no external components are required to generate the gate drive.

Drain Current Sense

The LTC1156 is configured to sense the drain current of the power MOSFET in high side applications. An internal 100mV reference is compared to the drop across a sense resistor (typically 0.002Ω to 0.1Ω) in series with the drain lead. If the drop across this resistor exceeds the internal 100mV threshold, the input latch is reset and the gate is quickly discharged by a large N-channel transistor. A simple RC network can be added to delay the over-current protection so that large in-rush current loads such as lamps or capacitors can be started.

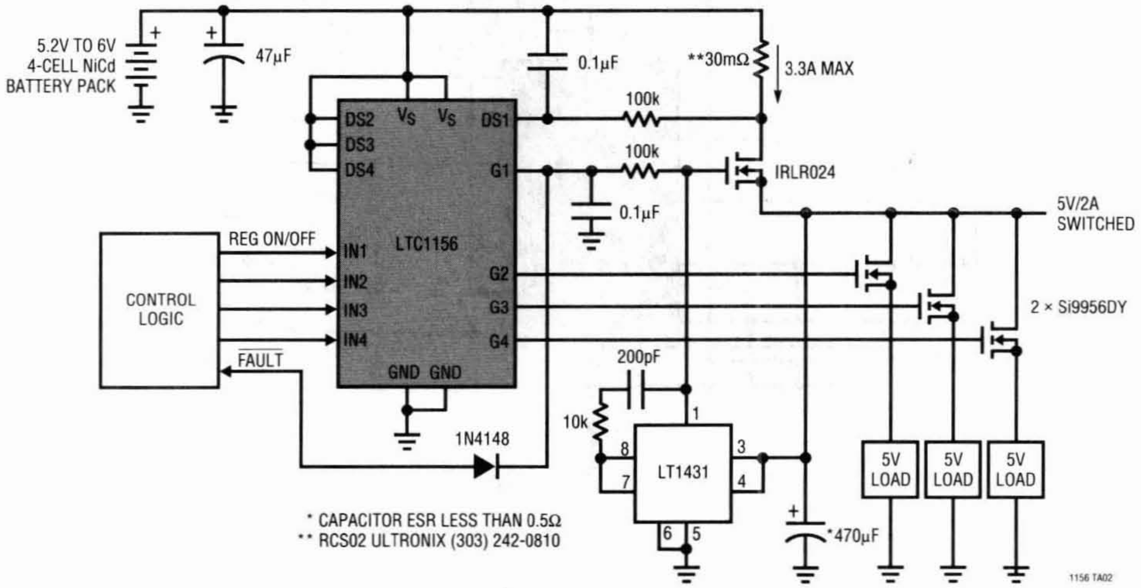
Supply and Ground Pins

The two supply pins (3 and 8) of the LTC1156 must be connected together at all times and the two ground pins (1 and 6) must be connected together at all times. The two supply pins should be connected to the "top" of the drain current sense resistor/s to ensure accurate sensing.

For further applications information, see the LTC1155 Dual High Side Micropower MOSFET Driver data sheet.

TYPICAL APPLICATIONS

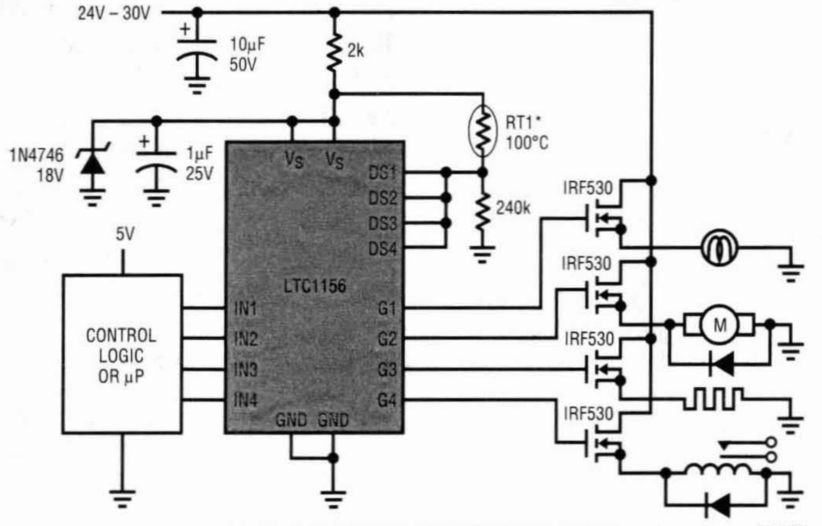
4-Cell Extremely Low Voltage Drop Regulator and Three Load Switches with Short-Circuit Protection and 20μA Standby Current


5.2V TO 6V
4-CELL NiCd
BATTERY PACK
47μF
0.1μF
**30mΩ
3.3A MAX
100k
100k
IRLR024
0.1μF
5V/2A
SWITCHED
DS2
DS3
DS4
VS
VS
DS1
G1
LTC1156
IN1
IN2
IN3
IN4
G2
G3
G4
GND
GND
REG ON/OFF
CONTROL
LOGIC
FAULT
2 × Si9956DY
200pF
10k
1N4148
LT1431
*470μF
5V
LOAD
5V
LOAD
5V
LOAD
1156 TA02

* CAPACITOR ESR LESS THAN 0.5Ω
** RCS02 ULTRONIX (303) 242-0810

TYPICAL APPLICATIONS

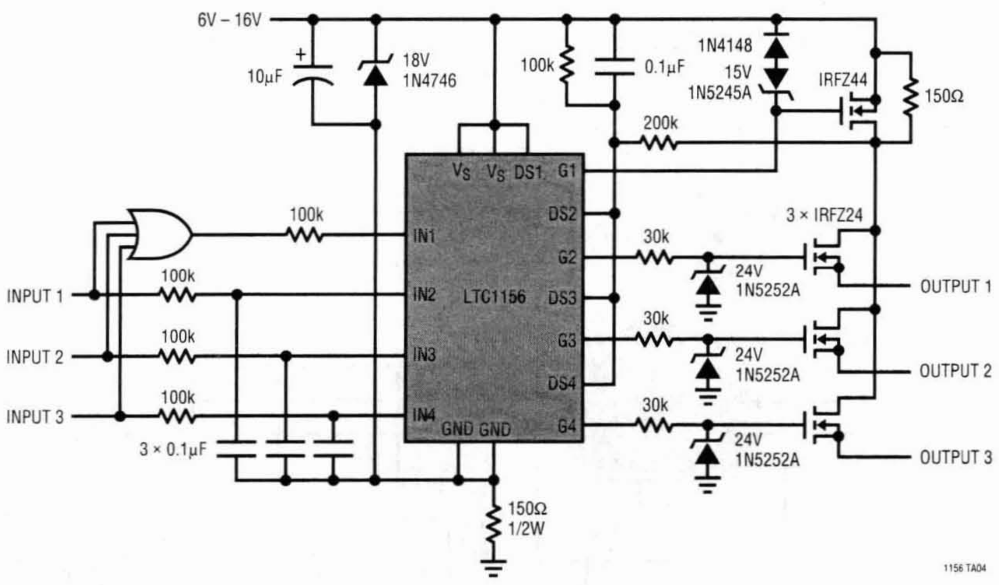
24V to 30V Quad Industrial Switch with Thermal Shutdown


24V – 30V
+
10µF
50V
2k
RT1*
100°C
1N4746
18V
+
1µF
25V
V_S V_S
DS1
DS2
DS3
DS4
240k
5V
LTC1156
CONTROL
LOGIC
OR µP
IN1
IN2
IN3
IN4
G1
G2
G3
G4
GND GND
IRF530
IRF530
IRF530
IRF530
M

* KEYSTONE RL2006-100-100-30-PT MOUNT ON HEATSINK.

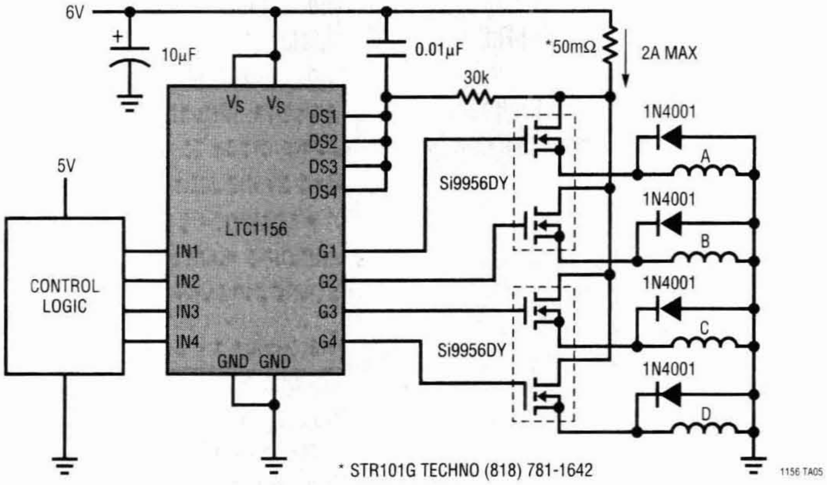
1156 TA03

Automotive Triple High Side Switch with Reverse Battery Interrupt, Short-Circuit and High-Voltage Transient Protection (20µA Standby Current)


6V – 16V
+
10µF
18V
1N4746
100k
0.1µF
1N4148
15V
1N5245A
IRFZ44
150Ω
200k
V_S V_S DS1 G1
DS2
G2
DS3
G3
DS4
G4
IN1
IN2
IN3
IN4
LTC1156
GND GND
100k
100k
100k
100k
INPUT 1
INPUT 2
INPUT 3
3 × 0.1µF
30k
30k
30k
24V
1N5252A
24V
1N5252A
24V
1N5252A
3 × IRFZ24
OUTPUT 1
OUTPUT 2
OUTPUT 3
150Ω
1/2W
1156 TA04

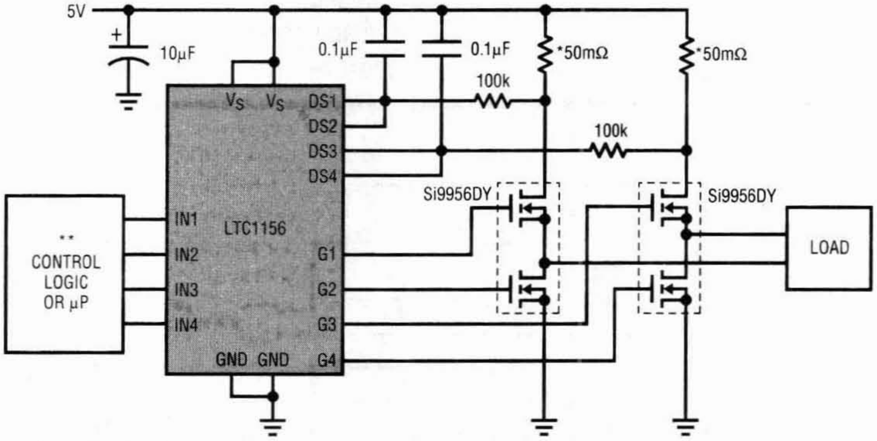
TYPICAL APPLICATIONS

4-Phase Stepper Motor Driver with Short-Circuit Protection


6V
10μF
0.01μF
*50mΩ
2A MAX
30k
1N4001
A
B
C
D
5V
V_S
V_S
DS1
DS2
DS3
DS4
LTC1156
IN1
IN2
IN3
IN4
G1
G2
G3
G4
GND
GND
CONTROL LOGIC
Si9956DY
Si9956DY
1156 TA05

* STR101G TECHNO (818) 781-1642

Full H-Bridge Driver with Short-Circuit Protection and 16μA Standby Current
Low Frequency Operation (<100Hz)


5V
10μF
0.1μF
0.1μF
*50mΩ
*50mΩ
100k
100k
V_S
V_S
DS1
DS2
DS3
DS4
LTC1156
IN1
IN2
IN3
IN4
G1
G2
G3
G4
GND
GND
**
CONTROL LOGIC OR μP
Si9956DY
Si9956DY
LOAD
1156 TA06

* STR101G TECHNO (818) 781-1642
** SOFTWARE (OR HARDWARE) DELAYS SHOULD BE PROVIDED TO AVOID CROSS-CONDUCTION. ALL COMPONENTS SHOWN ARE SURFACE MOUNT.

For more Typical Applications, see LTC1155 data sheet.

LT1188

1.5A High Side Switch

FEATURES

- 1.5A Bipolar Switch
- Controlled Output Slew Rate (2V/μs) to Limit R.F.I. Generation
- 60V Load Dump Capability with Inductive Kickback
- Internal Negative Voltage Clamp for Inductive Loads
- 500μA Standby Current
- Logic Input — TTL Levels
- Low Input Bias Current (20μA)
- Status Output
- Short Circuit Detection and Shutoff
- Open Circuit Detection
- Overtemp Detection and Shutoff

APPLICATIONS

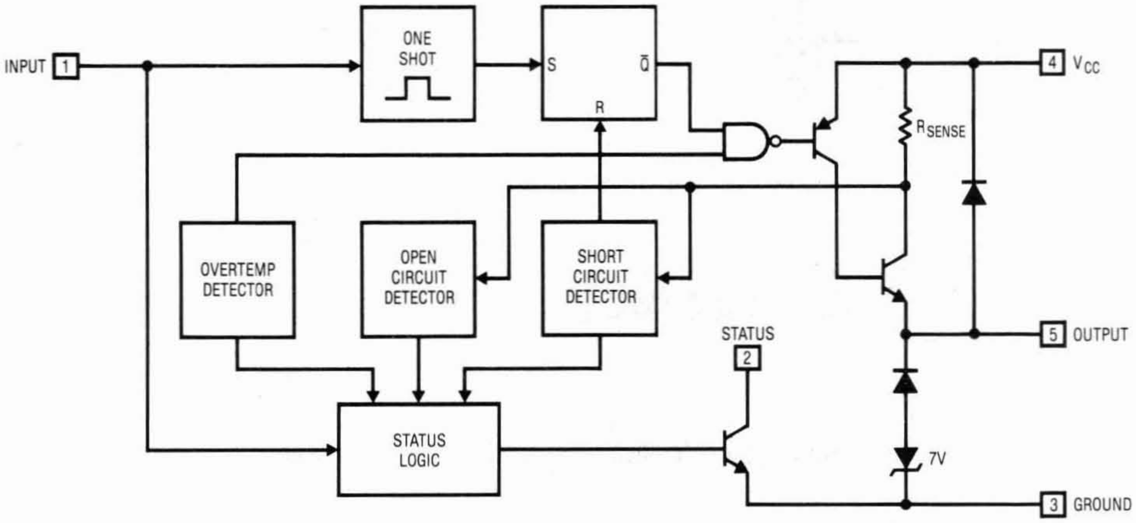
- Solenoid Driver
- Relay Driver
- Motor Driver

DESCRIPTION

The LT1188 is a monolithic high side switch employing bipolar technology. The device is designed to operate in harsh environments such as those encountered in the automotive industry. The device incorporates an internal clamp diode to clamp the negative voltage spikes generated by inductive loads such as solenoids and is capable of withstanding load dumps of 60V on the supply pin while clamping such spikes. Standby current is only 500μA and ground pin current, when driving a 1A load, is only 5mA.

The device's input logic levels are designed to be compatible with standard TTL levels while drawing only 20μA in the on state. A status output is provided to inform the user of the condition of the output load as well as the switch. The status pin will change state for shorted as well as open loads and will also indicate when the device is above normal operating temperature. The device protects itself against short circuited loads by limiting output current and then shutting itself off after a specified time if the short remains. The device protects itself against overtemperature by shutting itself off. Overtemperature shutoff occurs at a temperature above where the status pin overtemp indication occurs, allowing the user time to recognize and possibly correct the problem before drive to the load is removed.

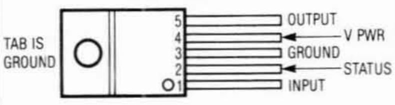
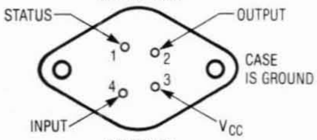
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 30V
Supply Voltage (Transient 200ms) 60V
Logic Input Voltage 30V
Operating Temperature Range
  LT1188M .... −55°C to 125°C
  LT1188C .... 0°C to 70°C
Junction Temperature Range
  LT1188M .... −55°C to 175°C
  LT1188C .... 0°C to 100°C
Storage Temperature .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
FRONT VIEW  TAB IS GROUND 5 4 3 2 1 OUTPUT V PWR GROUND STATUS INPUT T PACKAGE 5-LEAD TO-220	LT1188CT
BOTTOM VIEW  STATUS OUTPUT 1 2 4 3 CASE IS GROUND INPUT V_{CC} K PACKAGE 4-LEAD TO-3 METAL CAN	LT1188CK LT1188MK

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch Voltage Loss (V_{CC}-V_{OUT}, Switch On)	$I_{OUT} = 1.0A$, $5V \le V_{CC} \le 30V$	●		1.0	1.2	V
	$I_{OUT} = 1.5A$, $5V \le V_{CC} \le 30V$	●		1.2	1.4	V
Output Leakage Current	$V_{CC} = 30V$, $V_{OUT} = 0V$, $V_{IN} = 0V$	●		5	150	μA
High Level Input Voltage	$5V \le V_{CC} \le 30V$, $I_{OUT} = 1.5A$, (Note 2)	●	2.0			V
Low Level Input Voltage	$5V \le V_{CC} \le 30V$, $I_{OUT} = 0.0A$, (Note 3)	●			0.8	V
High Level Input Current	$5V \le V_{CC} \le 30V$, $V_{IN} = 2.0V$	●	5	20	60	μA
Low Level Input Current	$5V \le V_{CC} \le 30V$, $V_{IN} = 0.4V$	●		0	1	μA
Status Pin Saturation Voltage	$5V \le V_{CC} \le 30V$, $I_{STATUS} = 1mA$	●		0.2	0.4	V
Status Leakage Current	$V_{CC} = 30V$, $V_{STAT} = 5.5V$	●			1	μA
Standby Current	$V_{IN} = 0.4V$, $R_L = \infty$, $V_{CC} = 30V$					
	Status = High	●		500	650	μA
	Status = Low	●		550	750	μA
Ground Pin Current	$V_{CC} = 30V$, $I_{OUT} = 1.5A$	●		9	15	mA
Clamp Voltage	$I_{CLAMP} = 1.0A$, (Note 4)	●		8	10	V
	$I_{CLAMP} = 1.5A$, (Note 4)	●		9	12	V
Turn-On Delay	(Note 5)	●			30	μs
Turn-Off Delay	(Note 6)	●			30	μs
Output Slew Rate	$V_{CC} = 17V$, $R_L = 16\Omega$					
	Output Rising	●	0.5	1.2	5.0	V/μs
	Output Falling	●	0.5	2.0	5.0	V/μs
Short Circuit Current	V_{CC}-$V_{OUT} = 7V$			3.5		A
		●	2.0		4.7	A
	V_{CC}-$V_{OUT} = 17V$			2.5		A
		●	1.5		4.0	A
	V_{CC}-$V_{OUT} = 30V$			1.5		A
		●	0.5		3.0	A

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Short Circuit Sense Time (t_{SC})	$V_{CC} = 30V$	●	20	50	110	µs
Status Reset Time (t_R)	$V_{CC} = 30V$	 ●	 350	600 	 950	µs µs
Open Circuit Current Trip Level		●	18	40	75	mA
Overtemp Detection Point				150		°C
Thermal Resistance	Junction to Case (Note 7)				4.0	°C/W

Note 1: The ● denotes specifications which apply over the full operating temperature range.

Note 2: 2.0V is the minimum input voltage guaranteed to turn the device on. For input voltages greater than 2.0V the output voltage is guaranteed to be turned on.

Note 3: 0.8V is the maximum input voltage guaranteed to turn the device off. For input voltages less than 0.8V the device is guaranteed to be turned off.

Note 4: The negative voltage clamp is designed for intermittent operation such as clamping the reverse voltage spike caused by an inductive load. Clamp duration should be less than 100ms.

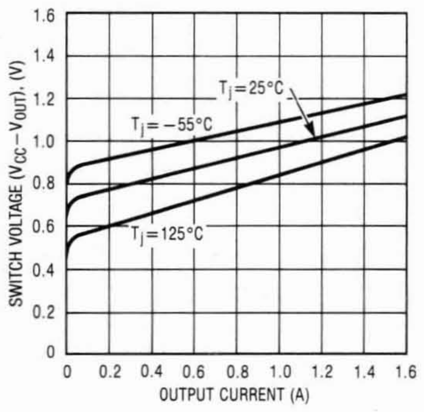
Note 5: Turn on delay time is defined to be the time from the rising edge of the input signal to the time that the output voltage is equal to 2V.

Note 6: Turn off delay time is defined to be the time from the falling edge of the input signal to the time that the output drops by 2V.

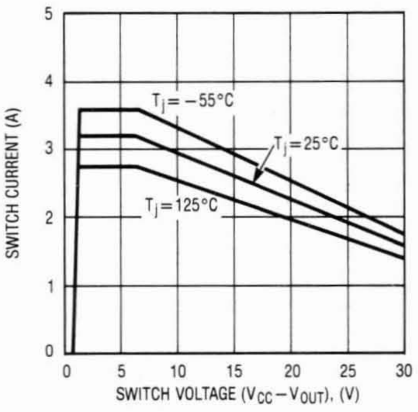
Note 7: Thermal resistance is from the junction of the switch transistor to the back of the case directly below the switch transistor. The device will be centered in the package and proper mounting techniques are required in order to have good thermal conduction away from this area of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

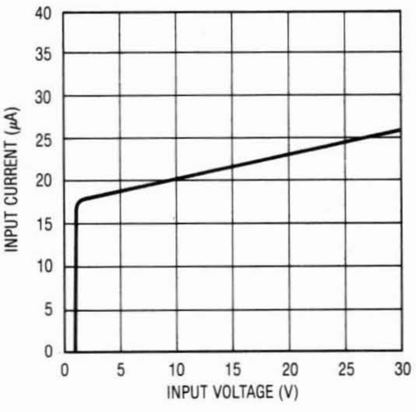
Switch Voltage Loss



Short Circuit Current

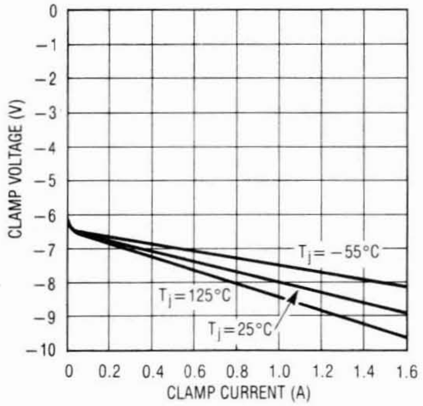


Input Current

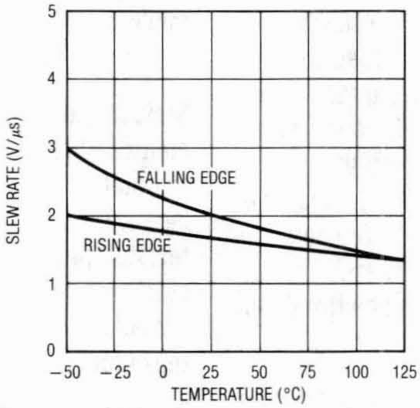


TYPICAL PERFORMANCE CHARACTERISTICS

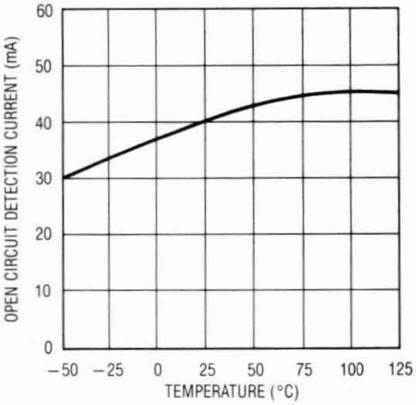
Clamp Voltage



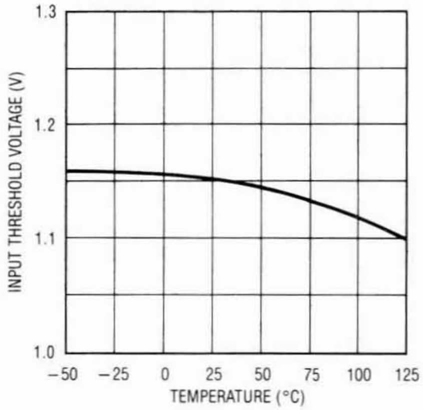
Slew Rate



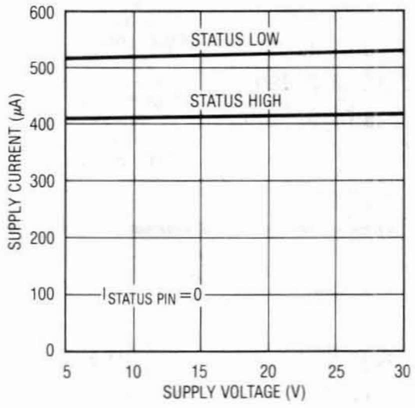
Open Circuit Detection Current



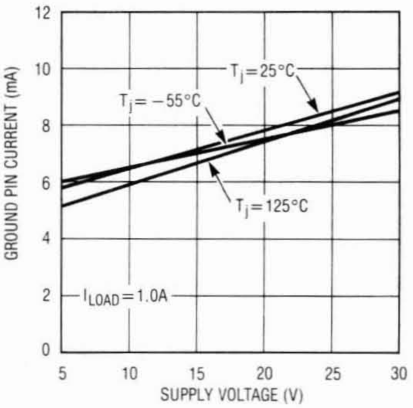
Input Threshold Voltage



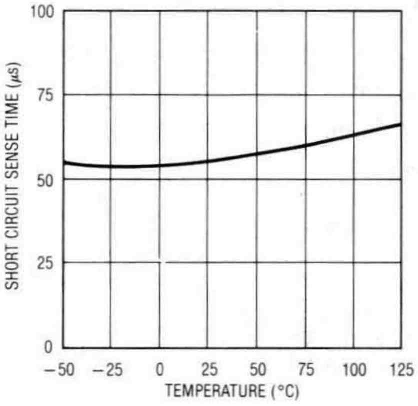
Supply Current (Switch Off)



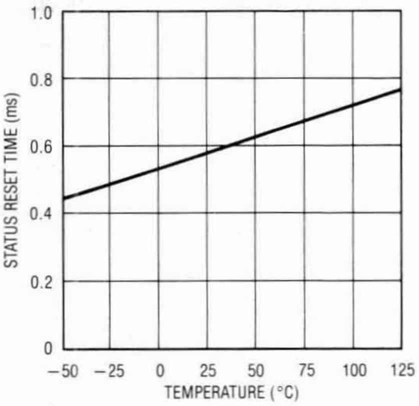
Ground Pin Current (Switch On)



Short Circuit Sense Time



Status Reset Time



PIN FUNCTIONS

Output: As can be seen from the block diagram the output of the device is the emitter of an NPN power transistor which can source current from the supply. The slew rate of the output, both rising and falling, is controlled to minimize the generation of RFI. In the negative direction the output pin is clamped to ground with a combination diode/zener clamp. This clamp is designed to clamp the flyback voltage spike of an inductive load such as a solenoid. This clamp is designed for intermittent operation. The duration of the flyback spike should be less than 100ms. This allows a wide range of inductive loads. In the positive direction the output pin is clamped to the supply with a diode.

Ground: The ground pin of the device must be connected for the device to turn on. For an open ground pin the device will be in an off state.

Input: The input pin of the device must be driven above the input voltage threshold for the device to turn on. The input voltage threshold is designed to be compatible with standard TTL levels, while the input impedance is high. Input current above the threshold is typically 20µA. For an open input pin the device will remain in an off state. The input logic requires a minimum input voltage slew rate of 3V/ms. This is several orders of magnitude slower than any logic family currently in use and should not normally cause any problems.

Status: The status output is the collector of a grounded emitter NPN transistor whose base is internally driven by the status logic. A logic low indicates a fault condition (see Truth Table). This output requires an external pull-up resistor that should be chosen so that the current into the status pin, when the status pin is pulled low, is <1mA. The breakdown voltage of this NPN collector is equal to that of the output switch.

Diagnostic Truth Table

	Input	Output	Status
Normal Operation	L H	L H	H H
Open Load	L H	X H	H L
Shorted Load	L H	L L	L L
Thermal Overload	L H	L L	H L

STATUS FUNCTIONS

Open Circuit Fault: The status output will be pulled low if the output current drops below the open circuit current threshold (typically 40mA). The open circuit detector is only active during the time that the switch is on (input high), and will only affect the status output during that time. For open circuit faults the status output will not latch low. The status line will be low only as long as the fault condition exists.

Short Circuit Fault: For short circuit faults lasting longer than the short circuit sense time (≈60µs), two things will occur; the output switch will be latched off and the status output will be latched low. The output will remain off until the input is recycled. The status output will remain low until both the short is removed and the input is recycled, and will be reset high after the status reset time (≈500µs) has elapsed. For continuous shorts the output will turn on, for the short circuit sense time, each time the input is cycled and the status output will remain latched low. The current at which the short circuit detector activates is a function of the supply voltage as can be seen by looking at the short circuit current curve in the typical performance characteristics.

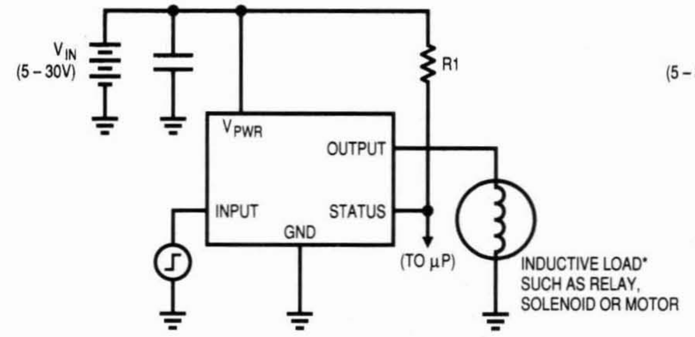
Thermal Fault: Thermal faults can occur for two reasons, heating from external sources or heating due to power dissipation in the switch itself. The device will act similarly for both cases. Thermal faults will only affect the status output during the time that the switch is on (input high). Thermal faults will cause the status output to latch low for the duration of an input cycle. The status output will be reset on the falling edge of the input waveform. There are two levels of thermal overload. At ≈150°C junction temperature the thermal sensing circuitry will latch the status output low, and the output will remain on (as long as the input is high). At ≈165°C the thermal sensing circuitry will

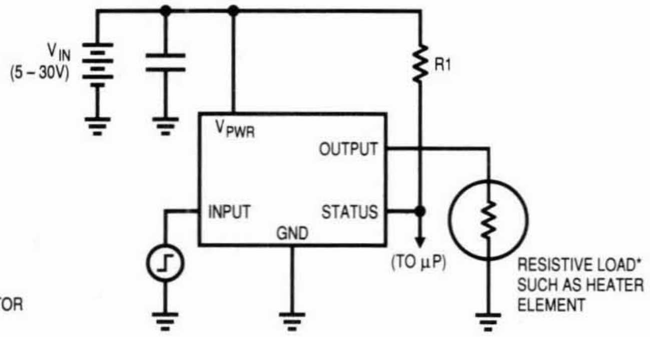
STATUS FUNCTIONS

turn the output off. If the junction temperature drops back below ≈165°C the output will turn back on. This means that if the thermal fault is caused by an external source the output will stay off as long as the temperature is held above ≈165°C. If the thermal fault is caused by internal power dissipation, the device will cycle on and off to maintain the junction temperature near 165°C. The status output gives a fault indication at a temperature below the actual shutdown temperature to allow the user time to sense and possibly correct the fault condition before the switch takes action to protect itself.

Load Dump: For transient supply voltages greater than 35V or for transient switch voltages greater than 35V, a separate clamp network will turn the output off. This is necessary to keep the switch within its safe operating area and also to prevent the device from passing the high voltage transient on to the load. To guarantee survival of the switch for load dump type transients the risetime of the supply voltage, at the supply pin of the device, should be limited to $<1V/\mu s$. This is to allow the device time to turn off between when the supply voltage reaches 35V and when the supply voltage reaches 50V so that the device is turned off well below its BVCEO voltage. If the device is bypassed closely, the series inductance and resistance of the supply leads along with the supply bypass capacitor will form an RLC filter and will limit the risetime. The slew rate limiting circuitry will be disabled during this transient turn off time. The output will remain off until the supply voltage drops back below 35V. During the time that the output is turned off by this clamp network the open circuit detector will still be active and will set the status pin low until the output comes back on and the output current is greater than the open circuit current.

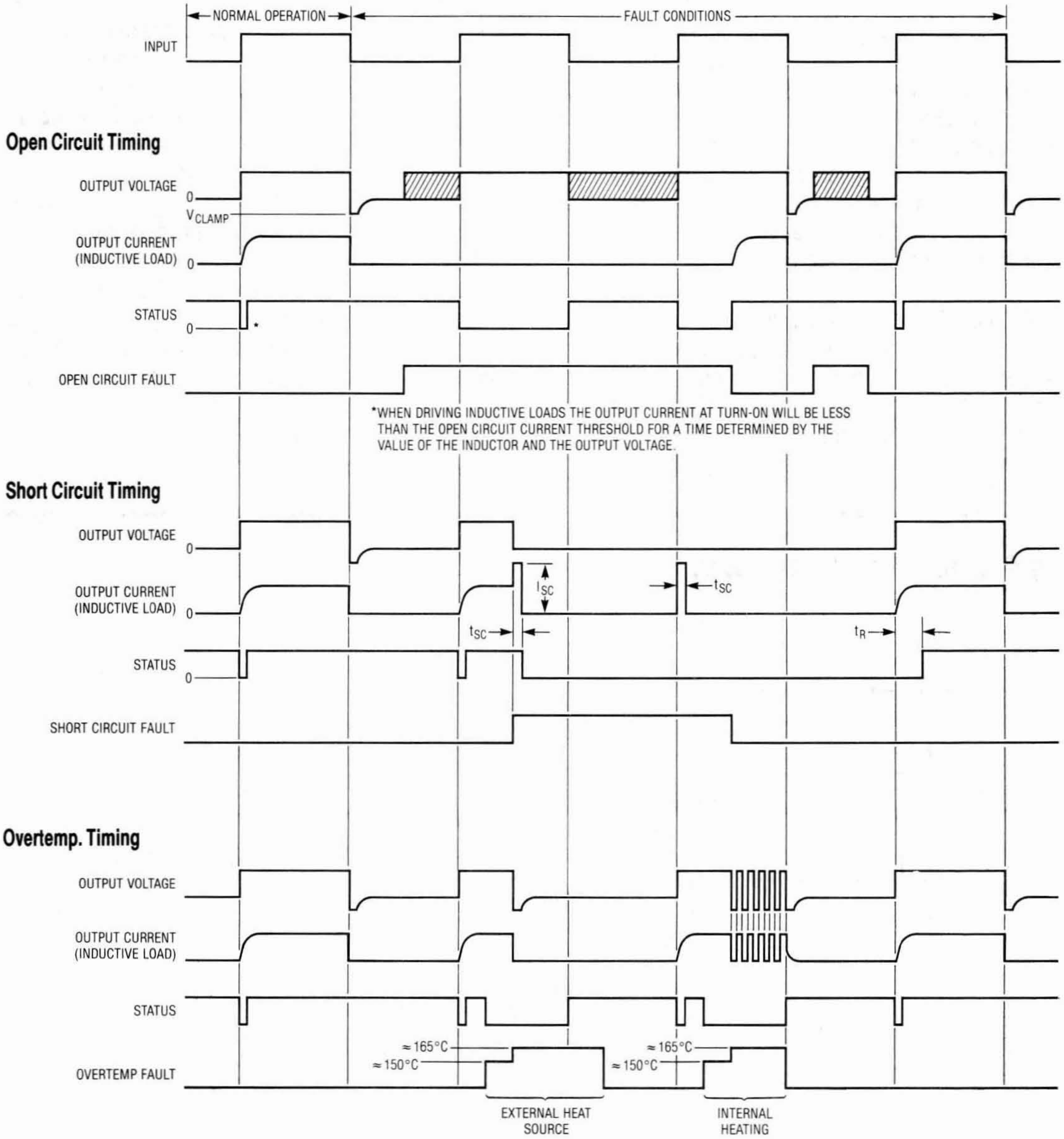
TYPICAL APPLICATIONS





* THE LT1188 IS NOT RECOMMENDED FOR DRIVING LIGHT BULBS DUE TO THEIR INHERENTLY HIGH INRUSH CURRENTS. HIGH INRUSH CURRENTS WILL ACTIVATE THE SHORT CIRCUIT PROTECTION CIRCUITRY OF THE DEVICE, CAUSING IT TO SHUT OFF AFTER ≈50µS (SHORT CURCUIT SENSE TIME).

TIMING DIAGRAM



Open Circuit Timing

*WHEN DRIVING INDUCTIVE LOADS THE OUTPUT CURRENT AT TURN-ON WILL BE LESS THAN THE OPEN CIRCUIT CURRENT THRESHOLD FOR A TIME DETERMINED BY THE VALUE OF THE INDUCTOR AND THE OUTPUT VOLTAGE.

Short Circuit Timing

Overtemp. Timing

NORMAL OPERATION
FAULT CONDITIONS
INPUT
OUTPUT VOLTAGE
0
V_{CLAMP}
OUTPUT CURRENT (INDUCTIVE LOAD)
0
STATUS
0
*
OPEN CIRCUIT FAULT
OUTPUT VOLTAGE
0
OUTPUT CURRENT (INDUCTIVE LOAD)
0
I_{SC}
t_{SC}
t_{SC}
t_R
STATUS
0
SHORT CIRCUIT FAULT
OUTPUT VOLTAGE
OUTPUT CURRENT (INDUCTIVE LOAD)
STATUS
≈165°C
≈150°C
≈165°C
≈150°C
OVERTEMP FAULT
EXTERNAL HEAT SOURCE
INTERNAL HEATING

SECTION 4—POWER PRODUCTS

LINEAR REGULATORS

LT1087, Adjustable Low Dropout Regulator with Kelvin-Sense Inputs 4-56
LT1117, 800mA Low Dropout Positive Regulators; Adjustable and Fixed 2.85V, 5V 4-63
LT1121-5, Micropower Low Dropout Regulator 13-46
LT1123, 5V Low Dropout Regulator Driver 4-75
LT1123-2.85, Low Dropout Regulator Driver for SCSI-2 Active Termination 13-48
LT1185, Low Dropout Regulator with Adjustable Current Limit 4-86

LT1087

Adjustable Low Dropout Regulator with Kelvin-Sense Inputs

FEATURES

- Separate Sense Inputs Allow True Kelvin Sensing
- Easily Parallelable
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.05% Line Regulation
- 0.1% Load Regulation at the Sense Point

APPLICATIONS

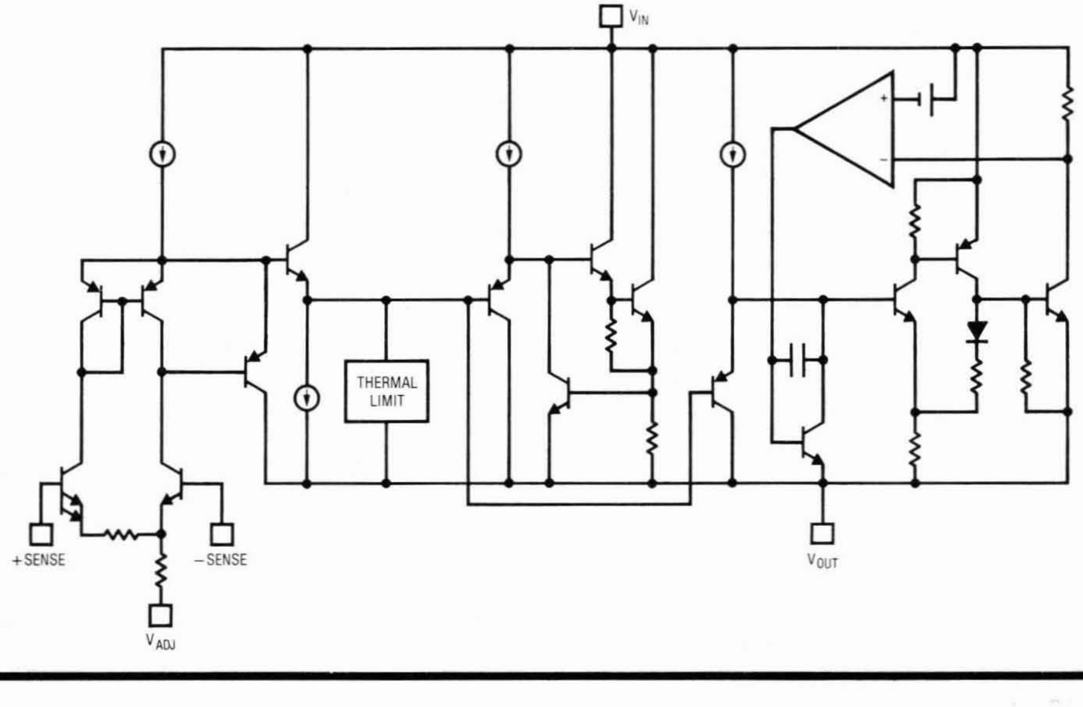
- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- High Current Regulators
- Remotely Sensed Regulators

DESCRIPTION

The LT1087 is a variation of the LT1084 Adjustable Low Dropout 3 Terminal Regulator. The sense points of the internal reference/error amp are brought out to allow added flexibility.

They can be used for true Kelvin sensing of the output voltage at a remotely located load. They can be used to force the devices to share current equally when more than one device is wired in parallel, allowing the user to easily build higher current modules. This device is designed to provide 5A of output current. All internal circuitry is designed to operate down to 1V input to output differential and the dropout voltage is fully specified as a function of load current. On-chip trimming adjusts the reference voltage to 1%. Current limit is also trimmed, minimizing the stress on both the regulator and power source circuitry under overload conditions. A 10µF output capacitor is required on these devices; however, this is usually included in most regulator designs.

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Power Dissipation .... Internally Limited

Input to Output Voltage Differential
- "M" Grade 35V
- "C" Grade 30V

Differential Voltage Between Sense Pins
- ($|V_{+SENSE} - V_{-SENSE}|$) 4V

Sense Pin Voltage
- Range .... (V_{OUT}* − 1V) ≤ $V_{\pm SENSE}$ ≤ (V_{OUT}* + 0.4V)

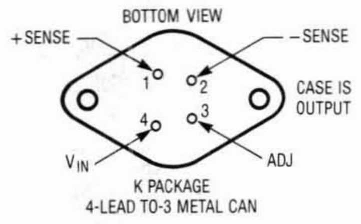
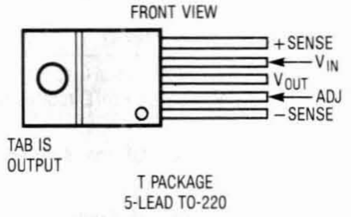
Operating Junction Temperature Range
- "M" Grade
  - Control Section .... −55°C to 150°C
  - Power Transistor .... −55°C to 200°C
- "C" Grade
  - Control Section...................... 0°C to 125°C
  - Power Transistor..................... 0°C to 150°C

Storage Temperature .... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) .... 300°C

*V_{OUT} is referring to the regulator output pin voltage.

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 BOTTOM VIEW +SENSE −SENSE 1 2 3 4 CASE IS OUTPUT V_{IN} ADJ K PACKAGE 4-LEAD TO-3 METAL CAN	LT1087MK LT1087CK
 FRONT VIEW +SENSE V_{IN} V_{OUT} ADJ −SENSE TAB IS OUTPUT T PACKAGE 5-LEAD TO-220	LT1087CT

PRECONDITIONING

100% Thermal Limit Burn-In

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	I_{OUT} = 10mA, T_j = 25°C, ($V_{IN} - V_{OUT}$) = 3V		1.238	1.250	1.262	V
	10mA ≤ I_{OUT} ≤ 5A 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 25V	●	1.225	1.250	1.270	V
Line Regulation	I_{LOAD} = 10mA, 1.5V ≤ ($V_{IN} - V_{OUT}$) ≤ 15V, T_j = 25°C			0.015	0.2	%
		●		0.035	0.2	%
	M Grade 15V ≤ ($V_{IN} - V_{OUT}$) ≤ 35V	●		0.05	0.5	%
	C Grade 15V ≤ ($V_{IN} - V_{OUT}$) ≤ 30V (Notes 1, 2)	●		0.05	0.5	%
Load Regulation	($V_{IN} - V_{OUT}$) = 3V 10mA ≤ I_{OUT} ≤ 5A T_j = 25°C (Notes 1, 2)			0.1	0.3	%
		●		0.2	0.4	%
Dropout Voltage	ΔV_{REF} = 1%, I_{OUT} = 5A, (Note 4)	●		1.3	1.5	V
Common Mode Range of Sense Pins ΔV_{REF}	(V_{OUT} − 1V) ≤ V_{+SENSE} ≤ V_{OUT}			0.4		mV
Differential Gain of Sense Pins $\Delta V_{REF}/\Delta V_{SENSE}$	V_{+SENSE} = V_{OUT} V_{-SENSE} = (V_{OUT} − 40mV)			11		V/V
Sense Pin Bias Current				0.3		µA
Minimum Load Current	($V_{IN} - V_{OUT}$) = 25V	●		5	10	mA
Thermal Regulation	T_A = 25°C, 30ms pulse			0.003	0.015	%/W

ELECTRICAL CHARACTERISTICS (See Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Ripple Rejection	f = 120Hz $C_{ADJ} = 25\mu F$, $C_{OUT} = 25\mu F$ Tantalum $I_{OUT} = 5A$, $(V_{IN} - V_{OUT}) = 3V$	●	60	75		dB
Adjust Pin Current	$T_j = 25°C$			55		μA
		●			120	μA
Adjust Pin Current Change	$10mA \leq I_{OUT} \leq 5A$ $1.5V \leq (V_{IN} - V_{OUT}) \leq 25V$	●		0.2	5	μA
Temperature Stability		●		0.5		%
Long Term Stability	$T_A = 125°C$, 1000 Hrs.			0.3	1	%
RMS Output Noise (% of V_{OUT})	$T_A = 25°C$ $10Hz = \leq f \leq 10kHz$			0.003		%
Thermal Resistance Junction to Case	K Package: Control Circuitry/Power Transistor T Package: Control Circuitry/Power Transistor				0.75/2.3 0.65/2.7	°C/W °C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing. Unless otherwise specified, + Sense, – Sense and V_{OUT} are tied together at the package.

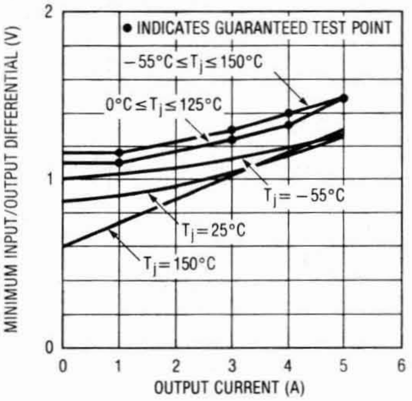
Note 2: Line and load regulation are guaranteed up to the maximum power dissipation (45W for the LT1087K, 30W for the LT1087T). Power dissipation is determined by the input/output differential and the output current. Guaranteed maximum power dissipation will not be available over the full input/output voltage range.

Note 3: Load regulation is defined to be the change in output voltage at the sense point. The sense point is defined to be the point at which the sense pins, output, and the top of the resistive divider that sets the output voltage are tied together. The voltage drop from the output pin of the device to the sense point must be < 1V.

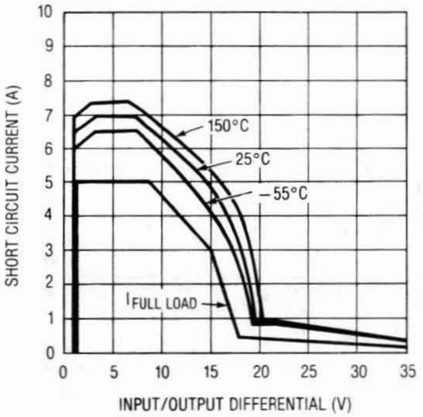
Note 4: Dropout voltage is specified over the full output current range of the device. Test points and limits are shown on the Dropout Voltage curve. Dropout voltage is defined to be the voltage from input to output and is tested with the sense pins tied to the output pin.

TYPICAL PERFORMANCE CHARACTERISTICS

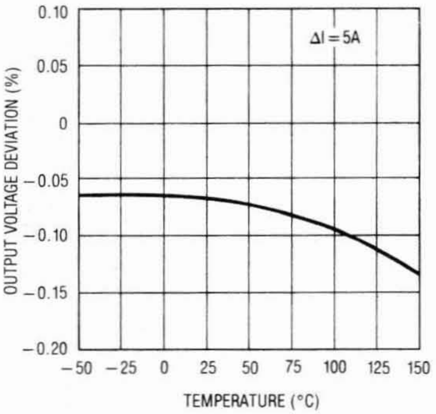
LT1087 Dropout Voltage



LT1087 Short Circuit Current

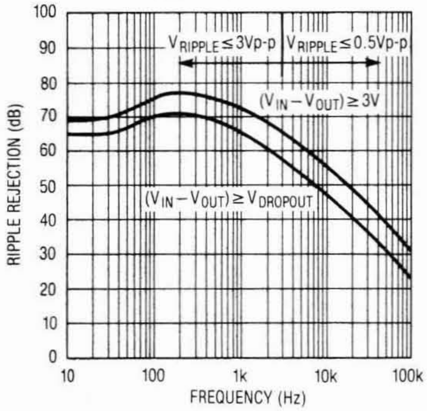


LT1087 Load Regulation

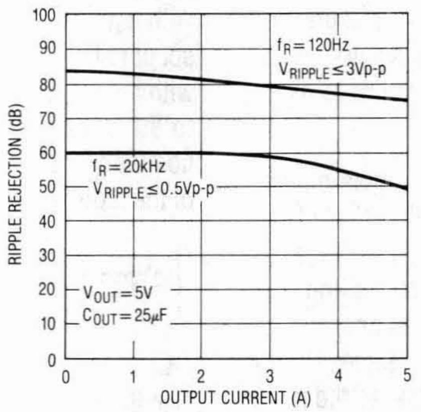


TYPICAL PERFORMANCE CHARACTERISTICS

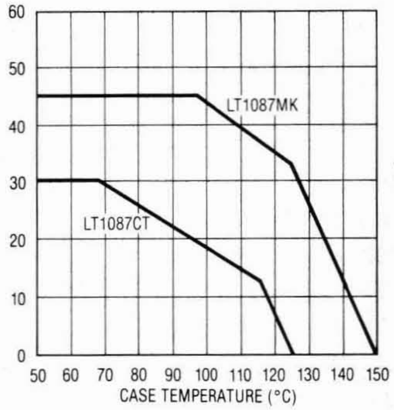
LT1087 Ripple Rejection



LT1087 Ripple Rejection vs Current

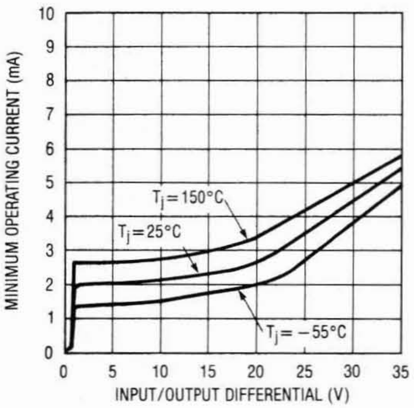


LT1087 Maximum Power Dissipation*

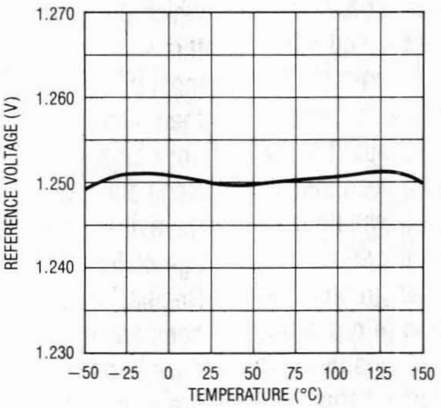


*AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

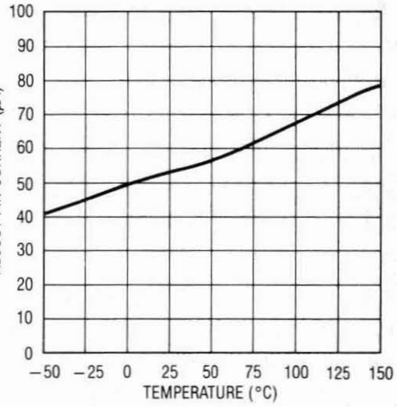
Minimum Operating Current



Temperature Stability



Adjust Pin Current



APPLICATION HINTS

The LT1087 is an adjustable voltage regulator with Kelvin sense inputs. These inputs can be used to fully Kelvin sense a remote load so that the regulation at the load is nearly perfect. The sense inputs can also be used in a 2-wire configuration to compensate for voltage drops in long output leads eliminating the two extra wires needed for full Kelvin sensing.

This regulator is easy to use and has all the protection features that are expected in high performance voltage regulators. They are short circuit protected, have safe area protection as well as thermal shutdown to turn-off the regulator should the temperature exceed about 165°C.

Sense Inputs

In a three terminal regulator the sense inputs are terminated at the output pin of the device (normally the case for adjustable regulators). This means that regulation will be best at the case of the device. Any wire resistance between the regulator and the actual load will degrade the regulation, especially at high currents. This five pin configuration allows the user to select the point where regulation will be optimized.

APPLICATION HINTS

The sense pins can be used in two basic configurations. They can be used to make a remote Kelvin sensed output, or they can be used as a differential amplifier to simply compensate for a long wire run.

For full Kelvin sensing of the output, the sense pins are tied together, then connected through a 1k resistor to the top of the R1/R2 divider that sets the output voltage. The 1k resistor is necessary to prevent high currents from flowing into the sense pins under fault conditions and will cause no significant error in the output voltage. The top and bottom of the R1/R2 divider are then tied to the points in the circuit where optimum regulation is desired. These connections must be made separate from the wires that carry the main load current. See the Remote Kelvin Sensed Output Circuit in the Typical Applications Section. At light load currents the voltage drop down the output lead will be small and the sense pins will be at approximately the same voltage as the output pin. For heavy load currents the output pin will be driven positive with respect to the sense pins by the value of the voltage drop across the output leads and the voltage at the sense points will be regulated. The output is allowed to go 1V above the sense pins in this configuration. For output pin voltages greater than 1V above the sense pins some degradation in regulation will occur. Since the output is allowed to go positive with respect to the sense pins by 1V and assuming that both the power lead to the load and the ground return are approximately equal, this configuration allows the user to have almost perfect regulation at the sense point with 2V of drop in the wire leads between the regulator and the load. Note that the input voltage to the regulator must provide enough headroom to the regulator to allow this to happen. The input voltage must be greater than the total of the regulated output voltage plus the wire drops plus the dropout voltage of the regulator (≈1.5V for LT1087 at 5A).

If the user does not want to run the extra two wires required for full Kelvin sensing, a second method can be used to compensate for wire drops. The sense inputs can be considered to be the inputs to a differential amplifier with a gain of 11 when the +Sense pin is positive with respect to the −Sense pin. Pulling the −Sense pin negative with respect to the +Sense pin (with the +Sense pin tied to the output) by 10mV will cause the reference voltage, nominally 1.25V, to increase by 110mV to 1.36V. The output of the regulator would then increase by the factor

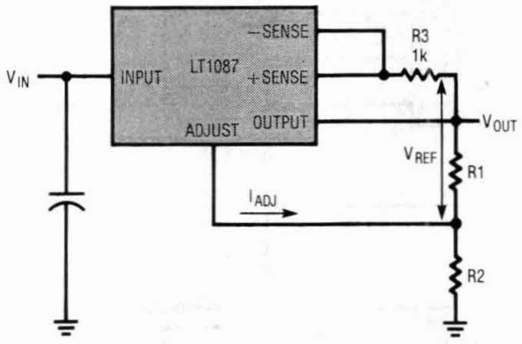
$$\left[\Delta V_{REF}\left(1+\frac{R2}{R1}\right)\right].$$

See the Remote Load Regulation Compensation Circuit in the Typical Applications. In this manner sensing across a small part of the output leads can compensate for the entire length. The maximum differential input voltage over which the differential gain holds true is 60mV at 25°C, and this voltage is proportional to absolute temperature. For most circuits the differential input voltage should be less than 40mV. Exceeding this small differential voltage will not damage the device until the differential exceeds 5V. Regulation, however, will be degraded. Assuming a maximum differential input voltage of 40mV and an output voltage of 5V, and using the formula from the Remote Load Regulation Compensation Circuit, this configuration can compensate out 1.76V of wire drop. For higher output voltages larger wire drops can be compensated out. As in the previous circuit the input voltage to the regulator must provide enough headroom for this to happen.

Output Voltage

The LT1087 develops and tries to maintain a 1.25V reference voltage between its sense pins and its adjust pin (see Figure 1). By placing a resistor between the device's sense point (the end of R3) and its adjust pin, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally R1 is chosen so that the current flowing through it is equal to the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared with the current through R1, it represents a small error and can usually be ignored.

APPLICATION HINTS



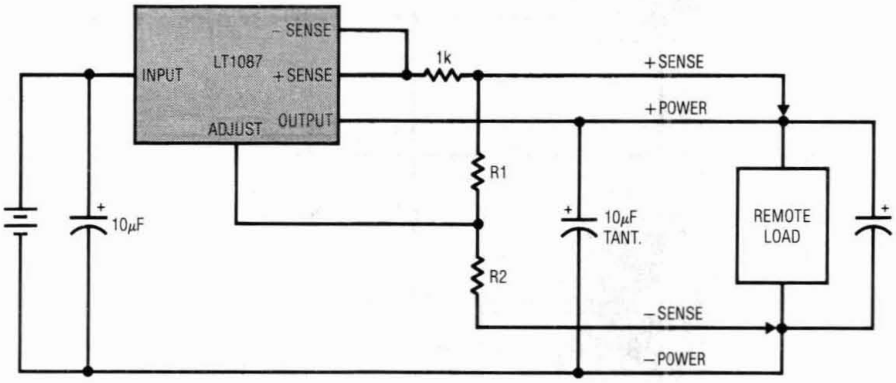
V_{IN}
INPUT
LT1087
–SENSE
+SENSE
ADJUST
OUTPUT
R3
1k
V_{OUT}
V_{REF}
R1
I_{ADJ}
R2

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + I_{ADJ} \bullet R2$$

Figure 1. Standard Connection

TYPICAL APPLICATIONS

Remote Kelvin Sensed Output (4-Wire)



INPUT
LT1087
– SENSE
+SENSE
ADJUST
OUTPUT
1k
+SENSE
+POWER
R1
R2
10μF
10μF
TANT.
REMOTE
LOAD
–SENSE
–POWER

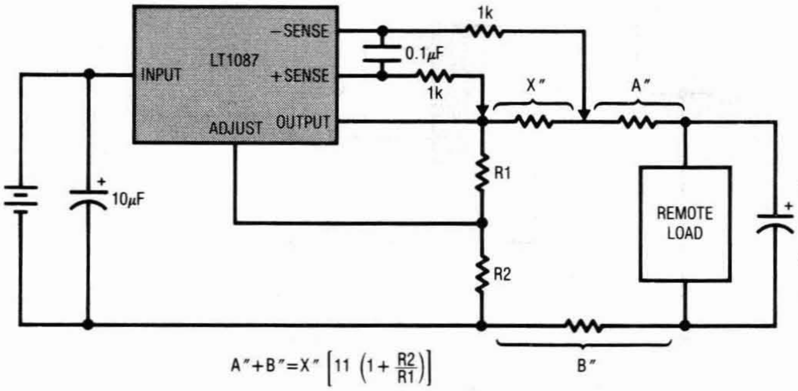
$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right)$

WHERE $V_{REF} = 1.25V$

$C_{LARGE} > 100\mu F$

TYPICAL APPLICATIONS

Remote Load Regulation Compensation (2-Wire)


LT1087
INPUT
–SENSE
+SENSE
ADJUST
OUTPUT
0.1µF
1k
1k
10µF
X″
A″
R1
R2
REMOTE LOAD
B″

$V_{OUT} = V_{REF}\left(1+\frac{R2}{R1}\right)$

WHERE $V_{REF} = 1.25V$

$C_{LARGE} > 100\mu F$

$A'' + B'' = X''\left[11\left(1+\frac{R2}{R1}\right)\right]$

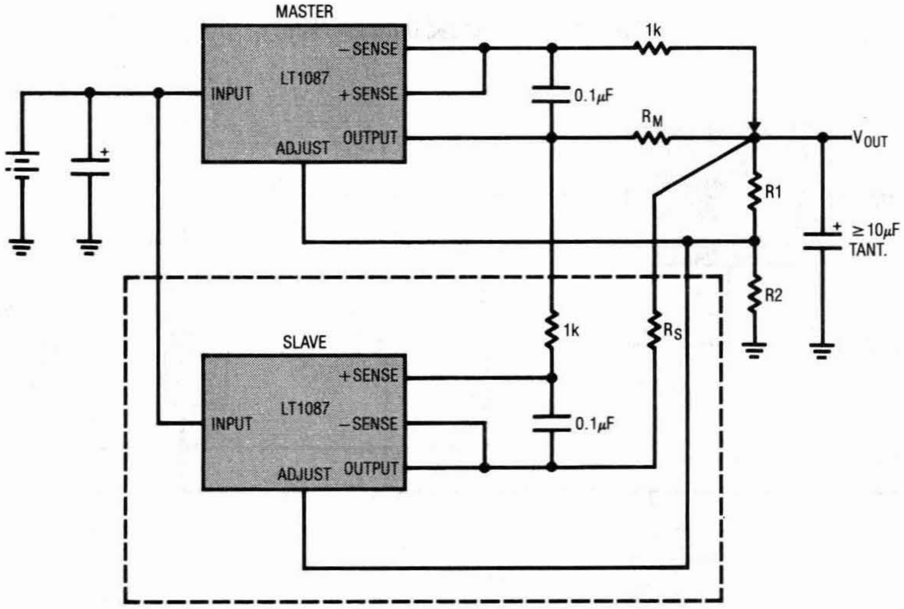
EXAMPLE: IF THE LOAD MUST BE LOCATED
10 FT. (120″) FROM THE REGULATOR
AND V_{OUT} IS 5V

THEN $(A''+B'') = 240''$ $R1 = 120\Omega$, $R2 = 360\Omega$

$X'' = \frac{(A''+B'')}{\left[11\left(1+\frac{R2}{R1}\right)\right]} \rightarrow X'' = 5.2''$

BY CONNECTING THE –SENSE PIN 5.2″ FURTHER DOWN THE OUTPUT WIRE THAN THE +SENSE PIN THE LOAD REGULATION CAUSED BY 20′ OF WIRE CAN BE COMPENSATED OUT.

Paralleling Devices for Higher Current


MASTER
LT1087
INPUT
–SENSE
+SENSE
ADJUST
OUTPUT
0.1µF
1k
R_M
V_{OUT}
R1
R2
≥ 10µF TANT.
SLAVE
LT1087
INPUT
+SENSE
–SENSE
ADJUST
OUTPUT
1k
R_S
0.1µF

FOR PARALLELING MORE THAN TWO DEVICES → DUPLICATE SLAVE SECTION.

MINIMUM LOAD CURRENT = (10mA) (# OF DEVICES IN PARALLEL)
R1, R2 NETWORK CAN BE USED AS THE MINIMUM LOAD

$R_M = 8m\Omega \approx 10''$ OF #20 A.W.G. SOLID WIRE (COPPER)
$R_S = 7.3m\Omega \approx 9.1''$ OF #20 A.W.G. SOLID WIRE (COPPER)

R_M AND R_S SHOULD BE NON-INDUCTIVE. THIS IS EASILY ACCOMPLISHED BY FOLDING THE WIRE BACK UPON ITSELF SO THAT THE FIELDS GENERATED, BY CURRENT FLOWING IN THE WIRE, CANCEL.

LT1117/LT1117-2.85/LT1117-5

800mA Low Dropout Positive Regulators Adjustable and Fixed 2.85V, 5V

FEATURES

- Space Saving SOT-223 Surface Mount Package
- Three Terminal Adjustable or Fixed 2.85V, 5V
- Output Current of 800mA
- Operates Down to 1V Dropout
- Guaranteed Dropout Voltage at Multiple Current Levels
- 0.2% Line Regulation Max
- 0.4% Load Regulation Max

APPLICATIONS

- Active SCSI Terminators
- High Efficiency Linear Regulators
- Post Regulators for Switching Supplies
- Battery Chargers
- 5V - 3.3V Linear Regulators

DESCRIPTION

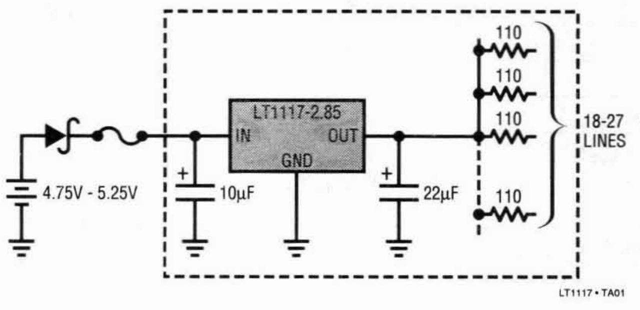
The LT1117 is a positive low dropout regulator designed to provide up to 800mA of output current. The device is available in an adjustable version and fixed output voltages of 2.85V and 5V. The 2.85V version is designed specifically to be used in Active Terminators for the SCSI bus. All internal circuitry is designed to operate down to 1V input to output differential. Dropout voltage is guaranteed at a maximum of 1.2V at 800mA, decreasing at lower load currents. On chip trimming adjusts the reference/output voltage to within ± 1%. Current limit is also trimmed in order to minimize the stress on both the regulator and the power source circuitry under overload conditions.

The low profile surface mount SOT-223 package allows the device to be used in applications where space is limited. The LT1117 requires a minimum of 10µF of output capacitance for stability. Output capacitors of this size or larger are normally included in most regulator designs.

Unlike PNP type regulators where up to 10% of the output current is wasted as quiescent current, the quiescent current of the LT1117 flows into the load, increasing efficiency.

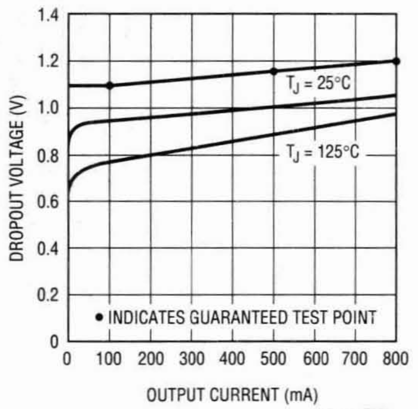
TYPICAL APPLICATION

Active Terminator for SCSI-2 Bus



LT1117 • TA01

Dropout Voltage (V_{IN} - V_{OUT})

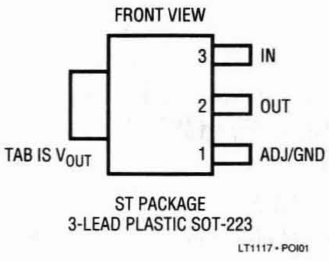


LT1117 • TPC01

ABSOLUTE MAXIMUM RATINGS

Input Voltage
Operating Voltage
LT1117, LT1117-5 .... 15V
LT1117-2.85 .... 10V
Surge Voltage
LT1117, LT1117-5 .... 20V
Operating JunctionTemperature Range...... 0°C to 125°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature .... (See Soldering Methods)

PACKAGE/ORDER INFORMATION



ST PACKAGE
3-LEAD PLASTIC SOT-223

LT1117 • POI01

ORDER PART NUMBER	PART MARKING
LT1117CST	1117
LT1117CST-2.85	11172
LT1117CST-5	11175

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage	LT1117	I_{OUT} = 10mA, (V_{IN} - V_{OUT}) = 2V, T_J = 25°C		1.238	1.250	1.262	V
		10 ≤ I_{OUT} ≤ 800mA, 1.4V ≤ (V_{IN} - V_{OUT}) ≤ 10V	●	1.225	1.250	1.270	
Output Voltage	LT1117-2.85	I_{OUT} = 10mA, V_{IN} = 4.85V, T_J = 25°C		2.820	2.850	2.880	V
		0 ≤ I_{OUT} ≤ 800mA, 4.25V ≤ V_{IN} ≤ 10V	●	2.790	2.850	2.910	
		0 ≤ I_{OUT} ≤ 500mA, V_{IN} = 3.95V	●	2.790	2.850	2.910	
	LT1117-5	I_{OUT} = 10mA, V_{IN} = 7V, T_J = 25°C		4.950	5.000	5.050	V
		0 ≤ I_{OUT} ≤ 800mA, 6.50V ≤ V_{IN} ≤ 12V	●	4.900	5.000	5.100	
Line Regulation	LT1117	I_{OUT} = 10mA, 1.5V ≤ V_{IN} - V_{OUT} ≤ 15V (Note 1)	●		0.035	0.2	%
	LT1117-2.85	I_{OUT} = 0mA, 4.25V ≤ V_{IN} ≤ 10V (Note 1)	●		1	6	mV
	LT1117-5	I_{OUT} = 0mA, 6.5V ≤ V_{IN} ≤ 15V (Note 1)	●		1	10	
Load Regulation	LT1117	(V_{IN} - V_{OUT}) = 3V, 10mA ≤ I_{OUT} ≤ 800mA (Note 1)	●		0.1	0.4	%
	LT1117-2.85	V_{IN} = 4.25V, 0 ≤ I_{OUT} ≤ 800mA (Note 1)	●		1	10	mV
	LT1117-5	V_{IN} = 6.5V, 0 ≤ I_{OUT} ≤ 800mA (Note 1)	●		1	15	
Dropout Voltage		I_{OUT} = 100mA (Note 2)	●		1.00	1.10	V
		I_{OUT} = 500mA (Note 2)	●		1.05	1.15	
		I_{OUT} = 800mA (Note 2)	●		1.10	1.20	
Current Limit		(V_{IN} - V_{OUT}) = 5V, T_J = 25°C,		800	950	1200	mA
Minimum Load Current	LT1117	(V_{IN} - V_{OUT}) = 15V (Note 3)	●		1.7	5	mA
Quiescent Current	LT1117-2.85	V_{IN} ≤ 10V	●		5	10	mA
	LT1117-5	V_{IN} ≤ 15V	●		5	10	mA
Thermal Regulation		T_A = 25°C, 30ms Pulse			0.01	0.1	%/W
Ripple Rejection		f_{RIPPLE} = 120Hz, (V_{IN} - V_{OUT}) = 3V, V_{RIPPLE} = 1Vp-p	●	60	75		dB
Adjust Pin Current			●		55	120	μA
Adjust Pin Current Change		10mA ≤ I_{OUT} ≤ 800mA, 1.4V ≤ (V_{IN} - V_{OUT}) ≤ 10V	●		0.2	5	μA
Temperature Stability					0.5		%
Long Term Stability		T_A = 125°C, 1000Hrs			0.3		%
RMS Output Noise		(% of V_{OUT}), 10Hz ≤ f ≤ 10kHz			0.003		%
Thermal Resistance		(Junction to Case, at Tab)			15		°C/W

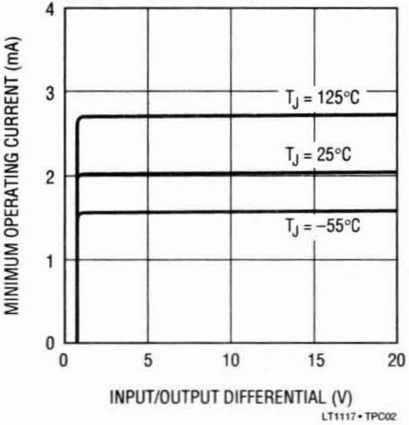
The ● denotes specifications which apply over the full operating temperature range.

Note 1: See thermal regulation specification for changes in output voltage due to heating effects. Load regulation and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

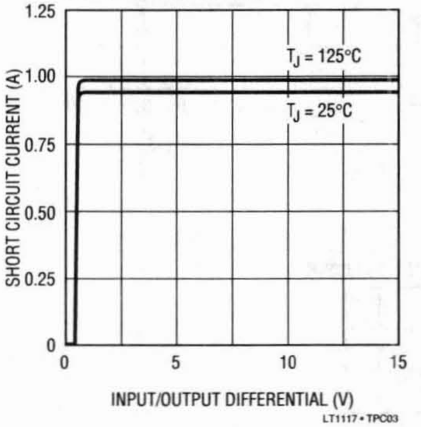
Note 2: Dropout voltage is specified over the full output current range of the device. Dropout voltage is defined as the minimum input/output differential measured at the specified output current. Test points and limits are also shown on the Dropout Voltage curve.

Note 3: Minimum load current is defined as the minimum output current required to maintain regulation.

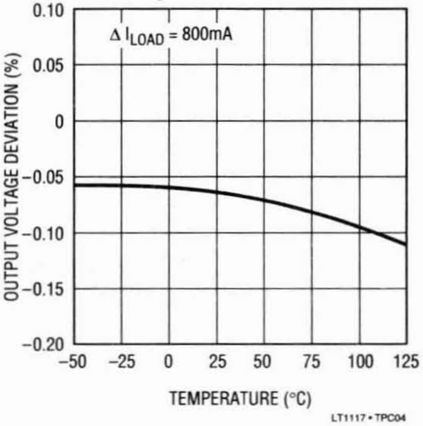
TYPICAL PERFORMANCE CHARACTERISTICS



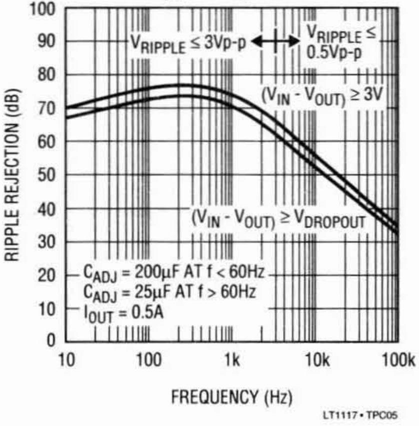
Minimum Operating Current (Adjustable Device)



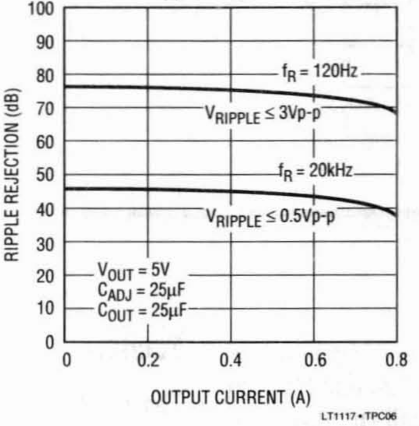
Short Circuit Current



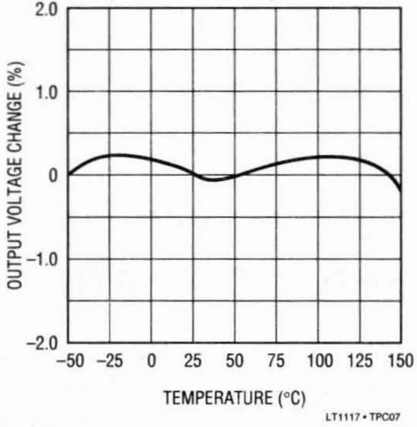
Load Regulation



LT1117 Ripple Rejection

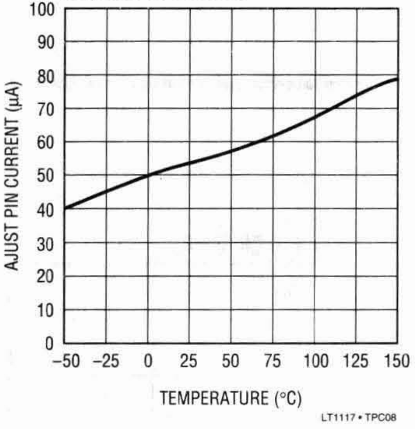


LT1117 Ripple Rejection vs Current

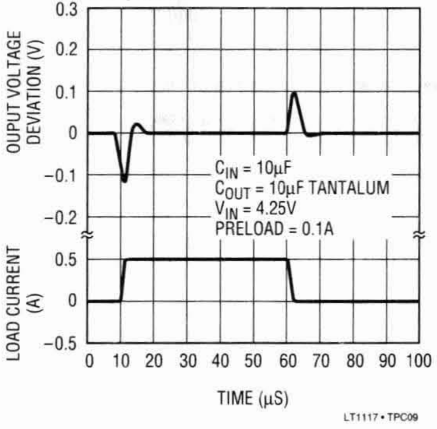


Temperature Stability

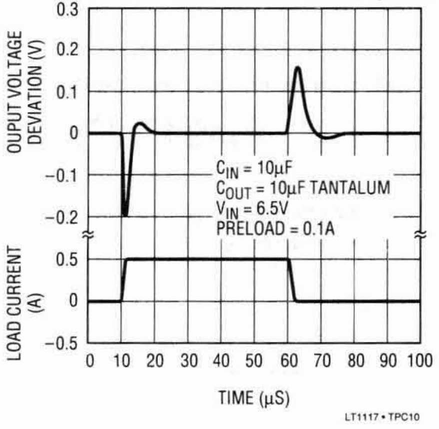
TYPICAL PERFORMANCE CHARACTERISTICS



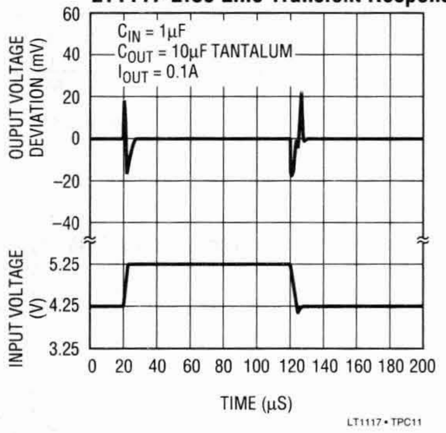
Adjust Pin Current



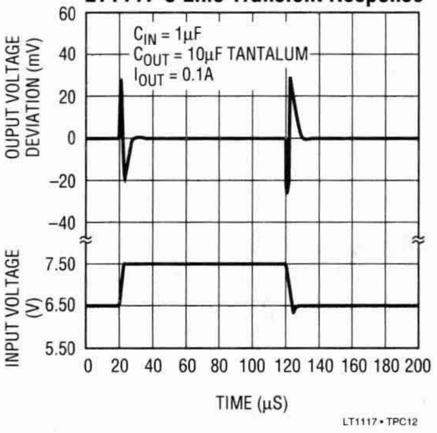
LT1117-2.85 Load Transient Response



LT1117-5 Load Transient Response



LT1117-2.85 Line Transient Response



LT1117-5 Line Transient Response

APPLICATION HINTS

The LT1117 family of three terminal regulators are easy to use. They are protected against short circuit and thermal overloads. Thermal protection circuitry will shutdown the regulator should the junction temperature exceed 165°C at the sense point. These regulators are pin compatible with older three terminal adjustable regulators, offer lower dropout voltage and more precise reference tolerance. Reference stability over temperature is improved over older types of regulators.

Stability

The LT1117 family of regulators requires an output capacitor as part of the device frequency compensation. A minimum of 10μF of tantalum or 50μF of aluminum electrolytic is required. The ESR of the output capacitor should be less than 0.5Ω. Surface mount tantalum capacitors, which have very low ESR, are available from several manufacturers.

APPLICATION HINTS

When using the LT1117 adjustable device the adjust terminal can be bypassed to improve ripple rejection. When the adjust terminal is bypassed the required value of the output capacitor increases. The device will require an output capacitor of 22µF tantalum or 150µF aluminum electrolytic when the adjust pin is bypassed.

Normally, capacitor values on the order of 100µF are used in the output of many regulators to ensure good load transient response with large load current changes. Output capacitance can be increased without limit and larger values of output capacitance further improve stability and transient response.

Protection Diodes

In normal operation, the LT1117 family does not need any protection diodes. Older adjustable regulators required protection diodes between the adjust pin and the output and between the output and input to prevent over stressing the die. The internal current paths on the LT1117 adjust pin are limited by internal resistors. Therefore, even with capacitors on the adjust pin, no protection diode is needed to ensure device safety under short circuit conditions. The adjust pin can be driven, on a transient basis, ±25V with respect to the output without any device degradation.

Diodes between input and output are not usually needed. The internal diode between the output and input pins of the device can withstand microsecond surge currents of 10A to 20A. Normal power supply cycling can not generate currents of this magnitude. Only with extremely large output capacitors, such as 1000µF and larger, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input of the LT1117 in combination with a large output capacitor could generate currents large enough to cause damage. In this case a diode from output to input is recommended, as shown in Figure 1.

Output Voltage

The LT1117 develops a 1.25V reference voltage between the output and the adjust terminal (see Figure 2). By placing a resistor between these two terminals, a constant current is caused to flow through R1 and down through R2 to set the overall output voltage. Normally this current is chosen to be the specified minimum load current of 10mA. Because I_{ADJ} is very small and constant when compared to the current through R1, it represents a small error and can usually be ignored. For fixed voltage devices R1 and R2 are included in the device.

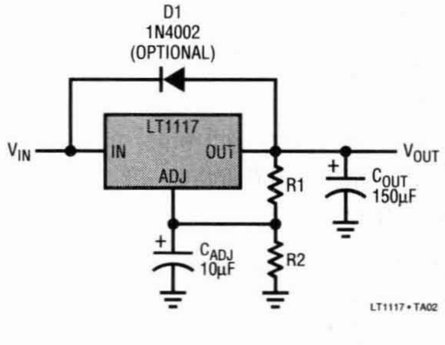


Figure 1.

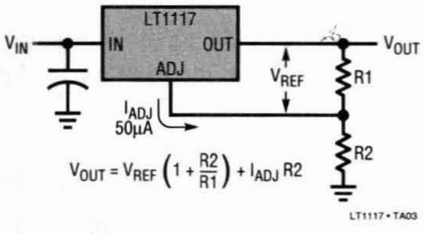


Figure 2. Basic Adjustable Regulator

APPLICATION HINTS

Load Regulation

Because the LT1117 is a three terminal device, it is not possible to provide true remote load sensing. Load regulation will be limited by the resistance of the wire connecting the regulator to the load. The data sheet specification for load regulation is measured at the output pin of the device. Negative side sensing is a true Kelvin connection, with the bottom of the output divider returned to the negative side of the load. Although it may not be immediately obvious, best load regulation is obtained when the top of the resistor divider (R1) is returned directly to the output pin of the device, not to the load. This is illustrated in Figure 3. Connected as shown, Rp is not multiplied by the divider ratio. If R1 were connected to the load, the effective resistance between the regulator and the load would be:

$$R_p \times \frac{R2+R1}{R1}, R_p = \text{Parasitic Line Resistance}$$

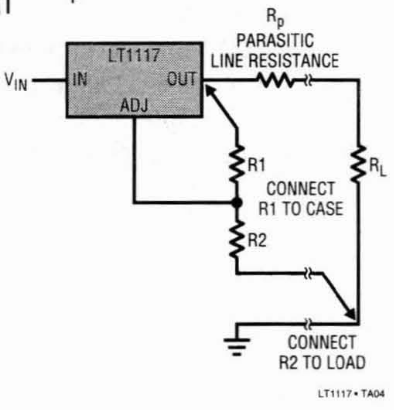


Figure 3. Connections for Best Load Regulation

For fixed voltage devices the top of R1 is internally Kelvin connected, and the ground pin can be used for negative side sensing.

Thermal Considerations

LT1117 series regulators have internal thermal limiting circuitry designed to protect the device during overload conditions. For continuous normal load conditions however, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. For the SOT-223 package, which is designed to be surface mounted, additional heat sources mounted near the device must also be considered. Heat sinking is accomplished using the heat spreading capability of the PC board and its copper traces. The thermal resistance of the LT1117 is 15°C/W from the junction to the tab. Thermal resistances from tab to ambient can be as low as 30°C/W. The total thermal resistance from junction to ambient can be as low as 45°C/W. This requires a reasonable sized PC board with at least one layer of copper to spread the heat across the board and couple it into the surrounding air. Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PC material can be very effective at transmitting heat between the pad area, attached to the tab of the device, and a ground plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PC material is high, the Length/ Area ratio of the thermal resistor between layers is small. The data in Table 1 was taken using 1/16" FR-4 board with 1oz. copper foil. It can be used as a rough guideline in estimating thermal resistance.

Table. 1

Copper Area			
Topside*	**Backside**	**Board Area**	**Thermal Resistance (Junction to Ambient)**
2500 Sq. mm	2500 Sq. mm	2500 Sq. mm	45°C/W
1000 Sq. mm	2500 Sq. mm	2500 Sq. mm	45°C/W
225 Sq. mm	2500 Sq. mm	2500 Sq. mm	53°C/W
100 Sq. mm	2500 Sq. mm	2500 Sq. mm	59°C/W
1000 Sq. mm	1000 Sq. mm	1000 Sq. mm	52°C/W
1000 Sq. mm	0	1000 Sq. mm	55°C/W

* Tab of device attached to topside copper

The thermal resistance for each application will be affected by thermal interactions with other components on the board. Some experimentation will be necessary to determine the actual value.

The power dissipation of the LT1117 is equal to:

$$Pd = (V_{IN} - V_{OUT})(I_{OUT})$$

Maximum junction temperature will be equal to:

$$T_J = \text{Tambient (Max)} + \text{Pd (Thermal Resistance (junction to ambient))}$$

Maximum junction temperature must not exceed 125°C.

APPLICATION HINTS

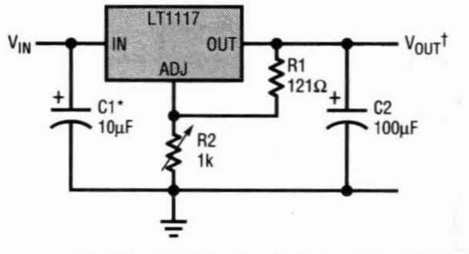
Ripple Rejection

The curves for Ripple Rejection were generated using an adjustable device with the adjust pin bypassed. These curves will hold true for all values of output voltage. For proper bypassing, and ripple rejection approaching the values shown, the impedance of the adjust pin capacitor, at the ripple frequency, should be < R1. R1 is normally in the range of 100Ω-200Ω. The size of the required adjust pin capacitor is a function of the input ripple frequency. At 120Hz, with R1=100Ω, the adjust pin capacitor should be > 13µF. At 10kHz only 0.16µF is needed.

For fixed voltage devices, and adjustable devices without an adjust pin capacitor, the output ripple will increase as the ratio of the output voltage to the reference voltage (V_{OUT}/V_{REF}). For example, with the output voltage equal to 5V, the output ripple will be increased by the ratio of 5V/1.25V. It will increase by a factor of four. Ripple rejection will be degraded by 12dB from the value shown on the curve.

TYPICAL APPLICATIONS

1.2V-10V Adjustable Regulator

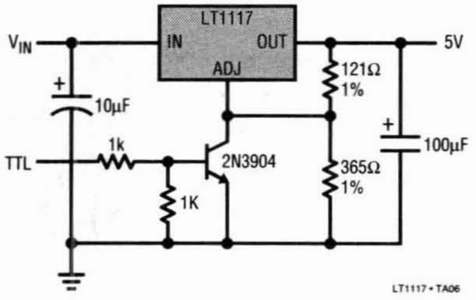


LT1117
IN
OUT
ADJ
V_{IN}
V_{OUT}†
R1
121Ω
C1*
10µF
R2
1k
C2
100µF
LT1117 • TA05

* NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

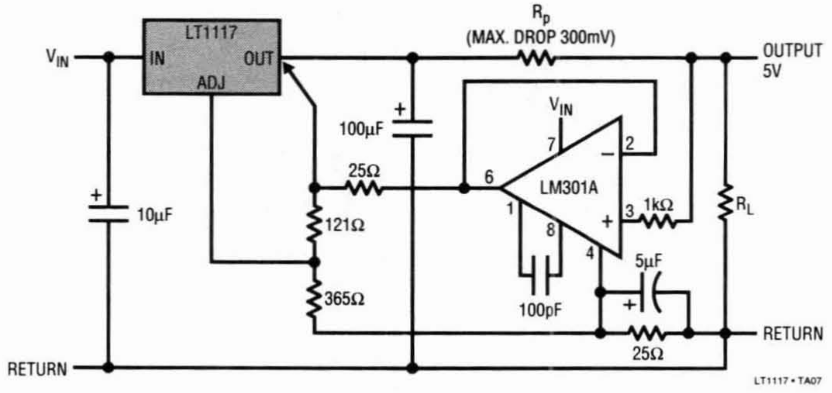
† $V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$

5V Regulator with Shutdown



LT1117
IN
OUT
ADJ
V_{IN}
5V
10µF
121Ω
1%
TTL
1k
2N3904
1K
365Ω
1%
100µF
LT1117 • TA06

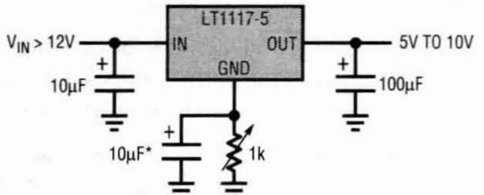
Remote Sensing



LT1117
IN
OUT
ADJ
V_{IN}
R_p
(MAX. DROP 300mV)
OUTPUT
5V
V_{IN}
7
2
100µF
25Ω
6
LM301A
1
3
1kΩ
R_L
8
10µF
121Ω
4
5µF
365Ω
100pF
RETURN
25Ω
RETURN
LT1117 • TA07

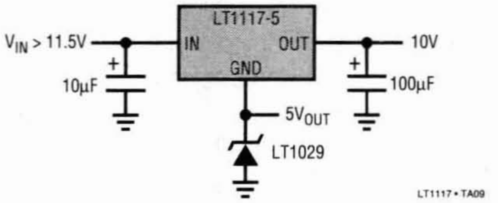
TYPICAL APPLICATIONS

Adjusting Output Voltage of Fixed Regulators

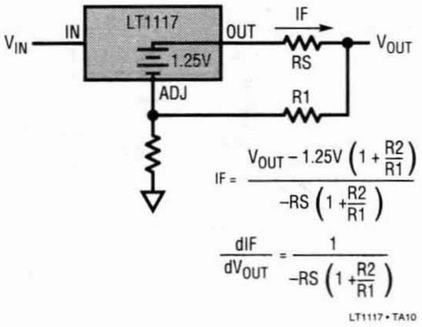

LT1117-5
V_{IN} > 12V
IN
OUT
GND
5V TO 10V
10µF
100µF
10µF*
1k
LT1117 • TA08

* OPTIONAL IMPROVES RIPPLE REJECTION

Regulator with Reference


LT1117-5
V_{IN} > 11.5V
IN
OUT
GND
10V
10µF
100µF
$5V_{OUT}$
LT1029
LT1117 • TA09

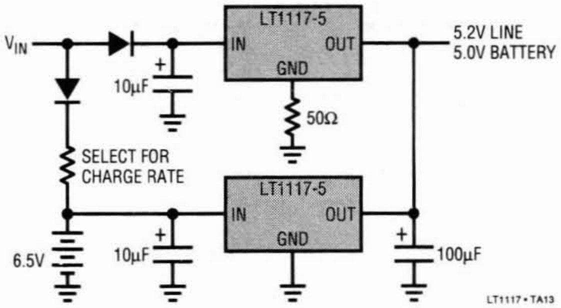
Battery Charger


LT1117
V_{IN}
IN
OUT
1.25V
ADJ
IF
RS
R1
V_{OUT}
LT1117 • TA10

$$IF = \frac{V_{OUT} - 1.25V\left(1 + \frac{R2}{R1}\right)}{-RS\left(1 + \frac{R2}{R1}\right)}$$

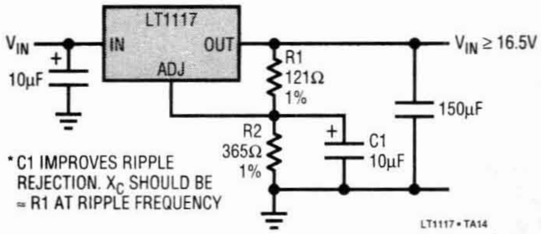
$$\frac{dIF}{dV_{OUT}} = \frac{1}{-RS\left(1 + \frac{R2}{R1}\right)}$$

Battery Backed Up Regulated Supply


V_{IN}
LT1117-5
IN
OUT
GND
5.2V LINE
5.0V BATTERY
10µF
50Ω
SELECT FOR
CHARGE RATE
LT1117-5
IN
OUT
GND
6.5V
10µF
100µF
LT1117 • TA13

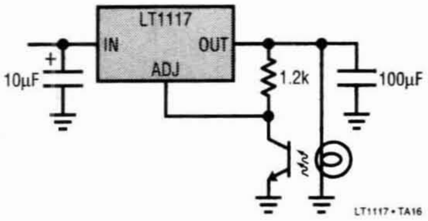
TYPICAL APPLICATIONS

Improving Ripple Rejection

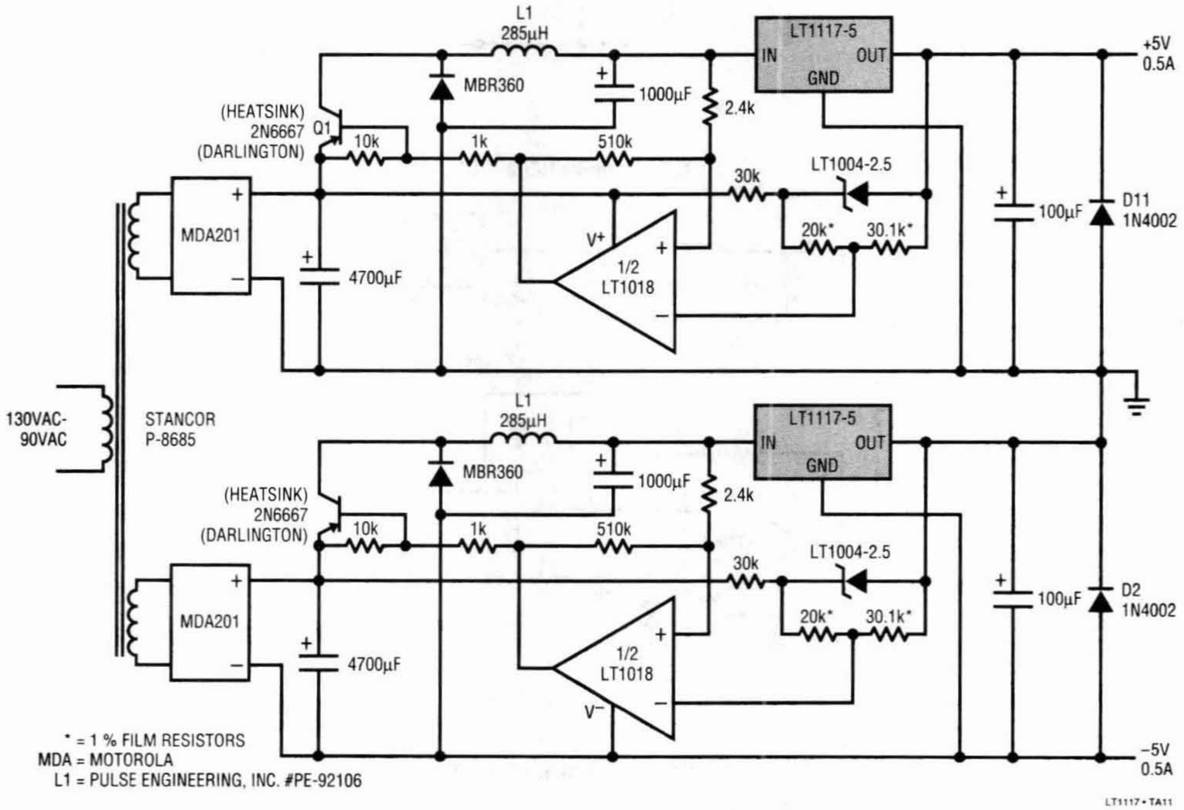

LT1117
IN
OUT
ADJ
V_IN
10µF
+
V_IN ≥ 16.5V
R1
121Ω
1%
R2
365Ω
1%
C1
10µF
150µF
LT1117 • TA14

*C1 IMPROVES RIPPLE REJECTION. X_C SHOULD BE ≈ R1 AT RIPPLE FREQUENCY

Automatic Light Control


LT1117
IN
OUT
ADJ
10µF
+
1.2k
100µF
LT1117 • TA16

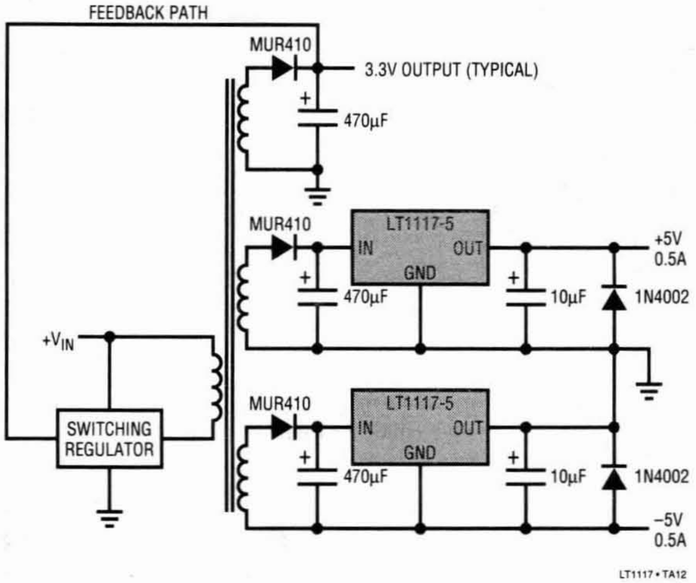
High Efficiency Dual Linear Supply


L1
285µH
LT1117-5
IN
OUT
GND
+5V
0.5A
MBR360
1000µF
2.4k
(HEATSINK)
2N6667
(DARLINGTON)
Q1
10k
1k
510k
30k
LT1004-2.5
100µF
D11
1N4002
MDA201
V+
1/2
LT1018
20k*
30.1k*
4700µF
130VAC-
90VAC
STANCOR
P-8685
L1
285µH
LT1117-5
IN
OUT
GND
MBR360
1000µF
2.4k
(HEATSINK)
2N6667
(DARLINGTON)
10k
1k
510k
30k
LT1004-2.5
100µF
D2
1N4002
MDA201
20k*
30.1k*
1/2
LT1018
V−
4700µF
−5V
0.5A
LT1117 • TA11

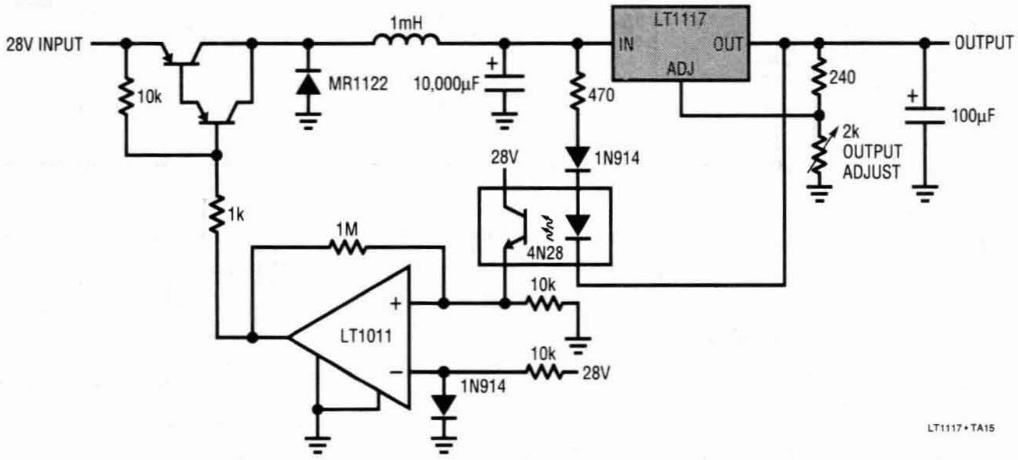
* = 1 % FILM RESISTORS
MDA = MOTOROLA
L1 = PULSE ENGINEERING, INC. #PE-92106

TYPICAL APPLICATIONS

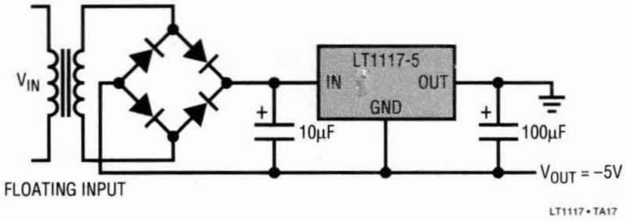
High Efficiency Dual Supply


FEEDBACK PATH
MUR410
3.3V OUTPUT (TYPICAL)
470μF
MUR410
LT1117-5
IN
OUT
GND
+5V
0.5A
470μF
10μF
1N4002
+V_{IN}
MUR410
LT1117-5
IN
OUT
GND
SWITCHING REGULATOR
470μF
10μF
1N4002
–5V
0.5A
LT1117 • TA12

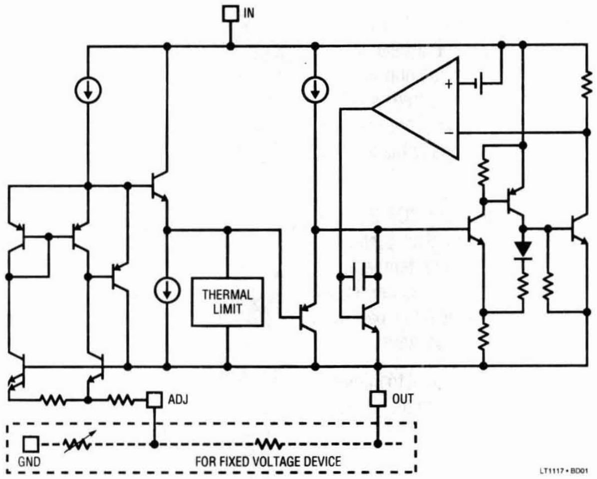
High Efficiency Regulator


28V INPUT
10k
1mH
MR1122
10,000μF
LT1117
IN
OUT
ADJ
OUTPUT
470
240
100μF
2k
OUTPUT ADJUST
28V
1N914
1k
4N28
1M
LT1011
10k
10k
28V
1N914
LT1117 • TA15

Low Dropout Negative Supply

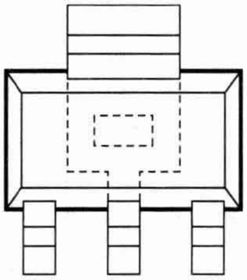

V_{IN}
LT1117-5
IN
OUT
GND
10μF
100μF
V_{OUT} = –5V
FLOATING INPUT
LT1117 • TA17

BLOCK DIAGRAM


IN
THERMAL LIMIT
+
−
ADJ
OUT
GND
FOR FIXED VOLTAGE DEVICE
LT1117 • BD01

SOLDERING METHODS

The SOT-223 is manufactured with gull wing leadform for surface mount applications. The leads and heatsink are solder plated and allow easy soldering using non-active or mildly active fluxes. The package is constructed with three leads exiting one side of the package and one heatsink exiting the other side, and the die attached to the heatsink internally.



The recommended methods of soldering SOT-223 are: vapor phase reflow and infrared reflow with preheat of component to within 65°C of the solder temperature. Hand soldering and wave soldering are not recommended since these methods can easily damage the part with excessive thermal gradients across the package.

Care must be exercised during surface mount to minimize large (> 30°C per second) thermal shock to the package.

LT1123

Low Dropout Regulator Driver

FEATURES

- Extremely Low Dropout
- Low Cost
- Fixed 5V Output, Trimmed to ±1%
- 700μA Quiescent Current
- 3-Pin TO-92 Package
- 1mV Line Regulation
- 5mV Load Regulation
- Thermal Limit
- 4A Output Current Guaranteed

DESCRIPTION

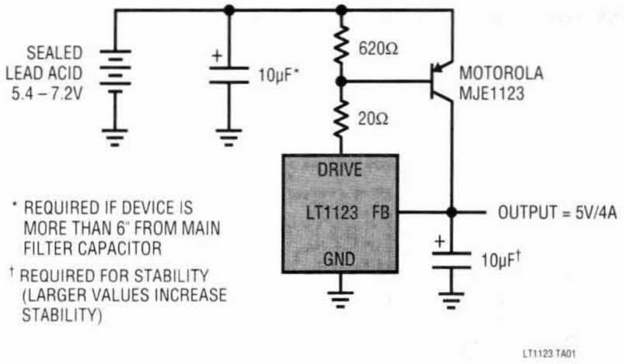
The LT1123 is a 3-pin bipolar device designed to be used in conjunction with a discrete PNP power transistor to form an inexpensive low dropout regulator. The LT1123 consists of a trimmed bandgap reference, error amplifier, and a driver circuit capable of sinking up to 125mA from the base of the external PNP pass transistor. The LT1123 is designed to provide a fixed output voltage of 5V.

The drive pin of the device can pull down to 2V at 125mA (1.4V at 10mA). This allows a resistor to be used to reduce the base drive available to the PNP and minimize the power dissipation in the LT1123. The drive current of the LT1123 is folded back as the feedback pin approaches ground to further limit the available drive current under short circuit conditions.

Total quiescent current for the LT1123 is only 700μA. The device is available in a low cost TO-92 package.

TYPICAL APPLICATION

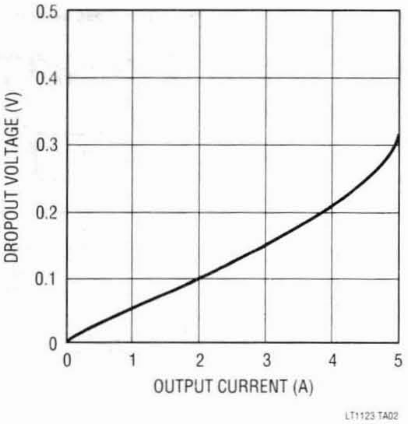
5V Low Dropout Regulator



* REQUIRED IF DEVICE IS MORE THAN 6" FROM MAIN FILTER CAPACITOR

† REQUIRED FOR STABILITY (LARGER VALUES INCREASE STABILITY)

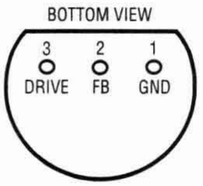
Dropout Voltage



ABSOLUTE MAXIMUM RATINGS

Drive Pin Voltage (V_{DRIVE} to Ground)	30V
Feedback Pin Voltage (V_{FB} to Ground)	30V
Operating Junction Temperature Range	0°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

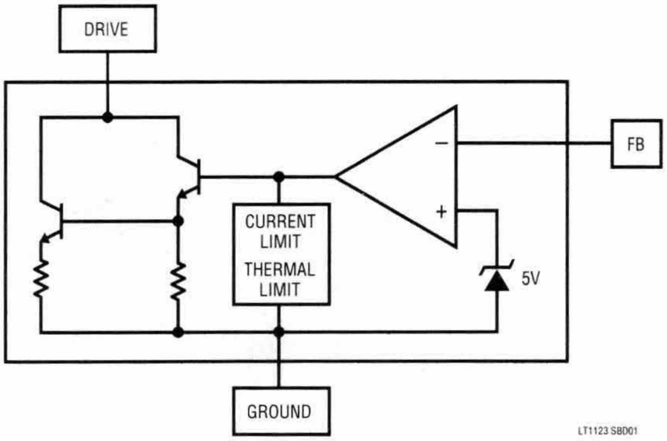
	ORDER PART NUMBER
 Z PACKAGE 3-LEAD TO-92 PLASTIC	LT1123CZ

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Voltage	I_{DRIVE} = 10mA, T_J = 25°C		4.90	5.00	5.10	V
	5mA ≤ I_{DRIVE} ≤ 100mA 3V ≤ V_{DRIVE} ≤ 20V	●	4.80	5.00	5.20	V
Feedback Pin Bias Current	V_{FB} = 5.00V, 2V ≤ V_{DRIVE} ≤ 15V	●		300	500	μA
Drive Current	V_{FB} = 5.20V, 2V ≤ V_{DRIVE} ≤ 15V	●		0.45	1.0	mA
	V_{FB} = 4.80V, V_{DRIVE} = 3V	●	125	170		
	V_{FB} = 0.5V, V_{DRIVE} = 3V, ≤ T_J ≤ 100°C		25	100	150	
Drive Pin Saturation Voltage	I_{DRIVE} = 10mA, V_{FB} = 4.5V			1.4		V
	I_{DRIVE} = 125mA, V_{FB} = 4.5V			2.0		
Line Regulation	5V < V_{DRIVE} < 20V	●		1.0	±20	mV
Load Regulation	ΔI_{DRIVE} = 10 to 100mA	●		−5	−50	mV
Temperature Coefficient of V_{OUT}				0.2		mV/°C

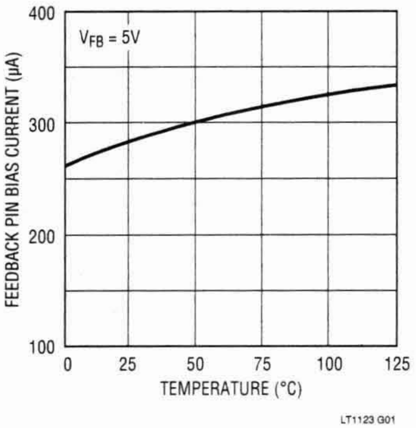
The ● indicates specifications which apply over the full operating temperature range.

SIMPLIFIED BLOCK DIAGRAM

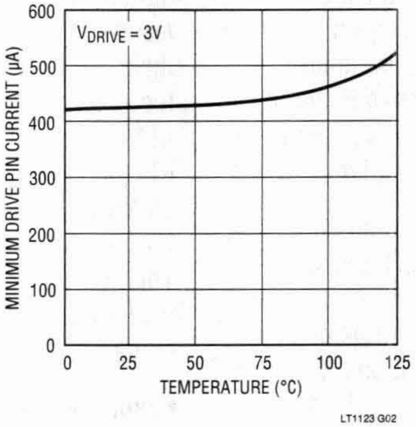


TYPICAL PERFORMANCE CHARACTERISTICS

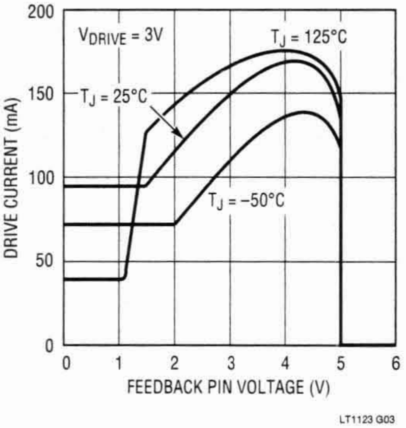
Feedback Pin Bias Current vs Temperature



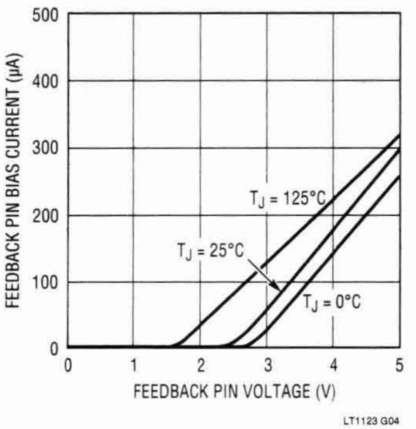
Minimum Drive Pin Current vs Temperature



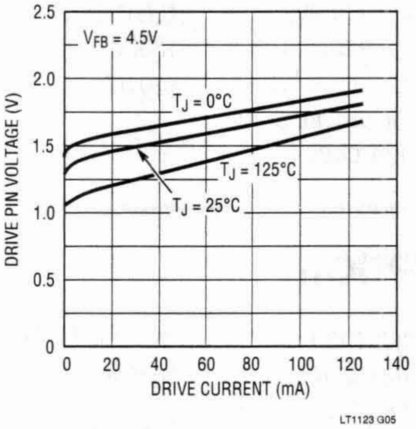
Drive Current vs Feedback Pin Voltage



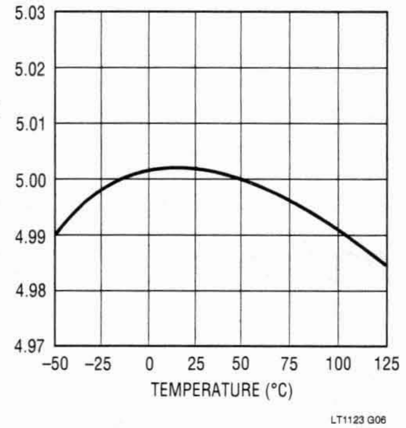
Feedback Pin Bias Current vs Feedback Pin Voltage



Drive Pin Saturation Voltage vs Drive Current



Output Voltage vs Temperature



FUNCTIONAL DESCRIPTION

The LT1123 is a three pin device designed to be used in conjunction with a discrete PNP transistor to form an inexpensive ultra-low dropout regulator. The device incorporates a trimmed 5V bandgap reference, error amplifier, a current-limited Darlington driver, and an internal thermal limit circuit. The internal circuitry connected to the drive pin is designed to function at the saturation voltage of the Darlington driver. This allows a resistor to be inserted in series with the drive pin. This resistor is used to limit the base drive to the PNP and also to limit the power dissipation in the LT1123. The value of this resistor will be defined by the operating requirements of the regulator circuit. The LT1123 is designed to sink a minimum of 125mA of base current. This is sufficient base drive to form a regulator circuit which can supply output currents up to 4A at a dropout voltage of less than 0.75V.

PIN FUNCTIONS

Drive Pin: The drive pin serves two functions. It provides current to the LT1123 for its internal circuitry including startup, bias, current limit, thermal limit and a portion of the base drive current for the output Darlington. The sum total of these currents (450μA typical) is equal to the minimum drive current. This current is listed in the specifications as Drive Current with V_{FB} = 5.2V. This is the minimum current required by the drive pin of the LT1123.

The second function of the drive pin is to sink the base drive current of the external PNP pass transistor. The available drive current is specified for two conditions. Drive current with V_{FB} = 4.80V gives the range of current available under nominal operating conditions, when the device is regulating. Drive current with V_{FB} = 0.5V gives the range of drive current available with the feedback pin pulled low as it would be during startup or during a short circuit fault. The drive current available when the feedback pin is pulled low is less than the drive current available when the device is regulating (V_{FB} = 5V). This can be seen in the curve of Drive Current vs V_{FB} Voltage in the Typical Performance Characteristic curves. This can provide some foldback in the current limit of the regulator circuit.

All internal circuitry connected to the drive pin is designed to operate at the saturation voltage of the Darlington output driver (1.4 – 2V). This allows a resistor to be inserted between the base of the external PNP device and the drive pin. This resistor is used to limit the base drive to the external PNP below the value set internally by the LT1123, and also to help limit power dissipation in the LT1123. The operating voltage range of this pin is from 0V to 30V. Pulling this pin below ground by more than one V_{BE} will forward bias the substrate diode of the device. This condition can only occur if the power supply leads are reversed and will not damage the device if the current is limited to less than 200mA.

Feedback Pin (V_{FB}): The feedback pin also serves two functions. It provides a path for the bias current of the reference and error amplifier and contributes a portion of the drive current for the Darlington output driver. The sum total of these currents is the Feedback Pin Bias Current (300μA typical). The second function of this pin is to provide the voltage feedback to the error amplifier.

APPLICATIONS INFORMATION

The LT1123 is designed to be used in conjunction with an external PNP transistor. The overall specifications of a regulator circuit using the LT1123 and an external PNP will be heavily dependent on the specifications of the external PNP. While there are a wide variety of PNP transistors available that can be used with the LT1123, the specifications given in typical transistor data sheets are of little use in determining overall circuit performance.

Linear Technology has solved this problem by cooperating with Motorola to design and specify the MJE1123. This transistor is specifically designed to work with the LT1123 as the pass element in a low dropout regulator. The specifications of the MJE1123 reflect the capability of the LT1123. For example, the dropout voltage of the MJE1123 is specified up to 4A collector current with base drive currents that the LT1123 is capable of generating (20mA to 120mA). Output currents up to 4A with dropout voltages less than 0.75V can be guaranteed.

The following sections describe how specifications can be determined for the basic regulator. The charts and graphs are based on the combined characteristics of the LT1123 and the MJE1123. Formulas are included that will enable the user to substitute other transistors that have been characterized. A chart is supplied that lists suggested resistor values for the most popular range of input voltages and output current.

BASIC REGULATOR CIRCUIT

The basic regulator circuit is shown in Figure 1. The LT1123 senses the voltage at its feedback pin and drives the base of the PNP (MJE1123) in order to maintain the

APPLICATIONS INFORMATION

output at 5V. The drive pin of the LT1123 can only sink current; R_B is required to provide pullup on the base of the PNP. R_B must be sized so that the voltage drop caused by the minimum drive pin current is less than the emitter/base voltage of the external PNP at light loads. The recommended value for R_B is 620Ω. For circuits that are required to run at junction temperatures in excess of 100°C the recommended value of R_B is 300Ω.

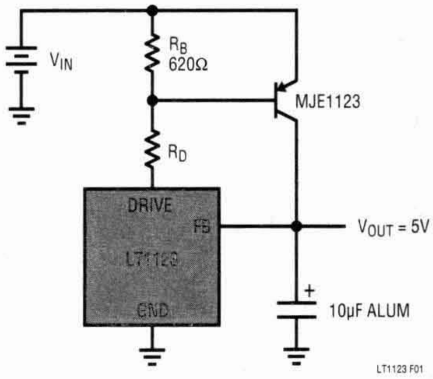


Figure 1. Basic Regulator Circuit

R_D is used to limit the drive current available to the PNP and to limit the power dissipation in the LT1123. Limiting the drive current to the PNP will limit the output current of the regulator which will minimize the stress on the regulator circuit under overload conditions. R_D is chosen based on the operating requirements of the circuit, primarily dropout voltage and output current.

DROPOUT VOLTAGE

The dropout voltage of an LT1123 based regulator circuit is determined by the V_{CE} saturation voltage of the discrete PNP when it is driven with a base current equal to the available drive current of the LT1123. The LT1123 can sink up to 150mA of base current (150mA typ., 125mA min.) when output voltage is up near the regulating point (5V). The available drive current of the LT1123 can be reduced by adding a resistor (R_D) in series with the drive pin (see the section below on current limit). The MJE1123 is specified for dropout voltage (V_{CE} sat.) at several values of output current and up to 120mA of base drive current. The chart below lists the operating points that can be guaranteed by the combined data sheets of the LT1123 and MJE1123. Figure 2 illustrates the chart in graphic form. Although these numbers are only guaranteed by the data sheet at 25°C, Dropout Voltage vs Temperature (Figure 3) clearly shows that the dropout voltage is nearly constant over a wide temperature range.

Dropout Voltage

		DROPOUT VOLTAGE	
DRIVE CURRENT	OUTPUT CURRENT	TYP	MAX
20mA	1A	0.16V	0.3V
50mA	1A	0.13V	0.25V
	2A	0.25V	0.4V
120mA	1A	0.2V	0.35V
	4A	0.45V	0.75V

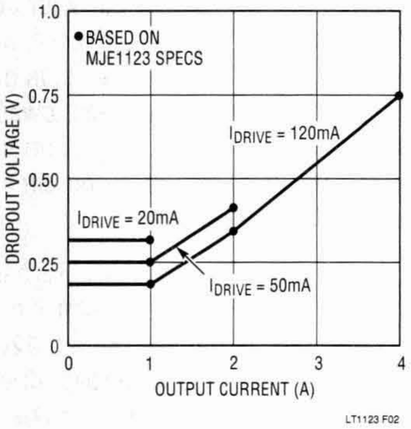


Figure 2. Maximum Dropout Voltage

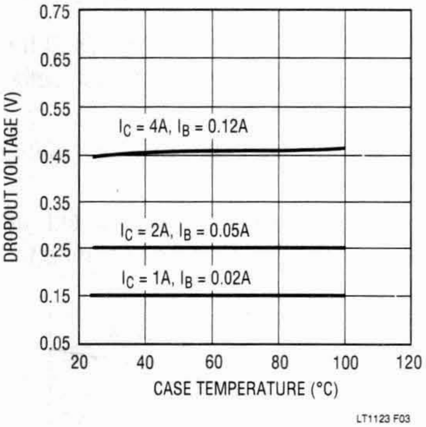


Figure 3. Dropout Voltage vs Temperature

APPLICATIONS INFORMATION

SELECTING R_D

In order to select R_D the user should first choose the value of drive current that will give the required value of output current. For circuits using the MJE1123 as a pass transistor this can be done using the graph of Dropout Voltage vs Output Current (Figure 2). For example, 20mA of drive current will guarantee a dropout voltage of 0.3V at 1A of output current. For circuits using transistors other than the MJE1123 the user must characterize the transistor to determine the drive current requirements. In general it is recommended that the user choose the lowest value of drive current that will satisfy the output current requirements. This will minimize the stress on circuit components during overload conditions.

Figure 4 can be used to select the value of R_D based on the required drive current and the minimum input voltage. Curves are shown for 20mA, 50mA, and 120mA drive current corresponding to the specified base drive currents for the MJE1123. The data for the curves was generated using the following formula:

$$R_D = (V_{IN} - V_{BE} - V_{DRIVE})/(I_{DRIVE} + 1mA)$$

where V_{IN} = the minimum input voltage to the circuit
V_{BE} = the maximum emitter/base voltage of the PNP pass transistor
V_{DRIVE} = the maximum Drive pin voltage of the LT1123
I_{DRIVE} = the minimum drive current required
The current through R_B is assumed to be 1mA

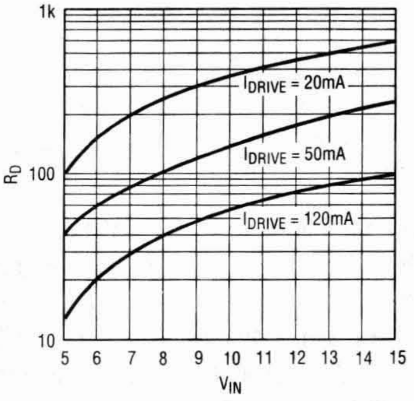


Figure 4. R_D Resistor Value

The following assumptions were made in calculating the data for the curves. Resistors are 5% tolerance and the values shown on the curve are nominal.

For 20mA drive current assume:
$V_{BE} = 0.95V$ at $I_C = 1A$
$V_{DRIVE} = 1.75V$

For 50mA drive current assume:
$V_{BE} = 1.2V$ at $I_C = 2A$
$V_{DRIVE} = 1.9V$

For 120mA drive current assume:
$V_{BE} = 1.4V$ at $I_C = 4A$
$V_{DRIVE} = 2.1V$

The R_D Selection Chart lists the recommended values for R_D for the most useful range of input voltage and output current. The chart includes a number for power dissipation for the LT1123 and R_D.

R_D Selection Chart

INPUT VOLTAGE	OUTPUT CURRENT: DROPOUT VOLTAGE:	0 – 1A 0.3V	0 – 2A 0.4V	0 – 4A 0.75V
5.5V	R_D	120Ω	43Ω	—
	Power (LT1123)	0.05W	0.14W	—
	Power (R_D)	0.12W	0.32W	—
6.0V	R_D	150Ω	51Ω	20Ω
	Power (LT1123)	0.05W	0.15W	0.37W
	Power (R_D)	0.13W	0.35W	0.76W
7.0V	R_D	180Ω	75Ω	27Ω
	Power (LT1123)	0.06W	0.14W	0.38W
	Power (R_D)	0.16W	0.36W	0.89W
8.0V	R_D	240Ω	91Ω	36Ω
	Power (LT1123)	0.06W	0.15W	0.38W
	Power (R_D)	0.17W	0.42W	0.97W
9.0V	R_D	270Ω	110Ω	43Ω
	Power (LT1123)	0.20W	0.16W	0.41W
	Power (R_D)	0.07W	0.47W	1.11W
10.0V	R_D	330Ω	130Ω	51Ω
	Power (LT1123)	0.22W	0.17W	0.43W
	Power (R_D)	0.07W	0.52W	1.25W

Note that in some conditions R_D may be replaced with a short. This is possible in circuits where an overload is unlikely and the input voltage and drive requirements are low. See the section on Thermal Considerations for more information.

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CURRENT LIMIT

For regulator circuits using the LT1123, current limiting is achieved by limiting the base drive to the external PNP pass transistor. This means that the actual system current limit will be a function of both the current limit of the LT1123 and the Beta of the external PNP. Beta-based current limit schemes are normally not practical because of uncertainties in the Beta of the pass transistor. Here the drive characteristics of the LT1123 combined with the Beta characteristics of the MJE1123 can provide reliable Beta-based current limiting. This is shown in Figure 5 where the current limit of 30 randomly selected transistors is plotted. The spread of current limit is reasonably well controlled.

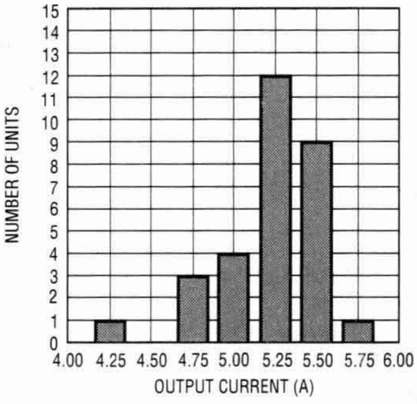


Figure 5. Short Circuit Current for 30 Random Devices

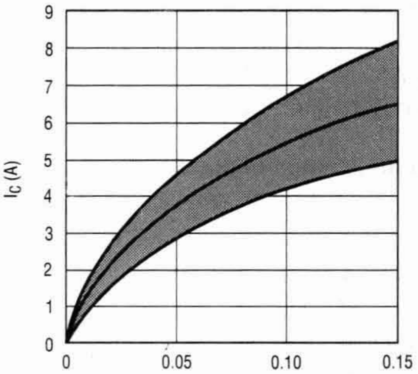


Figure 6. MJE1123 I_C vs I_B

The curve in Figure 6 can be used to determine the range of current limit of an LT1123 regulator circuit using an MJE1123 as a pass transistor. The curve was generated using the Beta versus I_C curve of the MJE1123. The minimum and maximum value curves are extrapolated from the minimum and maximum Beta specifications.

THERMAL CONSIDERATIONS

The thermal characteristics of three components need to be considered; the LT1123, the pass transistor, and R_D. Power dissipation should be calculated based on the worst case conditions seen by each component during normal operation.

The worst case power dissipation in the LT1123 is a function of drive current, supply voltage, and the value of R_D. Worst case dissipation for the LT1123 occurs when the drive current is equal to approximately one half of its maximum value. Figure 7 plots the worst case power dissipation in the LT1123 versus R_D and V_{IN}. The graph was generated using the following formula:

$$P_D = \frac{(V_{IN} - V_{BE})^2}{4R_D}; R_D > 10\Omega$$

where V_{BE} = the emitter/base voltage of the PNP pass transistor (assumed to be 0.6V)

For some operating conditions R_D may be replaced with a short. This is possible in applications where the operating

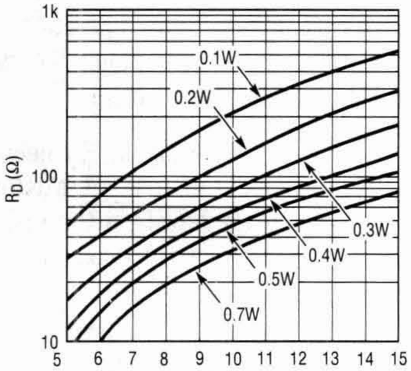


Figure 7. Power in LT1123

APPLICATIONS INFORMATION

requirements (input voltage and drive current) are at the low end and the output will not be shorted. For $R_D = 0$ the following formula may be used to calculate the maximum power dissipation in the LT1123.

$$P_D = (V_{IN} - V_{BE})(I_{DRIVE})$$

where V_{IN} = maximum input voltage
V_{BE} = emitter/base voltage of PNP
I_{DRIVE} = required maximum drive current

The maximum junction temperature rise above ambient for the LT1123 will be equal to the worst case power dissipation multiplied by the thermal resistance of the device. The thermal resistance of the device will depend upon how the device is mounted, and whether a heat sink is used. Measurements show that one of the most effective ways of heat sinking the TO-92 package is by utilizing the PC board traces attached to the leads of the package. The table below lists several methods of mounting and the measured value of thermal resistance for each method. All measurements were done in still air.

	THERMAL RESISTANCE
Package alone	220°C/W
Package soldered into PC board with plated through holes only	175°C/W
Package soldered into PC board with 1/4 sq. in. of copper trace per lead	145°C/W
Package soldered into PC board with plated through holes in board, no extra copper trace, and a clip-on type heat sink:	
Thermalloy type 2224B	160°C/W
Aavid type 5754	135°C/W

The maximum operating junction temperature of the LT1123 is 125°C. The maximum operating ambient temperature will be equal to 125°C minus the maximum junction temperature rise above ambient.

The worst case power dissipation in R_D needs to be calculated so that the power rating of the resistor can be determined. The worst case power in the resistor will occur when the drive current is at a maximum. Figure 8 plots the required power rating of R_D versus supply voltage and resistor value. Power dissipation can be calculated using the following formula:

$$P_{R_D} = \frac{(V_{IN} - V_{BE} - V_{DRIVE})^2}{R}$$

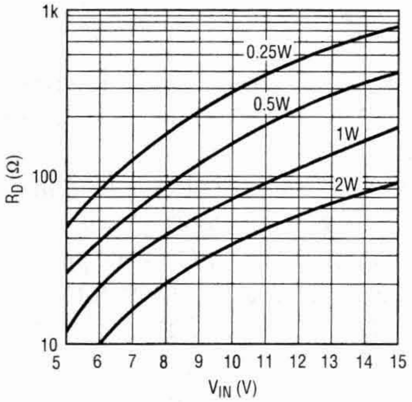


Figure 8. Power in R_D

where V_{BE} = emitter/base voltage of the PNP pass transistor
V_{DRIVE} = voltage at the drive pin of the LT1123
= V_{SAT} of the drive pin in the worst case

The worst case power dissipation in the PNP pass transistor is simply equal to:

$$P_{MAX} = (V_{IN} - V_{OUT})(I_{OUT})$$

where V_{IN} = Maximum V_{IN}
I_{OUT} = Maximum I_{OUT}

The thermal resistance of the MJE1123 is equal to:
70°C/W Junction to Ambient (no heat sink)
1.67°C/W Junction to Case

The PNP will normally be attached to either a chassis or a heat sink so the actual thermal resistance from junction to ambient will be the sum of the PNP's junction to case thermal resistance and the thermal resistance of the heat sink or chassis. For non-standard heat sinks the user will need to determine the thermal resistance by experiment.

The maximum junction temperature rise above ambient for the PNP pass transistor will be equal to the maximum power dissipation times the thermal resistance, junction to ambient, of the PNP. The maximum operating junction temperature of the MJE1123 is 150°C. The maximum operating ambient temperature for the MJE1123 will be equal to 150°C minus the maximum junction temperature rise.

APPLICATIONS INFORMATION

THERMAL LIMITING

The thermal limit of the LT1123 can be used to protect both the LT1123 and the PNP pass transistor. This is accomplished by thermally coupling the LT1123 to the power transistor. There are clip type heat sinks available for the TO-92 package that will allow the LT1123 to be mounted to the same heat sink as the PNP pass transistor. One example is manufactured by IERC (part #RUR67B1CB). The LT1123 should be mounted as close as possible to the PNP. If the output of the regulator circuit can be shorted, heat sinking must be adequate to limit the rate of temperature rise of the power device to approximately 50°C/minute. This can be accomplished with a fairly small heat sink, on the order of 3 – 4 square inches of surface area.

DESIGN EXAMPLE

Given the following operating requirements:

$5.5V < V_{IN} < 7V$
$I_{OUT_{MAX}} = 1.5A$
Max ambient temp. = 70°C
$V_{OUT} = 5V$

1. The first step is to determine the required drive current. This can be found from the Maximum Dropout Voltage curve. 50mA of drive current will guarantee 0.4V dropout at an output current of 2A. This satisfies our requirements.

$I_{DRIVE} = 50mA$

2. The next step is to determine the value of R_D. Based on 50mA of drive current and a minimum input voltage of 5.5V, we can select R_D from the graph of Figure 4. From the graph the value of R_D is equal to 50Ω, so we should use the next lowest 5% value which is 47Ω.

$R_D = 47\Omega$

3. We can now look at the thermal requirements of the circuit.

Worst case power in the LT1123 will be equal to:

$$\frac{\left(V_{IN_{MAX}} - V_{BE}\right)^2}{4R_D}$$

Given: $V_{IN_{MAX}} = 7V$, $V_{BE} = 0.6V$, $R_D = 47\Omega$
Then: P_{MAX} (LT1123) = 0.22W.

Assuming a thermal resistance of 150°C/W, the maximum junction temperature rise above ambient will be equal to $(P_{MAX})(150°C/W) = 33°C$. The maximum operating junction temperature will be equal to the maximum ambient temperature plus the junction temperature rise above ambient. In this case we have (maximum ambient = 70°C) plus (junction temperature rise = 33°C) is equal to 103°C. This is well below the maximum operating junction temperature of 125°C for the LT1123.

The power rating for R_D can be found from the plot of Figure 8 using $V_{IN} = 7V$ and $R_D = 47\Omega$. From the plot, R_D should be sized to dissipate a minimum of 1/2W.

The worst case power dissipation, for normal operation, in the MJE1123 will be equal to:

$$(V_{IN_{MAX}} - V_{OUT})(I_{OUT_{MAX}}) = (7V - 5V)(1.5A) = 3W$$

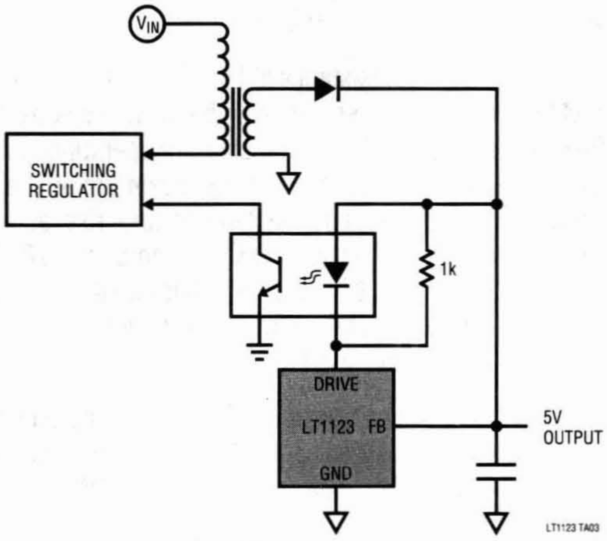
The maximum operating junction temperature of the MJE1123 is 150°C. The difference between the maximum operating junction temperature of 150°C and the maximum ambient temperature of 70°C is 80°C. The device must be mounted to a heat sink which is sized such that the thermal resistance from the junction of the MJE1123 to ambient is less than 80°C/3W = 26.7°C/W.

It is recommended that the LT1123 be thermally coupled to the MJE1123 so that the thermal limit circuit of the LT1123 can protect both devices. In this case the ambient temperature for the LT1123 will be equal to the temperature of the heat sink. The heat sink temperature, under normal operating conditions, will have to be limited such that the maximum operating junction temperature of the LT1123 is not exceeded.

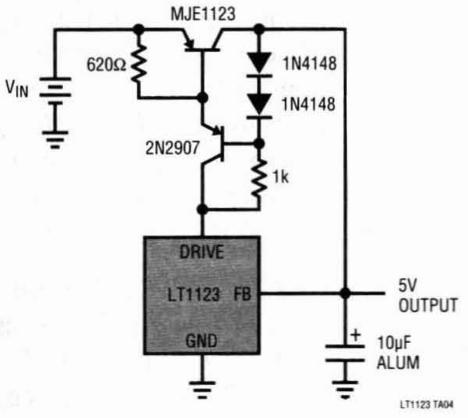
Refer to Linear Technology's list of Suggested Manufacturers of Specialized Components for information on where to find the required heat sinks, resistors and capacitors. This listing is available through Linear Technology's marketing department.

TYPICAL APPLICATIONS

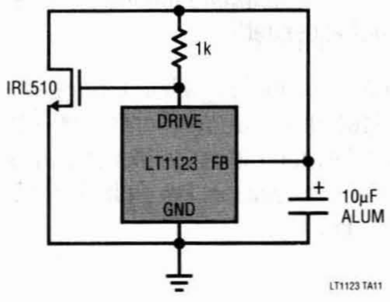
Isolated Feedback for Switching Regulators


VIN
SWITCHING REGULATOR
1k
DRIVE
LT1123 FB
GND
5V OUTPUT
LT1123 TA03

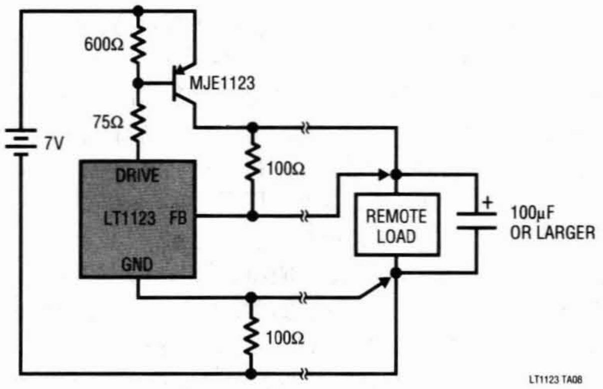
5V Regulator with Anti-Sat Miminizes Ground Pin Current in Dropout


MJE1123
VIN
620Ω
1N4148
1N4148
2N2907
1k
DRIVE
LT1123 FB
GND
5V OUTPUT
10µF ALUM
LT1123 TA04

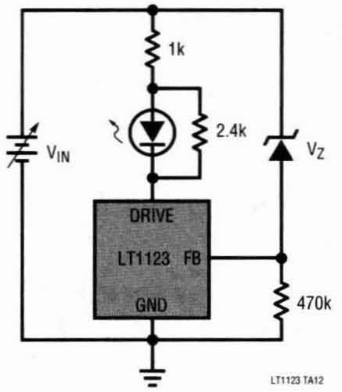
5V Shunt Regulator or Voltage Clamp


1k
IRL510
DRIVE
LT1123 FB
GND
10µF ALUM
LT1123 TA11

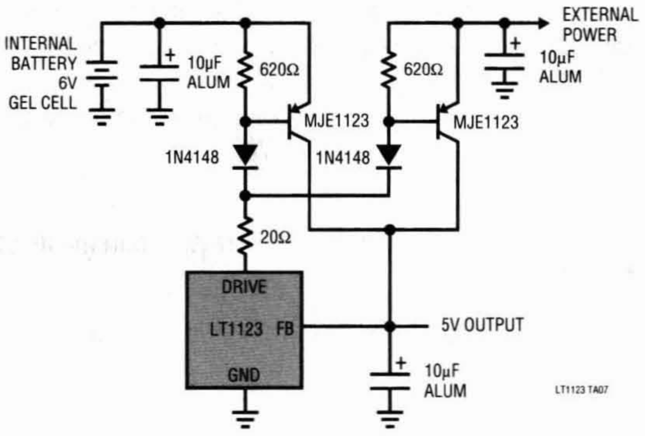
5V/2A Regulator with Remote Sensing


600Ω
MJE1123
75Ω
7V
100Ω
DRIVE
LT1123 FB
GND
REMOTE LOAD
100µF OR LARGER
100Ω
LT1123 TA08

Undervoltage Indicator On for V_{IN} < (V_Z +5V)

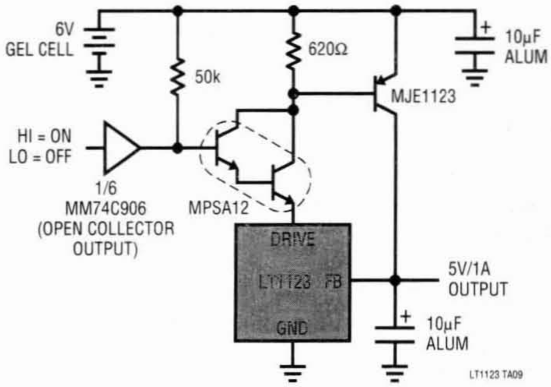

1k
2.4k
VIN
VZ
DRIVE
LT1123 FB
GND
470k
LT1123 TA12

Battery Backup Regulator

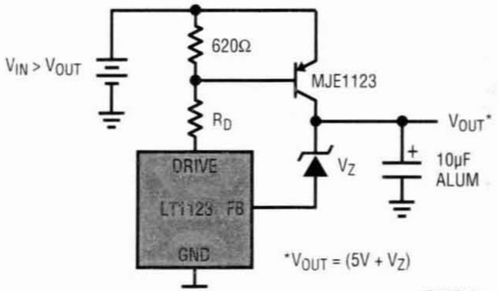

INTERNAL BATTERY 6V GEL CELL
10µF ALUM
620Ω
MJE1123
1N4148
EXTERNAL POWER
620Ω
10µF ALUM
MJE1123
1N4148
20Ω
DRIVE
LT1123 FB
GND
5V OUTPUT
10µF ALUM
LT1123 TA07

TYPICAL APPLICATIONS

5V/1A Regulator with Shutdown


6V
GEL CELL
50k
620Ω
10μF
ALUM
MJE1123
HI = ON
LO = OFF
1/6
MM74C906
(OPEN COLLECTOR
OUTPUT)
MPSA12
DRIVE
LT1123
FB
GND
5V/1A
OUTPUT
10μF
ALUM
LT1123 TA09

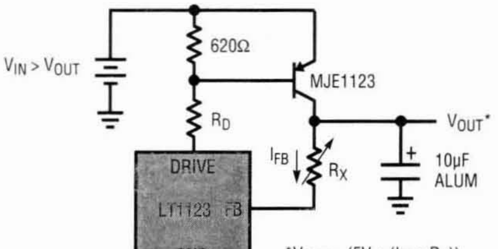
Adjusting V_{OUT}


$V_{IN} > V_{OUT}$
620Ω
MJE1123
R_D
V_{OUT}*
V_Z
10μF
ALUM
DRIVE
LT1123
FB
GND

*$V_{OUT} = (5V + V_Z)$

LT1123 TA13

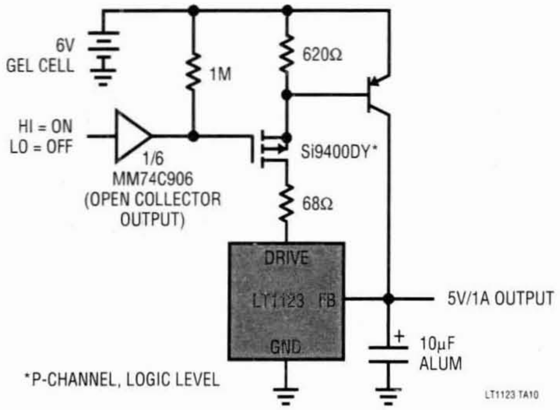
Adjusting V_{OUT}


$V_{IN} > V_{OUT}$
620Ω
MJE1123
R_D
V_{OUT}*
I_{FB}
R_X
10μF
ALUM
DRIVE
LT1123
FB
GND

*$V_{OUT} = (5V + (I_{FB} \bullet R_X))$
$I_{FB} \approx 300\mu A$

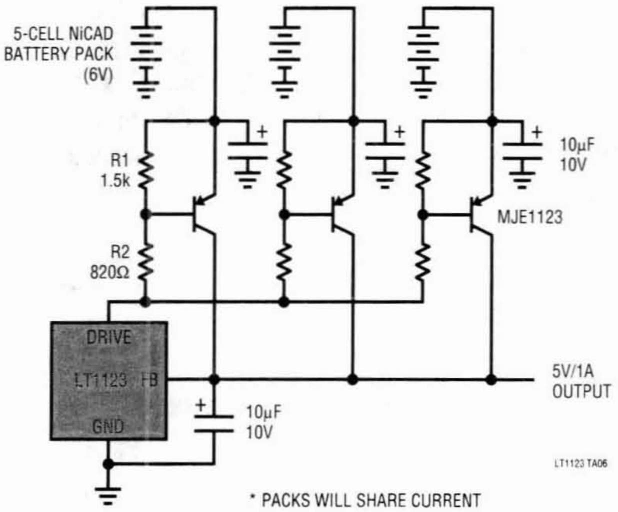
LT1123 TA14

5V/1A Regulator with Shutdown


6V
GEL CELL
1M
620Ω
HI = ON
LO = OFF
1/6
MM74C906
(OPEN COLLECTOR
OUTPUT)
Si9400DY*
68Ω
DRIVE
LT1123
FB
GND
5V/1A OUTPUT
10μF
ALUM
LT1123 TA10

*P-CHANNEL, LOGIC LEVEL

5V Regulator Powered by Multiple Battery Packs*


5-CELL NiCAD
BATTERY PACK
(6V)
R1
1.5k
R2
820Ω
10μF
10V
MJE1123
DRIVE
LT1123
FB
GND
5V/1A
OUTPUT
10μF
10V
LT1123 TA06

* PACKS WILL SHARE CURRENT

LT1185

Low Dropout Regulator

FEATURES

- Low Resistance Pass Transistor (0.25Ω)
- Dropout Voltage, 0.75V@3A
- ± 1% Reference Voltage
- **Accurate** Programmable Current Limit
- Shutdown Capability
- Internal Reference Available
- Standard 5-Lead Packages
- Full Remote Sense
- Low Quiescent Current, ≈2.5mA
- Good High Frequency Ripple Rejection

DESCRIPTION

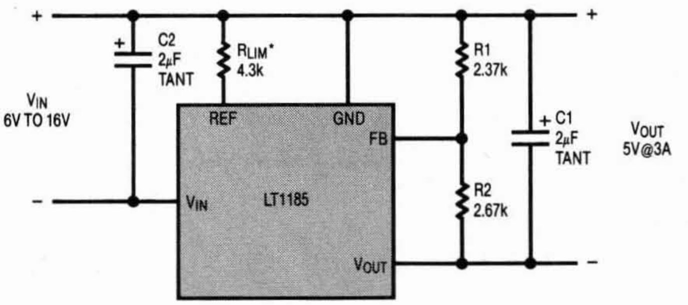
The LT1185 is a 3A low dropout regulator with adjustable current limit and remote sense capability. It can be used as a positive output regulator with floating input or as a standard negative regulator with grounded input. The output voltage range is 2.5V to 25V, with ± 1% accuracy on the internal reference voltage.

The LT1185 uses a saturation-limited NPN transistor as the pass element. This device gives the linear dropout characteristics of an FET pass element with significantly less die area. High efficiency is maintained by using special anti-saturation circuitry that adjusts base drive to track load current. The "on resistance" is typically 0.25Ω.

Accurate current limit is programmed with a single 1/8W external resistor, with a range of zero to three amperes. A second, fixed internal limit circuit prevents destructive currents if the programming current is accidentally overranged. Shutdown of the regulator output is guaranteed when the program current is less than 1μA, allowing external logic control of output voltage.

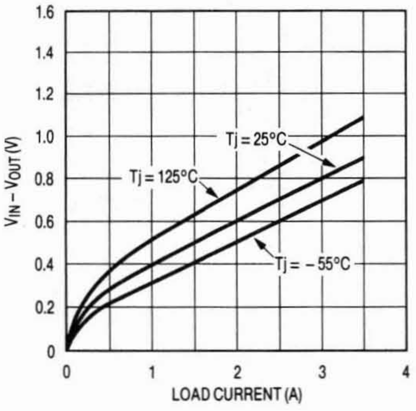
The LT1185 has all the protection features of previous LTC regulators, including power limiting and thermal shutdown. The 5-lead TO-3 package is specified for – 55°C to 150°C operation and the 5-lead TO-220 is specified over 0°C to 125°C.

5V, 3A Regulator with 3.5A Current Limit



*CURRENT LIMIT = 15k/R_{LIM} = 3.5A

Dropout Voltage

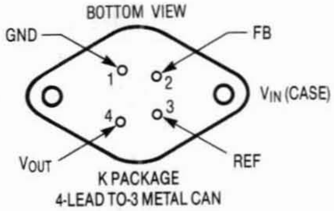
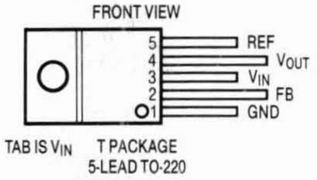


ABSOLUTE MAXIMUM RATINGS

Input Voltage 35V
Input-Output Differential 30V
FB Voltage 7V
REF Voltage 7V
Output Voltage 30V
Output Reverse Voltage 2V
Operating Ambient Temperature Range
  LT1185M .... −55°C to 125°C
  LT1185C .... 0°C to 70°C
Operating Junction Temperature Range*
Control Section
  LT1185M .... −55°C to 150°C
  LT1185C .... 0°C to 125°C
Power Transistor Section
  LT1185M .... −55°C to 175°C
  LT1185C .... 0°C to 150°C
Storage Temperature .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

*See Application Section for details on calculating operating junction temperature.

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 BOTTOM VIEW GND FB 1 2 3 4 V_{IN} (CASE) V_{OUT} REF K PACKAGE 4-LEAD TO-3 METAL CAN	LT1185MK
 FRONT VIEW 5 4 3 2 1 REF V_{OUT} V_{IN} FB GND TAB IS V_{IN} T PACKAGE 5-LEAD TO-220	LT1185CT

ELECTRICAL CHARACTERISTICS

Adjustable Version, V_{IN} = 7.4V, V_{OUT} = V_{REF}, I_{OUT} = 1mA, R_{LIM} = 4.02k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage (At FB Pin)				2.37		V
Reference Voltage Tolerance (Note 1)	$V_{IN} - V_{OUT} = 5V$			0.3	±1	%
	$1mA \le I_{OUT} \le 3A$ $V_{IN} - V_{OUT} = 1.2V$ to $V_{IN} = 30V$ $P \le 25W$ (Note 5) $T_{MIN} \le T_j = T_{MAX}$ (Note 8)	●		1.0	±2.5	%
Feedback Pin Bias Current		●		0.7	2	μA
Dropout Voltage (Note 2)	$I_{OUT} = 0.5A$ $I_{OUT} = 3A$			0.27 0.8	0.37 1.0	V V
Load Regulation (Note 6)	I_{OUT} = 5mA to 3A $V_{IN} - V_{OUT}$ = 1.5V to 10V			0.05	0.3	%
Line Regulation (Note 6)	$V_{IN} - V_{OUT}$ = 1V to 20V			0.002	0.01	%/V
Minimum Input Voltage	$I_{OUT} = 1A$ (Note 3) $I_{OUT} = 3A$			4 4.3		V V
Internal Current Limit (See Graph for Guaranteed Curve)	$1.5V \le V_{IN} - V_{OUT} \le 10V$		3.3	3.6	4.0	A
		●	3.1		4.2	A
	$V_{IN} - V_{OUT} = 15V$	●	2	3	4	A
	$V_{IN} - V_{OUT} = 20V$	●	1.2	1.7	2.6	A
	$V_{IN} - V_{OUT} = 30V$	●	0.2	0.4	1.0	A
External Current Limit Programming Constant	$5k \le R_{LIM} \le 15k$, $V_{OUT} = 1V$ (Note 10)	●		15k		A•Ω

ELECTRICAL CHARACTERISTICS

Adjustable Version, $V_{IN} = 7.4V$, $V_{OUT} = V_{REF}$, $I_{OUT} = 1mA$, $R_{LIM} = 4.02k$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
External Current Limit Error	$1A \le I_{LIM} \le 3A$			$0.02\ I_{LIM}$	$0.06\ I_{LIM} + 0.03$	A
	$R_{LIM} = 15k \bullet A/I_{LIM}$	●		$0.04\ I_{LIM}$	$0.09\ I_{LIM} + 0.05$	A
Quiescent Supply Current	$I_{OUT} = 5mV$ $4V \le V_{IN} \le 25V$ (Note 4)	●		2.5	3.5	mA
Supply Current Change with Load	$V_{IN} - V_{OUT} = V_{SAT}$ (Note 9)	●		25	40	mA/A
	$V_{IN} - V_{OUT} \ge 2V$	●		10	25	mA/A
REF Pin Shutoff Current		●	1	2	7	μA
Thermal Regulation (See Applications Information)	$V_{IN} - V_{OUT} = 10V$ $I_{OUT} = 5mA$ to $2A$			0.005	0.014	%/W
Reference Voltage Temperature Coefficient	(Note 7)			0.003	0.01	%/°C
Thermal Resistance Junction to Case	TO-3 Control Area				1	°C/W
	Power Transistor				3	°C/W
	TO-220 Control Area				1	°C/W
	Power Transistor				3	°C/W

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Reference voltage is guaranteed both at nominal conditions (no load, 25°C) and at worst case conditions of load, line, power, and temperature. An intermediate value can be calculated by adding the effects of these variables in the actual application. See the Applications Information section of this datasheet.

Note 2: Dropout voltage is tested by reducing input voltage until the output drops 1% below its nominal value. Tests are done at 0.5A and 3A. The power transistor looks basically like a pure resistance in this range so that minimum differential at any intermediate current can be calculated by interpolation; $V_{DROPOUT} = 0.25V + 0.25\Omega \bullet I_{OUT}$. For load current less than 0.5A, see graph.

Note 3: "Minimum input voltage" is limited by base emitter voltage drive of the power transistor section, not saturation as measured in Note 2. For output voltages below 4V, "minimum input voltage" specification may limit dropout voltage before the power transistor saturation limitation.

Note 4: Supply current is measured on the ground pin, and does not include load current, R_{LIM}, or output divider current.

Note 5: The 25W power level is guaranteed for an input-output voltage of 8.3V to 20V. At lower voltages the 3A limit applies, and at higher voltages the internal power limiting may restrict regulator power below 25W. See graphs.

Note 6: Line and load regulation are measured on a pulse basis with a pulse width of ≈2ms, to minimize heating. DC regulation will be affected by thermal regulation and temperature coefficient of the reference. See Application Section for details.

Note 7: Guaranteed by design and correlation to other tests, but not tested.

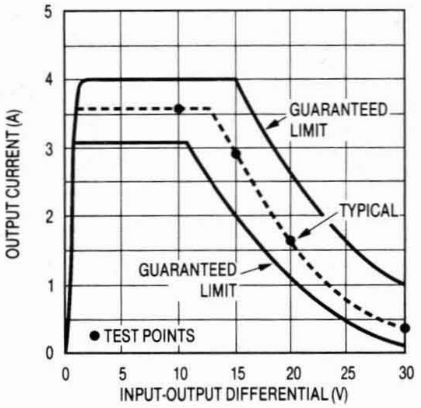
Note 8: $T_{jMIN} = -55°C$ for the LT1185M and 0°C for the LT1185C.
$T_{jMAX} = 150°C$ for the LT1185M and 125°C for the LT1185C.

Note 9: V_{SAT} is the maximum specified dropout voltage; $0.25V + (0.25)(I_{OUT})$.

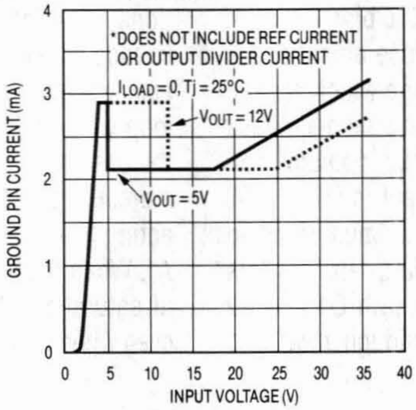
Note 10: Current limit is programmed with a resistor from REF pin to GND pin. The value is $15k\Omega/I_{LIM}$.

TYPICAL PERFORMANCE CHARACTERISTICS

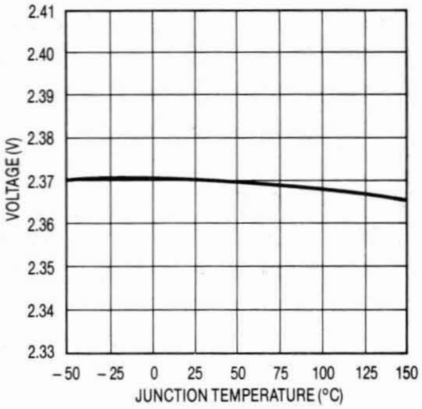
Internal Current Limit



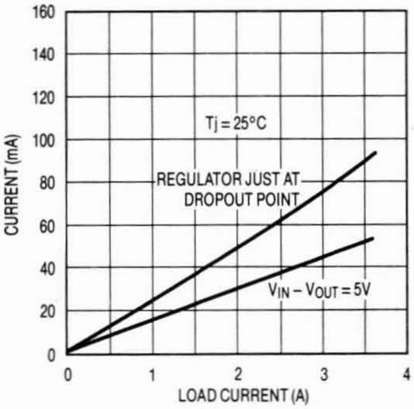
Quiescent Ground Pin Current*



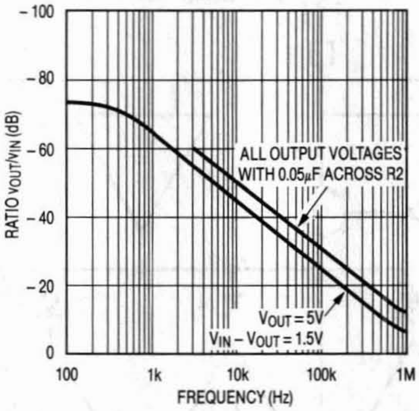
Feedback Pin Voltage Temperature Drift



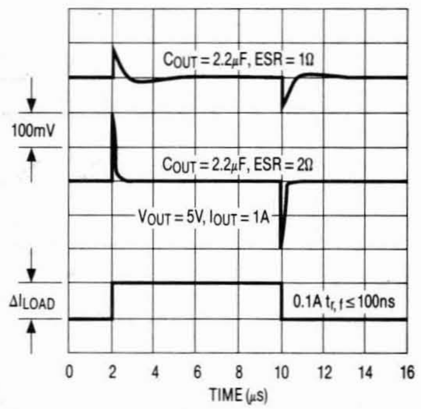
Ground Pin Current



Ripple Rejection vs Frequency

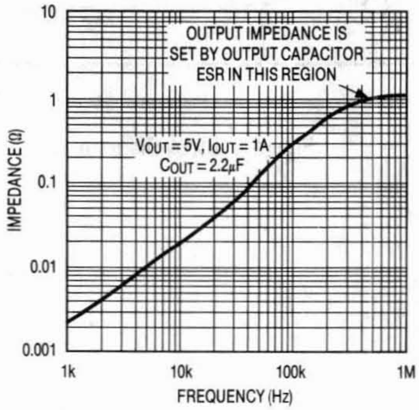


Load Transient Response



4

Output Impedance



APPLICATIONS INFORMATION

BLOCK DIAGRAM

A simplified block diagram of the LT1185 is shown in Figure 1. A 2.37V bandgap reference is used to bias the input of the error amplifier A1, and the reference amplifier A2. A1 feeds a triple NPN pass transistor stage which has the two driver collectors tied to ground so that the main pass transistor can completely saturate. This topology normally has a problem with unlimited current in Q1 and Q2 when the input voltage is less than the minimum required to create a regulated output. The standard "fix" for this problem is to insert a resistor in series with Q1 and Q2 collectors, but this resistor must be low enough in value to supply full base current for Q3 under worst case conditions, resulting in very high supply current when the input voltage is low. To avoid this situation, the LT1185 uses an auxiliary emitter on Q3 to create a drive limiting feedback loop which automatically adjusts the drive to Q1 so that the base drive to Q3 is just enough to saturate Q3, but no more. Under saturation conditions, the auxiliary emitter is acting like a collector to shunt away the output current of A1. When the input voltage is high enough to keep Q3 out of saturation, the auxiliary emitter current drops to zero even when Q3 is conducting full load current.

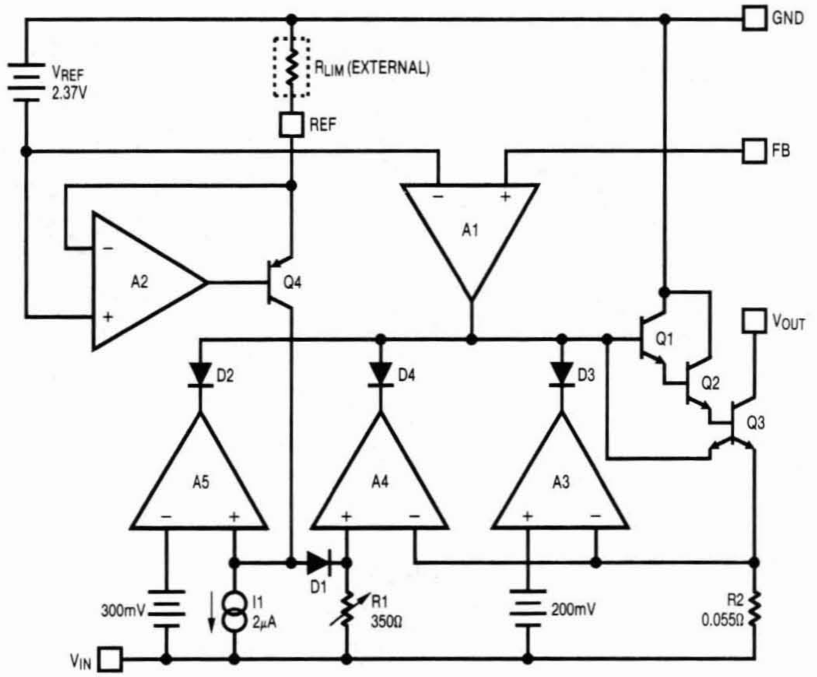


Figure 1. Block Diagram

TYPICAL APPLICATIONS

Amplifier A2 is used to generate an internal current through Q4 when an external resistor is connected from the REF pin to ground. This current is equal to 2.37V divided by R_{LIM}. It generates a current limit sense voltage across R1. The regulator will current limit via A4 when the voltage across R2 is equal to the voltage across R1. These two resistors essentially form a current "amplifier" with a gain of 350/0.055 = 6,360. Good temperature drift is inherent because R1 and R2 are made from the same diffusions. Their ratio, not absolute value, determines current limit. Initial accuracy is enhanced by trimming R1 slightly at wafer level. Current limit is equal to 15kΩ/R_{LIM}.

D1 and I1 are used to guarantee regulator shutdown when REF pin current drops below 2μA. A current less than 2μA through Q4 causes the + input of A5 to go low and shut down the regulator via D2.

A3 is an internal current limit amplifier which can override the external current limit. It provides "goof proof" protection for the pass transistor. Although not shown, A3 has a non-linear foldback characteristic at input-output voltages above 12V to guarantee safe area protection for Q3. See "Internal Current Limit" graph in the Typical Performance Characteristics of this datasheet.

SETTING OUTPUT VOLTAGE

The LT1185 output voltage is set by two external resistors (see Figure 2). Internal reference voltage is trimmed to 2.37V so that a standard 1% 2.37k resistor (R1) can be used to set divider current at 1mA. R2 is then selected from;

$$R2 = \frac{(V_{OUT} - 2.37)\,R1}{V_{REF}}$$

for $R1 = 2.37k$ and $V_{REF} = 2.37V$, this reduces to;

$$R2 = V_{OUT} - 2.37\ (k\Omega)$$

suggested values of 1% resistors are shown.

V_{OUT}	R2 WHEN R1 = 2.37k
5V	2.67k
5.2V	2.87k
6V	3.65k
12V	9.76k
15V	12.7k

OUTPUT CAPACITOR

The LT1185 has a collector output NPN pass transistor, which makes the open loop output impedance much higher than an emitter follower. Open loop gain is a direct function of load impedance, and causes a main loop "pole" to be created by the output capacitor, in addition to an internal pole in the error amplifier. To ensure loop stability, the output capacitor must have an ESR (effective series resistance) which has an upper limit of 2Ω, and a lower limit of 0.2 divided by the capacitance in μF. A 2μF output capacitor, for instance, should have a maximum ESR of 2Ω, and a minimum of 0.2/2 = 0.1Ω. These values are easily encompassed by standard solid tantalum capacitors, but occasionally a solid tantalum unit will have abnormally high ESR, especially at very low temperatures. The suggested 2μF value shown in the circuit applications should be increased to 4.7μF for −40°C and −55°C designs if the 2μF units cannot be guaranteed to stay below 2Ω at these temperatures.

Although solid tantalum capacitors are suggested, other types can be used if they meet the ESR requirements. Standard aluminum electrolytic capacitors need to be upward of 25μF in general to hold 2Ω maximum ESR, especially at low temperatures. Ceramic, plastic film, and monolithic capacitors have a problem with ESR being too *low*. These types should have a 1Ω carbon resistor in series to guarantee loop stability.

The output capacitor should be located close to the regulator (≤3″) to avoid excessive impedance due to lead inductance. 6″ lead length (2×3″) will generate an extra 0.8Ω inductive reactance at 1MHz, and unity gain frequency can be up to that value.

For remote sense applications, the capacitor should still be located close to the regulator. Additional capacitance can be added at the remote sense point, but the remote capacitor must be at least 2μF solid tantalum. It cannot be a low ESR type like ceramic or mylar unless a 0.5Ω–1Ω carbon resistor is added in series with the capacitor. Logic boards with multiple low ESR bypass capacitors should have a solid tantalum unit added in parallel whose value is approximately five times the combined value of low ESR capacitors.

APPLICATIONS INFORMATION

Large output capacitors (electrolytic or solid tantalum) will not cause the LT1185 to oscillate, but they will cause a damped "ringing" at light load currents where the ESR of the capacitor is several orders of magnitude lower than the load resistance. This ringing only occurs as a result of transient load or line conditions and normally causes no problems because of its low amplitude ($\leq 25mV$).

HEAT SINKING

The LT1185 will normally be used with a heatsink. The size of the heatsink is determined by load current, input and output voltage, ambient temperature, and the thermal resistance of the regulator, junction-to-case (θ_{jC}). The LT1185 has two separate values for θ_{jC}; one for the power transistor section, and a second, lower value for the control section. The reason for two values is that the power transistor is capable of operating at higher continuous temperatures than the control circuitry. At low power levels, the two areas are at nearly the same temperature, and maximum temperature is limited by the control area. At high power levels, the power transistor will be at a significantly higher temperature than the control area and its maximum operating temperature will be the limiting factor.

To calculate heatsink requirements, you must solve a thermal resistance formula twice, one for the power transistor and one for the control area. The *lowest* value obtained for heatsink thermal resistance must be used. In these equations, two values for maximum junction temperature and junction-to-case thermal resistance are used, as given in the Electrical Specifications.

$$\theta_{HS} = \frac{T_{jMAX} - T_{AMAX}}{P} - \theta_{jC} - \theta_{CHS}$$

θ_{HS} = Maximum heatsink thermal resistance.
θ_{jC} = LT1185 junction-to-case thermal resistance.
θ_{CHS} = Case to heatsink (interface) thermal resistance, including any insulating washers.
T_{jMAX} = LT1185 maximum operating junction temperature.
T_{AMAX} = Maximum ambient temperature in customers application.
P = Device dissipation
$= (V_{IN} - V_{OUT})(I_{OUT}) + \frac{I_{OUT}}{40}(V_{IN})$.

Example — A commercial version of the LT1185 in the TO-220 package is to be used with a maximum ambient temperature of 60°C. Output voltage is 5V at 2A. Input voltage can vary from 6V to 10V. Assume an interface resistance of 1°C/W.

First solve for control area, where the maximum junction temperature is 125°C for the TO-220 package, and $\theta_{jC} = 1°C/W$

$$P = (10V - 5V)(2A) + \frac{2A}{40}(10V) = 10.5W$$

$$\theta_{HS} = \frac{125°C - 60°C}{10.5W} - 1°C/W - 1°C/W = 4.2°C/W$$

Next, solve for power transistor limitation, with T_{jMAX} = 150°C, $\theta_{jC} = 3°C/W$

$$\theta_{HS} = \frac{150 - 60}{10.5} - 3 - 1 = 4.6°C/W$$

The lowest number must be used, so heatsink resistance must be less than 4.2°C/W.

Some heatsink datasheets show graphs of heatsink temperature rise vs power dissipation instead of listing a value for thermal resistance. The formula for θ_{HS} can be rearranged to solve for maximum heatsink temperature rise;

$$\Delta T_{HS} = T_{jMAX} - T_{AMAX} - P(\theta_{jC} + \theta_{CHS})$$

Using numbers from the previous example;

$$\Delta T_{HS} = 125°C - 60 - 10.5(1 + 1) = 44°C \text{ control section}$$
$$\Delta T_{HS} = 150°C - 60 - 10.5(3 + 1) = 48°C \text{ power transistor}$$

The smallest rise must be used, so heatsink temperature rise must be less than 44°C at a power level of 10.5W.

For board level applications, where heatsink size may be critical, one is often tempted to use a heatsink which barely meets the requirements. This is permissible *if* correct assumptions were made concerning maximum ambient temperature and power levels. One complicating factor is that local ambient temperature may be somewhat

APPLICATIONS INFORMATION

higher because of the point source of heat. The consequences of excess junction temperature include poor reliability, especially for plastic packages, and the possibility of thermal shutdown or degraded electrical characteristics. The final design should be checked *in situ* with a thermocouple attached to the regulator case under worst case conditions of high ambient, high input voltage, and full load.

What About Overloads?

IC regulators with thermal shutdown, like the LT1185, allow heatsink designs which concentrate on worst case "normal" conditions and ignore "fault" conditions. An output overload or short may force the regulator to exceed its maximum junction temperature rating, but thermal shutdown is designed to prevent regulator failure under these conditions. A word of caution however; thermal shutdown temperatures are typically 175°C in the control portion of the die and 180°C-225°C in the power transistor section. Extended operation at these temperatures can cause permanent degradation of plastic encapsulation. Designs which may be subjected to extended periods of overload should either use the hermetic TO-3 package or increase heatsink size. Foldback current limiting can be implemented to minimize power levels under fault conditions.

EXTERNAL CURRENT LIMIT

The LT1185 requires a resistor to set current limit. The value of this resistor is 15kΩ divided by the desired current limit (in amps). The resistor for 2A current limit would be $15k\Omega/2A = 7.5k\Omega$. Tolerance over temperature is ±10%, so current limit is normally set 15% above maximum load current. Foldback limiting can be employed if short circuit currents must be lower than full load current. (See Typical Applications.)

The LT1185 has internal current limiting which will override external curent limit if power in the pass transistor is excessive. The internal limit is ≈3.6A with a foldback characteristic which is dependent on input-output voltage, not output voltage *per se*. (See Typical Performance Characteristics.)

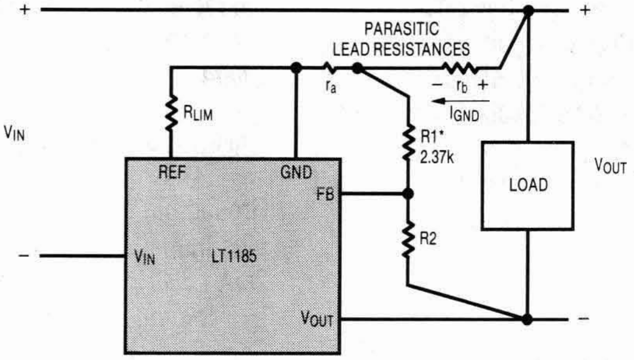
GROUND PIN CURRENT

Ground pin current for the LT1185 is approximately 2mA plus $I_{OUT}/40$. At $I_{OUT} = 3A$, ground pin current is typically $2mA + 3/40 = 77mA$. Worst case guarantees on the ratio of I_{OUT} to ground pin current are contained in the Electrical Specifications.

Ground pin current can be important for two reasons. It adds to power dissipation in the regulator and it can affect load/line regulation if a long line is run from the ground pin to load ground. The additional power dissipation is found by multiplying ground pin current by input voltage. In a typical example, with $V_{IN} = 8V$, $V_{OUT} = 5V$, and $I_{OUT} = 2A$, the LT1185 will dissipate $(8V-5V)(2A) = 6W$ in the pass transistor and $(2A/40)(8V) = 0.4W$ in the internal drive circuitry. This is only a 1.5% efficiency loss, and a 6.7% increase in regulator power dissipation, but these values will increase at higher output voltages.

Ground pin current can affect regulation as shown in Figure 2. Parasitic resistance in the ground pin lead will create a voltage drop which *increases* output voltage as load current is increased. Similarly, output voltage can *decrease* as input voltage increases because the "$I_{OUT}/40$" component of ground pin current drops significantly at higher input-output differentials. These effects are small enough to be ignored for local regulation applications, but for remote sense applications, they may need to be considered. 0.4Ω in the ground lead could cause an output voltage error of up to $(3A/40)(0.4\Omega) = 30mV$, or 0.6% at $V_{OUT} = 5V$. Note that if the sense leads are connected as shown in Figure 2, with $r_a \approx 0\Omega$, this error is a fixed number of millivolts, and does not increase as a function of DC output voltage.

APPLICATIONS INFORMATION



*R1 SHOULD BE CONNECTED DIRECTLY TO GROUND LEAD, NOT TO THE LOAD, SO THAT $r_a \approx 0\Omega$. THIS LIMITS THE OUTPUT VOLTAGE ERROR TO (I_{GND}) (r_b). ERRORS CREATED BY r_a ARE MULTIPLIED BY (1 + R2/R1). NOTE THAT V_{OUT} *INCREASES* WITH INCREASING GROUND PIN CURRENT. R2 SHOULD BE CONNECTED DIRECTLY TO LOAD FOR REMOTE SENSING.

Figure 2. Proper Connection of Positive Sense Lead

SHUTDOWN TECHNIQUES

The LT1185 can be shut down by open-circuiting the REF pin. The current flowing into this pin must be less than 1μA to guarantee shutdown. Figure 3 details several ways to create the "open" condition, with various logic levels. For variations on these schemes, simply remember that the voltage on the REF pin is 2.4V negative with respect to the ground pin.

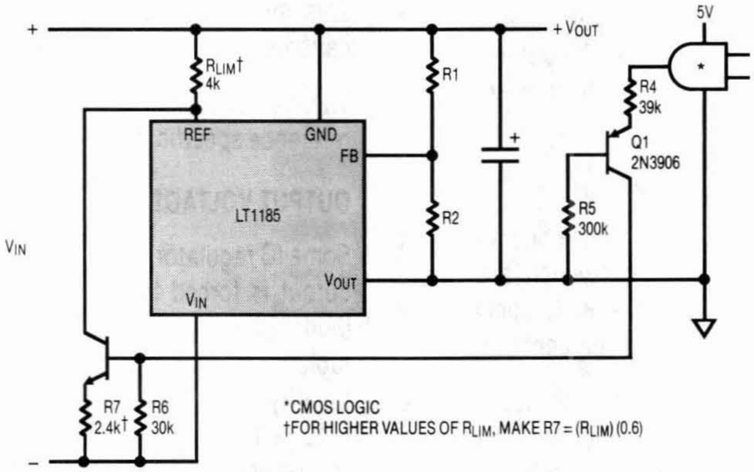
OUTPUT OVERSHOOT

Very high input voltage slew rate during startup may cause the LT1185 output to overshoot. Up to 20% overshoot could occur with input voltage ramp-up rate exceeding 1V/μs. This condition cannot occur with normal 50Hz to 400Hz rectified AC inputs because parasitic resistance and inductance will limit rate of rise even if the power switch is closed at the peak of the AC line voltage. This assumes that the switch is in the AC portion of the circuit. If instead, a switch is placed directly in the regulator input so that a large filter capacitor is precharged, fast input slew rates will occur on switch closure. The output of the regulator will slew at a rate set by current limit and output capacitor size; dVdt = I_{LIM}/C_{OUT}. 3.6A and 2.2μF allow the output to slew at 1.6V/μs and overshoot can occur. This overshoot can be reduced to a few hundred millivolts or less by increasing the output capacitor to 10μF and/or reducing current limit so that output slew rate is held below 0.5V/μs.

A second possibility for creating output overshoot is recovery from an output short. Again, the output slews at a rate set by current limit and output capacitance. To avoid overshoot, the ratio I_{LIM}/C_{OUT} should be less than 0.5×10^6. Remember that load capacitance can be added to C_{OUT} for this calculation. Many loads will have multiple supply bypass capacitors that total more than C_{OUT}.

APPLICATIONS INFORMATION

+5V Logic, Positive Regulated Output


+
−
V_{IN}
R_{LIM}†
4k
REF
GND
FB
LT1185
V_{OUT}
V_{IN}
R1
R2
+
+V_{OUT}
5V
*
R4
39k
Q1
2N3906
R5
300k
R7
2.4k†
R6
30k

*CMOS LOGIC
†FOR HIGHER VALUES OF R_{LIM}, MAKE R7 = (R_{LIM}) (0.6)

+5V Logic, Negative Regulated Output

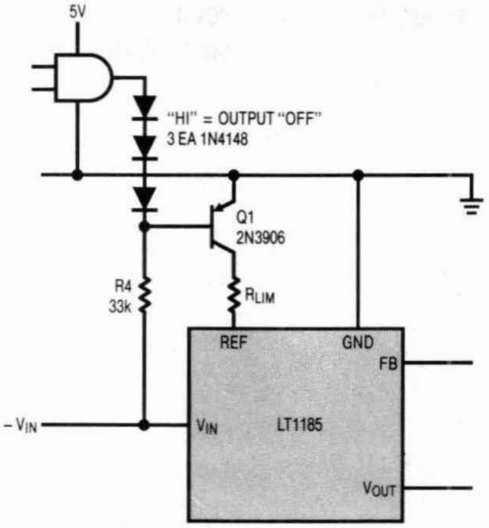

5V
"HI" = OUTPUT "OFF"
3 EA 1N4148
Q1
2N3906
R4
33k
R_{LIM}
REF
GND
FB
$-V_{IN}$
V_{IN}
LT1185
V_{OUT}

Figure 3. Shutdown Techniques

APPLICATIONS INFORMATION

THERMAL REGULATION

IC regulators have a regulation term not found in discrete designs because the power transistor is thermally coupled to the reference. This creates a shift in the output voltage which is proportional to power dissipation in the regulator.

$$\Delta V_{OUT} = P\,(K1 + K2\,\theta_{jA})$$
$$= (I_{OUT})\,(V_{IN} - V_{OUT})\,(K1 + K2\,\theta_{jA})$$

K1 and K2 are constants. K1 is a fast time constant effect caused by die temperature *gradients* which are established within 50ms of a power change. K1 is specified on the datasheet as thermal regulation, in percent per watt.

K2 is a long time constant term caused by the temperature drift of the regulator reference voltage. It is also specified, but in percent per degree centigrade. It must be multiplied by overall thermal resistance, junction-to-ambient, θ_{jA}.

As an example, assume a 5V regulator with an input voltage of 8V, load current of 2A, and a total thermal resistance of 4°C/W, including junction-to-case, (use control area specification), interface, and heatsink resistance. K1 and K2, respectively, from the datasheet are 0.014%/W and 0.01%/°C.

$$\Delta V_{OUT} = (2A)\,(8V - 5V)\,(0.014 + 0.01 \bullet 4)$$
$$= 0.32\%$$

This shift in output voltage could be in either direction because K1 and K2 can be either positive or negative.

Thermal regulation is already included in the worst case reference specification.

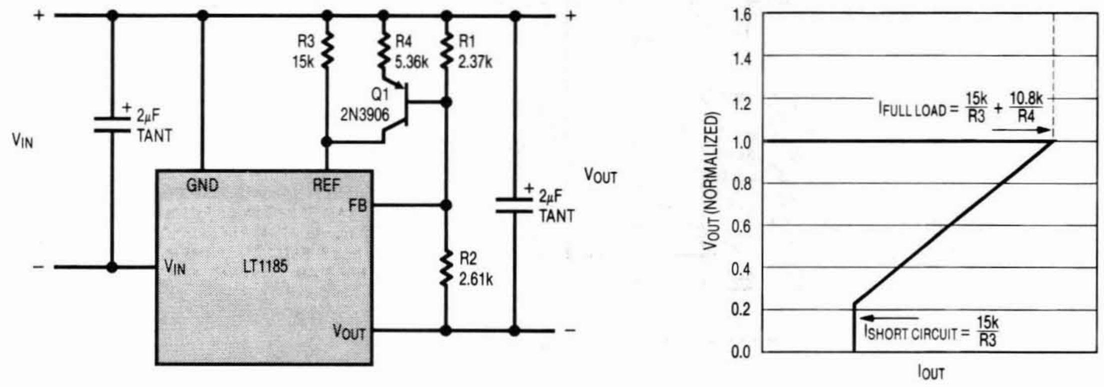
OUTPUT VOLTAGE REVERSAL

Some IC regulators suffer from a latch-up state when their output is forced to a reverse voltage of as little as one diode drop. The latch-up state can be triggered without a fault condition when the load is connected to an opposite polarity supply instead of to ground. If the second supply is turned-on first, it will pull the output of the first supply to a reverse voltage through the load. The first supply may then latch-off when turned on. This problem is particularly annoying because the diode clamps which should always be used to protect against polarity reversal do not usually stop the latch-up problem.

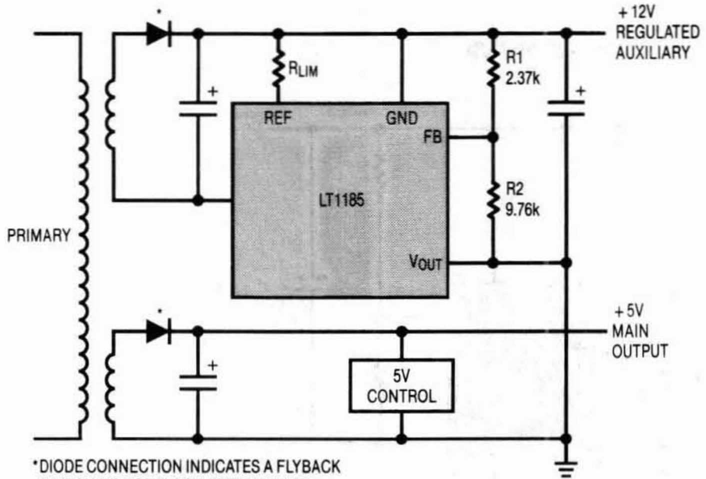
The LT1185 is designed to allow output reverse polarity of several volts without damage or latch-up, so that a simple diode clamp can be used.

TYPICAL APPLICATIONS

Foldback Current Limiting


+
VIN
−
2μF TANT
GND
REF
FB
VIN
LT1185
VOUT
R3 15k
R4 5.36k
R1 2.37k
Q1 2N3906
R2 2.61k
2μF TANT
+
VOUT
−
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
VOUT (NORMALIZED)
$I_{FULL\ LOAD} = \frac{15k}{R3} + \frac{10.8k}{R4}$
$I_{SHORT\ CIRCUIT} = \frac{15k}{R3}$
IOUT

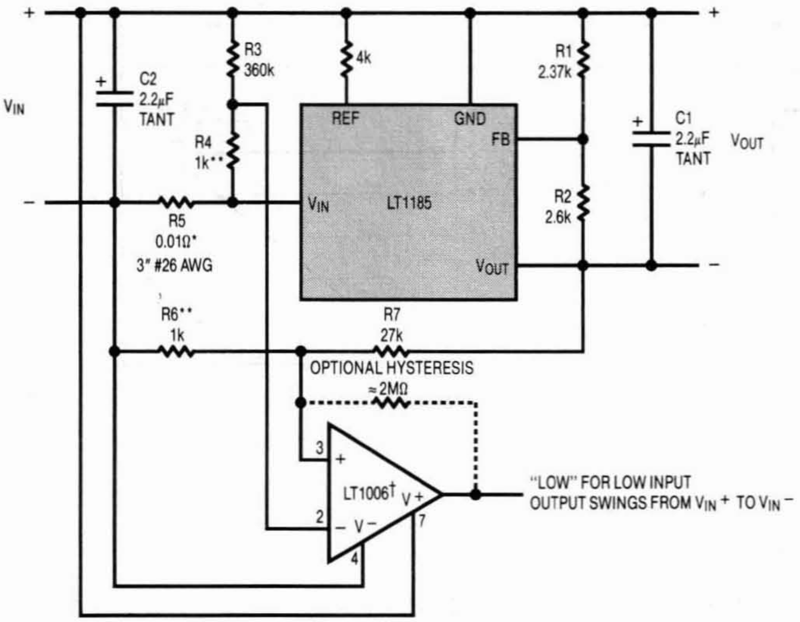
Auxiliary +12V Low Dropout Regulator for Switching Supply


*
RLIM
REF
GND
FB
LT1185
VOUT
R1 2.37k
R2 9.76k
+12V REGULATED AUXILIARY
PRIMARY
*
5V CONTROL
+5V MAIN OUTPUT

*DIODE CONNECTION INDICATES A FLYBACK SWITCHING TOPOLOGY, BUT FORWARD CONVERTORS MAY ALSO BE USED.

TYPICAL APPLICATIONS

Low Input Voltage Monitor Tracks Dropout Characteristic


+
+
VIN
C2
2.2µF
TANT
R3
360k
R4
1k**
4k
REF
GND
FB
VIN
LT1185
VOUT
R1
2.37k
R2
2.6k
C1
2.2µF
TANT
VOUT
R5
0.01Ω*
3" #26 AWG
R6**
1k
R7
27k
OPTIONAL HYSTERESIS
≈2MΩ
3
2
4
7
LT1006†
V+
V−
"LOW" FOR LOW INPUT
OUTPUT SWINGS FROM VIN+ TO VIN−

*3" #26 WIRE

**R4 DETERMINES TRIP POINT AT $I_{OUT} = 0$. R6 DETERMINES INCREASE OF TRIP POINT AS I_{OUT} INCREASES.

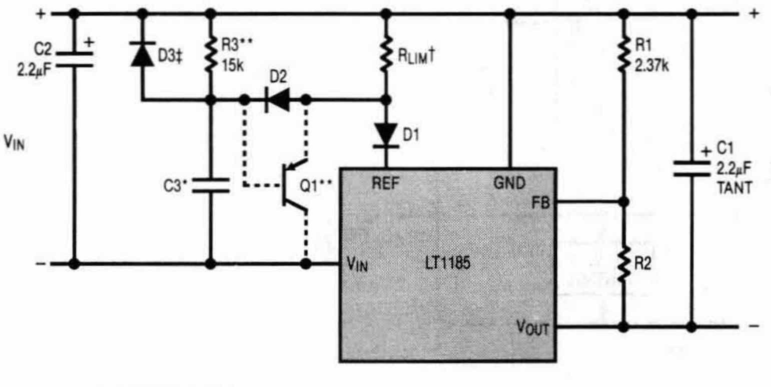
$$\text{TRIP POINT FOR } V_{IN} = V_{OUT}\left(1 + \frac{R4 \bullet R7}{R3 \bullet R6}\right) + I_{OUT}\frac{R5 \bullet R7}{R6}$$

FOR VALUES SHOWN, TRIP POINT FOR V_{IN} IS

$V_{OUT} + 0.37V$ AT $I_{OUT} = 0$, AND $V_{OUT} + 1.18V$ AT $I_{OUT} = 3A$

†DO NOT SUBSTITUTE. OP AMP MUST HAVE COMMON MODE RANGE EQUAL TO NEGATIVE SUPPLY.

Time Delayed Startup


+
+
C2
2.2µF
VIN
D3‡
R3**
15k
D2
RLIM†
D1
C3*
Q1**
REF
GND
FB
VIN
LT1185
VOUT
R1
2.37k
R2
C1
2.2µF
TANT
VOUT

ALL DIODES 1N4148

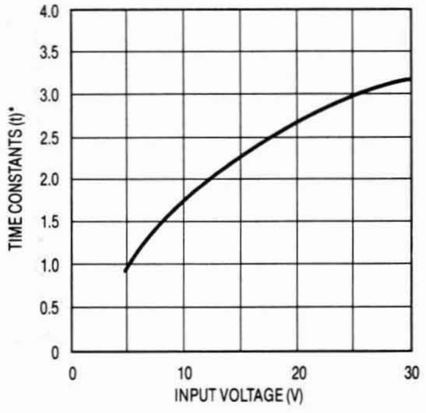
*SEE CHART FOR DELAY TIME VERSUS (C3) ($R3//R_{LIM}$) PRODUCT.

**FOR LONG DELAY TIMES, REPLACE D2 WITH 2N3906 TRANSISTOR AND USE R3 ONLY FOR CALCULATING DELAY TIME. R3 CAN INCREASE TO 100kΩ.

†I_{LIM} IS ≈ 11kΩ/R_{LIM}, INSTEAD OF 15kΩ, BECAUSE OF VOLTAGE DROP IN D1. TEMPERATURE COEFFICIENT OF I_{LIM} WILL BE ≈ +0.11%/°C, SO ADEQUATE MARGIN MUST BE ALLOWED FOR COLD OPERATION.

‡D3 PROVIDES FAST RESET OF TIMING. INPUT MUST DROP TO A LOW VALUE TO RESET TIMING.

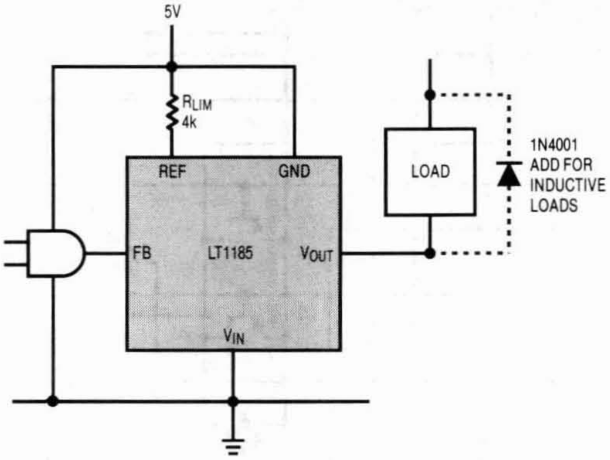
Delay Time



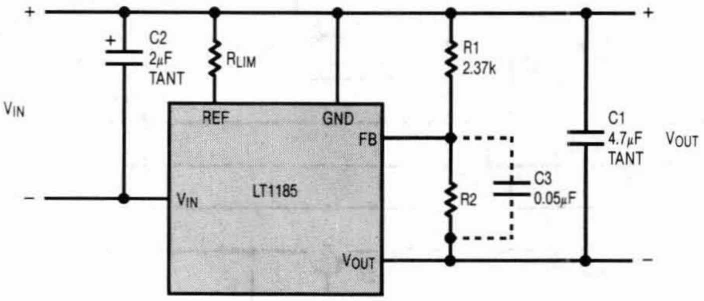
$$*t = (R3 /\!/ R_{LIM})(C3) = \left(\frac{R3 \bullet R_{LIM}}{R3 + R_{LIM}}\right)(C3)$$

TYPICAL APPLICATIONS

Logic Controlled 3A Low Side Switch with Fault Protection

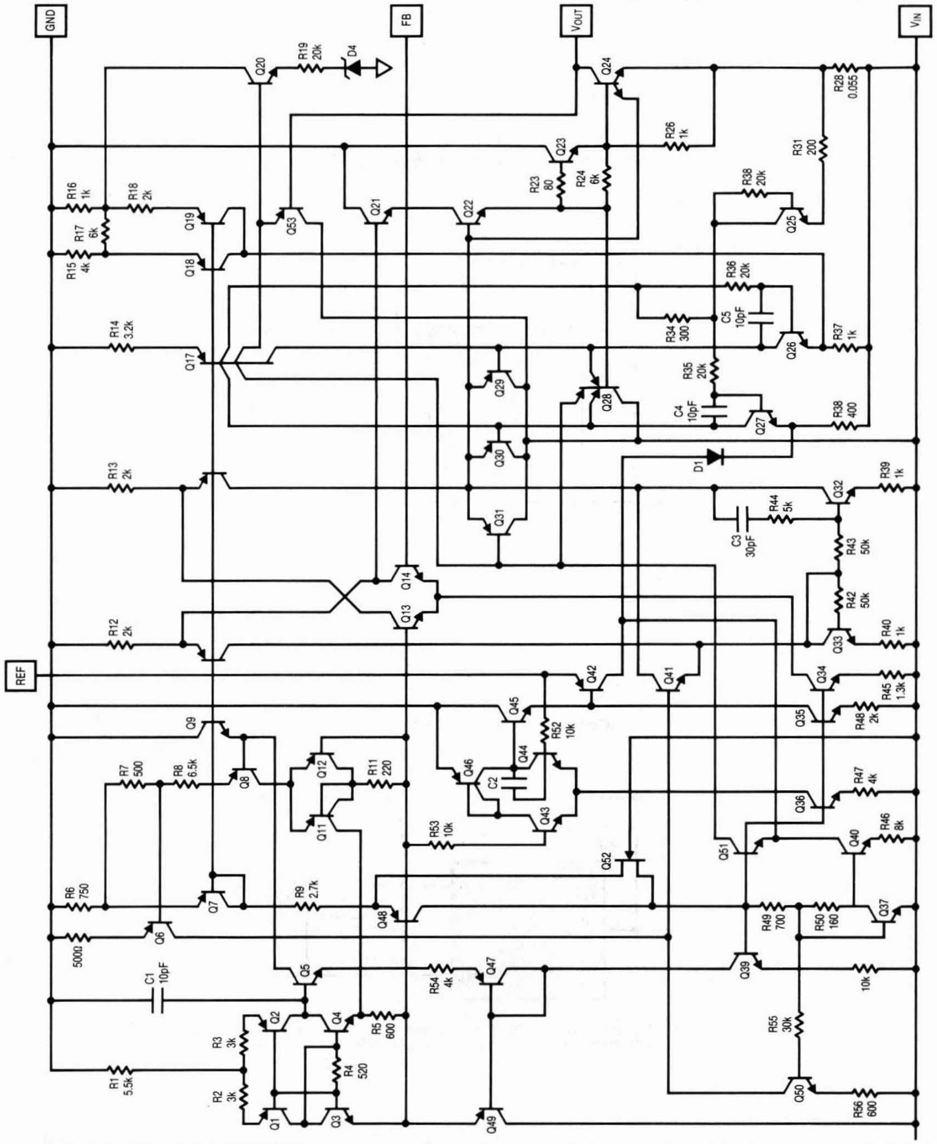

5V
RLIM
4k
REF
GND
FB
LT1185
VOUT
VIN
LOAD
1N4001
ADD FOR
INDUCTIVE
LOADS

Improved High Frequency Ripple Rejection


+
C2
2μF
TANT
RLIM
VIN
REF
GND
FB
LT1185
VIN
VOUT
–
R1
2.37k
R2
C3
0.05μF
C1
4.7μF
TANT
VOUT
+
–

C3 IMPROVES HIGH FREQUENCY RIPPLE REJECTION BY 6dB AT $V_{OUT} = 5V$, AND BY 14dB AT $V_{OUT} = 12V$. C1 IS INCREASED TO 4.7μF TO ENSURE GOOD LOOP STABILITY WHEN C3 IS USED.

SCHEMATIC DIAGRAM


GND
FB
VOUT
VIN
REF
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q11
Q12
Q13
Q14
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
Q39
Q40
Q41
Q42
Q43
Q44
Q45
Q46
Q47
Q48
Q49
Q50
Q51
Q52
Q53
R1 5.5k
R2 3k
R3 3k
R4 520
R5 600
500Ω
R6 750
R7 500
R8 6.5k
R9 2.7k
R11 220
R12 2k
R13 2k
R14 3.2k
R15 4k
R16 1k
R17 6k
R18 2k
R19 20k
R23 80
R24 6k
R26 1k
R28 0.055
R31 200
R34 300
R35 20k
R36 20k
R37 1k
R38 20k
R38 400
R39 1k
R40 1k
R42 50k
R43 50k
R44 5k
R45 1.3k
R46 8k
R47 4k
R48 2k
R49 700
R50 160
10k
R52 10k
R53 10k
R54 4k
R55 30k
R56 600
C1 10pF
C2
C3 30pF
C4 10pF
C5 10pF
D1
D4

SECTION 4—POWER PRODUCTS

POWER AND MOTOR CONTROL

LT1158, Half Bridge N-Channel Power MOSFET Driver 4-102
LT1241–45, High Speed Current Mode Pulse Width Modulators 4-122
LT1246, 1MHz Off-Line Current Mode PWM 4-134
LT1432, 5V High Efficiency Step-Down Switching Regulator Controller 4-145

LT1158

Half Bridge N-Channel Power MOSFET Driver

FEATURES

- Drives Gate of Top Side MOSFET Above V^+
- Operates at Supply Voltages from 5V to 30V
- 150ns Transition Times Driving 3000pF
- Adaptive Non-Overlap Gate Drives
- Continuous Current Limit Protection
- Auto Shutdown and Retry Capability
- Internal Charge Pump for DC Operation
- Built-In Gate Voltage Protection
- Compatible with Current-Sensing MOSFETs
- TTL/CMOS Input Levels
- Fault Output Indication

APPLICATIONS

- PWM of High Current Inductive Loads
- Half Bridge and Full Bridge Motor Control
- Synchronous Step-Down Switching Regulators
- Three-Phase Brushless Motor Drive
- High Current Transducer Drivers
- Battery Operated Logic-Level MOSFETs

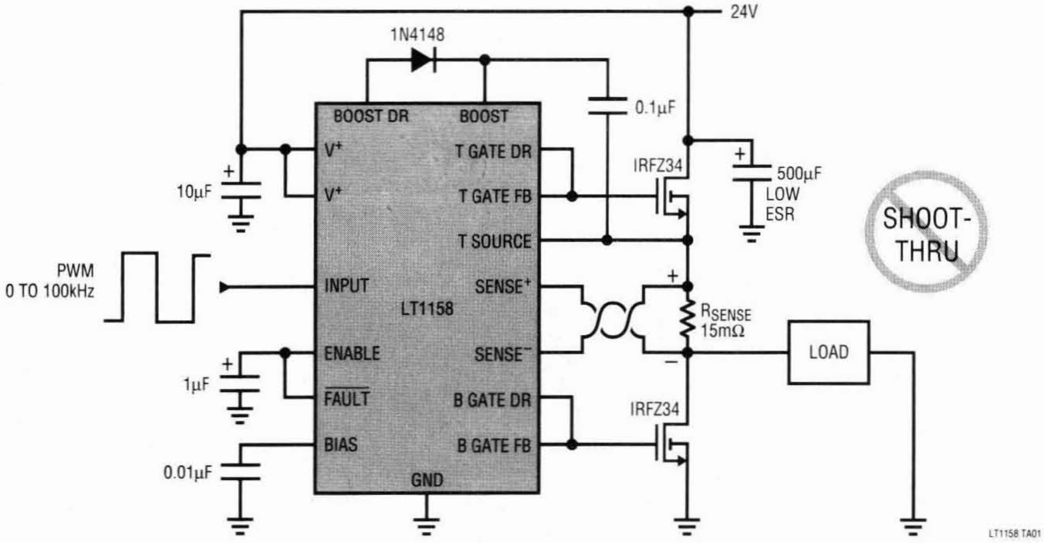
DESCRIPTION

A single input pin on the LT1158 synchronously controls two N-channel power MOSFETs in a totem pole configuration. Unique adaptive protection against shoot-through currents eliminates all matching requirements for the two MOSFETs. This greatly eases the design of high efficiency motor control and switching regulator systems.

A continuous current limit loop in the LT1158 regulates short-circuit current in the top power MOSFET. Higher start-up currents are allowed as long as the MOSFET V_{DS} does not exceed 1.2V. By returning the $\overline{\text{fault}}$ output to the enable input, the LT1158 will automatically shut down in the event of a fault and retry when an internal pullup current has recharged the enable capacitor.

An on-chip charge pump is switched in when needed to turn on the top N-channel MOSFET continuously. Special circuitry ensures that the top side gate drive is safely maintained in the transition between PWM and DC operation. The gate to source voltages are internally limited to 14.5V when operating at higher supply voltages.

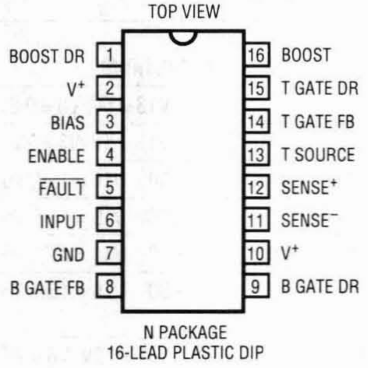
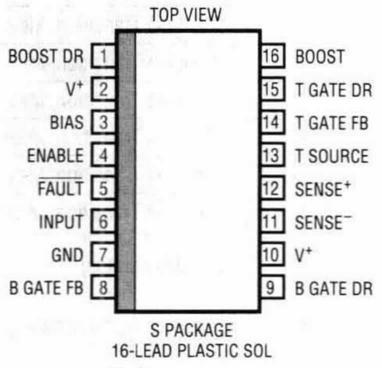
TYPICAL APPLICATION


24V
1N4148
BOOST DR
BOOST
0.1µF
V+
V+
T GATE DR
T GATE FB
T SOURCE
IRFZ34
500µF
LOW
ESR
10µF
SHOOT-
THRU
PWM
0 TO 100kHz
INPUT
LT1158
SENSE+
SENSE−
RSENSE
15mΩ
LOAD
ENABLE
FAULT
B GATE DR
B GATE FB
BIAS
GND
IRFZ34
1µF
0.01µF
LT1158 TA01

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pins 2, 10)	36V
Boost Voltage (Pin 16)	56V
Continuous Output Currents (Pins 1, 9, 15)	100mA
Sense Voltages (Pins 11, 12)	−5V to V^++5V
Top Source Voltage (Pin 13)	−5V to V^++5V
Boost to Source Voltage (V16 – V13)	−0.3V to 20V
Operating Temperature Range	
LT1158C	0°C to 70°C
LT1158I	−40°C to 85°C
Junction Temperature (Note 1)	
LT1158C	125°C
LT1158I	150°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW BOOST DR 1 V+ 2 BIAS 3 ENABLE 4 FAULT 5 INPUT 6 GND 7 B GATE FB 8 16 BOOST 15 T GATE DR 14 T GATE FB 13 T SOURCE 12 SENSE+ 11 SENSE− 10 V+ 9 B GATE DR N PACKAGE 16-LEAD PLASTIC DIP	LT1158IN LT1158CN
 TOP VIEW BOOST DR 1 V+ 2 BIAS 3 ENABLE 4 FAULT 5 INPUT 6 GND 7 B GATE FB 8 16 BOOST 15 T GATE DR 14 T GATE FB 13 T SOURCE 12 SENSE+ 11 SENSE− 10 V+ 9 B GATE DR S PACKAGE 16-LEAD PLASTIC SOL	LT1158IS LT1158CS

ELECTRICAL CHARACTERISTICS

Test Circuit, T_A = 25°C, V^+ = V16 = 12V, V11 = V12 = V13 = 0V, Pins 1 and 4 open, Gate Feedback pins connected to Gate Drive pins unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LT1158I MIN	LT1158I TYP	LT1158I MAX	LT1158C MIN	LT1158C TYP	LT1158C MAX	UNITS
$I_2 + I_{10}$	DC Supply Current (Note 2)	V^+ = 30V, V16 = 15V, V4 = 0.5V V^+ = 30V, V16 = 15V, V6 = 0.8V V^+ = 30V, V16 = 15V, V6 = 2V		 4.5 8	2.2 7 13	3 10 18	 4.5 8	2.2 7 13	3 10 18	mA mA mA
I_{16}	Boost Current	V^+ = V13 = 30V, V16 = 45V, V6 = 0.8V			3	4.5		3	4.5	mA
V6	Input Threshold		●	0.8	1.4	2	0.8	1.4	2	V
I_6	Input Current	V6 = 5V	●		5	15		5	15	μA
V4	Enable Low Threshold	V6 = 0.8V, Monitor V9	●	0.9	1.15	1.4	0.85	1.15	1.4	V
ΔV4	Enable Hysteresis	V6 = 0.8V, Monitor V9	●	1.3	1.5	1.7	1.2	1.5	1.8	V
I_4	Enable Pullup Current	V4 = 0V	●	15	25	35	15	25	35	μA
V15	Charge Pump Voltage	V^+ = 5V, V6 = 2V, Pin 16 open, V13 → 5V V^+ = 30V, V6 = 2V, Pin16 open, V13 → 30V	● ●	9 40	11 43	 47	9 40	11 43	 47	V V
V9	Bottom Gate "ON" Voltage	V^+ = V16 = 18V, V6 = 0.8V	●	12	14.5	17	12	14.5	17	V
V1	Boost Drive Voltage	V^+ = V16 = 18V, V6 = 0.8V, 100mA Pulsed Load	●	12	14.5	17	12	14.5	17	V

ELECTRICAL CHARACTERISTICS

Test Circuit, $T_A = 25°C$, $V^+ = V16 = 12V$, V11 = V12 = V13 = 0V, Pins 1 and 4 open, Gate Feedback pins connected to Gate Drive pins unless otherwise specified.

				LT1158I			LT1158C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V14 – V13	Top Turn-Off Threshold	$V^+ = V16 = 5V$, V6 = 0.8V		1	1.75	2.5	1	1.75	2.5	V
V8	Bottom Turn-Off Threshold	$V^+ = V16 = 5V$, V6 = 2V		1	1.5	2	1	1.5	2	V
I_5	Fault Output Leakage	$V^+ = 30V$, V16 = 15V, V6 = 2V	●		0.1	1		0.1	1	μA
V5	Fault Output Saturation	$V^+ = 30V$, V16 = 15V, V6 = 2V, I5 = 10mA			0.5	1		0.5	1	V
V12 – V11	Fault Conduction Threshold	$V^+ = 30V$, V16 = 15V, V6 = 2V, I5 = 100μA		90	110	130	85	110	135	mV
V12 – V11	Current Limit Threshold	$V^+ = 30V$, V16 = 15V, V6 = 2V, Closed Loop		130	150	170	120	150	180	mV
			●	120		180	120		180	mV
V12 – V11	Current Limit Inhibit V_{DS} Threshold	$V^+ = V12 = 12V$, V6 = 2V, Decrease V11 until V15 goes low		1.1	1.25	1.4	1.1	1.25	1.4	V
t_R	Top Gate Rise Time	Pin 6 (+) Transition, Meas. V15 – V13 (Note 3)	●		130	250		130	250	ns
t_D	Top Gate Turn-Off Delay	Pin 6 (–) Transition, Meas. V15 – V13 (Note 3)	●		350	550		350	550	ns
t_F	Top Gate Fall Time	Pin 6 (–) Transition, Meas. V15 – V13 (Note 3)	●		120	250		120	250	ns
t_R	Bottom Gate Rise Time	Pin 6 (–) Transition, Meas. V9 (Note 3)	●		130	250		130	250	ns
t_D	Bottom Gate Turn-Off Delay	Pin 6 (+) Transition, Meas. V9 (Note 3)	●		200	400		200	400	ns
t_F	Bottom Gate Fall Time	Pin 6 (+) Transition, Meas. V9 (Note 3)	●		100	200		100	200	ns

The ● denotes specifications that apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LT1158IN, LT1158CN: $T_J = T_A + (P_D \times 70°C/W)$

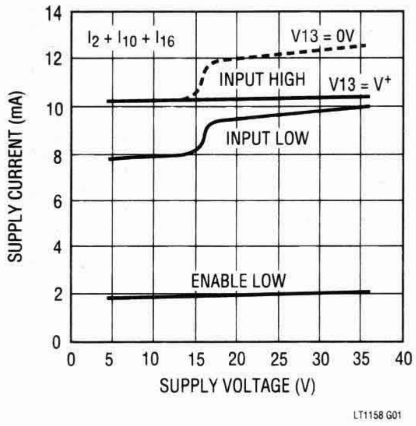
LT1158IS, LT1158CS: $T_J = T_A + (P_D \times 110°C/W)$

Note 2: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See typical performance characteristics and applications information.

Note 3: Gate rise times are measured from 2V to 10V, delay times are measured from the input transition to when the gate voltage has decreased to 10V, and fall times are measured from 10V to 2V.

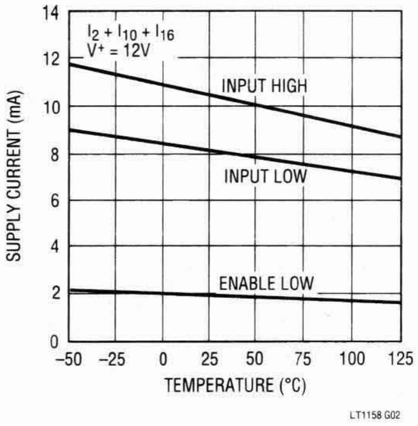
TYPICAL PERFORMANCE CHARACTERISTICS

DC Supply Current



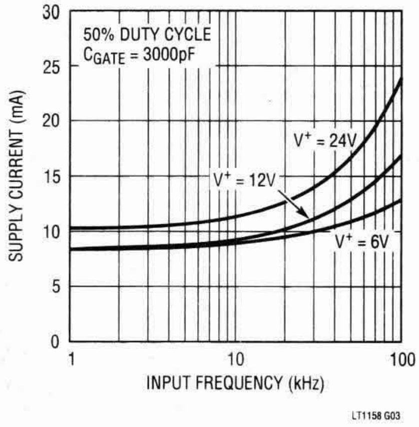
LT1158 G01

DC Supply Current



LT1158 G02

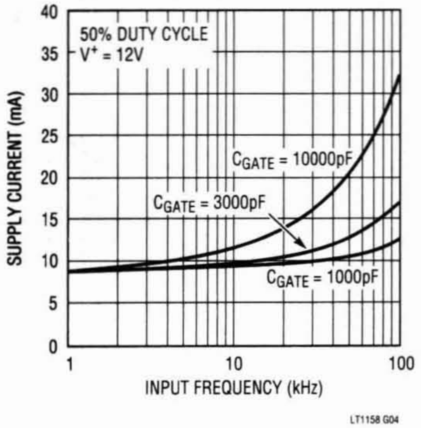
Dynamic Supply Current (V^+)



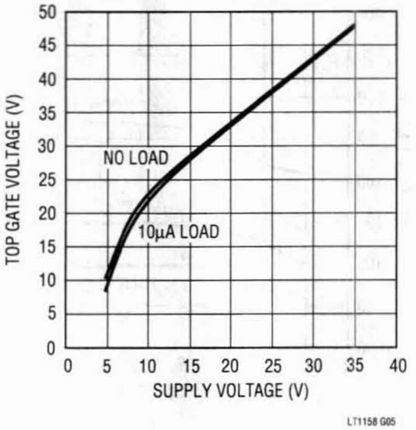
LT1158 G03

TYPICAL PERFORMANCE CHARACTERISTICS

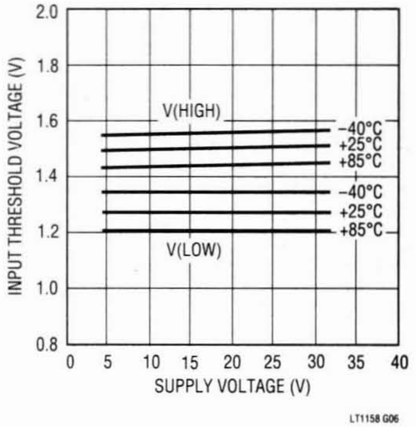
Dynamic Supply Current



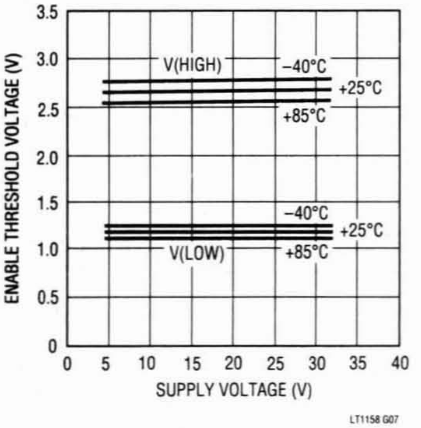
Charge Pump Output Voltage



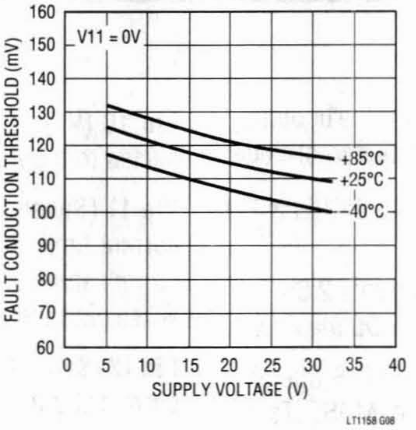
Input Thresholds



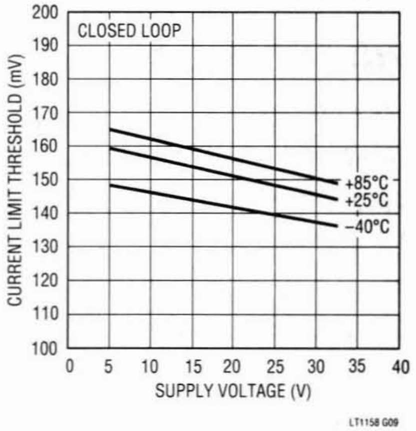
Enable Thresholds



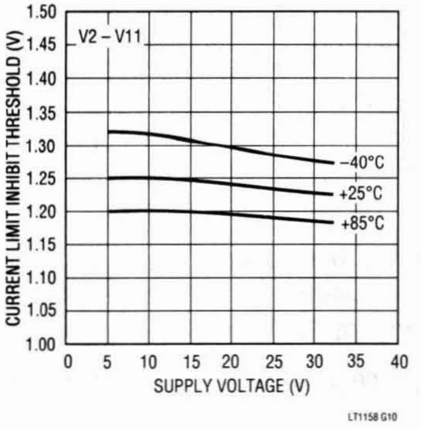
Fault Conduction Threshold



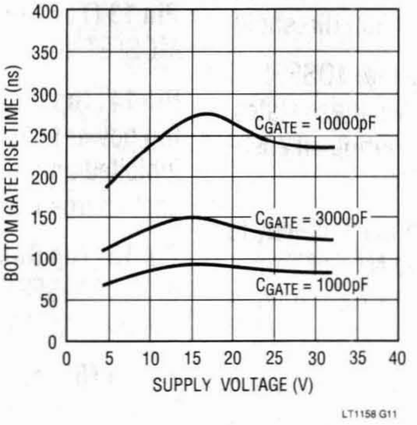
Current Limit Threshold



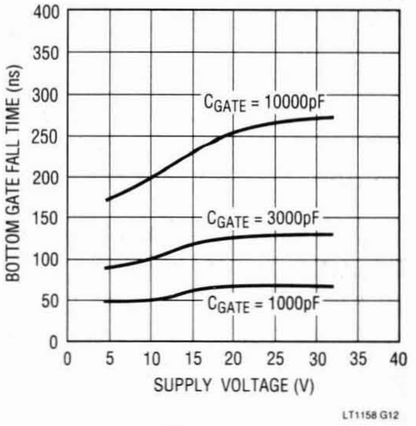
Current Limit Inhibit V_{DS} Threshold



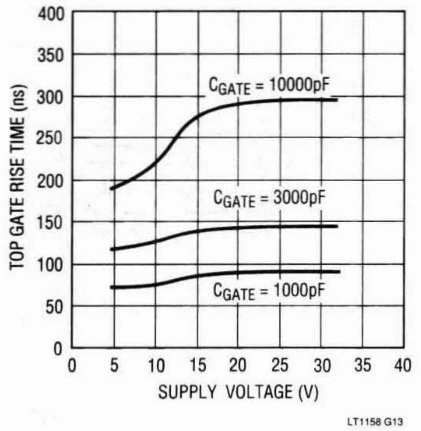
Bottom Gate Rise Time

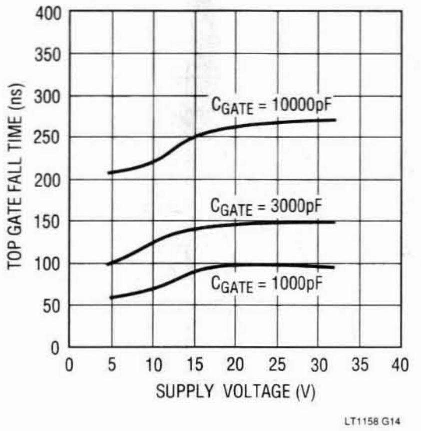


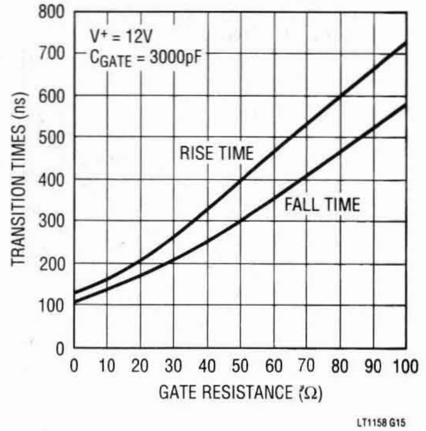
Bottom Gate Fall Time



TYPICAL PERFORMANCE CHARACTERISTICS


Top Gate Rise Time


Top Gate Fall Time


Transition Times vs R_{Gate}

PIN FUNCTIONS

Pin 1 (Boost Drive): Recharges and clamps the bootstrap capacitor to 14.5V higher than pin 13 via an external diode.

Pin 2 (V^+): Main supply pin; must be closely decoupled to the ground pin 7.

Pin 3 (Bias): Decouple point for the internal 2.6V bias generator. *Pin 3 cannot have any external DC loading.*

Pin 4 (Enable): When left open, the LT1158 operates normally. Pulling pin 4 low holds both MOSFETs off regardless of the input state.

Pin 5 ($\overline{\text{Fault}}$): Open collector NPN output which turns on when V12 – V11 exceeds the fault conduction threshold.

Pin 6 (Input): Taking pin 6 high turns the top MOSFET on and bottom MOSFET off; pin 6 low reverses these states. An input latch captures each low state, ignoring an ensuing high until pin 13 has gone below 2.6V.

Pin 8 (Bottom Gate Feedback): Must connect directly to the bottom power MOSFET gate. The top MOSFET turn-on is inhibited until pin 8 has discharged to 1.5V. A hold-on current source also feeds the bottom gate via pin 8.

Pin 9 (Bottom Gate Drive): The high current drive point for the bottom MOSFET. When a gate resistor is used, it is inserted between pin 9 and the gate of the MOSFET.

Pin 10 (V^+): Bottom side driver supply; must be connected to the same supply as pin 2.

Pin 11 (Sense Negative): The floating reference for the current limit comparator. Connects to the low side of a current shunt or Kelvin lead of a current-sensing MOSFET. When pin 11 is within 1.2V of V^+, current limit is inhibited.

Pin 12 (Sense Positive): Connects to the high side of the current shunt or sense lead of a current-sensing MOSFET. A built-in offset between pins 11 and 12 in conjunction with R_{SENSE} sets the top MOSFET short-circuit current.

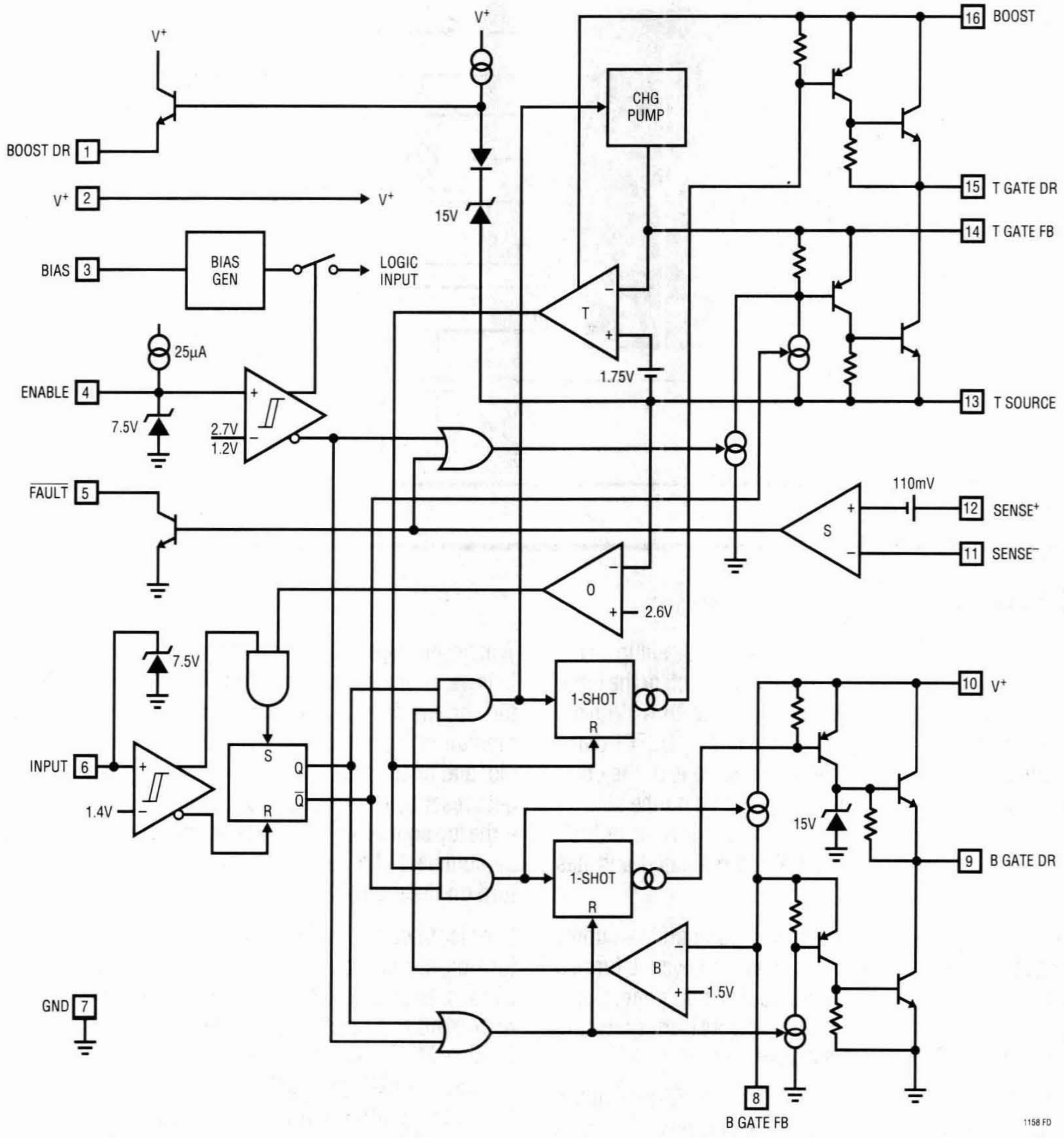
Pin 13 (Top Source): Top side driver return; connects to MOSFET source and low side of the bootstrap capacitor.

Pin 14 (Top Gate Feedback): Must connect directly to the top power MOSFET gate. The bottom MOSFET turn-on is inhibited until V14 – V13 has discharged to 1.75V. An on-chip charge pump also feeds the top gate via pin 14.

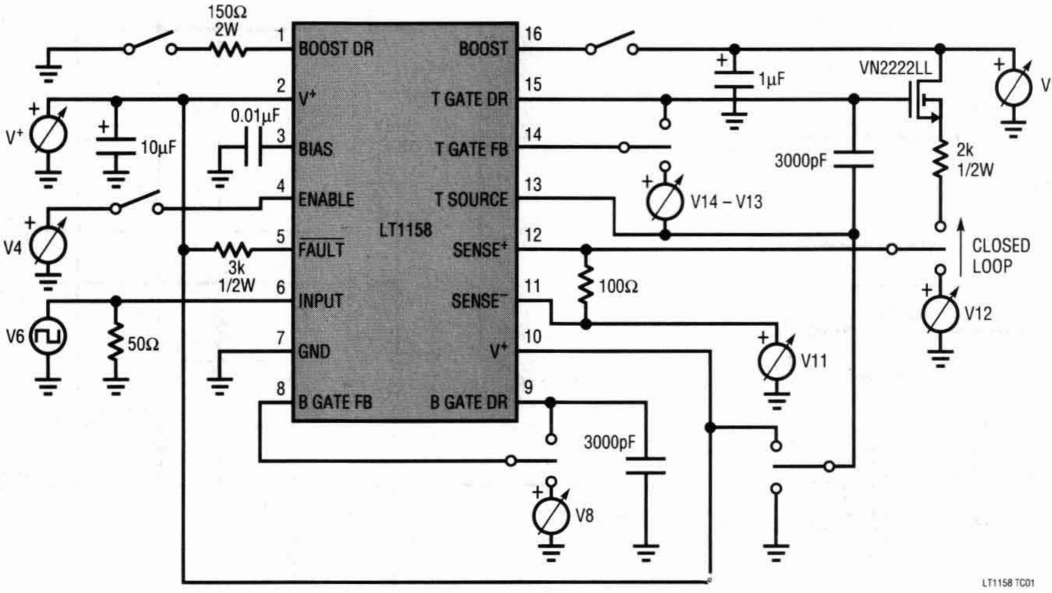
Pin 15 (Top Gate Drive): The high current drive point for the top MOSFET. When a gate resistor is used, it is inserted between pin 15 and the gate of the MOSFET.

Pin 16 (Boost): Top side driver supply; connects to the high side of the bootstrap capacitor and to a diode either from supply ($V^+ < 10V$) or from pin 1 ($V^+ > 10V$).

FUNCTIONAL DIAGRAM


V+
V+
BOOST DR 1
V+ 2
V+
BIAS 3
BIAS GEN
LOGIC INPUT
25µA
ENABLE 4
7.5V
2.7V
1.2V
FAULT 5
CHG PUMP
15V
T
1.75V
0
2.6V
S
110mV
16 BOOST
15 T GATE DR
14 T GATE FB
13 T SOURCE
12 SENSE+
11 SENSE−
7.5V
INPUT 6
1.4V
S
Q
R
Q̄
1-SHOT
R
1-SHOT
R
B
1.5V
15V
10 V+
9 B GATE DR
8 B GATE FB
GND 7
1158 FD

TEST CIRCUIT


150Ω
2W
1
BOOST DR
BOOST
16
2
V⁺
T GATE DR
15
0.01μF
3
BIAS
T GATE FB
14
4
ENABLE
T SOURCE
13
LT1158
5
FAULT
SENSE⁺
12
3k
1/2W
6
INPUT
SENSE⁻
11
7
GND
V⁺
10
8
B GATE FB
B GATE DR
9
V⁺
10μF
V4
V6
50Ω
1μF
VN2222LL
V16
3000pF
2k
1/2W
V14 – V13
CLOSED
LOOP
100Ω
V12
V11
3000pF
V8
LT1158 TC01

OPERATION (Refer to Functional Diagram)

The LT1158 self-enables via an internal 25μA pullup on the enable pin 4. When pin 4 is pulled down, much of the input logic is disabled, reducing supply current to 2mA. With pin 4 low, the input state is ignored and both MOSFET gates are actively held low. With pin 4 enabled, one or the other of the 2 MOSFETs is turned on, depending on the state of the input pin 6: high for top side on, and low for bottom side on. The 1.4V input threshold is regulated and has 200mV of hysteresis.

In order to allow operation over 5V to 30V nominal supply voltages, an internal bias generator is employed to furnish constant bias voltages and currents. The bias generator is decoupled at pin 3 to eliminate any effects from switching transients. *No DC loading is allowed on pin 3.*

The top and bottom gate drivers in the LT1158 each utilize two gate connections: 1) A gate drive pin, which provides the turn-on and turn-off currents through an optional series gate resistor; and 2) A gate feedback pin which connects directly to the gate to monitor the gate-to-source voltage and supply the DC gate sustaining current.

Whenever there is an input transition on pin 6, the LT1158 follows a logical sequence to turn off one MOSFET and turn on the other. First, turn-off is initiated, then VGS is monitored until it has decreased below the turn-off threshold, and finally the other gate is turned on. An input latch gets reset by every low state at pin 6, but can only be set if the top source pin has gone low, indicating that there will be sufficient charge in the bootstrap capacitor to safely turn on the top MOSFET.

In order to conserve power, the gate drivers only provide turn-on current for up to 2μs, set by internal one-shot circuits. Each LT1158 driver can deliver 500mA for 2μs, or 1000nC of gate charge – more than enough to turn on multiple MOSFETs in parallel. Once turned on, each gate is held high by a DC gate sustaining current: the bottom gate by a 100μA current source, and the top gate by an on-chip charge pump running at approximately 500kHz.

The floating supply for the top side driver is provided by a bootstrap capacitor between the boost pin 16 and top source pin 13. This capacitor is recharged each time pin

OPERATION (Refer to Functional Diagram)

13 goes low in PWM operation, and is maintained by the charge pump when the top MOSFET is on DC. A regulated boost driver at pin 1 employs a source-referenced 15V clamp that prevents the bootstrap capacitor from overcharging regardless of V^+ or output transients.

The LT1158 provides a current sense comparator and fault output circuit for protection of the top power MOSFET. The comparator input pins 11 and 12 are normally connected across a shunt in the source of the top power MOSFET (or to a current-sensing MOSFET). When pin 11 is more than 1.2V below V^+ and V12 – V11 exceeds the 110mV offset, $\overline{\text{fault}}$ pin 5 begins to sink current. During a short circuit, the feedback loop regulates V12 – V11 to 150mV, thereby limiting the top MOSFET current.

APPLICATIONS INFORMATION

Power MOSFET Selection

Since the LT1158 inherently protects the top and bottom MOSFETs from simultaneous conduction, there are no size or matching constraints. Therefore selection can be made based on the operating voltage and $R_{DS(ON)}$ requirements. The MOSFET BV_{DSS} should be at least 2 × V_{SUPPLY}, and should be increased to 3 × V_{SUPPLY} in harsh environments with frequent fault conditions. For the LT1158 maximum operating supply of 30V, the MOSFET BV_{DSS} should be from 60V to 100V.

The MOSFET $R_{DS(ON)}$ is specified at T_J = 25°C and is generally chosen based on the operating efficiency required as long as the maximum MOSFET junction temperature is not exceeded. The dissipation in each MOSFET is given by:

$$P = D\left(I_{DS}\right)^2\left(1+\partial\right)R_{DS(ON)}$$

where D is the duty cycle and is the increase in $R_{DS(ON)}$ at the anticipated MOSFET junction temperature. From this equation the required $R_{DS(ON)}$ can be derived:

$$R_{DS(ON)} = \frac{P}{D\left(I_{DS}\right)^2\left(1+\partial\right)}$$

For example, if the MOSFET loss is to be limited to 2W when operating at 5A and a 90% duty cycle, the required $R_{DS(ON)}$ would be 89m /(1 +). (1 +) is given for each MOSFET in the form of a normalized $R_{DS(ON)}$ vs. temperature curve, but = 0.007/°C can be used as an approximation for low voltage MOSFETs. Thus if T_A = 85°C and the available heat sinking has a thermal resistance of 20°C/W, the MOSFET junction temperature will be 125°C, and = 0.007(125 – 25) = 0.7. This means that the required $R_{DS(ON)}$ of the MOSFET will be 89m /1.7 = 52.3m , which can be satisfied by an IRFZ34.

Note that these calculations are for the continuous operating condition; power MOSFETs can sustain far higher dissipations during transients. Additional $R_{DS(ON)}$ constraints are discussed under **Starting High In-Rush Current Loads.**

Paralleling MOSFETs

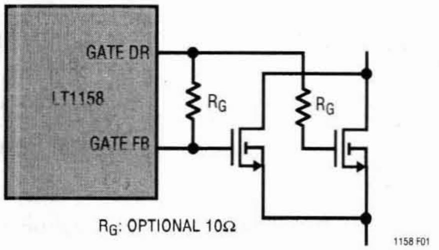


Figure 1. Paralleling MOSFETs

When the above calculations result in a lower $R_{DS(ON)}$ than is economically feasible with a single MOSFET, two or more MOSFETs can be paralleled. The MOSFETs will inherently share the currents according to their $R_{DS(ON)}$ ratio. The LT1158 top and bottom drivers can each drive four power MOSFETs in parallel with only a small loss in

APPLICATIONS INFORMATION

switching speeds (see Typical Performance Characteristics). Individual gate resistors may be required to "decouple" each MOSFET from its neighbors to prevent high frequency oscillations – consult manufacturer's recommendations. If individual gate decoupling resistors are used, the gate feedback pins can be connected to any one of the gates.

Driving multiple MOSFETs in parallel may restrict the operating frequency at high supply voltages to prevent over-dissipation in the LT1158 (see **Gate Charge and Driver Dissipation** below). When the total gate capacitance exceeds 10,000pF on the top side, the bootstrap capacitor should be increased proportionally above 0.1µF.

Gate Charge and Driver Dissipation

A useful indicator of the load presented to the driver by a power MOSFET is the total gate charge Q_G, which includes the additional charge required by the gate-to-drain swing. Q_G is usually specified for $V_{GS} = 10V$ and $V_{DS} = 0.8V_{DS(MAX)}$.

When the supply current is measured in a switching application, it will be larger than given by the DC electrical characteristics because of the additional supply current associated with sourcing the MOSFET gate charge:

$$I_{SUPPLY} = I_{DC} + \left(\frac{dQ_G}{dt}\right)_{TOP} + \left(\frac{dQ_G}{dt}\right)_{BOTTOM}$$

The actual increase in supply current is slightly higher due to LT1158 switching losses and the fact that the gates are being charged to more than 10V. Supply current vs. switching frequency is given in the Typical Performance Characteristics.

The LT1158 junction temperature can be estimated by using the equations given in Note 1 of the electrical characteristics. For example, the LT1158SI is limited to less than 25mA from a 24V supply:

$$\begin{aligned} T_J &= 85°C + (25mA \times 24V \times 110°C/W) \\ &= 151°C \text{ exceeds absolute maximum} \end{aligned}$$

In order to prevent the maximum junction temperature from being exceeded, the LT1158 supply current must be checked with the actual MOSFETs operating at the maximum switching frequency.

MOSFET Gate Drive Protection

For supply voltages of over 8V, the LT1158 will protect standard N-channel MOSFETs from under or over voltage gate drive conditions for any input duty cycle including DC. Gate-to-source zener clamps are not required and not recommended since they can reduce operating efficiency.

A discontinuity in tracking between the output pulse width and input pulse width may be noted as the top side MOSFET approaches 100% duty cycle. As the input low signal becomes narrower, it may become shorter than the time required to recharge the bootstrap capacitor to a safe voltage for the top side driver. Below this duty cycle the output pulse width will stop tracking the input until the input low signal is <100ns, at which point the output will jump to the DC condition of top MOSFET "on" and bottom MOSFET "off."

Low Voltage Operation

The LT1158 can operate from 5V supplies (4.5V min.) and in 6V battery-powered applications by using logic-level N-channel power MOSFETs. These MOSFETs have 2V maximum threshold voltages and guaranteed $R_{DS(ON)}$ limits at $V_{GS} = 4V$. The switching speed of the LT1158, unlike CMOS drivers, does not degrade at low supply voltages. For operation down to 4.5V, the boost pin should be connected as shown in Figure 2 to maximize gate drive to the top side MOSFET. Supply voltages over 10V should not be used with logic-level MOSFETs because of their lower maximum gate-to-source voltage rating.

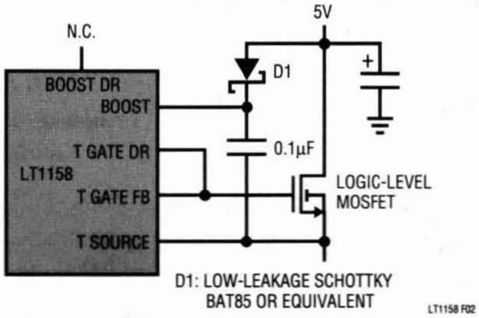


Figure 2. Low Voltage Operation

APPLICATIONS INFORMATION

Ugly Transient Issues

In PWM applications the drain current of the top MOSFET is a square wave at the input frequency and duty cycle. To prevent large voltage transients at the top drain, a low ESR electrolytic capacitor must be used and returned to the power ground. The capacitor is generally in the range of 250µF to 5000µF and must be physically sized for the RMS current flowing in the drain to prevent heating and premature failure. In addition, the LT1158 requires a separate 10µF capacitor connected closely between pins 2 and 7.

The LT1158 top source and sense pins are internally protected against transients below ground and above supply. However, the gate drive pins cannot be forced below ground. In most applications, negative transients coupled from the source to the gate of the top MOSFET do not cause any problems. However in some high current (10A and above) motor control applications, negative transients on the top gate drive may cause early tripping of the current limit. A small Schottky diode (BAT85) from pin 15 to ground avoids this problem.

Switching Regulator Applications

The LT1158 is ideal as a synchronous switch driver to improve the efficiency of step-down (buck) switching regulators. Most step-down regulators use a high current Schottky diode to conduct the inductor current when the switch is off. The fractions of the oscillator period that the switch is on (switch conducting) and off (diode conducting) are given by:

$$\text{SWITCH “ON”} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times \text{TOTAL PERIOD}$$

$$\text{SWITCH “OFF”} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right) \times \text{TOTAL PERIOD}$$

Note that for $V_{IN} > 2V_{OUT}$, the switch is off longer than it is on, making the diode losses more significant than the switch. The worst case for the diode is during a short circuit, when V_{OUT} approaches zero and the diode conducts the short circuit current almost continuosly.

Figure 3 shows the LT1158 used to synchronously drive a pair of power MOSFETs in a step-down regulator application, where the top MOSFET is the switch and the bottom MOSFET replaces the Schottky diode. Since both conduction paths have low losses, this approach can result in very high efficiency – from 90% to 95% in most applications. And for regulators under 5A, using low $R_{DS(ON)}$ N-channel MOSFETs eliminates the need for heatsinks.

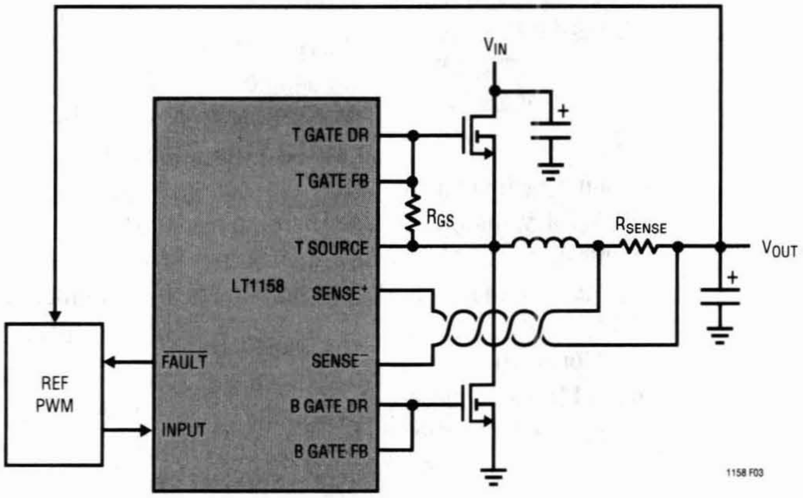


Figure 3. Adding Synchronous Switching to a Step-Down Switching Regulator

APPLICATIONS INFORMATION

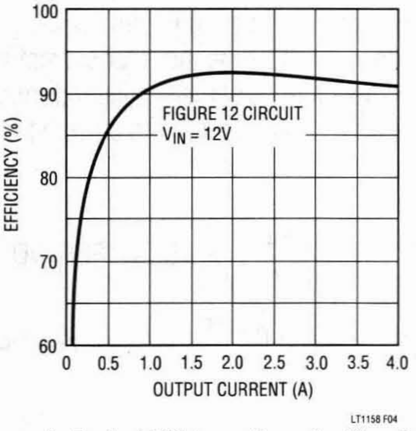


Figure 4. Typical Efficiency Curve for Step-Down Regulator with Synchronous Switch

One fundamental difference in the operation of a step-down regulator with synchronous switching is that it never becomes discontinuous at light loads. The inductor current doesn't stop ramping down when it reaches zero, but actually reverses polarity resulting in a constant ripple current independent of load. This does not cause any efficiency loss as might be expected, since the negative inductor current is returned to V_{IN} when the switch turns back on.

The LT1158 performs the synchronous MOSFET drive and current sense functions in a step-down switching regulator. A reference and PWM are required to complete the regulator. Any voltage-mode PWM controller may be used, but the LT3525 is particularly well suited to high power, high efficiency applications such as the 10A circuit shown in Figure 13. In higher current regulators a small Schottky diode across the bottom MOSFET helps to reduce reverse-recovery switching losses.

The LT1158 input pin can also be driven directly with a ramp or sawtooth. In this case, the DC level of the input waveform relative to the 1.4V threshold sets the LT1158 duty cycle. In the ultra low-dropout 5V circuit shown in Figure 11, an LT1431 controls the DC level of a triangle wave generated by a CMOS 555. The Figure 10 and 12 circuits use an RC network to ramp the LT1158 input back up to its 1.4V threshold following each switch cycle, setting a constant off time. Figure 4 shows the efficiency vs. output current for the Figure 12 regulator with V_{IN} = 12V.

Current Limit in Switching Regulator Applications

Current is sensed by the LT1158 by measuring the voltage across a current shunt (low-valued resistor). Normally, this shunt is placed in the source lead of the top MOSFET (see **Short-Circuit Protection in Bridge Applications**). However, in step-down switching regulator applications, the remote current sensing capability of the LT1158 allows the actual inductor current to be sensed. This is done by placing the shunt in the output lead of the inductor as shown in Figure 3. Routing of the sense$^+$ and sense$^-$ PC traces is critical to prevent stray pickup. These traces must be routed together at minimum spacing and use a Kelvin connection at the shunt.

When the voltage across R_{SENSE} exceeds 110mV, the LT1158 $\overline{\text{fault}}$ pin begins to conduct. By feeding the $\overline{\text{fault}}$ signal back to a control input of the PWM, the LT1158 will assume control of the duty cycle forming a true current mode loop to limit the output current:

$$I_{OUT} = \frac{110mV}{R_{SENSE}} \text{ in current limit}$$

In LT3525 based circuits, connecting the $\overline{\text{fault}}$ pin to the LT3525 soft-start pin accomplishes this function. In circuits where the LT1158 input is being driven with a ramp or sawtooth, the $\overline{\text{fault}}$ pin is used to pull down the DC level of the input.

The constant off time circuits shown in Figures 10 and 12 are unique in that they also use the current sense during normal operation. The LT1431 output reduces the normal LT1158 110mV fault conduction threshold such that the $\overline{\text{fault}}$ pin conducts at the required load current, thus discharging the input ramp capacitor. In current limit the LT1431 output turns off, allowing the fault conduction threshold to reach its normal value.

The resistor R_{GS} shown in Figure 3 is necessary to prevent output voltage overshoot due to charge coupled into the gate of the top MOSFET by a large startup dv/dt on V_{IN}. If DC operation of the top MOSFET is required, R_{GS} must be 330k or greater to prevent loading the charge pump.

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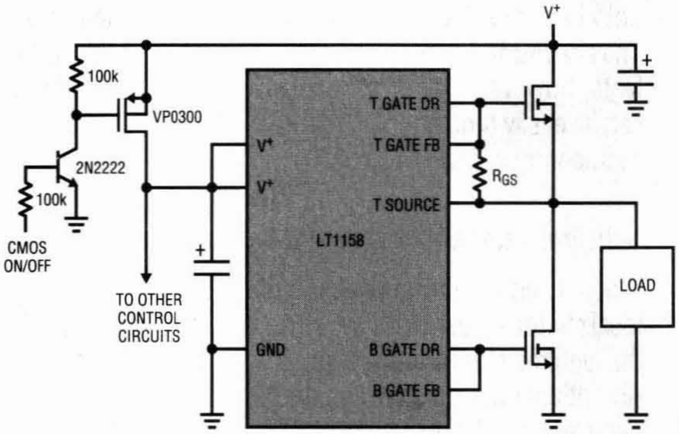
Low Current Shutdown

The LT1158 may be shutdown to a current level of 2mA by pulling the enable pin 4 low. In this state both the top and bottom MOSFETs are actively held off against any transients which might occur on the output during shutdown. This is important in applications such as 3-phase DC motor control when one of the phases is disabled while the other two are switching.

If zero standby current is required and the load returns to ground, then a switch can be inserted into the supply path of the LT1158 as shown in Figure 5. Resistor R_{GS} ensures that the top MOSFET gate discharges, while the voltage across the bottom MOSFET goes to zero. The voltage drop across the P-channel supply switch must be less than 300mV, and R_{GS} must be 330k or greater for DC operation. This technique is not recommended for applications which require the LT1158 V_{DS} sensing function.



V⁺
100k
VP0300
2N2222
100k
CMOS ON/OFF
TO OTHER CONTROL CIRCUITS
V⁺
V⁺
GND
LT1158
T GATE DR
T GATE FB
T SOURCE
B GATE DR
B GATE FB
R_{GS}
LOAD
1158 F05

Figure 5. Adding Zero Current Shutdown

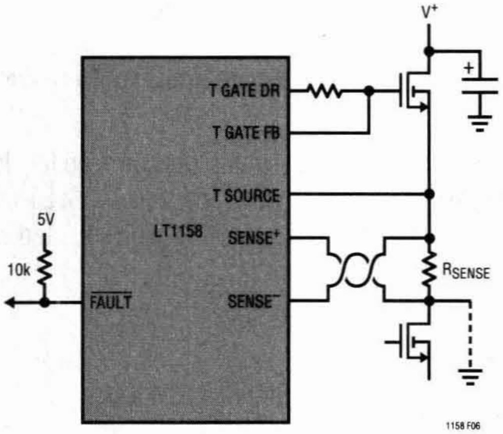
Short-Circuit Protection in Bridge Applications

The LT1158 protects the top power MOSFET from output shorts to ground, or in a full bridge application, shorts across the load. Both standard 3-lead MOSFETs and current-sensing 5-lead MOSFETs can be protected. The bottom MOSFET is not protected from shorts to supply.

Current is sensed by measuring the voltage across a current shunt in the source lead of a standard 3-lead MOSFET (Figure 6). For the current-sensing MOSFET shown in Figure 7, the sense resistor is inserted between the sense and Kelvin leads.

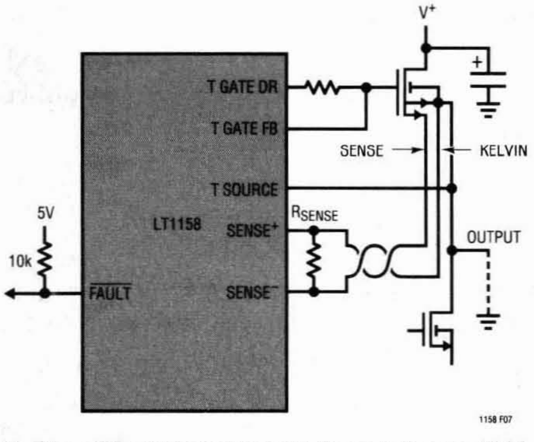
The sense⁺ and sense⁻ PC traces must be routed together at minimum spacing to prevent stray pickup, and a Kelvin connection must be used at the current shunt for the 3-lead MOSFET. Using a twisted pair is the safest approach and is recommended for sense runs of several inches.

When the voltage across R_{SENSE} exceeds 110mV, the LT1158 $\overline{\text{fault}}$ pin begins to conduct, signaling a fault condition. The current in a short circuit ramps very rapidly, limited only by the series inductance and ultimately the MOSFET and shunt resistance. Due to the response time of the LT1158 current limit loop, an initial current spike of



V⁺
5V
10k
LT1158
T GATE DR
T GATE FB
T SOURCE
SENSE⁺
SENSE⁻
FAULT
R_{SENSE}
1158 F06

Figure 6. Short-Circuit Protection with Standard MOSFET

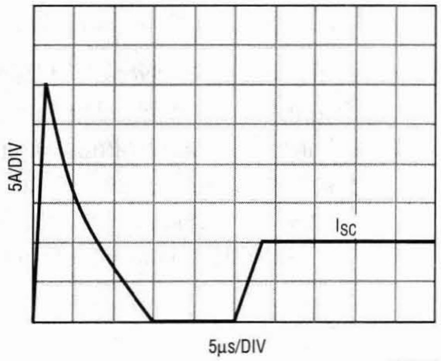


V⁺
5V
10k
LT1158
T GATE DR
T GATE FB
T SOURCE
SENSE⁺
SENSE⁻
FAULT
R_{SENSE}
SENSE
KELVIN
OUTPUT
1158 F07

Figure 7. Short-Circuit Protection with Current-Sensing MOSFET

APPLICATIONS INFORMATION

from 2 to 5 times the final value will be present for a few μs, followed by an interval in which $I_{DS} = 0$. The current spike is normally well within the safe operating area (SOA) of the MOSFET, but can be further reduced with a small (0.5μH) inductor in series with the output.



LT1158 F08

Figure 8. Top MOSFET Short-Circuit Turn-On current

If neither the enable nor input pins are pulled low in response to the fault indication, the top MOSFET current will recover to a steady-state value I_{SC} regulated by the LT1158 as shown in Figure 8:

$$\left.\begin{aligned} I_{SC} &= \frac{150mV}{R_{SENSE}} \\ R_{SENSE} &= \frac{150mV}{I_{SC}} \end{aligned}\right\} \text{Standard 3-Lead MOSFET}$$

$$\left.\begin{aligned} I_{SC} &= \frac{r(150mV)}{R_{SENSE}}\left(1-\frac{150mV}{\Delta V}\right)^{-2} \\ R_{SENSE} &= \frac{r(150mV)}{I_{SC}}\left(1-\frac{150mV}{\Delta V}\right)^{-2} \end{aligned}\right\} \text{5-Lead MOSFET}$$

r = current sense ratio, $\Delta V = V_{GS} - V_T$

The time for the current to recover to I_{SC} following the initial current spike is approximately $Q_{GS}/0.5mA$, where Q_{GS} is the MOSFET gate-to-source charge. I_{SC} need not be set higher than the required startup current for motors (see **Starting High In-Rush Current Loads**). Note that the value of R_{SENSE} for the 5-lead MOSFET increases by the current sensing ratio (typically 1000 – 3000), thus eliminating the need for a low-valued shunt. V is in the range of 1V to 3V in most applications.

Assuming a dead short, the MOSFET dissipation will rise to $V_{SUPPLY} \times I_{SC}$. For example, with a 24V supply and I_{SC} = 10A, the dissipation would be 240W. To determine how long the MOSFET can remain at this dissipation level before it must be shut down, refer to the SOA curves given in the MOSFET data sheet. For example, an IRFZ34 would be safe if shut down within 10ms.

A Tektronix A6303 current probe is highly recommended for viewing output fault currents.

If Short-Circuit Protection is Not Required

In applications which do not require the current sense capability of the LT1158, the sense pins 11 and 12 should both be connected to pin 13, and the $\overline{\text{fault}}$ pin 5 left open. The enable pin 4 may still be used to shut down the device. Note, however, that when unprotected the top MOSFET can be easily (and often dramatically) destroyed by even a momentary short.

Self-Protection with Automatic Restart

When using the current sense circuits of Figures 6 and 7, local shutdown can be achieved by connecting the $\overline{\text{fault}}$ pin through resistor R_F to the enable pin as shown in Figure 9. An optional thermostat mounted to the load or MOSFET heatsink can also be used to pull enable low.

An internal 25μA current source normally keeps the enable capacitor C_{EN} charged to the 7.5V clamp voltage (or to V^+, for $V^+ < 7.5V$). When a fault occurs, C_{EN} is discharged to below the enable low threshold (1.15V typ.) which shuts down both MOSFETs. When the $\overline{\text{fault}}$ pin or thermostat releases, C_{EN} recharges to the upper enable threshold where restart is attempted. In a sustained short circuit, $\overline{\text{fault}}$ will again pull low and the cycle will repeat until the short is removed. The time to shut down for a DC input or thermal fault is given by:

$t_{SHUTDOWN} = (100 + 0.8R_F)\, C_{EN}$ DC input

APPLICATIONS INFORMATION

Note that for the first event only, $t_{SHUTDOWN}$ is approximately twice the above value since C_{EN} is being discharged all the way from its quiescent voltage. Allowable values for R_F are from zero to 10k.

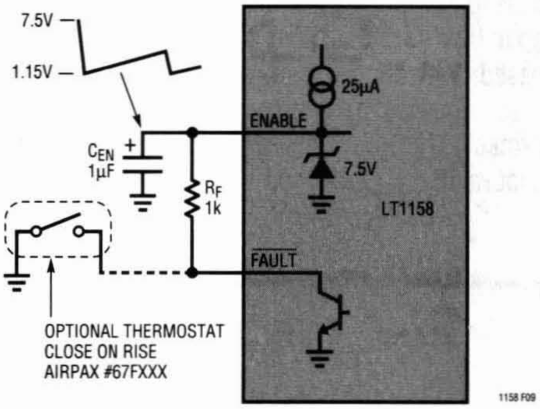


Figure 9. Self-Protection with Auto Restart

$t_{SHUTDOWN}$ becomes more difficult to analyze when the output is shorted with a PWM input. This is because the $\overline{\text{fault}}$ pin only conducts when fault currents are actually present in the MOSFET. $\overline{\text{Fault}}$ does not conduct while the input is low or during the interval $I_{DS} = 0$ in Figure 8. Thus $t_{SHUTDOWN}$ will safely increase when the duty cycle of the current in the top MOSFET is low, maintaining the average MOSFET current at a relatively constant level.

The length of time following shutdown before restart is attempted is given by:

$$t_{RESTART} = \left(\frac{1.5V}{25\mu A}\right)C_{EN} = \left(6\times10^4\right)C_{EN}$$

In Figure 9, the top MOSFET would shut down after being in DC current limit for 0.9ms and try to restart at 60ms intervals, thus producing a duty cyle of 1.5% in short circuit. The resulting average top MOSFET dissipation during a short is easily measured by taking the product of the supply voltage and the average supply current.

Starting High In-Rush Current Loads

The LT1158 has a V_{DS} sensing function which allows more than I_{SC} to flow in the top MOSFET providing that the sense⁻ pin is within 1.2V of supply. Under these conditions the current is limited only by the $R_{DS(ON)}$ in series with R_{SENSE}. For a 5-lead MOSFET the current is limited by $R_{DS(ON)}$ alone, since R_{SENSE} is not in the output path (see Figure 7). Again adjusting $R_{DS(ON)}$ for temperature, the worst-case start currents are:

$$I_{START} = \frac{1.2V}{\left(1+\partial\right)R_{DS(ON)} + R_{SENSE}} \quad \text{3-Lead MOSFET}$$

$$I_{START} = \frac{1.2V}{\left(1+\partial\right)R_{DS(ON)}} \quad \text{5-Lead MOSFET}$$

Properly sizing the MOSFET for I_{START} allows inductive loads with long time-constants, such as motors with high mechanical inertia, to be started.

Returning to the example used in **Power MOSFET Selection**, an IRFZ34 ($R_{DS(ON)} = 50$m max.) was selected for operation at 5A. If the short circuit current is also set at 5A, what start current can be supported? From the equation for R_{SENSE}, a 30m shunt would be required, allowing the worst-case start current to be calculated:

$$I_{START} = \frac{1.2V}{\left(1.7\right)50m\Omega + 30m\Omega} = 10A$$

This calculation gives the minimum current which could be delivered with the IRFZ34 at $T_J = 125°C$ without activating the $\overline{\text{fault}}$ pin on the LT1158. If more start current is required, using an IRFZ44 ($R_{DS(ON)} = 28$m max.) would increase I_{START} to over 15A at $T_J = 110°C$, even though the short circuit current remains at 5A.

In order for the V_{DS} sensing function to work properly, the supply pins for the LT1158 must be connected at the drain of the top MOSFET, which must be properly decoupled (see **Ugly Transient Issues**).

Driving Lamps

Incandescent lamps represent a challenging load because they have much in common with a short circuit when cold. The top gate driver in the LT1158 can be configured to turn on large lamps while still protecting the power MOSFET

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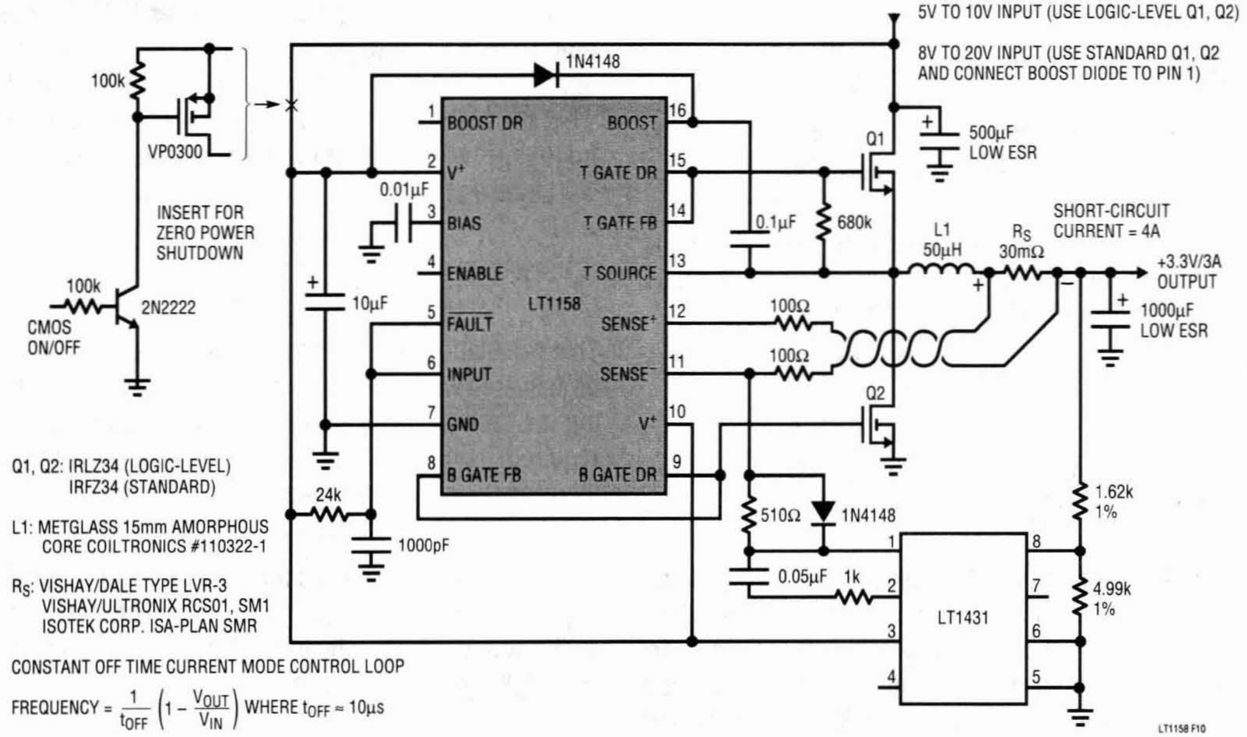
from a true short. This is done by using the current limit to control cold filament current in conjunction with the self-protection circuit of Figure 9. The reduced cold filament current also extends the life of the filament.

A good guideline is to choose R_{SENSE} to set I_{SC} at approximately twice the steady state "on" current of the lamp(s). $t_{SHUTDOWN}$ is then made long enough to guarantee that the lamp filaments heat and drop out of current limit before the enable capacitor discharges to the enable low threshold. For a short circuit, the enable capacitor will continue to discharge below the threshold, shutting down the top MOSFET. The LT1158 will then go into the automatic restart mode described in **Self-Protection with Automatic Restart** above.

The time constant for an incandescent filament is tens of milliseconds, which means that $t_{SHUTDOWN}$ will have to be longer than in most other applications. This places increased SOA demands on the MOSFET during a short circuit, requiring that a larger than normal device be used. A protected high current lamp driver application is shown in Figure 18.

TYPICAL APPLICATIONS


5V TO 10V INPUT (USE LOGIC-LEVEL Q1, Q2)
8V TO 20V INPUT (USE STANDARD Q1, Q2 AND CONNECT BOOST DIODE TO PIN 1)
1N4148
100k
VP0300
INSERT FOR ZERO POWER SHUTDOWN
100k
2N2222
CMOS ON/OFF
BOOST DR
BOOST
V⁺
T GATE DR
0.01μF
BIAS
T GATE FB
ENABLE
T SOURCE
10μF
FAULT
LT1158
SENSE⁺
INPUT
SENSE⁻
GND
V⁺
B GATE FB
B GATE DR
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
24k
1000pF
500μF LOW ESR
Q1
0.1μF
680k
SHORT-CIRCUIT CURRENT = 4A
L1 50μH
R_S 30mΩ
+3.3V/3A OUTPUT
100Ω
100Ω
1000μF LOW ESR
Q2
510Ω
1N4148
0.05μF
1k
LT1431
1.62k 1%
4.99k 1%
LT1158 F10

Q1, Q2: IRLZ34 (LOGIC-LEVEL)
IRFZ34 (STANDARD)

L1: METGLASS 15mm AMORPHOUS CORE COILTRONICS #110322-1

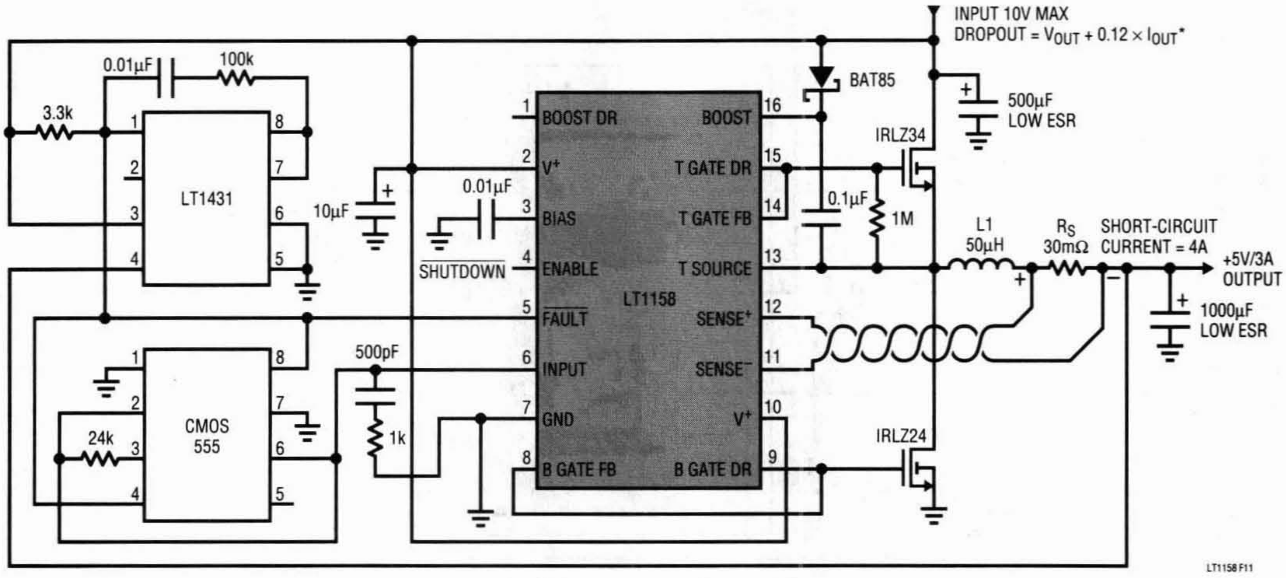
R_S: VISHAY/DALE TYPE LVR-3
VISHAY/ULTRONIX RCS01, SM1
ISOTEK CORP. ISA-PLAN SMR

CONSTANT OFF TIME CURRENT MODE CONTROL LOOP

$$\text{FREQUENCY} = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \text{ WHERE } t_{OFF} \approx 10\mu s$$

Figure 10. High Efficiency 3.3V Step-Down Switching Regulator (Requires No Heatsinks)

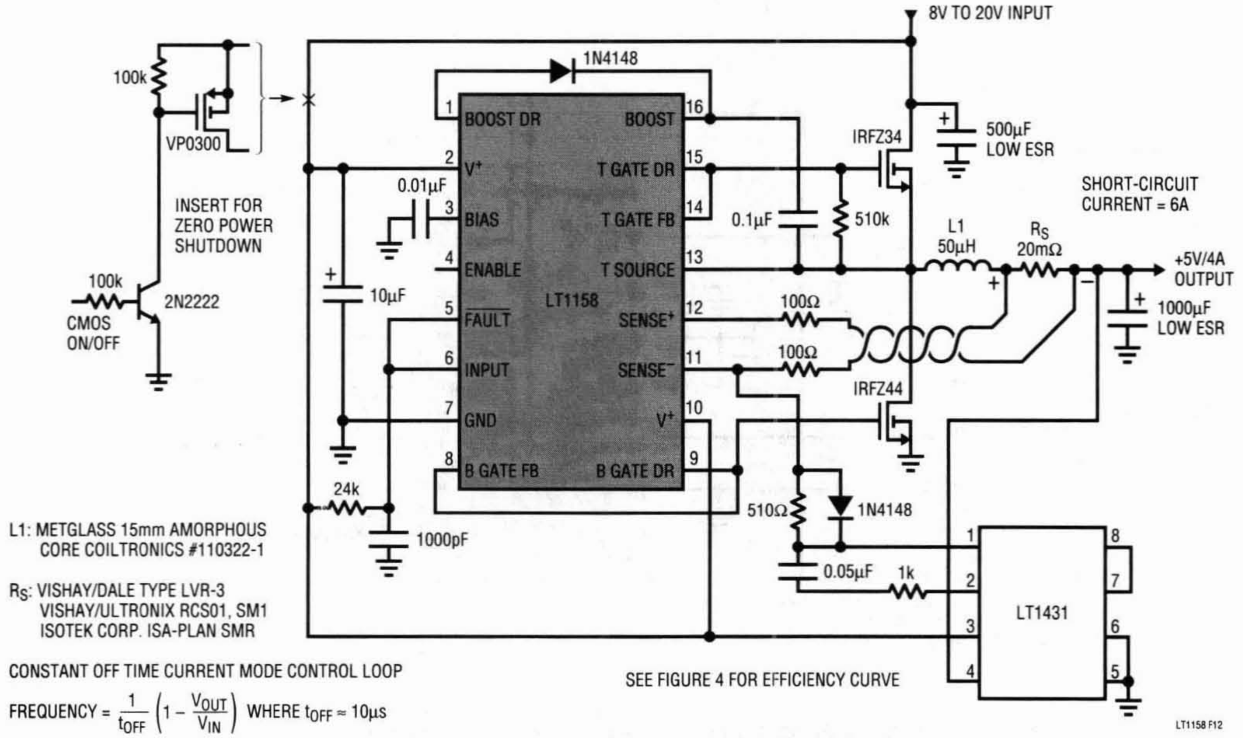
TYPICAL APPLICATIONS


INPUT 10V MAX
DROPOUT = V_{OUT} + 0.12 × I_{OUT}*
0.01µF
100k
3.3k
LT1431
10µF
0.01µF
SHUTDOWN
BOOST DR
V+
BIAS
ENABLE
FAULT
INPUT
GND
B GATE FB
BOOST
T GATE DR
T GATE FB
T SOURCE
SENSE+
SENSE−
V+
B GATE DR
LT1158
BAT85
500µF
LOW ESR
IRLZ34
0.1µF
1M
L1
50µH
R_S
30mΩ
SHORT-CIRCUIT
CURRENT = 4A
+5V/3A
OUTPUT
1000µF
LOW ESR
CMOS
555
24k
500pF
1k
IRLZ24
LT1158 F11

*THE LT1431 CONTROLS THE D.C. LEVEL OF THE CMOS 555 TRIANGLE WAVE OSCILLATOR. IN DROPOUT, THE TOP MOSFET IS TURNED ON CONTINUOUSLY AND THE OUTPUT VOLTAGE TRACKS THE INPUT.

CMOS 555: LMC555 OR TLC555
L1: COILTRONICS CTX50-3-MP
R_S: VISHAY/ULTRONIX RCS01, SM1
ISOTEK CORP. ISA-PLAN SMR

Figure 11. Ultra Low Dropout 5V Switching Regulator (Requires No Heatsinks)


8V TO 20V INPUT
100k
VP0300
INSERT FOR
ZERO POWER
SHUTDOWN
100k
2N2222
CMOS
ON/OFF
1N4148
BOOST DR
V+
BIAS
ENABLE
FAULT
INPUT
GND
B GATE FB
BOOST
T GATE DR
T GATE FB
T SOURCE
SENSE+
SENSE−
V+
B GATE DR
LT1158
0.01µF
10µF
24k
1000pF
500µF
LOW ESR
IRFZ34
0.1µF
510k
SHORT-CIRCUIT
CURRENT = 6A
L1
50µH
R_S
20mΩ
+5V/4A
OUTPUT
1000µF
LOW ESR
100Ω
100Ω
IRFZ44
510Ω
1N4148
0.05µF
1k
LT1431
LT1158 F12

L1: METGLASS 15mm AMORPHOUS CORE COILTRONICS #110322-1

R_S: VISHAY/DALE TYPE LVR-3
VISHAY/ULTRONIX RCS01, SM1
ISOTEK CORP. ISA-PLAN SMR

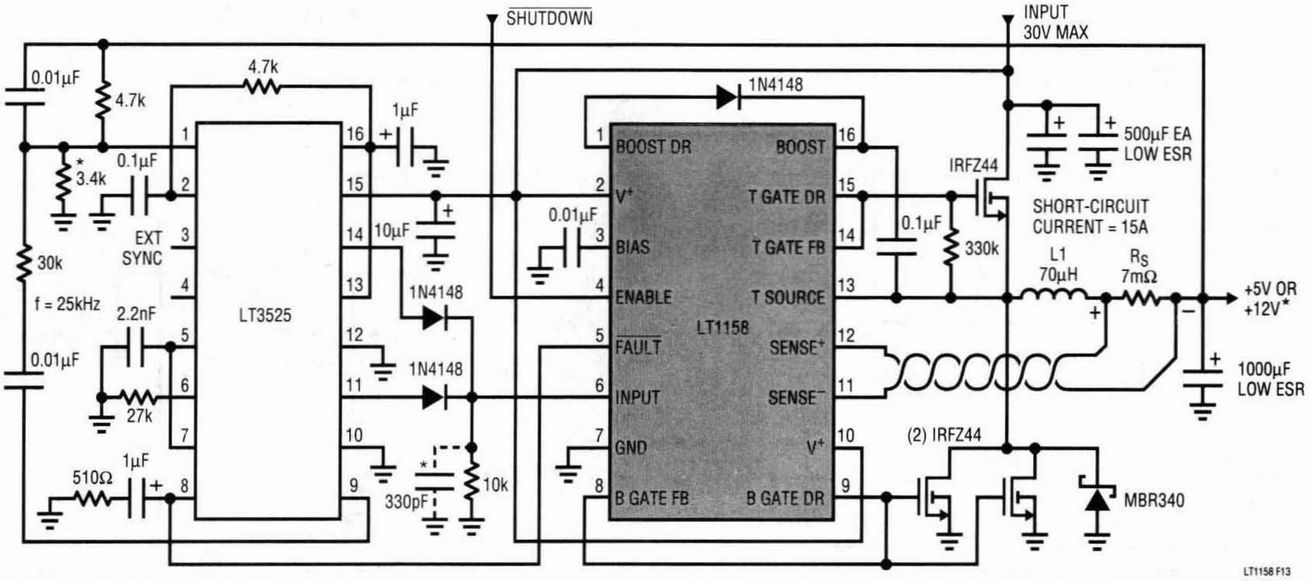
CONSTANT OFF TIME CURRENT MODE CONTROL LOOP

$$\text{FREQUENCY} = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \text{ WHERE } t_{OFF} \approx 10\mu s$$

SEE FIGURE 4 FOR EFFICIENCY CURVE

Figure 12. High Efficiency 5V Step-Down Switching Regulator (Requires No Heatsinks)

TYPICAL APPLICATIONS

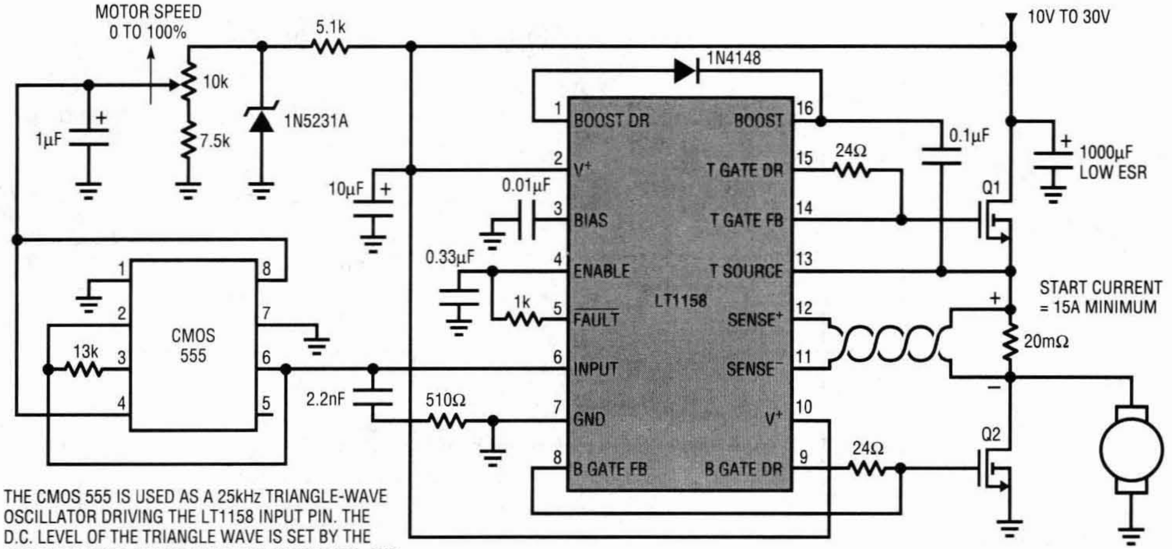

SHUTDOWN
INPUT
30V MAX
0.01µF
4.7k
4.7k
1µF
*
3.4k
0.1µF
EXT
SYNC
30k
f = 25kHz
2.2nF
0.01µF
27k
510Ω
1µF
LT3525
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
10µF
1N4148
1N4148
*
330pF
10k
1N4148
0.01µF
LT1158
BOOST DR
V⁺
BIAS
ENABLE
FAULT
INPUT
GND
B GATE FB
BOOST
T GATE DR
T GATE FB
T SOURCE
SENSE⁺
SENSE⁻
V⁺
B GATE DR
0.1µF
330k
IRFZ44
500µF EA
LOW ESR
SHORT-CIRCUIT
CURRENT = 15A
L1
70µH
RS
7mΩ
+5V OR
+12V*
1000µF
LOW ESR
(2) IRFZ44
MBR340
LT1158 F13

* ADD THESE COMPONENTS TO IMPLEMENT
LOW-DROPOUT 12V REGULATOR

L1: MAGNETICS CORE #55585-A2
30 TURNS 14GA MAGNET WIRE

R_S: DALE TYPE LVR-3
ULTRONIX RCS01

**Figure 13. 90% Efficiency 24V to 5V 10A Switching Regulator
95% Efficiency 24V to 12V 10A Low Dropout Switching Regulator**

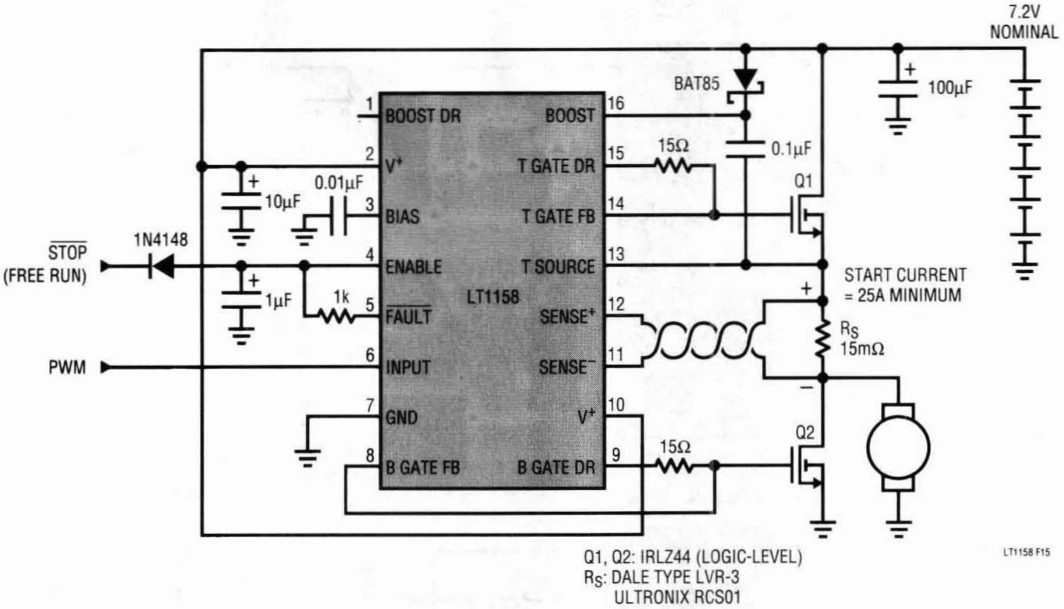

MOTOR SPEED
0 TO 100%
5.1k
10V TO 30V
1µF
10k
7.5k
1N5231A
1N4148
10µF
0.01µF
0.33µF
1k
LT1158
BOOST DR
V⁺
BIAS
ENABLE
FAULT
INPUT
GND
B GATE FB
BOOST
T GATE DR
T GATE FB
T SOURCE
SENSE⁺
SENSE⁻
V⁺
B GATE DR
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
24Ω
0.1µF
1000µF
LOW ESR
Q1
START CURRENT
= 15A MINIMUM
20mΩ
Q2
24Ω
CMOS
555
13k
2.2nF
510Ω
LT1158 F14

THE CMOS 555 IS USED AS A 25kHz TRIANGLE-WAVE OSCILLATOR DRIVING THE LT1158 INPUT PIN. THE D.C. LEVEL OF THE TRIANGLE WAVE IS SET BY THE POTENTIOMETER ON THE CMOS 555 SUPPLY PIN, AND ALLOW ADJUSTMENT OF THE LT1158 DUTY CYCLE FROM 0 TO 100%.

CMOS 555: LMC555 OR TLC555
Q1, Q2: MTP35N06E

Figure 14. Potentiometer-Adjusted Open Loop Motor Speed Control with Short-Circuit Protection

TYPICAL APPLICATIONS


7.2V
NOMINAL
BAT85
100μF
BOOST DR
BOOST
V+
T GATE DR
15Ω
0.1μF
Q1
10μF
0.01μF
BIAS
T GATE FB
STOP
(FREE RUN)
1N4148
ENABLE
T SOURCE
START CURRENT
= 25A MINIMUM
1μF
1k
FAULT
LT1158
SENSE+
RS
15mΩ
PWM
INPUT
SENSE–
GND
V+
Q2
B GATE FB
B GATE DR
15Ω
LT1158 F15

Q1, Q2: IRLZ44 (LOGIC-LEVEL)
RS: DALE TYPE LVR-3
ULTRONIX RCS01

Figure 15. High Efficiency 6-Cell NiCd Protected Motor Drive

4

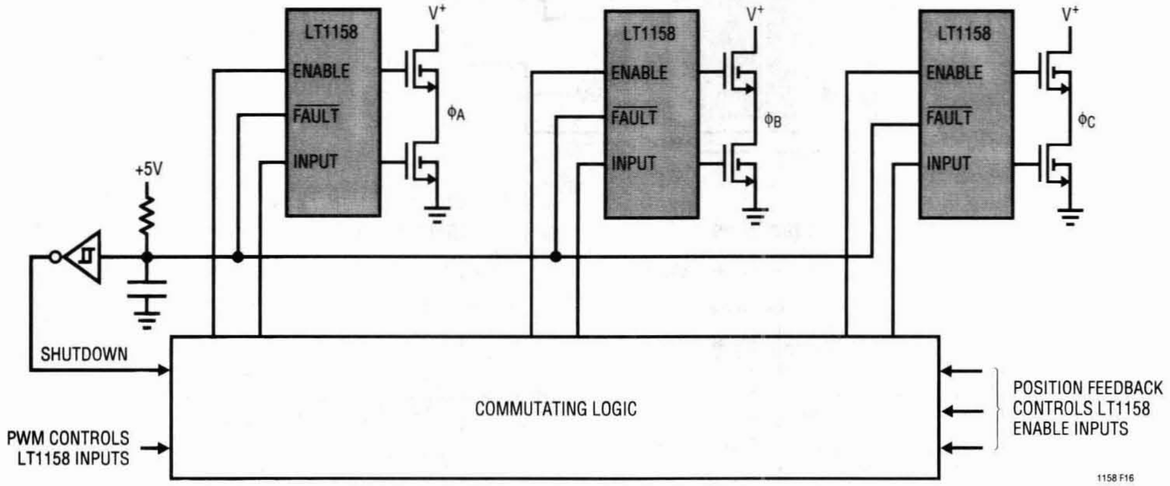
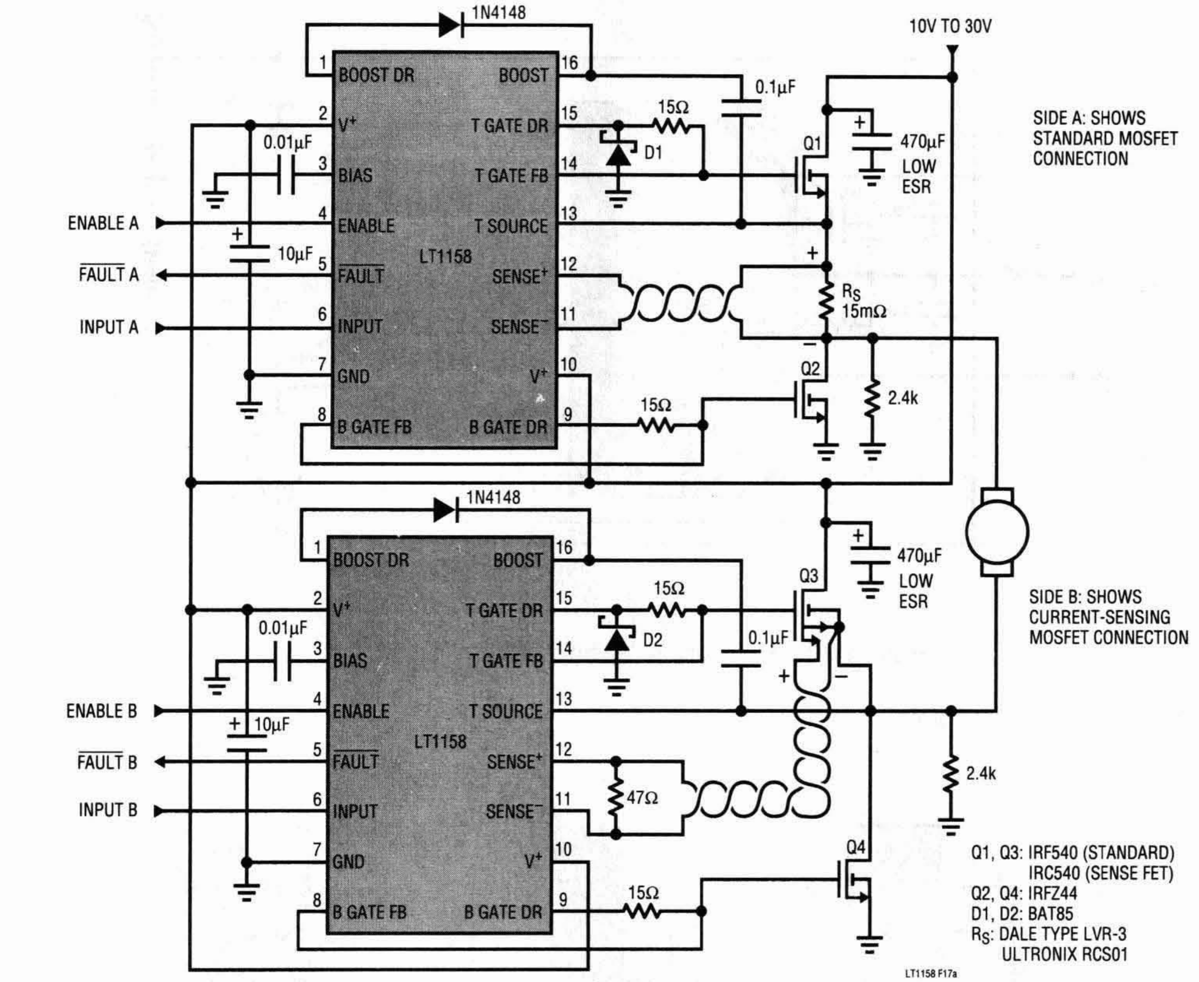
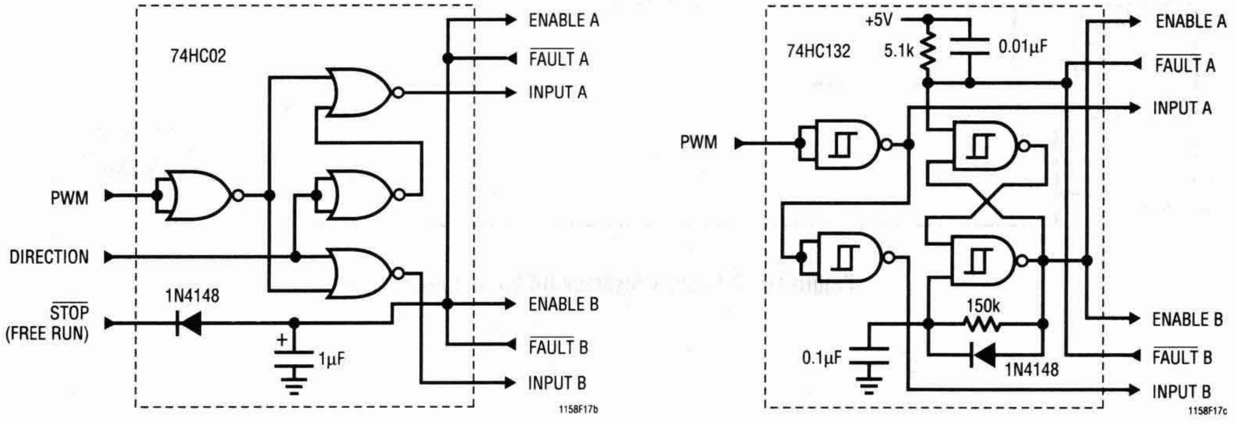

LT1158
ENABLE
FAULT
INPUT
V+
ϕA
ϕB
ϕC
+5V
SHUTDOWN
COMMUTATING LOGIC
PWM CONTROLS
LT1158 INPUTS
POSITION FEEDBACK
CONTROLS LT1158
ENABLE INPUTS
1158 F16

Figure 16. 3-Phase Brushless DC Motor Control

TYPICAL APPLICATIONS


1N4148
10V TO 30V
BOOST DR
BOOST
0.1µF
V+
T GATE DR
15Ω
0.01µF
D1
Q1
470µF LOW ESR
SIDE A: SHOWS STANDARD MOSFET CONNECTION
BIAS
T GATE FB
ENABLE A
ENABLE
T SOURCE
10µF
FAULT A
FAULT
LT1158
SENSE+
RS 15mΩ
INPUT A
INPUT
SENSE−
GND
V+
Q2
2.4k
B GATE FB
B GATE DR
15Ω
1N4148
BOOST DR
BOOST
470µF LOW ESR
Q3
SIDE B: SHOWS CURRENT-SENSING MOSFET CONNECTION
V+
T GATE DR
15Ω
0.01µF
D2
0.1µF
BIAS
T GATE FB
ENABLE B
ENABLE
T SOURCE
10µF
LT1158
FAULT B
FAULT
SENSE+
2.4k
47Ω
INPUT B
INPUT
SENSE−
GND
V+
Q4
B GATE FB
B GATE DR
15Ω
Q1, Q3: IRF540 (STANDARD)
IRC540 (SENSE FET)
Q2, Q4: IRFZ44
D1, D2: BAT85
RS: DALE TYPE LVR-3
ULTRONIX RCS01
LT1158 F17a


74HC02
PWM
DIRECTION
STOP (FREE RUN)
1N4148
1µF
ENABLE A
FAULT A
INPUT A
ENABLE B
FAULT B
INPUT B
1158F17b
+5V
74HC132
5.1k
0.01µF
PWM
150k
1N4148
0.1µF
ENABLE A
FAULT A
INPUT A
ENABLE B
FAULT B
INPUT B
1158F17c

Control Logic for Sign/Magnitude Drive

Control Logic for Locked Anti-Phase Drive
Motor stops if either side is shorted to ground

Figure 17. 10A Full Bridge Motor Control

TYPICAL APPLICATIONS

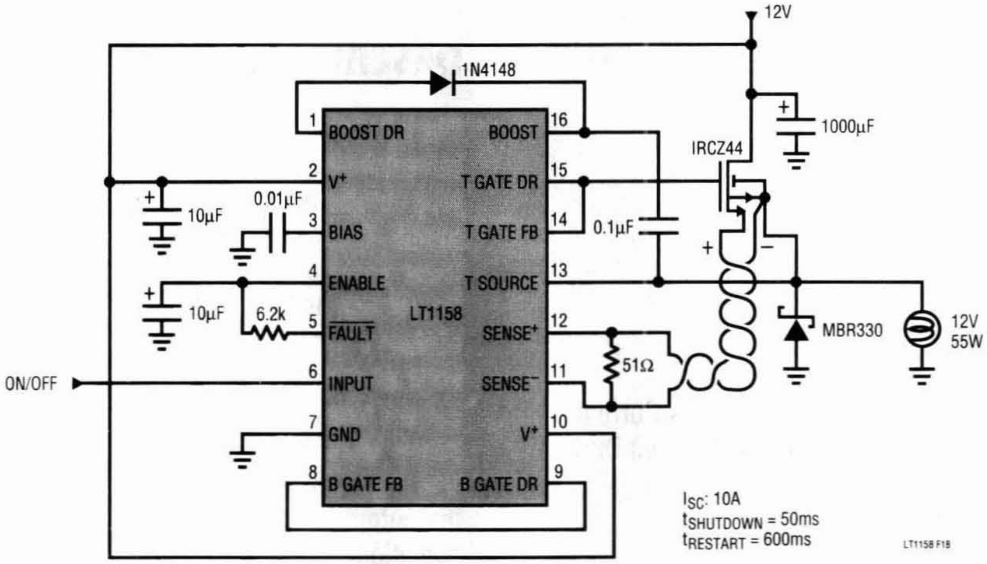

12V
1N4148
1
BOOST DR
BOOST
16
2
V+
T GATE DR
15
3
BIAS
T GATE FB
14
4
ENABLE
T SOURCE
13
5
FAULT
LT1158
SENSE+
12
6
INPUT
SENSE−
11
7
GND
V+
10
8
B GATE FB
B GATE DR
9
10µF
0.01µF
10µF
6.2k
ON/OFF
0.1µF
IRCZ44
1000µF
+
−
51Ω
MBR330
12V
55W
I_{SC}: 10A
$t_{SHUTDOWN}$ = 50ms
$t_{RESTART}$ = 600ms
LT1158 F18

Figure 18. High Current Lamp Driver with Short-Circuit Protection

LT1241 Series

High Speed Current Mode Pulse Width Modulators

FEATURES

- Low Start-Up Current (<250µA)
- 50ns Current Sense Delay
- Current Mode Operation to 500kHz
- Pin Compatible with UC1842 Series
- Under-Voltage Lockout with Hysteresis
- No Cross-Conduction Current
- Trimmed Bandgap Reference
- 1A Totem Pole Output
- Trimmed Oscillator Frequency and Sink Current
- Active Pull-Down on Reference and Output During Under-Voltage Lockout
- High Level Output Clamp (18V)
- Current Sense Leading Edge Blanking

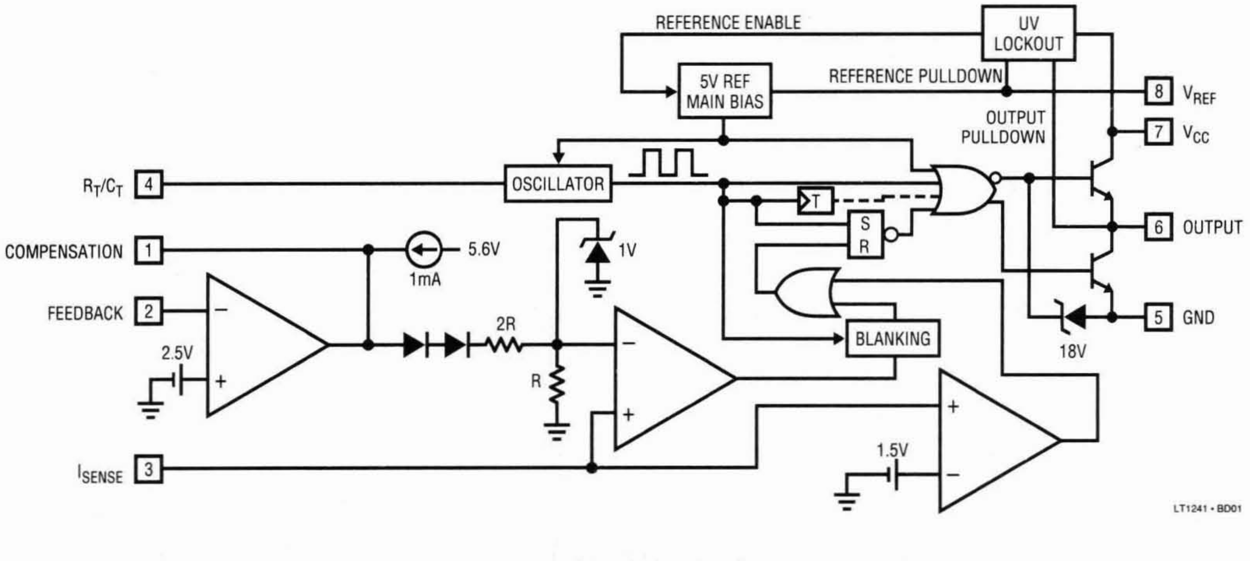
APPLICATIONS

- Off-Line Converters
- DC-DC Converters

DESCRIPTION

The LT1241 series devices are 8-pin, fixed frequency, current mode, pulse width modulators. They are improved plug compatible versions of the industry standard UC1842 series. These devices have both improved speed and lower quiescent current. The LT1241 series is optimized for off-line and DC-to-DC converter applications. They contain a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output stage ideally suited to driving power MOSFETs. Start-up current has been reduced to less than 250µA. Cross-conduction current spikes in the output stage have been eliminated, making 500kHz operation practical. Several new features have been incorporated. Leading edge blanking has been added to the current sense comparator. Trims have been added to the oscillator circuit for both frequency and sink current, and both of these parameters are tightly specified. The output stage is clamped to a maximum V_{OUT} of 18V in the on state. The output and the reference output are actively pulled low during under-voltage lockout.

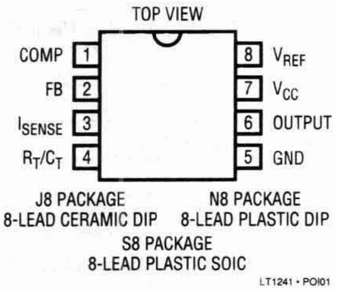
BLOCK DIAGRAM


REFERENCE ENABLE
UV LOCKOUT
5V REF MAIN BIAS
REFERENCE PULLDOWN
8 V_{REF}
7 V_{CC}
OUTPUT PULLDOWN
R_T/C_T 4
OSCILLATOR
T
S
R
6 OUTPUT
COMPENSATION 1
5.6V
1mA
1V
FEEDBACK 2
2.5V
2R
R
BLANKING
18V
5 GND
I_{SENSE} 3
1.5V
LT1241 • BD01

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+25V
Output Current	±1A*
Output Energy (Capacitive Load per Cycle)	5μJ
Analog Inputs (Pins 2, 3)	−0.3 to +6V
Error Amplifier Output Sink Current	10mA
Power Dissipation at $T_A \leq 25°C$	1W
Operating Junction Temperature Range	
LT124XC	0°C to +100°C
LT124XM	−55°C to +125°C
Thermal Resistance (Junction to Ambient)	
S8	150°C/W
J8	100°C/W
N8	130°C/W
Storage Temperature Range	− 65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT124XCJ8 LT124XMJ8 LT124XCN8 LT124XCS8
S8 PART MARKING
124X

*The 1A rating for output current is based on transient switching requirements.

ELECTRICAL CHARACTERISTICS (Notes 1, 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Section						
Output Voltage	I_O = 1mA, T_J = 25°C		4.925	5.000	5.075	V
Line Regulation	12V < V_{CC} < 25V	●		3	20	mV
Load Regulation	1mA < I_{VREF} < 20mA	●		−6	−25	mV
Temperature Stability				0.1		mV/°C
Total Output Variation	Line, Load, Temp	●	4.87		5.13	V
Output Noise Voltage	10Hz < F < 10kHz, T_J = 25°C			50		μV
Long Term Stability	T_A = 125°C, 1000 Hrs.			5	25	mV
Output Short Circuit Current		●	−30	−90	−180	mA
Oscillator Section						
Initial Accuracy	R_T = 10k, C_T = 3.3nF, T_J = 25°C		47.5	50	52.5	kHz
	R_T = 13.0k, C_T = 500pF, T_J = 25°C		228	248	268	kHz
Voltage Stability	12V < V_{CC} < 25V, T_J = 25°C				1	%
Temperature Stability	T_{MIN} < T_J < T_{MAX}			−0.05		%/°C
Amplitude	Pin 4, T_J = 25°C			1.7		V
Clock Ramp Reset Current	V_{OSC} (Pin 4) = 2V, T_J = 25°C		7.9	8.2	8.5	mA
Error Amplifier Section						
Feedback Pin Input Voltage	$V_{PIN\ 1}$ = 2.5V	●	2.42	2.50	2.58	V
Input Bias Current	V_{FB} = 2.5V	●			−2	μA
Open Loop Voltage Gain	2 < V_O < 4V	●	65	90		dB
Unity Gain Bandwidth	T_J = 25°C		0.7	1.3	2	MHz
Power Supply Rejection Ratio	12V < V_{CC} < 25V	●	60			dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	●	2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	●	−0.5	−0.75		mA

ELECTRICAL CHARACTERISTICS (Notes 1, 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier Section (cont'd)						
Output Voltage High Level	$V_{PIN\ 2}$ = 2.3V, R_L = 15k to GND	●	5	5.6		V
Output Voltage Low Level	$V_{PIN\ 2}$ = 2.7V, R_L = 15k to Pin 8	●		0.2	1.1	V
Current Sense Section						
Gain		●	2.85	3.00	3.15	V/V
Maximum Current Sense Input Threshold	$V_{PIN\ 3}$ < 1.1V	●	0.90	1.00	1.10	V
Power Supply Rejection Ratio		●		70		dB
Input Bias Current		●		−1	−10	µA
Delay to Output		●		50	100	ns
Blanking Time				100		ns
Blanking Override Voltage				1.5		V
Output Section						
Output Low Level	I_{OUT} = 20mA I_{OUT} = 200mA	● ●		0.25 0.75	0.4 2.2	V V
Output High Level	I_{OUT} = 20mA I_{OUT} = 200mA	● ●	12.0 11.75			V V
Rise Time	C_L = 1nF, T_J = 25°C			50	80	ns
Fall Time	C_L = 1.0nF, T_J = 25°C			30	60	ns
Output Clamp Voltage	I_O = 1mA	●		18	19	V
Under Voltage Lockout						
Start-Up Threshold LT1241 LT1242/LT1244 LT1243/LT1245		 ● ● ●	 9.0 15 7.8	 9.6 16 8.4	 10.2 17 9.0	 V V V
Minimum Operating Voltage LT1241/LT1243/LT1245 LT1242/LT1244		 ● ●	 7.0 9.0	 7.6 10	 8.2 11	 V V
Hysteresis LT1241 LT1242/LT1244 LT1243/LT1245			 1.6 5.5 0.4	 2.0 6.0 0.8		 V V V
PWM						
Maximum Duty Cycle LT1241/LT1244/LT1245 LT1242/LT1243	 T_J = 25°C T_J = 25°C		 46 94	 48 96		 % %
Minimum Duty Cycle		●		0		%
Total Device						
Start-Up Current		●		170	250	µA
Operating Current		●		7	10	mA

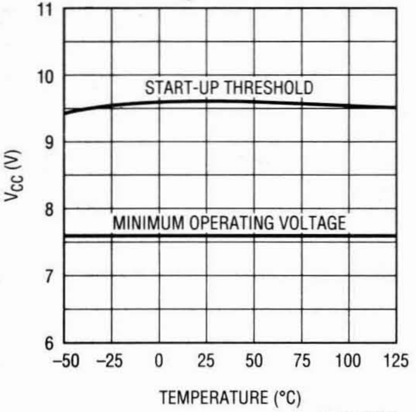
The ● denotes those specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, V_{CC} = 15V, R_T = 10k, C_T = 3.3nF.

Note 2: Low duty cycle pulse techniques are used during test to maintain junction temperature close to ambient.

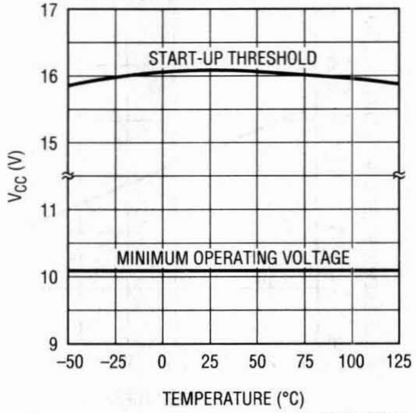
TYPICAL PERFORMANCE CHARACTERISTICS

Under-Voltage Lockout – LT1241



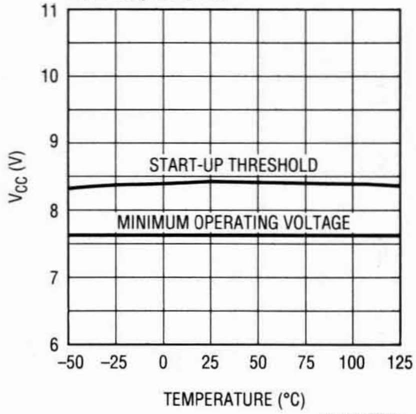
LT1241 • TPC01

Under-Voltage Lockout – LT1242, LT1244



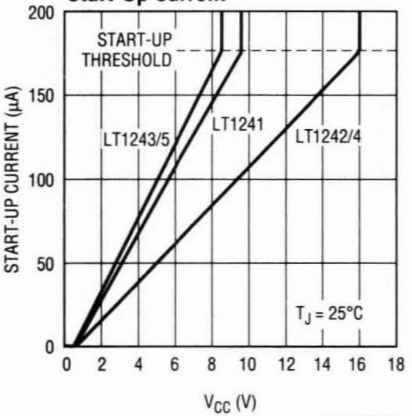
LT1241 • TPC02

Under-Voltage Lockout – LT1243, LT1245



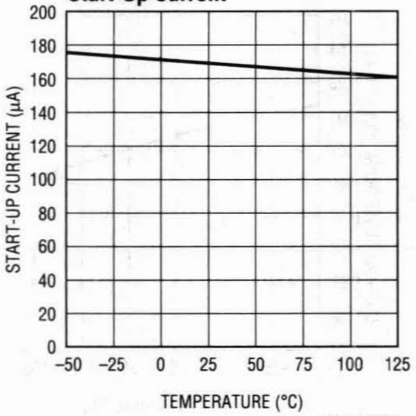
LT1241 • TPC03

Start-Up Current



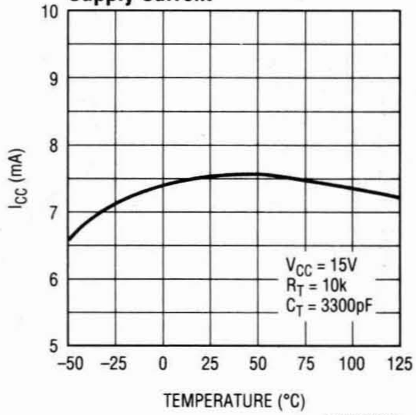
LT1241 • TPC04

Start-Up Current



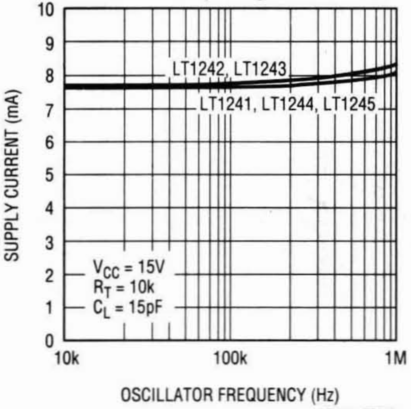
LT1241 • TPC05

Supply Current



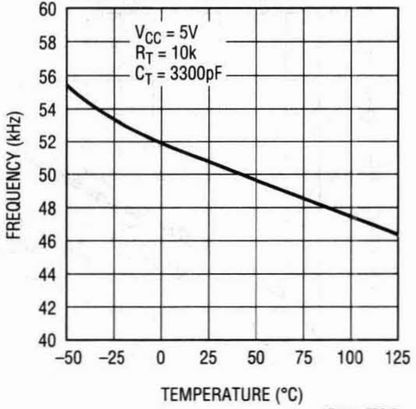
LT1241 • TPC06

Supply Current vs Oscillator Frequency



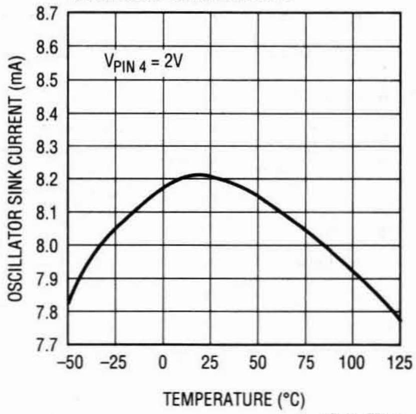
LT1241 • TPC18

Oscillator Frequency



LT1241 • TPC07

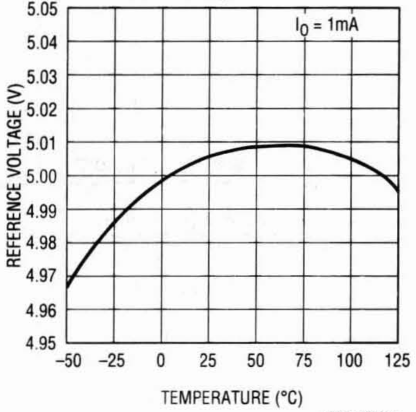
Oscillator Sink Current



LT1241 • TPC08

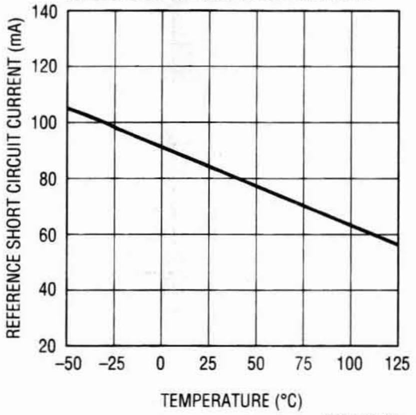
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Voltage



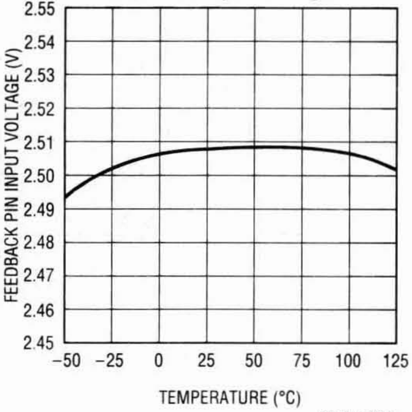
LT1241 • TPC10

Reference Short Circuit Current



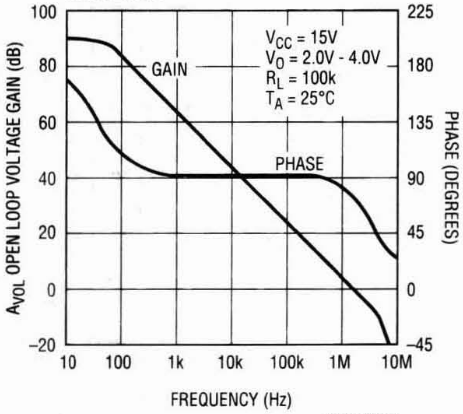
LT1241 • TPC09

Feedback Pin Input Voltage



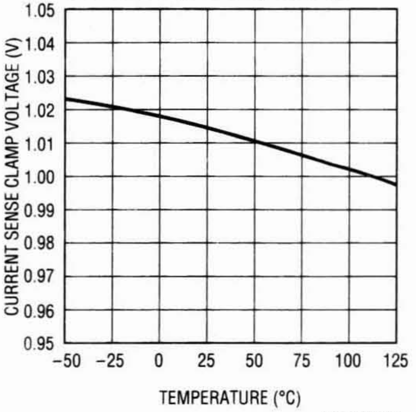
LT1241 • TPC11

Error Amplifier Open Loop Gain and Phase



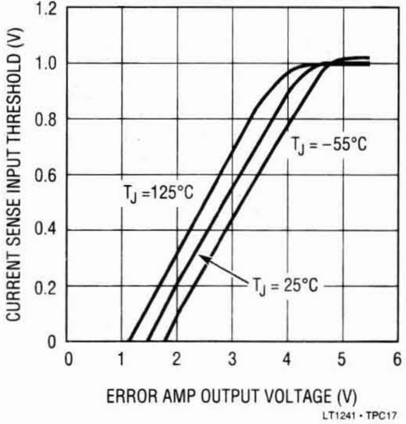
LT1241 • TPC16

Current Sense Clamp Voltage



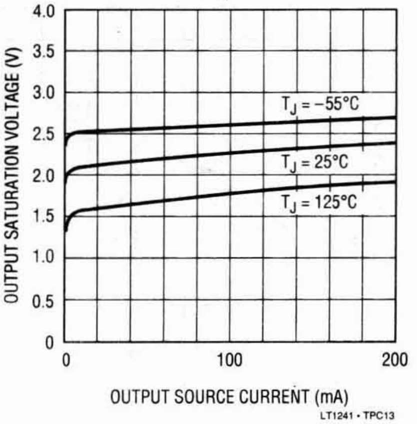
LT1241 • TPC12

Current Sense Input Threshold



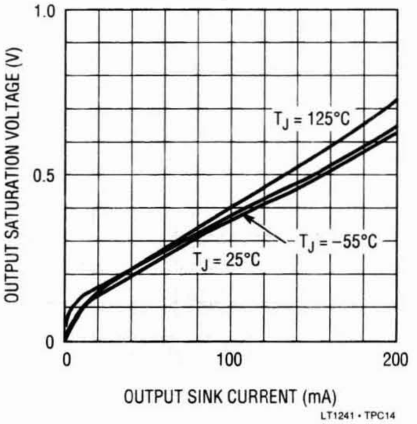
LT1241 • TPC17

High Level Output Saturation Voltage



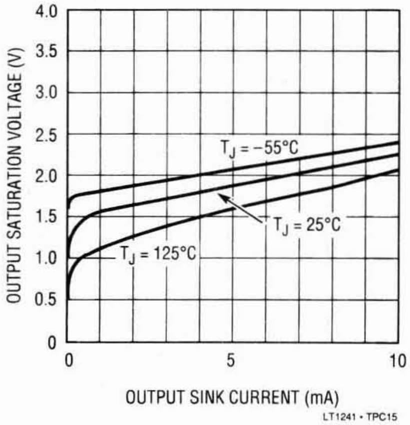
LT1241 • TPC13

Low Level Output Saturation Voltage



LT1241 • TPC14

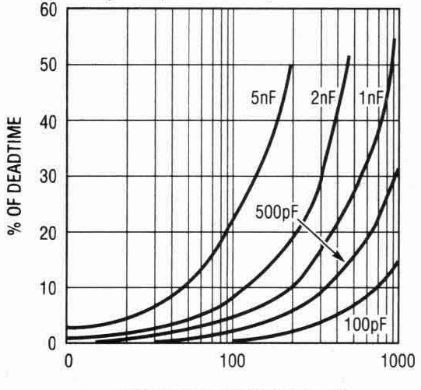
Low Level Output Saturation Voltage During Under-Voltage Lockout



LT1241 • TPC15

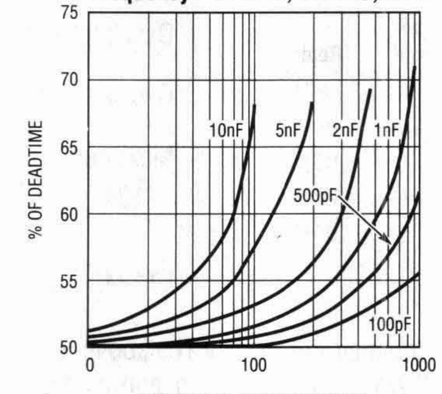
TYPICAL PERFORMANCE CHARACTERISTICS

Output Deadtime vs Oscillator Frequency – LT1242, LT1244



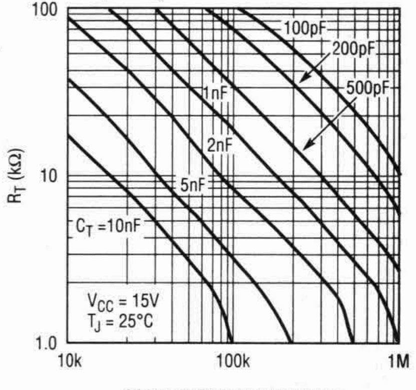
LT1241 • TPC19

Output Deadtime vs Oscillator Frequency – LT1241, LT1243,LT1245



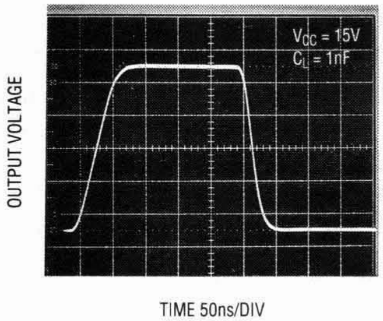
LT1241 • TPC20

Timing Resistor vs Oscillator Frequency



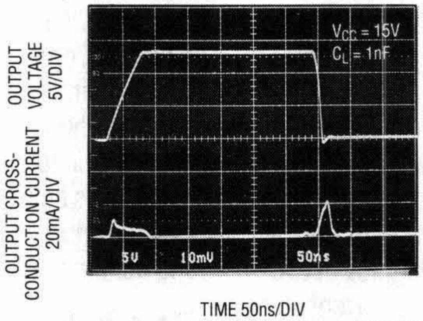
LT1241 • TPC21

Output Rise and Fall Time



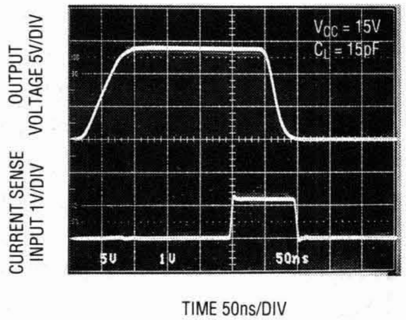
LT1241 • TPC22

Output Cross-Conduction Current



LT1241 • TPC23

Current Sense Delay



LT1241 • TPC24

PIN FUNCTIONS

Pin 1, Compensation: This pin is the output of the Error Amplifier and is made available for loop compensation. It can also be used to adjust the maximum value of the current sense clamp voltage to less than 1V. This pin can source a minimum of 0.5mA (0.8mA typ.) and sink a minimum of 2mA (4mA typ.)

Pin 2, Voltage Feedback: This pin is the inverting input of the Error Amplifier. The output voltage is normally fed back to this pin through a resistive divider. The non-inverting input of the Error Amplifier is internally committed to a 2.5V reference point.

Pin 3, Current Sense: This is the input to the current sense comparator. The trip point of the comparator is set by, and is proportional to, the output voltage of the Error Amplifier.

Pin 4, R_T/C_T: The oscillator frequency and the deadtime are set by connecting a resistor (R_T) from V_{REF} to R_T/C_T and a capacitor (C_T) from R_T/C_T to GND. The rise time of the oscillator waveform is set by the RC time constant of R_T and C_T. The fall time, which is equal to the output deadtime, is set by a combination of the RC time constant and the oscillator sink current (8.2mA typ.).

Pin 5, GND.

Pin 6, Output: This pin is the output of a high current totem pole output stage. It is capable of driving up to ±1A of current into a capacitive load such as the gate of a MOSFET.

Pin 7, V_{CC}: This pin is the positive supply of the control IC.

Pin 8, Reference: This is the reference output of the IC. The reference output is used to supply charging current to the external timing resistor R_T. The reference provides biasing to a large portion of the internal circuitry, and is used to generate several internal reference levels including the V_{FB} level and the current sense clamp voltage.

APPLICATIONS INFORMATION

Device	Start-Up Threshold	Minimum Operating Voltage	Maximum Duty Cycle	Replaces
LT1241	9.6V	7.6V	50%	NONE
LT1242	16V	10V	100%	UC1842
LT1243	8.4V	7.6V	100%	UC1843
LT1244	16V	10V	50%	UC1844
LT1245	8.4V	7.6V	50%	UC1845

Oscillator

The LT1241 series devices are fixed frequency current mode pulse width modulators. The oscillator frequency and the oscillator discharge current are both trimmed and tightly specified to minimize the variations in frequency and deadtime. The oscillator frequency is set by choosing a resistor and capacitor combination, R_T and C_T. This RC combination will determine both the frequency and the maximum duty cycle. The resistor R_T is connected from V_{REF} (pin 8) to the R_T/C_T pin (pin 4). The capacitor C_T is connected from the R_T/C_T pin to ground. The charging current for C_T is determined by the value of R_T. The discharge current for C_T is set by the difference between the current supplied by R_T and the discharge current of the LT124X. The discharge current of the device is trimmed to 8.2mA. For large values of R_T discharge time will be determined by the discharge current of the device and the value of C_T. As the value of R_T is reduced it will have more effect on the discharge time of C_T. During an oscillator cycle capacitor C_T is charged to approximately 2.8V and discharged to approximately 1.1V. The output is enabled during the charge time of C_T and disabled, in an off state, during the discharge time of C_T. The deadtime of the circuit is equal to the discharge time of C_T. The maximum duty cycle is limited by controlling the deadtime of the oscillator. There are many combinations of R_T and C_T that will yield a given oscillator frequency, however there is only one combination that will yield a specific deadtime at that frequency. Curves of oscillator frequency and deadtime for various values of R_T and C_T appear in the Typical Performance Characteristics section. Frequency and deadtime can also be calculated using the following formulas:

Oscillator Rise Time: $t_r = 0.583 \bullet RC$

Oscillator Discharge Time: $t_d = \dfrac{3.46 \bullet RC}{(0.0164)R - 11.73}$

Oscillator Period: $T_{OSC} = t_r + t_d$

Oscillator Frequency: $f_{OSC} = \dfrac{1}{T_{OSC}}$

Maximum Duty Cycle:

LT1241, LT1244, LT1245 $D_{MAX} = \dfrac{t_r}{2\,T_{OSC}} = \dfrac{T_{OSC} - t_d}{2\,T_{OSC}}$

LT1242, LT1243 $D_{MAX} = \dfrac{t_r}{T_{OSC}} = \dfrac{T_{OSC} - t_d}{T_{OSC}}$

The above formulas will give values that will be accurate to approximately ±5%, at the oscillator, over the full operating frequency range. This is due to the fact that the oscillator trip levels are constant versus frequency and the discharge current and initial oscillator frequency are trimmed. Some fine adjustment may be required to achieve more accurate results. Once the final R_T/C_T combination is selected the oscillator characteristics will be repeatable from device to device. Note that there will be some slight differences between maximum duty cycle at the oscillator and maximum duty cycle at the output due to the finite rise and fall times of the output.

The output switching frequency will be equal to the oscillator frequency for LT1242 and LT1243. The output switching frequency will be equal to one half the oscillator frequency for LT1241, LT1244, and LT1245. The oscillator of LT1241 series devices will run at frequencies up to 1MHz, allowing 500kHz output switching frequencies for all devices.

Error Amplifier

The LT1241 series of devices contain a fully compensated error amplifier with a DC gain of 90dB and a unity gain frequency of 1MHz. Phase margin at unity gain is 80°. The non-inverting input is internally committed to a 2.5V reference point derived from the 5V reference of pin 8. The inverting input (pin 2) and the output (pin 1) are made available to the user. The output voltage in a regulator circuit is normally fed back to the inverting input of the error amplifier through a resistive divider.

The output of the error amplifier is made available for external loop compensation. The output current of the error amplifier is limited to approximately 0.8mA sourcing

APPLICATIONS INFORMATION

and approximately 6mA sinking. In a current mode PWM the peak switch current is a function of the output voltage of the error amplifier. In the LT1241 series devices the output of the error amplifier is offset by two diodes (1.4V at 25°C), divided by a factor of three, and fed to the inverting input of the current sense comparator. For error amplifier output voltages less than 1.4V the duty cycle of the output stage will be zero. The maximum offset that can appear at the current sense input is limited by a 1V clamp. This occurs when the error amplifier output reaches 4.4V at 25°C.

The output of the error amplifier can be clamped below 4.4V in order to reduce the maximum voltage allowed across the current sensing resistor to less than 1V. The supply current will increase by the value of the output source current when the output voltage of the error amplifier is clamped.

Current Sense Comparator and PWM Latch

LT1241 series devices are current mode controllers. Under normal operating conditions the output (pin 6) is turned on at the start of every oscillator cycle, coincident with the rising edge of the oscillator waveform. The output is then turned off when the current reaches a threshold level proportional to the error voltage at the output of the error amplifier. Once the output is turned off it is latched off until the start of the next cycle. The peak current is thus proportional to the error voltage and is controlled on a cycle by cycle basis. The peak switch current is normally sensed by placing a sense resistor in the source lead of the output MOSFET. This resistor converts the switch current to a voltage that can be fed into the current sense input. For normal operating conditions the peak inductor current, which is equal to the peak switch current will be equal to:

$$I_{PK} = \frac{\left(V_{PIN\,1} - 1.4V\right)}{\left(3R_S\right)}$$

During fault conditions the maximum threshold voltage at the input of the current sense comparator is limited by the internal 1V clamp at the inverting input. The peak switch current will be equal to:

$$I_{PK(MAX)} = \frac{1.0V}{R_S}$$

In certain applications, such as high power regulators, it may be desirable to limit the maximum threshold voltage to less than 1V in order to limit the power dissipated in the sense resistor or to limit the short circuit current of the regulator circuit. This can be accomplished by clamping the output of the error amplifier. A voltage level of approximately 1.4V at the output of the error amplifier will give a threshold voltage of 0V. A voltage level of approximately 4.4V at the output of the error amplifier will give a threshold level of 1V. Between 1.4V and 4.4V the threshold voltage will change by a factor of one third of the change in the error amplifier output voltage. The threshold voltage will be 0.333V for an error amplifier voltage of 2.4V. To reduce the maximum current sense threshold to less than 1V the error amplifier output should be clamped to less than 4.4V.

Blanking

A unique feature of the LT1241 series devices is the built in blanking circuit at the output of the current sense comparator. A common problem with current mode PWM circuits is erratic operation due to noise at the current sense input. The primary cause of noise problems is the leading edge current spike due to transformer interwinding capacitance and diode reverse recovery time. This current spike can prematurely trip the current sense comparator causing an instability in the regulator circuit. A filter at the current sense input is normally required to eliminate this instability.

This filter will in turn slow down the current sense loop. A slow current sense loop will increase the minimum pulse width which will increase the short circuit current in an overload condition. The LT1241 series devices blank (lock out) the signal at the output of the current sense comparator for a fixed amount of time after the switch is turned on. This effectively prevents the PWM latch from tripping due to the leading edge current spike.

The blanking time will be a function of the voltage at the feedback pin (pin 2). The blanking time will be 100ns for normal operating conditions (V_{FB} = 2.5V). The blanking time goes to zero as the feedback pin is pulled to 0V. This means that the blanking time will be minimized during start-up and also during an output short circuit fault. This

APPLICATIONS INFORMATION

blanking circuit eliminates the need for an input filter at the current sense input except in extreme cases. Eliminating the filter allows the current sense loop to operate with minimum delays, reducing peak currents during fault conditions.

Under-Voltage Lockout

The LT1241 series devices incorporate an under-voltage lockout comparator which prevents the internal reference circuitry and the output from starting up until the supply voltage reaches the start-up threshold voltage. The quiescent current, below the start-up threshold, has been reduced to less than 250µA (170µA typ.) to minimize the power loss due to the bleed resistor used for start-up in off line converters. In under-voltage lockout both V_{REF} (pin 8) and the output (pin 6) are actively pulled low by Darlington connected PNP transistors. They are designed to sink a few milliamps of current and will pull down to about 1V. The pull-down transistor at the reference pin can be used to reset the external soft start capacitor. The pull-down transistor at the output eliminates the external pull-down resistor required, with earlier devices, to hold the external MOSFET gate low during under-voltage lockout.

Output

The LT1241 series devices incorporate a single high current totem pole output stage. This output stage is capable of driving up to ±1A of output current. Cross-conduction current spikes in the output totem pole have been eliminated. This device is primarily intended for driving MOSFET switches. Rise time is typically 40ns and fall time is typically 30ns when driving a 1.0nF load. A clamp is built into the device to prevent the output from rising above 18V in order to protect the gate of the MOSFET switch.

The output is actively pulled low during under-voltage lockout by a Darlington PNP. This PNP is designed to sink several milliamps and will pull the output down to approximately 1V. This active pull-down eliminates the need for an external resistor which was required in older designs. The output pin of the device connects directly to the emitter of the upper NPN drive transistor and the collector of the lower NPN drive transistor in the totem pole. The collector of the lower transistor, which is n-type silicon, forms a p-n junction with the substrate of the device. This junction is reverse biased during normal operation.

In some applications the parasitic LC of the external MOSFET gate can ring and pull the output pin below ground. If the output pin is pulled negative by more than a diode drop the parasitic diode formed by the collector of the output NPN and the substrate will turn on. This can cause erratic operation of the device. In these cases a Schottky clamp diode is recommended from the output to ground.

Reference

The internal reference of the LT1241 series devices is a 5V Bandgap reference, trimmed to within ±1% initial tolerance. The reference is used to power the majority of internal logic and the oscillator circuitry. The oscillator charging current is supplied from the reference. The feedback pin voltage and the clamp level for the current sense comparator are derived from the reference voltage. The reference can supply up to 20mA of current to power external circuitry. Note that using the reference in this manner, as a voltage regulator, will significantly increase power dissipation in the device which will reduce the useful operating ambient temperature range.

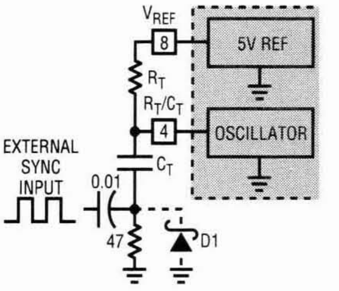
Design/Layout Considerations

LT1241 series devices are high speed circuits capable of generating pulsed output drive currents of up to 1A peak. The rise and fall time for the output drive current is in the range of 10ns to 20ns. High speed circuit techniques must be used to insure proper operation of the device. **Do not attempt to use Proto-boards or wire-wrap techniques to breadboard high speed switching regulator circuits. They will not work properly.**

Printed circuit layouts should include separate ground paths for the voltage feedback network, oscillator capacitor, and switch drive current. These ground paths should be connected together directly at the ground pin (pin 5) of the LT124X. This will minimize noise problems due to pulsed ground pin currents. V_{CC} should be bypassed, with a minimum of 0.1µF, as close to the device as possible. High current paths should be kept short and they should be separated from the feedback voltage network with shield traces if possible.

TYPICAL APPLICATIONS

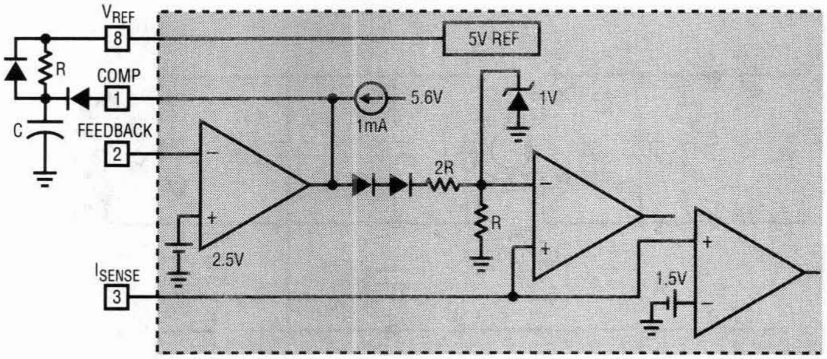
External Clock Synchronization


V_{REF}
8
5V REF
R_T
R_T/C_T
4
OSCILLATOR
EXTERNAL SYNC INPUT
0.01
C_T
47
D1

D1 IS REQUIRED IF THE SYNC AMPLITUDE IS LARGE ENOUGH TO PULL THE BOTTOM OF C_T MORE THAN 300mV BELOW GROUND.

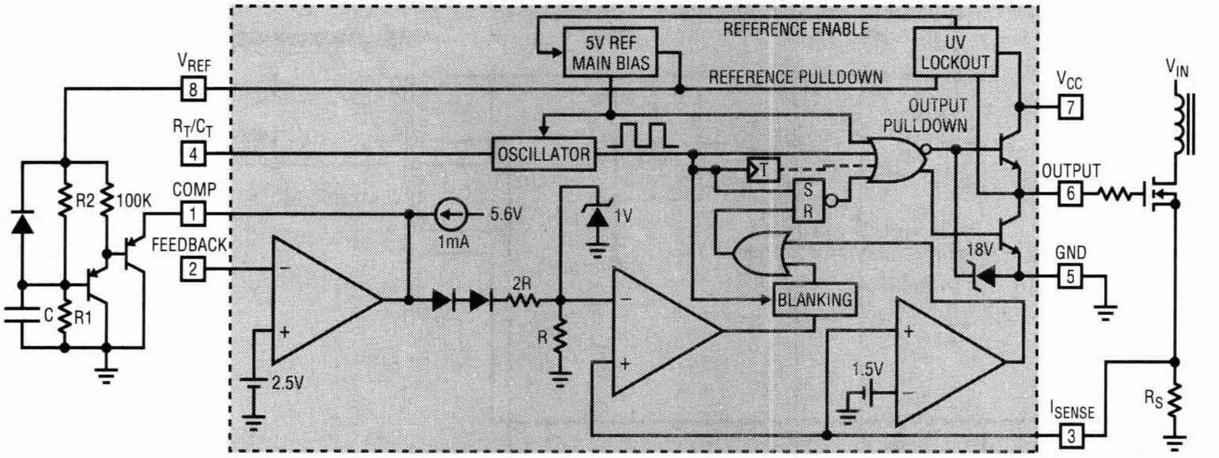
LT1241 • TA01

Soft Start


V_{REF}
8
5V REF
R
COMP
1
5.6V
1mA
1V
C
FEEDBACK
2
2R
R
2.5V
I_{SENSE}
3
1.5V

LT1241 • TA02

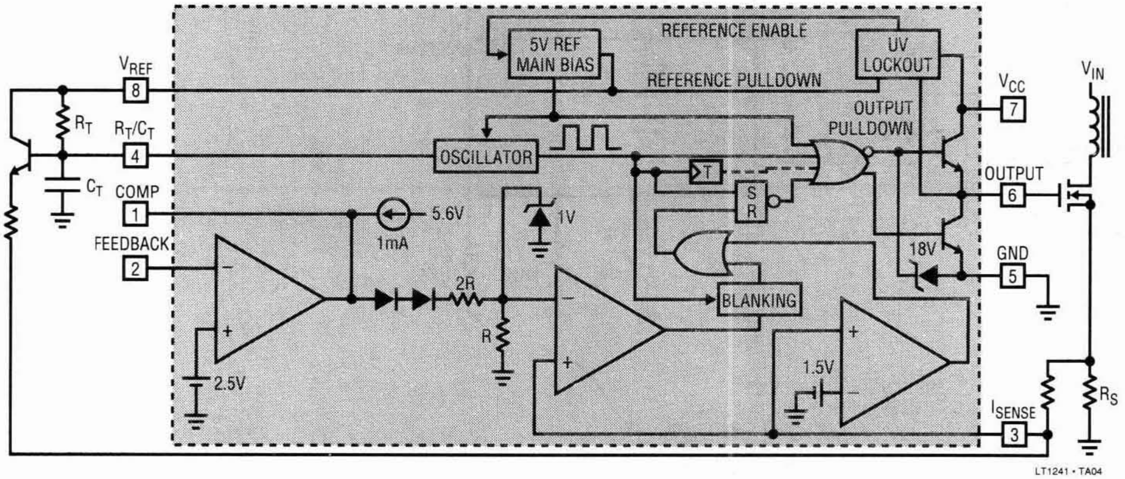
Adjustable Clamp Level with Soft Start


REFERENCE ENABLE
5V REF MAIN BIAS
UV LOCKOUT
V_{REF}
8
REFERENCE PULLDOWN
V_{IN}
V_{CC}
7
R_T/C_T
4
OUTPUT PULLDOWN
OSCILLATOR
T
OUTPUT
6
COMP
1
R2
100K
S
R
5.6V
1mA
1V
18V
FEEDBACK
2
GND
5
BLANKING
2R
C
R1
R
1.5V
2.5V
R_S
I_{SENSE}
3

$V_{CLAMP} \approx \dfrac{1.67}{\left(\dfrac{R2}{R1}+1\right)}$ $\quad I_{PK\,(MAX)} \approx \dfrac{V_{CLAMP}}{R_S}$ $\quad$ WHERE: $0 \le V_{CLAMP} \le 1.0V$ $\quad t_{SOFT\ START} = -\ln\left[1-\dfrac{V_C}{3 \cdot V_{CLAMP}}\right] C\,\dfrac{R1\,R2}{R1+R2}$

LT1241 • TA03

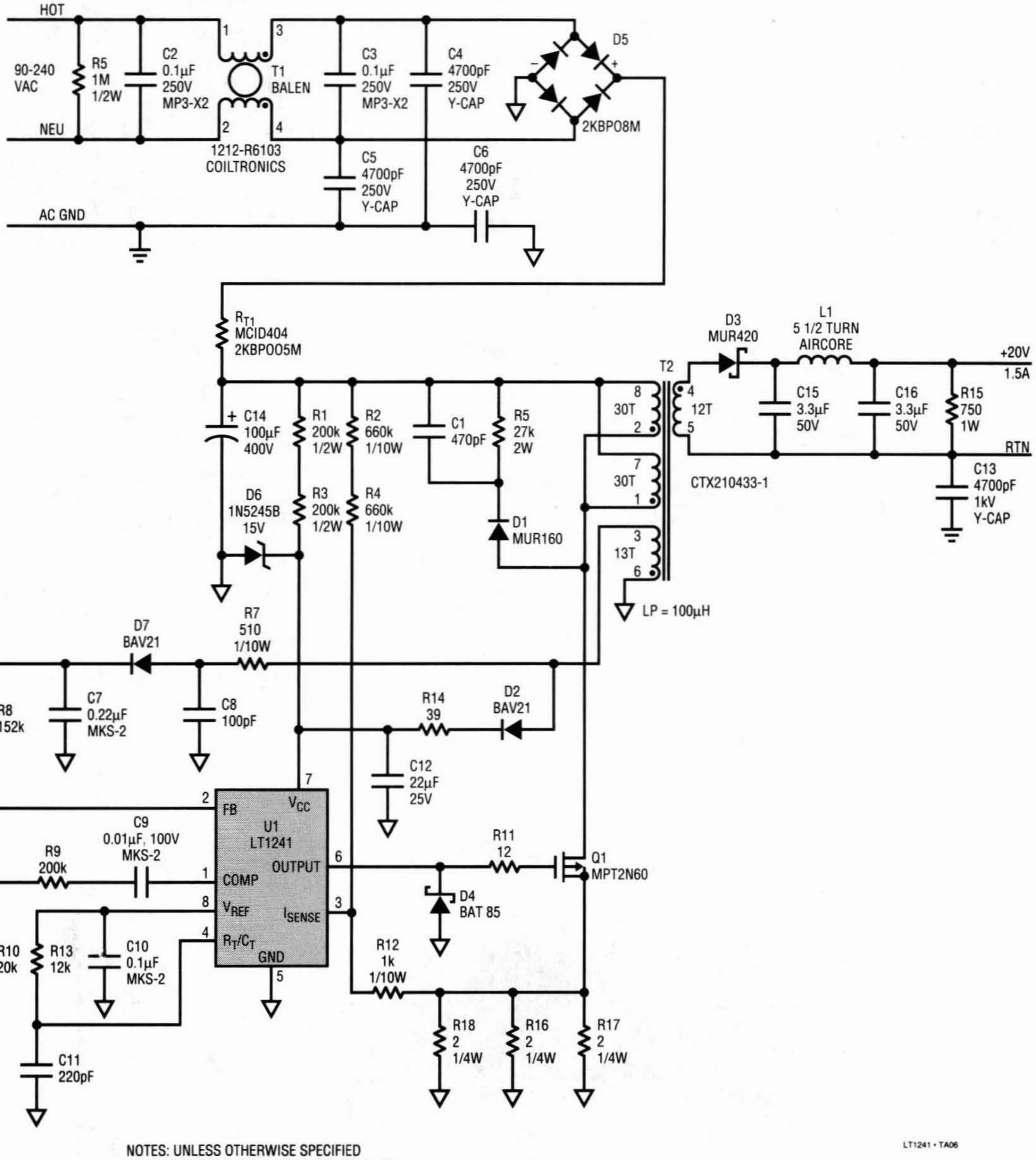
Slope Compensation at I_{SENSE} Pin


REFERENCE ENABLE
5V REF MAIN BIAS
UV LOCKOUT
V_{REF}
8
REFERENCE PULLDOWN
V_{CC}
7
V_{IN}
R_T
R_T/C_T
OUTPUT PULLDOWN
4
OSCILLATOR
T
C_T
COMP
1
S
R
OUTPUT
6
5.6V
1mA
1V
FEEDBACK
2
18V
GND
5
BLANKING
2R
R
1.5V
2.5V
I_{SENSE}
3
R_S

LT1241 • TA04

TYPICAL APPLICATIONS

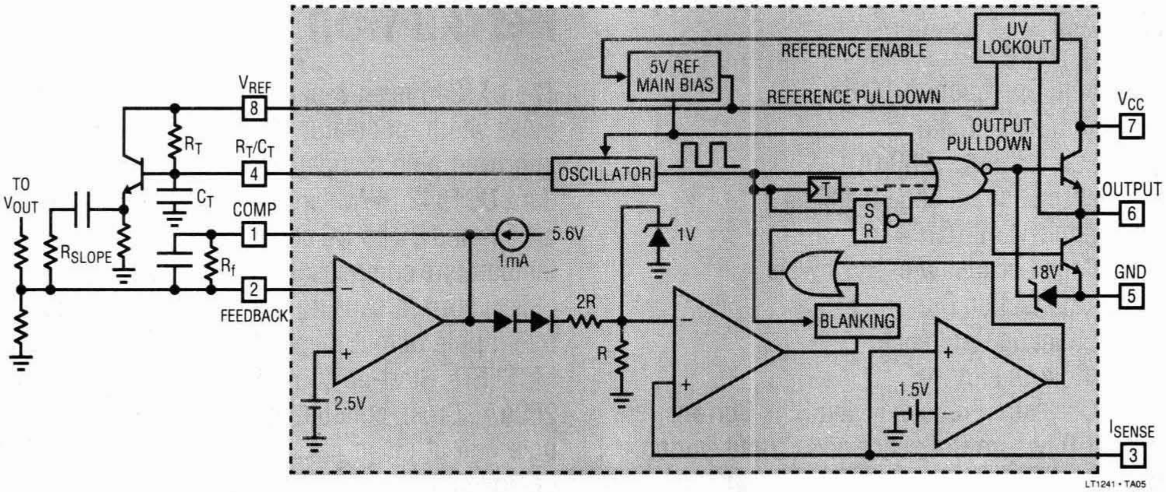
300kHz Off-Line Power Supply


HOT
90-240 VAC
NEU
AC GND
R5 1M 1/2W
C2 0.1μF 250V MP3-X2
1 3 2 4
T1 BALEN
1212-R6103 COILTRONICS
C3 0.1μF 250V MP3-X2
C4 4700pF 250V Y-CAP
C5 4700pF 250V Y-CAP
C6 4700pF 250V Y-CAP
D5
2KBPO8M
R_{T1} MCID404 2KBPOO5M
C14 100μF 400V
R1 200k 1/2W
R2 660k 1/10W
C1 470pF
R5 27k 2W
R3 200k 1/2W
R4 660k 1/10W
D6 1N5245B 15V
D1 MUR160
T2
8 30T 2
7 30T 1
3 13T 6
4 12T 5
CTX210433-1
LP = 100μH
D3 MUR420
L1 5 1/2 TURN AIRCORE
C15 3.3μF 50V
C16 3.3μF 50V
R15 750 1W
+20V 1.5A
RTN
C13 4700pF 1kV Y-CAP
D7 BAV21
R7 510 1/10W
R8 152k
C7 0.22μF MKS-2
C8 100pF
R14 39
D2 BAV21
C12 22μF 25V
U1 LT1241
2 FB
7 V_{CC}
1 COMP
6 OUTPUT
8 V_{REF}
3 I_{SENSE}
4 R_T/C_T
5 GND
C9 0.01μF, 100V MKS-2
R9 200k
R11 12
Q1 MPT2N60
D4 BAT 85
R10 20k
R13 12k
C10 0.1μF MKS-2
R12 1k 1/10W
R18 2 1/4W
R16 2 1/4W
R17 2 1/4W
C11 220pF
LT1241 • TA06

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITANCES ARE IN MICRO-FARADS, 50V, 10%.

TYPICAL APPLICATIONS

Slope Compensation at Error Amp


REFERENCE ENABLE
UV LOCKOUT
5V REF MAIN BIAS
REFERENCE PULLDOWN
VREF
8
RT
RT/CT
4
OSCILLATOR
OUTPUT PULLDOWN
VCC
7
TO VOUT
CT
COMP
1
T
S
R
OUTPUT
6
RSLOPE
Rf
5.6V
1mA
1V
18V
GND
5
2
FEEDBACK
2R
BLANKING
R
2.5V
1.5V
ISENSE
3
LT1241 • TA05

LT1246

1MHz Off-Line Current Mode PWM

FEATURES

- Current Mode Operation to 1MHz
- 30ns Current Sense Delay
- Low Start-Up Current (<250μA)
- Current Sense Leading Edge Blanking
- Pin Compatible with UC1842
- Under-Voltage Lockout with Hysteresis
- No Cross-Conduction Current
- Trimmed Bandgap Reference
- 1A Totem Pole Output
- Trimmed Oscillator Frequency and Sink Current
- Active Pull-Down on Reference and Output During Under-Voltage Lockout
- High Level Output Clamp (18V)

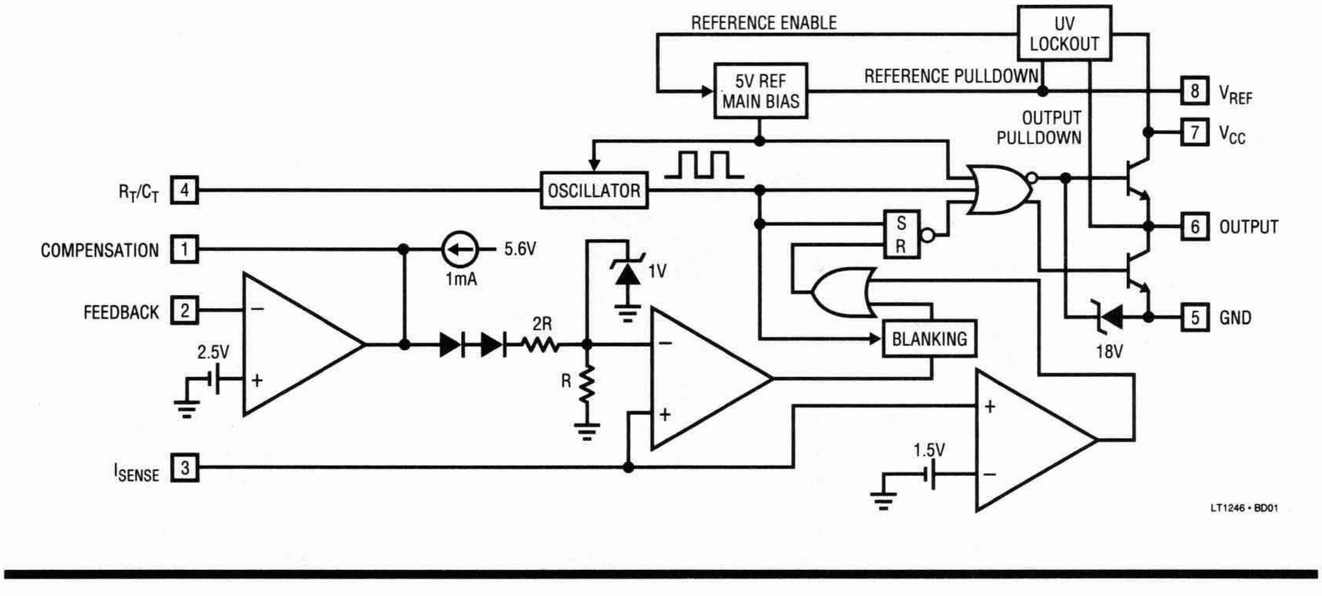
APPLICATIONS

- Off-Line Converters
- DC-DC Converters

DESCRIPTION

The LT1246 is an 8-pin, fixed frequency, current mode, pulse width modulator. The device is designed to be an improved plug compatible version of the industry standard UC1842 PWM circuit. The LT1246 is optimized for off-line and DC-to-DC converter applications. It contains a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output stage ideally suited to driving power MOSFETs. Start-up current has been reduced to less than 250μA. Cross-conduction current spikes in the totem pole output stage have been eliminated, making 1MHz operation practical. Several new features have been incorporated. Leading edge blanking has been added to the current sense comparator. This minimizes or eliminates the filter that is normally required. Eliminating this filter allows the current sense loop to operate with minimum delays. Trims have been added to the oscillator circuit for both frequency and sink current, and both of these parameters are tightly specified. The output stage is clamped to a maximum V_{OUT} of 18V in the on state. The output and the reference output are actively pulled low during under-voltage lockout.

BLOCK DIAGRAM

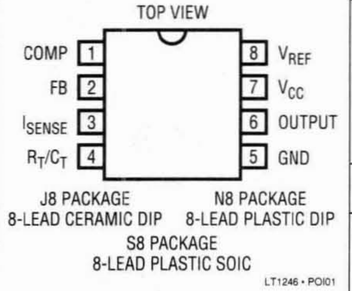


REFERENCE ENABLE
UV LOCKOUT
5V REF MAIN BIAS
REFERENCE PULLDOWN
8 V_REF
7 V_CC
OUTPUT PULLDOWN
R_T/C_T 4
OSCILLATOR
S
R
6 OUTPUT
COMPENSATION 1
5.6V
1mA
1V
FEEDBACK 2
2R
5 GND
18V
BLANKING
2.5V
R
1.5V
I_SENSE 3
LT1246 • BD01

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+25V
Output Current	±1A*
Output Energy (Capacitive Load per Cycle)	5µJ
Analog Inputs (Pins 2, 3)	−0.3 to +6V
Error Amplifier Output Sink Current	10mA
Power Dissipation at $T_A \le 25°C$	1W
Operating Junction Temperature Range	
LT1246C	0°C to +100°C
LT1246M	−55°C to +125°C
Thermal Resistance (Junction to Ambient)	
S8	150°C/W
J8	100°C/W
N8	130°C/W
Storage Temperature Range	− 65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1246CJ8 LT1246MJ8 LT1246CN8 LT1246CS8
S8 PART MARKING
1246

*The 1A rating for output current is based on transient switching requirements.

ELECTRICAL CHARACTERISTICS (Notes 1, 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Section						
Output Voltage	$I_O = 1mA$, $T_J = 25°C$		4.925	5.000	5.075	V
Line Regulation	$12V < V_{CC} < 25V$	●		3	20	mV
Load Regulation	$1mA < I_{REF} < 20mA$	●		−6	−25	mV
Temperature Stability				0.1		mV/°C
Total Output Variation	Line, Load, Temp	●	4.87		5.13	V
Output Noise Voltage	$10Hz < F < 10kHz$, $T_J = 25°C$			50		µV
Long Term Stability	$T_A = 125°C$, 1000 Hrs.			5	25	mV
Output Short Circuit Current		●	−30	−90	−180	mA
Oscillator Section						
Initial Accuracy	$R_T = 10k$, $C_T = 3.3nF$, $T_J = 25°C$		47.5	50	52.5	kHz
	$R_T = 6.2k$, $C_T = 500pF$, $T_J = 25°C$		465	500	535	kHz
Voltage Stability	$12V < V_{CC} < 25V$, $T_J = 25°C$				1	%
Temperature Stability	$T_{MIN} < T_J < T_{MAX}$			−0.05		%/°C
Amplitude	Pin 4			1.7		V
Clock Ramp Reset Current	V_{OSC} (Pin 4) = 2V, $T_J = 25°C$		7.9	8.2	8.5	mA
Error Amplifier Section						
Feedback Pin Input Voltage	$V_{PIN\ 1} = 2.5V$	●	2.42	2.50	2.58	V
Input Bias Current	$V_{FB} = 2.5V$	●			−2	µA
Open Loop Voltage Gain	$2 < V_O < 4V$	●	65	90		dB
Unity Gain Bandwidth	$T_J = 25°C$		1	2		MHz
Power Supply Rejection Ratio	$12V < V_{CC} < 25V$	●	60			dB
Output Sink Current	$V_{PIN\ 2} = 2.7V$, $V_{PIN\ 1} = 1.1V$	●	2	6		mA
Output Source Current	$V_{PIN\ 2} = 2.3V$, $V_{PIN\ 1} = 5V$	●	−0.5	−0.75		mA

ELECTRICAL CHARACTERISTICS (Notes 1, 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier Section (cont'd)						
Output Voltage High Level	$V_{PIN\ 2} = 2.3V$, $R_L = 15k$ to GND	●	5	5.6		V
Output Voltage Low Level	$V_{PIN\ 2} = 2.7V$, $R_L = 15k$ to Pin 8	●		0.2	1.1	V
Current Sense Section						
Gain		●	2.85	3.00	3.15	V/V
Maximum Current Sense Input Threshold	$V_{PIN\ 3} < 1.1V$	●	0.90	1.00	1.10	V
Power Supply Rejection Ratio				70		dB
Input Bias Current		●		−1	−10	μA
Delay to Output				30		ns
Blanking Time				60		ns
Blanking Override Voltage				1.5		V
Output Section						
Output Low Level	$I_{OUT} = 20mA$ $I_{OUT} = 200mA$	● ●		0.25 0.75	0.4 2.2	V V
Output High Level	$I_{OUT} = 20mA$ $I_{OUT} = 200mA$	● ●	12.0 11.75			V V
Rise Time	$C_L = 1nF$, $T_J = 25°C$			30	70	ns
Fall Time	$C_L = 1.0nF$, $T_J = 25°C$			20	60	ns
Output Clamp Voltage	$I_O = 1mA$	●		18	19	V
Under-Voltage Lockout						
Start-Up Threshold		●	15	16	17	V
Minimum Operating Voltage		●	9.0	10	11	V
Hysteresis			5.5	6.0		V
PWM						
Maximum Duty Cycle	$T_J = 25°C$		94		100	%
Minimum Duty Cycle	$T_J = 25°C$			0		%
Total Device						
Start-Up Current		●		170	250	μA
Operating Current		●		13	20	mA

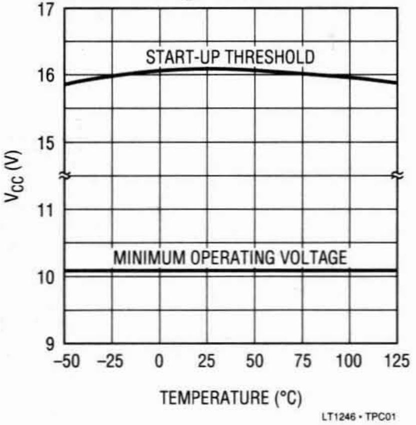
The ● denotes those specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, $V_{CC} = 15V$, $R_T = 10k$, $C_T = 3.3nF$.

Note 2: Low duty cycle pulse techniques are used during test to maintain junction temperature close to ambient.

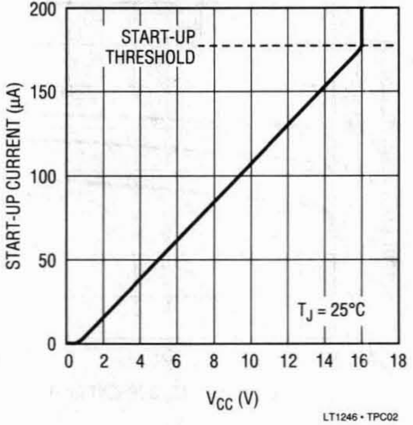
TYPICAL PERFORMANCE CHARACTERISTICS

Under-Voltage Lockout



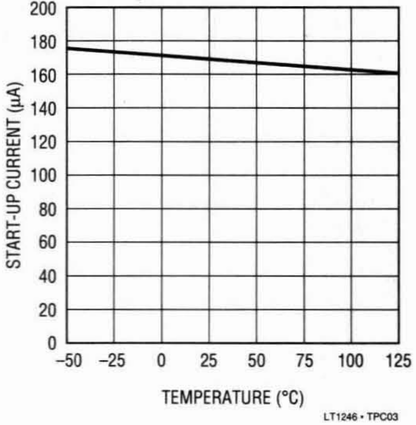
LT1246 • TPC01

Start-Up Current



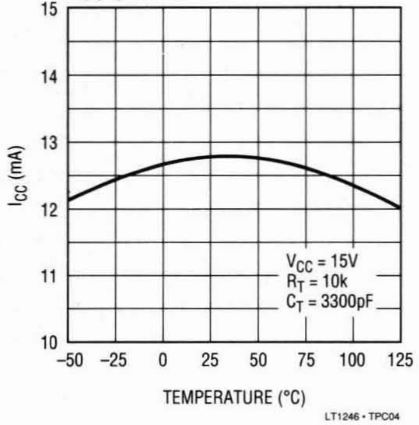
LT1246 • TPC02

Start-Up Current



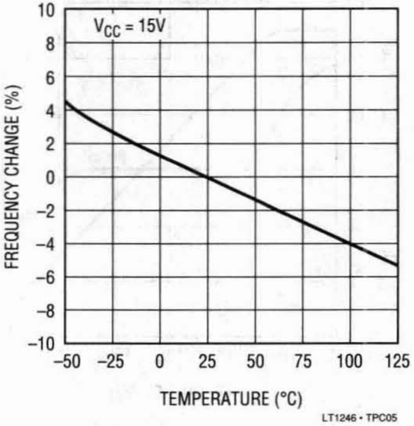
LT1246 • TPC03

Supply Current



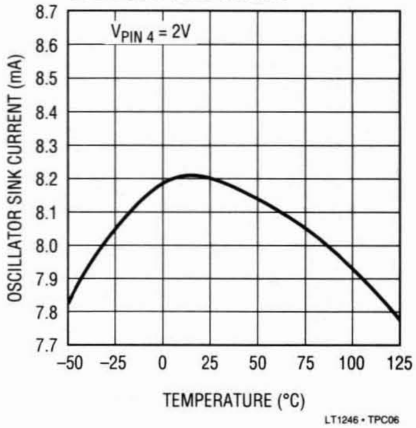
LT1246 • TPC04

Oscillator Frequency



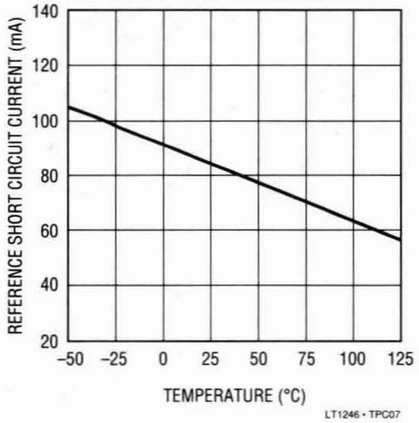
LT1246 • TPC05

Oscillator Sink Current



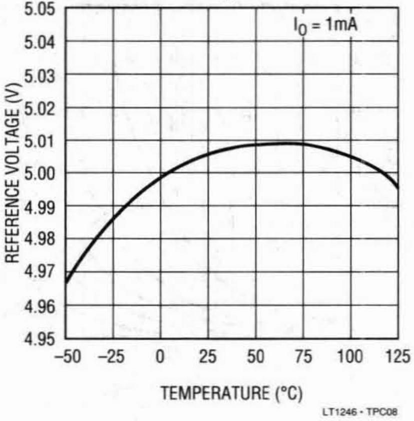
LT1246 • TPC06

Reference Short Circuit Current



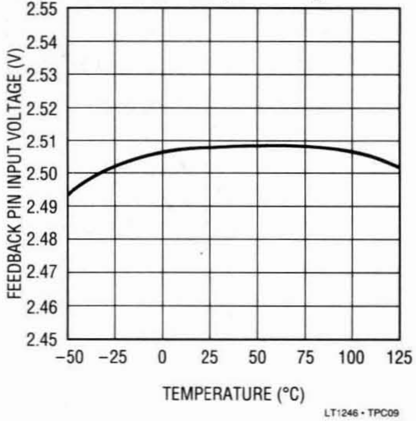
LT1246 • TPC07

Reference Voltage



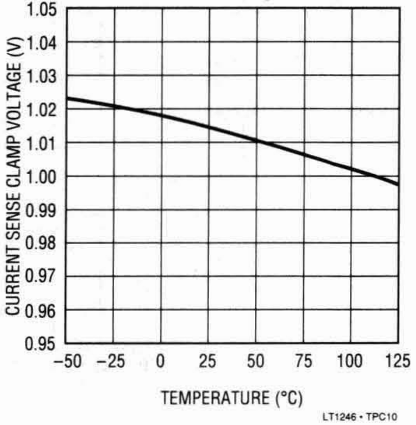
LT1246 • TPC08

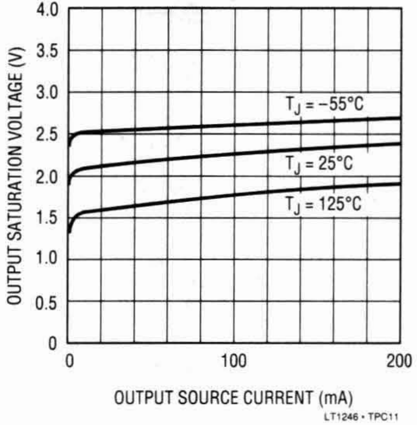
Feedback Pin Input Voltage

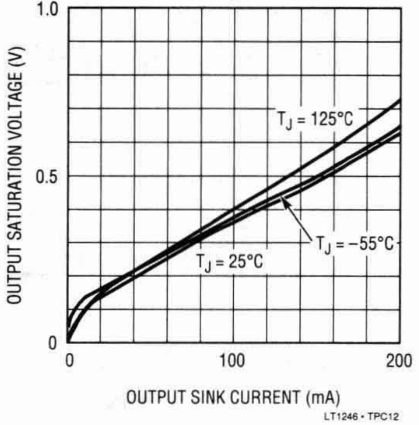


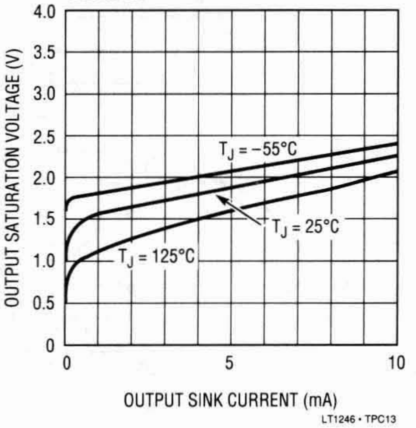
LT1246 • TPC09

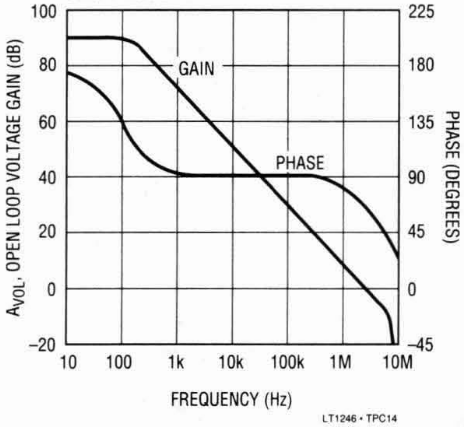
TYPICAL PERFORMANCE CHARACTERISTICS

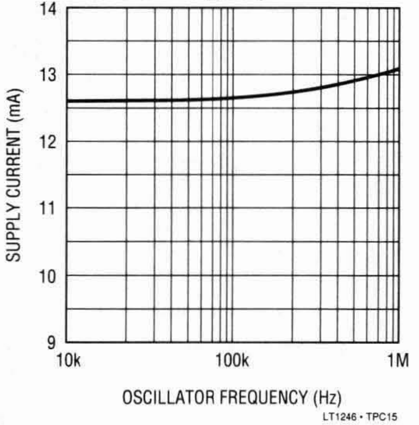

Current Sense Clamp Voltage

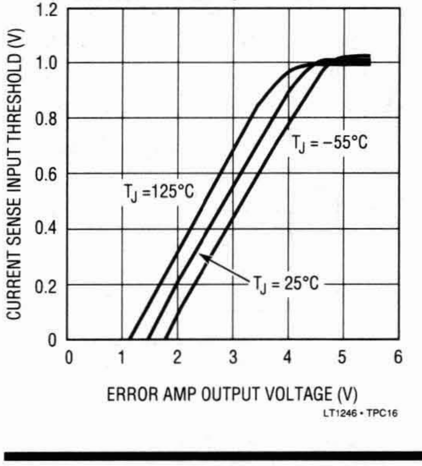

High Level Output Saturation Voltage

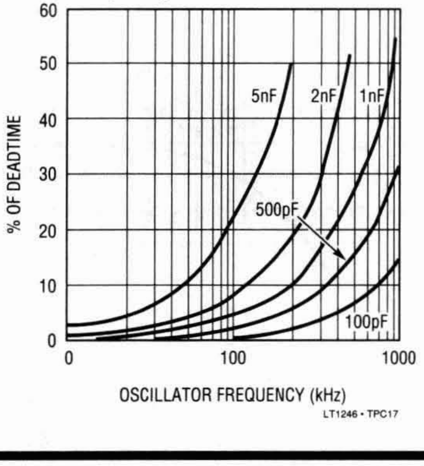

Low Level Output Saturation Voltage

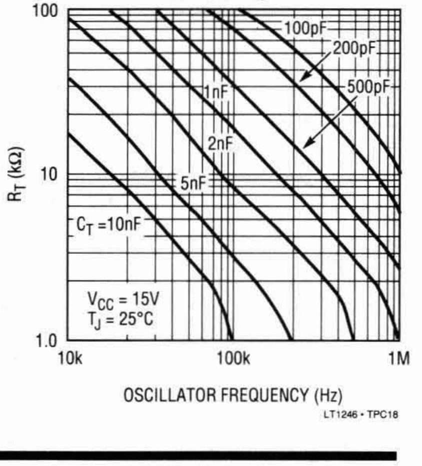

Low Level Output Saturation Voltage During Under-Voltage Lockout


Error Amplifier Open Loop Gain and Phase


Supply Current vs Oscillator Frequency

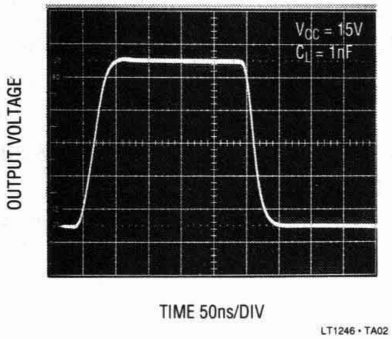

Current Sense Input Threshold


Output Deadtime vs Oscillator Frequency

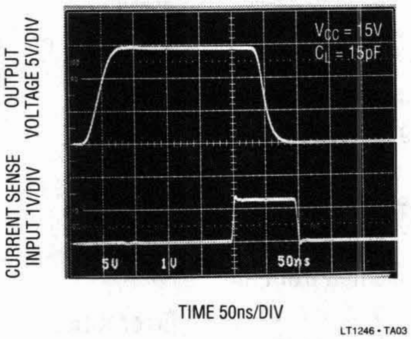

Timing Resistor vs Oscillator Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

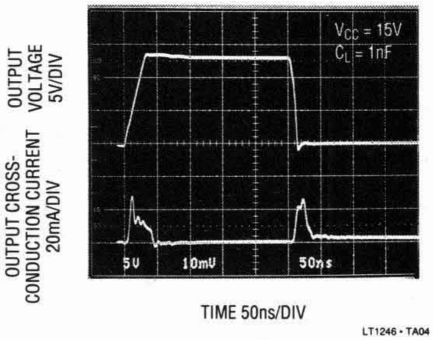
Output Rise and Fall Time



Current Sense Delay



Output Cross-Conduction



PIN FUNCTIONS

Pin 1, Compensation: This pin is the output of the Error Amplifier and is made available for loop compensation. It can also be used to adjust the maximum value of the current sense clamp voltage to less than 1V. This pin can source a minimum of 0.5mA (0.8mA typ.) and sink a minimum of 2mA (4mA typ.)

Pin 2, Voltage Feedback: This pin is the inverting input of the Error Amplifier. The output voltage is normally fed back to this pin through a resistive divider. The non-inverting input of the Error Amplifier is internally committed to a 2.5V reference point.

Pin 3, Current Sense: This is the input to the current sense comparator. The trip point of the comparator is set by, and is proportional to, the output voltage of the Error Amplifier.

Pin 4, R_T/C_T: The oscillator frequency and the deadtime are set by connecting a resistor (R_T) from V_{REF} to R_T/C_T and a capacitor (C_T) from R_T/C_T to GND.

The rise time of the oscillator waveform is set by the RC time constant of R_T and C_T. The fall time, which is equal to the output deadtime, is set by a combination of the RC time constant and the oscillator sink current (8.2mA typ.).

Pin 5, GND.

Pin 6, Output: This pin is the output of a high current totem pole output stage. It is capable of driving up to ±1A of current into a capacitive load such as the gate of a MOSFET.

Pin 7, V_{CC}: This pin is the positive supply of the control IC.

Pin 8, Reference: This is the reference output of the IC. The reference output is used to supply charging current to the external timing resistor R_T. The reference provides biasing to a large portion of the internal circuitry, and is used to generate several internal reference levels including the V_{FB} level and the current sense clamp voltage.

APPLICATIONS INFORMATION

Oscillator

The LT1246 is a fixed frequency current mode pulse width modulator. The oscillator frequency and the oscillator discharge current are both trimmed and tightly specified to minimize the variations in frequency and deadtime. The oscillator frequency is set by choosing a resistor and capacitor combination, R_T and C_T. This RC combination will determine both the frequency and the maximum duty cycle. The resistor R_T is connected from V_{REF} (pin 8) to the R_T/C_T pin (pin 4). The capacitor C_T is connected from the R_T/C_T pin to ground. The charging current for C_T is determined by the value of R_T. The discharge current for C_T is set by the difference between the current supplied by R_T and the discharge current of the LT1246. The discharge current of the device is trimmed to 8.2mA. For large values of R_T discharge time will be determined by the discharge current of the device and the value of C_T. As the value of R_T is reduced it will have more effect on the discharge time of C_T. During an oscillator cycle capacitor C_T is charged to approximately 2.8V and discharged to approximately 1.1V. The output is enabled during the charge time of C_T and disabled, in an off state, during the discharge time of C_T. The deadtime of the circuit is equal to the discharge time of C_T. The maximum duty cycle is limited by controlling the deadtime of the oscillator. There are many combinations of R_T and C_T that will yield a given oscillator frequency, however there is only one combination that will yield a specific deadtime at that frequency. Curves of oscillator frequency and deadtime for various values of R_T and C_T appear in the Typical Performance Characteristics section. Frequency and deadtime can also be calculated using the following formulas:

$$\text{Oscillator Rise Time: } t_r = 0.583 \bullet RC$$

$$\text{Oscillator Discharge Time: } t_d = \frac{3.46 \bullet RC}{0.0164R - 11.73}$$

$$\text{Oscillator Period: } T_{OSC} = t_r + t_d$$

$$\text{Oscillator Frequency: } f_{OSC} = \frac{1}{T_{OSC}}$$

$$\text{Maximum Duty Cycle: } D_{MAX} = \frac{t_r}{T_{OSC}} = \frac{T_{OSC} - t_d}{T_{OSC}}$$

The above formulas will give values that will be accurate to approximately ±5%, at the oscillator, over the full operating frequency range. This is due to the fact that the oscillator trip levels are constant versus frequency and the discharge current and initial oscillator frequency are trimmed. Some fine adjustment may be required to achieve more accurate results. Once the final R_T/C_T combination is selected the oscillator characteristics will be repeatable from device to device. Note that there will be some slight differences between maximum duty cycle at the oscillator and maximum duty cycle at the output due to the finite rise and fall times of the output.

Error Amplifier

The LT1246 contains a fully compensated error amplifier with a DC gain of 90dB and a unity gain frequency of 2MHz. Phase margin at unity gain is 80°. The non-inverting input is internally committed to a 2.5V reference point derived from the 5V reference of pin 8. The inverting input (pin 2) and the output (pin 1) are made available to the user. The output voltage in a regulator circuit is normally fed back to the inverting input of the error amplifier through a resistive divider. The output of the error amplifier is made available for external loop compensation. The output current of the error amplifier is limited to approximately 0.8mA sourcing and approximately 6mA sinking.

In a current mode PWM the peak switch current is a function of the output voltage of the error amplifier. In the LT1246 the output of the error amplifier is offset by two diodes (1.4V at 25°C), divided by a factor of three, and fed to the inverting input of the current sense comparator. For output voltages less than 1.4V the duty cycle of the output stage will be zero. The maximum offset that can appear at the current sense input is limited by a 1V clamp. This occurs when the error amplifier output reaches 4.4V at 25°C. The output of the error amplifier can be clamped below 4.4V in order to reduce the maximum voltage allowed across the current sensing resistor to less than 1V. The supply current will increase by the value of the output source current when the output voltage of the error amplifier is clamped.

APPLICATIONS INFORMATION

Current Sense Comparator and PWM Latch

LT1246 is a current mode controller. Under normal operating conditions the output (pin 6) is turned on at the start of every oscillator cycle, coincident with the rising edge of the oscillator waveform. The output is then turned off when the switch current reaches a threshold level proportional to the error voltage at the output of the error amplifier. Once the output is turned off it is latched off until the start of the next cycle. The peak switch current is thus proportional to the error voltage and is controlled on a cycle by cycle basis. The peak switch current is normally sensed by placing a sense resistor in the source lead of the output MOSFET. This resistor converts the switch current to a voltage that can be fed into the current sense input. For normal operating conditions the peak inductor current, which is equal to the peak switch current, will be equal to:

$$I_{PK} = \frac{\left(V_{PIN\,1} - 1.4V\right)}{\left(3R_S\right)}$$

During fault conditions the maximum threshold voltage at the input of the current sense comparator is limited by the internal 1V clamp at the inverting input. The peak switch current will be equal to:

$$I_{PK\,(MAX)} = \frac{1.0V}{R_S}$$

In certain applications such as high power regulators it may be desirable to limit the maximum threshold voltage to less than 1V in order to limit the power dissipated in the sense resistor or to limit the short circuit current of the regulator circuit. This can be accomplished by clamping the output of the error amplifier. A voltage level of approximately 1.4V at the error amplifier output will give a threshold voltage of 0V. A voltage level of approximately 4.4V at the output of the error amplifier will give a threshold level of 1V. Between 1.4V and 4.4V the threshold voltage will change by a factor of one third of the change in the error amplifier output voltage. The threshold voltage will be 0.333V for an error amplifier voltage of 2.4V. To reduce the maximum current sense threshold to less than 1V the error amplifier output should be clamped to less than 4.4V.

Blanking

A unique feature of the LT1246 is the built in blanking circuit at the output of the current sense comparator. A common problem with current mode PWM circuits is erratic operation due to noise at the current sense input. The primary cause of noise problems is the leading edge current spike due to transformer interwinding capacitance and diode reverse recovery time. This current spike can prematurely trip the current sense comparator causing an instability in the regulator circuit. A filter at the current sense input is normally required to eliminate this instability. This filter will in turn slow down the current sense loop. A slow current sense loop will increase the minimum pulse width which will increase the short circuit current in an overload condition. The LT1246 blanks (locks out) the signal at the output of the current sense comparator for a fixed amount of time after the switch is turned on. This prevents the PWM latch from tripping due to the leading edge current spike. The blanking time will be a function of the voltage at the feedback pin (pin 2). The blanking time will be 60ns for normal operating conditions ($V_{FB} = 2.5V$). The blanking time goes to zero as the feedback pin is pulled to 0V. This means that the blanking time will be minimized during start-up and also during an output short circuit fault. This blanking circuit eliminates the need for an input filter at the current sense input except in extreme cases. Eliminating the filter allows the current sense loop to operate with minimum delays, reducing peak currents during fault conditions.

Under-Voltage Lockout

The LT1246 incorporates an under-voltage lockout comparator which prevents the internal reference circuitry and the output from starting up until the supply voltage reaches the start-up threshold voltage. The quiescent current, below the start-up threshold, has been reduced to less than 250μA (170μA typ.). This minimizes the power loss due to the start-up resistor used in off-line converters. In under-voltage lockout both V_{REF} (pin 8) and the Output (pin 6) are actively pulled low by Darlington connected PNP transistors. They are designed to sink a few milliamps of current and will pull down to about 1V. The pull-down transistor at the reference pin can be used to reset the

APPLICATIONS INFORMATION

external soft start capacitor. The pull-down transistor at the output eliminates the external pull-down resistor required, with earlier devices, to hold the external MOSFET gate low during under-voltage lockout.

Output

The LT1246 incorporates a single high current totem pole output stage. This output stage is capable of driving up to ±1A of output current. Cross-conduction current spikes in the output totem pole have been eliminated. This device is primarily intended for driving MOSFET switches. Rise time is typically 30ns and fall time is typically 20ns when driving a 1.0nF load. A clamp is built into the device to prevent the output from rising above 18V in order to protect the gate of the MOSFET switch. The output is actively pulled low during under-voltage lockout by a Darlington PNP. This PNP is designed to sink several milliamps and will pull the output down to approximately 1V. This active pull-down eliminates the need for the external resistor which was required in older designs.

The output pin of the device connects directly to the emitter of the upper NPN drive transistor and the collector of the lower NPN drive transistor in the totem pole. The collector of the lower transistor, which is n-type silicon, forms a p-n junction with the substrate of the device. The substate of the device is tied to ground. This junction is reverse biased during normal operation. In some applications the parasitic LC of the external MOSFET gate can ring and pull the output pin below ground. If the output pin is pulled negative by more than a diode drop the parasitic diode formed by the collector of the output NPN and the substrate will turn on. This can cause erratic operation of the device. In these cases a Schottky clamp diode is recommended from output to ground.

Reference

The internal reference of the LT1246 is a 5V Bandgap reference, trimmed to within ±1% initial tolerance. The reference is used to power the majority of the internal logic and the oscillator circuitry. The oscillator charging current is supplied from the reference. The feedback pin voltage and the clamp level for the current sense comparator are derived from the reference voltage. The reference can supply up to 20mA of current to power external circuitry. Note that using the reference in this manner, as a voltage regulator, will significantly increase the power dissipation in the device, which will reduce the operating ambient temperature range.

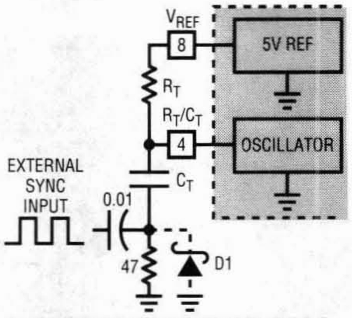
Design/Layout Considerations

LT1246 is a high speed circuit capable of generating pulsed output drive currents of up to 1A peak. The rise and fall time for the output drive current is in the range of 10ns to 20ns. High speed circuit layout techniques must be used to insure proper operation of the device. **Do not attempt to use Proto-boards or wire-wrap techniques to breadboard high speed switching regulator circuits. They will not work properly.**

Printed circuit layouts should include separate ground paths for the voltage feedback network, oscillator capacitor, and switch drive current. These ground paths should be connected together directly at the ground pin (pin 5) of the LT1246. This will minimize noise problems due to pulsed ground pin currents. V_{CC} should be bypassed, with a minimum of 0.1μF, as close to the device as possible. High current paths should be kept short and they should be separated from the feedback voltage network with shield traces if possible.

TYPICAL APPLICATIONS

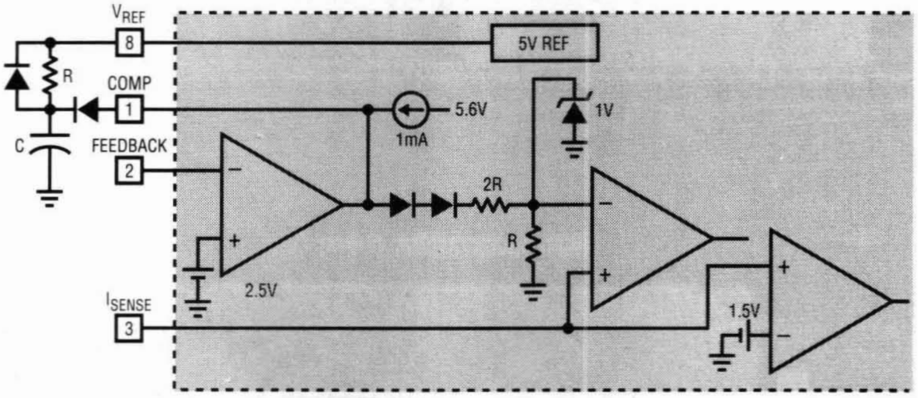
External Clock Synchronization


V_REF
8
5V REF
R_T
R_T/C_T
4
OSCILLATOR
C_T
EXTERNAL
SYNC
INPUT
0.01
47
D1

D1 IS REQUIRED IF THE SYNC AMPLITUDE IS LARGE ENOUGH TO PULL THE BOTTOM OF C_T MORE THAN 300mV BELOW GROUND.

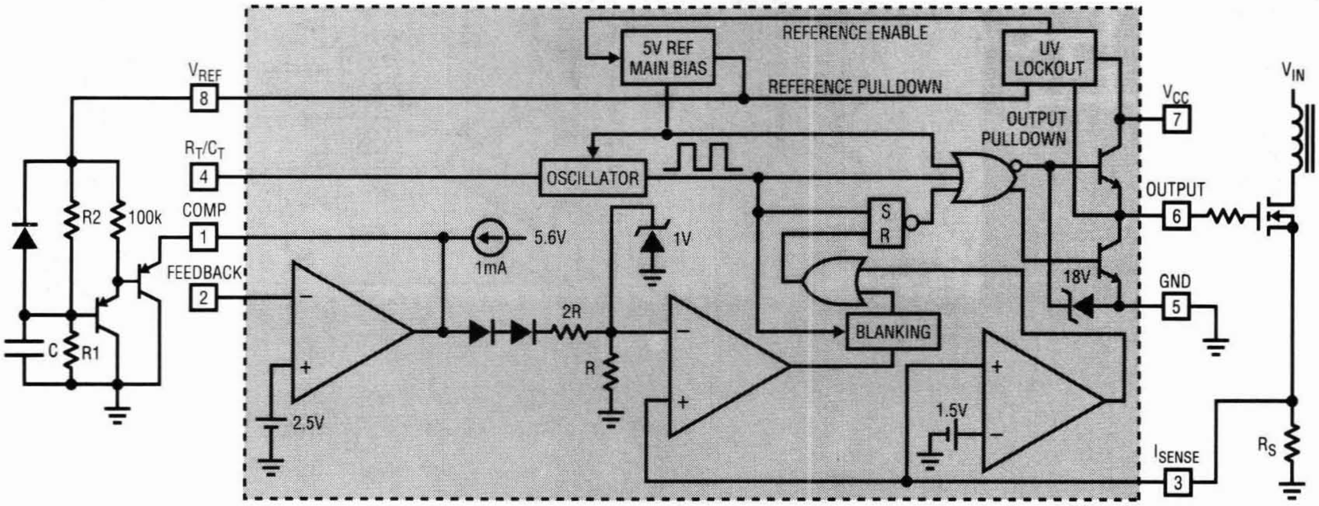
LT1246 • TA05

Soft Start


V_REF
8
5V REF
R
COMP
1
5.6V
1mA
1V
C
FEEDBACK
2
2R
R
2.5V
I_SENSE
3
1.5V

LT1246 • TA06

Adjustable Clamp Level with Soft Start

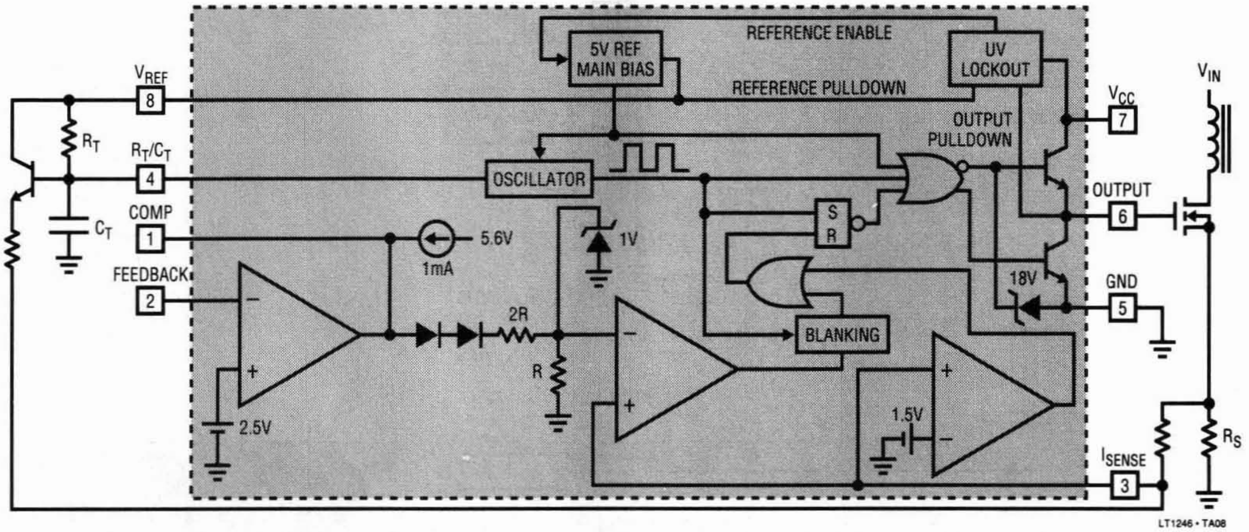

REFERENCE ENABLE
5V REF
MAIN BIAS
UV
LOCKOUT
V_IN
V_REF
8
REFERENCE PULLDOWN
V_CC
7
OUTPUT
PULLDOWN
R_T/C_T
4
OSCILLATOR
OUTPUT
6
S
R
R2
100k
COMP
1
5.6V
1V
1mA
18V
GND
FEEDBACK
2
5
2R
BLANKING
C
R1
R
1.5V
2.5V
I_SENSE
3
R_S

$V_{CLAMP} \approx \frac{1.67}{\left(\frac{R2}{R1}+1\right)}$ $I_{PK\,(MAX)} \approx \frac{V_{CLAMP}}{R_S}$ WHERE: $0 \le V_{CLAMP} \le 1.0V$ $t_{SOFT\ START} = -\ln\left[1 - \frac{V_C}{3 \bullet V_{CLAMP}}\right] C\,\frac{R1\,R2}{R1 + R2}$

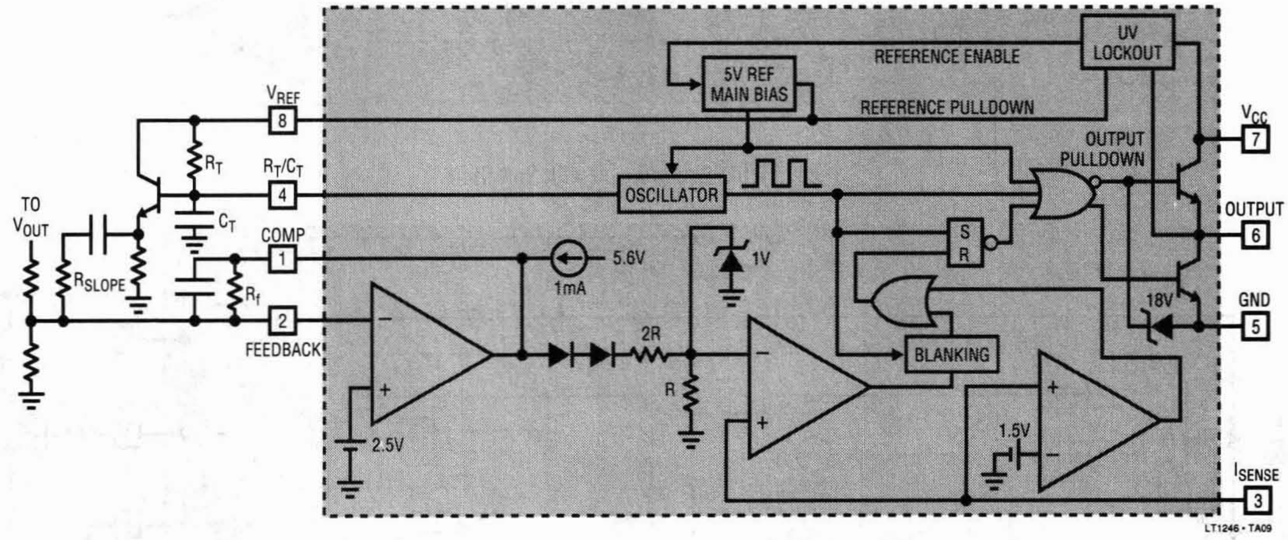
LT1246 • TA07

TYPICAL APPLICATIONS

Slope Compensation at I_{SENSE} Pin


REFERENCE ENABLE
5V REF MAIN BIAS
UV LOCKOUT
REFERENCE PULLDOWN
V_{REF}
8
R_T
R_T/C_T
4
C_T
COMP
1
FEEDBACK
2
OSCILLATOR
OUTPUT PULLDOWN
V_{CC}
7
V_{IN}
OUTPUT
6
S
R
5.6V
1mA
1V
18V
GND
5
BLANKING
2R
R
2.5V
1.5V
I_{SENSE}
3
R_S
LT1246 • TA08

Slope Compensation at Error Amp


REFERENCE ENABLE
UV LOCKOUT
5V REF MAIN BIAS
REFERENCE PULLDOWN
V_{REF}
8
R_T
R_T/C_T
4
TO V_{OUT}
C_T
COMP
1
R_{SLOPE}
R_f
2
FEEDBACK
OSCILLATOR
OUTPUT PULLDOWN
V_{CC}
7
OUTPUT
6
S
R
5.6V
1mA
1V
18V
GND
5
BLANKING
2R
R
2.5V
1.5V
I_{SENSE}
3
LT1246 • TA09

LINEAR TECHNOLOGY

LT1432

5V High Efficiency Step-Down Switching Regulator Controller

FEATURES

- Accurate Preset +5V Output
- Up to 90% Efficiency
- Optional Burst Mode for Light Loads
- Can be Used with Many LTC Switching ICs
- Accurate Ultra-Low-Loss Current Limit
- Operates with Inputs from 6V to 30V
- Shutdown Mode Draws Only 15μA
- Uses Small 50μH Inductor

APPLICATIONS

- Laptop and Palmtop Computers
- Portable Data-Gathering Instruments
- DC Bus Distribution Systems
- Battery-Powered Digital Widgets

DESCRIPTION

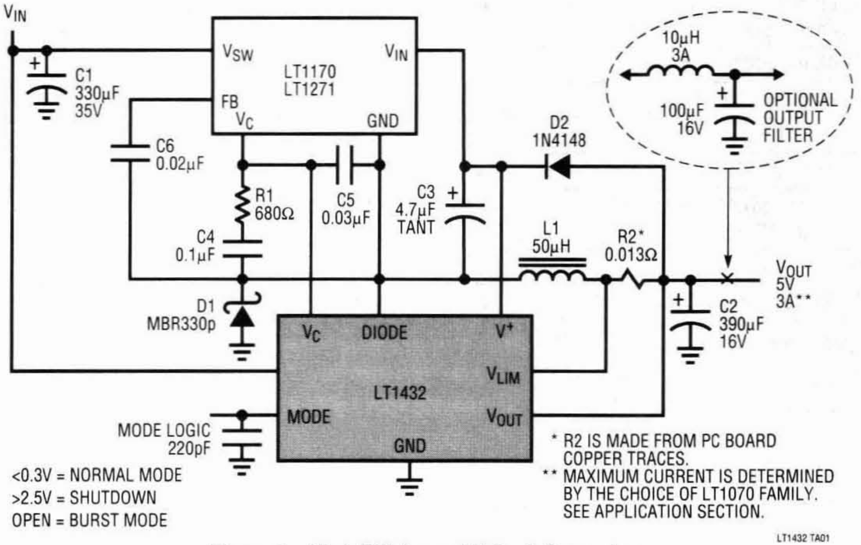
The LT1432 is a control chip designed to operate with the LT1170/LT1270 family of switching regulators to make a very high efficiency 5V step-down (buck) switching regulator. A minimum of external components is needed.

Included is an accurate current limit which uses only 60mV sense voltage and uses "free" PC board trace material for the sense resistor. Logic controlled electronic shutdown mode draws only 15μA battery current. The switching regulator operates down to 6V input.

The LT1432 has a logic controlled "burst" mode to achieve high efficiency at very light load currents (0 to 100mA) such as memory keep-alive. In normal switching mode, the standby power loss is about 60mW, limiting efficiency at light loads. In burst mode, standby loss is reduced to approximately 15mW. Output current in this mode is typically in the 5mA to 100mA range.

The LT1432 is available in 8-pin surface mount and DIP packages. The LT1170/LT1270 family will also be available in a surface mount version of the 5-pin TO-220 package. For 3.3V versions contact Linear Technology Corporation.

TYPICAL APPLICATION

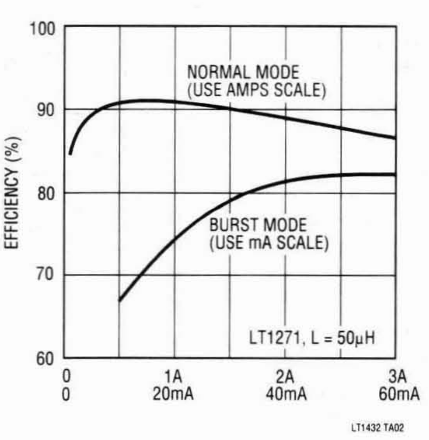

V_{IN}
C1
330μF
35V
V_{SW}
V_{IN}
LT1170
LT1271
FB
V_C
GND
C6
0.02μF
R1
680Ω
C5
0.03μF
C3
4.7μF
TANT
C4
0.1μF
D1
MBR330p
D2
1N4148
L1
50μH
R2*
0.013Ω
10μH
3A
100μF
16V
OPTIONAL OUTPUT FILTER
V_{OUT}
5V
3A**
C2
390μF
16V
V_C
DIODE
V^+
V_{LIM}
LT1432
MODE
V_{OUT}
GND
MODE LOGIC
220pF
LT1432 TA01

<0.3V = NORMAL MODE
>2.5V = SHUTDOWN
OPEN = BURST MODE

* R2 IS MADE FROM PC BOARD COPPER TRACES.
** MAXIMUM CURRENT IS DETERMINED BY THE CHOICE OF LT1070 FAMILY. SEE APPLICATION SECTION.

Figure 1. High Efficiency 5V Buck Converter

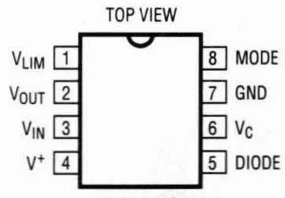
Efficiency



ABSOLUTE MAXIMUM RATINGS

V_{IN} Pin	30V
V^+ Pin	40V
V_C	35V
V_{LIM} and V_{OUT} Pins	7V
Diode Pin Voltage	30V
Mode Pin Current (Note 2)	1mA
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SO

ORDER PART NUMBER
LT1432CN8 LT1432CS8
S8 PART MARKING
1432

ELECTRICAL CHARACTERISTICS

$V_C = 6V$, $V_{IN} = 12V$, $V^+ = 10V$, V_{DIODE} = Open, $V_{LIM} = V_{OUT}$, $V_{MODE} = 0V$, $T_J = 25°C$
Device is in standard test loop unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Regulated Output Voltage	V_C Current = 220µA	●	4.9	5.0	5.1	V
Output Voltage Line Regulation	V_{IN} = 6V to 30V	●		5	20	mV
Input Supply Current (Note 1)	V_{IN} = 6V to 30V, $V^+ = V_{IN} + 5V$, $V_C = V_{IN} + 1V$	●		0.3	0.5	mA
Quiescent Output Load Current				0.9	1.2	mA
Mode Pin Current	V_{MODE} = 0V (current is out of pin) V_{MODE} = 5V (shutdown)	● ●		30 15	50 30	µA µA
Mode Pin Threshold Voltage (Normal to Burst)	I_{MODE} = 10µA (out of pin)	●	0.6	0.9	1.5	V
V_C Pin Saturation Voltage	V_{OUT} = 5.5V (forced)	●		0.25	0.45	V
V_C Pin Maximum Sink Current	V_{OUT} = 5.5V (forced)	●	0.45	0.8	1.5	mA
V_C Pin Source Current	V_{OUT} = 4.5V (forced)	●	40	60	100	µA
Current Limit Sense Voltage (Note 3)	Device in Current Limit Loop		56	60	64	mV
V_{LIM} Pin Current	Device in Current Limit Loop (current is out of pin)	●	30	45	70	µA
Supply Current in Shutdown	$V_{MODE} > 3V$, $V_{IN} < 30V$, V_C and $V^+ = 0V$	●		15	60	µA
Burst Mode Output Ripple	Device in Burst Test Circuit			100		mV_{p-p}
Burst Mode Average Output Voltage	Device in Burst Test Circuit	●	4.8	5	5.2	V
Clamp Diode Forward Voltage	I_F = 1mA, All Other Pins Open	●		0.5	0.65	V
Startup Drive Current	V_{OUT} = 2.5V (forced), V^+ = 5V to 25V, V_{IN} = 6V to 26V, $V^+ = V_{IN} - 1V$, $V_C = V_{IN} - 1.5V$	●	30	45		mA
Restart Time Delay	(Note 4)		1	1.8	10	ms
Transconductance, Output to V_C Pin	I_C = 150µA to 250µA	●	1500	2000	2800	µmho

The ● denotes specifications which apply over the operating temperature range.

Note 1: Does not include current drawn by the LT1070 IC. See operating parameters in standard circuit.

Note 2: Breakdown voltage on the mode pin is 7V. External current must be limited to value shown.

Note 3: Current limit sense voltage temperature coefficient is +0.33%/°C to match TC of copper trace material.

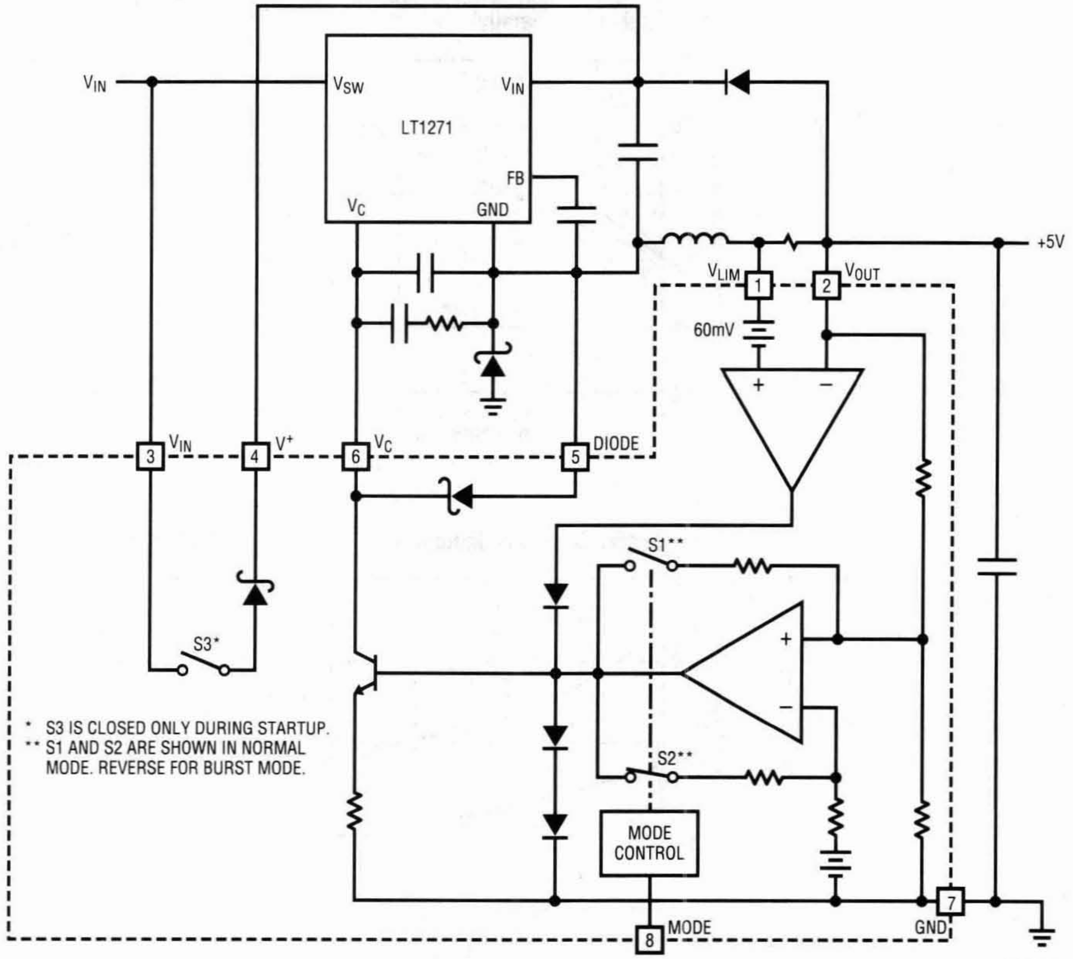
Note 4: V_{OUT} pin switched from 5.5Vto 4.5V.

ELECTRICAL CHARACTERISTICS

Operating parameters in standard circuit configuration.
V_{IN} = +12V, I_{OUT} = 0, unless otherwise noted. These parameters guaranteed where indicated, but not tested.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Burst Mode Quiescent Input Supply Current			1.3	1.8	mA
Burst Mode Output Ripple Voltage	I_{OUT} = 0 I_{OUT} = 50mA		100 130		mV_{p-p} mV_{p-p}
Normal Mode Equivalent Input Supply Current	Extrapolated from I_{OUT} = 20mA		6		mA
Normal Mode Minimum Operating Input Voltage	100mA < I_{OUT} < 1.5A		6		V
Burst Mode Minimum Operating Input Voltage	5mA < I_{OUT} < 50mA		6.2		V
Efficiency	Normal Mode I_{OUT} = 0.5A Burst Mode I_{OUT} = 25mA		91 77		% %
Load Regulation	Normal Mode 50mA < I_{OUT} < 2A Burst Mode 0 < I_{OUT} < 50mA		10 50	25	mV mV

EQUIVALENT SCHEMATIC



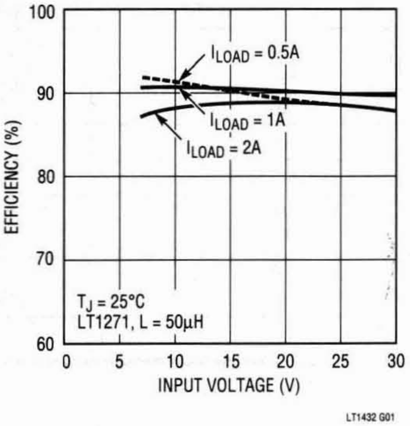
VIN
VSW
VIN
LT1271
FB
VC
GND
+5V
VLIM
1
2
VOUT
60mV
+
−
3
VIN
4
V+
6
VC
5
DIODE
S1**
S3*
+
−
S2**
MODE CONTROL
7
GND
8
MODE
LT1432 F02

* S3 IS CLOSED ONLY DURING STARTUP.
** S1 AND S2 ARE SHOWN IN NORMAL MODE. REVERSE FOR BURST MODE.

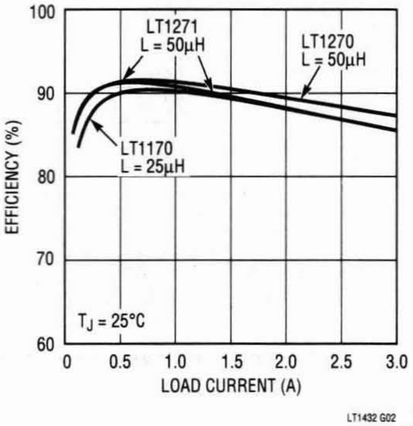
Figure 2

TYPICAL PERFORMANCE CHARACTERISTICS

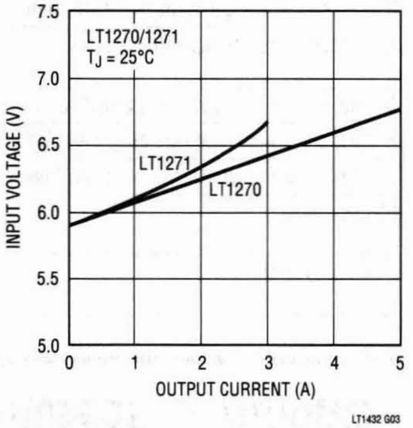
Efficiency vs Input Voltage



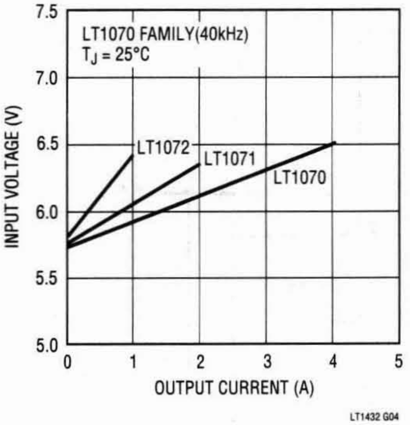
Efficiency vs Load Current



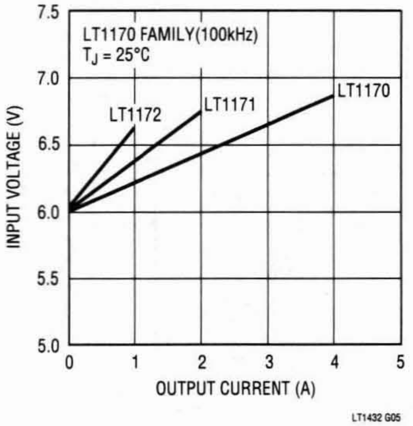
Minimum Input Voltage – Normal Mode (1270/1271)



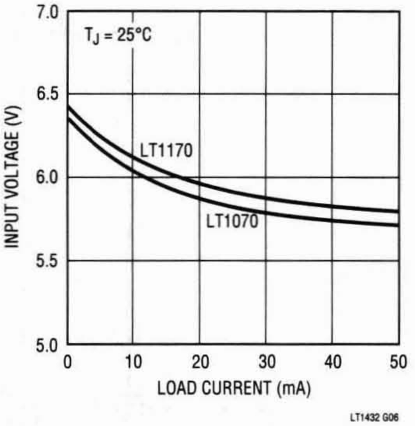
Minimum Input Voltage – Normal Mode (1070 Family)



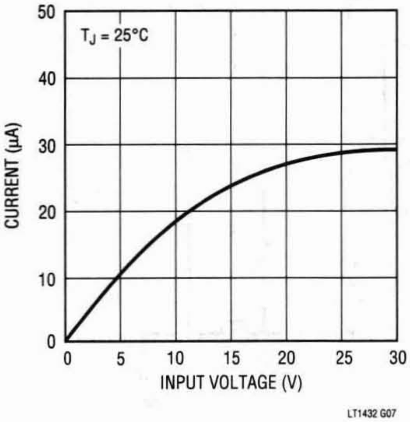
Minimum Input Voltage – Normal Mode (1170 Family)



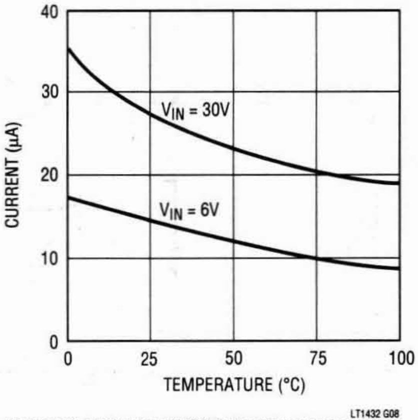
Burst Mode Minimum Input Voltage



Shutdown Current vs Input Voltage

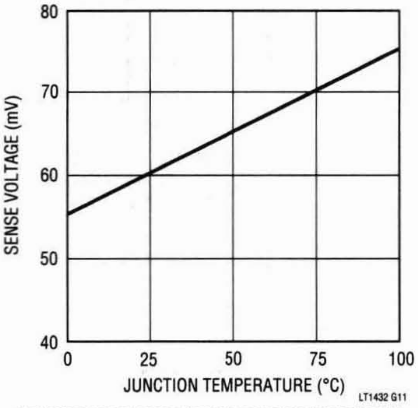


Battery Current in Shutdown*



*DOES NOT INCLUDE LT1271 SWITCH LEAKAGE.

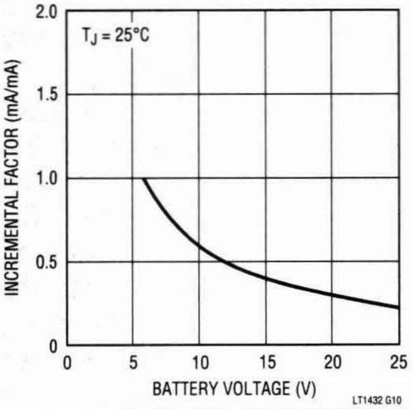
Current Limit Sense Voltage*



* TEMPERATURE COEFFICIENT OF SENSE VOLTAGE IS DESIGNED TO TRACK COPPER RESISTANCE.

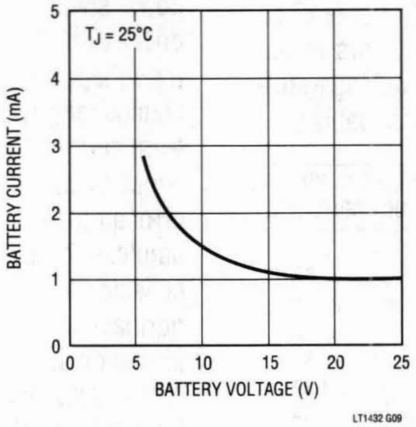
TYPICAL PERFORMANCE CHARACTERISTICS

Incremental Battery Current * in Burst Mode

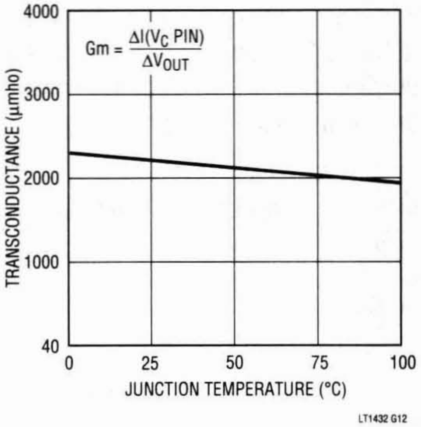


* TO CALCULATE TOTAL BATTERY CURRENT IN BURST MODE, MULTIPLY LOAD CURRENT BY INCREMENTAL FACTOR AND ADD NO-LOAD CURRENT.

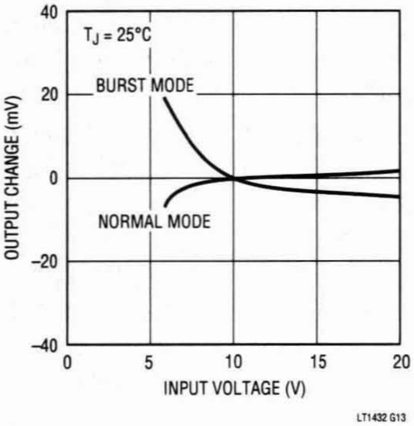
No Load Battery Current in Burst Mode



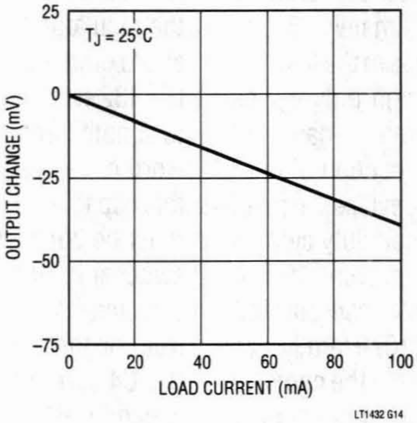
Transconductance – V_{OUT} to V_C Current



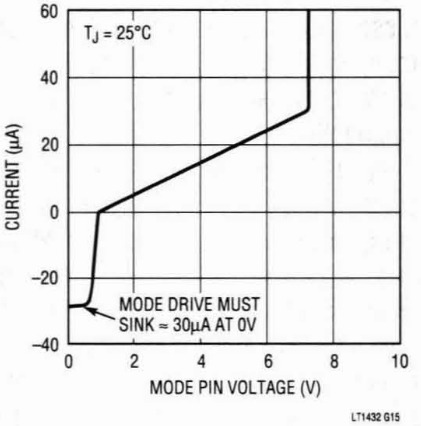
Line Regulation



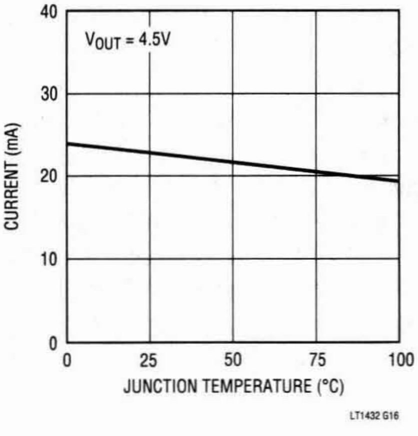
Burst Mode Load Regulation



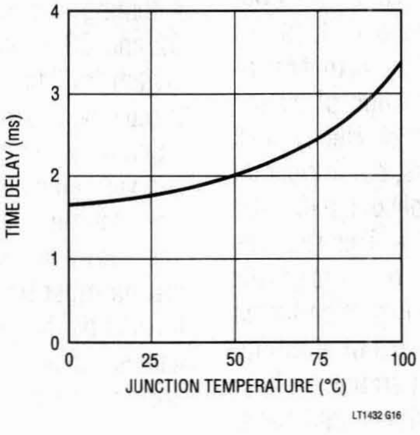
Mode Pin Current



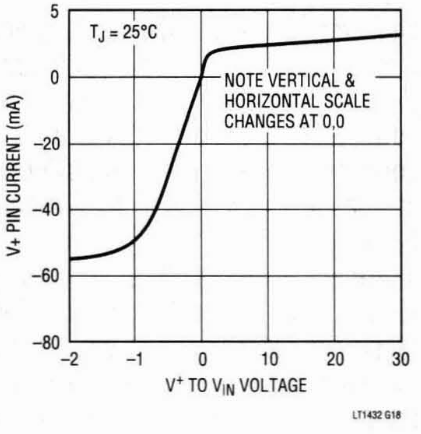
Restart Load Current



Restart Time Delay



Startup Switch Characteristics



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Basic Circuit Description

The LT1432 is a dedicated 5V buck converter driver chip intended to be used with an IC switcher from the LT1070 family. This family of current mode switchers includes current ratings from 1.25A to 10A, and switching frequencies from 40kHz to 100kHz as shown in the table below.

DEVICE	SWITCH CURRENT	FREQUENCY	OUTPUT CURRENT IN BUCK CONVERTER
LT1270A	10A	60kHz	7.5A
LT1270	8A	60kHz	6A
LT1170	5A	100kHz	3.75A
LT1070	5A	40kHz	3.75A
LT1271	4A	60kHz	3A
LT1171	2.5A	100kHz	1.8A
LT1071	2.5A	40kHz	1.8A
LT1172	1.25A	100kHz	0.9A
LT1072	1.25A	40kHz	0.9A

The maximum load current which can be delivered by these chips in a buck converter is approximately 75% of their switch current rating. This is partly due to the fact that buck converters must operate at very high duty cycles when input voltage is low. The "current mode" nature of the LT1070 family requires an internal reduction of peak current limit at high duty cycles, so these devices are rated at only 80% of their full current rating when duty cycle is 80%. A second factor is inductor ripple current, half of which subtracts from maximum available load current. See Inductor Selection for details. The LT1070 family was originally intended for topologies which have the negative side of the switch grounded, such as boost converters. It has an extremely efficient quasi-saturating NPN switch which mimics the linear resistive nature of a MOSFET but consumes much less die area. Driver losses are kept to a minimum with a patented adaptive antisat drive that maintains a forced beta of 40 over a wide range of switch currents. This family is attractive for high efficiency buck converters because of the low switch loss, but to operate as a positive buck converter, the ground pin of the IC must be floated to act as the switch output node. This requires a floating power supply for the chip and some means for level shifting the feedback signal. The LT1432 performs these functions as well as adding current limiting, micropower shutdown, and dual mode operation for high conversion efficiency with both heavy and very light loads.

The circuit in Figure 1 is a basic 5V positive buck converter which can operate with input voltage from 6V to 30V. The power switch is located between the V_{SW} pin and GND pin on the LT1271. Its current and duty cycle are controlled by the voltage on the V_C pin with respect to the GND pin. This voltage ranges from 1V to 2V as switch current increases from zero to full scale. Correct output voltage is maintained by the LT1432 which has an internal reference and error amplifier (see Equivalent Schematic in Figure 2). The amplifier output is level shifted with an internal open collector NPN to drive the V_C pin of the switcher. The normal resistor divider feedback to the switcher feedback pin cannot be used because the feedback pin is referenced to the GND pin, which is switching up and down. The feedback pin (FB) is simply bypassed with a capacitor. This forces the switcher V_C pin to swing high with about 200μA sourcing capability. The LT1432 V_C pin then sinks this current to control the loop. Transconductance from the regulator output to the V_C pin current is controlled to approximately 2000μmhos by local feedback around the LT1432 error amplifier (S2 closed in Figure 2). This is done to simplify frequency compensation of the overall loop. A word of caution about the FB pin bypass capacitor (C6): this capacitor value is very non-critical, but the capacitor must be connected directly to the GND pin or tab of the switcher to avoid differential spikes created by fast switch currents flowing in the external PCB traces. This is also true for the frequency compensation capacitors C4 and C5. C4 forms the dominant loop pole with a loop zero added by R1. C5 forms a higher frequency loop pole to control switching ripple at the V_C pin.

A floating 5V power supply for the switcher is generated by D2 and C3 which peak detect the output voltage during switch "off" time. The diode used for D2 is a low capacitance type to avoid spikes at the output. Do not substitute a Schottky diode for D2 (they are high capacitance). This is a very efficient way of powering the switcher because power drain does not increase with regulator input voltage. However, the circuit is not self-starting, so some means must be used to start the regulator. This is performed by the internal current path of the LT1432 which allows current to flow from the input supply to the V^+ pin during startup.

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D1, L1 and C2 act as the conventional catch diode and output filter of the buck converter. These components should be selected carefully to maintain high efficiency and acceptable output ripple. See other sections of this data sheet for detailed discussions of these parts.

Current limiting is performed by R2. Sense voltage is only 60mV to maintain high efficiency. This also reduces the value of the sense resistor enough to utilize a printed circuit board trace as the sense resistor. The sense voltage has a positive temperature coefficient of 0.33%/°C to match the temperature coefficient of copper. See Current Limiting section for details.

The basic regulator has three different operating modes, defined by the mode pin drive. Normal operation occurs when the mode pin is grounded. A low quiescent current "burst" mode can be initiated by floating the mode pin. Input supply current is typically 1.3mA in this mode, and output ripple voltage is $100mV_{p-p}$. Pulling the mode pin above 2.5V forces the entire regulator into micropower shutdown where it typically draws less than 20µA. See Mode Pin Drive for details.

Efficiency

Efficiency in normal mode is maximum at about 500mA load current, where it exceeds 90%. At lower currents, the operating supply current of the switching IC dominates losses. The power loss due to this term is approximately 8mA × 5V, or 40mW. This is 4% of output power at a load current of 200mA. At higher load currents, losses in the switch, diode, and inductor series resistance begin to increase as the square of current and quickly become the dominant loss terms.

Loss in inductor series resistance;

$$P = R_S\,(I_{OUT})^2$$

Loss in switch on resistance;

$$P = \frac{V_{OUT}(R_{SW})(I_{OUT})^2}{V_{IN}}$$

Loss in switch driver current;

$$P = \frac{I_{OUT}(V_{OUT})^2}{40V_{IN}}$$

Diode loss;

$$P = \frac{V_F(V_{IN} - V_{OUT})(I_{OUT})}{V_{IN}}$$

(Use V_F *vs* I_F graph on diode data sheet, assuming $I_F = I_{OUT}$)

R_S = Inductor series resistance
R_{SW} = Switch resistance of LT1271, etc.
I_F = Diode current
V_F = Diode forward voltage at $I_F = I_{OUT}$

Inductor core loss depends on peak-to-peak ripple current in the inductor, which is independent of load current for any load current large enough to establish continuous current in the inductor. Believe it or not, core loss is also independent of the physical size of the core. It depends only on core material, inductance value, and switching frequency for fixed regulator operating conditions. Increasing inductance or switching frequency will reduce core loss, because of the resultant decrease in ripple current. For high efficiency, low loss cores such as ferrites or Magnetics Inc. molypermalloy or KoolMµ are recommended. The lower cost Type 52 powdered iron from Phillips is acceptable only if larger inductance is used and the increased size and slight loss in efficiency is acceptable. In a typical buck converter using the LT1271 (60kHz) with a 12V input, and a 50µH inductor, core loss with a Type 52 powdered iron core is 203mW. A molypermalloy core reduces this figure to 28mW. With a 1A output, this translates to 4% and 0.56% core loss respectively – a big difference in a high efficiency converter. For details on inductor design and losses, see Application Note 44.

What are the benefits of using an active (synchronous) switch to replace the catch diode? This is the trendy thing to do, but calculations and actual breadboards show that the improvement in efficiency is only a few percent at best. This can be shown with the following simplified formulas:

$$\text{Diode Loss} = \frac{V_F(V_{IN} - V_{OUT})(I_{OUT})}{V_{IN}}$$

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$$\text{FET Switch Loss} = \frac{(V_{IN} - V_{OUT})(R_{SW})(I_{OUT})^2}{V_{IN}}$$

(Ignoring gate drive power)

The change in efficiency is:

$$\frac{(\text{Diode Loss} - \text{FET Loss})(\text{Efficiency})^2}{(V_{IN})(V_{OUT})}$$

This is equal to:

$$\frac{(V_{IN} - V_{OUT})(V_F - R_{FET} \times I_{OUT})(E)^2}{(V_{IN})(V_{OUT})}$$

If V_F (diode forward voltage) = 0.45V, V_{IN} = 10V, V_{OUT} = 5V, R_{FET} = 0.1Ω, I_{OUT} = 1A, and efficiency = 90%, the improvement in efficiency is only:

$$\frac{(10V - 5V)(0.45V - 0.1\Omega \times 1A)(0.9)^2}{(10V)(5V)} = 2.8\%$$

This does not take FET gate drive losses into account, which can easily reduce this figure to less than 2%. The added cost, size, and complexity of a synchronous switch configuration would be warranted only in the most extreme circumstances.

Burst mode efficiency is limited by quiescent current drain in the LT1432 and the switching IC. The typical burst mode zero-load input power is 27mW. This gives about one month battery life for a 12V, 1.2AHr battery pack. Increasing load power reduces discharge time proportionately. Full shutdown current is only about 15µA, which is considerably less than the self-discharge rate of typical batteries.

Burst Mode Operation

Burst mode is initiated by allowing the mode pin to float, where it will assume a DC voltage of approximately 1V. If AC pickup from surrounding logic lines is likely, the mode pin should be bypassed with a 200pF capacitor. Burst mode is used to reduce quiescent operating current when the regulator output current is very low, as in "sleep" mode in a lap-top computer. In this mode, hysteresis is added to the error amplifier to make it switch on and off, rather than maintain a constant amplifier output. This forces the switching IC to either provide a rapidly increasing current or to go into full micropower shutdown. Current is delivered to the output capacitor in pulses of higher amplitude and low duty cycle rather than a continuous stream of low amplitude pulses. This maximizes efficiency at light load by eliminating quiescent current in the switching IC during the period between bursts.

The result of pulsating currents into the output capacitor is that output ripple amplitude increases, and ripple frequency becomes a function of load current. The typical output ripple in burst mode is 150mVp-p, and ripple frequency can vary from 50Hz to 2kHz. This is not normally a problem for the logic circuits which are kept "alive" during sleep mode.

Some thought must be given to proper sequencing between normal mode and burst mode. A heavy (>100mA) load in burst mode can cause excessive output ripple, and an abnormally light load (10mA to 30mA, see curves) in normal mode can cause the regulator to revert to a quasi-burst mode that also has higher output ripple. The worst condition is a sudden, large increase in load current (>100mA) during this quasi-burst mode or just after a switch from burst mode to normal mode. This can cause the output to sag badly while the regulator is establishing normal mode operation (100µs). To avoid problems, it is suggested that the power-down sequence consist of reducing load current to below 100mA, but greater than the minimum for normal mode, then switching to burst mode, followed by a reduction of load current to the final sleep value. Power-up would consist of increasing the load current to the minimum for normal mode, then switching to normal mode, pausing for 1ms, followed by return to full load.

If this sequence is not possible, an alternative is to minimize normal mode settling time by adding a 47kΩ resistor between V^+ and V_C pins. The output capacitor should be increased to >680µF and the compensation capacitors should also be as small as possible, consistent with adequate phase margin. These modifications will

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often allow the power-down sequence to consist of simultaneous turn-off of load current and switch to burst mode. Power-up is accomplished by switching to normal mode and simultaneously increasing load current to the lowest possible value (30mA to 500mA), followed by a short pause and return to full load current.

Full Shutdown

When the mode pin is driven high, full shutdown of the regulator occurs. Regulator input current will then consist of the LT1432 shutdown current (≈15µA) plus the switch leakage of the switching IC (≈1µA to 25µA). Mode input current (≈15µA at 5V) must also be considered. Startup from shutdown can be in either normal or burst mode, but one should always check startup overshoot, especially if the output capacitor or frequency compensation components have been changed.

Switching Waveforms in Normal Mode

The waveforms in Figures 3 through 10 were taken with an input voltage of 12V. Figure 3 shows the classic buck converter waveforms of switch output voltage (5V/DIV) at the top and switch current (1A/DIV) underneath, at an output current of 2A. The regulator is operating in "continuous" mode as evidenced by the fact that switch current does not start at zero at switch turn-on. Instead, it jumps to an initial value, then continues to slope upward during the duration of switch on time. The slope of the current waveform is determined by the difference between input and output voltage, and the value of inductor used.

$$\frac{dI}{dt} = \frac{\left(V_{IN} - V_{OUT}\right)}{L}$$

According to theory, the average switch current during switch on time should be equal to the 2A output current and this is confirmed in the photograph. The peak switch current, however, is about 2.4A.This peak current must be considered when calculating maximum available load current because both the LT1432 and the LT1070 family current limit on instantaneous switch current.

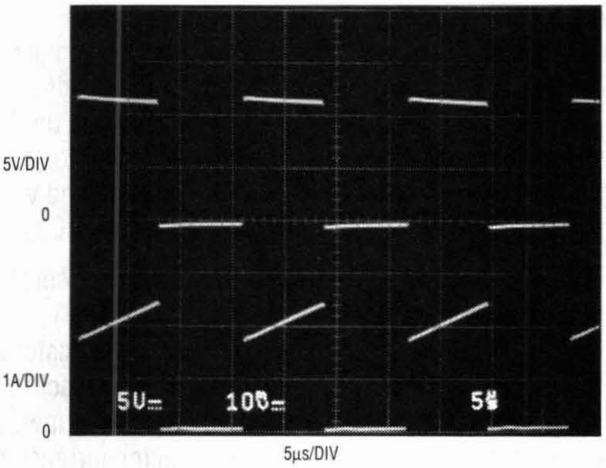

Figure 3

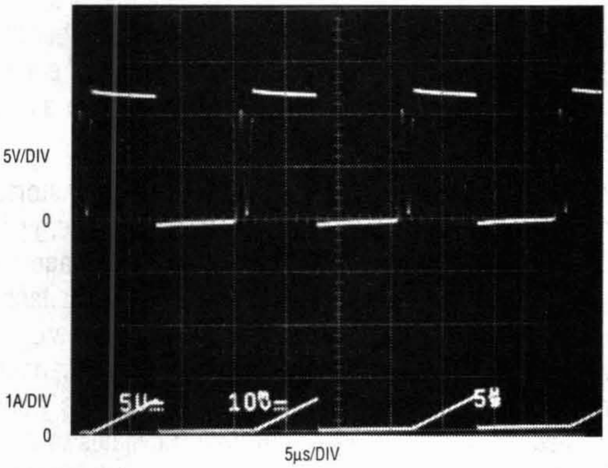

Figure 4

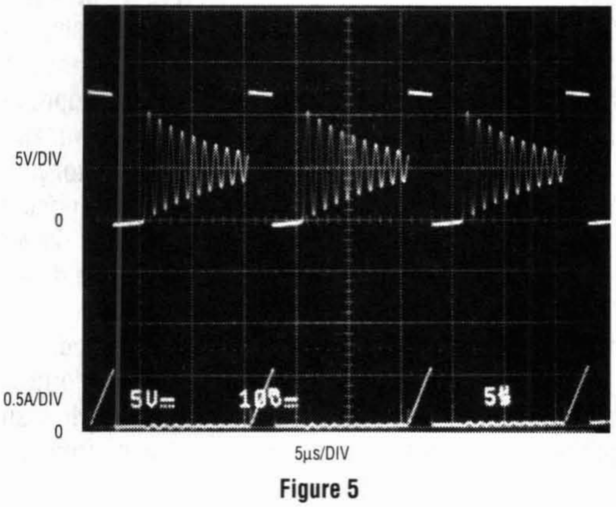

Figure 5

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Note that the switch output voltage is nearly identical to the 12V input during switch on time, a necessary requirement for high efficiency, and indicative of an efficient switch topology. Also note the fast, clean edges on the switching waveforms, an additional requirement for high efficiency. The "overlap time" of switch current and voltage, which leads to AC switching losses, is only 10ns.

Figure 4 shows the same waveforms when load current has been reduced to 0.25A, and Figure 5 is at 25mA (note the scale change for current in Figure 5). The regulator is now into discontinuous mode as shown by the fact that switch current has no initial jump, but starts its upward slope from zero. This implies that the inductor current has dropped to zero during switch off time, and that is shown by the "ringing" waveform on the rising edge of switch voltage. The switch has not yet been turned on, but the voltage at its output rises and rings as the "input" end of the inductor tries to settle to the same voltage as its "output" end (5V).

This ringing is not an oscillation. It is the result of stored energy in the catch diode capacitance. This energy is transferred to the inductor as the inductor voltage attempts to rise to 5V. The inductor and diode capacitance tank circuit continues to ring until the stored energy is dissipated by losses in the core and parasitic resistances. The relatively undamped nature in this case is good because it shows low losses and that translates to high efficiency. EMI is not increased by operating in this mode.

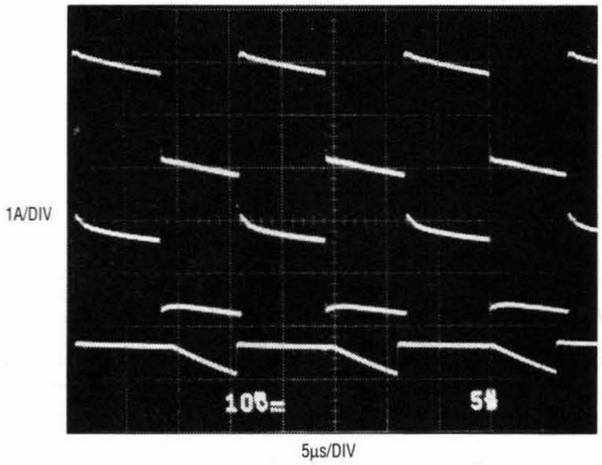

Figure 6. Input Capacitor Current

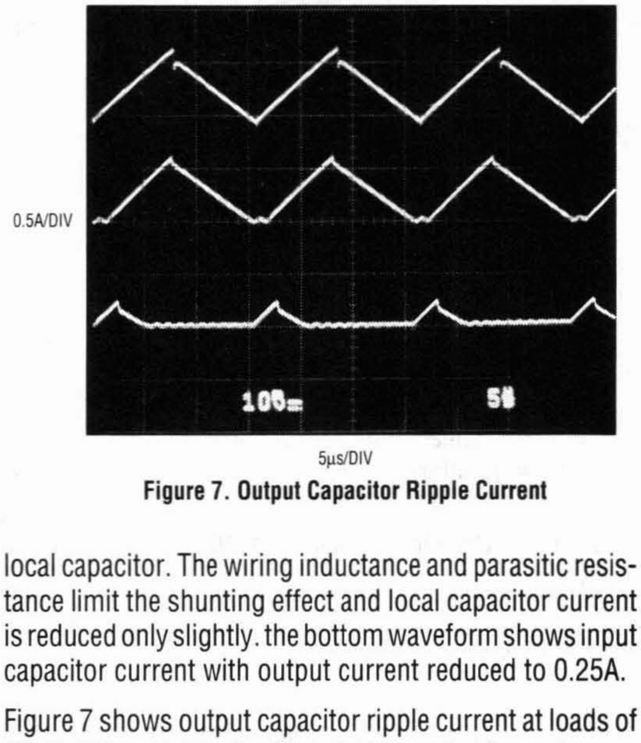

Figure 7. Output Capacitor Ripple Current

Figure 6 shows input capacitor current (1A/DIV) with I_{OUT} = 2A. The theoretical peak-to-peak value (ignoring sloping waveforms) is equal to output current, and this is indeed what the top waveform shows. The RMS value is approximately equal to one half output current. This is a major consideration because the physical size of a capacitor with 1A ripple current rating may make it the largest component in the regulator (see output capacitor section). Clever desigers may hit on the idea of utilizing battery impedance or remote input capacitors to divert some of the current away from the actual local capacitor to reduce its size. This is not too practical as shown by the middle waveform in Figure 6, which shows input capacitor current when an additional large capacitor is added about 6" away from the local capacitor. The wiring inductance and parasitic resistance limit the shunting effect and local capacitor current is reduced only slightly. the bottom waveform shows input capacitor current with output current reduced to 0.25A.

Figure 7 shows output capacitor ripple current at loads of 2A, 0.25A, and 25mA respectively starting from the top. Note that ripple current is independent of load current until the load drops well into the discontinuous region. The small steps superimposed on the triangular ripple are caused by loading of the diode which pumps the power supply capacitor on the LT1271. Amplitude of the ripple current is about 0.7Ap-p in this case, or approximately

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0.2A RMS. Theoretically the output capacitor size would be minimized by using one which just met this ripple current, but in practice, this would yield such high output ripple voltage that an additional output filter would have to be added. A better solution in the case of buck converters is usually just to increase the size of the output capacitor to meet output ripple voltage requirements.

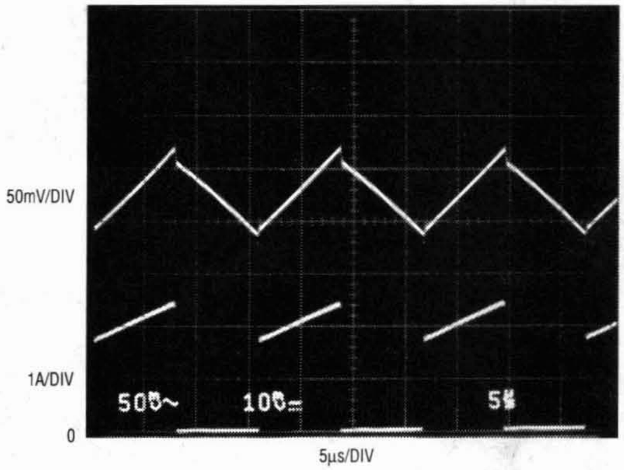

Figure 8. Output Ripple Current

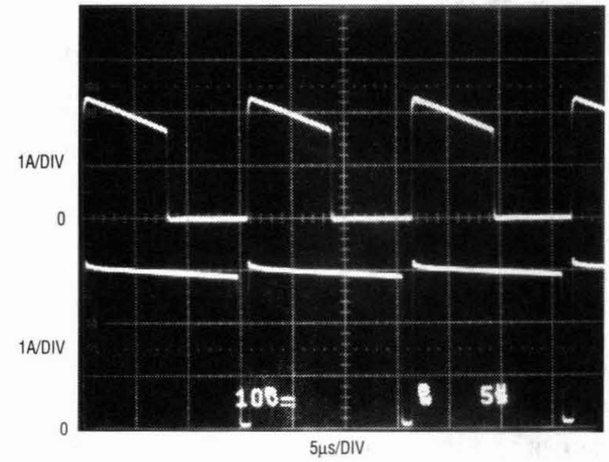

Figure 9. Diode Current

Figure 8 shows output ripple voltage at the top and switch current below. Peak-to-peak ripple voltage is 80mV. This implies an output capacitor effective series resistance (ESR) of 80mV/0.7A = 0.11Ω. Capacitor ESR varies significantly with temperature, increasing at low temperatures, so be sure to check ESR ratings at the lowest expected operating temperature. Ripple voltage can be reduced by increasing the inductor value, but this has rapidly diminishing returns because of typical size restraints.

Figure 9 shows diode current under normal load conditions of 2A, and with the output shorted. Current limit has been set at 3A. Average diode current at I_{OUT} = 2A is only about 1A because of duty cycle considerations. Under short circuit conditions, duty cycle is nearly 100% for the diode (switch duty cycle is near zero), and diode average current is nearly 3A. Designs which must tolerate continuous short circuit conditions should be checked carefully for diode heating. Foldback current limiting can be used if necessary.

Figure 10 shows inductor current (0.5A/DIV) with a 2A and 100mA load. Average inductor current is always equal to output current, but it is obvious that with 100mA load, inductor current drops to zero for part of the switching cycle, indicating dicontinuous mode. When selecting an inductor, keep in mind that RMS current determines copper losses, peak-to-peak current determines core loss, and peak current must be calculated to avoid core saturation. Also, remember that during short circuit conditions, inductor current will increase to the full current limit value. Inductor failure is normally caused by overheating of the winding insulation with resultant turn-to-turn shorts. Foldback current limiting will be helpful.

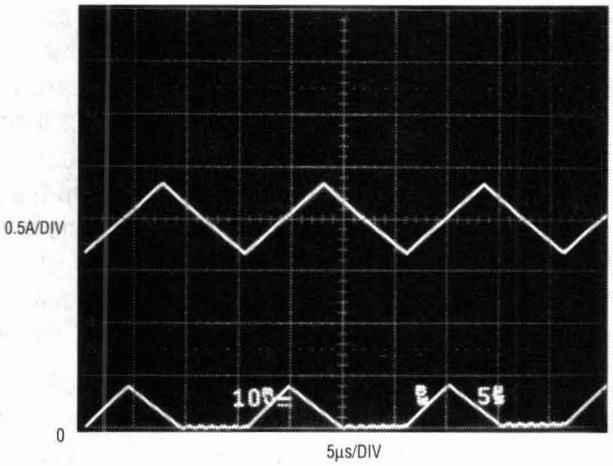

Figure 10. Inductor Current

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Switching Waveforms in Burst Mode

In burst mode, the LT1432 amplifier is converted to a comparator with hysteresis. This causes its V_C pin current drive to be either zero (output low), or full "on" at about 0.8mA (output high). The LT1271 therefore is either driven to full on condition or forced into complete micropower shutdown. This makes a dramatic reduction in quiescent current losses because the switching regulator chip draws supply current only during the relatively short "on" periods. This burst mode results in a battery drain of only 1.2mA with zero output load, even though the nominal quiescent current of the switcher chip is 7mA. This low battery drain is accomplished at the expense of higher output ripple voltage, but the ripple is still well within the normal requirements for logic chips.

Figure 11 shows burst mode output ripple at load currents of 0 (top trace), and 50mA (bottom trace). Ripple amplitude is nominally set by the 100mV hysteresis built into the LT1432, but in most applications, other effects come into play which can significantly modify this value. The first is delay in turning off the switcher. This causes the output to overshoot slightly and therefore increases output ripple. Delay is caused by the compensation capacitors used to maintain a stable loop in the normal mode. Another effect, however, is the ESR of the output capacitor. The surge current from the switcher creates a step across the capacitor ESR which prematurely trips the LT1432 comparator, *reducing* ripple amplitude. A second delay occurs in turning the switcher back on when the output falls below its lower level. This delay is somewhat longer, but because the output normally falls at a much slower rate than it rises, this delay is not significant until output current exceeds 10mA. Falling rate is set by the output capacitor (including any secondary filter capacitor), and the actual load current, $dV_{OUT}/dt = I_{OUT}/C_{OUT}$. The slope in the top traces implies a load current of approximately 2mA. This is the sum of the 1mA output quiescent current of the LT1432 and the 1mA drawn by the V_C pin and shunted through the internal Schottky diode during the switcher "off" period.

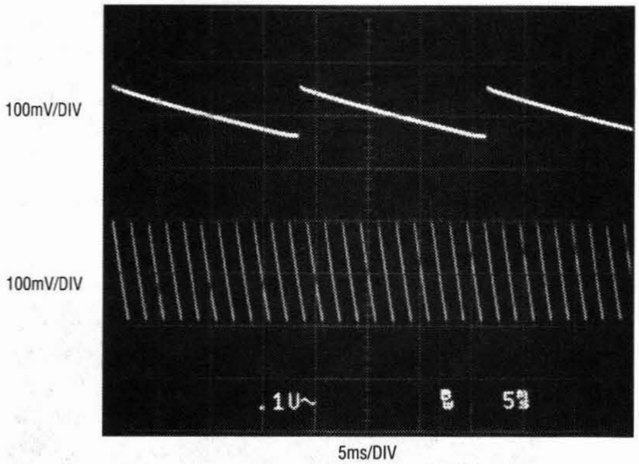

Figure 11. Burst Mode Output Ripple Voltage

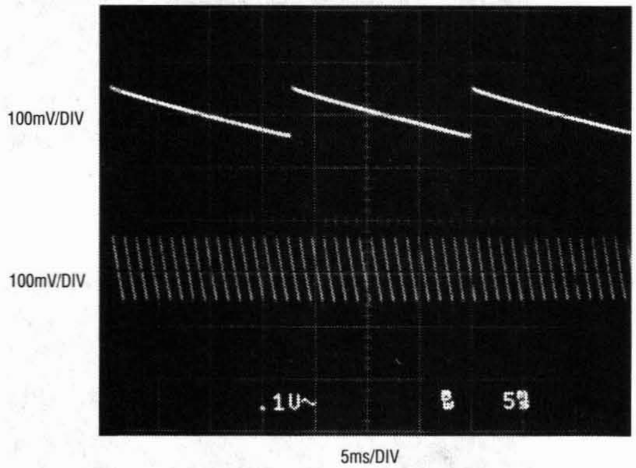

Figure 12. Burst Mode Output Ripple Voltage

The bottom trace at I_{OUT} = 50mA shows increased ripple caused by turn-on delay. Note that ripple frequency has increased from 50Hz to about 600Hz and amplitude has more than doubled. Figure 12 shows the same conditions except that a 47kΩ resistor is connected from the LT1271 V_{IN} pin to the V_C pin to provide more start-up current. These additions reduce ripple amplitude at 50mA load current to a value only slightly higher than the no-load condition.

Although it is difficult to see in Figures 11 and 12, there is a narrow spike on the leading edge of the ripple caused by the burst current and capacitor ESR. Figure 13 shows this spike in more detail, both with and without an output filter.

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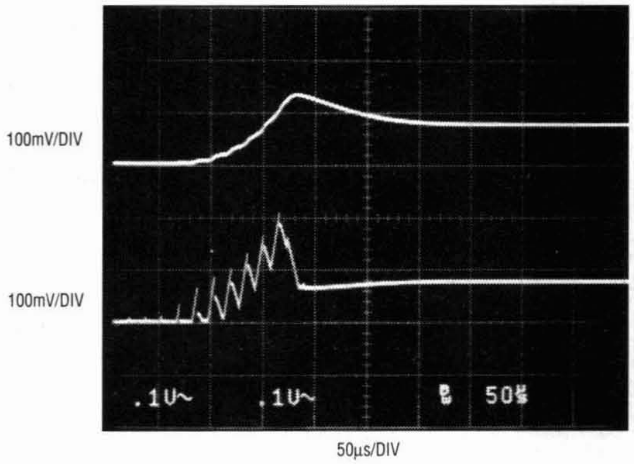

Figure 13

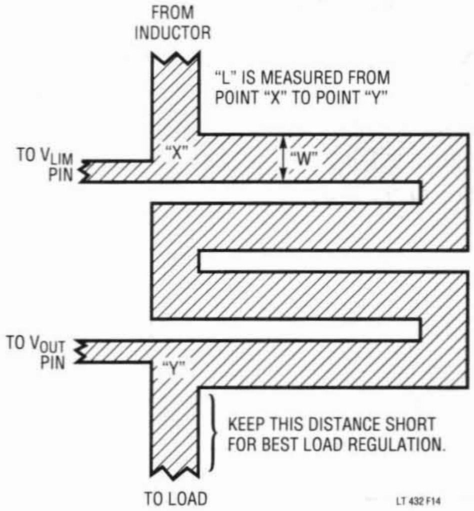
FROM INDUCTOR
"L" IS MEASURED FROM POINT "X" TO POINT "Y"
TO V_{LIM} PIN
"X"
"W"
TO V_{OUT} PIN
"Y"
KEEP THIS DISTANCE SHORT FOR BEST LOAD REGULATION.
TO LOAD
LT 432 F14

Figure 14. PC trace Current Limit Sense Resistor with Kelvin Contacts

Time scale has been expanded to 50µs/DIV. The spike consists of several switching cycles of the LT1271 as shown in the lower trace. In the upper trace, the output filter has smoothed the switching frequency content of the spike, but the actual spike amplitude is only modestly reduced. Increasing the output filter constants from 10µH and 220µF to 20µH and 330µF would eliminate most of the spike.

Current Limiting

The LT1432 has true switching current limit with a sense voltage of 60mV. This low sense voltage is used to maintain high efficiency with normal loads and to make it possible to use the printed circuit board trace material as the sense resistor. The sense resistor value must take ripple current into account because the LT1432 limits on the peak of the inductor ripple current. Errors in the sense resistor must also be allowed for.

$$R_{SENSE} = \frac{V_{SENSE}}{I_{MAX}(1.2)^{*} + \frac{I_{RIP}}{2}}$$

R_{SENSE} = Required sense resistor
V_{SENSE} = 60mV
I_{MAX} = Maximum load current, including any surge longer than 50µs

* 1.2 is a fudge factor for errors in R_{SENSE} and V_{SENSE}.

$$\frac{I_{RIP}}{2} = 1/2 \text{ Peak to Peak Inductor Ripple Current}$$

$$= \frac{V_{OUT}(V_{IN} - V_{OUT})}{2V_{IN}(f)(L)}$$

f = Frequency
L = Inductance
Use V_{IN} maximum

Example: I_{MAX} = 2A, f = 60kHz, maximum V_{IN} = 15V, L = 50µH;

$$\frac{I_{RIP}}{2} = \frac{5(15-5)}{2(15)\left(60E^{3}\right)\left(50E^{-6}\right)} = 0.55A$$

$$R_{SENSE} = \frac{60mV}{2A(1.2) + 0.55A} = 0.02\Omega$$

The formula for R_{SENSE} shows a 1.2 multiplier term in the denominator which makes typical current limit 20% above full load current. This accounts for small errors in the PCB trace resistance. Trace resistance errors are kept to a minimum by using internal traces (on multilayer boards)

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because these traces do not have errors caused by plating operations. The suggested trace width for 1/2oz foil is 0.03" for each 1A of current limit to keep trace temperature rise reasonable. 3A current limit would require the width to be 0.09". 1oz foil can reduce trace width to 0.02" per amp. Inductance in the trace is not critical so the trace can be wound serpentine or any other shape that fits available space. Kelvin connections should be used as shown in Figure 14 to avoid errors due to termination resistance.

The length of the sense resistor trace can be calculated from:

$$\text{Length} = \frac{W(R_{SENSE})}{R_{CU}}\text{Inches}$$

W = width of copper trace (0.03" per amp for 1/2oz copper foil)

R_{CU} = resistivity of PCB trace, expressed as Ω per square. It is found by calculating the resistance of a section of trace with equal length and width. For typical 1/2oz material, R_{CU} is approximately 1mΩ per square. In the example shown above, with width = 2A times 0.03" = 0.06";

$$\text{Length} = \frac{0.06(0.02)}{0.001} = 1.2\text{ Inches}$$

Current limiting maintains true switching action, but power dissipation in the IC switch and catch diode will shift depending on output voltage. At output voltages near the correct regulated value, power will be distributed between switch and the diode according to the usual calculations. Under short circuit conditions, switch duty cycle will drop to a very low value, and power will concentrate in the diode, which will be running at near 100% duty cycle. If continuous shorts must be tolerated, the catch diode must be sized to handle the full current limit value, or foldback current can be used.

Foldback Current Limiting

Foldback current limiting makes the short circuit current limit somewhat lower than the full load current limit to reduce component stress under short circuit conditions. This is shown in Figure 15 with the addition of R3 and R4. The voltage drop across R3 adds to the 60mV current limit

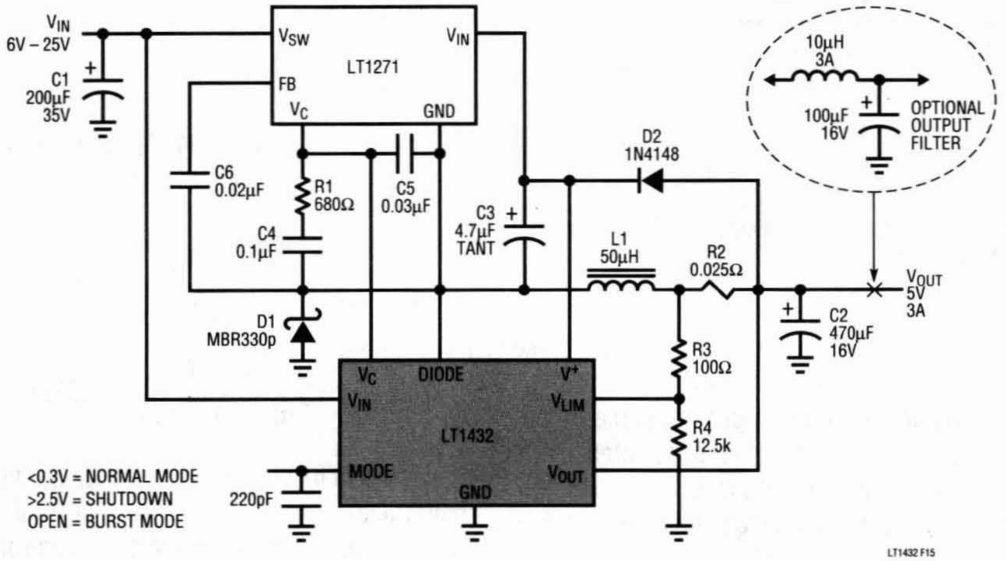
V_IN
6V – 25V
C1
200µF
35V
+
V_SW
LT1271
V_IN
FB
V_C
GND
C6
0.02µF
R1
680Ω
C5
0.03µF
C4
0.1µF
C3
4.7µF
TANT
+
D2
1N4148
L1
50µH
R2
0.025Ω
10µH
3A
100µF
16V
+
OPTIONAL
OUTPUT
FILTER
V_OUT
5V
3A
C2
470µF
16V
+
D1
MBR330p
V_C
DIODE
V+
V_IN
V_LIM
LT1432
MODE
V_OUT
GND
R3
100Ω
R4
12.5k
<0.3V = NORMAL MODE
>2.5V = SHUTDOWN
OPEN = BURST MODE
220pF
LT1432 F15

Figure 15. Adding Foldback Current Limiting

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voltage. This extra sense voltage is set by output voltage and R4 under normal loads, but drops to near zero when the output is shorted.

The 40μA bias current flowing out of the V_{LIM} pin must be accounted for when calculating a value for R4. This current flows through R3, causing a 4mV *decrease* in sense voltage for R3 = 100Ω. The following formulas define current limit conditions:

Current limit at V_{OUT} = 5V

$$= \frac{60\text{mV} - I_B(R3) + (V_{OUT})\left(\frac{R3}{R4}\right) - (R_{SENSE})\left(\frac{I_{RIP}}{2}\right)}{R_{SENSE}}$$

$$\text{Short Circuit Current} = \frac{60\text{mV} - I_B(R3)}{R_{SENSE}}$$

$$R_{SENSE} = \frac{V_{LIM}}{I_{MAX}(1.2)}$$

$$R4 = \frac{V_{OUT}(R3)}{V_S - 60\text{mV} + I_B(R3) + (R_{SENSE})\left(\frac{I_{RIP}}{2}\right)}$$

V_S = Desired full load sense voltage.

I_{MAX} = Peak load current (for any time greater than 50μs)

I_B = V_{LIM} pin bias current (≈40mA)

To maintain high efficiency and avoid any startup problems with loads that have non-linear V/I characteristics, a 100mV (average) sense voltage is suggested for foldback current limiting. The suggested value for R3 is 100Ω. This is a compromise value to keep errors due to V_{LIM} bias current low, and to minimize current drain on the output created by the R3/R4 path. From the previous design example, with I_{MAX} = 2A and $I_{RIP}/2$ = 0.55A, and assuming R3 = 100Ω, V_{LIM} = 100mV:

$$R_{SENSE} = \frac{100\text{mV}}{2\text{A}(1.2)} = 0.042\Omega$$

$$R4 = \frac{5\text{V}(100\Omega)}{100\text{mV} - 60\text{mV} + 100\Omega(40\mu\text{A}) - 0.042(0.55)}$$

$$= 7.45\text{k}\Omega$$

Current limit at V_{OUT} = 5V

$$= \frac{60\text{mV} - 40\mu\text{A}(100\Omega) + 5\text{V}\left(\frac{100}{7.45\text{k}}\right)(0.042)(0.55)}{0.042\Omega}$$

$$= 2.38\text{A}$$

Current limit (output shorted)

$$= \frac{60\text{mV} - 100\Omega(40\mu\text{A})}{0.042\Omega} = 1.33\text{A}$$

Minimum Input Voltage

Minimum input voltage for a buck converter using the LT1432 is actually limited by the IC switcher used with it. There are three factors which contribute to the minimum voltage. At very light loads, the charge pump technique used to provide the floating power for the switcher chip is unable to provide sufficient current. See Figure 16 for the minimum load required as a function of input voltage when operating in the normal mode.

At moderate to heavy loads, switch on-resistance and maximum duty cycle will limit minimum input voltage. Graphs in the Typical Performance Characteristics section show minimum input voltage as a function of load current. At moderate loads, maximum switch duty cycle is the limiting factor. The LT1070 family, operating at 40kHz has a maximum duty cycle of about 94%. The LT1170 family runs at 100kHz and has a maximum duty cycle of 90%. The LT1270 and LT1271 operate at 60kHz with a maximum duty cycle of 92%. The curves were generated using the expected worst case duty cycle for these devices over the commercial operating temperature range (0°C to 100°C junction temperature). Note that the lower frequency devices will operate at lower input voltage because of their higher duty cycle. These devices will require larger inductors, however. (Yet another example of the universal "no free lunch" syndrome).

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At heavy loads, switch on-resistance increases minimum input voltage. With an LT1071 for instance, minimum input is 6.1V at 1A load, but increases to 6.3V at 2A load. If absolute minimum input voltage is needed, use lower frequency devices with higher current rating than is actually needed. The LT1070, for instance, operates down to 6.15V at 2A. Current limit is defined by the LT1432, so higher current switchers used in lower current applications do not degrade performance or reliability.

Minimum Load Current in Normal Mode

There is a minimum load current requirement in normal mode. This is caused by the necessity to "pump" the IC switcher floating power supply capacitor during switch "off" time. This pumping current comes from inductor current, so load current must not be allowed to drop too low, or the floating bias supply for the switcher will collapse. Minimum load current is a function of input voltage as shown in Figure 16.

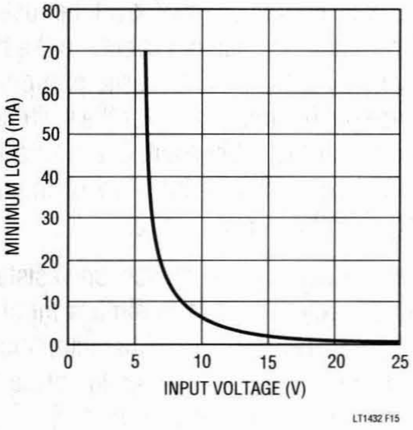

Figure 16. Minimum Normal Mode Load Current

Inductor Selection

Inductor selection would be easy if money and space didn't count. Unfortunately, these two factors usually count the most, and compromises must be made. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive cores such as ferrite, molypermalloy, or KoolMμ. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core loss goes down. Unfortunately, increased inductance requires more turns of wire and therefore copper loss will increase. The trick is to find the smallest inductor whose inductance is high enough to limit core loss, and whose series resistance is low enough to limit copper loss. Historically, inductor manufacturers have a tendency to be ultra conservative when designing inductors, and unless you are very specific about your constraints and requirements, they will more often than not come up with a unit which is 50% larger than the optimum. Part of this is due to manufacturing considerations. The trade-off of core loss and copper loss is optimized by "filling the winding window" with wire, but especially for toroids this can require more expensive winding techniques than the widely used "single layer" design. The lesson here is to spend time with the manufacturer exploring the cost trade-offs of different inductor designs. The following guidelines may be helpful in this regard.

1. For most buck converter applications using the LT1070, LT1170, or LT1270 families of parts at 40kHz to 100kHz, inductor value will be in the range of 25μH to 200μH. The lower values would be used for higher output currents and/or higher frequencies, with higher values used for low output current, low frequency applications. Lower inductance obviously means smaller size, but at some point the core loss will begin to hurt, or the large peak-to-peak inductor currents will cause high output ripple voltage or limit available output current. The following formula is a rough guide for picking an initial inductor value:

$$L = \frac{8}{(I_{MAX})(f)}$$

I_{MAX} = maximum load current, including surges
f = switching frequency

This formula assumes that a switcher IC is selected which has a maximum switch current of 1.5 to 2.5 times maximum load current. For a 2.5A design using the LT1271 at 60kHz, L would calculate to 53μH. This formula is very arbitrary, so do not hesitate to modify the calculated value by as much as 2:1 if the need arises. Keep in mind that all the IC switchers have a peak current rating which is a

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function of duty cycle. Care must be taken to ensure that the sum of output current plus 1/2 inductor p-p ripple current does not exceed the switch current limit at the highest duty cycle (lowest input voltage).

$$\text{Duty Cycle (maximum)} = \frac{V_{OUT} + Vf}{V_{IN(MIN)}}$$

Vf = Diode forward voltage

$$\text{1/2 p-p Ripple Current} = \frac{(V_{OUT})(V_{IN} - V_{OUT})}{2(V_{IN})(f)(L)}$$

(Use minimum V_{IN} +2V)

A 2.5A design using an LT1271 at 60kHz, with a minimum input voltage of 7V and a 50µH inductor, would have a maximum duty cycle of (5 + 0.5)/7 = 79%. 1/2 p-p ripple current would be:

$$\frac{(5)(7+2-5)}{2(7+2)\left(60E^{3}\right)\left(50E^{-6}\right)} = 0.37A$$

Output current plus 1/2 ripple current = 2.5 + 0.37 = 2.9A. The switch current rating for the LT1271 is shown on the data sheet as 4A for duty cycle below 50% and 2.67 (2–DC) for duty cycles greater than 50%. With DC = 79%, switch current rating would be 2.67 (2 – 0.79) = 3.23A, so this meets the guidelines. It should be noted that if normal running load current conditions result in switch currents that are close to the maximum switch ratings, efficiency will drop. Switch voltage loss at maximum switch current rating is typically 0.7V, and this represents a significant loss, especially at low input voltages. In most laptop computer designs, surge currents from hard or floppy disks require an oversized switcher, so normal running currents are typically less than one half rated switch current and efficiency is high except during the short surge periods.

2. Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. The downside is that the finished unit will almost surely be larger than a molypermalloy toroid design because of the basic topological limitations of the ferrite/bobbin arrangement. Newer low-profile ferrite cores are even less space efficient than older configurations. Cost may also be higher. Ferrite core material saturates "hard," which means that inductance collapses abruptly when peak design current is exceeded. This may be a problem in current limit or if peak load requirements are not well characterized.

3. Molypermalloy (from Magnetics, Inc.) is a very good, low loss core material for toroids, but it is (naturally) rather expensive. A reasonable substitute is KoolMµ (same manufacturer). Toroids are very space efficient, especially when you can convince the manufacturer to use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. Newer designs for surface mount are available (Coiltronics), which are nested in a ring that does not increase the height significantly.

Catch Diode

The catch diode carries load current only during switch "off" time. Its average current is therefore dependent on switch duty cycle. At high input voltages, the diode conducts most of the time, and as V_{IN} approaches V_{OUT}, it conducts only a small fraction of the time. The current rating of the diode should be higher than maximum load current for two reasons. First, conservative diode current improves efficiency because the diode forward voltage is lower, and second, short circuit conditions result in near 100% diode duty cycle at currents higher than full load unless some form of foldback current limiting is used. Schottky diodes are a must for their low forward drop and fast switching times.

Maximum diode reverse voltage is equal to maximum input voltage. However, do not over-specify the diode for breakdown voltage. Schottky diodes are made with lighter silicon doping as breakdown ratings increase. This gives higher forward voltage and degrades regulator efficiency. An MBR350 (3A, 50V) has almost 100mV higher forward voltage than the MBR330 (3A, 30V).

Diode current ratings are predicated on proper thermal mounting techniques. Check the manufacturers assumptions carefully before assuming that a 3A diode is actually capable of carrying 3A continuously. Pad size may have to be larger than normal to meet the mounting requirements for full current capability.

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Input Supply Bypass Capacitor

The input capacitor on a step-down (buck) switching regulator must handle switching currents with a peak-to-peak amplitude at least equal to the output current. The RMS value of capacitor current is approximately equal to:

$$I_{RMS} = \frac{I_{OUT}\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where I_{RMS} is equal to $I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations from $V_{IN}/2$ do not offer much relief. A 2A output (transient loads can be ignored if they last less than 30 seconds) therefore requires an input capacitor with a 1A ripple current rating. *Don't cheat*, and read the output capacitor section for details on ripple current! The input capacitor may well be the largest component in the switching regulator. Spend time playing with aspect ratios of various capacitor families and don't hesitate to parallel several units to achieve a low profile.

Output Voltage Ripple

Output voltage ripple is determined by the main inductor value, switching frequency, input voltage, and the ESR (effective series resistance) of the output capacitor. The following formula assumes a load current high enough to establish continuous current in the inductor.

Output Ripple Voltage = $V_{p\text{-}p}$

$$= \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)(ESR)}{V_{IN}(f)(L)} V_{p\text{-}p}$$

With $V_{IN} = 12V$, ESR = 0.05Ω, f = 60kHz, and L = 50μH

$$V_{p\text{-}p} = \frac{5(12-5)(0.05)}{(12)\left(60E^3\right)\left(50E^{-6}\right)} = 48.6mV_{p\text{-}p}$$

If low output ripple voltage is a requirement, larger output capacitors and/or inductors may not be the answer. An output filter can be added at modest cost which will attenuate ripple much more space-effectively than an oversized output capacitor or inductor. The thing to keep in mind when adding an output filter is that if the filter capacitor is small, it may allow large output perturbations if large load transients occur. This effect should be carefully checked before finalizing any filter design. For more details on output filters, consult Application Notes 19 and 44.

Output Capacitor

To avoid overheating, the output capacitor must be large enough to handle the ripple current generated by the main inductor. It must also have low enough effective series resistance (ESR) to meet output ripple voltage requirements. RMS ripple current in the output capacitor is given by:

$$I_{RIPPLE(RMS)} = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{3.5V_{IN}(f)(L)}$$

(use maximum V_{IN})

For $V_{IN} = 15V$, f = 60kHz, L = 50μH,

$$I_{RIPPLE(RMS)} = \frac{5(15-5)}{3.5(15)\left(60E^3\right)\left(50E^{-6}\right)} = 0.32A_{RMS}$$

Ripple current ratings are specified on capacitors intended for switching applications, but the number is subject to much manipulation. The high frequency number is greater than the low frequency value, and theoretically one can multiply the ripple number by significant amounts at temperatures below the typical 85°C or 105°C rating point. The problem is that the ripple ratings are already unrealistically high at the rated temperature because they are typically based on a 2000 hour life. I assume this is an unacceptable lifetime number, so the ripple rating must be *reduced* to extend life. The net result of all this fiddling with the numbers is generally a headache, but it is probably conservative to use the stated high frequency rating at temperatures below 60°C for a 105°C capacitor, and assume that the unit will last at least 50,000 hours. Remember to factor in *actual* operating time at elevated temperatures. Laptop computers, for instance, might be expected to operate no more than four hours a day on

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average, so a ten year life is only 15,000 hours. The manufacturer should be consulted for a final blessing. See Application Note 46 for specific formulas for calculating the life time or allowed ripple current in capacitors.

The reason for all this attention to ripple rating is that everyone is in a size squeeze, and the temptation is to use the smallest possible components. Do not cheat here folks, or you may be faced with costly field failures.

ESR on the output capacitor determines output voltage ripple, so this is also of much concern. Mother Nature has decreed that for a given capacitor technology, ESR is a direct function of the *volume* of the capacitor. In other words, if you want low ESR you must consume *space*. This is quickly confirmed by scanning the ESR numbers for a wide range of capacitor values and voltage ratings within a given family of capacitors. It is immediately obvious that can size determines ESR, not capacitance, or voltage rating. The only way to cheat on this limitation is to find the best family of capacitors. Manufacturers such as Nichicon, Chemicon, and Sprague should be checked. Sanyo makes a very low ESR capacitor type know as OSCON, utilizing a semiconductor dielectric. Its major disadvantage is somewhat higher price, and a tendency to make regulator feedback loops unstable because of its extremely low ESR. Most switching regulator loops depend to some extent on the output capacitor ESR for a phase lead!

Output Filters

Output ripple voltage at the switching frequency is a fact of life with switching regulators. Everyone knows that this ripple must be held below some level to guarantee that it does not affect system performance. The question is, what is that level? For sensitive analog systems with wide bandwidths, supply ripple may have to be a 1mV or less. Digital systems can often tolerate $400mV_{P-P}$ ripple with no effect on performance. In most of these digital applications of the LT1432 as a buck converter, an output filter is not needed because output ripple is normally in the 25mV to $100mV_{P-P}$ range without a filter. Note that burst mode ripple is at low frequencies where small output filters are not effective. The decision to add an output filter does allow the main filter capacitor to get smaller, so the overall board space may not increase prohibitively. See the discussion of waveforms for load transient response implications when adding a filter.

If modest reductions in output ripple are required, one can increase the size of the main inductor and/or the output capacitor. Buck converters are easier than other types because the main inductor acts as a filter element. The square wave voltage is converted to a triangular current before being fed to the output capacitor. Actually, at switching frequencies, the output capacitor is resistive and output ripple voltage is determined not by the capacitor value in µF, but rather by the capacitor effective series resistance (ESR). This parameter is determined by capacitor volume within any given family, so to get ESR down, one must still use a "bigger" capacitor. The problem is that often the main inductor/capacitor becomes physically too large if low output ripple is needed. Inverters, such as the positive to negative converter, tend to have much higher output ripple voltage because the main inductor is not a filter element – it simply acts as an energy storage device for shuttling essentially square wave currents from input to output. Unlike the buck converter, these currents can be much higher in amplitude than the output current.

An output filter of very modest size can reduce normal mode output ripple voltage by a factor of ten or more. The formula for filter attenuation in buck converters and inverters is shown below.

$$\text{Attenuation} = \frac{ESR}{8(L)(f)} \qquad \text{(BUCK CONVERTER)}$$

$$\text{Attenuation} = \frac{(ESR)}{4(L)(f)} \qquad \text{(INVERTER)}$$

(The factor "4" is an approximation assuming worst case duty cycle of 50%)

A 10µH, 100µF (ESR = 0.4Ω) filter on a buck converter using a 60kHz LT1271 will give an attenuation of:

$$\frac{0.4}{8\left(10E^{-6}\right)\left(60E^{3}\right)} = 0.083$$

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100mV output ripple on the main capacitor will be reduced to (0.083)(100) = 8.3mV at the output of the filter.

Layout Considerations

Although buck converters are fairly tolerant with regard to layout issues, there are still several important things to keep in mind. Most of these revolve around spikes created by switching high currents at high speeds. If 3A of current is switched in 30ns, the rate of change of current is 10E8 A/S. Voltage generated across wires will be equal to this rate multiplied by the approximate 20nH per inch of wire. This calculates to 2V per inch of wire or trace!! Needless to say, connections should be kept short if the circuitry connected to these lines is sensitive to narrow spikes.

1. The input bypass capacitor must be kept as close to the switcher IC as possible, and its ground return must go directly to the ground plane with no other component grounds tied to it. The output capacitor should also connect directly to the ground plane.

2. The frequency compensation components shown in Figure 1 (R1 + C4, and C5) and the feedback pin bypass capacitor (C6) are shown connected to the floating ground pin of the IC switcher. This ground pin is also the high current path for the switch. To avoid differential spikes being coupled into the V_C and FB pins, these components must tie together and then be connected through a direct trace to the IC switcher ground pin. No other components should be connected anywhere on this trace and the trace area should be minimized. A separate wide trace must be used to connect the IC ground pin to the catch diode and inductor. Smaller traces can be used to connect the floating supply capacitor (C3) and the diode pin of the LT1432 to the wide trace reasonably close to the IC ground pin.

3. Traces which carry high current must be sized correctly. To limit temperature rise to 20°C, using 1oz copper, the trace width must be 20 mils for each ampere of current. 1/2oz copper requires 30 mils/A. These high current paths include the IC switcher ground pin and switch pin, the inductor, the catch diode, the current limit sense resistor, and the input bypass capacitor. If vias are used to connect these components on multiple layer boards, their maximum rated current must also be considered. For currents greater than 1A, multiple vias may have to be used.

4. The catch diode has large square wave currents flowing in it. Connect the anode directly to the ground plane and the cathode directly to the IC ground pin.

5. The ground pin of the LT1432 is the reference point for output voltage. It should be routed separately to power ground as near to the load as is reasonable.

Transient Response

Load transient response may be important in portable applications where parts of the system are switched on and off to save power. There are two types of problems that differ by time scale. The first occurs very rapidly and is caused by the surge current created in charging the supply bypass capacitors on the switched load. This can be a very serious problem if large (>0.1μF) capacitors must be charged. No regulator can respond fast enough to handle the surge if the load switch on-resistance is low and it is driven quickly. The solution here is to limit the rise time of the switch drive so that the load rise time is limited to approximately $25 \times C_{LOAD}$. A 1μF load capacitor would require a 25μs load rise time, etc. This limits surge to about 200mA. This time frame is still too quick for a switching regulator to adjust to, but the surge is limited to a low enough value that the output capacitor will attenuate the surge voltage to an acceptable level.

A second problem is the change in DC load current. Switching regulators take many switching cycles to respond to sudden output load changes. During this time, the output shifts by an amount equal to Δload (ESR + t/C), where ESR is the series resistance of the output capacitor, t is the time for the regulator to shift output current, and C is the output capacitor value. For example, if the load change is 0.5A, ESR is 0.1Ω, t is 30μs, and C = 390μF, the shift in output voltage would be:

$$\Delta V_{OUT} = 0.5A\left(0.1\Omega + \frac{30\mu s}{390\mu F}\right) = 0.088V$$

APPLICATIONS INFORMATION

Figure 17 shows the effect of a 500mA transient load (0.3A to 0.8A) on the LT1432, both with and without an output filter. The top trace with no filter shows about a 60mV deviation with a settling time of 300μs. Astute switching regulator designers may notice the lack of switching ripple in this trace. To make a clean display the actual trace was fed through a one pole filter with 16μs time constant to eliminate most of the switching ripple. This had very little effect on the shape or amplitude of the response waveform (you'll have to trust me on this one). In the middle trace, an output filter of 10μH and 200μF was added to the regulator to achieve very low output ripple. The load transient response is obviously degraded because the second filter capacitor, following normal design practice, is somewhat smaller than the main output capacitor, and therefore also has higher ESR. Note the slight ringing caused by the "Q" of the output filter. Calculated ringing frequency is $1/(2\pi\sqrt{LC}) = 3.4kHz$. Also note the small step in DC level between the two load conditions on the filtered output. To maintain good loop stability, the added filter is left "outside" the feedback loop. Therefore, the DC resistance of the 10μH inductor will add to load regulation. The 10mV step implies a resistance of 10mV/0.5A = 0.02Ω. The message in all this is to be careful when adding output filters if transient load response or load regulation is critical. The second filter capacitor may have to be as large as the main filter capacitor.

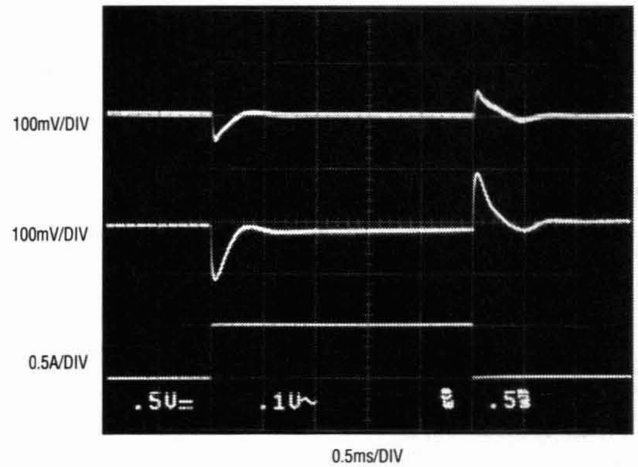


Figure 17

Mode Pin Drive

The mode pin defines operating conditions for the LT1432. A low state programs the IC to operate in "normal" mode as a constant frequency, current mode, buck converter. Floating the pin converts the internal error amplifier to a comparator which puts the LT1432 into a low-power "burst" mode. In this mode, the pin assumes an open circuit voltage of approximately 1V. To ensure stable operation, current into or out of the pin must be limited to 2μA. If the pin is routed near any switching or logic signals it should be bypassed with a 200pF capacitor to avoid pickup.

Driving the mode pin high causes the LT1432 to go into complete shutdown. An internal resistor limits mode pin current to about 15μA at 5V. A 7V zener diode is also in parallel with the pin, so input voltages higher than 6.5V must be externally limited with a resistor. The current/voltage characteristics of the mode pin are shown in Typical Performance Characteristics. Note that the drive signal must sink about 30μA when pulling the mode pin to its worst case low threshold of 0.6V. This should not be a problem for any standard open drain or three-state output.

If all three states are desired and a three-state drive is not available, the circuit shown in Figure 18 can be used. Two separate logic inputs are used. Both low will allow the mode pin to float for burst mode. "A" high, "B" low will generate shutdown, and "B" high, "A" low forces normal mode operation. Both high will also force normal mode operation, but this is not an intended state and R1 is included to limit overload of "A" if this occurs. C1 is suggested if the mode pin line can pick up capacitively coupled stray switching or logic signals.

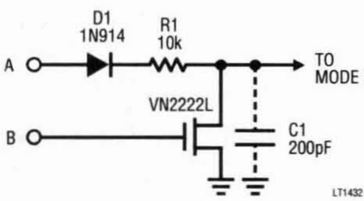


Figure 18. Two Input Mode Drive

APPLICATIONS INFORMATION

Internal Restart Sequence

At very light load currents (>10mA), coupled with low input voltages (<8.5V), it is possible for the basic architecture used by the LT1432 to assume a stable output state of less than 5V. To avoid this possibility, the LT1432 has an internal timer which applies a temporary 20mA load to the output if the output is below its regulated value for more than 1.8ms. This action is normally transparent to the user.

Auxiliary Outputs – "Free" Extra Voltages

Semi-regulated secondary outputs may be added to buck converters by adding additional windings to the main inductor. These outputs will have a typical regulation of 5 to 10%, but have one very important limitation. *The total output power of the auxiliary windings is limited by the output power of the main output.* If this limit is exceeded, the auxiliary winding voltages will begin to collapse, although the main 5V output is unaffected by collapse of the secondary. The auxiliary power available is also a function of input voltage. At higher input voltages significantly more power is available.

Figure 19 shows the ratio of maximum auxiliary power to main output power, versus input voltage. The auxiliary output was loaded until its output voltage dropped 10%. For applications which push the limit of theoretically available current, care should be used in winding the inductor. The effects of leakage inductance and series resistance are magnified at low input voltage where auxiliary winding currents are many times DC load current. Also, be aware that output voltage ripple on the 5V main output can increase significantly when the auxiliary output is heavily loaded. The inductor is acting partially like a transformer, so the AC current delivered to the 5V output capacitor increases in amplitude and shifts from a tri-wave to a trapezoid with much faster edges.

A typical example would be a +5V buck converter with a minimum load of 500mA. Output power is 5V × 0.5A = 2.5W. Maximum power from the auxiliary windings would be 1.25W for input voltages of 9V and above. If we assume a low dropout linear regulator on the auxiliary output, with a regulated output voltage of minus 5V, the auxiliary winding output would have to be about minus 7V. Maximum output current from the 7V output would be 1.25W/7V = 178mA. Note that the power restriction is the *total* for all auxiliary outputs.

The formula to calculate turns ratio for the auxiliary windings versus main winding is simple:

$$N_{AUX} = \frac{N_{MAIN}\left[V_{AUX} + \left(V_{DO} = 2V\right) + V_{DA}\right]}{5V + V_D}$$

N_{MAIN} = Number of turns on main inductor winding

N_{AUX} = Number of turns on auxiliary winding

V_{DA} = Auxiliary diode forward voltage

V_D = Main 5V catch diode forward voltage

V_{DO} = Allowance for regulation of auxiliary winding and dropout voltage of low-dropout linear regulator used on auxiliary winding. Set equal to zero if no regulator is used.

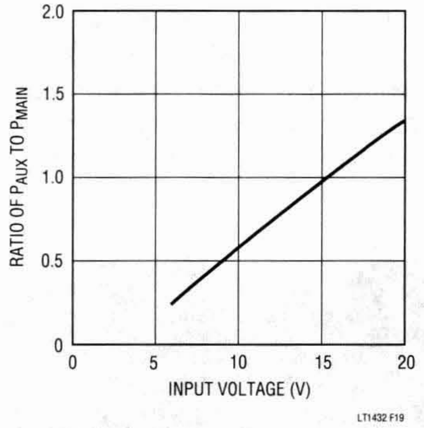


Figure 19. Auxiliary Power vs 5V Power

It is not necessary to use a linear regulator on the auxiliary winding if 5 to 10% regulation is adequate. Line regulation will be fairly good, but variations in auxiliary voltage will occur with load changes on either the auxiliary winding or the 5V output. For relatively constant loads, regulation will be significantly better.

APPLICATIONS INFORMATION

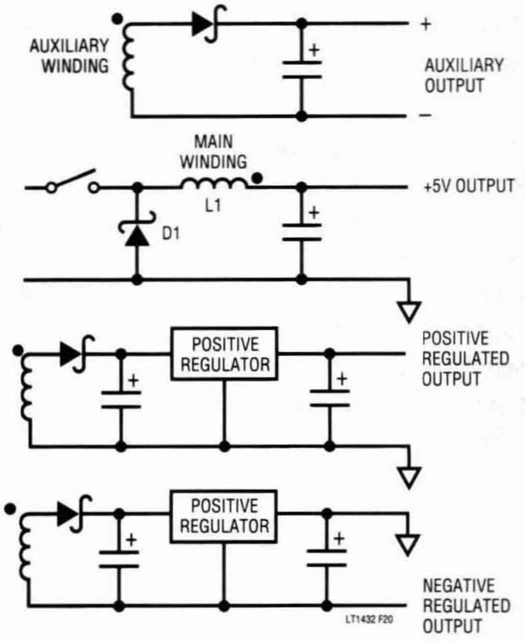


Figure 20

Figure 20 shows how to connect the auxiliary windings. Dots indicate winding polarity. Pay attention here -- history shows that with a 50% chance of connecting up the auxiliary correctly when you ignore the dots, in actual practice you will be wrong 90% of the time.

The floating output can have either end grounded, depending on the need for a positive or negative output. Also shown are the connections for both positive and negative outputs using a linear regulator. Note that the two circuits are identical! The floating auxiliary winding allows the use of a positive low-dropout regulator for negative outputs. These positive regulators are more readily available, especially at lower current levels.

There is a way to "cheat" somewhat on auxiliary power for positive outputs higher than the 5V main output. The auxiliary winding return can be connected to the 5V output. This reduces the winding voltage so that more current is available, and at the same time it actually adds a load to the 5V output to bootstrap itself. Figure 21 shows maximum current out of a 14V auxiliary (used to power a 12V linear regulator) connected in this fashion. The auxiliary winding voltage is actually 9V. Note that for lighter 5V loads, there is an inflection point in the curves at about 11V. That is because theoretically the bootstrapping effect should allow one to draw *unlimited power* from the auxiliary winding when duty cycle exceeds 50%. The actual available current above 50% duty cycle is limited by parasitic losses. At high 5V loads, the inflection disappears for the same reason. The curves asymptotically approach 1 amp at high input voltage because the criteria used to generate the curves was a drop in auxiliary output voltage to 13.5V, and again parasitic resistance limits output current.

Auxiliary windings deliver current in triangular or quasi-square waves only during switch off time. Therefore the amplitude of these pulses will be somewhat higher than the DC auxiliary load current, especially at low input voltage. This means that in the "stacked" connection, ripple voltage on the 5V output will increase with auxiliary load current.

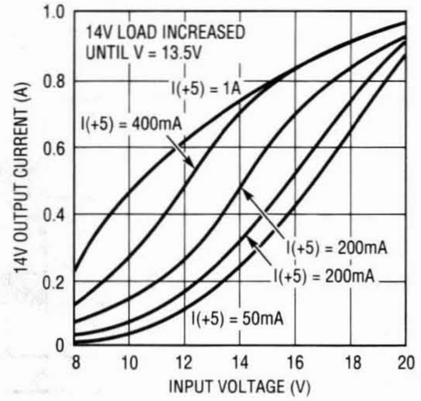


Figure 21

POSITIVE TO NEGATIVE CONVERTER

The circuit in Figure 22 will convert a variable positive input voltage to a regulated –5V output. By selecting different members of the LT1070 family, this basic design can provide up to 6A output current at high input voltages, and up to 3A with a five volt input supply. As shown using an LT1271, maximum load current has been reduced to 1A by utilizing the current limit circuit in the LT1432. Unlike a positive buck converter, it is not possible to sense output current directly. Instead, switch/inductor current is sensed. This would normally result in a DC output current limit value that changes considerably with input voltage, but the addition of R2 and R3 alters peak current limit as a function of input voltage to correct for this effect. Maximum load current and short circuit current are shown as a function of input voltage in Figure 23. A 0.02Ω sense resistor was used, so other values of current limit can be scaled from this value.

This circuit uses the same basic connections between the LT1432 and the LT1271 as the buck converter. The difference is in the way power flows in the catch diode, inductor, and switch. In a buck converter, current flows simultaneously in the switch, inductor, and output. This makes maximum output current approximately equal to maximum switch current. In inverting designs, current delivered to the output is zero during switch on-time. The switch allows current to flow directly from the input supply through the inductor to ground. At switch turn-off, induc-

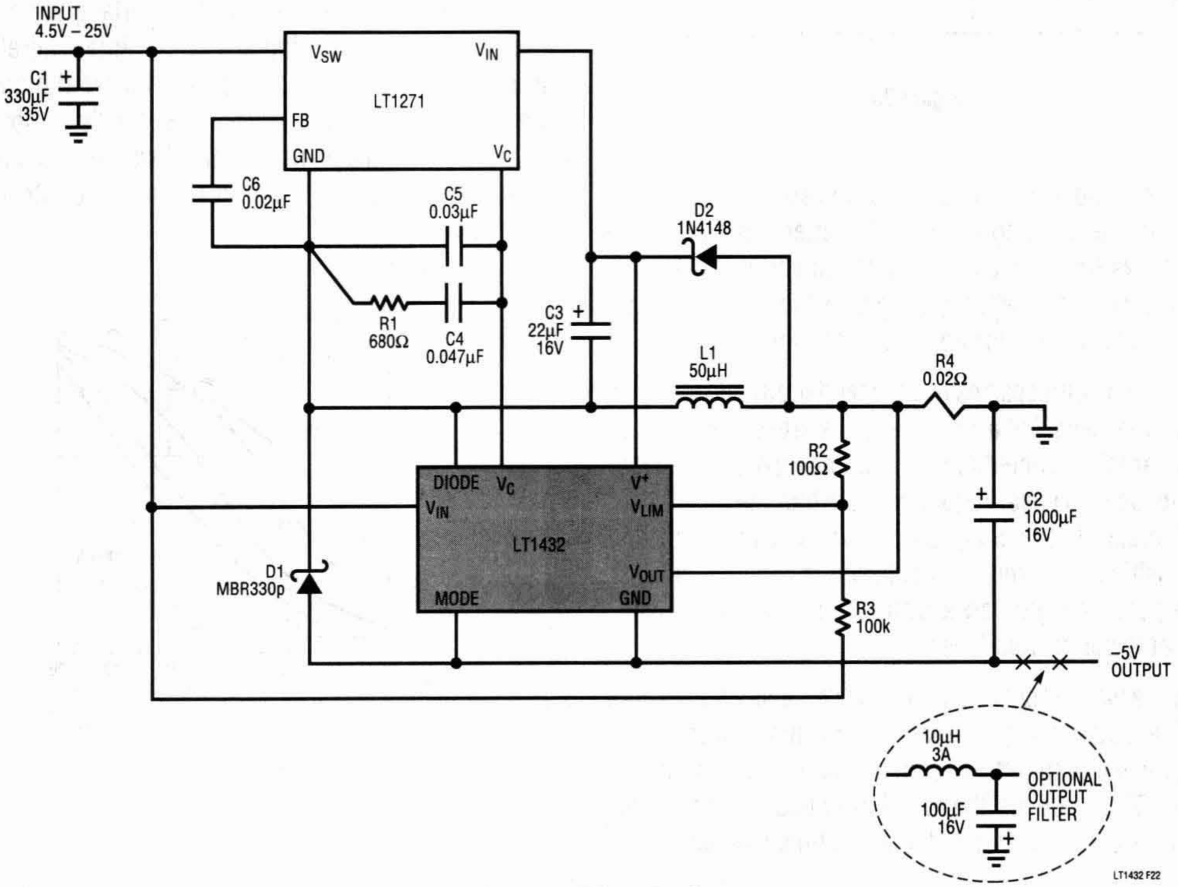

INPUT
4.5V – 25V
C1
330μF
35V
V_{SW}
V_{IN}
LT1271
FB
GND
V_C
C6
0.02μF
C5
0.03μF
R1
680Ω
C4
0.047μF
C3
22μF
16V
D2
1N4148
L1
50μH
R4
0.02Ω
R2
100Ω
DIODE
V_C
V^+
V_{IN}
V_{LIM}
LT1432
V_{OUT}
MODE
GND
D1
MBR330p
R3
100k
C2
1000μF
16V
–5V
OUTPUT
10μH
3A
100μF
16V
OPTIONAL
OUTPUT
FILTER
LT1432 F22

Figure 22. Positive-to-Negative Converter

POSITIVE TO NEGATIVE CONVERTER

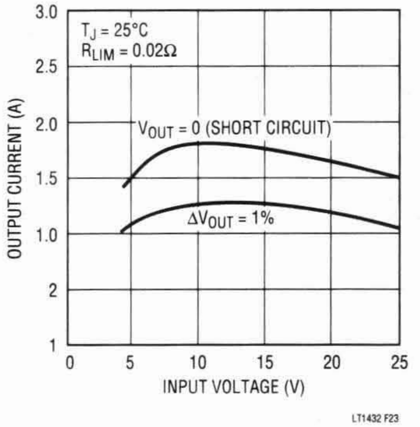


Figure 23. Positive-to-Negative Converter Output Current

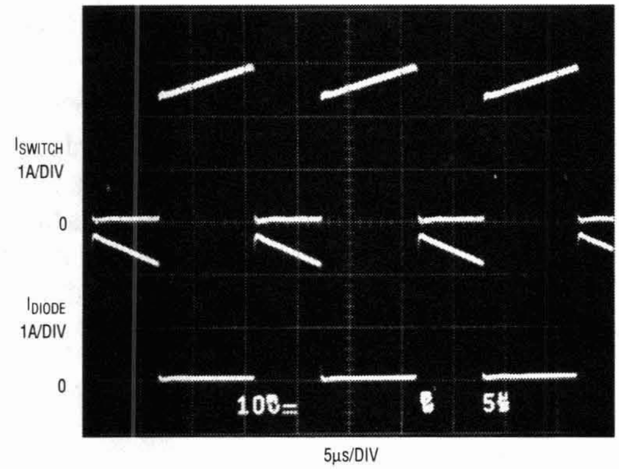


Figure 24. Positive-to-Negative Converter Switch and Diode Current

tor current is diverted through the catch diode to the output. Figure 24 shows switch current (1A/DIV) with the upper waveform, and catch diode current (which is delivered to the output) in the lower waveform, with a +5V input and 1A load. Note that switch, inductor, and diode currents are much higher than output current as required by the fact that current is delivered to the output during only part of a switch cycle. An approximate formula for peak switch current required in an inverting design is:

$$I_{SW(PEAK)} = I_{OUT}\left(1+\frac{V_{OUT}+V_F}{V_{IN}-I_{OUT}(R_{SW})\dfrac{(V_{IN}+V_{OUT})}{V_{IN}}}\right)+\frac{V_{IN}(V_{OUT})}{2(L)(f)(V_{IN}+V_{OUT})}$$

V_F = Forward voltage of catch diode

R_{SW} = Switch on-resistance

L = Inductor value

f = Switching frequency

If V_{IN} is 4.7V (minimum),

$V_F = 0.4V$, $R_{SW} = 0.25\Omega$,

$L = 50\mu H$, $f = 60kHz$, and $I_{OUT} = 1A$;

$$I_{SW(PEAK)} = 1\left(1+\frac{5+0.4}{4.7-1(0.25)\dfrac{(4.7+5)}{4.7}}\right)+\frac{4.75(5)}{2\left(50E^{-6}\right)\left(60E^{3}\right)(4.75+5)}$$

$$= 2.29 + 0.4 = 2.69A$$

The first term (2.29A) represents the minimum switch current required if the inductor were infinitely large. A finite inductor value requires additional switch current. The 0.4A represents one-half the peak-to-peak inductor ripple current. The end result is that peak switch current is almost three times output load current. This multiplier drops rapidly at higher input voltages, so worst case is calculated at lower input voltage.

Figure 25 shows the efficiency of this converter. At higher input voltages and modest output currents efficiency hovers around 85%, quite good for a 5V output inverter. Low input voltage reduces efficiency because of increased currents in the switch, catch diode, and inductor. High input voltage and low output current also show lower efficiency due to quiescent currents in the ICs. Note that the efficiency is actually significantly improved in this regard over a more conventional design because the

POSITIVE TO NEGATIVE CONVERTER

LT1271 operates from a constant 5V supply voltage rather than the high input voltage.

Output voltage ripple in an inverter can be much higher than a buck converter because current is delivered to the output capacitor in high amplitude square waves rather than a DC level with superimposed tri-wave. C2 is therefore somewhat larger than in a buck design. Also C2 must be rated to handle the large RMS current pulses fed into it. This RMS current is approximately equal to:

$$I_{OUT}\left(\sqrt{\frac{V_{OUT}}{V_{IN}}}\right)$$

For 1A output current, with 5V input, this computes to $1A_{RMS}$ in the output capacitor. A small additional output filter would reduce output ripple voltage, but it does not change the current rating requirement for the main output capacitor. The reader is referred to a switching regulator CAD program (SwitcherCAD) supplied by LTC for further insight into converters. It is suggested that the reader fool the program by asking for a negative input, positive output design. It will then select the LT1070 family of ICs which normally are not used in positive to negative converters. Efficiency calculations will be somewhat in error at higher input voltages because the program assumes full input voltage across the IC. Later versions of SwitcherCAD will have a special section for this particular design.

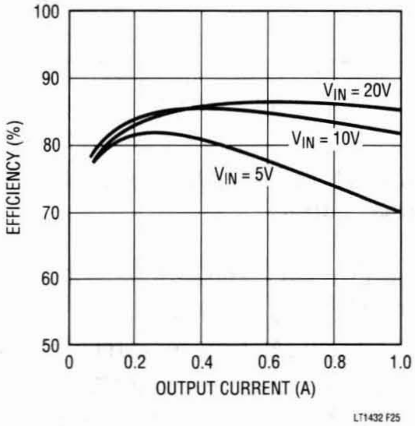
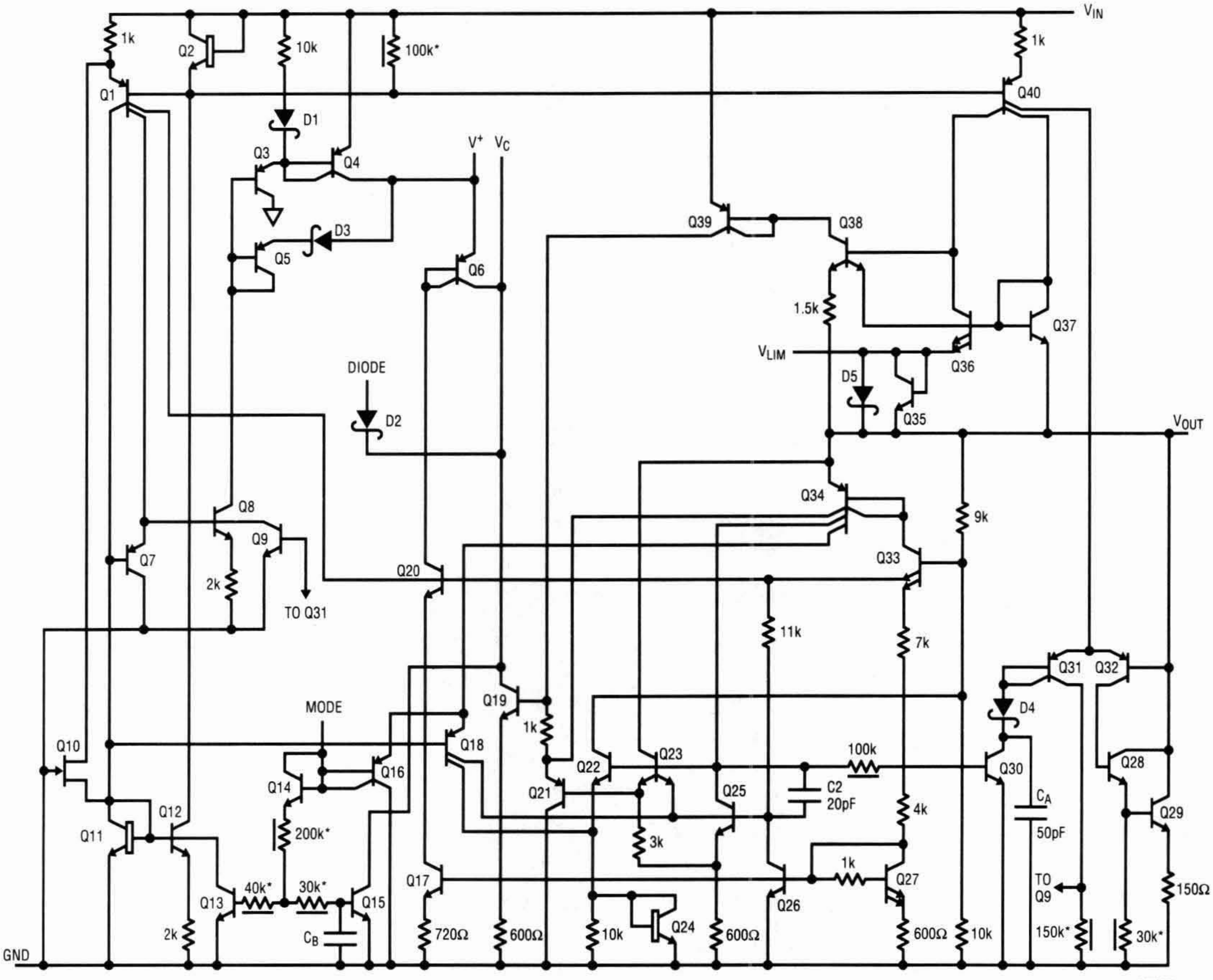


Figure 25. Positive-to-Negative Converter Efficiency

SCHEMATIC DIAGRAM



V_{IN}
1k
Q2
10k
100k*
1k
Q1
Q40
D1
Q3
Q4
V^+
V_C
D3
Q5
Q6
Q39
Q38
1.5k
Q37
V_{LIM}
Q36
D5
Q35
DIODE
D2
V_{OUT}
Q34
9k
Q8
Q9
Q7
2k
TO Q31
Q20
Q33
11k
7k
Q31
Q32
MODE
Q19
D4
Q10
1k
Q18
Q16
Q22
Q23
100k
Q14
Q21
Q25
C2
20pF
Q30
Q28
C_A
Q11
Q12
200k*
3k
4k
50pF
Q29
1k
Q27
Q13
40k*
30k*
Q15
Q17
Q26
TO
Q9
150Ω
2k
C_B
720Ω
600Ω
10k
Q24
600Ω
600Ω
10k
150k*
30k*
GND
LT1432 F26

* —— INDICATES PINCH RESISTOR

NOTES

SECTION 4—POWER PRODUCTS

SWITCHING REGULATORS

LT1073, Micropower DC-DC Converter Adjustable and Fixed 5V, 12V 4-174
LT1074/LT1076, Step-Down Switching Regulator 4-193
LT1076-5, 5V Step-Down Switching Regulator 4-208
LT1082, 1A High Voltage High Efficiency Switching Regulator 13-29
LT1103/LT1105, Off-Line Switching Regulator 4-211
LT1108, Micropower DC-DC Converter Adjustable and Fixed 5V, 12V 13-37
LT1109, Flash Memory Vpp Generator/Low Cost DC-to-DC Converter 4-238
LT1109A, Micropower Low Cost DC-to-DC Converter Adjustable and Fixed 5V, 12V 13-41
LT1110, Micropower DC-DC Converter Adjustable and Fixed 5V, 12V, High Frequency 4-245
LT1111, Micropower DC-to-DC Converter Adjustable and Fixed 5V, 12V, High Frequency 4-260
LT1129-2.85, LT1129-3.3, LT1129-5, 500mA Low Iq Low Dropout Regulator 13-51
LT1173, Micropower DC-DC Converter Adjustable and Fixed 5V, 12V 4-275
LT1270/LT1270A, 8A and 10A High Efficiency Switching Regulators 4-290
LT1271, 4A High Efficiency Switching Regulator 13-88

LT1073

Micropower DC-DC Converter Adjustable and Fixed 5V, 12V

FEATURES

- No Design Required
- Operates at Supply Voltages From 1.0V to 30V
- Consumes Only 95µA Supply Current
- Works in Step-Up or Step-Down Mode
- Only Three External Off-the-Shelf Components Required
- Low-Battery Detector Comparator On-Chip
- User-Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space-Saving 8-Pin MiniDIP or SO8 Package

APPLICATIONS

- Pagers
- Cameras
- Single-Cell to 5V Converters
- Battery Backup Supplies
- Laptop and Palmtop Computers
- Cellular Telephones
- Portable Instruments
- 4mA-20mA Loop Powered Instruments
- Hand-Held Inventory Computers
- Battery-Powered α, β, γ Particle Detectors

DESCRIPTION

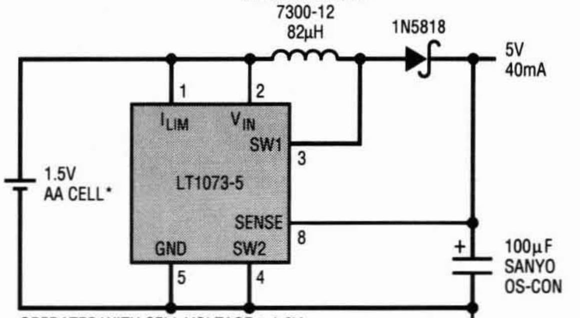
The LT1073 is a versatile micropower DC-DC converter. The device requires only three external components to deliver a fixed output of 5V or 12V. The very low minimum supply voltage of 1.0V allows the use of the LT1073 in applications where the primary power source is a single cell. An on-chip auxiliary gain block can function as a low-battery detector or linear post-regulator.

Average current drain of the LT1073-5 used as shown in the Typical Application circuit below is just 135µA unloaded, making it ideal for applications where long battery life is important. The circuit shown can deliver 5V at 40mA from an input as low as 1.25V, and 5V at 10mA from a 1.00V input.

The device can easily be configured as a step-up or step-down converter, although for most step-down applications or input sources greater than 3V, the LT1173 is recommended. Switch current limiting is user-adjustable by adding a single external resistor. Unique reverse-battery protection circuitry limits reverse current to safe, non-destructive levels at reverse supply voltages up to 1.6V.

TYPICAL APPLICATION

Single-Cell to 5V Converter

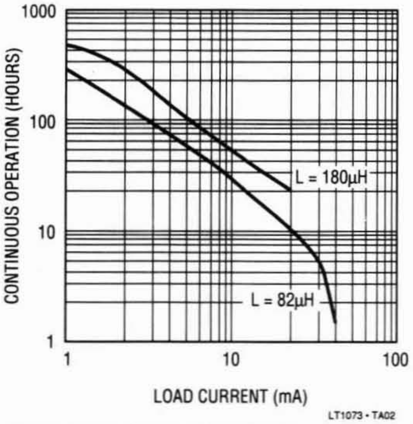


OPERATES WITH CELL VOLTAGE ≥ 1.0V

*ADD 10µF DECOUPLING CAPACITOR IF BATTERY IS MORE THAN 2" AWAY FROM LT1073.

LT1073 • TA01

Single Alkaline "AA" Cell Operating Hours vs DC Load Current

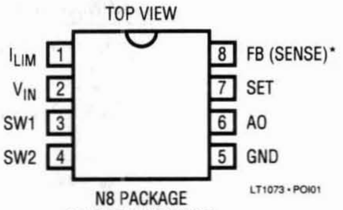


LT1073 • TA02

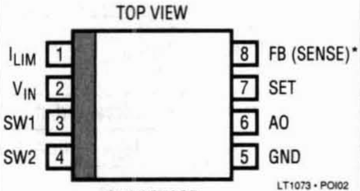
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Step-Up Mode 15V
Supply Voltage, Step-Down Mode 36V
SW1 Pin Voltage 50V
SW2 Pin Voltage .... −0.4V to V_{IN}
Feedback Pin Voltage (LT1073) 5V
Switch Current 1.5A
Maximum Power Dissipation 500mW
Operating Temperature Range (LT1073C) ...0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
*FIXED VERSIONS



S8 PACKAGE
8-LEAD PLASTIC SOIC
*FIXED VERSIONS

ORDER PART NUMBER
LT1073CN8 LT1073CN8-5 LT1073CN8-12
LT1073CS8 LT1073CS8-5 LT1073CS8-12
S8 PART MARKING
1073 07305 07312

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{IN} = 1.5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off		●		95	130	μA
I_Q	Quiescent Current, Step-Up Mode Configuration	No Load	LT1073-5			135		μA
			LT1073-12			250		
V_{IN}	Input Voltage	Step-Up Mode		●	1.15		12.6	V
					1.0		12.6	
		Step-Down Mode		●			30	
	Comparator Trip Point Voltage	LT1073 (Note 1)		●	202	212	222	mV
V_{OUT}	Output Sense Voltage	LT1073-5 (Note 2)		●	4.75	5.00	5.25	V
		LT1073-12 (Note 2)		●	11.4	12.00	12.6	
	Comparator Hysteresis	LT1073		●		5	10	mV
	Output Hysteresis	LT1073-5		●		125	250	mV
		LT1073-12		●		300	600	
f_{OSC}	Oscillator Frequency			●	15	19	23	kHz
DC	Duty Cycle	Full Load ($V_{FB} < V_{REF}$)		●	65	72	80	%
t_{ON}	Switch ON Time			●	30	38	50	μs
I_{FB}	Feedback Pin Bias Current	LT1073, V_{FB} = 0V		●		10	50	nA
I_{SET}	Set Pin Bias Current	$V_{SET} = V_{REF}$		●		60	120	nA
V_{AO}	AO Output Low	I_{AO} = −100mA		●		0.15	0.4	V
	Reference Line Regulation	1.0V ≤ V_{IN} ≤ 1.5V		●		0.35	1.0	%/V
		1.5V ≤ V_{IN} ≤ 12V		●		0.05	0.1	

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 1.5V$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CESAT}	Switch Saturation Voltage Step-Up Mode	$V_{IN} = 1.5V$, $I_{SW} = 400mA$			300	400	mV
			●			600	
		$V_{IN} = 1.5V$, $I_{SW} = 500mA$			400	550	
			●			750	
		$V_{IN} = 5V$, $I_{SW} = 1A$			700	1000	
			●			1500	
A_V	A2 Error Amp Gain	$R_L = 100k\Omega$ (Note 3)	●	400	1000		V/V
I_{REV}	Reverse Battery Current	(Note 4)			750		mA
I_{LIM}	Current Limit	220Ω Between I_{LIM} and V_{IN}			400		mA
	Current Limit Temperature Coefficient				– 0.3		%/°C
I_{LEAK}	Switch OFF Leakage Current	Measured at SW1 Pin			1	10	μA
V_{SW2}	Maximum Excursion Below GND	$I_{SW1} \leq 10\mu A$, Switch Off			– 400	– 350	mV

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: This specification guarantees that both the high and low trip point of the comparator fall within the 202mV to 222mV range.

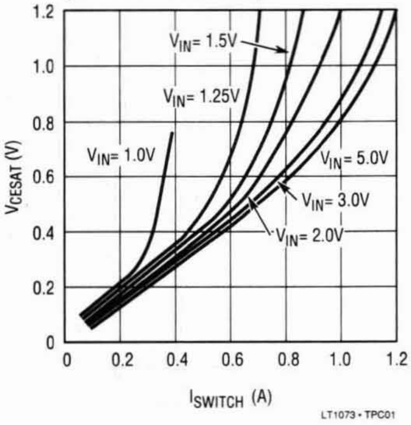
Note 2: This specification guarantees that the output voltage of the fixed versions will always fall within the specified range. The waveform at the sense pin will exhibit a sawtooth shape due to the comparator hysteresis.

Note 3: 100kΩ resistor connected between a 5V source and the AO pin.

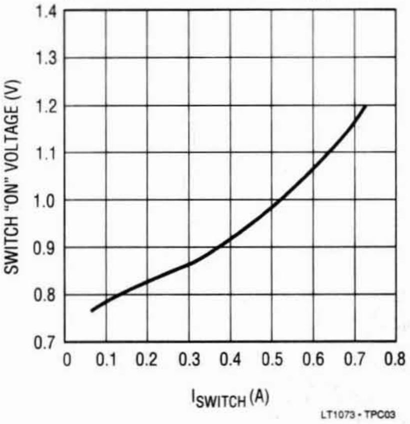
Note 4: The LT1073 is guaranteed to withstand continuous application of +1.6V applied to the GND and SW2 pins while V_{IN}, I_{LIM}, and SW1 pins are grounded.

TYPICAL PERFORMANCE CHARACTERISTICS

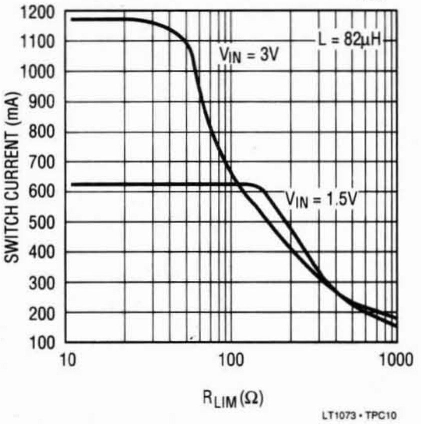
Saturation Voltage Step-Up Mode (SW2 Pin Grounded)



Switch ON Voltage Step-Down Mode (SW1 Pin Connected to V_{IN})

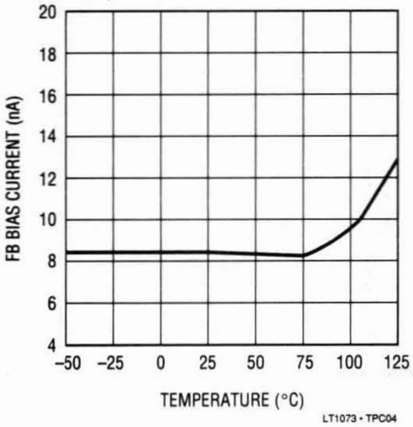


Maximum Switch Current vs R_{LIM}

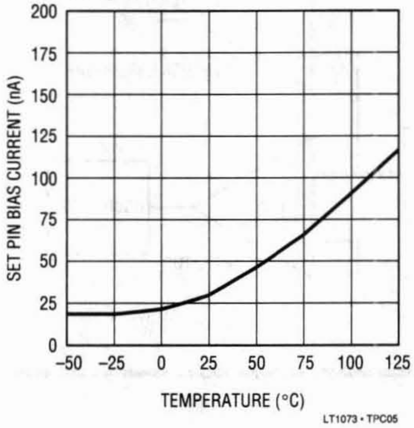


TYPICAL PERFORMANCE CHARACTERISTICS

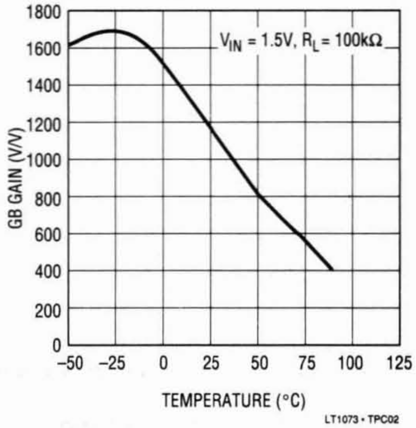
Feedback Pin Bias Current vs Temperature



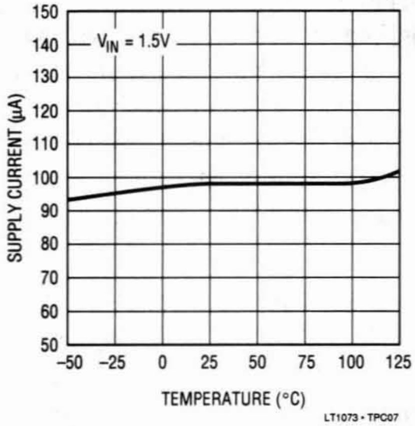
Set Pin Bias Current vs Temperature



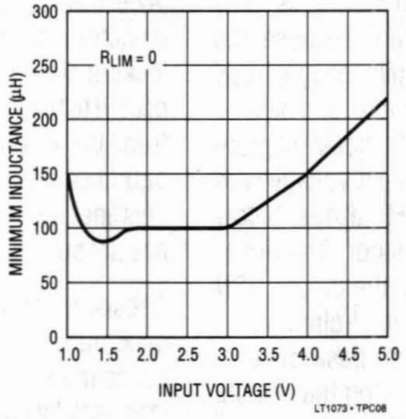
"Gain Block" Gain



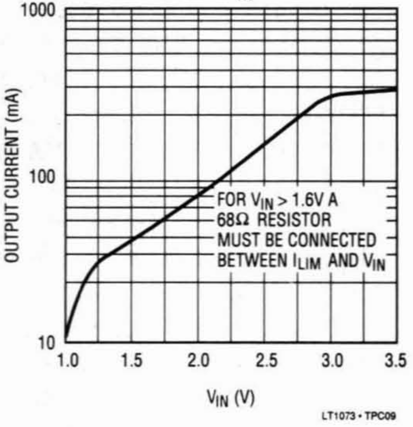
Supply Current vs Temperature



Recommended Minimum Inductance Value



Guaranteed Minimum Output Current at 5V vs V_{IN}



PIN FUNCTIONS

I_{LIM} (Pin 1): Connect this pin to V_{IN} for normal use. Where lower current limit is desired, connect a resistor between I_{LIM} and V_{IN}. A 220Ω resistor will limit the switch current to approximately 400mA.

V_{IN} (Pin 2): Input supply voltage.

SW1 (Pin 3): Collector of power transistor. For step-up mode connect to inductor/diode. For step-down mode connect to V_{IN}.

SW2 (Pin 4): Emitter of power transistor. For step-up mode connect to ground. For step-down mode connect to inductor/diode. This pin must never be allowed to go more than a Schottky diode drop below ground.

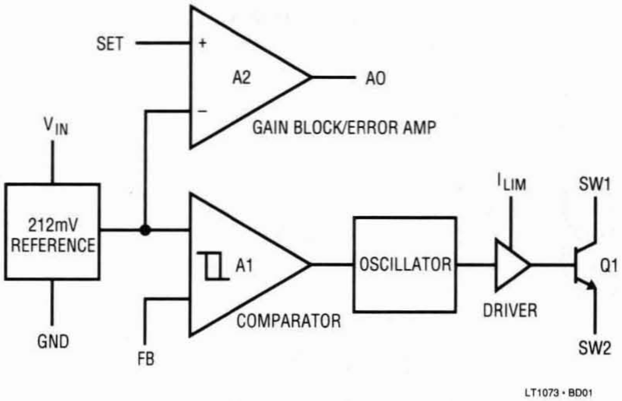
GND (Pin 5): Ground.

AO (Pin 6): Auxiliary Gain Block (GB) output. Open collector, can sink 100µA.

SET (Pin 7): GB input. GB is an op amp with positive input connected to SET pin and negative input connected to 212mV reference.

FB/SENSE (Pin 8): On the LT1073 (adjustable) this pin goes to the comparator input. On the LT1073-5 and LT1073-12, this pin goes to the internal application resistor that sets output voltage.

LT1073 BLOCK DIAGRAM



LT1073 OPERATION

The LT1073 is a gated oscillator switcher. This type architecture has very low supply current because the switch is cycled only when the feedback pin voltage drops below the reference voltage. Circuit operation can best be understood by referring to the LT1073 block diagram above. Comparator A1 compares the FB pin voltage with the 212mV reference signal. When FB drops below 212mV, A1 switches on the 19kHz oscillator. The driver amplifier boosts the signal level to drive the output NPN power switch Q1. An adaptive base drive circuit senses switch current and provides just enough base drive to ensure switch saturation without overdriving the switch, resulting in higher efficiency. The switch cycling action raises the output voltage and FB pin voltage. When the FB voltage is sufficient to trip A1, the oscillator is gated off. A small amount of hysteresis built into A1 ensures loop stability without external frequency compensation. When the comparator is low the oscillator and all high current circuitry is turned off, lowering device quiescent current to just 95µA for the reference, A1 and A2.

The oscillator is set internally for 38µs ON time and 15µs OFF time, optimizing the device for step-up circuits where $V_{OUT} \approx 3V_{IN}$, e.g., 1.5V to 5V. Other step-up ratios as well as step-down (buck) converters are possible at slight losses in maximum achievable power output.

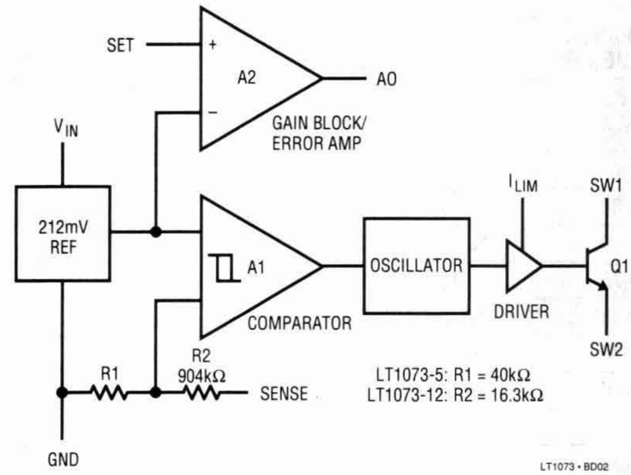
A2 is a versatile gain block that can serve as a low-battery detector, a linear post-regulator, or drive an undervoltage lockout circuit. The negative input of A2 is internally connected to the 212mV reference. An external resistor divider from V_{IN} to GND provides the trip point for A2. The AO output can sink 100µA (use a 56k resistor pull-up to +5V). This line can signal a microcontroller that the battery voltage has dropped below the preset level.

A resistor connected between the I_{LIM} pin and V_{IN} adjusts maximum switch current. When the switch current exceeds the set value, the switch is turned off. This feature is especially useful when small inductance values are used with high input voltages. If the internal current limit of 1.5A is desired, I_{LIM} should be tied directly to V_{IN}. Propagation delay through the current-limit circuitry is about 2µs.

In step-up mode, SW2 is connected to ground and SW1 drives the inductor. In step-down mode, SW1 is connected to V_{IN} and SW2 drives the inductor. Output voltage is set by the following equation in either step-up or step-down modes where R1 is connected from FB to GND and R2 is connected from V_{OUT} to FB.

$$V_{OUT} = (212\text{mV})\left(\frac{R2}{R1} + 1\right) \qquad (01)$$

LT1073-5, -12 BLOCK DIAGRAM


SET
+
A2
–
AO
GAIN BLOCK/
ERROR AMP
V_{IN}
212mV
REF
A1
COMPARATOR
OSCILLATOR
I_{LIM}
DRIVER
SW1
Q1
SW2
R1
R2
904kΩ
SENSE
GND
LT1073-5: R1 = 40kΩ
LT1073-12: R2 = 16.3kΩ
LT1073 • BD02

LT1073-5, -12 OPERATION

The LT1073-5 and LT1073-12 fixed output voltage versions have the gain-setting resistors on-chip. Only three external components are required to construct a fixed-output converter. 5μA flows through R1 and R2 in the LT1073-5, and 12.3μA flows in the LT1073-12. This current represents a load and the converter must cycle from time to time to maintain the proper output voltage. Output ripple, inherently present in gated-oscillator designs, will typically run around 150mV for the LT1073-5 and 350mV for the LT1073-12 with the proper inductor/capacitor selection. This output ripple can be reduced considerably by using the gain block amp as a pre-amplifier in front of the FB pin. See the applications section for details.

APPLICATIONS INFORMATION

Measuring Input Current at Zero or Light Load

Obtaining meaningful numbers for quiescent current and efficiency at low output current involves understanding how the LT1073 operates. At very low or zero load current, the device is idling for seconds at a time. When the output voltage falls enough to trip the comparator, the power switch comes on for a few cycles until the output voltage rises sufficiently to overcome the comparator hysteresis. When the power switch is on, inductor current builds up to hundreds of milliamperes. Ordinary digital multimeters are not capable of measuring average current because of bandwidth and dynamic range limitations. A different approach is required to measure the 100μA off-state and 500mA on-state currents of the circuit.

Quiescent current can be accurately measured using the circuit in Figure 1. V_{SET} is set to the input voltage of the LT1073. The circuit must be "booted" by shorting V2 to V_{SET}. After the LT1073 output voltage has settled, disconnect the short. Input voltage is V2, and average input current can be calculated by this formula:

$$I_{IN} = \frac{V2 - V1}{100\Omega} \qquad (02)$$

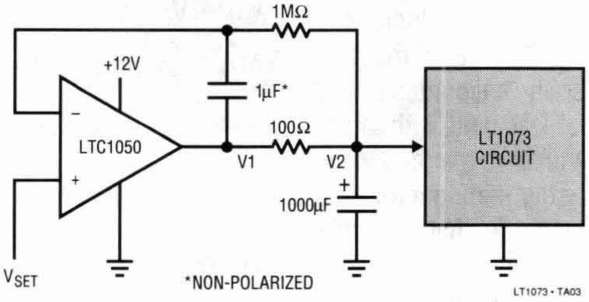

1MΩ
+12V
1μF*
–
LTC1050
+
100Ω
V1
V2
+
1000μF
LT1073
CIRCUIT
V_{SET}
*NON-POLARIZED
LT1073 • TA03

Figure 1. Test Circuit Measures No-Load Quiescent Current of LT1073 Converter

APPLICATIONS INFORMATION

Table 1. Component Selection for Step-Up Converters

INPUT VOLTAGE	BATTERY TYPE	OUTPUT VOLTAGE	OUTPUT CURRENT (MIN)	INDUCTOR VALUE (μH)	INDUCTOR PART NUMBER	CAPACITOR VALUE	NOTES
1.55-1.25	Single Alkaline	3.0V	60mA	82	G GA10-822K, CB 7300-12	150μF	
1.30-1.05	Single Ni-Cad	3.0V	20mA	180	G GA10-183K, CB 7300-16	47μF	
1.55-1.25	Single Alkaline	5.0V	30mA	82	G GA10-822K, CB 7300-12	100μF	
1.30-1.05	Single Ni-Cad	5.0V	10mA	180	G GA10-183K, CB 7300-16	22μF	
3.1-2.1	Two Alkaline	5.0V	80mA	120	G GA10-123K, CB 7300-14	470μF	*
3.1-2.1	Two Alkaline	5.0V	25mA	470	G GA10-473K, CB 7300-21	150μF	*
3.3-2.5	Lithium	5.0V	100mA	150	G GA40-153K, CB 6860-15	470μF	*
3.1-2.1	Two Alkaline	12V	25mA	120	G GA10-123K, CB 7300-14	220μF	
3.1-2.1	Two Alkaline	12V	5mA	470	G GA10-473K, CB 7300-21	100μF	
3.3-2.5	Lithium	12V	30mA	150	G GA10-153K, CB 7300-15	220μF	
4.5-5.5	TTL Supply	12V	90mA	220	G GA40-223K, CB 6860-17	470μF	*
4.5-5.5	TTL Supply	12V	22mA	1000	G GA10-104K, CB 7300-25	100μF	*
4.5-5.5	TTL Supply	24V	35mA	220	G GA40-223K, CB 6860-17	150μF	*

G = GOWANDA CB = CADDELL-BURNS

* Add 68Ω from I_{LIM} to V_{IN}

Inductor Selection

A DC-DC converter operates by storing energy as magnetic flux, in an inductor core, and then switching this energy into the load. Since it is flux, not charge, that is stored, the output voltage can be higher, lower, or opposite in polarity to the input voltage by choosing an appropriate switching topology. To operate as an efficient energy transfer element, the inductor must fulfill three requirements. First, the inductance must be low enough for the inductor to store adequate energy under the worst-case condition of minimum input voltage and switch ON time. The inductance must also be high enough so that maximum current ratings of the LT1073 and inductor are not exceeded at the other worst-case condition of maximum input voltage and ON time. Additionally, the inductor core must be able to store the required flux, i.e., it must not *saturate*. At power levels generally encountered with LT1073-based designs, small axial-lead units with saturation current ratings in the 300mA to 1A range (depending on application) are adequate. Lastly, the inductor must have sufficiently low DC resistance so that excessive power is not lost as heat in the windings. An additional consideration is Electro-Magnetic Interference (EMI). Toroid and pot core type inductors are recommended in applications where EMI must be kept to a minimum; for example, where there are sensitive analog circuitry or transducers nearby. Rod core types are a less expensive choice where EMI is not a problem.

Specifying a proper inductor for an application requires first establishing minimum and maximum input voltage, output voltage, and output current. In a step-up converter, the inductive events add to the input voltage to produce the output voltage. Power required from the inductor is determined by

$$P_L = \left(V_{OUT} + V_D - V_{IN}\right)\left(I_{OUT}\right) \qquad (03)$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky).

Maximum power in the inductor is

$$\begin{aligned} P_L &= E_L \bullet f_{OSC} \qquad (04) \\ &= \frac{1}{2} L\, i^2_{PEAK} \bullet f_{OSC} \end{aligned}$$

where

$$i_{PEAK} = \left(\frac{V_{IN}}{R}\right)\left(1 - e\,\frac{-Rt_{ON}}{L}\right) \qquad (05)$$

APPLICATIONS INFORMATION

R = Switch equivalent resistance (1.0Ω maximum) added to the DC resistance of the inductor, and t_{ON} = ON time of the switch.

At maximum V_{IN} and ON time, i_{PEAK} should not be allowed to exceed the maximum switch current shown in Figure 2. Some input/output voltage combinations will cause continuous[1] mode operation. In these cases a resistor is needed between I_{LIM} (pin 1) and V_{IN} (pin 2) to keep switch current under control. See the "Using the I_{LIM} Pin" section for details.

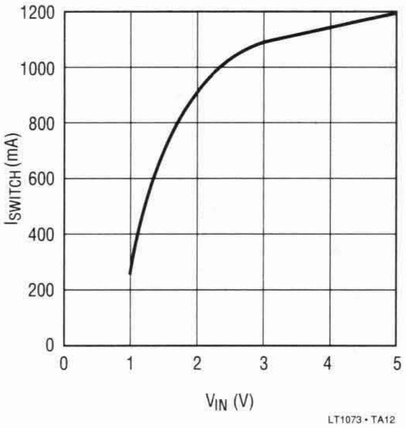


Figure 2. Maximum Switch Current vs Input Voltage

Capacitor Selection

Selecting the right output capacitor is almost as important as selecting the right inductor. A poor choice for a filter capacitor can result in poor efficiency and/or high output ripple. Ordinary aluminum electrolytics, while inexpensive and readily available, may have unacceptably poor equivalent series resistance (ESR) and ESL (inductance). There are low-ESR aluminum capacitors on the market specifically designed for switch-mode DC-DC converters which work much better than general-purpose units. Tantalum capacitors provide still better performance at more expense. We recommend OS-CON capacitors from Sanyo Corporation (San Diego, CA). These units are physically quite small and have extremely low ESR. To illustrate, Figures 3, 4, and 5 show the output voltage of an LT1073-based converter with three 100µF capacitors. The peak switch current is 500mA in all cases. Figure 3 shows a Sprague 501D aluminum capacitor. V_{OUT} jumps by over 150mV when the switch turns off, followed by a drop in voltage as the inductor dumps into the capacitor. This works out to be an ESR of over 300mΩ. Figure 4 shows the same circuit, but with a Sprague 150D tantalum capacitor replacing the aluminum unit. Output jump is now about 30mV, corresponding to an ESR of 60mΩ. Figure 5 shows the circuit with an OS-CON unit. ESR is now only 30mΩ.

In very low power applications where every microampere is important, leakage current of the capacitor must be considered. The OS-CON units do have leakage current in the 5µA to 10µA range. If the load is also in the microampere range, a leaky capacitor will noticeably decrease efficiency. In this type application tantalum capacitors are the best choice, with typical leakage currents in the 1µA to 5µA range.

Diode Selection

Speed, forward drop, and leakage current are the three main considerations in selecting a catch diode for LT1073 converters. "General-purpose" rectifiers such as the 1N4001 are *unsuitable* for use in *any* switching-regulator application. Although they are rated at 1A, the switching time of a 1N4001 is in the 10µs-50µs range. At best, efficiency will be severely compromised when these di-

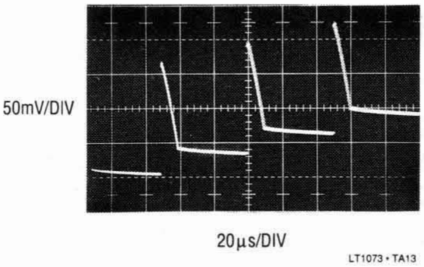


Figure 3. Aluminum

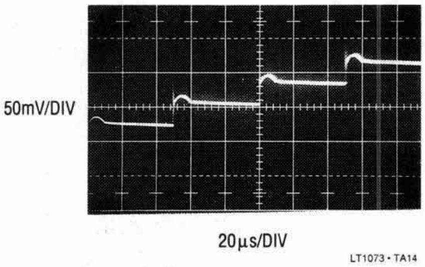


Figure 4. Tantalum

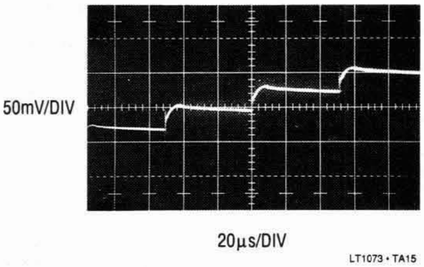


Figure 5. OS-CON

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[1] i.e., inductor current does not go to zero when the switch is off.

APPLICATIONS INFORMATION

odes are used, and at worst, the circuit may not work at all. Most LT1073 circuits will be well served by a 1N5818 Schottky diode. The combination of 500mV forward drop at 1A current, fast turn-on and turn-off time, and 4µA to 10µA leakage current fit nicely with LT1073 requirements. At peak switch currents of 100mA or less, a 1N4148 signal diode may be used. This diode has leakage current in the 1nA-5nA range at 25°C and lower cost than a 1N5818. (You can also use them to get your circuit up and running, but beware of destroying the diode at 1A switch currents.) In situations where the load is intermittent and the LT1073 is idling most of the time, battery life can sometimes be extended by using a silicon diode such as the 1N4933, which can handle 1A but has leakage current of less than 1µA. Efficiency will decrease somewhat compared to a 1N5818 while delivering power, but the lower idle current may be more important.

Step-Up (Boost Mode) Operation

A step-up DC-DC converter delivers an output voltage higher than the input voltage. Step-up converters are *not* short-circuit protected since there is a DC path from input to output.

The usual step-up configuration for the LT1073 is shown in Figure 6. The LT1073 first pulls SW1 low causing V_{IN}-V_{CESAT} to appear across L1. A current then builds up in L1. At the end of the switch ON time the current in L1 is[2]:

$$i_{PEAK} = \frac{V_{IN}}{L} t_{ON} \qquad (06)$$

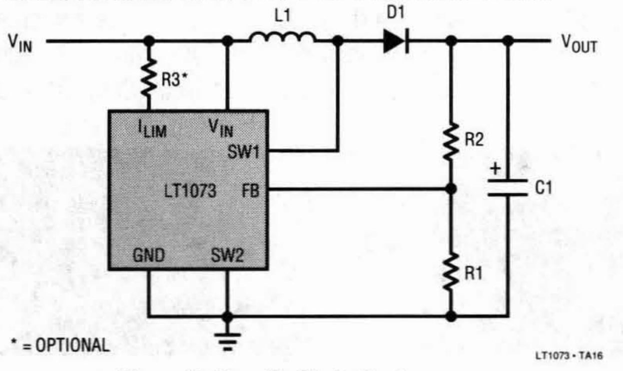

Figure 6. Step-Up Mode Hookup. Refer to Table 1 for Component Values

Immediately after switch turn-off, the SW1 voltage pin starts to rise because current cannot instantaneously stop flowing in L1. When the voltage reaches $V_{OUT} + V_D$, the inductor current flows through D1 into C1, increasing V_{OUT}. This action is repeated as needed by the LT1073 to keep V_{FB} at the internal reference voltage of 212mV. R1 and R2 set the output voltage according to the formula

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(212\text{mV}) \qquad (07)$$

Step-Down (Buck Mode) Operation

A step-down DC-DC converter converts a higher voltage to a lower voltage. It is short-circuit protected because the switch is in series with the output. Step-down converters are characterized by low output voltage ripple but high input current ripple. The usual hookup for an LT1073-based step-down converter is shown in Figure 7.

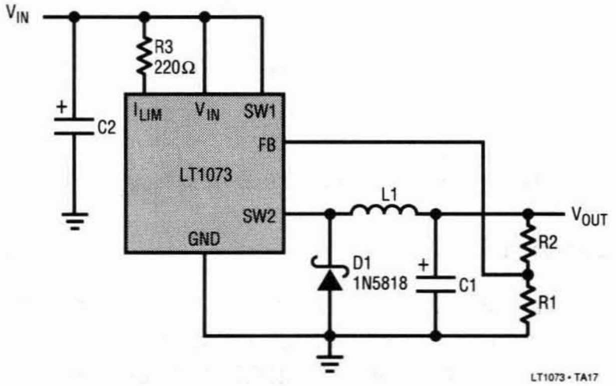

Figure 7. Step-Down Mode Hookup

When the switch turns on, SW2 pulls up to $V_{IN} - V_{SW}$. This puts a voltage across L1 equal to $V_{IN} - V_{SW} - V_{OUT}$, causing a current to build up in L1. At the end of the switch ON time, the current in L1 is equal to

$$i_{PEAK} = \frac{V_{IN} - V_{SW} - V_{OUT}}{L} t_{ON} \qquad (08)$$

When the switch turns off the SW2 pin falls rapidly and actually goes below ground. D1 turns on when SW2 reaches 0.4V below ground. *D1 MUST BE A SCHOTTKY DIODE.* The voltage at SW2 must never be allowed to go below −0.5V. A silicon diode such as the 1N4933 will allow

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[2] This simple expression neglects the effect of switch and coil resistance. These are taken into account in the "Inductor Selection" section.

APPLICATIONS INFORMATION

SW2 to go to −0.8V, causing potentially destructive power dissipation inside the LT1073. Output voltage is determined by

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(212mV) \quad (09)$$

R3 programs switch current limit. This is especially important in applications where the input varies over a wide range. Without R3, the switch stays on for a fixed time each cycle. Under certain conditions the current in L1 can build up to excessive levels, exceeding the switch rating and/or saturating the inductor. The 220Ω resistor programs the switch to turn off when the current reaches approximately 400mA. When using the LT1073 in step-down mode, output voltage should be limited to 6.2V or less.

Inverting Configurations

The LT1073 can be configured as a positive-to-negative converter (Figure 8), or a negative-to-positive converter (Figure 9). In Figure 8, the arrangement is very similar to a step-down, except that the high side of the feedback is referred to ground. This level shifts the output negative. As in the step-down mode, D1 must be a Schottky diode, and $|V_{OUT}|$ should be less than 6.2V.

In Figure 9, the input is negative while the output is positive. In this configuration, the magnitude of the input voltage can be higher or lower than the output voltage. A level shift, provided by the PNP transistor, supplies proper polarity feedback information to the regulator.

Using the I_{LIM} Pin

The LT1073 switch can be programmed to turn off at a set switch current, a feature not found on competing devices. This enables the input to vary over a wide range without exceeding the maximum switch rating or saturating the inductor. Consider the case where analysis shows the LT1073 must operate at an 800mA peak switch current with a 2.0V input. If V_{IN} rises to 4V, the peak switch current will rise to 1.6A, exceeding the maximum switch current rating. With the proper resistor (see the "Maximum Switch Current vs R_{LIM}" characteristic) selected, the switch current will be limited to 800mA, even if the input voltage increases. The LT1073 does this by sampling a small fraction of the switch current and passing this current through the external resistor. When the voltage on the I_{LIM} pin drops a V_{BE} below V_{IN}, the oscillator terminates the cycle. Propagation delay through this loop is about 2µs.

Another situation where the I_{LIM} feature is useful is when the device goes into continuous mode operation. This occurs in step-up mode when

$$\frac{V_{OUT} + V_{DIODE}}{V_{IN} - V_{SW}} < \frac{1}{1 - DC} \quad (10)$$

When the input and output voltages satisfy this relationship, inductor current does not go to zero during the switch OFF time. When the switch turns on again, the current ramp starts from the non-zero current level in the inductor just prior to switch turn-on. As shown in Figure 10, the inductor current increases to a high level before the comparator turns off the oscillator. This high current can

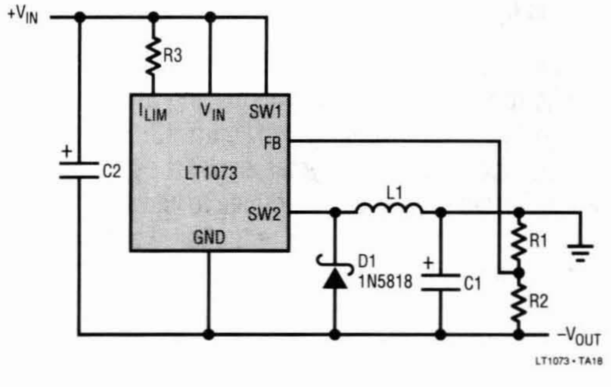


Figure 8. Positive-to-Negative Converter

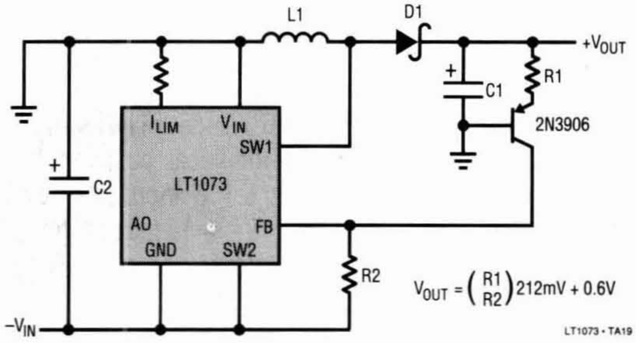


Figure 9. Negative-to-Positive Converter

APPLICATIONS INFORMATION

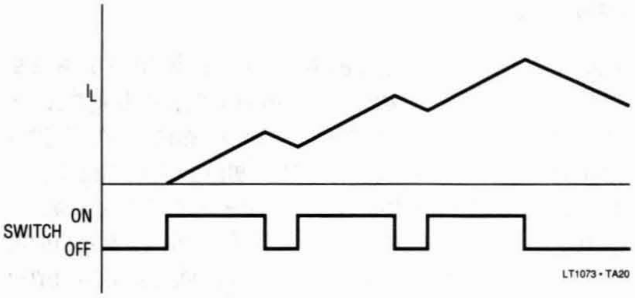


Figure 10. No Current Limit Causes Large Inductor Current Build-Up

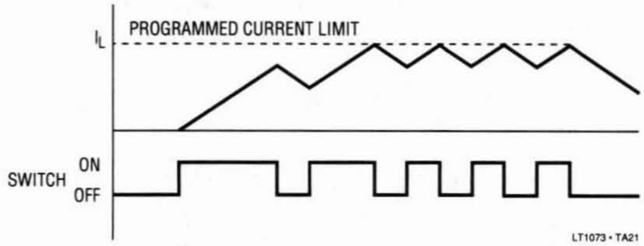
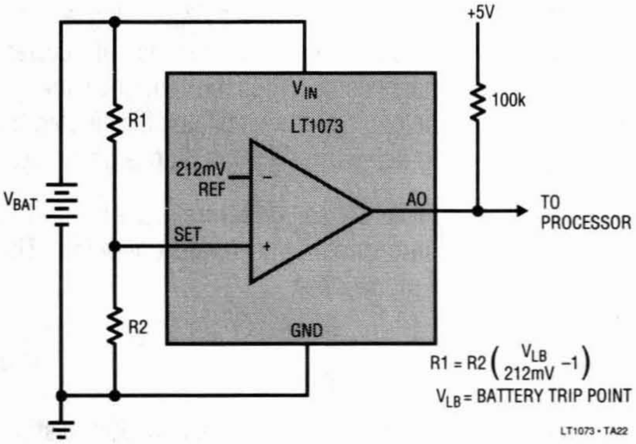
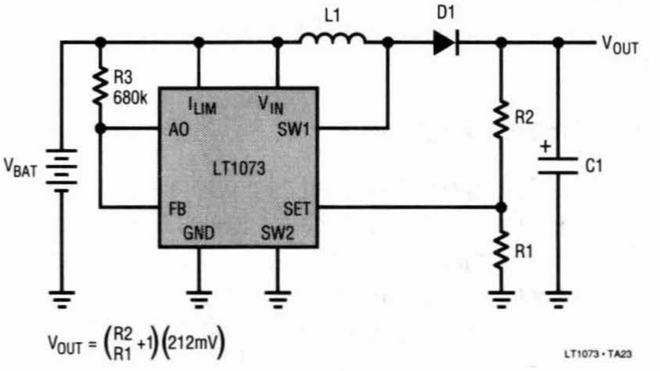


Figure 11. Current Limit Keeps Inductor Current Under Control



+5V
100k
V_{IN}
LT1073
R1
212mV REF
AO
SET
TO PROCESSOR
V_{BAT}
R2
GND
$R1 = R2\left(\frac{V_{LB}}{212mV} - 1\right)$
V_{LB} = BATTERY TRIP POINT
LT1073 • TA22

Figure 12. Setting Low Battery Detector Trip Point



L1
D1
V_{OUT}
R3
680k
I_{LIM}
V_{IN}
AO
SW1
R2
LT1073
V_{BAT}
C1
FB
SET
GND
SW2
R1
$V_{OUT} = \left(\frac{R2}{R1} + 1\right)(212mV)$
LT1073 • TA23

Figure 13. Output Ripple Reduction Using Gain Block

cause excessive output ripple and requires oversizing the output capacitor and inductor. With the I_{LIM} feature, however, the switch current turns off at a programmed level as shown in Figure 11, keeping output ripple to a minimum.

Using the Gain Block

The gain block (GB) on the LT1073 can be used as an error amplifier, low-battery detector or linear post-regulator. The gain block itself is a very simple PNP input op amp with an open-collector NPN output. The (–) input of the gain block is tied internally to the 212mV reference. The (+) input comes out on the SET pin.

Arrangement of the gain block as a low battery detector is straightforward. Figure 12 shows hookup. R1 and R2 need only be low enough in value so that the bias current of the SET input does not cause large errors. 100kΩ for R2 is adequate.

Output ripple of the LT1073, normally 150mV at $5V_{OUT}$, can be reduced significantly by placing the gain block in front of the FB input as shown in Figure 13. This effectively reduces the comparator hysteresis by the gain of the gain block. Output ripple can be reduced to just a few millivolts using this technique. Ripple reduction works with step-down or inverting modes as well.

APPLICATIONS INFORMATION

Table 2. Inductor Manufacturers

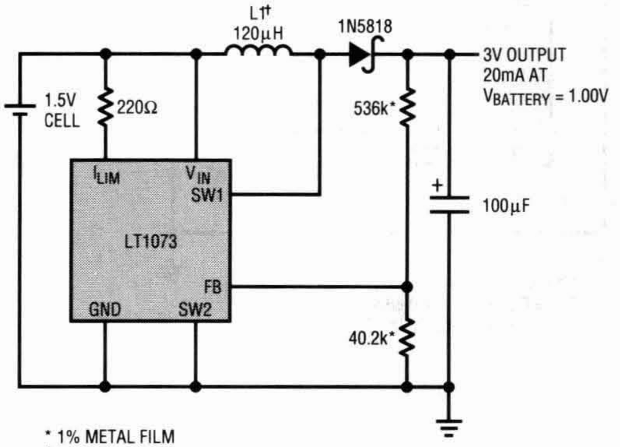
MANUFACTURER	PART NUMBERS
Gowanda Electronics Corporation 1 Industrial Place Gowanda, NY 14070 716-532-2234	GA10 Series GA40 Series
Caddell-Burns 258 East Second Street Mineola, NY 11501 516-746-2310	7300 Series 6860 Series
Coiltronics International 984 S.W. 13th Court Pompano Beach, FL 33069 305-781-8900	Custom Toroids Surface Mount
Toko America Incorporated 1250 Feehanville Drive Mount Prospect, IL 60056 312-297-0070	Type 8RBS
Renco Electronics Incorporated 60 Jefryn Boulevard, East Deer Park, NY 11729 800-645-5828	RL1283 RL1284

Table 3. Capacitor Manufacturers

MANUFACTURER	PART NUMBERS
Sanyo Video Components 1201 Sanyo Avenue San Diego, CA 92073 619-661-6322	OS-CON Series
Nichicon America Corporation 927 East State Parkway Schaumberg, IL 60173 708-843-7500	PL Series
Sprague Electric Company Lower Main Street Sanford, ME 04073 207-324-4140	150D Solid Tantalums 550D Tantalex

TYPICAL APPLICATIONS

1.5V to 3V Step-Up Converter

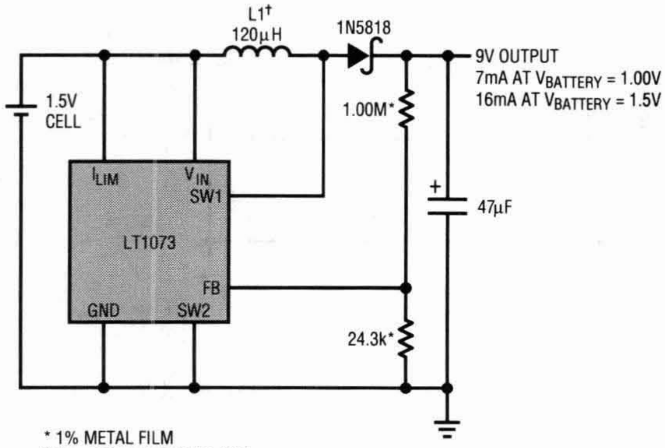


L1†
120µH
1N5818
3V OUTPUT
20mA AT
V_BATTERY = 1.00V
1.5V
CELL
220Ω
536k*
I_LIM
V_IN
SW1
LT1073
FB
GND
SW2
100µF
40.2k*

* 1% METAL FILM
† L1 = GOWANDA GA10-123k
OR CADDELL-BURNS 7300-14

LT1073 • TA24

1.5V to 9V Step-Up Converter



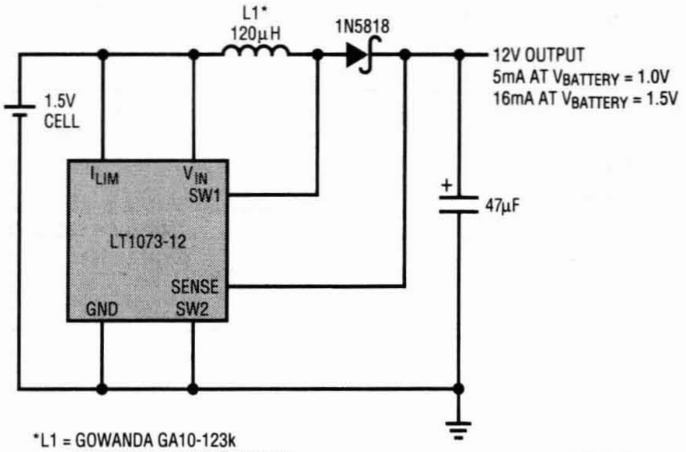
L1†
120µH
1N5818
9V OUTPUT
7mA AT V_BATTERY = 1.00V
16mA AT V_BATTERY = 1.5V
1.5V
CELL
1.00M*
I_LIM
V_IN
SW1
LT1073
FB
GND
SW2
47µF
24.3k*

* 1% METAL FILM
† L1 = GOWANDA GA10-123k
OR CADDELL-BURNS 7300-14

LT1073 • TA25

TYPICAL APPLICATIONS

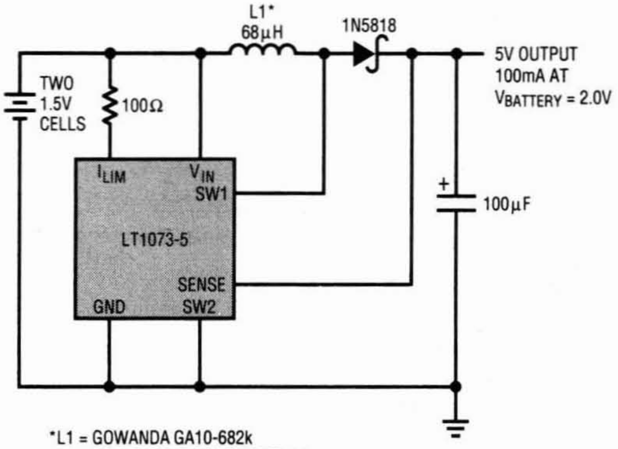
1.5V to 12V Step-Up Converter


L1*
120μH
1N5818
12V OUTPUT
5mA AT $V_{BATTERY}$ = 1.0V
16mA AT $V_{BATTERY}$ = 1.5V
1.5V
CELL
I_{LIM}
V_{IN}
SW1
LT1073-12
SENSE
GND
SW2
47μF

*L1 = GOWANDA GA10-123k
OR CADDELL-BURNS 7300-14

LT1073 • TA26

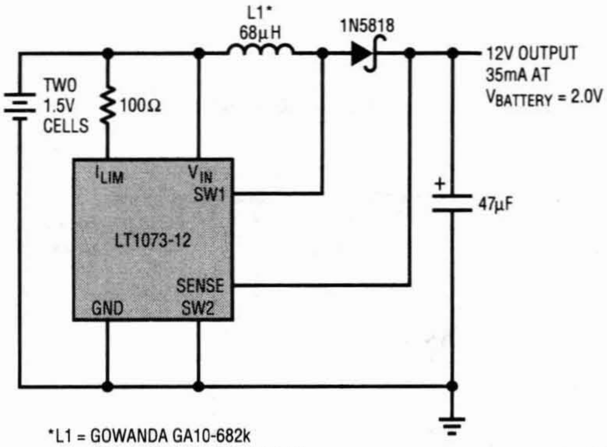
3V to 5V Step-Up Converter


L1*
68μH
1N5818
5V OUTPUT
100mA AT
$V_{BATTERY}$ = 2.0V
TWO
1.5V
CELLS
100Ω
I_{LIM}
V_{IN}
SW1
LT1073-5
SENSE
GND
SW2
100μF

*L1 = GOWANDA GA10-682k
OR CADDELL-BURNS 7300-11

LT1073 • TA27

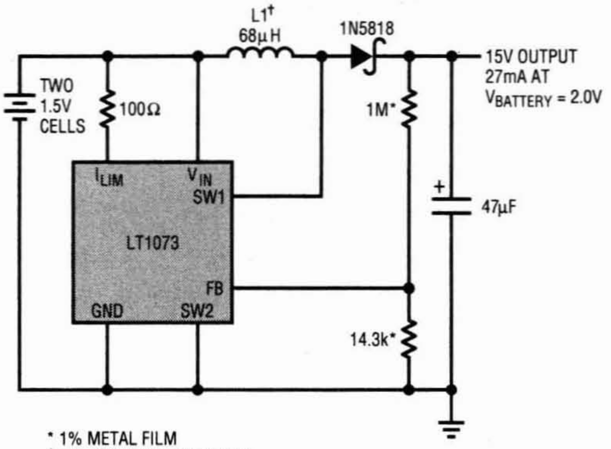
3V to 12V Step-Up Converter


L1*
68μH
1N5818
12V OUTPUT
35mA AT
$V_{BATTERY}$ = 2.0V
TWO
1.5V
CELLS
100Ω
I_{LIM}
V_{IN}
SW1
LT1073-12
SENSE
GND
SW2
47μF

*L1 = GOWANDA GA10-682k
OR CADDELL-BURNS 7300-11

LT1073 • TA28

3V to 15V Step-Up Converter

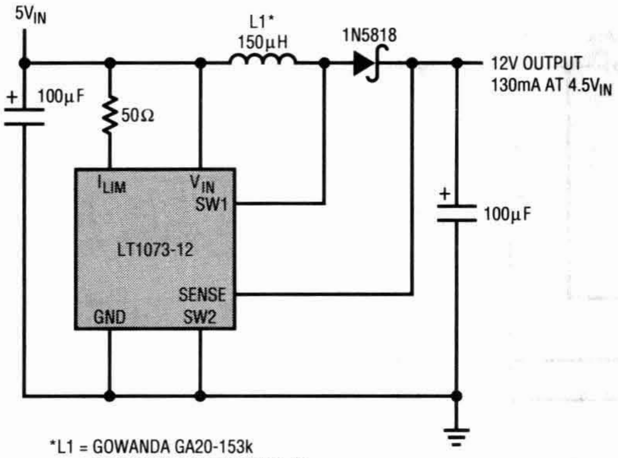

L1†
68μH
1N5818
15V OUTPUT
27mA AT
$V_{BATTERY}$ = 2.0V
TWO
1.5V
CELLS
100Ω
1M*
I_{LIM}
V_{IN}
SW1
LT1073
FB
GND
SW2
47μF
14.3k*

* 1% METAL FILM
† L1 = GOWANDA GA10-682k
OR CADDELL-BURNS 7300-11

LT1073 • TA29

TYPICAL APPLICATIONS

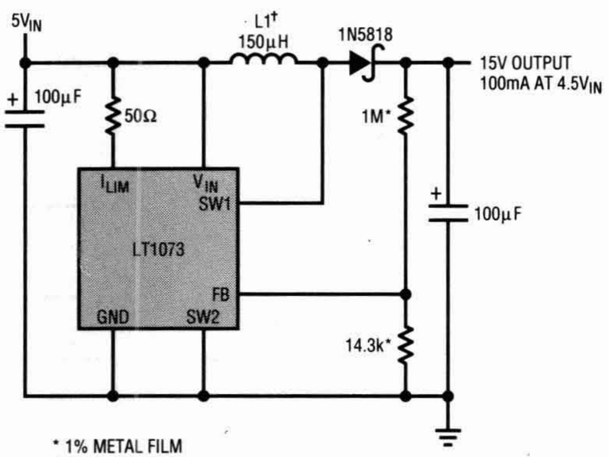
5V to 12V Step-Up Converter


5V$_{IN}$
L1*
150μH
1N5818
12V OUTPUT
130mA AT 4.5V$_{IN}$
100μF
50Ω
I$_{LIM}$
V$_{IN}$
SW1
LT1073-12
SENSE
GND
SW2
100μF

*L1 = GOWANDA GA20-153k
OR CADDELL-BURNS 7200-15

LT1073 • TA30

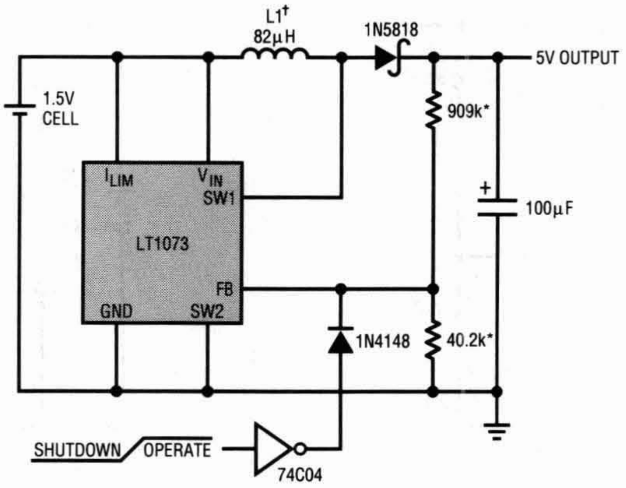
5V to 15V Step-Up Converter


5V$_{IN}$
L1†
150μH
1N5818
15V OUTPUT
100mA AT 4.5V$_{IN}$
100μF
50Ω
1M*
I$_{LIM}$
V$_{IN}$
SW1
LT1073
FB
GND
SW2
100μF
14.3k*

* 1% METAL FILM
† L1 = GOWANDA GA20-153k
OR CADDELL-BURNS 7200-15

LT1073 • TA31

1.5V to 5V Step-Up Converter with Logic Shutdown

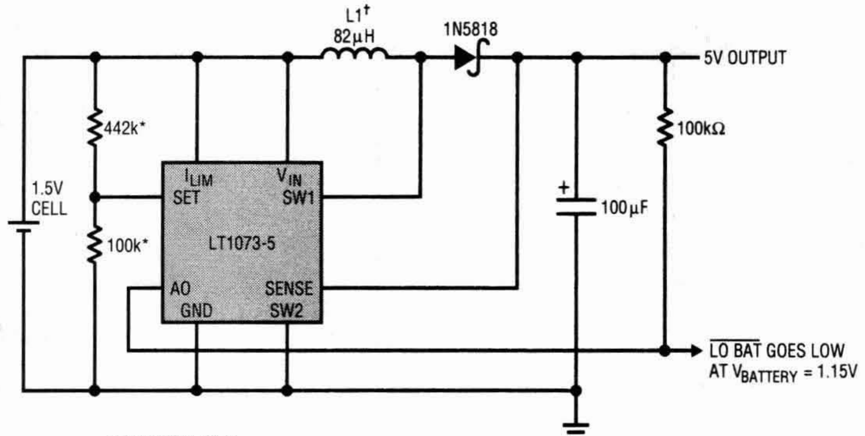

L1†
82μH
1N5818
5V OUTPUT
1.5V
CELL
909k*
I$_{LIM}$
V$_{IN}$
SW1
LT1073
FB
GND
SW2
100μF
1N4148
40.2k*
SHUTDOWN/OPERATE
74C04

* 1% METAL FILM
† L1 = GOWANDA GA10-822k
OR CADDELL-BURNS 7300-12

LT1073 • TA32

TYPICAL APPLICATIONS

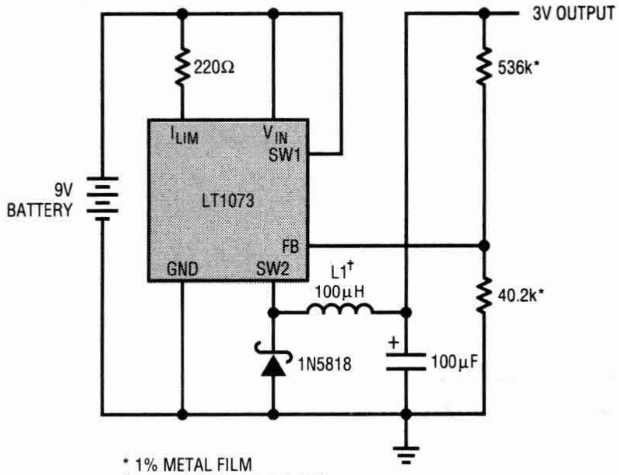
1.5V to 5V Step-Up Converter with Low-Battery Detector


L1†
82μH
1N5818
5V OUTPUT
442k*
100kΩ
1.5V
CELL
I_LIM
SET
V_IN
SW1
LT1073-5
100k*
+
100μF
AO
SENSE
GND
SW2
LO BAT GOES LOW
AT V_BATTERY = 1.15V

* 1% METAL FILM
† L1 = GOWANDA GA10-822k
OR CADDELL-BURNS 7300-12

LT1073 • TA33

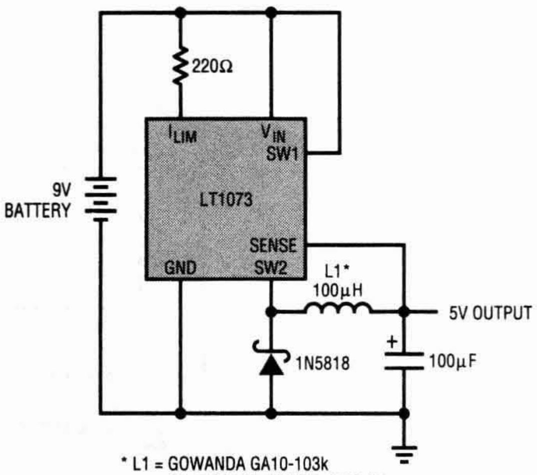
9V to 3V Step-Down Converter


3V OUTPUT
220Ω
536k*
I_LIM
V_IN
SW1
9V
BATTERY
LT1073
FB
GND
SW2
L1†
100μH
40.2k*
+
1N5818
100μF

* 1% METAL FILM
† L1 = GOWANDA GA10-103k
OR CADDELL-BURNS 7300-13

LT1073 • TA34

9V to 5V Step-Down Converter

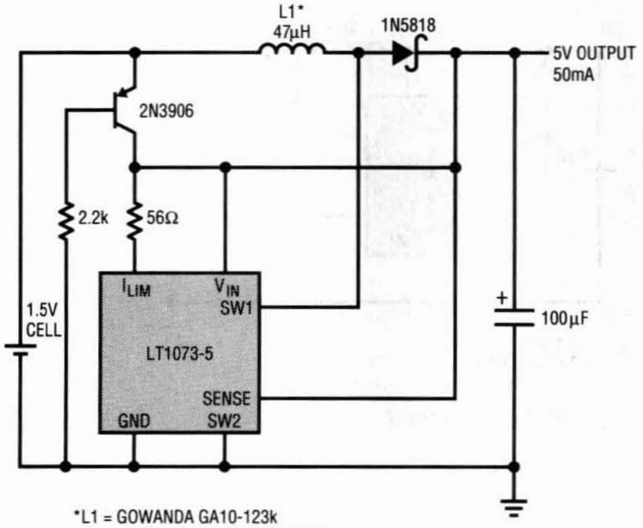

220Ω
I_LIM
V_IN
SW1
9V
BATTERY
LT1073
SENSE
GND
SW2
L1*
100μH
5V OUTPUT
+
1N5818
100μF

* L1 = GOWANDA GA10-103k
OR CADDELL-BURNS 7300-13

LT1073 • TA35

TYPICAL APPLICATIONS

1.5V to 5V Bootstrapped Step-Up Converter

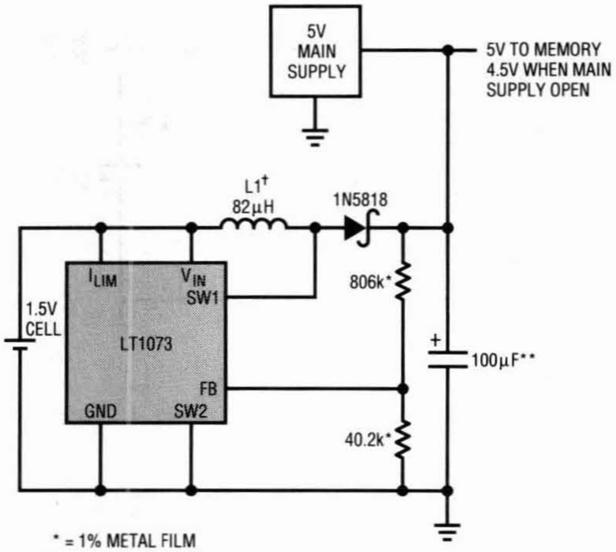

L1*
47μH
1N5818
5V OUTPUT
50mA
2N3906
2.2k
56Ω
1.5V CELL
I_LIM
V_IN
SW1
LT1073-5
SENSE
GND
SW2
+
100μF

*L1 = GOWANDA GA10-123k
OR CADDELL-BURNS 7300-14

MINIMUM START-UP VOLTAGE = 1.1V

LT1073 • TA36

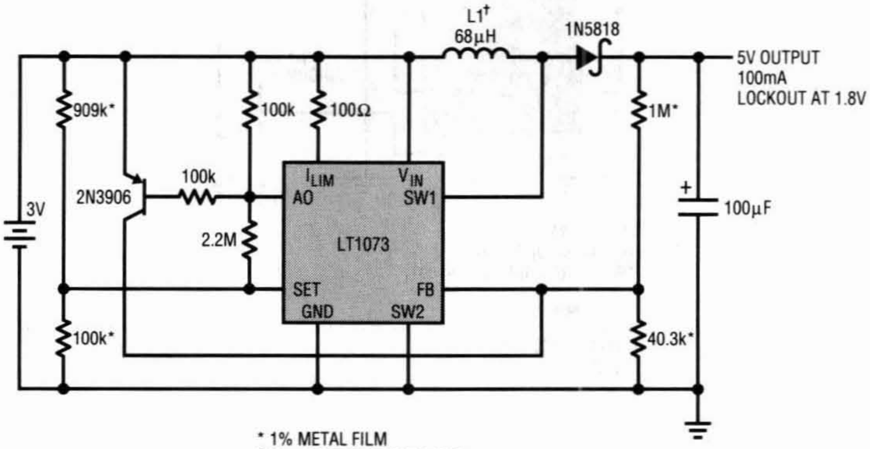
Memory Backup Supply


5V MAIN SUPPLY
5V TO MEMORY
4.5V WHEN MAIN
SUPPLY OPEN
L1†
82μH
1N5818
806k*
1.5V CELL
I_LIM
V_IN
SW1
LT1073
FB
GND
SW2
+
100μF**
40.2k*

* = 1% METAL FILM
** = OPTIONAL
†L1 = GOWANDA GA10-822k
OR CADDELL-BURNS 7300-12

LT1073 • TA38

3V to 5V Step-Up Converter with Under-Voltage Lockout

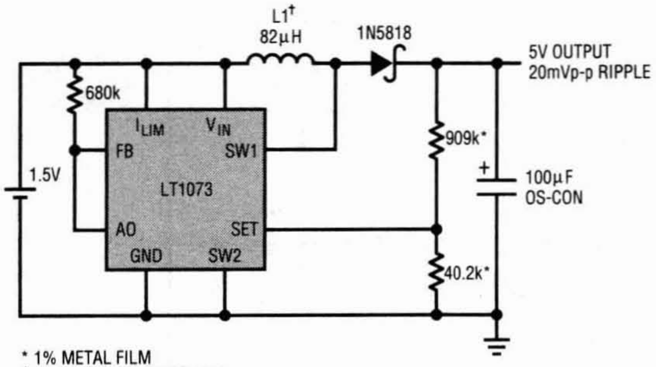

L1†
68μH
1N5818
5V OUTPUT
100mA
LOCKOUT AT 1.8V
909k*
100k
100Ω
1M*
2N3906
100k
I_LIM
AO
V_IN
SW1
3V
2.2M
LT1073
+
100μF
SET
GND
FB
SW2
100k*
40.3k*

* 1% METAL FILM
† L1 = GOWANDA GA10-682k
OR CADDELL-BURNS 7300-11

LT1073 • TA37

TYPICAL APPLICATIONS

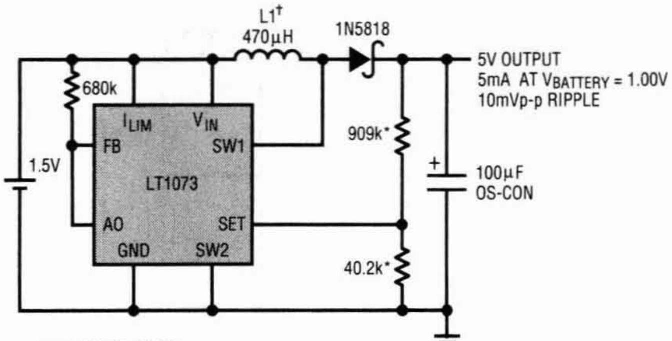
1.5V to 5V Low Noise Step-Up Converter


L1†
82µH
1N5818
5V OUTPUT
20mVp-p RIPPLE
680k
I_{LIM}
V_{IN}
FB
SW1
909k*
1.5V
LT1073
100µF
OS-CON
AO
SET
GND
SW2
40.2k*

* 1% METAL FILM
† L1 = GOWANDA GA10-822k
OR CADDELL-BURNS 7300-12

LT1073 • TA04

1.5V to 5V Very Low Noise Step-Up Converter

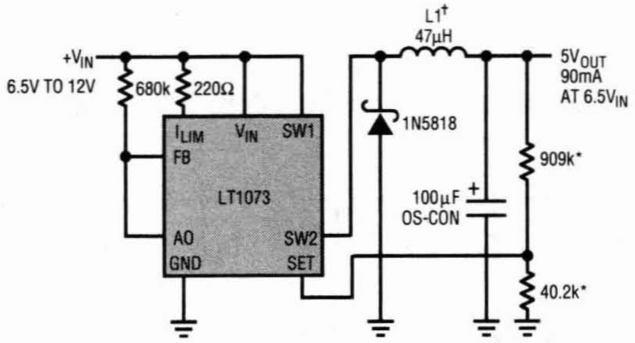

L1†
470µH
1N5818
5V OUTPUT
5mA AT $V_{BATTERY}$ = 1.00V
10mVp-p RIPPLE
680k
I_{LIM}
V_{IN}
FB
SW1
909k*
1.5V
LT1073
100µF
OS-CON
AO
SET
GND
SW2
40.2k*

* 1% METAL FILM
† L1 = GOWANDA GA10-473k
OR CADDELL-BURNS 7300-21

EFFICIENCY = 83% AT 5mA LOAD

LT1073 • TA05

9V to 5V Reduced Noise Step-Down Converter


L1†
47µH
$+V_{IN}$
6.5V TO 12V
680k
220Ω
$5V_{OUT}$
90mA
AT $6.5V_{IN}$
I_{LIM}
V_{IN}
SW1
FB
1N5818
909k*
LT1073
100µF
OS-CON
AO
SW2
GND
SET
40.2k*

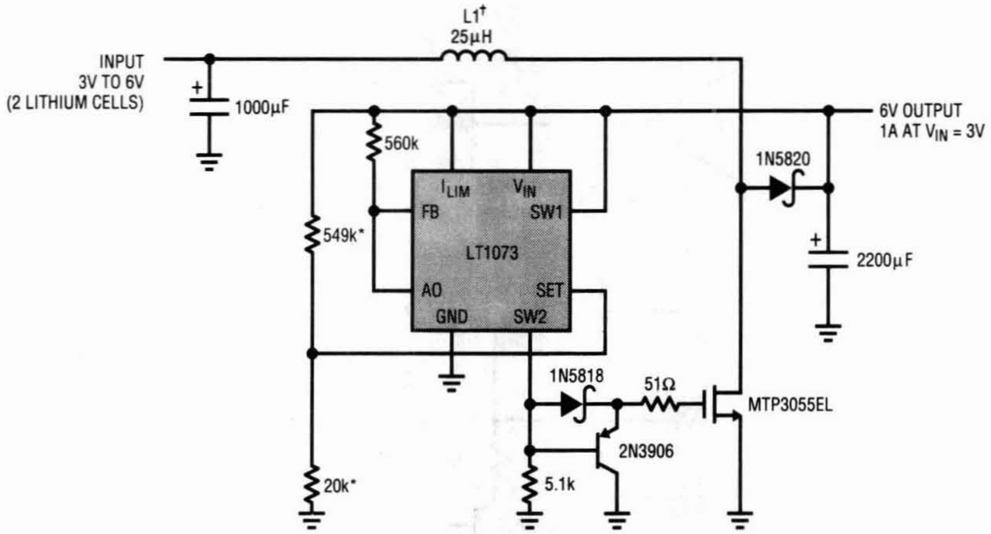
* 1% METAL FILM
† L1 = GOWANDA GA10-472k
OR CADDELL-BURNS 7300-09

EFFICIENCY ≈ 80%
$I_Q \approx 130\mu A$
OUTPUT NOISE ≈ 100mVp-p

LT1073 • TA06

TYPICAL APPLICATIONS

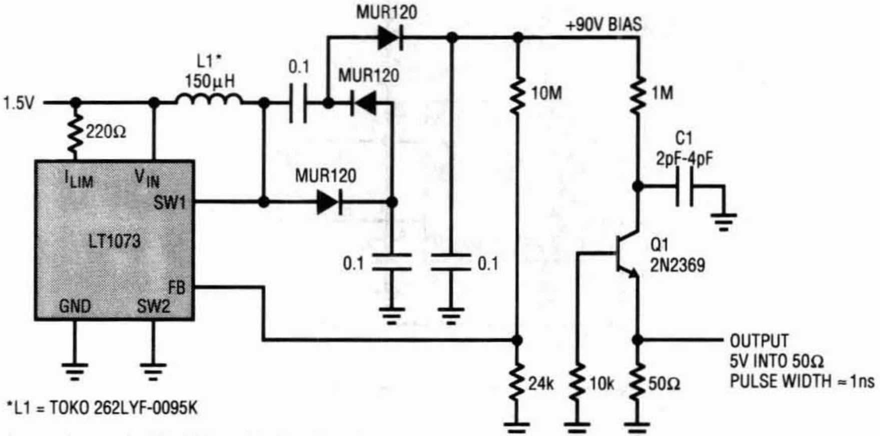
3V to 6V @ 1A Step-Up Converter


L1†
25μH
INPUT
3V TO 6V
(2 LITHIUM CELLS)
1000μF
560k
549k*
ILIM
VIN
FB
SW1
LT1073
AO
SET
GND
SW2
6V OUTPUT
1A AT VIN = 3V
1N5820
2200μF
1N5818
51Ω
MTP3055EL
2N3906
20k*
5.1k

* 1% METAL FILM
† L1 = COILTRONICS CTX25-5-52
LOW I_Q (< 250μA)

LT1073 • TA07

1.5V Powered 350ps Risetime Pulse Generator


MUR120
+90V BIAS
L1*
150μH
0.1
MUR120
1.5V
220Ω
10M
1M
C1
2pF-4pF
ILIM
VIN
SW1
MUR120
LT1073
Q1
2N2369
0.1
0.1
FB
GND
SW2
OUTPUT
5V INTO 50Ω
PULSE WIDTH ≈ 1ns
24k
10k
50Ω

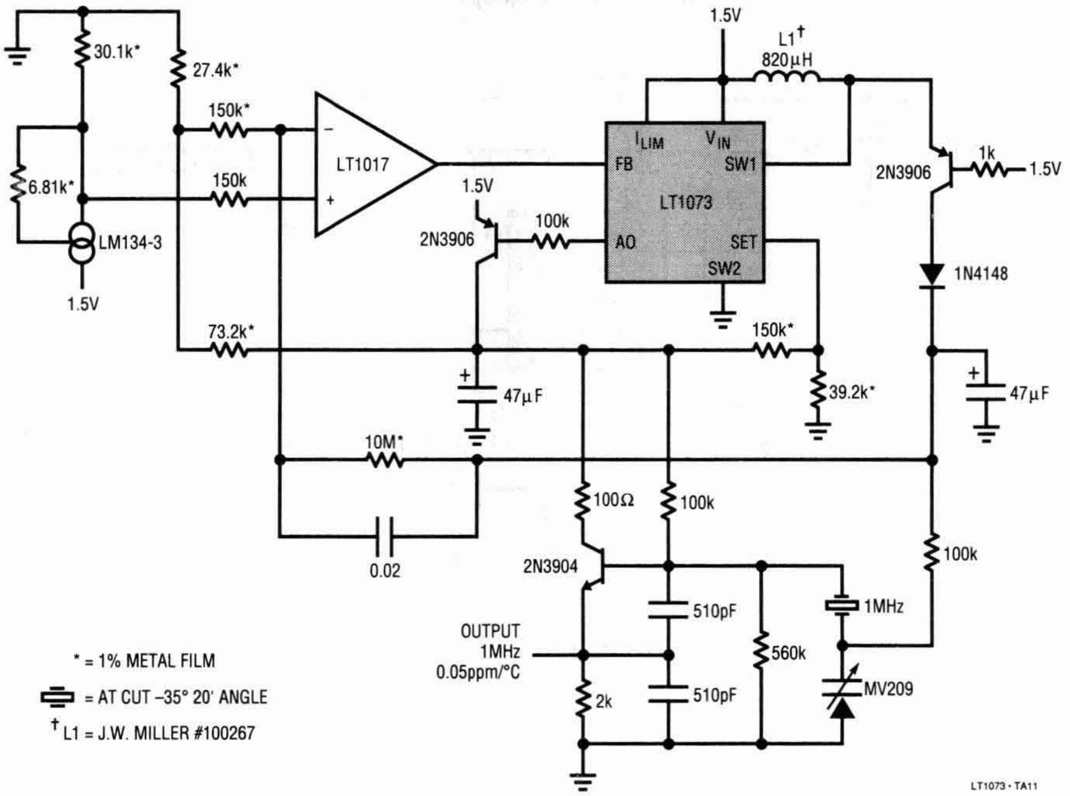
*L1 = TOKO 262LYF-0095K

SELECT Q1 AND C1 FOR OPTIMUM RISE AND FALL

LT1073 • TA08

TYPICAL APPLICATIONS

1.5V Powered Temperature Compensated Crystal Oscillator

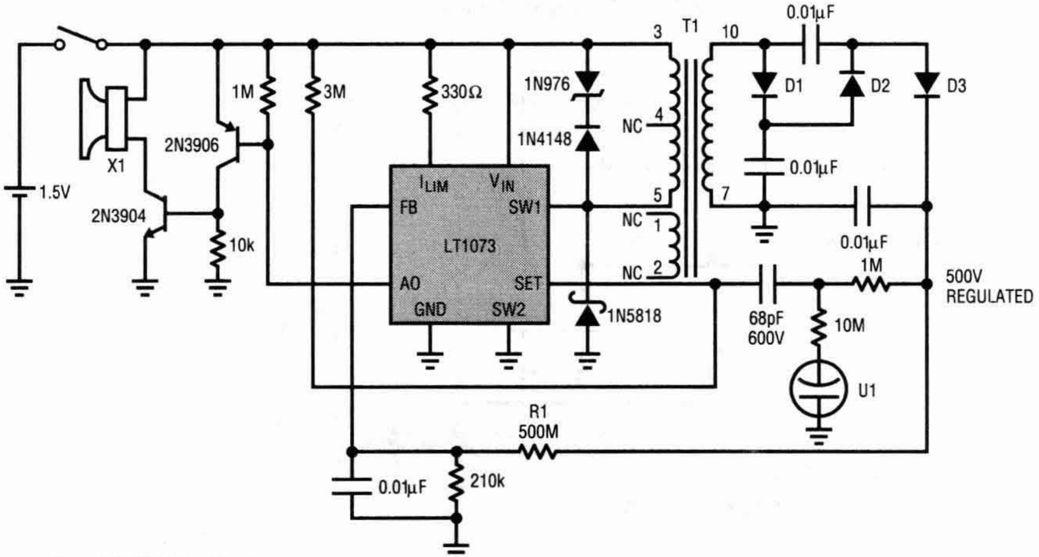

1.5V
L1†
820µH
30.1k*
27.4k*
150k*
150k
6.81k*
LM134-3
1.5V
LT1017
1.5V
2N3906
100k
I_LIM
V_IN
FB
SW1
LT1073
AO
SET
SW2
2N3906
1k
1.5V
1N4148
73.2k*
150k*
47µF
39.2k*
47µF
10M*
0.02
100Ω
100k
100k
2N3904
510pF
1MHz
OUTPUT
1MHz
0.05ppm/°C
560k
2k
510pF
MV209
LT1073 • TA11

* = 1% METAL FILM

= AT CUT –35° 20' ANGLE

† L1 = J.W. MILLER #100267

1.5V Powered α, β, γ Particle Detector


0.01µF
3
T1
10
1M
3M
330Ω
1N976
D1
D2
D3
X1
2N3906
1N4148
NC
4
0.01µF
1.5V
I_LIM
V_IN
FB
SW1
5
7
2N3904
LT1073
NC
1
0.01µF
10k
NC
2
1M
AO
SET
500V
REGULATED
GND
SW2
1N5818
68pF
600V
10M
U1
R1
500M
0.01µF
210k

T1 = COILTRONICS CTX10052-1
X1 = PROJECTS UNLIMITED AT-11k OR 8Ω SPEAKER
D1, D2, D3 = MUR1100
R1 = VICTOREEN MOX-300
U1 = LND-712 LND CORP., OCEANSIDE, NY

LT1073 • TA10

Step-Down Switching Regulator

FEATURES

- 5A On-Board Switch (LT1074)
- Up to 200kHz Switching Frequency
- Greatly Improved Dynamic Behavior
- Available in Low Cost 5-Lead Packages
- Only 8.5mA Quiescent Current
- Programmable Current Limit
- Operates Up to 60V Input
- Includes Output Voltage Monitor
- Micropower Shutdown Mode

APPLICATIONS

- Buck Converter with Output Voltage Range of 2.5V to 50V
- Tapped Inductor Buck Converter with 10A Output at 5V
- Positive-to-Negative Converter
- Negative Boost Converter
- Multiple Output Buck Converter

DESCRIPTION

The LT1074 is a 5A (LT1076 is rated at 2A) monolithic bipolar switching regulator which requires only a few external parts for normal operation. The power switch, all oscillator and control circuitry, all current limit components, and an output monitor are included on the chip. The topology is a classic positive "buck" configuration but several design innovations allow this device to be used as a positive to negative converter, a negative boost converter, and as a flyback converter. The switch output is specified to swing 40V below ground, allowing the LT1074 to drive a tapped inductor in the buck mode with output currents up to 10A.

The LT1074 uses a true analog multiplier in the feedback loop. This makes the device respond nearly instantaneously to input voltage fluctuations and makes loop gain independent of input voltage. As a result, dynamic behavior of the regulator is significantly improved over previous designs.

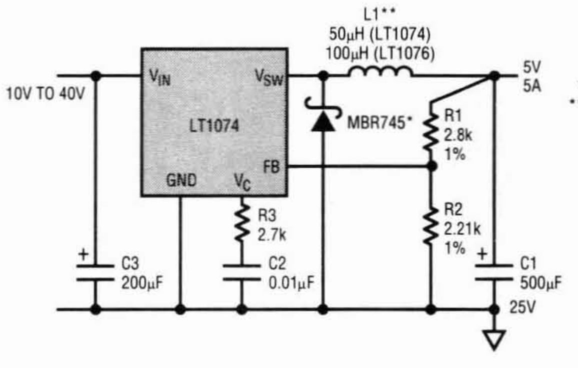
On-chip pulse by pulse current limiting makes the LT1074 nearly bust-proof for output overloads or shorts. The input voltage range as a buck converter is 8V to 60V, but a self-boot feature allows input voltages as low as 5V in the inverting and boost configurations.

The LT1074 is available in low cost 5-lead TO-220 or TO-3 packages with frequency pre-set at 100kHz and current limit at 6.5A (LT1076 = 2.6A). An 11-pin single-in-line package (SIP) is also available which allows switching frequency to be increased to 200kHz and current limit to be adjusted down to zero. In addition, full micropower shutdown can be programmed as well as external current sensing, and soft start. An output monitor "status" pin can be used as a microprocessor reset, and a complementary output pin will allow implementation of extra-high-efficiency designs. See Application Note 44 for design details.

A fixed 5V output, 2A version is also available. See LT1076-5.

TYPICAL APPLICATION

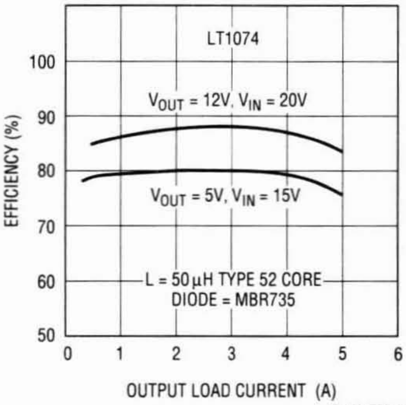
Basic Positive Buck Converter



*USE MBR340 FOR LT1076
**COILTRONICS #50-2-52 (LT1074)
#100-1-52 (LT1076)
PULSE ENGINEERING, INC.
#PE-92114 (LT1074)
#PE-92102 (LT1076)
HURRICANE #HL-AK147QQ (LT1074)
#HL-AG210LL (LT1076)

LT1074 • TA01

Buck Converter Efficiency



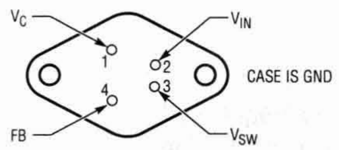
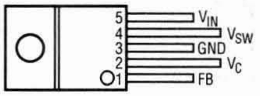
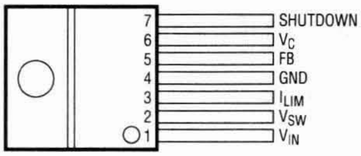
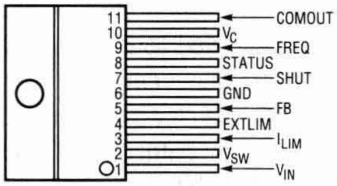
LT1074 • TPC27

ABSOLUTE MAXIMUM RATINGS

Input Voltage
 LT1074/ LT1076 .... 45V
 LT1074HV/76HV 64V
Switch Voltage with Respect to Input Voltage
 LT1074/ 76 .... 64V
 LT1074HV/76HV 75V
Switch Voltage with Respect to Ground Pin (V_{SW} **Negative**)
 LT1074/76 (Note 6) 35V
 LT1074HV/76HV (Note 6) 45V
Feedback Pin Voltage .... −2V, +10V
Shutdown Pin Voltage (Not to Exceed V_{IN}) 40V
Status Pin Voltage* 30V
 (Current Must Be Limited to 5mA When Status Pin Switches "On")
Complementary Output Voltage* 30V
 (Current Must Be Limited to 20mA When Output Switches "On")
I_{LIM} Pin Voltage (Forced) 5.5V
EXTLIM Pin Voltage* .... V_{IN} −2V to V_{IN} +0.4V
Freq Pin Voltage* 5.5V
Maximum Operating Ambient Temperature Range
 LT1074C/76C, LT1074HVC/76HVC .... 0°C to 70°C
 LT1074M/76M, LT1074HVM/76HVM ..−55°C to 125°C
 LT1074I/76I, LT1074HVI/76HVI .... −40°C to 85°C
Maximum Operating Junction Temperature Range
 LT1074C/76C, LT1074HVC/76HVC .... 0°C to 125°C
 LT1074M/76M, LT1074HVM/76HVM ...−55°C to 150°C
 LT1074I/76I, LT1074HVI/76HVI .... −40°C to 125°C
Maximum Storage Temperature .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

*** Refers to pins on the 11-pin package, which is not recommended for new designs.**

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  V_C V_{IN} 1 2 3 4 CASE IS GND FB V_{SW} K PACKAGE 4-LEAD TO-3 METAL CAN	LT1074MK LT1074CK LT1074HVCK LT1076MK
FRONT VIEW  5 4 3 2 1 V_{IN} V_{SW} GND V_C FB T PACKAGE 5-LEAD TO-220 LEADS ARE FORMED STANDARD. FOR STRAIGHT LEADS, ORDER FLOW 06.	LT1074CT LT1074HVCT LT1076CT LT1076HVCT LT1074IT LT1074HVIT LT1076IT LT1076HVIT
FRONT VIEW  7 6 5 4 3 2 1 SHUTDOWN V_C FB GND I_{LIM} V_{SW} V_{IN} Y PACKAGE 7-LEAD TO-220	LT1074CY
FRONT VIEW  11 10 9 8 7 6 5 4 3 2 1 COMOUT V_C FREQ STATUS SHUT GND FB EXTLIM I_{LIM} V_{SW} V_{IN} V PACKAGE 11-LEAD SIP CASE IS CONNECTED TO GROUND. LEADS ARE FORMED.	LT1074CV LT1074HVCV LT1076CV LT1076HVCV

ELECTRICAL CHARACTERISTICS

T_j = 25°C, V_{IN} = 25V, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Switch "On" Voltage (Note 1)	LT1074	I_{SW} = 1A, $T_j \geq$ 0°C				1.85	V
		I_{SW} = 1A, $T_j <$ 0°C				2.10	V
		I_{SW} = 5A, $T_j \geq$ 0°C				2.30	V
		I_{SW} = 5A, $T_j <$ 0°C				2.50	V
	LT1076	I_{SW} = 0.5A	●			1.2	V
		I_{SW} = 2A	●			1.7	V
Switch "Off" Leakage	LT1074	$V_{IN} \leq$ 25V, V_{SW} = 0			5	300	µA
		V_{IN} = V_{MAX}, V_{SW} = 0 (Note 7)			10	500	µA
	LT1076	V_{IN} = 25V, V_{SW} = 0				150	µA
		V_{IN} = V_{MAX}, V_{SW} = 0 (Note 7)				250	µA
Supply Current (Note 2)	V_{FB} = 2.5V, $V_{IN} \leq$ 40V		●		8.5	11	mA
	40V < V_{IN} < 60V		●		9	12	mA
	V_{SHUT} = 0.1V (Device Shutdown) (Note 8)		●		140	300	µA

ELECTRICAL CHARACTERISTICS $T_j = 25°C$, $V_{IN} = 25V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Supply Voltage	Normal Mode	●		7.3	8.0	V
	Startup Mode (Note 3)	●		3.5	4.8	V
Switch Current Limit (Note 4)	LT1074 I_{LIM} Open	●	5.5	6.5	8.5	A
	R_{LIM} = 10k (Note 5)			4.5		A
	R_{LIM} = 7k (Note 5)			3		A
	LT1076 I_{LIM} Open	●	2	2.6	3.2	A
	R_{LIM} = 10k (Note 5)			1.8		A
	R_{LIM} = 7k (Note 5)			1.2		A
Maximum Duty Cycle		●	85	90		%
Switching Frequency			90	100	110	kHz
	$T_j \le 125°C$	●	85		120	kHz
	$T_j > 125°C$	●	85		125	kHz
	V_{FB} = 0V through 2kΩ (Note 4)			20		kHz
Switching Frequency Line Regulation	$8V \le V_{IN} \le V_{MAX}$ (Note 7)	●		0.03	0.1	%/V
Error Amplifier Voltage Gain (Note 6)	$1V \le V_C \le 4V$			2000		V/V
Error Amplifier Transconductance			3700	5000	8000	μmho
Error Amplifier Source and Sink Current	Source (V_{FB} = 2V)		100	140	225	μA
	Sink (V_{FB} = 2.5V)		0.7	1	1.6	mA
Feedback Pin Bias Current	$V_{FB} = V_{REF}$	●		0.5	2	μA
Reference Voltage	V_C = 2V	●	2.155	2.21	2.265	V
Reference Voltage Tolerance	V_{REF} (Nominal) = 2.21V			±0.5	±1.5	%
	All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	●		±1	±2.5	%
Reference Voltage Line Regulation	$8V \le V_{IN} \le V_{MAX}$ (Note 7)	●		0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle				1.5		V
	Over Temperature	●		−4		mV/°C
Multiplier Reference Voltage				24		V
Shutdown Pin Current	V_{SH} = 5V	●	5	10	20	μA
	$V_{SH} \le V_{THRESHOLD}$ (≅2.5V)	●			50	μA
Shutdown Thresholds	Switch Duty Cycle = 0	●	2.2	2.45	2.7	V
	Fully Shut Down	●	0.1	0.3	0.5	V
Status Window*	As a Percent of Feedback Voltage		4	±5	6	%
Status High Level*	I_{STATUS} = 10μA Sourcing	●	3.5	4.5	5.0	V
Status Low Level*	I_{STATUS} = 1.6mA Sinking	●		0.25	0.4	V
Status Delay Time*				9		μs
Status Minimum Width*				30		μs
Freq Pin Voltage*	R_{FREQ} = 15k			1.55		V
COMOUT Saturation Voltage*	I_{SINK} = 10mA	●		0.5	1	V
COMOUT Leakage*	V_{COMOUT} = 30V	●			50	μA
Thermal Resistance Junction to Case	LT1074				2.5	°C/W
	LT1076				4.0	°C/W

*** Refers to pins on the 11-pin package, which is not recommended for new designs.**

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "on" voltage at currents between low and high conditions, a linear interpolation may be used.

Note 2: A feedback pin voltage (V_{FB}) of 2.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero.

Note 3: Total voltage from V_{IN} pin to ground pin must be ≥ 8V after startup for proper regulation. For $T_A < 25°C$, limit = 5V.

Note 4: Switch frequency is internally scaled down when the feedback pin voltage is less than 1.3V to avoid extremely short switch on times. During testing, V_{FB} is adjusted to give a minimum switch on time of 1μs.

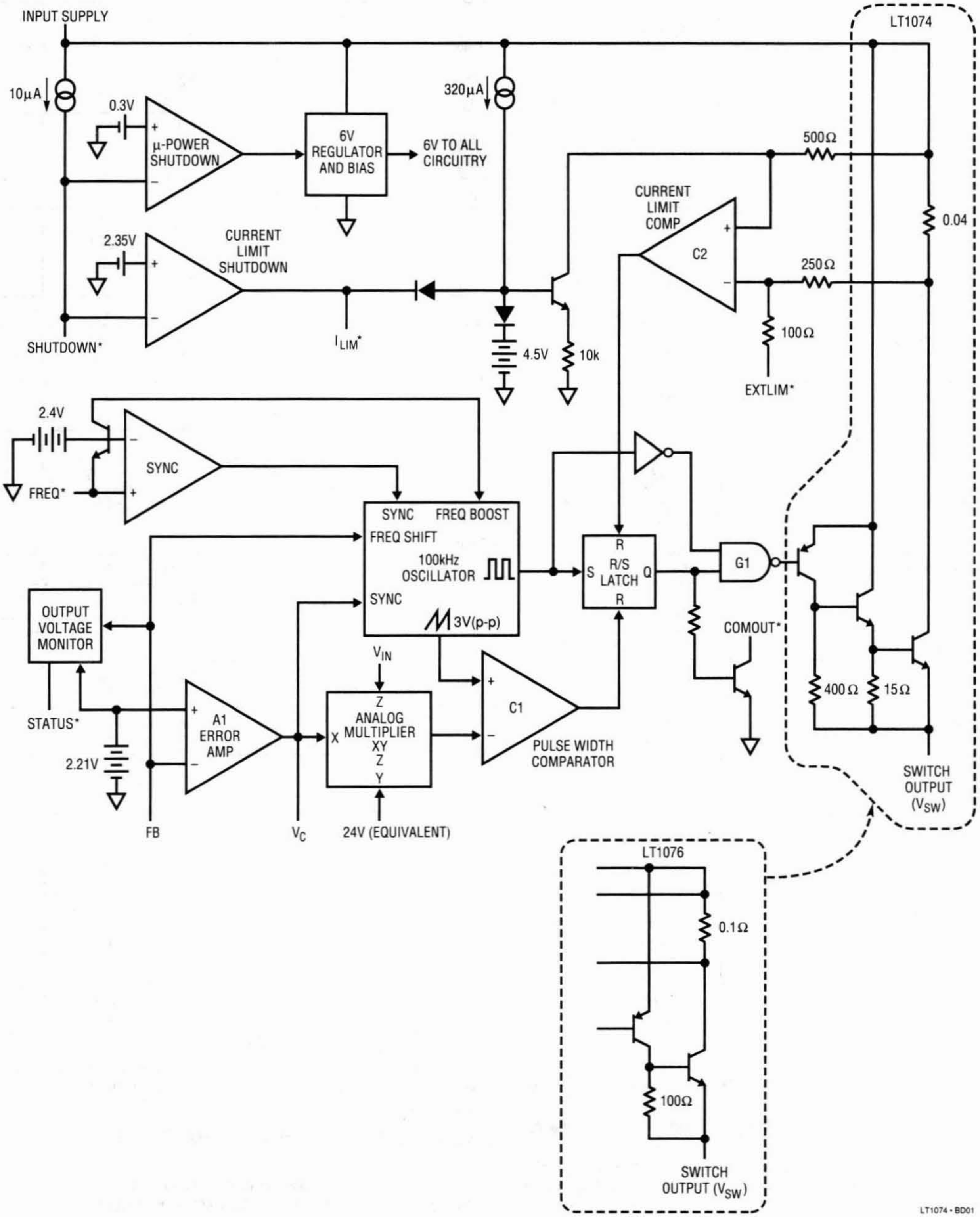
Note 5: $I_{LIM} \approx \frac{R_{LIM} - 1k}{2k}$ (LT1074), $I_{LIM} \approx \frac{R_{LIM} - 1k}{5.5k}$ (LT1076).

Note 6: Switch to input voltage limitation must also be observed.

Note 7: V_{MAX} = 40V for the LT1074/76 and 60V for the LT1074HV/76HV.

Note 8: Does not include switch leakage.

BLOCK DIAGRAM


INPUT SUPPLY
LT1074
10μA
0.3V
μ-POWER SHUTDOWN
6V REGULATOR AND BIAS
6V TO ALL CIRCUITRY
320μA
500Ω
CURRENT LIMIT COMP
C2
0.04
2.35V
CURRENT LIMIT SHUTDOWN
250Ω
100Ω
SHUTDOWN*
I_{LIM}*
4.5V
10k
EXTLIM*
2.4V
SYNC
FREQ*
SYNC
FREQ BOOST
FREQ SHIFT
100kHz OSCILLATOR
SYNC
3V(p-p)
S
R
R/S LATCH
Q
R
G1
COMOUT*
OUTPUT VOLTAGE MONITOR
STATUS*
V_{IN}
A1 ERROR AMP
2.21V
Z
X
ANALOG MULTIPLIER
XY
Z
Y
C1
PULSE WIDTH COMPARATOR
400Ω
15Ω
SWITCH OUTPUT (V_{SW})
FB
V_C
24V (EQUIVALENT)
LT1076
0.1Ω
100Ω
SWITCH OUTPUT (V_{SW})
LT1074 • BD01

***Available only on the 11-pin package, which is not recommended for new designs.**

BLOCK DIAGRAM DESCRIPTION

A switch cycle in the LT1074 is initiated by the oscillator setting the R/S latch. The pulse that sets the latch also locks out the switch via gate G1. The effective width of this pulse is approximately 700ns, which sets the maximum switch duty cycle to approximately 93% at 100kHz switching frequency. The switch is turned off by comparator C1, which resets the latch. C1 has a sawtooth waveform as one input and the output of an analog multiplier as the other input. The multiplier output is the product of an internal reference voltage, and the output of the error amplifier, A1, divided by the regulator input voltage. In standard buck regulators, this means that the output voltage of A1 required to keep a constant regulated output is independent of regulator input voltage. This greatly improves line transient response, and makes loop gain independent of input voltage. The error amplifier is a transconductance type with a G_M at null of approximately 5000µmho. Slew current going positive is 140µA, while negative slew current is about 1.1mA. This asymmetry helps prevent overshoot on startup. Overall loop frequency compensation is accomplished with a series RC network from V_C to ground.

Switch current is continuously monitored by C2, which resets the R/S latch to turn the switch off if an overcurrent condition occurs. The time required for detection and switch turn off is approximately 600ns. So minimum switch "on" time in current limit is 600ns. Under dead shorted output conditions, switch duty cycle may have to be as low as 2% to maintain control of output current. This would require switch on time of 200ns at 100kHz switching frequency, so frequency is reduced at very low output voltages by feeding the FB signal into the oscillator and creating a linear frequency downshift when the FB signal drops below 1.3V. Current trip level is set by the voltage on the I_{LIM} pin which is driven by an internal 320µA current source. When this pin is left open, it self-clamps at about 4.5V and sets current limit at 6.5A for the LT1074 and 2.6A for the LT1076. An external resistor can be connected from the I_{LIM} pin to ground to set a lower current limit. A capacitor in parallel with this resistor will soft start the current limit. A slight offset in C2 guarantees that when the I_{LIM} pin is pulled to within 200mV of ground, C2 output will stay high and force switch duty cycle to zero.

An output voltage monitor is included on the chip. Its output is available only on the 11-pin* version. The monitor output* goes low when the voltage on the FB pin is more than 5% above or below the normal regulated value. This pin can be used to "hold off" load functions until the regulator output is normal or it can be used as a microprocessor reset.

The "Freq" pin* is used to raise switching frequency, and to synchronize the oscillator to an external signal. A resistor to ground will raise frequency. A 3V-5V pulse coupled through a diode will synchronize the internal oscillator from 110% to 160% of its normal frequency. The pulse should be 300ns wide. Synchronizing can also be done with the 5-lead LT1074 by pulling the V_C pin to ground for 300ns with a transistor. This has only a slight effect on regulated output voltage if the series resistor in the frequency compensation network is at least 1kΩ.

The "Shutdown" pin is used to force switch duty cycle to zero by pulling the I_{LIM} pin low, or to completely shut down the regulator. Threshold for the former is approximately 2.35V, and for complete shutdown, approximately 0.3V. Total supply current in shutdown is about 150µA. A 10µA pull-up current forces the shutdown pin high when left open. A capacitor can be used to generate delayed startup. A resistor divider will program "undervoltage lockout" if the divider voltage is set at 2.35V when the input is at the desired trip point.

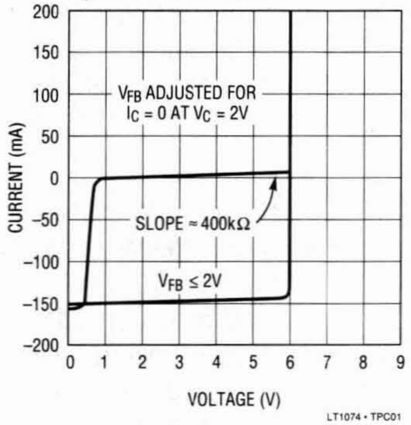
The "Comout" pin* is an open collector switch whose voltage is the complement of the switch output (V_{SW}). In addition, the edges of Comout are slightly time-shifted to avoid overlap with V_{SW}. Comout is used to drive external MOSFETs in certain mutliple-output and high efficiency applications.

The switch used in the LT1074 is a Darlington NPN (single NPN for LT1076) driven by a saturated PNP. Special patented circuitry is used to drive the PNP on and off very quickly even from the saturation state. This particular switch arrangement has no "isolation tubs" connected to the switch output, which can therefore swing to 40V below ground.

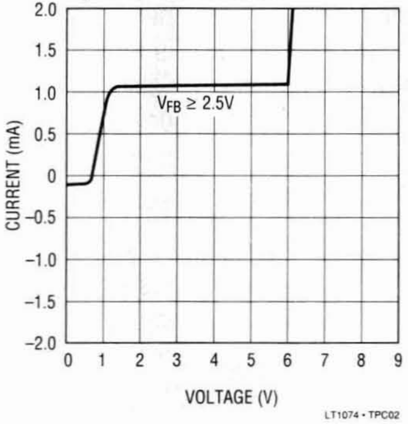
***Available only on the 11-pin package, which is not recommended for new designs.**

TYPICAL PERFORMANCE CHARACTERISTICS

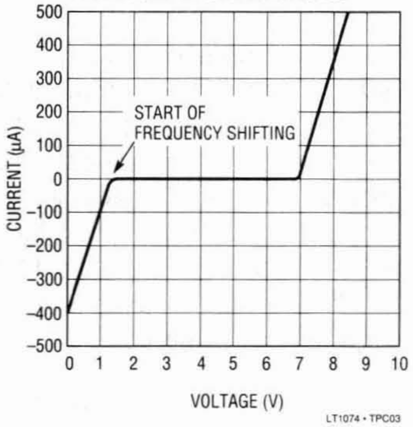
V_C Pin Characteristics



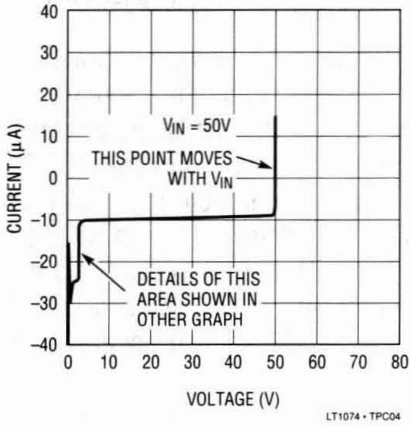
V_C Pin Characteristics



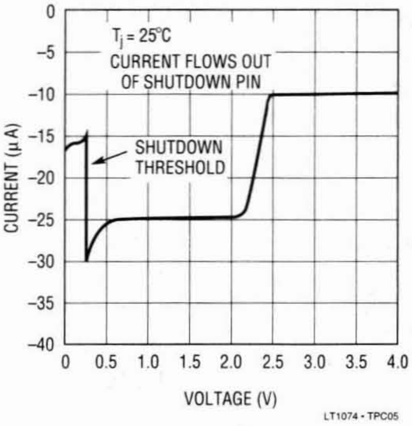
Feedback Pin Characteristics



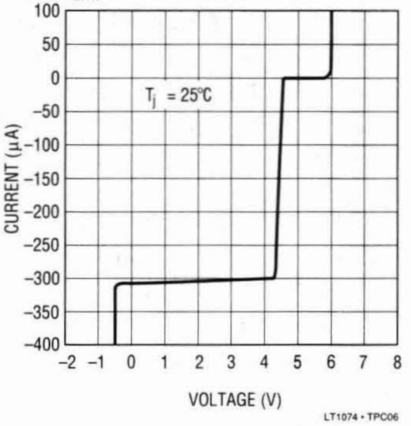
Shutdown Pin Characteristics



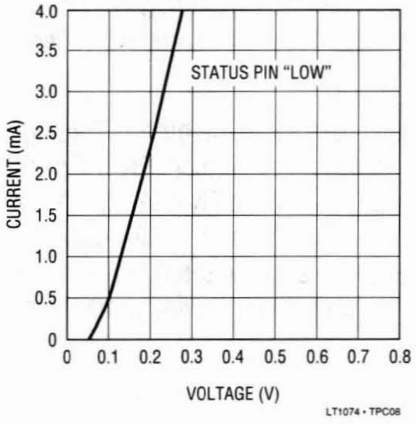
Shutdown Pin Characteristics



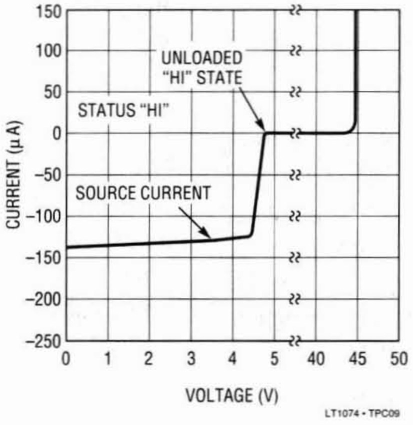
I_{LIM} Pin Characteristics



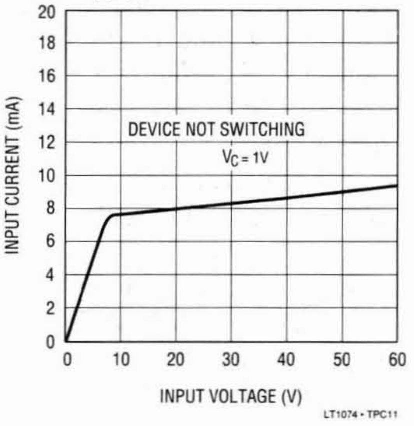
Status Pin Characteristics



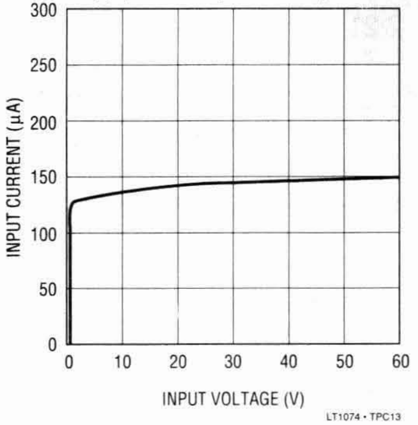
Status Pin Characteristics

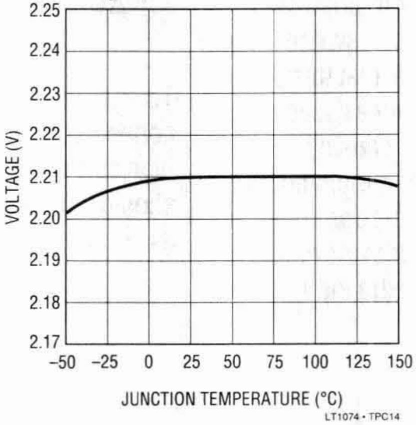


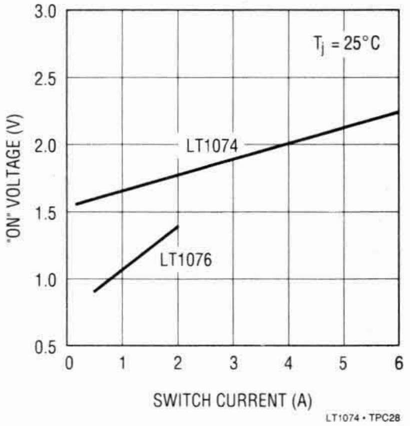
Supply Current

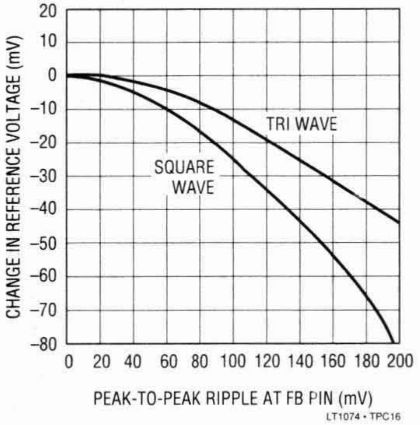


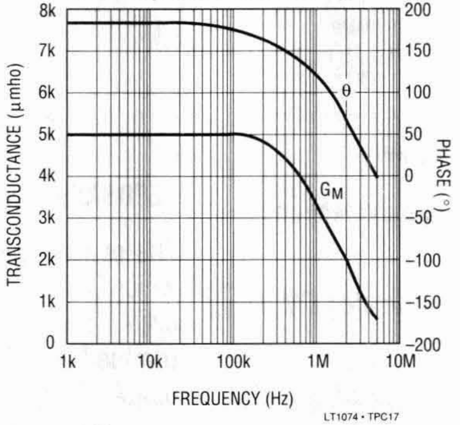
TYPICAL PERFORMANCE CHARACTERISTICS

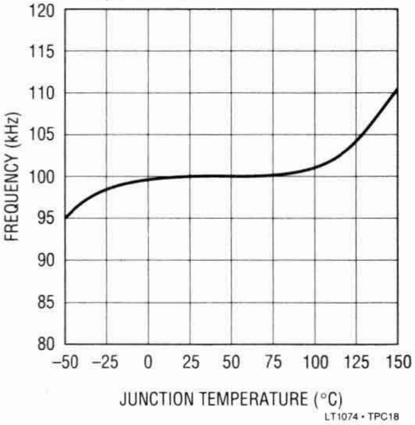

Supply Current (Shutdown)

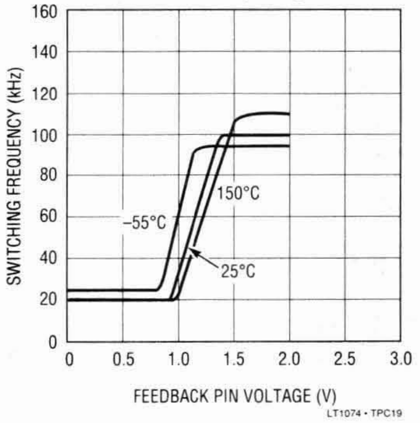

Reference Voltage vs Temperature

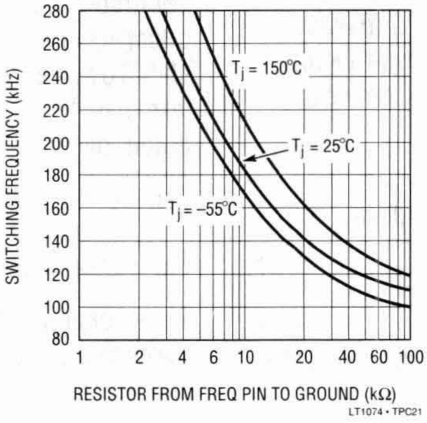

Switch "On" Voltage

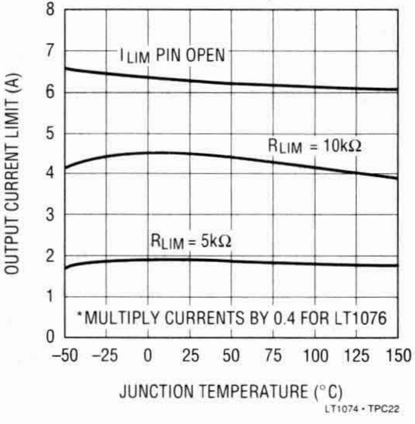

Reference Shift with Ripple Voltage


Error Amplifier Phase and G_M


Switching Frequency vs Temperature


Feedback Pin Frequency Shift


Frequency Boost


Current Limit vs Temperature*

PIN DESCRIPTIONS

V_{IN} PIN

The V_{IN} pin is both the supply voltage for internal control circuitry and one end of the high current switch. It is important, *especially at low input voltages*, that this pin be bypassed with a low ESR, and low inductance capacitor to prevent transient steps or spikes from causing erratic operation. At full switch current of 5A, the switching transients at the regulator input can get very large as shown in Figure 1. Place the input capacitor very close to the regulator and connect it with wide traces to avoid extra inductance. Use radial lead capacitors.

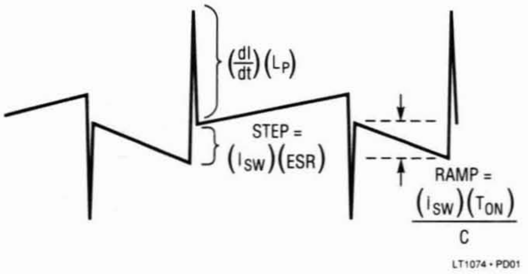


Figure 1. Input Capacitor Ripple

L_P = Total inductance in input bypass connections and capacitor.

"Spike" height $\left(\frac{dI}{dt} \bullet L_P\right)$ is approximately 2V *per inch* of lead length.

Step = 0.25V for ESR = 0.05Ω and I_{SW} = 5A is 0.25V.

Ramp = 125mV for C = 200µF, T_{ON} = 5µs, and I_{SW} = 5A is 125mV.

Input current on the V_{IN} Pin in shutdown mode is the sum of actual supply current (≈140µA, with a maximum of 300µA) and switch leakage current. Consult factory for special testing if shutdown mode input current is critical.

GROUND PIN

It might seem unusual to describe a ground pin, but in the case of regulators, the ground pin must be connected properly to ensure good load regulation. The internal reference voltage is referenced to the ground pin; so any error in ground pin voltage will be multiplied at the output;

$$\Delta V_{OUT} = \frac{(\Delta V_{GND})(V_{OUT})}{2.21}$$

To ensure good load regulation, the ground pin must be connected directly to the proper output node, so that no high currents flow in this path. The output divider resistor should also be connected to this low current connection line as shown in Figure 2.

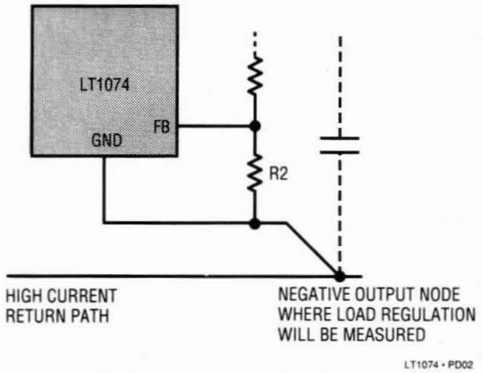


Figure 2. Proper Ground Pin Connection

FEEDBACK PIN

The feedback pin is the inverting input of an error amplifier which controls the regulator output by adjusting duty cycle. The non-inverting input is internally connected to a trimmed 2.21V reference. Input bias current is typically 0.5µA when the error amplifier is balanced (I_{OUT} = 0). The error amplifier has asymmetrical G_M for large input signals to reduce startup overshoot. This makes the amplifier more sensitive to large ripple voltages at the feedback pin. 100mVp-p ripple at the feedback pin will create a 14mV offset in the amplifier, equivalent to a 0.7% output voltage shift. To avoid output errors, output ripple (p-p) should be less than 4% of DC output voltage at the point where the output divider is connected.

See the "Error Amplifier" section for more details.

Frequency Shifting at the Feedback Pin

The error amplifier feedback pin (FB) is used to downshift the oscillator frequency when the regulator output voltage

PIN DESCRIPTIONS

is low. This is done to guarantee that output short circuit current is well controlled even when switch duty cycle must be extremely low. Theoretical switch "on" time for a buck converter in continuous mode is;

$$t_{ON} = \frac{V_{OUT} + V_D}{V_{IN} \bullet f}$$

V_D = Catch diode forward voltage ($\approx$ 0.5V)
f = Switching frequency

At f = 100kHz, t_{ON} must drop to 0.2µs when V_{IN} = 25V and the output is shorted (V_{OUT} = 0V). In current limit, the LT1074 can reduce t_{ON} to a minimum value of $\approx$ 0.6µs, much too long to control current correctly for V_{OUT} = 0. To correct this problem, switching frequency is lowered from 100kHz to 20kHz as the FB pin drops from 1.3V to 0.5V. This is accomplished by the circuitry shown in Figure 3.

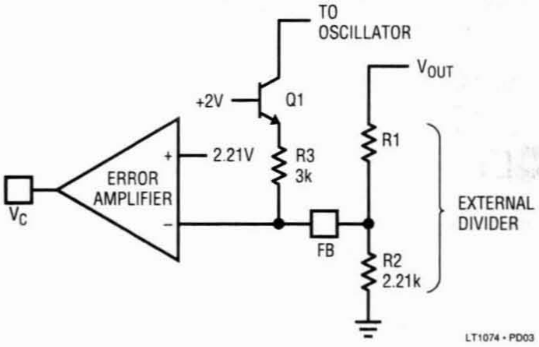


Figure 3. Frequency Shifting

Q1 is off when the output is regulating (V_{FB} = 2.21V). As the output is pulled down by an overload, V_{FB} will eventually reach 1.3V, turning on Q1. As the output continues to drop, Q1 current increases proportionately and lowers the frequency of the oscillator. Frequency shifting starts when the output is $\approx$ 60% of normal value, and is down to its minimum value of $\cong$ 20kHz when the output is $\cong$ 20% of normal value. The rate at which frequency is shifted is determined by both the internal 3k resistor R3 and the external divider resistors. For this reason, R2 should not be increased to more than 4kΩ, if the LT1074 will be subjected to the simultaneous conditions of high input voltage and output short circuit.

Frequency Pin*

The frequency pin can be used to raise switching frequency either by drawing a DC current to ground through a resistor or by feeding in a synchronizing pulse as shown in Figure 4. They can also be done simultaneously. The resistor pulls current through Q_A to increase oscillator ramp current. A pulse fed into the FREQ pin will toggle the sync comparator which will synchronize the oscillator. Figure 5 shows switching frequency versus temperature and resistance value.

A logic level pulse through a diode will synchronize the internal oscillator over a range equal to actual internal frequency up to 1.9 times that frequency. This does *not* mean that an unboosted LT1074 can always be synchronized at 100kHz because the actual switching frequency over temperature can range from 90kHz to 110kHz. Units above 100kHz would not synchronize at 100kHz. Designed synchronizing frequency must be higher than the *maximum* unsynchronized frequency and lower than 1.8 times the *minimum* unsynchronized frequency. For an unboosted unit, this would be 115kHz to 171kHz.

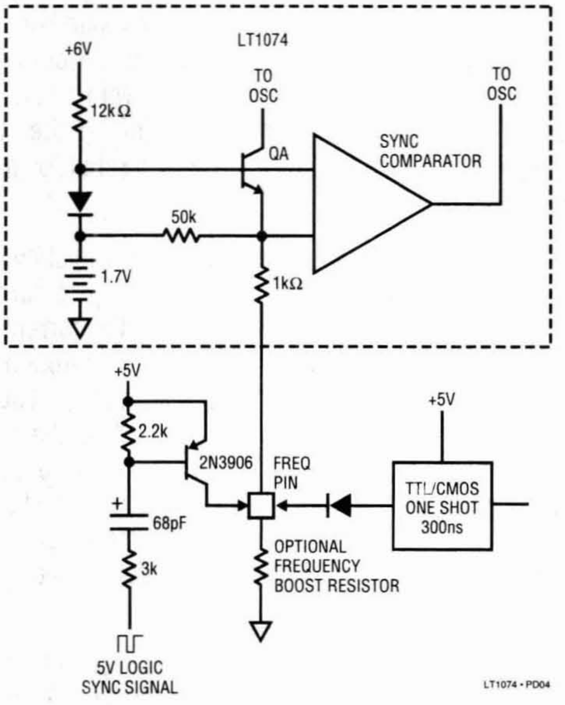


Figure 4. Frequency Pin

***Available only on the 11-pin package, which is not recommended for new designs.**

PIN DESCRIPTIONS

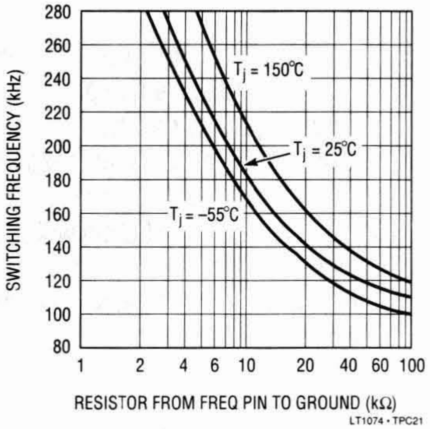


Figure 5. Frequency Boost

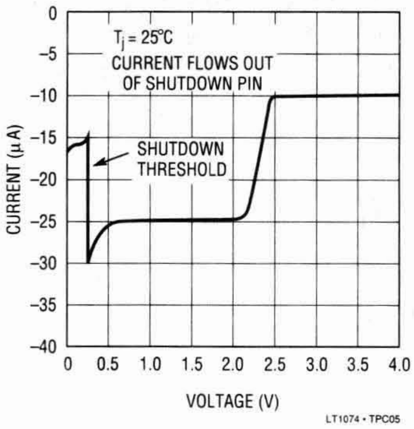


Figure 6. Shutdown Pin Characteristics

The synchronizing pulse should be ≅ 300ns wide. Figure 4 shows how this can be generated with a PNP transistor when the synchronizing signal is wider than 300ns. If a logic one-shot is used, couple it with a diode as shown in Figure 4.

SHUTDOWN PIN

The shutdown pin is used for undervoltage lockout, micropower shutdown, soft start, delayed start, or as a general purpose on/off control of the regulator output. It controls switching action by pulling the I_{LIM} pin low, which forces the switch to a continuous "off" state. Full micropower shutdown is initiated when the shutdown pin drops below 0.3V.

The V/I characteristics of the shutdown pin are shown in Figure 6. For voltages between 2.5V and ≈V_{IN}, a current of 10μA flows *out* of the shutdown pin. This current increases to ≈25μA as the shutdown pin moves through the 2.35V threshold. The current increases further to ≈ 30μA at the 0.3V threshold, then drops to ≈15μA as the shutdown voltage falls below 0.3V. The 10μA current source is included to pull the shutdown pin to its high or default state when left open. It also provides a convenient pullup for delayed start applications with a capacitor on the shutdown pin.

When activated, the typical collector current of Q1 in Figure 7, is ≈ 2mA. A soft start capacitor on the I_{LIM} pin will delay regulator shutdown in response to C1, by ≈(5V)(C_{LIM})/2mA. Soft start after full micropower shutdown is ensured by coupling C2 to Q1.

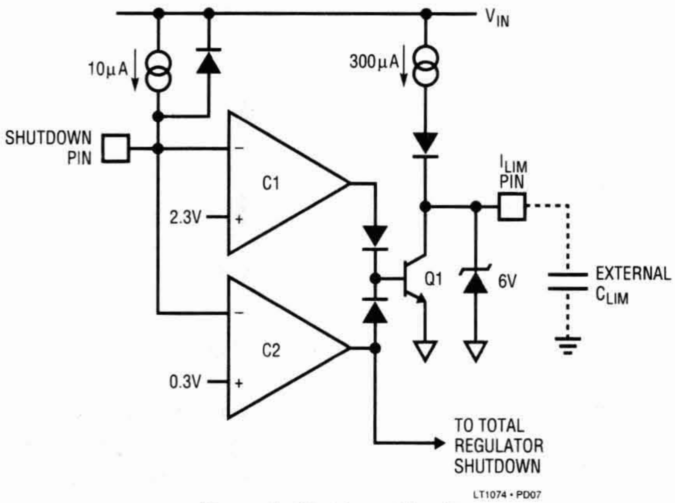


Figure 7. Shutdown Circuitry

Undervoltage Lockout

Undervoltage lockout point is set by R1 and R2 in Figure 8. To avoid errors due to the 10μA shutdown pin current, R2 is usually set at 5k, and R1 is found from:

$$R1 = R2\frac{(V_{TP} - V_{SH})}{V_{SH}}$$

V_{TP} = Desired undervoltage lockout voltage.

V_{SH} = Threshold for lockout on the shutdown pin = 2.45V.

PIN DESCRIPTIONS

If quiescent supply current is critical, R2 may be increased up to 15kΩ, but the denominator in the formula for R2 should replace V_{SH} with $V_{SH} - (10\mu A)(R2)$.

Hysteresis in undervoltage lockout may be accomplished by connecting a resistor (R3) from the I_{LIM} pin to the shutdown pin as shown in Figure 9. D1 prevents the shutdown divider from altering current limit.

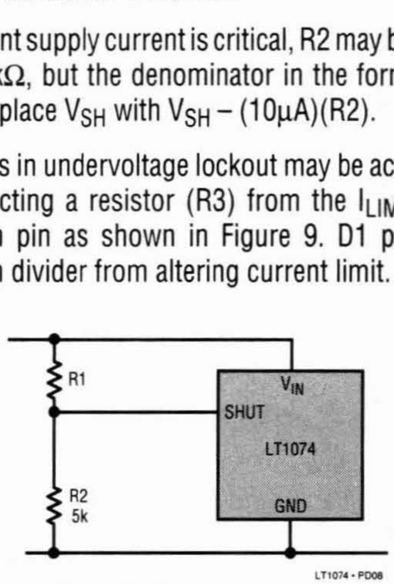
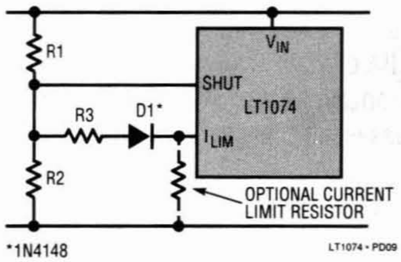

R1
R2
5k
V_{IN}
SHUT
LT1074
GND
LT1074 • PD08

Figure 8. Undervoltage Lockout


R1
R2
R3
D1*
V_{IN}
SHUT
LT1074
I_{LIM}
OPTIONAL CURRENT LIMIT RESISTOR
LT1074 • PD09

*1N4148

Figure 9. Adding Hysteresis

$$\text{Trip Point} = V_{TP} = 2.35V\left(1 + \frac{R1}{R2}\right)$$

If R3 is added, the lower trip point (V_{IN} descending) will be the same. The upper trip point (V_{UTP}) will be;

$$V_{UTP} = V_{SH}\left(1 + \frac{R1}{R2} + \frac{R1}{R3}\right) - 0.8V\left(\frac{R1}{R3}\right)$$

If R1 and R2 are chosen, R3 is given by

$$R3 = \frac{(V_{SH} - 0.8V)(R1)}{V_{UTP} - V_{SH}\left(1 + \dfrac{R1}{R2}\right)}$$

Example: An undervoltage lockout is required such that the output will not start until V_{IN} = 20V, but will continue to operate until V_{IN} drops to 15V. Let R2 = 2.32k.

$$R1 = (2.32k)\frac{(15V - 2.35V)}{2.35V} = 12.5k$$

$$R3 = \frac{(2.35 - 0.8)(12.5)}{20 - 2.35\left(1 + \dfrac{12.5}{2.32}\right)} = 3.9k$$

STATUS PIN*

The status pin is the output of a voltage monitor "looking" at the feedback pin. It is low for a feedback voltage which is more than 5% above or below nominal. "Nominal" in this case means the internal reference voltage, so that the ±5% window tracks the reference voltage. A time delay of ≈ 10µs prevents short spikes from tripping the status low. Once it does go low, a second timer forces it to stay low for a minimum of ≈ 30µs.

The status pin is modeled in Figure 10 with a 130µA pullup to a 4.5V clamp level. The sinking drive is a saturated NPN

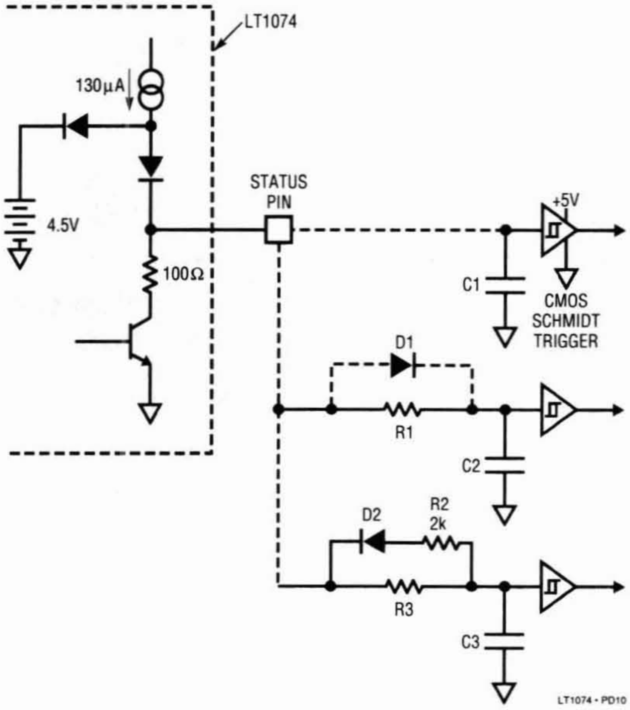

LT1074
130µA
4.5V
100Ω
STATUS PIN
+5V
C1
CMOS SCHMIDT TRIGGER
D1
R1
C2
D2
R2
2k
R3
C3
LT1074 • PD10

Figure 10. Adding Time Delays to Status Output

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*Available only on the 11-pin package, which is not recommended for new designs.

PIN DESCRIPTIONS

with ≈100Ω resistance and a maximum sink current of approximately 5mA. An external pullup resistor can be added to increase output swing up to a maximum of 20V.

When the status pin is used to indicate "output OK," it becomes important to test for conditions which might create unwanted status states. These include output overshoot, large signal transient conditions, and excessive output ripple. "False" tripping of the status pin can usually be controlled by a pulse stretcher network as shown in Figure 10. A single capacitor (C1) will suffice to delay an output "OK" (status high) signal to avoid false "true" signals during start-up, etc. Delay time for status high will be approximately (2.3×10^4) (C1), or 23ms/µF. Status low delay will be much shorter, ≈ 600µs/µF.

If false tripping of status "low" could be a problem, R1 can be added. Delay of status high remains the same if R1 ≤ 10kΩ. Status low delay is extended by R1 to approximately R1 • C2 seconds. Select C2 for high delay and R1 for low delay.

Example: Delay status high for 10ms, and status low for 3ms.

$$C2 = \frac{10\text{ms}}{23\text{ms}/\mu\text{F}} = 0.47\mu\text{F}\ (\text{Use } 0.47\mu\text{F})$$

$$R1 = \frac{3\text{ms}}{C2} = \frac{3\text{ms}}{0.47\mu\text{F}} = 6.4\text{k}\Omega$$

In this example D1 is not needed because R1 is small enough to not limit the charging of C2.

If very fast "low" tripping combined with long "high" delays is desired, use the D2, R2, R3, C3 configuration. C3 is chosen first to set "low" delay

$$C3 \approx \frac{t_{LOW}}{2\text{k}\Omega}$$

R3 is then selected for "high" delay

$$R3 \approx \frac{t_{HIGH}}{C3}$$

For t_{LOW} = 100µs and t_{HIGH} = 10ms, C3 = 0.05µF and R3 = 200kΩ.

COMOUT PIN*

The comout pin is intended to be used to drive an external low on-resistance MOSFET which parallels the catch diode. This can improve efficiency considerably for higher input voltages where the diode is "on" for most of the time. Comout is an open collector NPN with 30V maximum operating voltage and a saturation resistance of ≈ 50Ω. It has a typical sink current of 40mA with the saturation voltage guaranteed at 20mA.

EXTLIM PIN*

EXTLIM is intended as a sense pin for current limit when external power transistors are added. It can also be used to raise internal current limit by connecting an external resistor from EXTLIM to the V_{IN} pin. Current limit (minimum) can be increased from 5.5A to 6.5A with a 5.6kΩ resistor. This is allowed only for commercial parts operated at less than 40V input voltage. Capacitance between the EXTLIM pin and V_{SW} pin or ground should be minimized. Do not bypass the EXTLIM pin to V_{IN} with a capacitor; this increases internal current limit to a destructive level.

I_{LIM} PIN

The I_{LIM} pin is used to reduce current limit below the preset value of 6.5A. The equivalent circuit for this pin is shown in Figure 11.

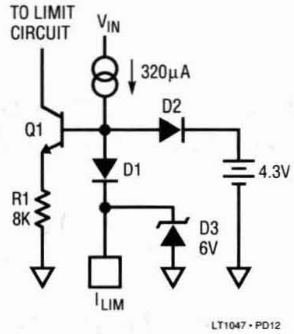

Figure 11. I_{LIM} Pin Circuit

When I_{LIM} is left open, the voltage at Q1 base clamps at 5V through D2. Internal current limit is determined by the current through Q1. If an external resistor is connected

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*Available only on the 11-pin package, which is not recommended for new designs.

PIN DESCRIPTIONS

between I_{LIM} and ground, the voltage at Q1 base can be reduced for lower current limit. The resistor will have a voltage across it equal to (320μA) (R), limited to ≈ 5V when clamped by D2. Resistance required for a given current limit is

$$R_{LIM} = I_{LIM}\,(2k\Omega) + 1k\Omega \text{ (LT1074)}$$

$$R_{LIM} = I_{LIM}\,(5.5k\Omega) + 1k\Omega \text{ (LT1076)}$$

As an example, a 3A current limit would require 3A (2k) + 1k = 7kΩ for the LT1074. The accuracy of these formulas is ±25% for $2A \le I_{LIM} \le 5A$ (LT1074) and $0.7A \le I_{LIM} \le 1.8A$ (LT1076), so I_{LIM} should be set at least 25% above the *peak* switch current required.

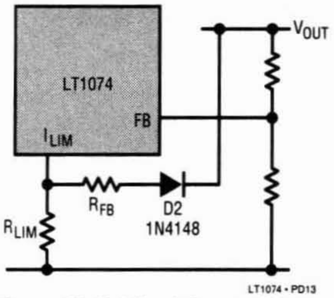


Figure 12. Foldback Current Limit

Foldback current limiting can be easily implemented by adding a resistor from the output to the I_{LIM} pin as shown in Figure 12. This allows full desired current limit (with or without R_{LIM}) when the output is regulating, but reduces current limit under short circuit conditions. A typical value for R_{FB} is 5kΩ, but this may be adjusted up or down to set the amount of foldback. D2 prevents the output voltage from forcing current back into the I_{LIM} pin. To calculate a value for R_{FB}, first calculate R_{LIM}, then R_{FB};

$$R_{FB} = \frac{\left(I_{SC} - 0.44^*\right)\left(R_L\right)}{0.5^*\left(R_L - 1k\Omega\right) - I_{SC}} \left(R_L \text{ in} k\Omega\right)$$

*Change 0.44 to 0.16, and 0.5 to 0.18 for LT1076.

Example: $I_{LIM} = 4A$, $I_{SC} = 1.5A$, $R_{LIM} = (4)(2k) + 1k = 9k$

$$R_{FB} = \frac{(1.5 - 0.44)(9k\Omega)}{0.5(9k - 1k) - 1.5} = 3.8k\Omega$$

ERROR AMPLIFIER

The error amplifier in Figure 13 is a single stage design with added inverters to allow the output to swing above and below the common mode input voltage. One side of the amplifier is tied to a trimmed internal reference voltage of 2.21V. The other input is brought out as the FB (feedback) pin. This amplifier has a G_M (voltage "in" to current "out") transfer function of ≈5000μmho. Voltage gain is determined by multiplying G_M times the total equivalent output loading, consisting of the output resistance of Q4 and Q6 in parallel with the series RC external frequency compensation network. At DC, the external RC is ignored, and with a parallel output impedance for Q4 and Q6 of 400kΩ, voltage gain is ≈ 2000. At frequencies above a few hertz, voltage gain is determined by the external compensation, R_C and C_C.

$$A_V = \frac{G_m}{2\pi \bullet f \bullet C_C} \text{ at midfrequencies}$$

$$A_V = G_m \bullet R_C \text{ at highfrequencies}$$

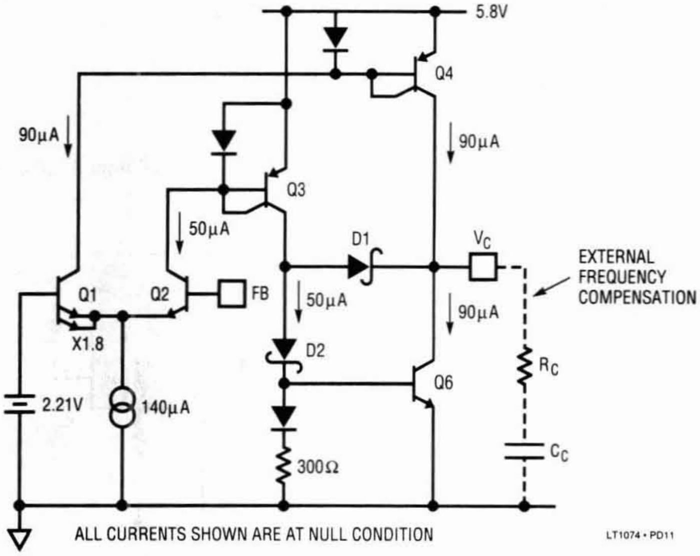


Figure 13. Error Amplifier

PIN DESCRIPTIONS

Phase shift from the FB pin to the V_C pin is 90° at mid-frequencies where the external C_C is controlling gain, then drops back to 0° (actually 180° since FB is an inverting input) when the reactance of C_C is small compared to R_C. The low frequency "pole" where the reactance of C_C is equal to the output impedance of Q4 and Q6 (r_O), is

$$f_{POLE} = \frac{1}{2\pi \bullet r_O \bullet C} \quad r_O \approx 400k\Omega$$

Although f_{POLE} varies as much as 3:1 due to r_O variations, mid-frequency gain is dependent only on G_M, which is specified much tighter on the data sheet. The higher frequency "zero" is determined solely by R_C and C_C.

$$f_{ZERO} = \frac{1}{2\pi \bullet R_C \bullet C_C}$$

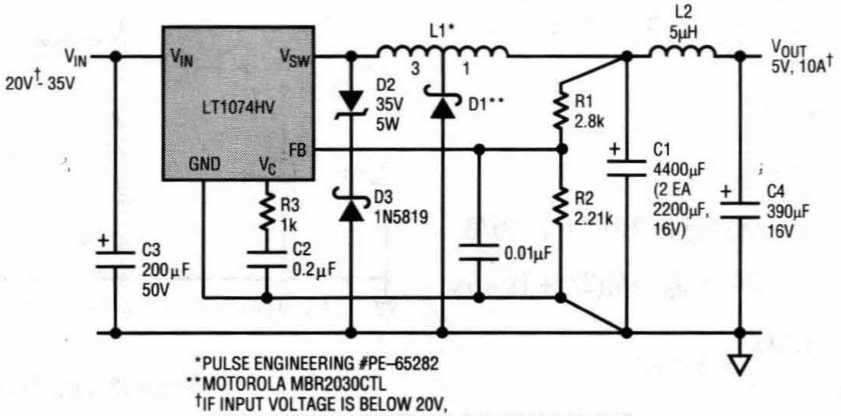
The error amplifier has *asymmetrical* peak output current. Q3 and Q4 current mirrors are unity gain, but the Q6 mirror has a gain of 1.8 at output null and a gain of 8 when the FB pin is high (Q1 current = 0). This results in a maximum positive output current of 140µA and a maximum negative (sink) output current of ≅ 1.1mA. The asymmetry is deliberate — it results in much less regulator output overshoot during rapid startup or following the release of an output overload. Amplifier offset is kept low by area scaling Q1 and Q2 at 1.8:1.

Amplifier swing is limited by the internal 5.8V supply for positive outputs and by D1 and D2 when the output goes low. Low clamp voltage is approximately one diode drop (≈ 0.7V – 2mV/°C).

Note that both the FB pin and the V_C pin have other internal connections. Refer to the frequency shifting and synchronizing discussions.

TYPICAL APPLICATIONS

Tapped Inductor Buck Converter

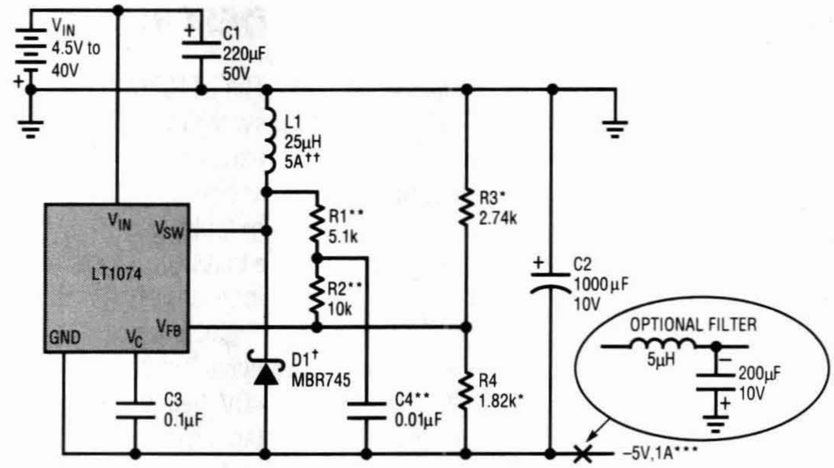


*PULSE ENGINEERING #PE–65282
**MOTOROLA MBR2030CTL
†IF INPUT VOLTAGE IS BELOW 20V,
MAXIMUM OUTPUT CURRENT WILL BE REDUCED. SEE AN44

LT1074 • TA02

TYPICAL APPLICATIONS

Positive to Negative Converter



V_IN
4.5V to
40V
C1
220µF
50V
L1
25µH
5A††
LT1074
V_IN
V_SW
V_FB
GND
V_C
R1**
5.1k
R2**
10k
R3*
2.74k
C2
1000µF
10V
D1†
MBR745
C3
0.1µF
C4**
0.01µF
R4
1.82k*
OPTIONAL FILTER
5µH
200µF
10V
–5V,1A***

* = 1% FILM RESISTORS
D1 = MOTOROLA-MBR745
C1 = NICHICON-UPL1C221MRH6
C2 = NICHICON-UPL1A102MRH6
L1 = COILTRONICS-CTX25-5-52

† LOWER REVERSE VOLTAGE RATING MAY BE USED FOR LOWER INPUT VOLTAGES. LOWER CURRENT RATING IS ALLOWED FOR LOWER OUTPUT CURRENT. SEE AN44.

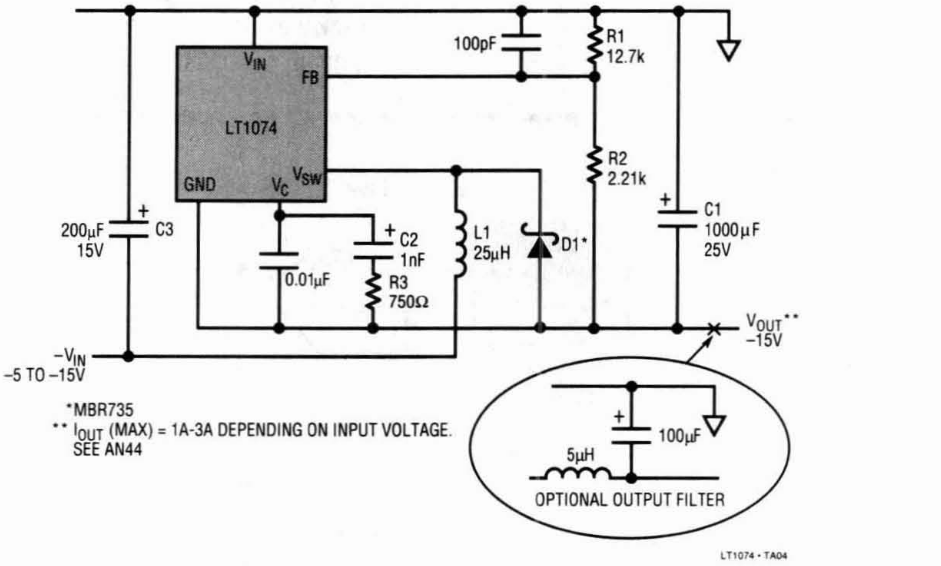
†† LOWER CURRENT RATING MAY BE USED FOR LOWER OUTPUT CURRENT. SEE AN44.

** R1, R2, AND C4 ARE USED FOR LOOP FREQUENCY COMPENSATION, BUT R1 AND R2 MUST BE INCLUDED IN THE CALCULATION FOR OUTPUT VOLTAGE DIVIDER VALUES. FOR HIGHER OUTPUT VOLTAGES, INCREASE R1, R2 AND R3 PROPORTIONATELY;
$R3 = V_{OUT} - 2.37$ (KΩ)
R1 = (R3) (1.86)
R2 = (R3) (3.65)

*** MAXIMUM OUTPUT CURRENT OF 1A IS DETERMINED BY MINIMUM INPUT VOLTAGE OF 4.5V. HIGHER MINIMUM INPUT VOLTAGE WILL ALLOW MUCH HIGHER OUTPUT CURRENTS. SEE AN44.

LT1074 • TA03

Negative Boost Converter



LT1074
V_IN
FB
GND
V_C
V_SW
100pF
R1
12.7k
R2
2.21k
C1
1000µF
25V
200µF
15V
C3
0.01µF
C2
1nF
R3
750Ω
L1
25µH
D1*
–V_IN
–5 TO –15V
V_OUT**
–15V
100µF
5µH
OPTIONAL OUTPUT FILTER

*MBR735
** I_{OUT} (MAX) = 1A-3A DEPENDING ON INPUT VOLTAGE. SEE AN44

LT1074 • TA04

LT1076-5

5V Step-Down Switching Regulator

FEATURES

- Fixed 5V Output
- 2A On-Board Switch
- 100kHz Switching Frequency
- 2% Output Voltage Tolerance Over Temperature
- Greatly Improved Dynamic Behavior
- Available in Low Cost 5-Lead Package
- Only 9.5mA Quiescent Current
- Operates Up to 60V Input

APPLICATIONS

- 5V Output Buck Converter
- Tapped Inductor Buck Converter with 4A Output at 5V
- Positive-to-Negative Converter

DESCRIPTION

The LT1076-5 is a 2A fixed 5V output monolithic bipolar switching regulator which requires only a few external parts for normal operation. The power switch, all oscillator and control circuitry, all current limit components, and an output monitor are included on the chip. The topology is a classic positive "buck" configuration but several design innovations allow this device to be used as a positive-to-negative converter, a negative boost converter, and as a flyback converter. The switch output is specified to swing 40V below ground, allowing the LT1076-5 to drive a tapped inductor in the buck mode with output currents up to 4A.

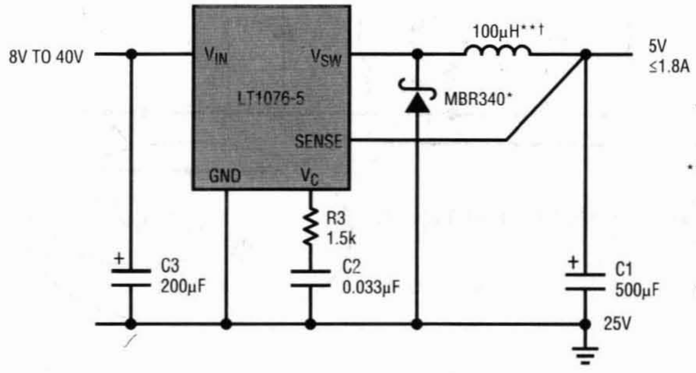
The LT1076-5 uses a true analog multiplier in the feedback loop. This makes the device respond nearly instantaneously to input voltage fluctuations and makes loop gain independent of input voltage. As a result, dynamic behavior of the regulator is significantly improved over previous designs.

On-chip pulse by pulse current limiting makes the LT1076-5 nearly bust-proof for output overloads or shorts. The input voltage range as a buck converter is 8V to 60V, but a self-boot feature allows input voltages as low as 5V in the inverting and boost configurations.

The LT1076-5 is available in a low cost 5-lead TO-220 package with frequency pre-set at 100kHz and current limit at 2.6A. See Application Note 44 for design details.

TYPICAL APPLICATION

Basic Positive Buck Converter



* MBR330P MAY BE USED FOR $V_{IN} \leq 25V$

** COILTRONICS #100-1-52

PULSE ENGINEERING, INC. #PE-92102

HURRICANE #HL-AG210LL

† VALUE MAY BE REDUCED TO 50μH FOR OUTPUT LOADS BELOW 1.5A

LT1076-5 TA01

ABSOLUTE MAXIMUM RATINGS

Input Voltage
- LT1076-5 .... 45V
- LT1076HV-5 .... 64V

Switch Voltage with Respect to Input Voltage
- LT1076-5 .... 64V
- LT1076HV-5 .... 75V

Switch Voltage with Respect to Ground Pin (V_{SW} **Negative**)
- LT1076-5 (Note 5) 35V
- LT1076HV-5 (Note 5) 45V

Sense Pin Voltage .... –2V, +10V

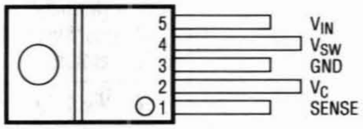
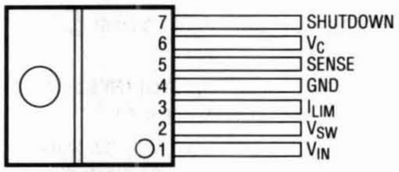
Maximum Operating Ambient Temperature Range
- LT1076C-5, LT1076HVC-5 .... 0°C to 70°C

Maximum Operating Junction Temperature Range
- LT1076C-5, LT1076HVC-5 .... 0°C to 125°C

Maximum Storage Temperature .... –65°C to 150°C

Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
FRONT VIEW  5 4 3 2 1 V_{IN} V_{SW} GND V_C SENSE T PACKAGE 5-LEAD TO-220 FOR STRAIGHT LEADS, ORDER FLOW 06	LT1076CT-5 LT1076HVCT-5
FRONT VIEW  7 6 5 4 3 2 1 SHUTDOWN V_C SENSE GND I_{LIM} V_{SW} V_{IN} Y PACKAGE 7-LEAD TO-220	LT1076CY-5 LT1076HVCY-5

ELECTRICAL CHARACTERISTICS $T_J = 25°C$, $V_{IN} = 25V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch "On" Voltage (Note 1)	$I_{SW} = 0.5A$	●			1.2	V
	$I_{SW} = 2A$	●			1.7	V
Switch "Off" Leakage	$V_{IN} = 25V$, $V_{SW} = 0$				150	µA
	$V_{IN} = V_{MAX}$, $V_{SW} = 0$ (Note 6)				250	µA
Supply Current (Note 2)	$V_{OUT} = 5.5V$, $V_{IN} \leq 40V$	●		8.5	11	mA
	$40V < V_{IN} < 60V$	●		9.0	12	mA
Minimum Supply Voltage	Normal Mode	●		7.3	8.0	V
	Startup Mode (Note 3)	●		3.5	4.8	V
Switch Current Limit (Note 4)		●	2	2.6	3.2	A
Maximum Duty Cycle		●	85	90		%
Switching Frequency			90	100	110	kHz
	$T_J \leq 125°C$	●	85		120	kHz
	$V_{OUT} = V_{SENSE} = 0V$ (Note 4)			20		kHz
Switching Frequency Line Regulation	$8V \leq V_{IN} \leq V_{MAX}$ (Note 7)	●		0.03	0.1	%/V
Error Amplifier Voltage Gain (Note 7)	$1V \leq V_C \leq 4V$			2000		V/V
Error Amplifier Transconductance (Note 7)			3700	5000	8000	µmho
Error Amplifier Source and Sink Current	Source ($V_{SENSE} = 4.5V$)		100	140	225	µA
	Sink ($V_{SENSE} = 5.5V$)		0.7	1.0	1.6	mA
Sense Pin Divider Resistance			3	5	8	kΩ
Sense Voltage	$V_C = 2V$	●	4.85	5	5.15	V

ELECTRICAL CHARACTERISTICS $T_J = 25°C$, $V_{IN} = 25V$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Tolerance	V_{OUT} (Nominal) = 5V			±0.5	±2	%
	All Conditions of Input Voltage, Output Voltage, Temperature and Load Current	●		±1.0	±3	%
Output Voltage Line Regulation	$8V \le V_{IN} \le V_{MAX}$ (Note 6)	●		0.005	0.02	%/V
V_C Voltage at 0% Duty Cycle				1.5		V
	Over Temperature	●		−4.0		mV/°C
Multiplier Reference Voltage				24		V
Thermal Resistance Junction to Case					4	°C/W

The ● denotes specifications which apply over the full operating temperature range.

Note 1: To calculate maximum switch "on" voltage at currents between low and high conditions, a linear interpolation may be used.

Note 2: A sense pin voltage (V_{SENSE}) of 5.5V forces the V_C pin to its low clamp level and the switch duty cycle to zero. This approximates the zero load condition where duty cycle approaches zero.

Note 3: Total voltage from V_{IN} pin to ground pin must be ≥ 8V after startup for proper regulation.

Note 4: Switch frequency is internally scaled down when the sense pin voltage is less than 2.6V to avoid extremely short switch on times. During current limit testing, V_{SENSE} is adjusted to give a minimum switch on time of 1µs.

Note 5: Switch to input voltage limitation must also be observed.

Note 6: V_{MAX} = 40V for the LT1076-5 and 60V for the LT1076HV-5.

Note 7: Error amplifier voltage gain and transconductance are specified relative to the internal feedback node. To calculate gain and transconductance from the sense pin (Output) to the V_C pin, multiply by 0.44.

LT1103/LT1105

Offline Switching Regulator

FEATURES

- ±1% Line and Load Regulation with No Opto-Coupler
- Switch Frequency up to 200kHz
- Internal 2A Switch and Current Sense (LT1103)
- Internal 1A Totem Pole Driver (LT1105)
- Start-Up Mode Draws Only 200µA
- Fully Protected Against Overloads
- Overvoltage Lockout of Main Supply
- Protected Against Underdrive or Overdrive to FET
- Operates in Continuous or Discontinuous Mode
- Ideal for Flyback and Forward Topologies
- Isolated Flyback Mode Has Fully Floating Outputs

APPLICATIONS

- Up to 250W Isolated Mains Converter
- Up to 50W Isolated Telecom Converter
- Fully Isolated Multiple Outputs
- Distributed Power Conversion Networks

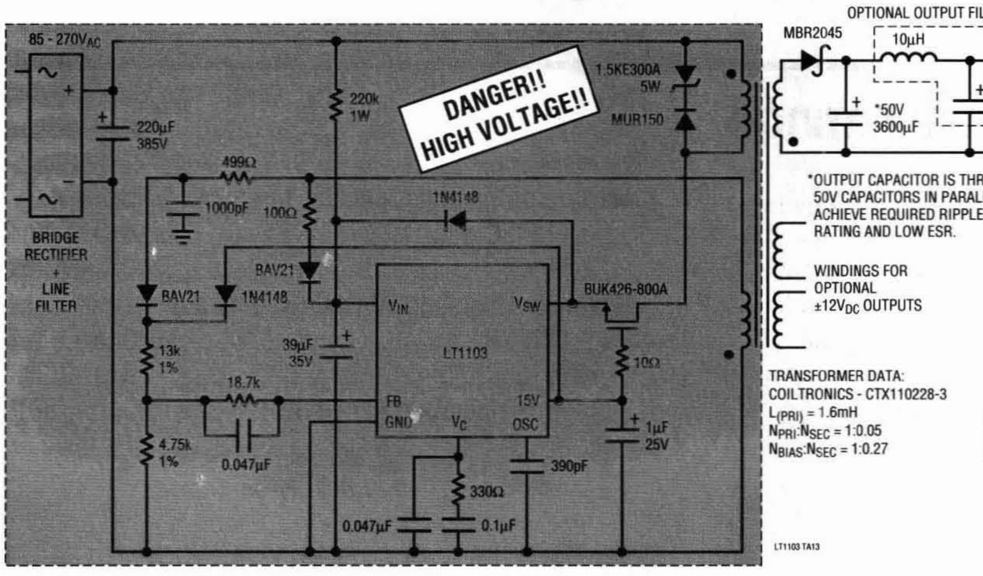
DESCRIPTION

The LT1103 Offline Switching Regulator is designed for high input voltage applications using an external FET switch whose source is driven by the open collector output of the LT1103. The LT1103 is optimized for 15W–100W applications. For higher power applications or additional switch current flexibility, the LT1105 is available and its totem pole output drives the gate of an external FET. Unique design of the LT1103/LT1105 eliminates the need for an opto-coupler while still providing ±1% load and line regulation in a magnetic flux-sensed converter. This significantly simplifies the design of offline power supplies and reduces the number of components which must cross the isolation barrier to one, the transformer.

The LT1103/LT1105 current mode switching techniques are well suited to transformer-isolated flyback and forward topologies while providing ease of frequency compensation with a minimum of external components. Low external part count for a typical application combines with

TYPICAL APPLICATION

Fully-Isolated Flyback 100kHz 50W Converter with Load Regulation Compensation


85 - 270V$_{AC}$
BRIDGE RECTIFIER + LINE FILTER
220µF 385V
220k 1W
DANGER!! HIGH VOLTAGE!!
1.5KE300A 5W
MUR150
499Ω
1000pF
100Ω
1N4148
BAV21
BAV21
1N4148
V$_{IN}$
V$_{SW}$
LT1103
BUK426-800A
39µF 35V
10Ω
13k 1%
18.7k
FB
GND
V$_C$
15V
OSC
1µF 25V
4.75k 1%
0.047µF
390pF
330Ω
0.047µF
0.1µF
MBR2045
OPTIONAL OUTPUT FILTER
10µH
5V 10A
*50V 3600µF
50V 470µF
LT1103 TA13

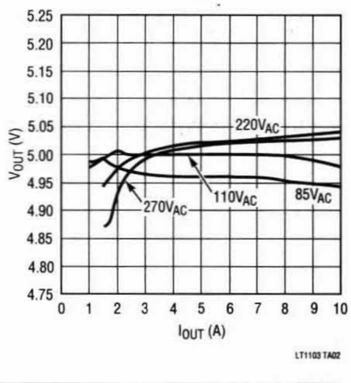
*OUTPUT CAPACITOR IS THREE 1200µF, 50V CAPACITORS IN PARALLEL TO ACHIEVE REQUIRED RIPPLE CURRENT RATING AND LOW ESR.

WINDINGS FOR OPTIONAL ±12V$_{DC}$ OUTPUTS

TRANSFORMER DATA:
COILTRONICS - CTX110228-3
$L_{(PRI)}$ = 1.6mH
$N_{PRI}:N_{SEC}$ = 1:0.05
$N_{BIAS}:N_{SEC}$ = 1:0.27

Danger!! Lethal Voltages Present – See Text

Load Regulation



DESCRIPTION

a 200kHz maximum switching frequency to achieve high power density. Performance at switching frequencies above 100kHz may be degraded due to internal timing constraints associated with fully-isolated flyback mode.

Included are the oscillator, control, and protection circuitry such as current limit and overvoltage lockout. Switch frequency and maximum duty cycle are adjustable. Bootstrap circuitry draws 200μA for startup of isolated topologies. A 5V reference as well as a 15V gate bias are available to power external primary-side circuitry. No external current sense resistor is necessary with LT1103 because it is integrated with the high current switch. The LT1105 brings out the input to the current limit amplifier and requires the use of an external sense resistor.

The LT1103/LT1105 have unique features not found on other offline switching regulators. Adaptive anti-sat switch drive allows wide-ranging load currents while maintaining high efficiency. The external FET is protected from insufficient or excessive gate drive voltage with a drive detection circuit. An externally activated shutdown mode reduces total supply current to less than 200μA, typical for standby operation. Fully isolated and regulated outputs can be generated in the optional isolated flyback mode without the need for opto-couplers or other isolated feedback paths.

WARNING!

DANGEROUS AND LETHAL POTENTIALS ARE PRESENT IN OFFLINE CIRCUITS!

BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF OFFLINE CIRCUITS. HIGH VOLTAGE, AC LINE-CONNECTED POTENTIALS ARE PRESENT IN THESE CIRCUITS. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THESE CIRCUITS. REPEAT: OFFLINE CIRCUITS CONTAIN DANGEROUS, AC LINE-CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.

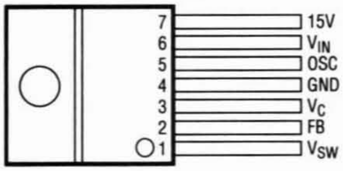
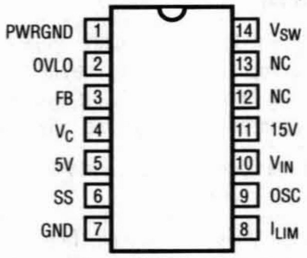
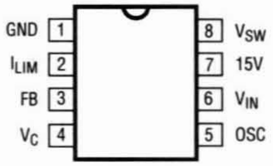
ALL TESTING PERFORMED ON AN OFFLINE CIRCUIT MUST BE DONE WITH AN ISOLATION TRANSFORMER CONNECTED BETWEEN THE OFFLINE CIRCUIT'S INPUT AND THE AC LINE. USERS AND CONSTRUCTORS OF OFFLINE CIRCUITS MUST OBSERVE THIS PRECAUTION WHEN CONNECTING TEST EQUIPMENT TO THE CIRCUIT TO AVOID ELECTRIC SHOCK. REPEAT: AN ISOLATION TRANSFORMER MUST BE CONNECTED BETWEEN THE CIRCUIT INPUT AND THE AC LINE IF ANY TEST EQUIPMENT IS TO BE CONNECTED.

ABSOLUTE MAXIMUM RATINGS

V_{IN}	30V
V_{SW} Output Voltage (LT1103)	50V
V_{SW} Output Current (200ns)(LT1105)	±1.5A
V_C, FB, OSC, SS	6V
I_{LIM} (LT1105)	3V
OVLO Input Current	1mA
Lead Temperature (Soldering, 10 sec.)	300°C

Maximum Operating Ambient Temperature Range	
LT1103C	0°C to 70°C
LT1105C	0°C to 70°C
Maximum Operating Junction Temperature Range	
LT1103C	0°C to +100°C
LT1105C	0°C to +100°C
Storage Temperature Range	−65°C to +150°C

PACKAGE/ORDER INFORMATION

FRONT VIEW  7 15V 6 V_{IN} 5 OSC 4 GND 3 V_C 2 FB 1 V_{SW} Y PACKAGE 7-LEAD TO-220 CASE IS CONNECTED TO GROUND. LEADS ARE FORMED.	TOP VIEW  PWRGND 1 OVLO 2 FB 3 V_C 4 5V 5 SS 6 GND 7 14 V_{SW} 13 NC 12 NC 11 15V 10 V_{IN} 9 OSC 8 I_{LIM} N PACKAGE 14-LEAD PLASTIC DIP PINS 1 AND 7 MUST BE TIED TOGETHER.	TOP VIEW  GND 1 I_{LIM} 2 FB 3 V_C 4 8 V_{SW} 7 15V 6 V_{IN} 5 OSC N8 PACKAGE 8-LEAD PLASTIC DIP
ORDER PART NUMBER	ORDER PART NUMBER	ORDER PART NUMBER
LT1103CY	LT1105CN	LT1105CN8

ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	8V < V_{IN} < 30V, After device has started	●	10	18	25	mA
I_{START}	Start-Up Current	V_{IN} < V_{IN} Start Threshold	●		200	400	µA
	V_{IN} Start Threshold		●	14.5	16.0	17.5	V
	V_{IN} Shutdown Threshold	Note: Switching stops when V_{SW} < 10V (LT1103) Note: Switching stops when V_{GATE} < 10V (LT1105)	●	6.5	7.0	8.0	V
V_{REF}	5V Reference Voltage		●	4.80	4.95	5.20	V
	V_{REF} Line Regulation	10V < V_{IN} < 30V	●		0.025	0.075	%/V
	V_{REF} Load Regulation	0mA < I_L < 20mA	●		0.025	0.05	%/mA
	V_{REF} Short Circuit Current		●	25	60	110	mA
V_{GATE}	15V Gate Bias Reference	17 < V_{IN} < 30V, 0mA < I_L < 30mA	●	13.8	15.0	16.2	V
	15V Dropout Voltage	V_{IN} = 15V, I_L = 30mA	●		2.0	2.5	V
	15V Short Circuit Current		●	30	70	130	mA
SF	Oscillator Scaling Factor	FB = 4V, V_C = Open, Measured at V_{SW}, I_{SW} = 25mA, OVLO = 5V, F_{OSC} = SF/C_{OSC}, 40kHz < F_{OSC} < 200kHz	●	36 32	40 40	44 48	Hz • µF Hz • µF
	Oscillator Valley Voltage				2.0		V
	Oscillator Peak Voltage				4.5		V

ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITONS		MIN	TYP	MAX	UNIT
DC	Preset Max. Switch Duty Cycle (LT1103)	FB = 4V, V_C = Open, F_{OSC} = 40kHz, I_{SW} = 25mA, Note: Maximum Duty Cycle can be altered at OSC pin	●	58	65	72	%
	Preset Max. Switch Duty Cycle (LT1105)	FB = 4V, V_C = Open, F_{OSC} = 40kHz, I_{SW} = 25mA, Note: Maximum Duty Cycle can be altered at OSC pin	●	56	63	70	%
	OVLO Threshold	Overvoltage Lockout Threshold at which switching is inhibited	●	2.3	2.5	2.7	V
	OVLO Input Bias Current	OVLO = 2V, Measured out of pin (Note 1)	●		1.0	3.0	µA
V_{FB}	FB Threshold Voltage	$I(V_C)$ = 0mA		4.425	4.50	4.575	V
			●	4.400	4.50	4.600	V
	FB Input Bias Current	FB = 4V (Note 2)	●	5	10	20	µA
	Change in FB Input Bias Current with Change in V_C	FB = 4V, V_C = 1V to 4V (Note 2)		9	11	13	µA/V
			●	8	11	14	µA/V
	FB Threshold Line Regulation	10V < V_{IN} < 30V	●		0.025	0.05	%/V
gm	Error Amp Transconductance	$\Delta I(V_C) = \pm 50\mu A$		9k	12k	15k	µmho
			●	6k	12k	18k	µmho
A_V	Error Amp Voltage Gain	1V < V_C < 3V	●	500	1250		V/V
	V_C Switching Threshold	Switch Duty Cycle = 0%	●	0.85	1.25	1.4	V
	Shutdown Threshold Voltage		●	75	150	250	mV
	Error Amp Source Current		●	150	275	350	µA
	Error Amp Sink Current		●	1.5	3	4.5	mA
	Error Amp Clamp Voltage	FB = 4.75V	●	0.3	0.7	0.9	V
		FB = 4.0V	●	4.2	4.4	4.6	V
	Soft-Start Charging Current	SS = 0V	●	25	40	60	µA
	Soft-Start Reset Current	V_{IN} = 6V, SS = 0.3V	●	1	2		mA
	Output Switch Leakage (LT1103)	V_{SW} = 45V	●			500	µA
		V_{SW} = 15V	●			200	µA
BV	Switch Breakdown Voltage (LT1103)	I_{SW} = 5mA	●	50	70		V
	V_{SW} Current Limit (LT1103)	Duty Cycle = 25% (Note 3)	●	2.0	2.5	3.0	A
	Output Switch ON Resistance (LT1103)		●		0.4	0.75	Ω
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	I_Q Increase During Switch ON Time (LT1103)	I_{SW} = 0.5A to 1.5A	●		30	50	mA/A
	Switch Output High Level (LT1105)	I_{SW} =200mA, V_{GATE} = 15V	●	13.0	13.5		V
		I_{SW} = 750mA, V_{GATE} = 15V	●	12.5	13.2		V
	Switch Output Low Level (LT1105)	I_{SW} = 200mA	●		0.25	0.50	V
		I_{SW} = 750mA	●		0.75	1.50	V
	Rise Time (LT1105)	CL = 1000pF			50		ns
	Fall Time (LT1105)	CL = 1000pF			20		ns

ELECTRICAL CHARACTERISTICS

V_{IN} = 20V, V_C = 0.85V, OVLO = 0V, V_{SW} Open, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITONS		MIN	TYP	MAX	UNIT
	I_{LIM} Threshold Voltage (LT1105)	Duty Cycle = 25% (Note 4)	●	300	375	450	mV
	Low Switch Drive Lockout Threshold	Measured at V_{SW} (LT1103) Measured at 15V Gate Bias Reference (LT1105)	●	9.0	9.5	10.5	V
	High Switch Drive Lockout Threshold	Measured at V_{SW} (LT1103) Measured at 15V Gate Bias Reference (LT1105)	●	17.0	18.5	20.0	V

The ● denotes specifications which apply over the full operating temperature range.

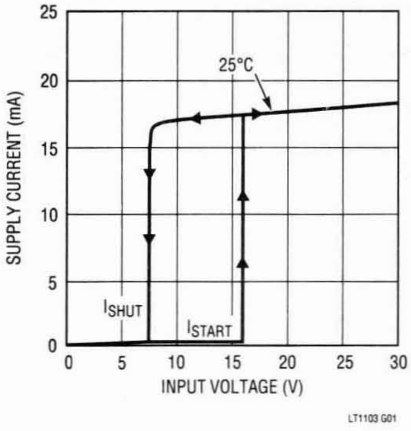
Note 1: The OVLO pin is clamped with a 5.5V Zener and can sink a maximum input current of 1mA.

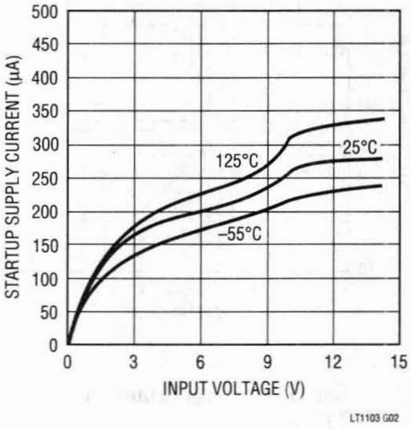
Note 2: FB input bias current changes as a function of the V_C pin voltage. Rate of change of FB input bias current is 11μA/V of change on V_C. By including a resistor in series with the FB pin, load regulation can be set to zero.

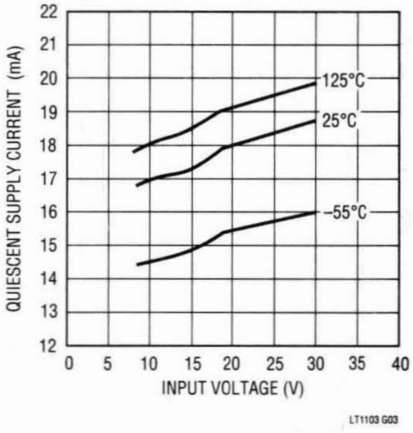
Note 3: Current limit on V_{SW} is constant for DC < 35% and decreases for DC > 35% due to internal slope compensation circuity. The LT1103 switch current limit is given by I_{LIM} = 1.76 (1.536 – DC) above 35% duty cycle.

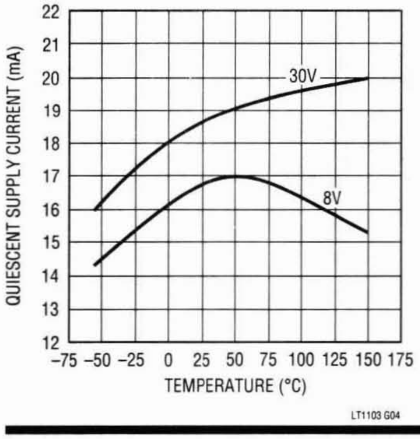
Note 4: The current limit threshold voltage is constant for DC < 35% and decreases for DC > 35% due to internal slope compensation circuitry. The LT1105 switch current limit threshold voltage is given by V_{LIM} = 0.264 (1.536 – DC) above 35% duty cycle.

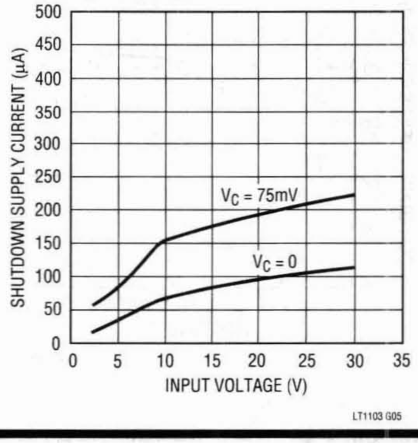
TYPICAL PERFORMANCE CHARACTERISTICS

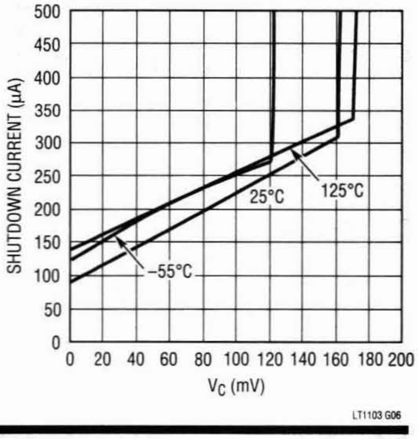

Supply Current vs Input Voltage


Startup Supply Current vs Input Voltage

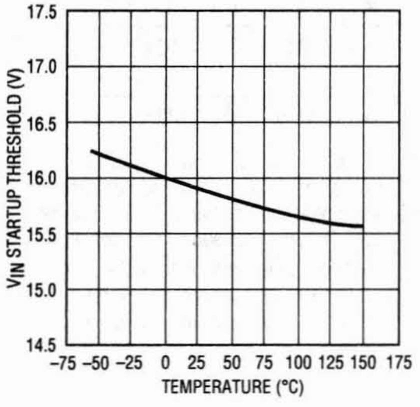

Quiescent Supply Current vs Input Voltage


Quiescent Supply Current vs Temperature

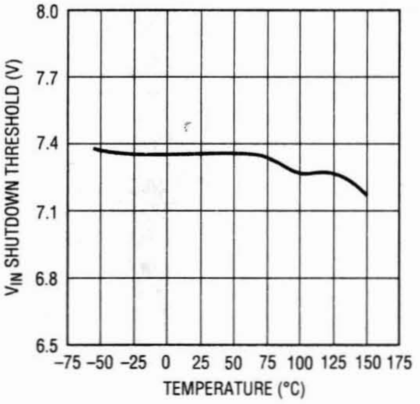

Shutdown Supply Current vs Input Voltage


Shutdown Supply Current vs V_C Voltage

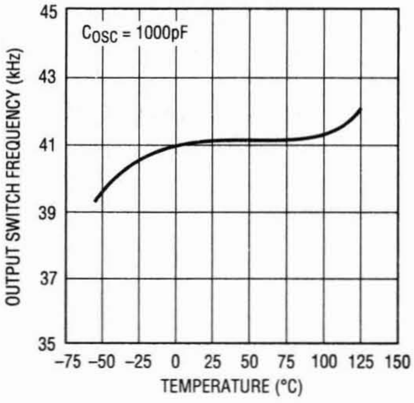
TYPICAL PERFORMANCE CHARACTERISTICS


V_{IN} Start-Up Threshold vs Temperature

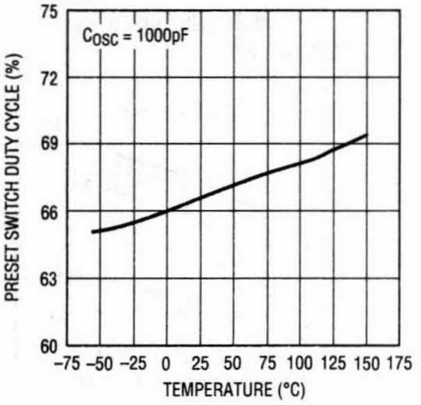
LT1103 G07


V_{IN} Shutdown Threshold vs Temperature

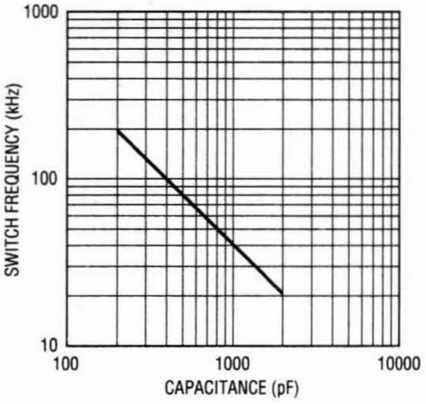
LT1103 G08


Output Switch Frequency vs Temperature

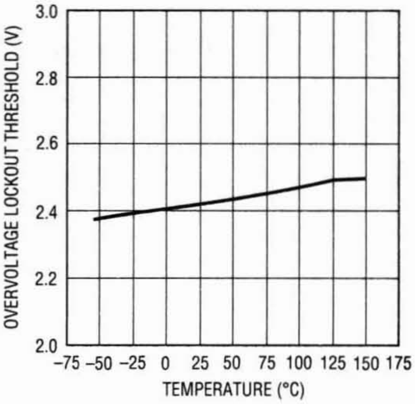
LT1103 G09


Preset Switch Maximum Duty Cycle vs Temperature

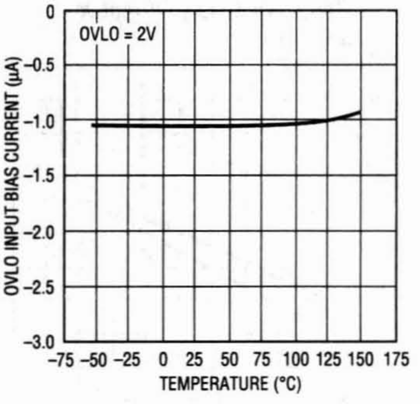
LT1103 G10


Switch Oscillator Frequency vs Capacitance

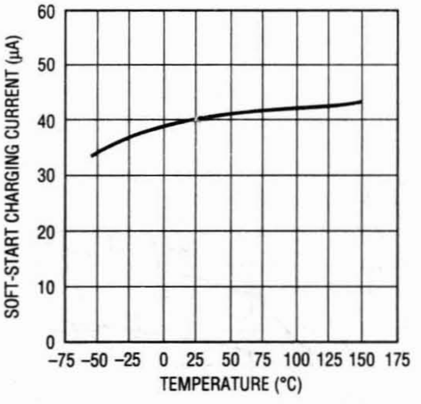
LT1103 G11


Overvoltage Lockout Threshold vs Temperature

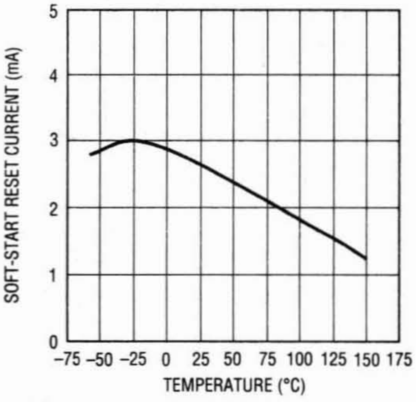
LT1103 G12


OVLO Input Bias Current vs Temperature

LT1103 G13


Soft-Start Charging Current vs Temperature

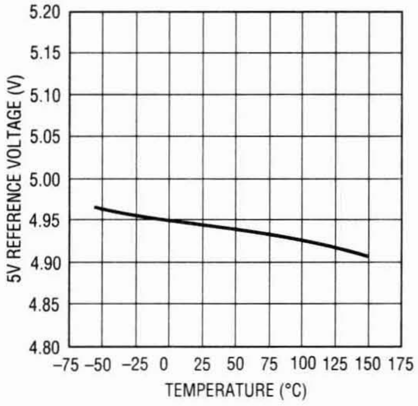
LT1103 G14


Soft-Start Reset Current vs Temperature

LT1103 G15

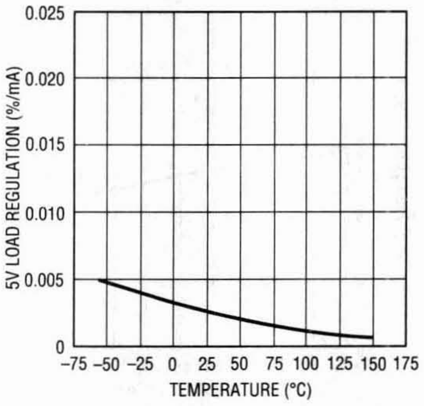
TYPICAL PERFORMANCE CHARACTERISTICS

5V Reference Voltage vs Temperature



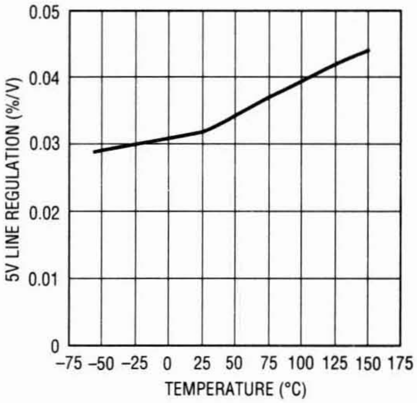
LT1103 G16

5V Load Regulation vs Temperature



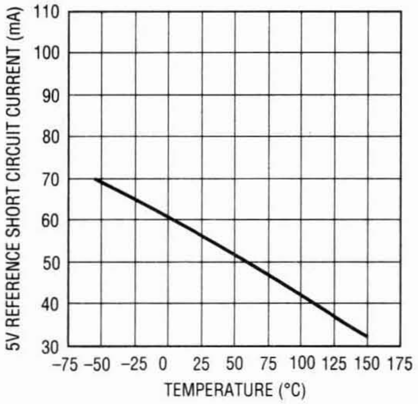
LT1103 G17

5V Line Regulation vs Temperature



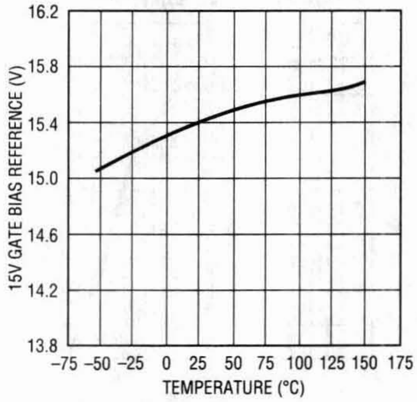
LT1103 G18

5V Reference Short Circuit Current vs Temperature



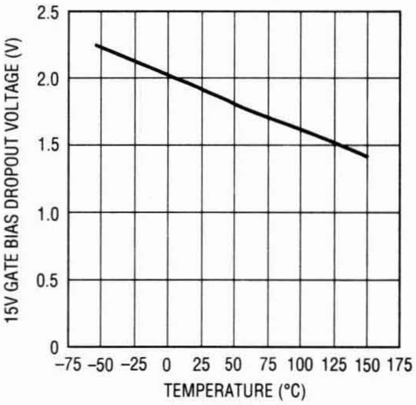
LT1103 G19

15V Gate Bias Reference vs Temperature



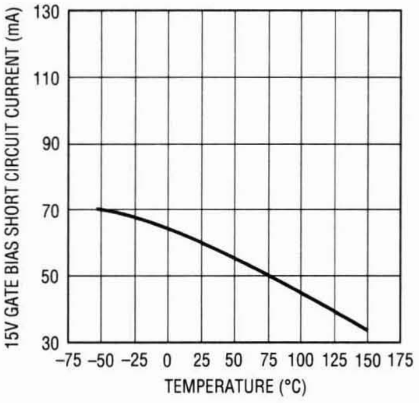
LT1103 G20

15V Gate Bias Dropout Voltage vs Temperature



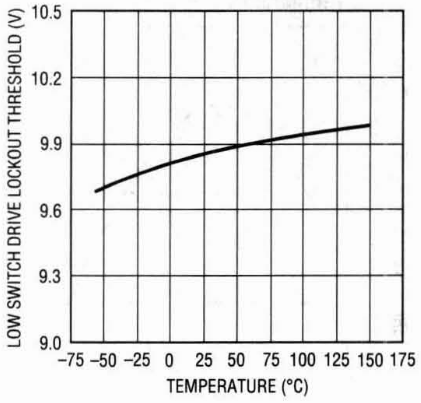
LT1103 G21

15V Gate Bias Short Circuit Current vs Temperature



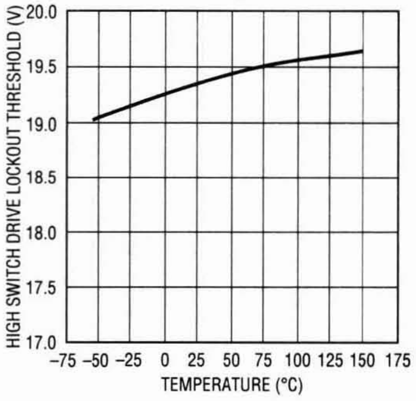
LT1103 G22

Low Switch Drive Lockout Threshold vs Temperature



LT1103 G23

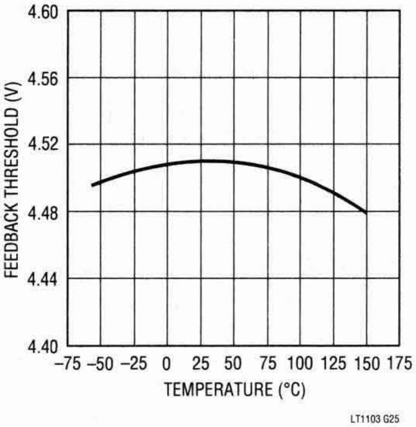
High Switch Drive Lockout Threshold vs Temperature



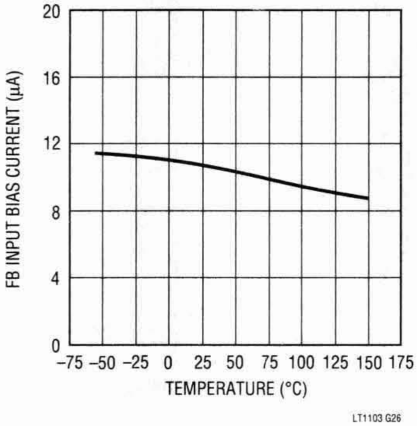
LT1103 G24

TYPICAL PERFORMANCE CHARACTERISTICS

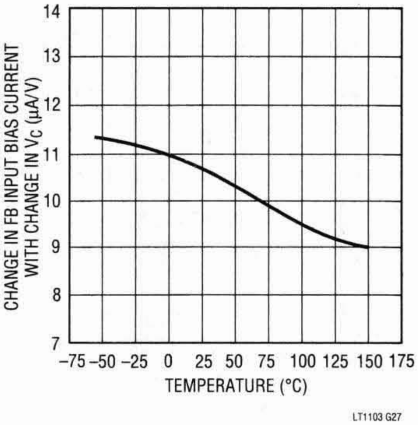
Feedback Threshold vs Temperature



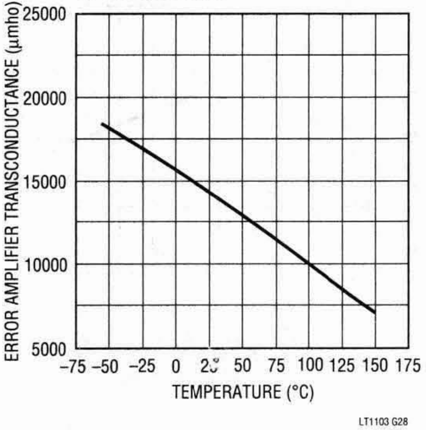
FB Input Bias Current vs Temperature (V_C = 1V)



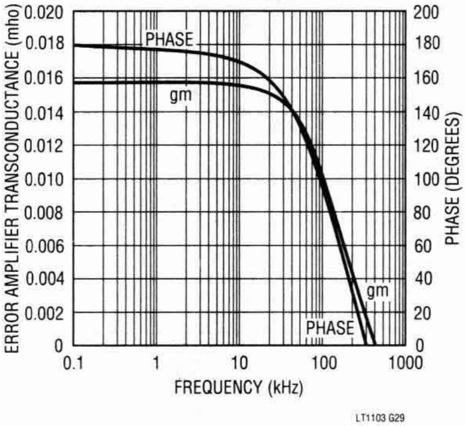
Change in FB Input Bias Current with Change in V_C vs Temperature (V_C = 1V to 4V)



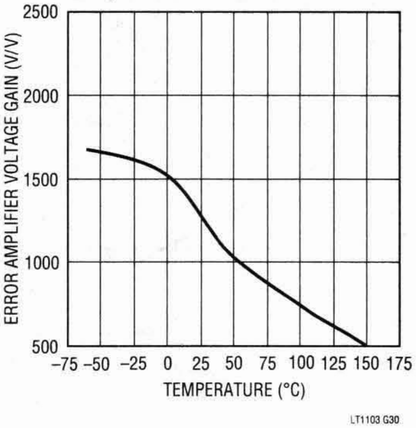
Error Amplifier Transconductance vs Temperature



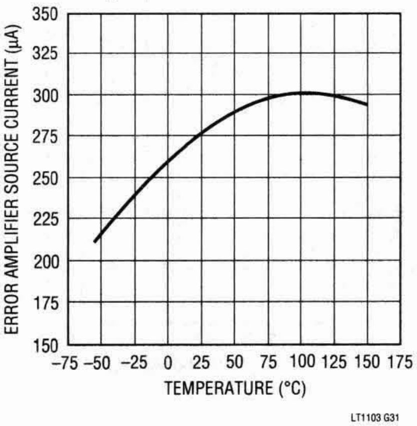
Error Amplifier Transconductance and Phase vs Frequency



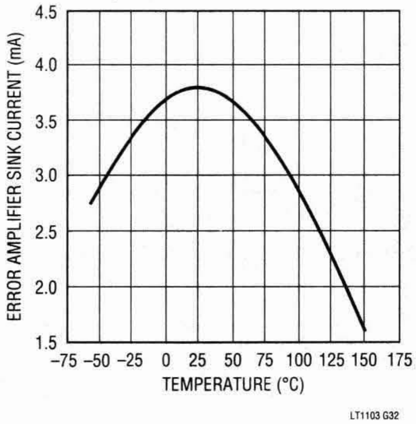
Error Amplifier Voltage Gain vs Temperature



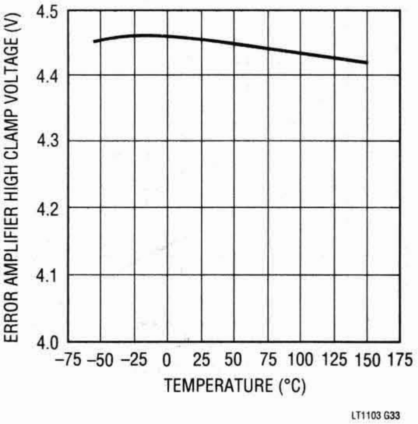
Error Amplifier Source Current vs Temperature



Error Amplifier Sink Current vs Temperature

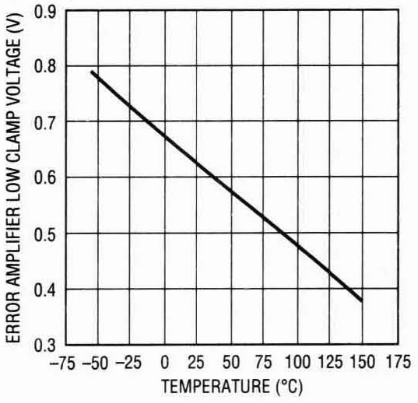


Error Amplifier High Clamp Voltage vs Temperature (FB = 4V)



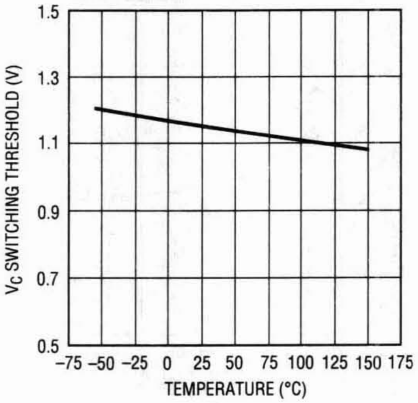
TYPICAL PERFORMANCE CHARACTERISTICS

Error Amplifier Low Clamp Voltage vs Temperature (FB = 4.75V)



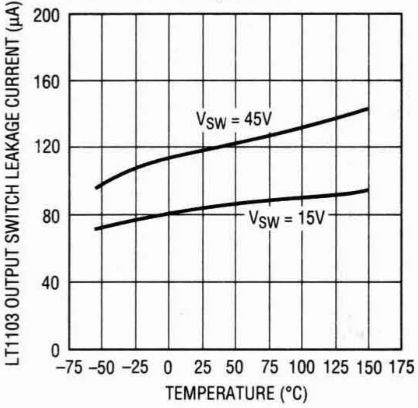
LT1103 G34

V_C Switching Threshold Voltage vs Temperature



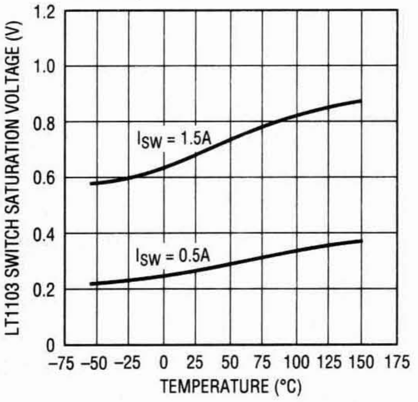
LT1103 G35

LT1103 Output Switch Leakage Current vs Temperature



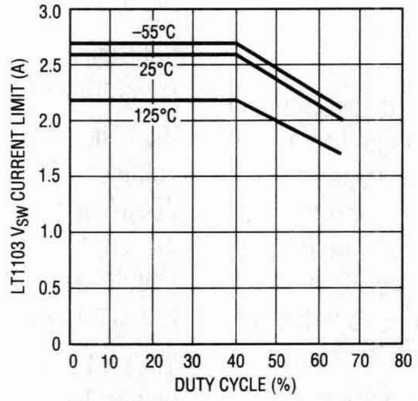
LT1103 G36

LT1103 Switch Saturation Voltage vs Temperature



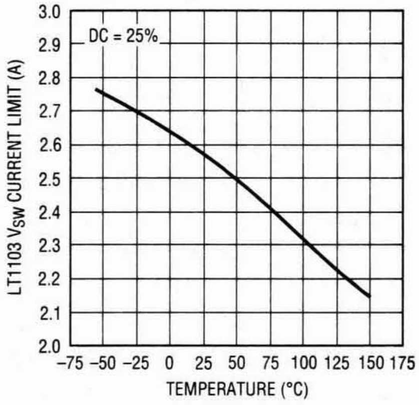
LT1103 G38

LT1103 V_{SW} Current Limit vs Duty Cycle



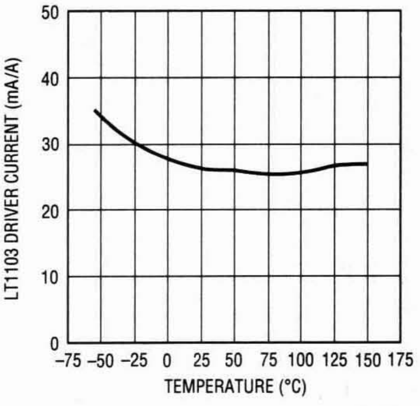
LT1103 G39

LT1103 V_{SW} Current Limit vs Temperature



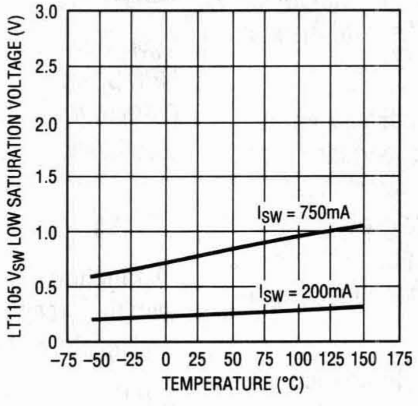
LT1103 G40

LT1103 Driver Current vs Temperature



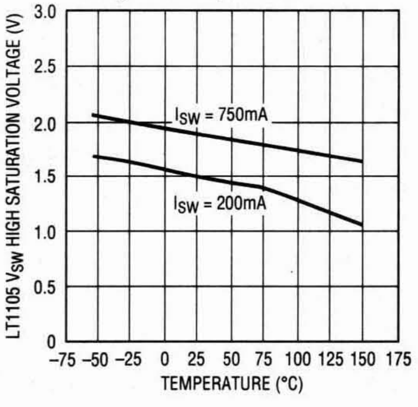
LT1103 G41

LT1105 V_{SW} Low Saturation Voltage vs Temperature



LT1103 G42

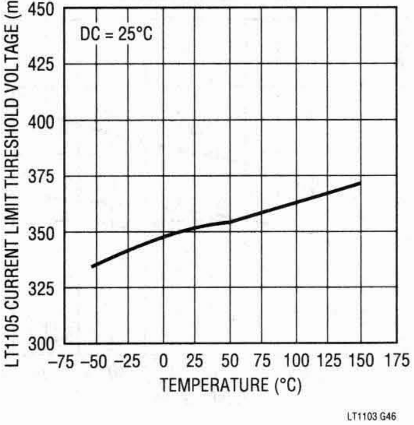
LT1105 V_{SW} High Saturation Voltage vs Temperature



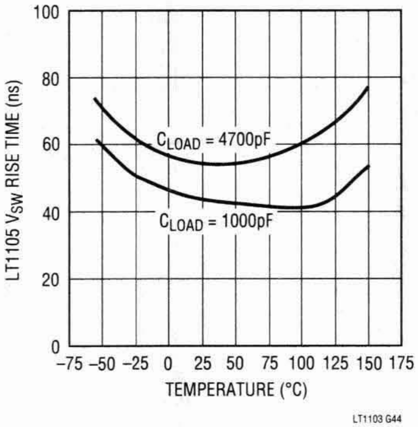
LT1103 G43

TYPICAL PERFORMANCE CHARACTERISTICS

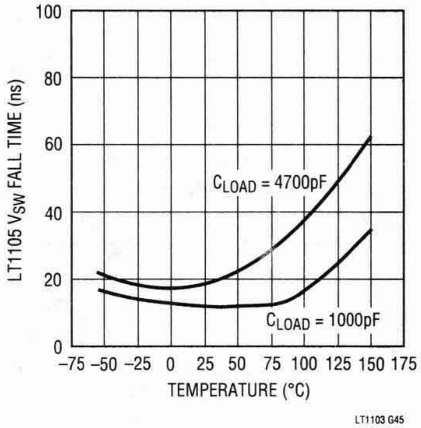
LT1105 Current Limit Threshold Voltage vs Temperature



LT1105 V_{SW} Rise Time vs Temperature



LT1105 V_{SW} Fall Time vs Temperature



PIN FUNCTIONS

LT1103

FB: The Feedback pin is the inverting input to the sampling error amplifier. The noninverting input is tied to a 4.5V reference. The FB pin is used for output voltage sensing. The input bias current is a function of the control pin V_C voltage and can be used for load regulation compensation by including a resistor in series with the FB pin. The sampling error amplifier has a typical gm of 0.012 mhos and the output of the sampling error amplifier has asymmetrical slew rate to reduce overshoot during startup conditions or following the release of an output overload.

V_C: The V_C control pin is used for frequency compensation, current limiting and shutdown. It is the high impedance output of the sampling error amplifier and the input of the current limit comparator.

GND: The Ground pin acts as both the negative sense point for the internal sampling error amplifier feedback signal and as the high current path for the 2A switch. Also, the case of the 7-lead TO-220 is connected to ground. Proper connections to ground for signal paths and high current paths must be made in order to insure good load regulation.

OSC: The Oscillator pin sets the operating frequency of the regulator with one external capacitor to ground. Maximum duty cycle can also be adjusted by using an external resistor to alter the charge/discharge ratio.

V_{IN}: The Input Supply pin is designed to operate with voltages of 12V to 30V. The supply current is typically 200μA up to the startup threshold of 16V. Normal operating supply current is fairly flat at 18mA down to the shutdown threshold of 7V. Switching is inhibited for V_{IN} less than 12V due to the gate drive detection circuit.

15V: A 15V reference is used to bias the gate of an external power FET. The voltage temperature coefficient is typically 3mV/°C and the output can source 30mA. Typical dropout voltage is 1.5V for V_{IN} less than 17V and 30mA of load current.

V_{SW}: The Switch Output pin is the collector of the internal NPN power switch. This pin has a typical ON resistance of 0.4Ω and a minimum breakdown voltage of 50V. This pin also ties to the FET gate drive detection circuit.

LT1105

All functions on the LT1105 are equivalent to the LT1103 with the exception of the V_{SW} pin and the I_{LIM} pin and the availability of the OVLO, 5V, and SS functions.

OVLO: The Overvoltage Lockout pin inhibits switching when the pin is pulled above its threshold voltage of 2.5V.

PIN FUNCTIONS

OVLO is implemented with a resistor divider network from the rectified DC line and is used to protect the external FET from an overvoltage condition in the off state. This function is only available on the 14-lead DIP.

5V: A 5V reference is available to power primary-side circuitry. The temperature coefficient is typically 50ppm/°C and the output can source 25mA. This function is only available on the 14-lead DIP.

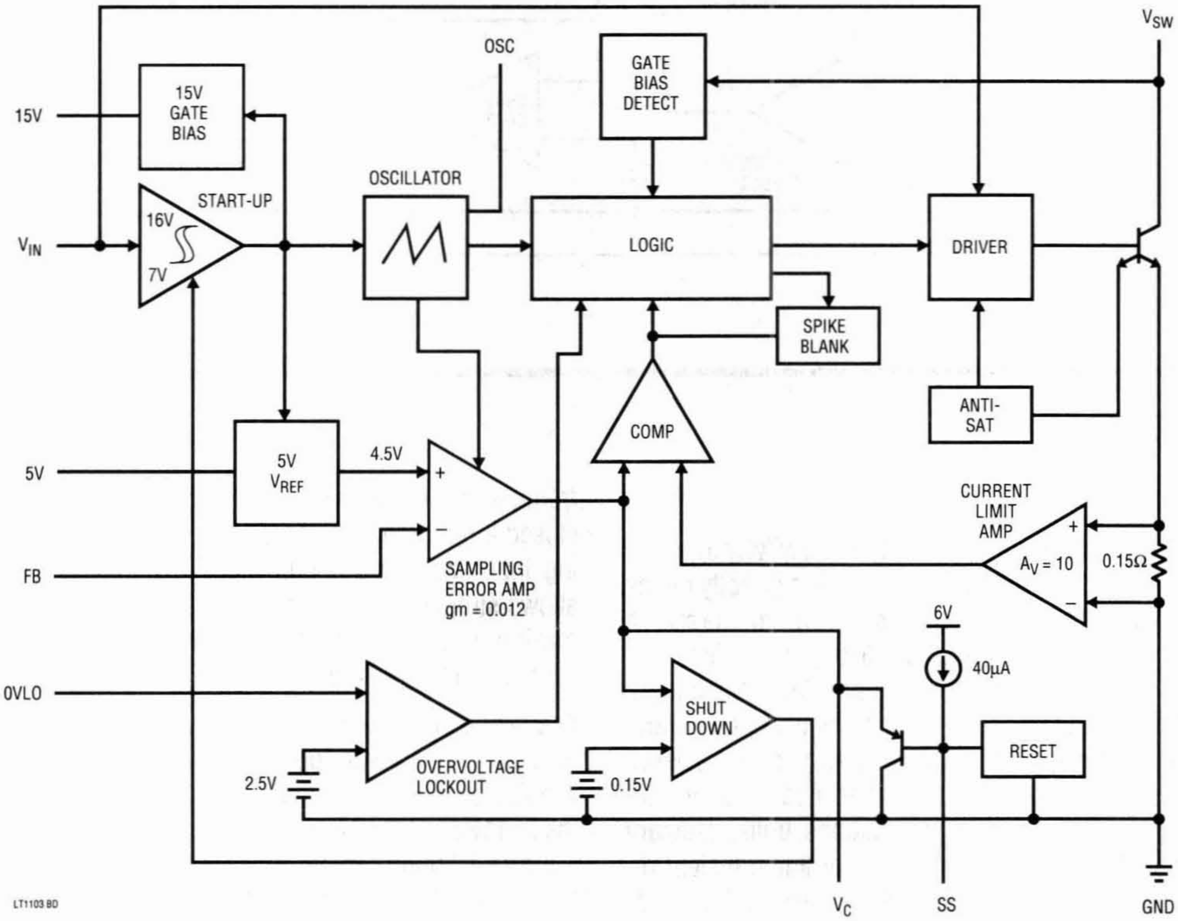
SS: The Soft-start pin is used to either program start-up time with a capacitor to ground or to set external current limit with a resistor divider. The SS pin has a 40µA pullup current and is reset to 0V by a 1mA pulldown current during startup and shutdown. This function is only available on the 14-lead DIP.

V_{SW}: The Switch Output pin is the output of a 1A NPN totem pole stage. The V_{SW} pin turns the external FET on by pulling its gate high. Break-Before-Make action of 200ns on each switch edge is built in to eliminate cross-conduction currents.

I_{LIM}: The I_{LIM} pin is the input to the current limit amplifier and requires the use of a non-inductive, power sense resistor from I_{LIM} to ground to set current limit. The typical current limit threshold voltage is 350mV.

BLOCK DIAGRAMS

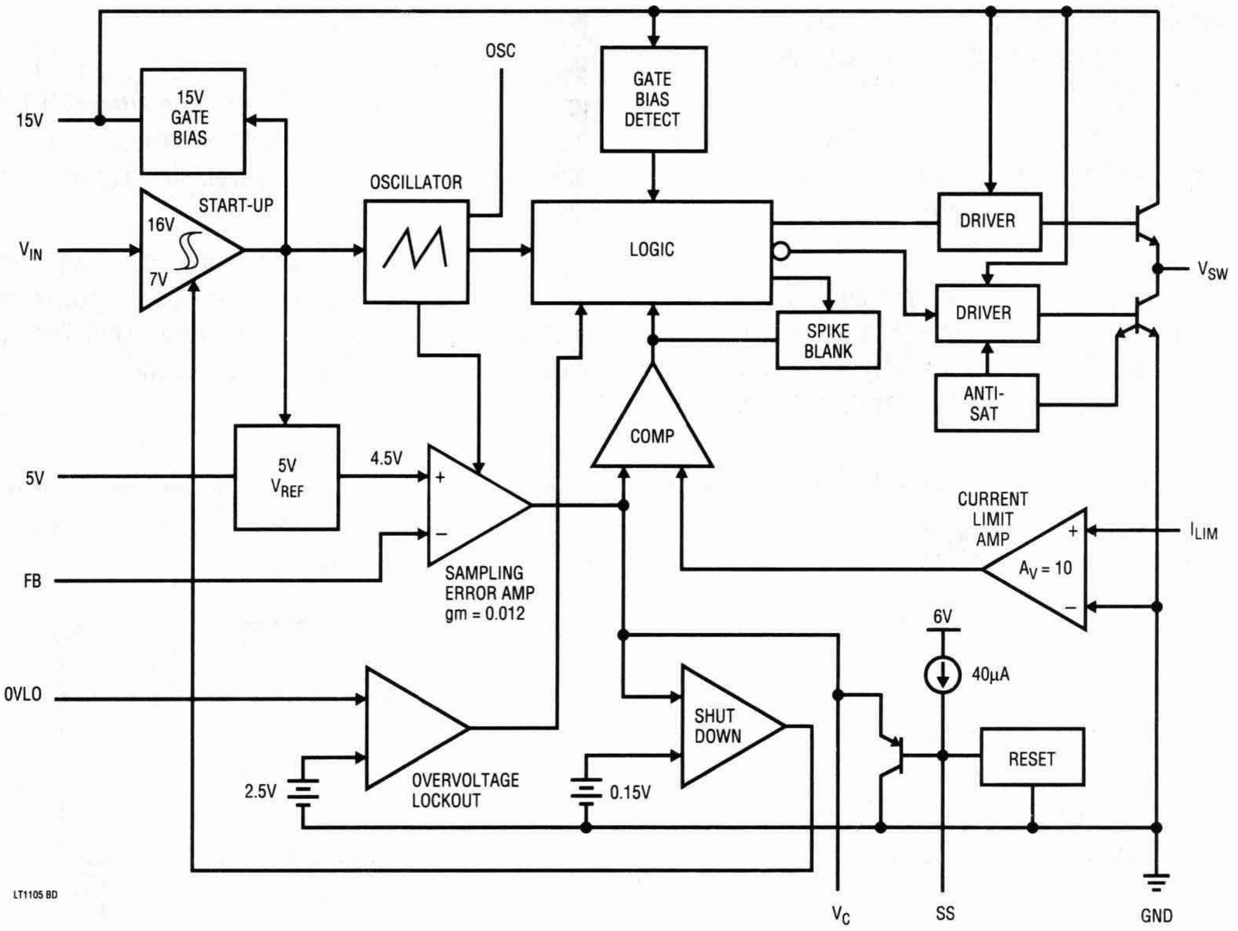
LT1103



15V
V_IN
5V
FB
OVLO
15V GATE BIAS
START-UP
16V
7V
OSCILLATOR
OSC
GATE BIAS DETECT
LOGIC
DRIVER
V_SW
SPIKE BLANK
COMP
ANTI-SAT
5V V_REF
4.5V
+
−
SAMPLING ERROR AMP gm = 0.012
CURRENT LIMIT AMP
A_V = 10
0.15Ω
6V
40µA
OVERVOLTAGE LOCKOUT
2.5V
SHUT DOWN
0.15V
RESET
V_C
SS
GND
LT1103 BD

BLOCK DIAGRAMS

LT1105


15V
15V GATE BIAS
GATE BIAS DETECT
OSC
OSCILLATOR
START-UP
16V
7V
VIN
LOGIC
DRIVER
DRIVER
SPIKE BLANK
ANTI-SAT
V_SW
COMP
5V
5V V_REF
4.5V
+
−
SAMPLING ERROR AMP gm = 0.012
FB
CURRENT LIMIT AMP
A_V = 10
I_LIM
6V
40μA
OVLO
OVERVOLTAGE LOCKOUT
2.5V
SHUT DOWN
0.15V
RESET
V_C
SS
GND
LT1105 BD

OPERATION

LT1103

The LT1103 is a current-mode switcher. Switch duty cycle is controlled by switch current rather than directly by the output voltage. Referring to the block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a pre-determined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the transformer. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

A start-up loop with hysteresis allows the IC supply voltage to be bootstrapped from an extra primary-side winding on the power transformer. From 0V to 16V on V_{IN}, the LT1103 is in a pre-start mode and total input current is typically 200μA. Above 16V, up to 30V, the 6V regulator that biases the internal circuitry and the externally avail-

OPERATION

able 15V regulator is turned on. The internal circuitry remains biased on until V_{IN} drops below 7V and the part returns to the pre-start mode. Output switching stops when the V_{SW} drive is less than 10V corresponding to V_{IN} of about 12V.

The oscillator provides the basic clock for all internal timing. Frequency is adjustable to 200kHz with one external capacitor from OSC to ground. The oscillator turns on the output switch via the logic and driver circuitry. Adaptive anti-sat circuitry detects the onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

The LT1103 is designed to drive the source of an external power FET in common-gate configuration. The 15V regulator biases the gate to guarantee the FET is on when the switch is on. Special drive detection circuitry senses the gate bias voltage and prevents the output switch from turning on if the gate voltage is less than 10V or greater than 20V, the industry standards for power MOSFET operation.

The switch current is sensed internally and amplified to trip the comparator and turn off the switch according to the V_C pin control voltage. A blanking circuit suppresses the output of the current limit comparator for 500ns at the beginning of each switch cycle. This prevents false tripping of the comparator due to current spikes caused by external parasitic capacitance and diode stored charge.

The 4.5V Zener-based reference biases the positive input of the sampling error amplifier. The negative input (FB) is used for output voltage sensing. The sampling error amplifier allows the LT1103 to operate in fully-isolated flyback mode by regulating from the flyback voltage of the bootstrap winding. The leakage inductance spike at the leading edge of the flyback waveform is ignored with a blanking circuit. The flyback waveform is directly proportional to the output voltage in a transformer-coupled flyback topology. Output voltages are fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings.

The error signal developed at the comparator input is brought out externally. This V_C pin has three functions including frequency compensation, current limit adjustment, and total regulator shutdown. During normal operation, this pin sits at a voltage between 1.2V (low output current) and 4.4V (high output current). The error amplifier is a current output (gm) type, so this voltage can be externally clamped for adjusting current limit. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1103 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown and places the LT1103 in a pre-start mode.

LT1105

The LT1105 is a current-mode switcher. Switch duty cycle is controlled by switch current rather than directly by output voltage. Referring to the block diagram, the switch is turned on at the start of each oscillator cycle. It is turned off when switch current reaches a pre-determined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the transformer. This greatly simplifies closed loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

A start-up loop with hysteresis allows the IC supply voltage to be bootstrapped from an extra primary-side winding on the power transformer. From 0V to 16V on V_{IN}, the LT1105 is in pre-start mode and total input current is typically 200μA. Above 16V, up to 30V, the 6V regulator that biases the internal circuitry and the externally available 5V and 15V regulators are turned on. The internal circuitry remains biased on until V_{IN} drops below 7V and the part returns to pre-start mode. Output switching stops when the 15V gate bias reference is less than 10V corresponding to V_{IN} of about 12V.

OPERATION

The oscillator provides the basic clock for all internal timing. Frequency is adjustable to 200kHz with one external capacitor from OSC to ground. The oscillator turns on the output switch via the logic and driver circuitry.

The LT1105 is designed to drive the gate of an external power FET in common-source configuration. The drivers and the 1A maximum totem-pole output stage are biased from the 15V gate bias reference. Special drive detection circuity senses the gate bias reference voltage and prevents the output switch from turning on if this voltage is less than 10V or greater than 20V. Break-Before-Make action of 200ns is built into each switch edge to eliminate cross conduction currents.

Switch current is sensed externally through a precision, power resistor. This allows for greater flexibility in switch current and output power than allowed by the LT1103. The voltage across the sense resistor is fed into the I_{LIM} pin and amplified to trip the comparator and turn off the switch according to the V_C pin control voltage. A blanking circuit suppresses the output of the current limit comparator for 500ns at the beginning of each switch cycle. This prevents false tripping of the comparator due to current spikes caused by external parasitic capacitance and diode stored charge.

A 4.5V Zener-based reference biases the positive input of the sampling error amplifier. The negative input (FB) is used for output voltage sensing. The sampling error amplifier allows the LT1105 to operate in fully-isolated flyback mode by regulating the flyback voltage of the bootstrap winding. The leakage inductance spike at the leading edge of the flyback waveform is ignored with a blanking circuit. The flyback waveform is directly proportional to the output voltage in the transformer-coupled flyback topology. Output voltages are fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings.

The error signal developed at the comparator input is brought out externally. The V_C pin has three functions including frequency compensation, current limit adjustment, and total regulator shutdown. During normal operation, this pin sits at a voltage between 1.2V (low output current) and 4.4V (high output current). The error amplifier is a current output (gm) type, so this voltage can be externally clamped for adjusting current limit. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1105 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown and places the LT1105 in pre-start mode.

The SS pin implements soft-start with one external capacitor to ground. The internal pullup current and clamp transistor limit the voltage at V_C to one diode drop above the voltage at the SS pin, thereby controlling the rate of rise of switch current in the regulator. The SS pin is reset to 0V when the LT1105 is in pre-start mode.

A final protection feature includes overvoltage lockout monitoring of the main supply voltage on the OVLO pin. If the OVLO pin is greater than 2.5V, the output switch is prevented from turning on. This function can be disabled by grounding the OVLO pin.

APPLICATIONS INFORMATION

Bootstrap Start

It is inefficient as well as impractical to power a switching regulator control IC from the rectified DC input as this voltage is several hundred volts. Self-biased switching regulator topologies take advantage of a lower voltage auxiliary winding on the power transformer or inductor to power the regulator, but require a startup cycle to begin regulation.

Start-up circuitry with hysteresis built into the LT1103/LT1105 allows the input voltage to increase from 0V to 16V before the regulator tries to start. During this time the startup current of the switching regulator is typically 200μA and all internal voltage regulators are off. The low quiescent current allows the input voltage to be trickled up with only 500μA of current from the rectified DC line voltage, thereby minimizing power dissipation in the startup resistor. At 16V, the internal voltage regulators are turned

APPLICATIONS INFORMATION

on and switching begins. If enough power feeds back through the auxiliary winding to keep the input voltage to the switching regulator above 12V, then switching continues and a bootstrap start is accomplished. If the input voltage drops below 12V, then the FET drive detection circuit locks out switching. The input voltage continues to fall as the V_{IN} bypass capacitor is discharged by the normal quiescent current of the LT1103/LT1105. Once the input voltage falls below 7V, the internal voltage regulators are turned off and the switching regulator returns to the low startup current state. A continuous "burp start" mode indicates a fault condition or an incomplete power loop.

The trickle current required to bootstrap the regulator input voltage is typically generated with a resistor from the rectified DC input voltage. When combined with the regulator input bypass capacitor, the startup resistor creates a ramp whose slope governs the turn-on time of the regulator as well as the period of the "burp start" mode. The design trade-offs are power dissipated in the trickle resistor, the turn-on time of the regulator, and the hold-up time of the regulator input bypass capacitor. The value of the startup resistor is set by the minimum rectified DC input voltage to guarantee sufficient startup current. The recommended minimum trickle current is 500µA. The power rating of the startup resistor is set by the maximum rectified DC input voltage. A final consideration for the startup resistor is to insure that the maximum voltage rating of the resistor is not exceeded. Typical carbon film resistors have a voltage rating of 250V. The most reliable and economical solution for the startup resistor is generally provided by placing several 0.25W resistor in series.

The LT1103/LT1105 is designed to operate with supply pin voltages up to 30V. However, the auxiliary bias winding should be designed for a typical output voltage of 17V to minimize IC power dissipation and efficiency loss. Allowances must also be made for cross regulation of the bias voltage due to variations in the rectified DC line voltage and output load current.

Soft-Start

Soft-start refers to the controlled increase of switch current from a startup or shutdown state. This allows the power supply to come up to voltage in a controlled manner and charge the output capacitor without activating current limit. In general, soft-start is not required on the LT1105 due to the design of the sampling error amplifier gm stage which generates asymmetrical slew capability on the V_C pin.

This feature exhibits itself as a typical 3mA sink current capability on the V_C pin whereas source current is only 275µA. The low gm of the error amplifier allows small-valued compensation capacitors to be used on V_C. This allows the sink current to slew the compensation capacitor quickly. Therefore, overshoot of the output voltage on startup sequences and recovery from overload or short circuit conditions is prevented. However, if a longer startup period is required, the soft-start function can be used.

Soft-start is implemented with an internal 40µA pullup and a transistor clamp on the V_C pin so that a single external capacitor from SS ground can define the linear ramp function. The voltage at V_C is limited to one V_{BE} above the Soft-start pin (SS). The time to maximum switch current is defined as the capacitance on SS multiplied by the active range in volts of the V_C pin divided by the pullup current:

$$T = \frac{C \bullet (3.2V)}{40\mu A}$$

SS is reset to 0V whenever V_{IN} is less than 7V (pre-start mode) or when shutdown is activated by pulling V_C below 0.15V. The SS pin has a guaranteed reset sink current of 1mA when either the regulator supply voltage V_{IN} falls below 7V or the regulator is placed in shutdown.

Shutdown

The LT1103/LT1105 can be put in a low quiescent current shutdown mode by pulling V_C below 150mV. In the shutdown mode the internal voltage regulators are turned off, SS is reset to 0V and the part draws less than 200µA. To initiate shutdown, about 400µA must be pulled out of V_C until the internal voltage regulators turn off. Then, less than 50µA pulldown current is required to maintain shutdown. The shutdown function has about 60mV of hysteresis on the V_C pin before the part returns to normal

APPLICATIONS INFORMATION

operation. Soft-start, if used, controls the recovery from shutdown.

5V Reference

A 5V reference output is available for the user's convenience to power primary-side circuitry or to generate a clamp voltage for switch current limiting. The output will source 25mA and the voltage temperature coefficient is typically 50ppm/°C. If bypassing of the 5V reference is required, a 0.1µF is recommended. Values of capacitance greater than 1µF may be susceptible to ringing due to decreased phase margin. In such cases, the capacitive load can be isolated from the reference output with a small series resistor at the expense of load regulation performance.

Overvoltage Lockout

The switching supply and primarily the external power MOSFET can be protected from an extreme surge of the input line voltage with the overvoltage lockout feature implemented on the OVLO pin. If the voltage on OVLO rises above its typical threshold voltage of 2.5V, output switching is inhibited. This feature can be implemented with a resistive divider off of the rectified DC input voltage. This feature is only available on the LT1105 in the 14-lead DIP and must be tied to ground if left unused.

Ground (LT1103)

The ground pin of the LT1103 is important because it acts as the negative sense point for the internal error amplifier feedback signal, the negative sense point for the current limit amplifier and as the high current path for the 2A switch. The tab of the 7-lead TO-220 is internally connected to ground (pin 4).

To avoid degradation of load regulation, the feedback resistor divider string and the reference side of the bias winding should be directly connected to the ground pin on the package. These ground connections should not be mixed with high current carrying ground return paths. The length of the switch current ground path should be as short as possible to the input supply bypass capacitor and low resistance for best performance. The case of the LT1103 package is desirable to use as the high current ground return path as this is a lower resistive and inductive path than that of the actual package pin and will help minimize voltage spikes associated with the high dI/dt switch current.

Avoiding long wire runs to the ground pin minimizes load regulation effects and inductive voltages created by the high dI/dt switch current. Ground plane techniques should also be used and will help keep EMI to a minimum. Grounding techniques are illustrated in the Typical Applications section.

Ground (LT1105)

The ground pin of the LT1105 is important because it acts as the negative sense point for the internal error amplifier feedback signal and as the negative sense point for the current limit amplifier. The LT1105 8-pin MiniDIP has pin 1 as its ground. The LT1105 14-pin DIP has pin 1 and pin 7 as grounds and must be tied together for proper operation.

To avoid degradation of load regulation, the feedback resistor divider should be directly connected to the package ground pin. These ground connections should not be mixed with high current carrying ground return paths. The length of the switch current ground path should be as short as possible to the input supply bypass capacitor and low resistance for best performance. This will help minimize voltage spikes associated with the high dI/dt switch current.

Avoiding long wire runs to the ground pin minimizes load regulation effects and inductive voltages created by the high dI/dt switch current. Ground plane techniques should also be used and will help keep EMI to a minimum. Grounding techniques are illustrated in the Typical Applications section.

Oscillator

The oscillator of the LT1103/LT1105 is a linear ramp type powered from the internal 6V bias line. The charging currents and voltage thresholds are generated internally so that only one external capacitor is required to set the frequency. The 150µA pullup current, which is on all the time, sets the preset maximum on-time of the switch and

APPLICATIONS INFORMATION

the 450μA pulldown current which is turned on and off, sets the dead time. The threshold voltages are typically 2V and 4.5V, so for a 400pF capacitor the ramp-up time of the voltage on the OSC pin is 6.67μs and the ramp-down time is 3.3μs, resulting in an operating frequency of 100kHz. Although the oscillator, as well as the rest of the switching regulator, will function at higher frequencies, 200kHz is the practical upper limit that will allow control range for line and load regulation. The lowest operating frequency is limited by the sampling error amplifier to about 10kHz.

The frequency temperature coefficient is typically –80ppm/°C with a good low T.C. capacitor. This means that with a low temperature coefficient capacitor, the temperature coefficient of the currents and the temperature coefficient of the thresholds sum to –80ppm/°C over the commercial temperature range. Bowing in the temperature coefficient of the currents affects the frequency about ±3% at the extremes of the military temperature range. The capacitor type chosen will have a direct effect on the frequency tempco.

Maximum duty cycle is set internally by the pullup and pulldown currents, independent of frequency. It can be adjusted externally by modifying the fixed pullup current with an additional resistor. In practice, one resistor from the OSC pin to the 5V reference or to ground does the job. Note that the capacitor value must change to maintain the same frequency. For example, a 24k resistor from 5V to OSC and a 440pF capacitor from OSC to ground will yield 100kHz with 50% maximum duty cycle. A 56k resistor and a 280pF capacitor from OSC to ground will yield 100 kHz with 80% maximum duty cycle.

The oscillator can be synchronized to an external clock by coupling a sync pulse into the OSC pin. The width of this pulse should be a minimum of 500ns. The oscillator can only be synchronized up in frequency and the synchronizing frequency must be greater than the maximum possible unsynchronized frequency (for the chosen oscillator capacitor value). The amplitude of the sync pulse must be chosen so that the sum of the oscillator voltage amplitude plus the sync pulse amplitude does not exceed the 6V bias reference. Otherwise, the oscillator pullup current source will saturate and erroneous operation will result. If the LT1103/LT1105 is positioned on the primary side of the transformer and the external clock on the isolated secondary output side, the sync signal must be coupled into the OSC pin using a pulse transformer. The pulse transformer must meet all safety/isolation requirements as it also crosses the isolation boundary. An example of externally synchronizing the oscillator is shown in the Typical Applications section.

Gate Biasing (LT1103)

The LT1103 is designed to drive an external power MOSFET in the common-gate or cascode connection with the V_{SW} pin. The advantage is that the switch current can be sensed internally, eliminating a low-value, power sense resistor. The gate needs to be biased at a voltage high enough to guarantee that the FET is saturated when the open-collector source drive is on. This means 10V as specified in FET data sheets, plus 1V for the typical switch saturation voltage, plus a couple of volts for temperature variations and processing tolerances. This leads to 15V for a practical gate bias voltage.

Power MOSFETs are well suited to switching power supplies because their high speed switching characteristics promote high switching efficiency. To achieve high switching speed, the gate capacitance must be charged and discharged quickly with high peak currents. In particular, the turn-off current can be as high as the peak switch current. The switching speed is controlled by the impedance seen by the gate capacitance. Practically speaking, zero impedance is not desirable because of the high frequency noise spikes introduced to the system. The gate bias should be bypassed with a 1μF low ESR capacitor to ground and should have a 5Ω resistor or larger in series with the gate to define the source impedance.

The LT1103 provides a 15V output intended for biasing the gate of the MOSFET. It will source 30mA into a capacitive load with no stability problems. The voltage temperature coefficient is +3mV/°C. If V_{IN} drops below 17V, the 15V output follows about 2.0V below V_{IN} until the part shuts down. If the 15V output is pulled above 17.5V, it will sink 5mA.

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A special circuit in the LT1103 senses the voltage at V_{SW} prior to turning on the switch. V_{SW} is tied to the source of the FET and should represent the bias voltage on the gate when the switch is off. When the switch first turns off, the drain flies back until it is clamped by a snubber network. The source also flies high due to parasitic capacitive coupling on the FET and parasitic inductance of the leads. An extra diode from the source to the gate or V_{IN} will provide insurance against fault conditions that might otherwise damage the FET. The diode clamps the source to one diode drop above the gate or V_{IN}, thereby limiting the gate-source reverse bias. Once the energy in the leakage inductance spike is dissipated and the primary is being regulated to its flyback voltage, the diode shuts off. The source is then floating and its voltage will be close to the gate voltage. If the sensed voltage on V_{SW} is less than 10V or greater than 20V, the circuit prevents the switch from turning on. This protects the FET from dissipating high power in a non-saturated state or from excessive gate-source voltage. The oscillator continues to run and the net effect is to skip switching cycles until the gate bias voltage is corrected. One consequence of the gate bias detection circuit is that the startup window is 6V if the gate is biased from V_{IN} and to 4V if the gate is biased from the 15V output. This influences the size of the bypass capacitor on V_{IN}.

V_{SW} Output (LT1103)

The V_{SW} pin of the LT1103 is the collector of an internal NPN power switch. This NPN has a typical on resistance of 0.4Ω and a typical breakdown voltage (BV_{CBO}) of 75V. Fast switching times and high efficiency are obtained by using a special driver loop which automatically adapts base drive current to the minimum required to keep the switch in a quasi-saturated state. The key element in the loop is an extra emitter on the output power transistor as seen in the block diagram. This emitter carries no current when the NPN output transistor collector is high (unsaturated). In this condition, the driver circuit can deliver very high base drive to the switch for fast turn-on. When the switch saturates, the extra emitter acts as a collector of an NPN operating in inverted mode and pulls base current away from the driver. This linear feedback loop serves itself to keep the switch just at the edge of saturation. Very low switch current results in nearly zero driver current and high switch currents automatically increase driver current as necessary. The ratio of switch current to driver current is approximately 30:1. This ratio is determined by the sizing of the extra emitter and the value of the current source feeding the driver circuitry. The quasi-saturation state of the switch permits rapid turn-off without the need for reverse base-emitter voltage drive.

Gate Biasing (LT1105)

The LT1105 is designed to drive an external power MOSFET in the common-source configuration with the totem-pole output V_{SW} pin. The advantage is added switch current flexibility (limited only by the choice of external power FET) and higher output power applications than allowed by LT1103. An external, non-inductive, power sense resistor must be used in series with the source of the FET to detect switch current and must be tied to the input of the current limit amplifier. The gate needs to be biased at a voltage high enough to guarantee that the FET is saturated when the totem-pole gate drive is on. This means 10V as specified in FET data sheets, plus the totem-pole high side saturation voltage plus a couple of volts for temperature variations and processing tolerances. This leads to 15V for a practical gate bias voltage.

Power MOSFETs are well suited to switching power supplies because their high speed switching characteristics promote high switching efficiency. To achieve high switching speed, the gate capacitance must be charged and discharged quickly with high peak currents. In particular, the turn-off current can be as high as the peak switch current. The switching speed is controlled by the impedance seen by the gate capacitance. Practically speaking, zero impedance is not desirable because of the high frequency noise spikes introduced to the system. The gate bias supply which drives the totem-pole output stage should be bypassed with a 1μF low ESR capacitor to ground. This capacitor supplies the energy to charge the gate capacitance during gate drive turn-on. The power MOSFET should have a 5Ω

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resistor or larger in series with its gate from the V_{SW} pin to define the source impedance.

The LT1105 provides a 15V regulated output intended for driving the totem-pole output stage. It will source 30mA into a capacitive load with no stability problems. The output voltage temperature coefficient is +3mV/°C. If V_{IN} drops below 17V, the 15V output follows about 2.0V below V_{IN} until the part shuts down. If the 15V output is pulled above 17.5V, it will sink 5mA.

A special circuit in the LT1105 senses the voltage at the 15V regulated output prior to turning on the switch. The 15V regulator drives the totem-pole output stage and the V_{SW} pin will pull the gate of the FET very close to the value of the 15V output when V_{SW} turns on. Therefore, the 15V output represents what the gate bias voltage on the FET will be when the FET is turned on. If the sensed voltage on the 15V output is less than 10V or greater than 20V, the circuit prevents the switch from turning on. This protects the FET from dissipating high power in a non-saturated state or from excessive gate-source voltage. The oscillator continues to run and the net effect is to skip switching cycles until the gate bias voltage is corrected. One consequence of the gate bias detection circuit is that the startup window is 4V. This influences the size of the bypass capacitor on V_{IN}.

V_{SW} Output (LT1105)

The V_{SW} pin of the LT1105 is the output of a 1A totem-pole driver stage. This output stage turns an external power MOSFET on by pulling its gate high. Break-Before-Make action of 200ns is built into each switch edge to eliminate cross-conduction currents. Fast switching times and high efficiency are obtained by using a low loss output stage and a special driver loop which automatically adapts base drive current to the totem-pole low-side drive. The key element in the loop is an extra emitter on the output pull-down transistor as seen in the block diagram. This emitter carries no current when the low-side transistor collector is high (unsaturated). In this condition, the driver can deliver very high base drive to the output transistor for fast turn-off. When the low-side transistor saturates, the extra emitter acts as a collector of an NPN operating in inverted mode and pulls base current away from the driver. This linear feedback loop serves itself to keep the switch just at the edge of saturation. This results in nearly zero driver current. The quasi-saturation state of the low-side switch permits rapid turn-on of the external FET when V_{SW} pulls high.

Fully-Isolated Flyback Mode

A unique sampling error amplifier included in the control loop of the LT1103/LT1105 eliminates the need for an opto-isolator while providing ±1% line and load regulation in a magnetic flux-sensed flyback converter. In this mode, the flyback voltage on the primary during "switch off" time is sensed and regulated. It is difficult to derive a feedback signal directly from the primary flyback voltage as this voltage is typically several hundred volts. A dedicated winding is not required because the bias winding for the regulator lends itself to flux-sensing. Flux-sensing made practical simplifies the design of offline power supplies by minimizing the total number of external components and reduces the components which must cross the isolation barrier to one, the transformer. This inherently implies greater safety and reliability. The transformer must be optimized for coupling between the bias winding and the secondary output winding(s) while maintaining the required isolation and minimizing the parasitic leakage inductances.

Although magnetic flux-sensing has been used in the past, the technique has exhibited poor output voltage regulation due to the parasitics present in a transformer-coupled design. Transformers which provide the safety and isolation as required by various international safety/regulatory agencies also provide the poorest output voltage regulation. Solutions to these parasitic elements have been achieved with the novel sampling error amplifier of the LT1103/LT1105. A brief review of flyback converter operation and the problems which create a poorly regulated output will provide insight on how the sampling error amplifier of the LT1103/LT1105 addresses the regulation issue of magnetic flux-sensed converters.

The following figure shows a simplified diagram of a flyback converter using magnetic flux-sensing. The major parasitic elements present in the transformer-coupled

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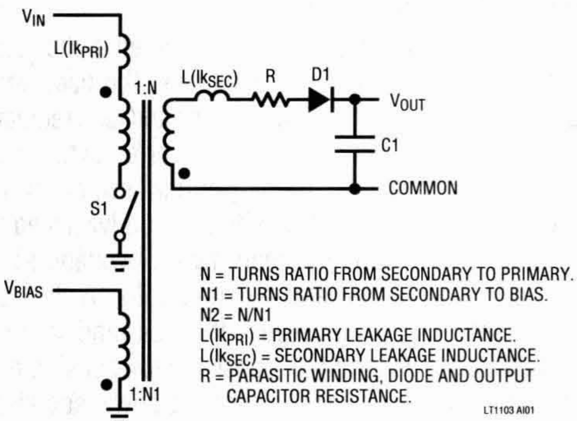
design are indicated. The relationships between the primary voltage, the secondary voltage, the bias voltage and the winding currents are indicated in the figures found on the following page for both continuous and discontinuous modes of operation.

Simplified Flyback Converter



N = TURNS RATIO FROM SECONDARY TO PRIMARY.
N1 = TURNS RATIO FROM SECONDARY TO BIAS.
N2 = N/N1
$L(Ik_{PRI})$ = PRIMARY LEAKAGE INDUCTANCE.
$L(Ik_{SEC})$ = SECONDARY LEAKAGE INDUCTANCE.
R = PARASITIC WINDING, DIODE AND OUTPUT CAPACITOR RESISTANCE.

When the switch "turns on," the primary winding sees the input voltage and the secondary and bias windings go to negative voltages as a function of the turns ratio. Current builds in the primary winding as the transformer stores energy. When the switch "turns off," the voltage across the switch flies back to a clamp level as defined by a snubber network until the energy in the leakage inductance of the primary dissipates. Leakage inductance is one of the main parasitic elements in a flux-sensed converter and is modeled as an inductor in series with the primary and secondary of the transformer. These parasitic inductances contribute to changes in the bias winding voltage and thus the output voltage with increasing load current.

The energy stored in the transformer transfers through the secondary and bias windings during "switch off" time. Ideally, the voltage across the bias winding is set by the DC output voltage, the forward voltage of the output diode, and the turns ratio of the transformer after the energy in the leakage inductance spike of the primary is dissipated.

This relationship holds until the energy in the transformer drops to zero (discontinuous mode) or the switch turns on again (continuous mode). Either case results in the voltage across the secondary and bias windings decreasing to zero or changing polarity. Therefore, the voltage on the bias winding is only valid as a representation of the output voltage while the secondary is delivering current.

Although the bias winding flyback voltage is a representation of the output voltage, its voltage is not constant. For a brief period following the leakage inductance spike, the bias winding flyback voltage decreases due to nonlinearities and parasitics present in the transformer. Following this nonlinear behavior is a period where the bias winding flyback voltage decreases linearly. This behavior is easily explained. Current flow in the secondary decreases linearly at a rate determined by the voltage across the secondary and the inductance of the secondary. The parasitic secondary leakage inductance appears as an impedance in series with the secondary winding. In addition, parasitic resistances exist in the secondary winding, the output diode and the output capacitor. These impedances can be combined to form a lumped sum equivalent and which cause a voltage drop as secondary current flows. This voltage drop is coupled from the secondary to the bias winding flyback voltage and becomes more significant as the output is loaded more heavily. This voltage drop is largest at the beginning of "switch off" time and smallest just prior to either all transformer energy being depleted or the switch turning on again.

The best representation of the output voltage is just prior to either all transformer energy being used up and the bias winding voltage collapsing to zero or just prior to the switch turning on again and the bias winding going negative. This point in time also represents the smallest forward voltage for the output diode. It is possible to redefine the relationship between the secondary winding voltage and the bias winding voltage as:

$$V_{BIAS} = \frac{\left(V_{OUT} + Vf + I \bullet R_P\right)}{N1}$$

where Vf is the forward voltage of the output diode, I is the current flowing in the secondary, R_P is the lumped sum equivalent secondary parasitic impedance and N1 is thetransformer turns ratio from the secondary to the bias winding. It is apparent that even though the above point in

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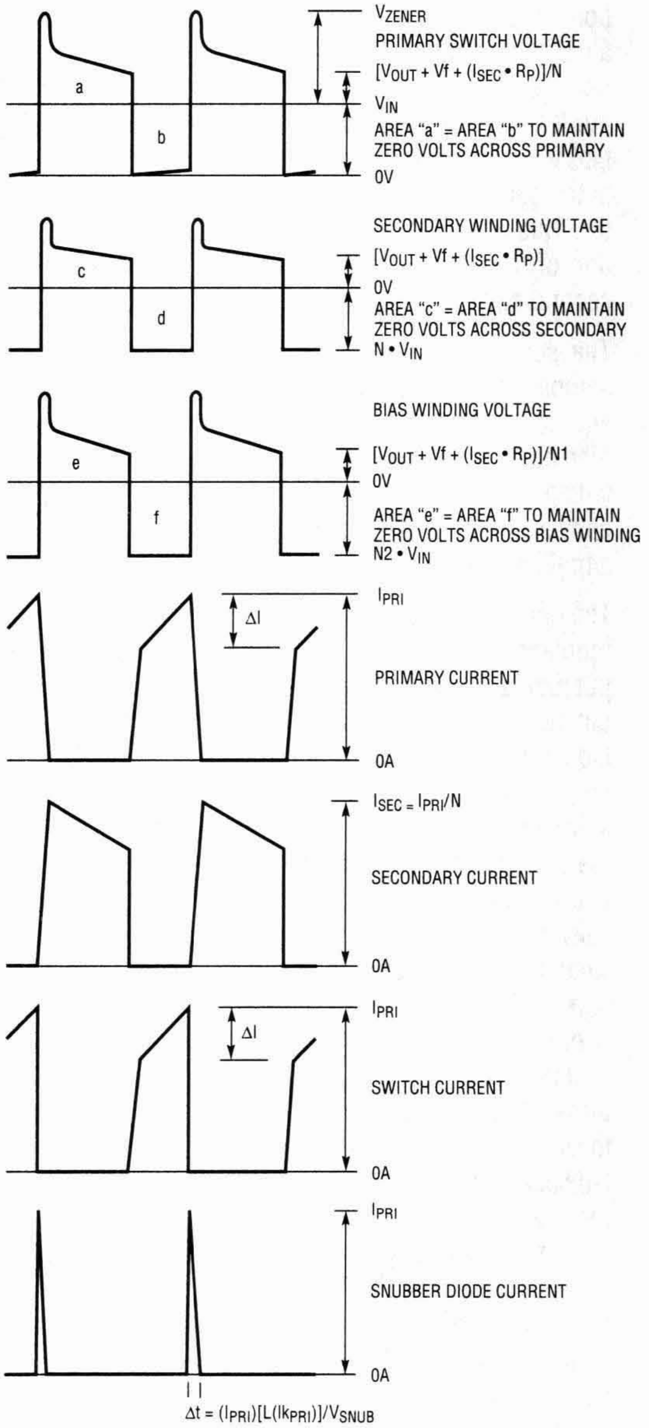
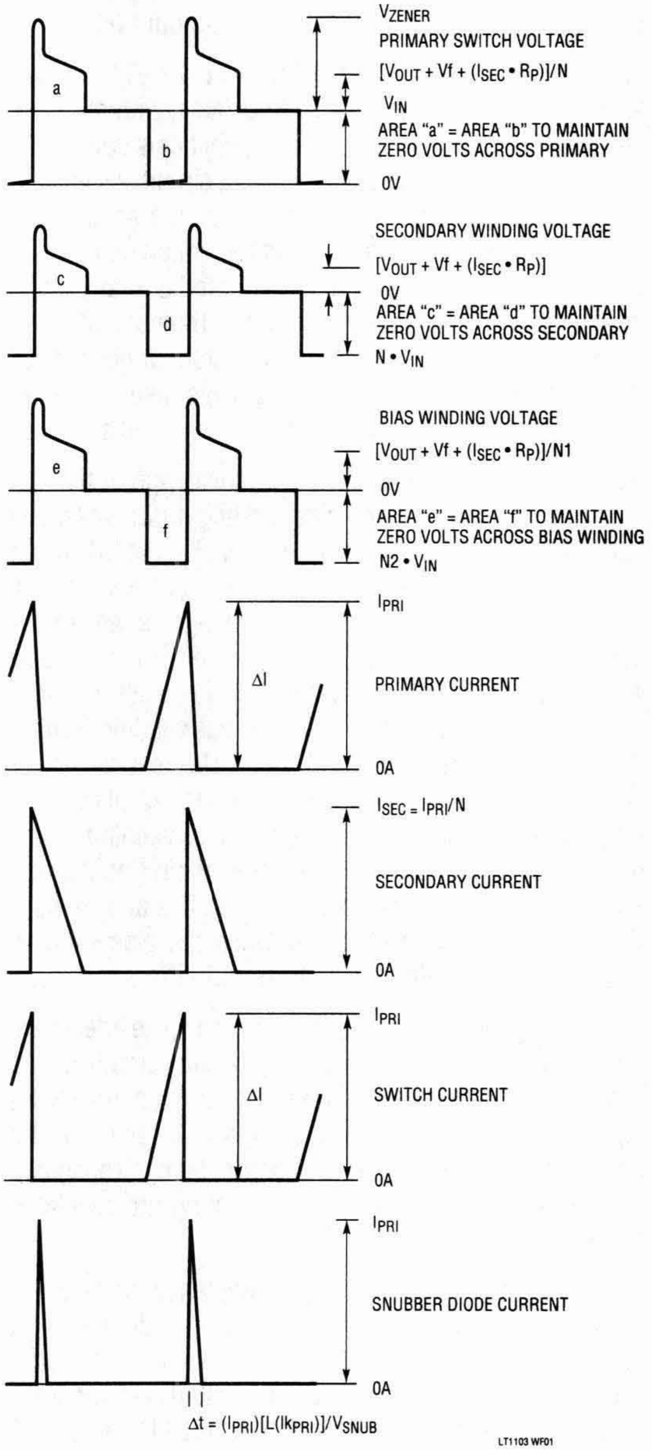
Flyback Waveform for Continuous Mode Operation


V_{ZENER}
PRIMARY SWITCH VOLTAGE
$[V_{OUT} + Vf + (I_{SEC} \bullet R_P)]/N$
V_{IN}
AREA "a" = AREA "b" TO MAINTAIN ZERO VOLTS ACROSS PRIMARY
0V
a
b
SECONDARY WINDING VOLTAGE
$[V_{OUT} + Vf + (I_{SEC} \bullet R_P)]$
0V
AREA "c" = AREA "d" TO MAINTAIN ZERO VOLTS ACROSS SECONDARY
$N \bullet V_{IN}$
c
d
BIAS WINDING VOLTAGE
$[V_{OUT} + Vf + (I_{SEC} \bullet R_P)]/N1$
0V
AREA "e" = AREA "f" TO MAINTAIN ZERO VOLTS ACROSS BIAS WINDING
$N2 \bullet V_{IN}$
e
f
I_{PRI}
ΔI
PRIMARY CURRENT
0A
$I_{SEC} = I_{PRI}/N$
SECONDARY CURRENT
0A
I_{PRI}
ΔI
SWITCH CURRENT
0A
I_{PRI}
SNUBBER DIODE CURRENT
0A
$\Delta t = (I_{PRI})[L(lk_{PRI})]/V_{SNUB}$

Flyback Waveform for Discontinuous Mode Operation


V_{ZENER}
PRIMARY SWITCH VOLTAGE
$[V_{OUT} + Vf + (I_{SEC} \bullet R_P)]/N$
V_{IN}
AREA "a" = AREA "b" TO MAINTAIN ZERO VOLTS ACROSS PRIMARY
0V
a
b
SECONDARY WINDING VOLTAGE
$[V_{OUT} + Vf + (I_{SEC} \bullet R_P)]$
0V
AREA "c" = AREA "d" TO MAINTAIN ZERO VOLTS ACROSS SECONDARY
$N \bullet V_{IN}$
c
d
BIAS WINDING VOLTAGE
$[V_{OUT} + Vf + (I_{SEC} \bullet R_P)]/N1$
0V
AREA "e" = AREA "f" TO MAINTAIN ZERO VOLTS ACROSS BIAS WINDING
$N2 \bullet V_{IN}$
e
f
I_{PRI}
ΔI
PRIMARY CURRENT
0A
$I_{SEC} = I_{PRI}/N$
SECONDARY CURRENT
0A
I_{PRI}
ΔI
SWITCH CURRENT
0A
I_{PRI}
SNUBBER DIODE CURRENT
0A
$\Delta t = (I_{PRI})[L(lk_{PRI})]/V_{SNUB}$
LT1103 WF01

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time is the most accurate representation of the output voltage, the answer given by the bias winding voltage is still off from the "true" answer by the amount I•R_P/N1.

The sampling error amplifier of the LT1103/LT1105 provides solutions to the errors associated with the bias winding flyback voltage. The error amplifier is comprised of a leakage inductance spike blanking circuit, a slew rate limited tracking amplifier, a level detector, a sample and hold, an output gm stage and load regulation compensation circuitry. This all seems complicated at first glance, but its operation is straightforward and transparent to the user of the IC. When viewed from a system or block level, the sampling error amplifier behaves like a simple transconductance amplifier. Here's how it works.

The sampling error amplifier takes advantage of the fact that the voltage across the bias winding during at least a portion of switch-off time is proportional to the DC output voltage of the secondary winding. The feedback network used to sense the bias winding voltage is no longer comprised of a traditional peak detector in conjunction with a resistor divider network. The feedback network consists of a diode in series with the bias winding feeding the resistor divider network directly. The resultant error signal is then fed into the input of the error amplifier. The purpose of the diode in series with the bias winding is now not to peak detect, but to prevent the FB pin (input of the error amplifier) from being pulled negative and forward biasing the substrate of the IC when the bias winding changes polarity with "switch turn-on."

The primary winding leakage inductance spike effects are first eliminated with an internal blanking circuit in the LT1103/LT1105 which suppresses the input of the FB pin for 1.5µs at the start of "switch off" time. This prevents the primary leakage inductance spike from being propagated through the error amplifier and affecting the regulated output voltage.

With the effects of the leakage inductance spike eliminated, the effects of decreasing bias winding flyback voltage can be addressed. With the traditional diode/capacitor peak detector circuitry eliminated from the feedback network, the tracking amplifier of the LT1103/LT1105 follows the flyback waveform as it changes with time and amplifies the difference between the flyback signal and the internal 4.5V reference. Tracking is maintained until the point in time where the bias winding voltage collapses as a result of all transformer energy being depleted (discontinuous mode) or the switch turning on again (continuous mode). The level detector circuit senses the fact that the bias winding flyback voltage is no longer a representation of the output voltage and activates an internal peak detector. This effectively saves the most accurate representation of the output voltage which is then buffered to the second stage of the error amplifier.

The second stage of the error amplifier consists of a sample and hold. When the switch turns on, the sample and hold samples the buffered error voltage for 1µs and then holds for the remainder of the switch cycle. This held voltage is then processed by the output gm stage and converted into a control signal at the output of the error amplifier, the V_C pin.

The final adjustment in regulation is provided by the load regulation compensation circuitry. As stated earlier, output regulation degrades with increasing load current (output power). The effect is traced to secondary leakage inductance and parasitic secondary winding, diode and output capacitor resistances. Even though the tracking amplifier has obtained the most accurate representation of the output voltage, its answer is still flawed by the amount of the voltage drop across the secondary parasitic lumped sum equivalent impedance which is coupled to the bias winding voltage. This error increases with increasing load current. Therefore, a technique for sensing load current conditions has been added to the LT1103/LT1105. The switch current is proportional to the load current by the turns ratio of the transformer. A small current proportional to switch current is generated in the LT1103/LT1105 and fed back to the FB pin. This allows the input bias current of the sampling error amplifier to be a function of load current. A resistor in series with the FB pin generates a linear increase in the effective reference voltage with increasing load current. This translates to a linear increase in output voltage with increasing load current. By adjusting the value of the series resistor, the slope of the load compensation can be set to cancel the effects of these parasitic voltage drops. The feature can be ignored by

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eliminating the series resistor and lowering the equivalent divider impedance to swamp out the effects of the input bias current.

Frequency Compensation

In order to prevent a regulator loop using the LT1103/LT1105 from oscillating, frequency compensation is required. Although the architecture of the LT1103/LT1105 is simple enough to lend itself to a mathematical approach to frequency compensation, the added complication of input/or output filters, unknown capacitor ESR, and gross operating point changes with input voltage and load current variations all suggest a more practical empirical approach. Many hours spent on breadboards have shown that the simplest way to optimize the frequency compensation of the LT1103/LT1105 is to use transient response techniques and an "R-C" box to quickly iterate toward the final compensation network. Additional information on this technique of frequency compensation can be found in Linear Technology's Application Note 19.

In general, frequency compensation is accomplished with an R-C series network on the V_C pin. The error amplifier has a Gm (voltage "in" to current "out") of ≈ 12000 µmhos. Voltage gain is determined by multiplying Gm times the total equivalent error amplifier output loading, consisting of the error amplifier output impedance in parallel with the series R-C external frequency compensation network. At DC, the external R-C can be ignored. The output impedance of the error amplifier is typically 100kΩ resulting in a voltage gain of ≈ 1200. At frequencies just above DC, the voltage gain is determined by the external compensation, R_C and C_C. The gain at mid frequencies is given by:

$$A_V = \frac{Gm}{2\pi \bullet f \bullet C_C}$$

The gain at high frequencies is given by:

$$A_V = Gm \bullet R_C$$

Phase shift from the FB pin to the V_C pin is 90° at mid frequencies where the external C_C is controlling gain, then drops back to 0° (actually 180° since FB is an inverting input) when the reactance of C_C is small compared to R_C. Thus, this R-C series network forms a pole-zero pair. The pole is set by the high impedance output of the error amplifier and the value of C_C on the V_C pin. The zero is formed by the value of C_C and the value of R_C in series with C_C on the V_C pin. The R-C series network will have capacitor values in the range of 0.1µF – 1.0µF and series resistor values in the range of 100Ω – 1000Ω.

It is noted that the R-C network on the V_C pin forms the main compensation network for the regulator loop. However, if the load regulation compensation feature is used as explained in the section on fully-isolated flyback mode, additional frequency compensation components are required. The load regulation compensation feature involves the use of local positive feedback from the V_C pin to the FB pin. Thus, it is possible to add enough load regulation compensation to make the loop oscillate. In order to prevent oscillation, it is necessary to roll off this local positive feedback at high frequencies. This is accomplished by placing a capacitor in parallel with the compensation resistor which is in series with the FB pin. A value for this capacitor in the range of 0.01µF to 0.1µF is recommended. The time constant associated with this R/C combination will be longer than that associated with the loop bandwidth. Thus, transient response will be affected in that settling time will be increased. However, this is typically not as important as controlling the absolute under or overshoot amplitude of the system in response to load current changes which could cause deleterious system operation.

Switching Regulator Topologies

Two basic switching regulator topologies are pertinent to the LT1103/LT1105, the flyback and forward converter. The flyback converter employs a transformer to convert one voltage to either a higher or lower output voltage. V_{OUT} in *continuous mode* is defined as:

$$V_{OUT} = V_{IN} \bullet N \bullet \frac{DC}{(1-DC)}$$

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where N is the transformer turns ratio of secondary to primary and DC is the duty cycle. This formula can be rewritten in terms of duty cycle as:

$$DC = \frac{V_{OUT}}{\left(V_{OUT} + N \bullet V_{IN}\right)}$$

It is important to define the full range of input voltage, the range of output loading conditions and the regulation requirements for a design. Duty cycle should be calculated for both minimum and maximum input voltage.

In many applications, N can vary over a wide range without degrading performance. If maximum output power is desired, N can be optimized:

$$N_{(OPT)} = \frac{V_{OUT} + Vf}{\left(V_M - V_{IN(MAX)} - V_{SNUB}\right)}$$

where Vf = Forward voltage of the output diode

V_M = Maximum switch voltage

V_{SNUB} = Snubber clamp level – primary flyback voltage.

In the isolated flyback mode, the LT1103/LT1105 sense and regulate the transformer primary voltage V_{PRI} during "switch off" time. The secondary output voltage will be regulated if V_{PRI} is regulated. V_{PRI} is related to V_{OUT} by:

$$V_{PRI} = \frac{\left(V_{OUT} + Vf\right)}{N}$$

This allows duty cycle for an isolated flyback converter to be rewritten as:

$$DC = \text{Duty Cycle} = \frac{V_{PRI}}{\left(V_{PRI} + V_{IN}\right)}$$

An important transformer parameter to be determined is the primary inductance L_{PRI}. The value of this inductance is a trade-off between core size, regulation requirements, leakage inductance effects and magnetizing current ΔI. Magnetizing current is the difference between the primary current at the start of "switch on" time and the current at the end of "switch on" time. If maximum output power is needed, a reasonable starting value is found by assigning ΔI a value of 20% of the peak switch current (2A for the LT1103 and set by the external FET rating used with the LT1105). With this design approach, L_{PRI} is defined as:

$$L_{PRI} = \frac{V_{IN}}{(\Delta I)(f)\left(1 + \frac{V_{IN}}{V_{PRI}}\right)}$$

If maximum output power is not required, then ΔI can be increased which results in lower primary inductance and smaller magnetics. Maximum output power with an isolated flyback converter is defined by the primary flyback voltage and the peak allowed switch current and is limited to:

$$P_{OUT(MAX)} = \frac{\left(V_{PRI}\right)}{\left(V_{PRI} + V_{IN}\right)}\left[V_{IN}\left(I_P - \frac{\Delta I}{2}\right) - (I_P)^2 R\right]E$$

where R = Total "switch" ON resistance

I_P = Maximum switch current

E = Overall efficiency ≈ 75%

Peak primary current is used to determine core size for the transformer and is found from:

$$I_{PRI} = \frac{\left(V_{OUT}\right)\left(I_{OUT}\right)\left(V_{PRI} + V_{IN}\right)}{E\left(V_{PRI}\right)\left(V_{IN}\right)} + \frac{\Delta I}{2}$$

A second consideration on primary inductance is the transition point from continuous mode to discontinuous mode. At light loads, the flyback pulse across the primary will drop to zero before the end of switch "off" time. The load current at which this starts to occur can be calculated from:

$$I_{OUT(TRANSITION)} = \frac{\left(V_{PRI} \bullet V_{IN}\right)^2}{\left(V_{PRI} + V_{IN}\right)^2\left(2V_{OUT}\right)(f)\left(L_{PRI}\right)}$$

The forward converter as shown below is another transformer-based topology that converts one voltage to either a higher or a lower voltage.

V_{OUT} in *continuous mode* is defined as:

$$V_{OUT} = V_{IN} \bullet N \bullet DC$$

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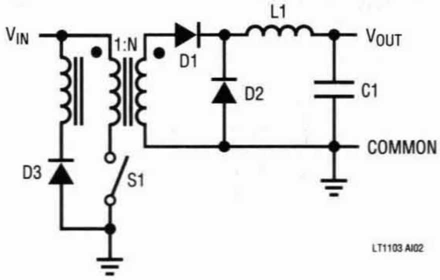
Simplified Forward Converter

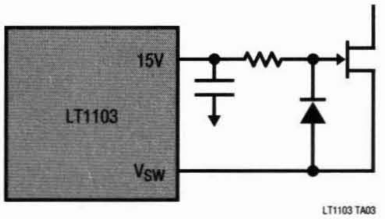

V_IN
1:N
D1
L1
V_OUT
D2
C1
COMMON
D3
S1
LT1103 AI02

The secondary voltage charges up L1 through D1 when S1 is on. When S1 is off, energy in L1 is transferred through free-wheeling diode D2 to C1. The extra transformer winding and diode D3 are needed in a single switch forward converter to define the switch voltage when S1 is off. This "reset" winding limits the maximum duty cycle allowed for the switch. This topology trades off reduced transformer size for increased complexity and parts count. A separate isolated feedback path is required for full isolation from input to output because voltages on the primary are no longer related to the DC output voltage during switch off time.

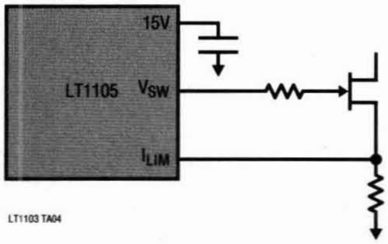
The isolated feedback path can take several forms. A second transformer in a modulator/demodulator scheme provides the isolation, but with significant complexity. An opto-isolator can be substituted for the transformer with a savings in volume to be traded off with component variations and possible aging problems with the opto-isolator transfer function. Finally, an extra winding closely coupled to the output inductor L1 can sense the flux in this element and give a representation of the output voltage when S1 is off.

TYPICAL APPLICATIONS

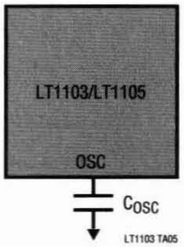
LT1103 FET Connection


15V
LT1103
V_SW
LT1103 TA03

LT1105 FET Connection


15V
LT1105
V_SW
I_LIM
LT1103 TA04

Setting Oscillator Frequency

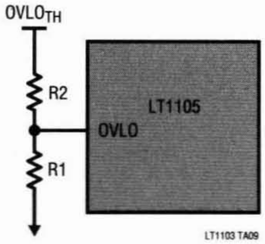

LT1103/LT1105
OSC
C_OSC
LT1103 TA05

CHOOSE $20\text{kHz} \le F_{OSC} \le 200\text{kHz}$

$$C_{OSC} = \frac{SF}{F_{OSC}} = \frac{I}{(\Delta V)(F_{OSC})} = \frac{100\mu A}{(2.5V)(F_{OSC})}$$

$DC \cong 0.66 \Rightarrow 66\%$

Setting Overvoltage Lockout


OVLO_TH
R2
R1
LT1105
OVLO
LT1103 TA09

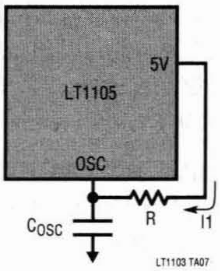
CHOOSE $OVLO_{TH}$

LET R1 = 5k

$$R2 = \left(\frac{OVLO_{TH}}{2.5V} - 1\right) R1$$

TYPICAL APPLICATIONS

Decreasing Oscillator Maximum Duty Cycle


LT1105
5V
OSC
C_{OSC}
R
I1
LT1103 TA07

CHOOSE $0 \le DC \le 0.66$

SOLVE FOR $X \Rightarrow X = \dfrac{(6 - 9DC)}{2}$

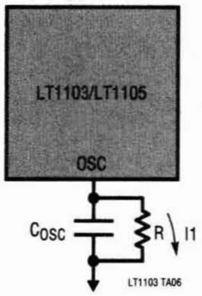
$0 \le X \le 3$

$\Rightarrow I1 = X \bullet I = X \bullet 100\mu A$

$\Rightarrow R = \dfrac{1.75V}{I1}$

$$C_{OSC} = \frac{100\mu A}{(2.5V)(F_{OSC})} \bullet \left[1 + \frac{(3X - 2X^2)}{9}\right]$$

Increasing Oscillator Maximum Duty Cycle


LT1103/LT1105
OSC
C_{OSC}
R
I1
LT1103 TA06

CHOOSE $0.66 \le DC \le 1.0$

SOLVE FOR $X \Rightarrow X = \dfrac{(9DC - 6)}{2}$

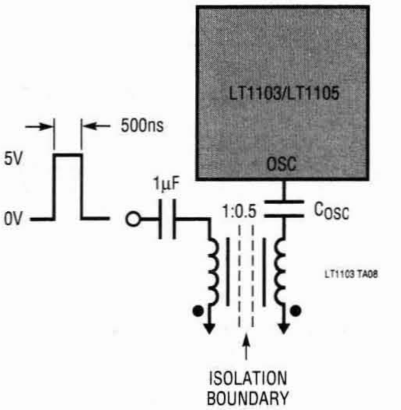
$0 \le X \le 1.5$

$\Rightarrow I1 = X \bullet I = X \bullet 100\mu A$

$\Rightarrow R = \dfrac{3.25V}{I1}$

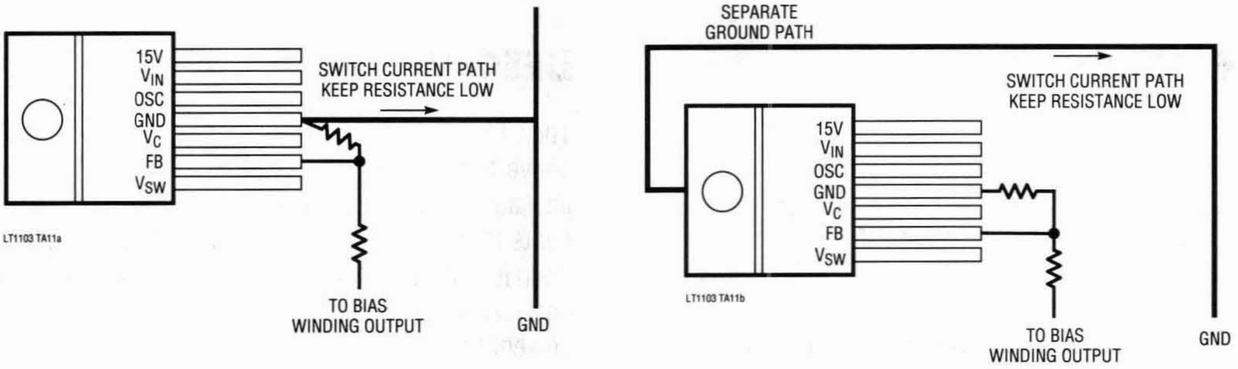
$$C_{OSC} = \frac{100\mu A}{(2.5V)(F_{OSC})} \bullet \left[1 - \frac{(3X + 2X^2)}{9}\right]$$

Synchronizing Oscillator Frequency to an External Clock

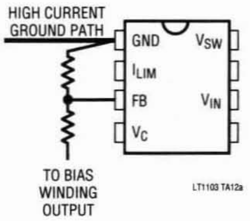

LT1103/LT1105
OSC
500ns
5V
0V
1µF
1:0.5
C_{OSC}
LT1103 TA08
ISOLATION
BOUNDARY

TYPICAL APPLICATIONS

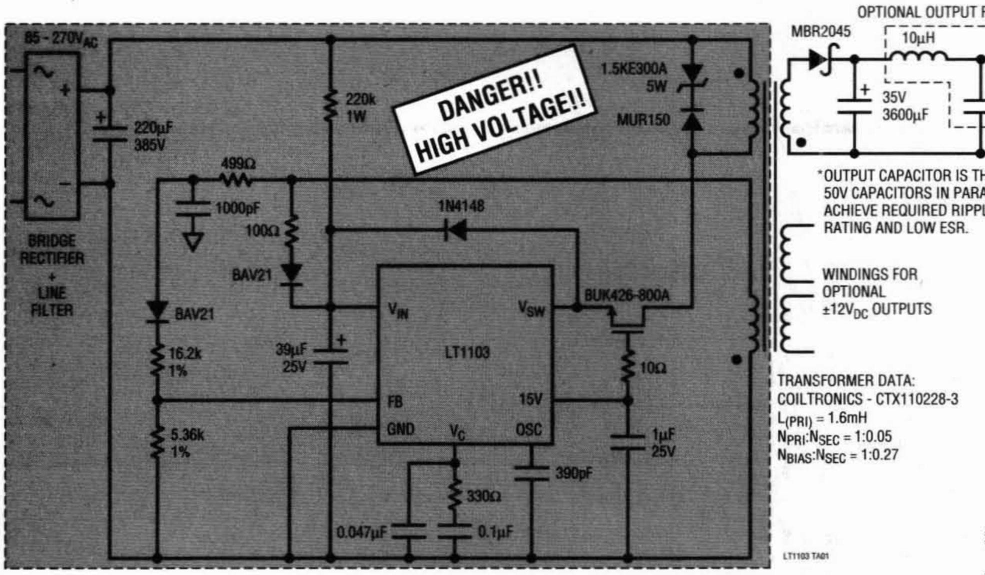
LT1103 Ground Connections


15V
V_{IN}
OSC
GND
V_C
FB
V_{SW}
SWITCH CURRENT PATH
KEEP RESISTANCE LOW
TO BIAS
WINDING OUTPUT
GND
LT1103 TA11a
SEPARATE
GROUND PATH
SWITCH CURRENT PATH
KEEP RESISTANCE LOW
LT1103 TA11b
TO BIAS
WINDING OUTPUT
GND

1105 Ground Connections


HIGH CURRENT
GROUND PATH
GND
V_{SW}
I_{LIM}
FB
V_{IN}
V_C
TO BIAS
WINDING
OUTPUT
LT1103 TA12a

Minimum Parts Count Fully-Isolated Flyback 100kHz 50W Converter


85 - 270V_{AC}
BRIDGE
RECTIFIER
+
LINE
FILTER
220µF
385V
220k
1W
DANGER!!
HIGH VOLTAGE!!
1.5KE300A
5W
MUR150
499Ω
1000pF
100Ω
BAV21
1N4148
BAV21
16.2k
1%
5.36k
1%
39µF
25V
V_{IN}
V_{SW}
LT1103
FB
GND
V_C
15V
OSC
BUK426-800A
10Ω
1µF
25V
390pF
330Ω
0.047µF
0.1µF
LT1103 TA01
OPTIONAL OUTPUT FILTER
MBR2045
10µH
5V
10A
35V
3600µF
50V
470µF

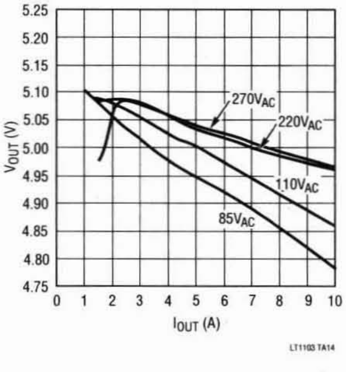
*OUTPUT CAPACITOR IS THREE 1200µF, 50V CAPACITORS IN PARALLEL TO ACHIEVE REQUIRED RIPPLE CURRENT RATING AND LOW ESR.

WINDINGS FOR OPTIONAL ±12V_{DC} OUTPUTS

TRANSFORMER DATA:
COILTRONICS - CTX110228-3
$L_{(PRI)}$ = 1.6mH
$N_{PRI}:N_{SEC}$ = 1:0.05
$N_{BIAS}:N_{SEC}$ = 1:0.27

Danger!! Lethal Voltages Present – See Text

Load Regulation



LT1109

Micropower Low Cost
DC-to-DC Converter
Fixed 5V, 12V

FEATURES

- Uses Off-the-Shelf Inductors
- Only 33µH Inductor Required
- Low Cost
- 3-Lead TO-92, SO8, or 8-Pin DIP
- Fixed 5V or 12V Output
- 120kHz Oscillator
- Only Three External Components Required
- 320µA I_Q
- 1.6V Minimum Start-Up Voltage
- Logic Controlled Shutdown

APPLICATIONS

- Flash Memory Vpp Generators
- 3V to 5V Converters
- 5V to 12V Converters
- Disk Drives
- PC Plug-In Cards
- Peripherals
- Battery Powered Equipment

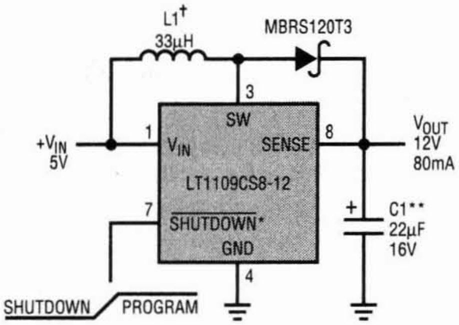
DESCRIPTION

The LT1109-5 and LT1109-12 are simple step-up DC-DC converters. Available in 3-lead TO-92, 8-pin SO or miniDIP packages, the devices require only three external components to construct a complete DC-DC converter. Current drain is just 320µA at no load, making the device ideal for cost-sensitive applications where standby current must be kept to a minimum.

The LT1109-5 can deliver 5V at 100mA from a 3V input and the LT1109-12 can deliver 12V at 60mA from a 5V input. The 8-pin versions also feature a logic controlled $\overline{\text{SHUTDOWN}}$ pin that turns off the oscillator when taken low. The gated-oscillator design requires no frequency compensation components. The high frequency 120kHz oscillator permits the use of small surface mount inductors and capacitors. For a 5V to 12V at 120mA converter, see the LT1109A.

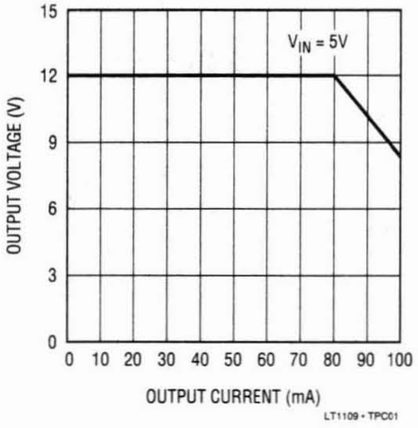
TYPICAL APPLICATION

All Surface Mount Flash Memory Vpp Generator

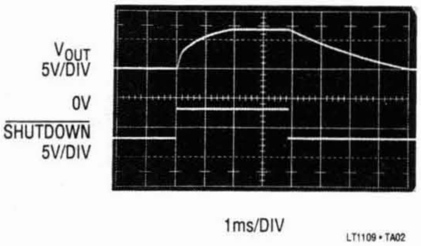


* 8-PIN PACKAGE ONLY
† L1 = SUMIDA CD54-330LC (I_{OUT} = 80mA)
MURATA-ERIE LQH4N330K (I_{OUT} = 50mA)
ISI LCS2414-330K (I_{OUT} = 50mA)
**C1 = MATSUO 267M1602226 OR EQUIVALENT

Output Current



Flash Memory Program Output

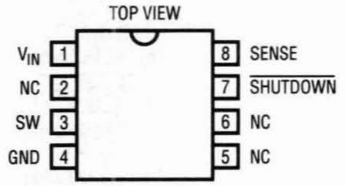


ABSOLUTE MAXIMUM RATINGS

(Voltages Referred to GND Pin)

Supply Voltage (V_{OUT})	–0.4 to 20V
SW Pin Voltage	–0.4 to 50V
$\overline{\text{SHUTDOWN}}$ Pin Voltage	6.0V
Maximum Power Dissipation	300mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Switch Current	1.2A

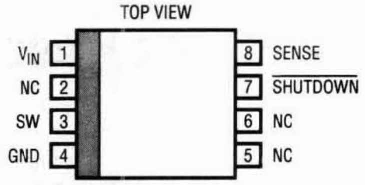
PACKAGE/ORDER INFORMATION


TOP VIEW
VIN 1
NC 2
SW 3
GND 4
8 SENSE
7 SHUTDOWN
6 NC
5 NC
LT1109 • POI02

N8 PACKAGE
8-LEAD PLASTIC DIP

ORDER PART NUMBER

LT1109CN8-5
LT1109CN8-12

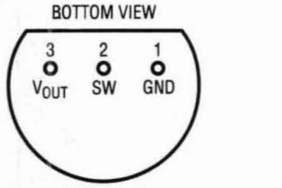

TOP VIEW
VIN 1
NC 2
SW 3
GND 4
8 SENSE
7 SHUTDOWN
6 NC
5 NC
LT1109 • POI03

S8 PACKAGE
8-LEAD PLASTIC SOIC

LT1109CS8-5
LT1109CS8-12

S8 PART MARKING

10905
10912


BOTTOM VIEW
3
2
1
VOUT
SW
GND
LT1109 • POI01

Z PACKAGE
3-LEAD TO-92 PLASTIC

LT1109CZ-5
LT1109CZ-12

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 3V (LT1109CN8, LT1109CS8), unless otherwise specified.

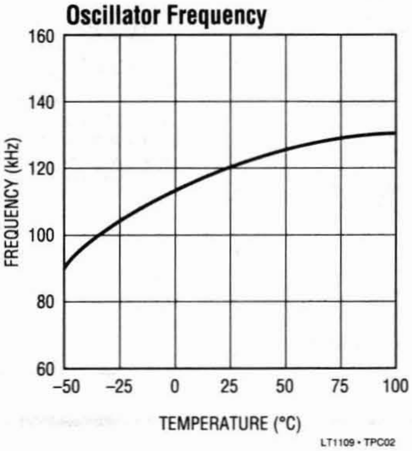
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off	●		320	550	µA
	Minimum Start-Up Voltage at V_{OUT} Pin (Z Package)			1.6			V
V_{IN}	Input Voltage (N8, S8 Package)		●	3			V
V_{OUT}	Output Voltage	LT1109-5; 3V ≤ V_{IN} ≤ 5V	●	4.75	5.00	5.25	V
		LT1109-12; 3V ≤ V_{IN} ≤ 12V	●	11.45	12.00	12.55	
	Output Voltage Ripple	LT1109-5	●		25	50	mV
		LT1109-12	●		60	120	
f_{OSC}	Oscillator Frequency			100	120	140	kHz
			●	90		150	
t_{ON}	Switch ON Time			3.3	4.2	5.3	µs
			●	3.0		5.5	
DC	Duty Cycle	Full Load	●	45	50	60	%
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 500mA			0.4	0.7	V
		LT1109-5: V_{IN} = 3V; LT1109-12: V_{IN} = 5V	●		0.5	0.8	
	Switch Leakage Current	V_{SW} = 12V			1	10	µA

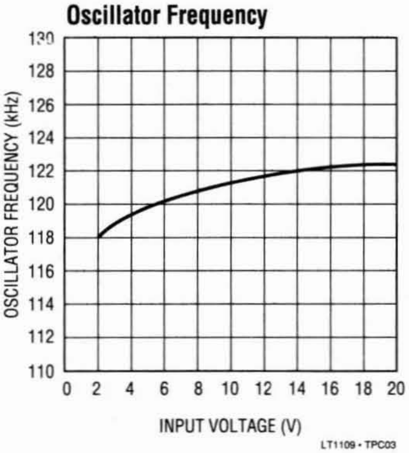
ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 3V$ (LT1109CN8, LT1109CS8), unless otherwise specified.

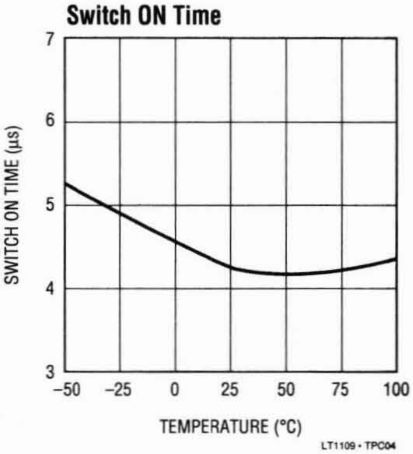
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	$\overline{\text{SHUTDOWN}}$ Pin High	N8, S8 Package	●	2.0			V
V_{IL}	$\overline{\text{SHUTDOWN}}$ Pin Low	N8, S8 Package	●			0.8	V
I_{IH}	$\overline{\text{SHUTDOWN}}$ Pin Input Current	N8, S8 Package, $V_{\overline{SHUTDOWN}} = 4V$	●			10	μA
I_L		N8, S8 Package, $V_{\overline{SHUTDOWN}} = 0V$	●			20	μA

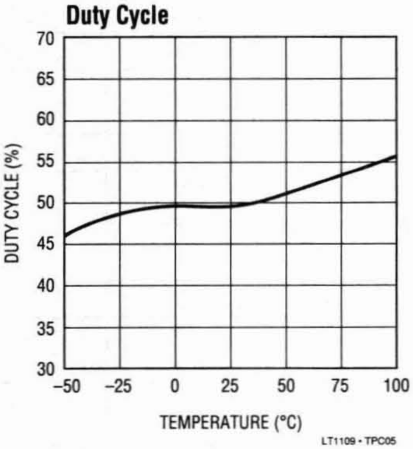
The ● denotes the specifications which apply over the full operating temperature range.

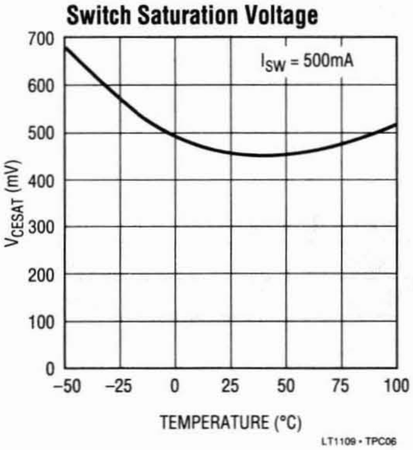
TYPICAL PERFORMANCE CHARACTERISTICS

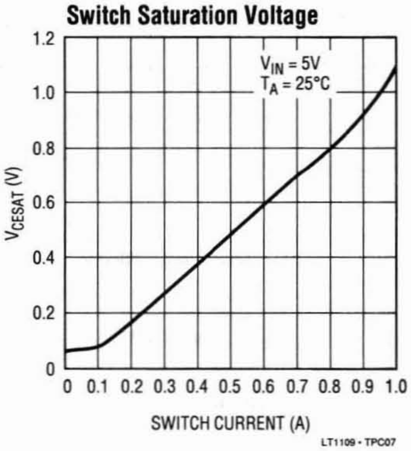

Oscillator Frequency


Oscillator Frequency

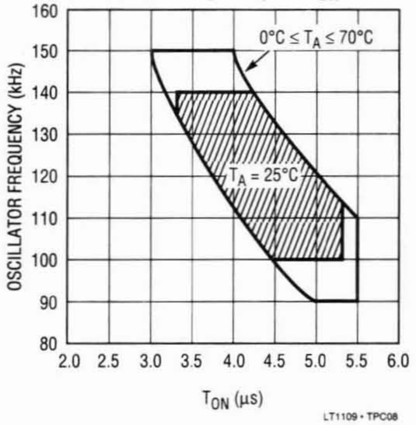

Switch ON Time

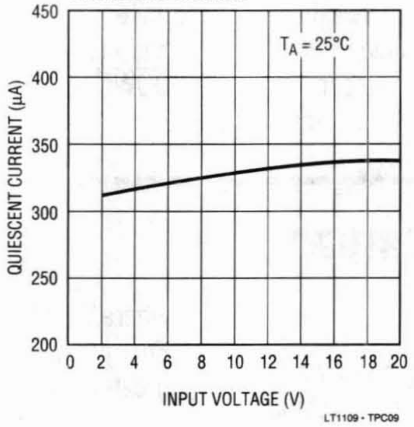

Duty Cycle

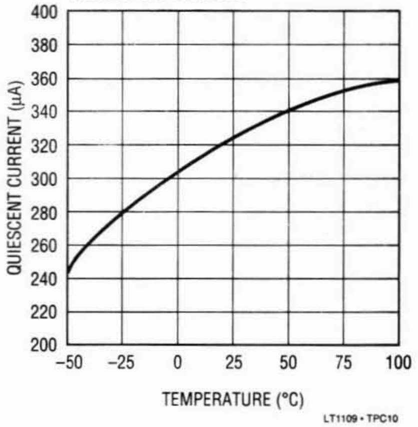

Switch Saturation Voltage


Switch Saturation Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

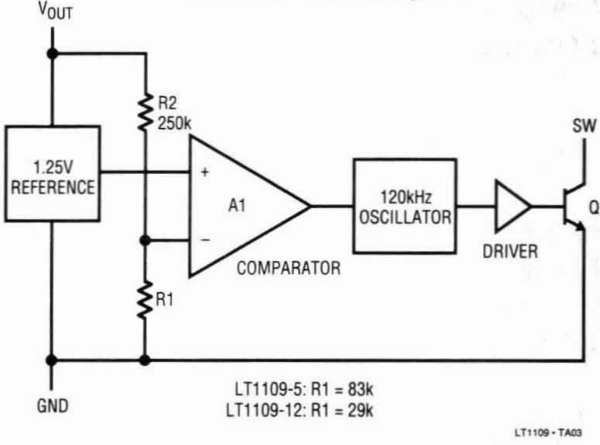

Minimum/Maximum Oscillator Frequency vs T_{ON}


Quiescent Current

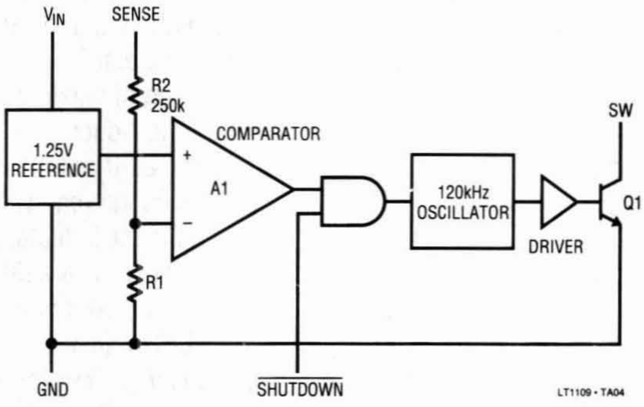

Quiescent Current

BLOCK DIAGRAMS

LT1109-5, -12 Z Package


V_OUT
R2
250k
1.25V
REFERENCE
+
A1
−
COMPARATOR
120kHz
OSCILLATOR
DRIVER
SW
Q1
R1
GND
LT1109-5: R1 = 83k
LT1109-12: R1 = 29k
LT1109 • TA03

LT1109-5, -12 N8, S8 Package


V_IN
SENSE
R2
250k
1.25V
REFERENCE
COMPARATOR
+
A1
−
120kHz
OSCILLATOR
DRIVER
SW
Q1
R1
GND
SHUTDOWN
LT1109 • TA04

LT1109Z OPERATION

The LT1109Z-5 and LT1109Z-12 are fixed output voltage step-up DC-to-DC converters in a 3-pin TO-92 package. Power for internal regulator circuitry is taken from the V_{OUT} pin, a technique known as "bootstrapping." Circuit operation can be best understood by referring to the block diagram. V_{OUT}, attenuated by R1 and R2, is applied to the negative input of comparator A1. When this voltage falls below the 1.25V reference voltage, the oscillator is turned on and the power switch Q1 cycles at the oscillator frequency of 120kHz. Switch cycling alternately builds current in the inductor, then dumps it into the output capacitor, increasing the output voltage. When A1's negative input rises above 1.25V, it turns off the oscillator. A small amount of hysteresis in A1 obviates the need for frequency compensation circuitry. When Q1 is off, current into the V_{OUT} pin drops to just 320µA. Quiescent current from the battery will be higher because the device operates off the *stepped-up* voltage.

LT1109 S8 AND N8 OPERATION

The 8-pin versions of the LT1109 have separate pins for V_{IN} and SENSE and also have a $\overline{\text{SHUTDOWN}}$ pin. Separating the device V_{IN} pin from the SENSE pin allows the device to be powered from the (lower) input voltage rather than the (higher) output voltage. Although quiescent *current* remains constant, quiescent *power* will be reduced by using the 8-pin version since the quiescent current flows from a lower voltage source. The $\overline{\text{SHUTDOWN}}$ pin disables the oscillator when taken to a logic "0." If left floating or tied high, the converter operates normally. With $\overline{\text{SHUTDOWN}}$ low, quiescent current remains at 320μA.

APPLICATIONS INFORMATION

Inductor Selection

A DC-DC converter operates by storing energy as magnetic flux in an inductor core, and then switching this energy into the load. To operate as an efficient energy transfer element, the inductor must fulfill three requirements. First, the inductance must be low enough for the inductor to store adequate energy under the worst case condition of minimum input voltage and switch ON time. The inductance must also be high enough so that maximum current ratings of the LT1109 and inductor are not exceeded at the other worst case condition of maximum input voltage and ON time. Additionally, the inductor core must be able to store the required flux; i.e., it must not *saturate*. At power levels generally encountered with LT1109 designs, small ferrite surface-mount inductors will function well. Lastly, the inductor must have sufficiently low DC resistance so that excessive power is not lost as heat in the windings. Look for DCR values in the inductors' specification tables; values under 0.5Ω will give best efficiency. An additional consideration is Electro-Magnetic Interference (EMI). Toroid and pot core type inductors are recommended in applications where EMI must be kept to a minimum; for example, where there are sensitive analog circuitry or transducers nearby. Rod core types are a less expensive choice where EMI is not a problem.

Specifying a proper inductor for an application requires first establishing minimum and maximum input voltage, output voltage, and output current. In a step-up converter, the inductive events add to the input voltage to produce the output voltage. Power required from the inductor is determined by

$$P_L = (V_{OUT} + V_D - V_{IN})(I_{OUT}) \qquad (01)$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky). Energy required by the inductor per cycle must be equal or greater than

$$\frac{P_L}{F_{OSC}} \qquad (02)$$

in order for the converter to regulate the output.

When the switch is closed, current in the inductor builds according to

$$I_L(t) = \frac{V_{IN}}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \qquad (03)$$

where R' is the sum of the switch equivalent resistance (0.8 typical at 25°C) and the inductor DC resistance. When the drop across the switch is small compared to V_{IN}, the simple lossless equation

$$I_L(t) = \frac{V_{IN}}{L}t \qquad (04)$$

can be used. These equations assume that at t = 0, inductor current is zero. This situation is called "discontinuous mode operation" in switching regulator parlance. Setting "t" to the switch ON time from the LT1109 specification table (typically 4.2μs) will yield I_{PEAK} for a specific "L" and V_{IN}. Once I_{PEAK} is known, energy in the inductor at the end of the switch ON time can be calculated as

$$E_L = \frac{1}{2}LI^2_{PEAK} \qquad (05)$$

E_L must be greater than P_L/F_{OSC} for the converter to deliver the required power. For best efficiency I_{PEAK} should be

APPLICATIONS INFORMATION

kept to 600mA or less. Higher switch currents will cause excessive drop across the switch resulting in reduced efficiency. In general, switch current should be held to as low a value as possible in order to keep switch, diode and inductor losses at a minimum.

As an example, suppose 12V at 60mA is to be generated from a 4.5V input. Recalling Equation 01,

$$P_L = (12V + 0.5V - 4.5V)\ (60mA) = 480mW. \qquad (06)$$

Energy required from the inductor is

$$\frac{P_L}{F_{OSC}} = \frac{480mW}{120kHz} = 4.0\mu J. \qquad (07)$$

Picking an inductor value of 33µH with 0.2Ω DCR results in a peak switch current of

$$I_{PEAK} = \frac{4.5V}{1.0\Omega}\left(1 - e^{\frac{-1.0 \bullet 4.2\mu s}{33\mu H}}\right) = 538mA. \qquad (08)$$

Substituting I_{PEAK} into Equation 03 results in

$$E_L = \frac{1}{2}(33\mu H)(0.538A)^2 = 4.77\mu J. \qquad (09)$$

Since 4.77µJ > 4µJ the 33µH inductor will work. This trial-and-error approach can be used to select the optimum inductor. Keep in mind the switch current maximum rating of 1.2A. If the calculated peak current exceeds this, the input voltage must be increased or the load decreased.

Capacitor Selection

The output capacitor should be chosen on the basis of its equivalent series resistance (ESR). Surface-mount tantalum electrolytics can be used provided the ESR value is sufficiently low. An ESR of 0.1Ω will result in a 50mV step at the output of the converter when the peak inductor current is 500mA. Physically larger capacitors have lower ESR.

Diode Selection

Speed, forward drop, and leakage current are the three main considerations in selecting a catch diode for LT1109 converters. General purpose rectifiers such as the 1N4001 are *unsuitable* for use in *any* switching regulator application. Although they are rated at 1A, the switching time of a 1N4001 is in the 10µs-50µs range. At best, efficiency will be severely compromised when these diodes are used; at worst, the circuit may not work at all. Most LT1109 circuits will be well served by a 1N5818 Schottky diode. The combination of 500mV forward drop at 1A current, fast turn ON and turn OFF time, and 4µA to 10µA leakage current fit nicely with LT1109 requirements. At peak switch currents of 100mA or less, a 1N4148 signal diode may be used. This diode has leakage current in the 1nA-5nA range at 25°C and lower cost than a 1N5818.

Table 1. Inductor Manufacturers

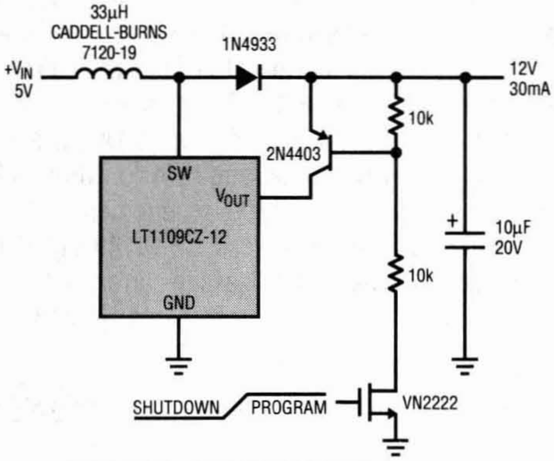
MANUFACTURER	PART NUMBERS
Caddell-Burns 258 East Second Street Mineola, NY 11501 516-746-2310	7120 Series
Coiltronics International 984 S.W. 13th Court Pompano Beach, FL 33069 305-781-8900	Surface Mount CTX-100 Series
Toko America Incorporated 1250 Feehanville Drive Mount Prospect, IL 60056 312-297-0070	Type 8RBS
Sumida Electric Co., Ltd. 637 E. Golf Road, Suite 209 Arlington Heights, IL 60005 708-956-0666	CD54 CD105 Surface Mount

Table 2. Capacitor Manufacturers

MANUFACTURER	PART NUMBERS
Sanyo Video Components 1201 Sanyo Avenue San Diego, CA 92073 619-661-6322	OS-CON Series
Matsuo Electronics 2134 Main Street, Suite 200 Huntington Beach, CA 92648 714-969-2491	267 Series
Kemet Electronics Corporation Box 5928 Greenville, SC 29606 803-963-6621	T491 Series
Philips Components 2001 W. Blue Heron Blvd. P.O. Box 10330 Riviera Beach, FL 33404 407-881-3200	49MC Series

TYPICAL APPLICATIONS

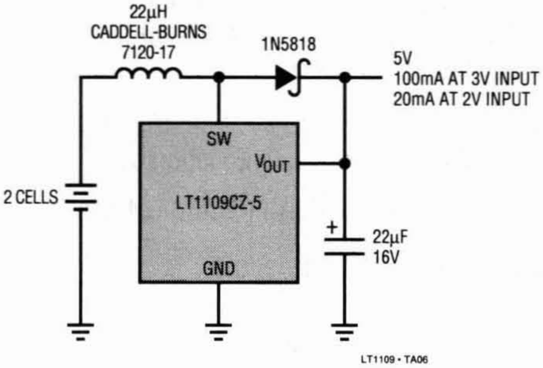
3-Pin Package Flash Memory Vpp Generator


33µH
CADDELL-BURNS
7120-19
1N4933
+V_{IN} 5V
12V
30mA
10k
2N4403
SW
V_{OUT}
LT1109CZ-12
GND
10µF
20V
10k
SHUTDOWN / PROGRAM
VN2222

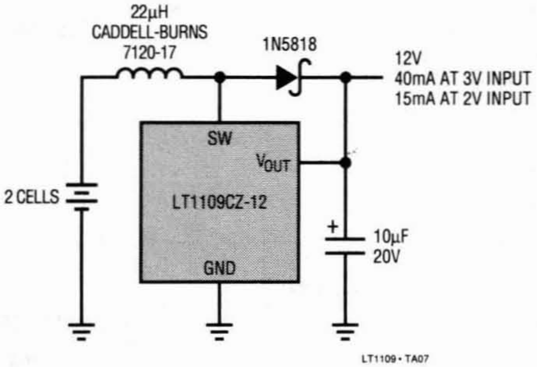
QUIESCENT CURRENT = 0 IN SHUTDOWN

LT1109 • TA05

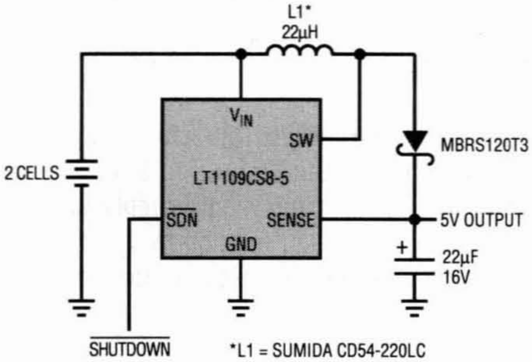
3V to 5V Converter


22µH
CADDELL-BURNS
7120-17
1N5818
5V
100mA AT 3V INPUT
20mA AT 2V INPUT
SW
V_{OUT}
2 CELLS
LT1109CZ-5
22µF
16V
GND
LT1109 • TA06

3V to 12V Converter


22µH
CADDELL-BURNS
7120-17
1N5818
12V
40mA AT 3V INPUT
15mA AT 2V INPUT
SW
V_{OUT}
2 CELLS
LT1109CZ-12
10µF
20V
GND
LT1109 • TA07

3V to 5V Converter with Shutdown


L1*
22µH
V_{IN}
SW
MBRS120T3
2 CELLS
LT1109CS8-5
SDN
SENSE
5V OUTPUT
GND
22µF
16V
SHUTDOWN

*L1 = SUMIDA CD54-220LC

LT1109 • TA08

LT1110

Micropower DC-DC Converter Adjustable and Fixed 5V, 12V

FEATURES

- Operates at Supply Voltages From 1.0V to 30V
- Works in Step-Up or Step-Down Mode
- Only Three External Off-the-Shelf Components Required
- Low-Battery Detector Comparator On-Chip
- User-Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space-Saving 8-Pin MiniDIP or S8 Package

APPLICATIONS

- Pagers
- Cameras
- Single-Cell to 5V Converters
- Battery Backup Supplies
- Laptop and Palmtop Computers
- Cellular Telephones
- Portable Instruments
- Laser Diode Drivers
- Hand-Held Inventory Computers

DESCRIPTION

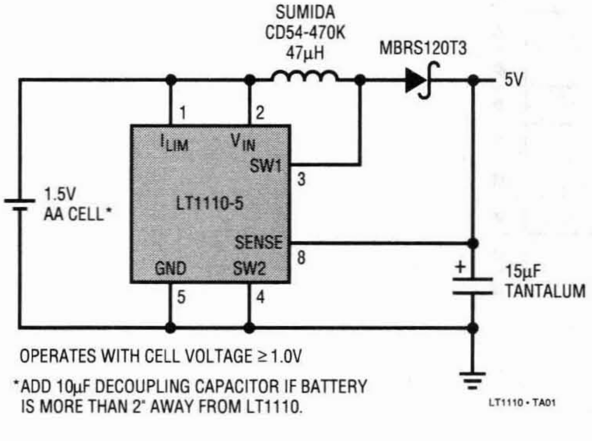
The LT1110 is a versatile micropower DC-DC converter. The device requires only three external components to deliver a fixed output of 5V or 12V. The very low minimum supply voltage of 1.0V allows the use of the LT1110 in applications where the primary power source is a single cell. An on-chip auxiliary gain block can function as a low battery detector or linear post regulator.

The 70kHz oscillator allows the use of surface mount inductors and capacitors in many applications. Quiescent current is just 300µA, making the device ideal in remote or battery powered applications where current consumption must be kept to a minimum.

The device can easily be configured as a step-up or step-down converter, although for most step-down applications or input sources greater than 3V, the LT1111 is recommended. Switch current limiting is user-adjustable by adding a single external resistor. Unique reverse battery protection circuitry limits reverse current to safe, non-destructive levels at reverse supply voltages up to 1.6V.

TYPICAL APPLICATION

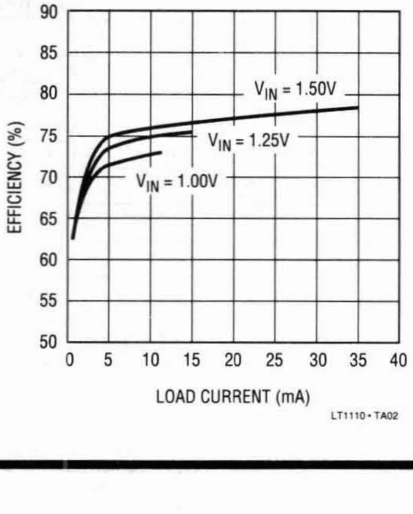
All Surface Mount Single Cell to 5V Converter



OPERATES WITH CELL VOLTAGE ≥ 1.0V

*ADD 10µF DECOUPLING CAPACITOR IF BATTERY IS MORE THAN 2" AWAY FROM LT1110.

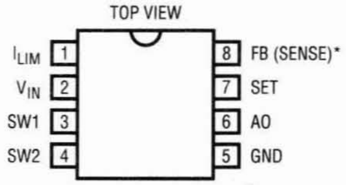
Efficiency



ABSOLUTE MAXIMUM RATINGS

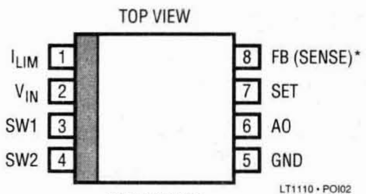
Supply Voltage, Step-Up Mode	15V
Supply Voltage, Step-Down Mode	36V
SW1 Pin Voltage	50V
SW2 Pin Voltage	−0.5V to V_{IN}
Feedback Pin Voltage (LT1110)	5.5V
Switch Current	1.5A
Maximum Power Dissipation	500mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
*FIXED VERSIONS

LT1110 • POI01



LT1110 • POI02

S8 PACKAGE
8-LEAD PLASTIC SOIC
*FIXED VERSIONS

ORDER PART NUMBER
LT1110CN8 LT1110CN8-5 LT1110CN8-12
LT1110CS8 LT1110CS8-5 LT1110CS8-12

S8 PART MARKING
1110 11005 11012

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 1.5V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off	●		300		µA
V_{IN}	Input Voltage	Step-Up Mode	●	1.15		12.6	V
				1.0		12.6	V
		Step-Down Mode	●			30	V
	Comparator Trip Point Voltage	LT1110 (Note 1)	●	210	220	230	mV
V_{OUT}	Output Sense Voltage	LT1110-5 (Note 2)	●	4.75	5.00	5.25	V
		LT1110-12 (Note 2)	●	11.4	12.00	12.6	V
	Comparator Hysteresis	LT1110	●		4	8	mV
	Output Hysteresis	LT1110-5	●		90	180	mV
		LT1110-12	●		200	400	mV
f_{OSC}	Oscillator Frequency		●	52	70	90	kHz
DC	Duty Cycle	Full Load ($V_{FB} < V_{REF}$)	●	62	69	78	%
t_{ON}	Switch ON Time		●	7.5	10	12.5	µs
I_{FB}	Feedback Pin Bias Current	LT1110, $V_{FB} = 0V$	●		70	150	nA
I_{SET}	Set Pin Bias Current	$V_{SET} = V_{REF}$	●		100	300	nA
V_{AO}	AO Output Low	$I_{AO} = -300µA$, $V_{SET} = 150mV$	●		0.15	0.4	V
	Reference Line Regulation	$1.0V \le V_{IN} \le 1.5V$	●		0.35	1.0	%/V
		$1.5V \le V_{IN} \le 12V$	●		0.05	0.1	%/V

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 1.5V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CESAT}	Switch Saturation Voltage Step-Up Mode	$V_{IN} = 1.5V$, $I_{SW} = 400mA$			300	400	mV
			●			600	mV
		$V_{IN} = 1.5V$, $I_{SW} = 500mA$			400	550	mV
			●			750	mV
		$V_{IN} = 5V$, $I_{SW} = 1A$			700	1000	mV
A_V	A2 Error Amp Gain	$R_L = 100k\Omega$ (Note 3)	●	1000	5000		V/V
I_{REV}	Reverse Battery Current	(Note 4)			750		mA
I_{LIM}	Current Limit	220Ω Between I_{LIM} and V_{IN}			400		mA
	Current Limit Temperature Coefficient				−0.3		%/°C
I_{LEAK}	Switch OFF Leakage Current	Measured at SW1 Pin			1	10	μA
V_{SW2}	Maximum Excursion Below GND	$I_{SW1} \leq 10\mu A$, Switch Off			−400	−350	mV

The ● denotes the specifications which apply over the full operating temperature range.

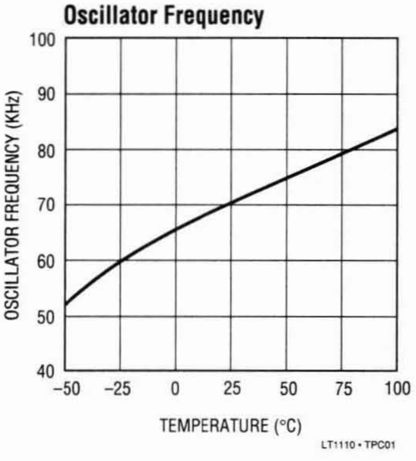
Note 1: This specification guarantees that both the high and low trip point of the comparator fall within the 210mV to 230mV range.

Note 2: This specification guarantees that the output voltage of the fixed versions will always fall within the specified range. The waveform at the sense pin will exhibit a sawtooth shape due to the comparator hysteresis.

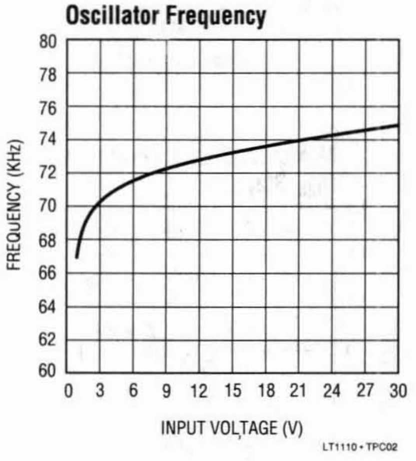
Note 3: 100kΩ resistor connected between a 5V source and the AO pin.

Note 4: The LT1110 is guaranteed to withstand continuous application of +1.6V applied to the GND and SW2 pins while V_{IN}, I_{LIM}, and SW1 pins are grounded.

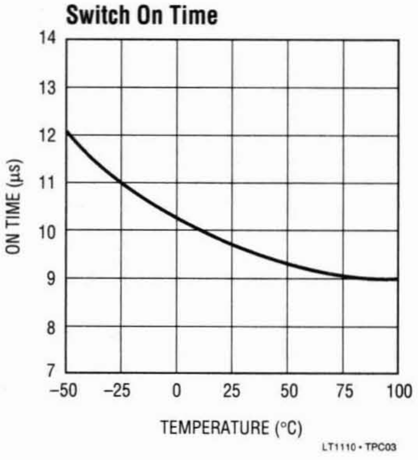
TYPICAL PERFORMANCE CHARACTERISTICS



Oscillator Frequency

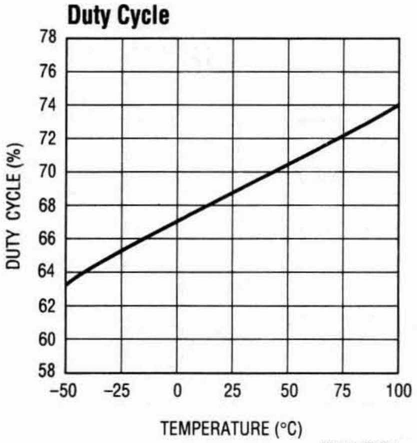


Oscillator Frequency

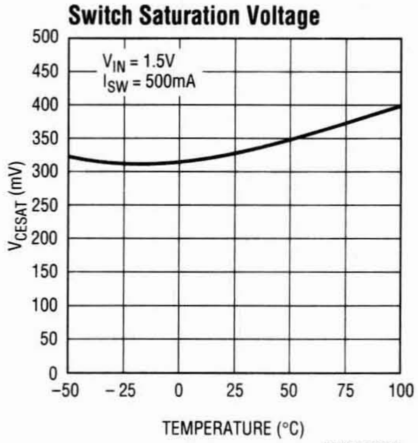


Switch On Time

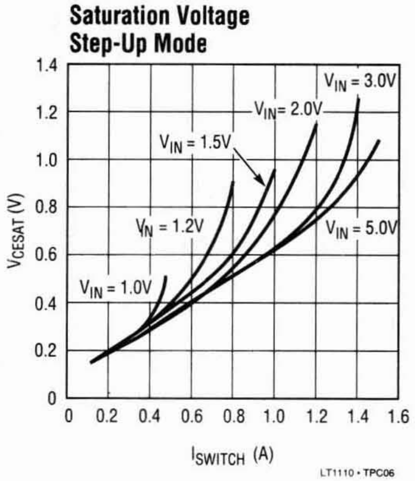
TYPICAL PERFORMANCE CHARACTERISTICS


Duty Cycle

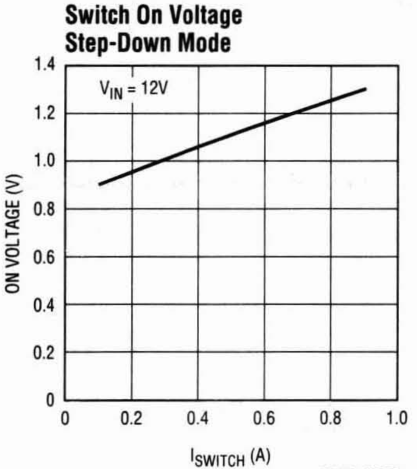
LT1110 • TPC04


Switch Saturation Voltage

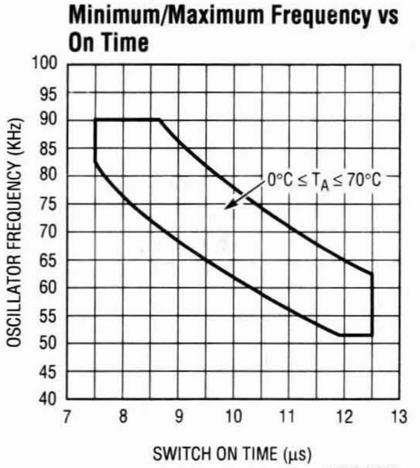
LT1110 • TPC05


Saturation Voltage Step-Up Mode

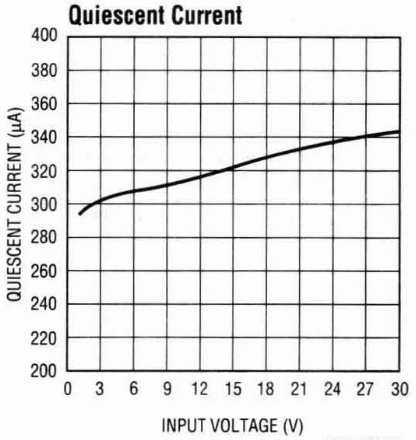
LT1110 • TPC06


Switch On Voltage Step-Down Mode

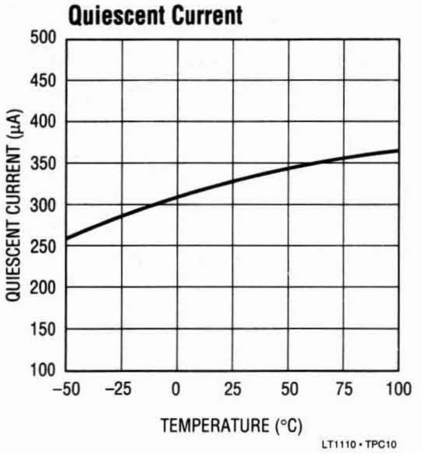
LT1110 • TPC07


Minimum/Maximum Frequency vs On Time

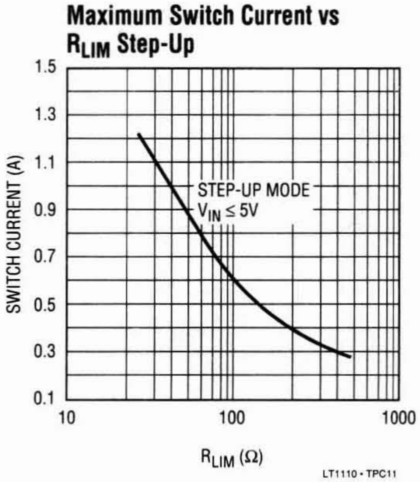
LT1110 • TPC08


Quiescent Current

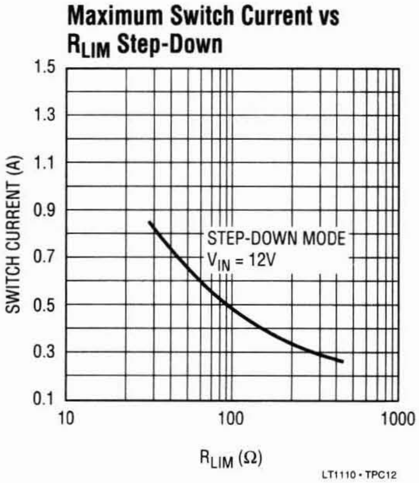
LT1110 • TPC09


Quiescent Current

LT1110 • TPC10


Maximum Switch Current vs R_{LIM} Step-Up

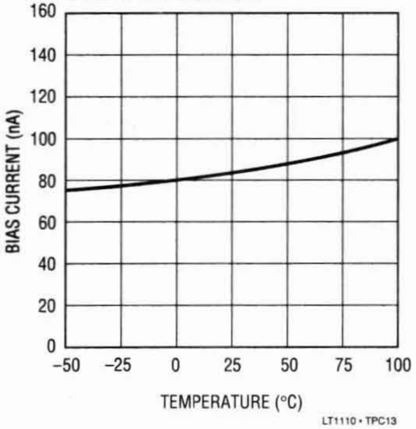
LT1110 • TPC11


Maximum Switch Current vs R_{LIM} Step-Down

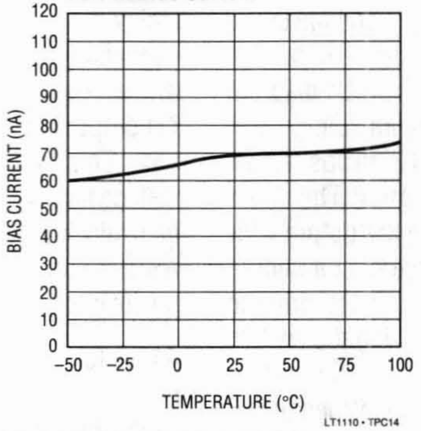
LT1110 • TPC12

TYPICAL PERFORMANCE CHARACTERISTICS

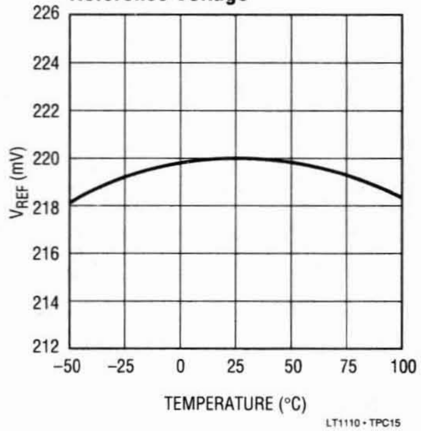
Set Pin Bias Current



FB Pin Bias Current



Reference Voltage



PIN FUNCTIONS

I_{LIM} (Pin 1): Connect this pin to V_{IN} for normal use. Where lower current limit is desired, connect a resistor between I_{LIM} and V_{IN}. A 220Ω resistor will limit the switch current to approximately 400mA.

V_{IN} (Pin 2): Input supply voltage.

SW1 (Pin 3): Collector of power transistor. For step-up mode connect to inductor/diode. For step-down mode connect to V_{IN}.

SW2 (Pin 4): Emitter of power transistor. For step-up mode connect to ground. For step-down mode connect to inductor/diode. This pin must never be allowed to go more than a Schottky diode drop below ground.

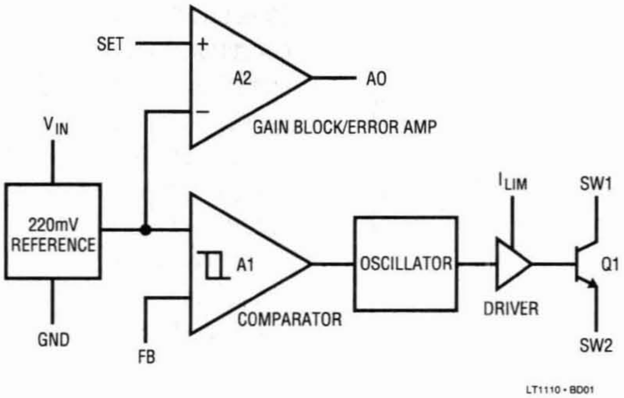
GND (Pin 5): Ground.

AO (Pin 6): Auxiliary Gain Block (GB) output. Open collector, can sink 300μA.

SET (Pin 7): GB input. GB is an op amp with positive input connected to SET pin and negative input connected to 220mV reference.

FB/SENSE (Pin 8): On the LT1110 (adjustable) this pin goes to the comparator input. On the LT1110-5 and LT1110-12, this pin goes to the internal application resistor that sets output voltage.

LT1110 BLOCK DIAGRAM



LT1110 OPERATION

The LT1110 is a gated oscillator switcher. This type architecture has very low supply current because the switch is cycled only when the feedback pin voltage drops below the reference voltage. Circuit operation can best be understood by referring to the LT1110 block diagram above. Comparator A1 compares the FB pin voltage with the 220mV reference signal. When FB drops below 220mV, A1 switches on the 70kHz oscillator. The driver amplifier boosts the signal level to drive the output NPN power switch Q1. An adaptive base drive circuit senses switch current and provides just enough base drive to ensure switch saturation without overdriving the switch, resulting in higher efficiency. The switch cycling action raises the output voltage and FB pin voltage. When the FB voltage is sufficient to trip A1, the oscillator is gated off. A small amount of hysteresis built into A1 ensures loop stability without external frequency compensation. When the comparator is low the oscillator and all high current circuitry is turned off, lowering device quiescent current to just 300μA for the reference, A1 and A2.

The oscillator is set internally for 10μs ON time and 5μs OFF time, optimizing the device for step-up circuits where $V_{OUT} \approx 3V_{IN}$, e.g., 1.5V to 5V. Other step-up ratios as well as step-down (buck) converters are possible at slight losses in maximum achievable power output.

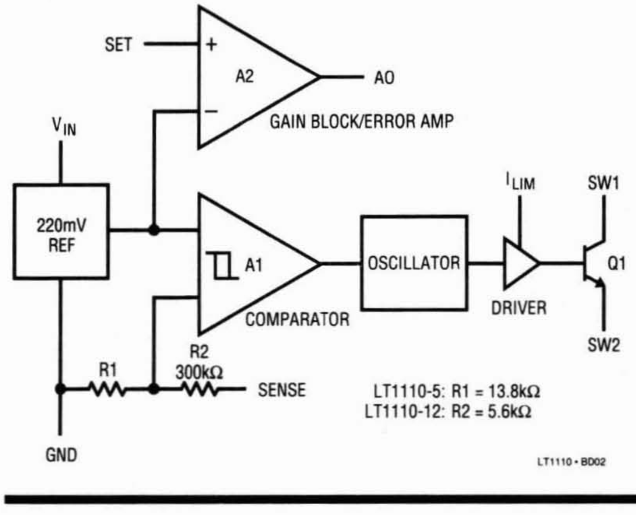
A2 is a versatile gain block that can serve as a low battery detector, a linear post regulator, or drive an under voltage lockout circuit. The negative input of A2 is internally connected to the 220mV reference. An external resistor divider from V_{IN} to GND provides the trip point for A2. The AO output can sink 300μA (use a 47k resistor pull up to +5V). This line can signal a microcontroller that the battery voltage has dropped below the preset level. To prevent the gain block from operating in its linear region, a 2MΩ resistor can be connected from AO to SET. This provides positive feedback.

A resistor connected between the I_{LIM} pin and V_{IN} adjusts maximum switch current. When the switch current exceeds the set value, the switch is turned off. This feature is especially useful when small inductance values are used with high input voltages. If the internal current limit of 1.5A is desired, I_{LIM} should be tied directly to V_{IN}. Propagation delay through the current limit circuitry is about 700ns.

In step-up mode, SW2 is connected to ground and SW1 drives the inductor. In step-down mode, SW1 is connected to V_{IN} and SW2 drives the inductor. Output voltage is set by the following equation in either step-up or step-down modes where R1 is connected from FB to GND and R2 is connected from V_{OUT} to FB.

$$V_{OUT} = (220\text{mV})\left(\frac{R2}{R1} + 1\right) \qquad (01)$$

LT1110-5, -12 BLOCK DIAGRAM



LT1110-5, -12 OPERATION

The LT1110-5 and LT1110-12 fixed output voltage versions have the gain setting resistors on-chip. Only three external components are required to construct a 5V or 12V output converter. 16μA flows through R1 and R2 in the LT1110-5, and 39μA flows in the LT1110-12. This current represents a load and the converter must cycle from time to time to maintain the proper output voltage. Output ripple, inherently present in gated oscillator designs, will typically run around 90mV for the LT1110-5 and 200mV for the LT1110-12 with the proper inductor/capacitor selection. This output ripple can be reduced considerably by using the gain block amp as a pre-amplifier in front of the FB pin. See the Applications section for details.

APPLICATIONS INFORMATION

Inductor Selection — General

A DC-DC converter operates by storing energy as magnetic flux in an inductor core, and then switching this energy into the load. Since it is flux, not charge, that is stored, the output voltage can be higher, lower, or opposite in polarity to the input voltage by choosing an appropriate switching topology. To operate as an efficient energy transfer element, the inductor must fulfill three requirements. First, the inductance must be low enough for the inductor to store adequate energy under the worst case condition of minimum input voltage and switch ON time. The inductance must also be high enough so maximum current ratings of the LT1110 and inductor are not exceeded at the other worst case condition of maximum input voltage and ON time. Additionally, the inductor core must be able to store the required flux; i.e., it must not *saturate*. At power levels generally encountered with LT1110 based designs, small surface mount ferrite core units with saturation current ratings in the 300mA to 1A range and DCR less than 0.4Ω (depending on application) are adequate. Lastly, the inductor must have sufficiently low DC resistance so excessive power is not lost as heat in the windings. An additional consideration is Electro-Magnetic Interference (EMI). Toroid and pot core type inductors are recommended in applications where EMI must be kept to a minimum; for example, where there are sensitive analog circuitry or transducers nearby. Rod core types are a less expensive choice where EMI is not a problem. Minimum and maximum input voltage, output voltage and output current must be established before an inductor can be selected.

Inductor Selection — Step-Up Converter

In a step-up, or boost converter (Figure 4), power generated by the inductor makes up the difference between input and output. Power required from the inductor is determined by

$$P_L = \left(V_{OUT} + V_D - V_{IN\,MIN}\right)\left(I_{OUT}\right) \qquad (01)$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky).

Energy required by the inductor per cycle must be equal or greater than

$$\frac{P_L}{f_{OSC}} \qquad (02)$$

in order for the converter to regulate the output.

When the switch is closed, current in the inductor builds according to

$$I_L(t) = \frac{V_{IN}}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \qquad (03)$$

where R' is the sum of the switch equivalent resistance (0.8Ω typical at 25°C) and the inductor DC resistance. When the drop across the switch is small compared to V_{IN}, the simple lossless equation

$$I_L(t) = \frac{V_{IN}}{L}t \qquad (04)$$

can be used. These equations assume that at t = 0, inductor current is zero. This situation is called "discontinuous mode operation" in switching regulator parlance. Setting "t" to the switch ON time from the LT1110 specification table (typically 10μs) will yield I_{PEAK} for a specific "L" and V_{IN}. Once I_{PEAK} is known, energy in the inductor at the end of the switch ON time can be calculated as

$$E_L = \frac{1}{2}LI^2_{PEAK} \qquad (05)$$

E_L must be greater than P_L/f_{OSC} for the converter to deliver the required power. For best efficiency I_{PEAK} should be kept to 1A or less. Higher switch currents will cause excessive drop across the switch resulting in reduced efficiency. In general, switch current should be held to as low a value as possible in order to keep switch, diode and inductor losses at a minimum.

As an example, suppose 12V at 120mA is to be generated from a 4.5V to 8V input. Recalling equation (01),

$$P_L = \left(12V + 0.5V - 4.5V\right)\left(120mA\right) = 960mW. \qquad (06)$$

Energy required from the inductor is

$$\frac{P_L}{f_{OSC}} = \frac{960mW}{70kHz} = 13.7\mu J. \qquad (07)$$

APPLICATIONS INFORMATION

Picking an inductor value of 47µH with 0.2Ω DCR results in a peak switch current of

$$I_{PEAK} = \frac{4.5V}{1.0\Omega}\left[1 - e^{\frac{-1.0\Omega \bullet 10\mu s}{47\mu H}}\right] = 862mA. \tag{08}$$

Substituting I_{PEAK} into Equation 05 results in

$$E_L = \frac{1}{2}\left(47\mu H\right)\left(0.862A\right)^2 = 17.5\mu J. \tag{09}$$

Since 17.5µJ > 13.7µJ, the 47µH inductor will work. This trial-and-error approach can be used to select the optimum inductor. Keep in mind the switch current maximum rating of 1.5A. If the calculated peak current exceeds this, an external power transistor can be used.

A resistor can be added in series with the I_{LIM} pin to invoke switch current limit. The resistor should be picked such that the calculated I_{PEAK} at minimum V_{IN} is equal to the Maximum Switch Current (from Typical Performance Characteristic curves). Then, as V_{IN} increases, switch current is held constant, resulting in increasing efficiency.

Inductor Selection — Step-Down Converter

The step-down case (Figure 5) differs from the step-up in that the inductor current flows through the load during both the charge and discharge periods of the inductor. Current through the switch should be limited to ~800mA in this mode. Higher current can be obtained by using an external switch (see Figure 6). The I_{LIM} pin is the key to successful operation over varying inputs.

After establishing output voltage, output current and input voltage range, peak switch current can be calculated by the formula

$$I_{PEAK} = \frac{2I_{OUT}}{DC}\left[\frac{V_{OUT} + V_D}{V_{IN} - V_{SW} + V_D}\right] \tag{10}$$

where DC = duty cycle (0.69)
V_{SW} = switch drop in step-down mode
V_D = diode drop (0.5V for a 1N5818)
I_{OUT} = output current
V_{OUT} = output voltage
V_{IN} = minimum input voltage

V_{SW} is actually a function of switch current which is in turn a function of V_{IN}, L, time and V_{OUT}. To simplify, 1.5V can be used for V_{SW} as a very conservative value.

Once I_{PEAK} is known, inductor value can be derived from

$$L = \frac{V_{INMIN} - V_{SW} - V_{OUT}}{I_{PEAK}} \bullet t_{ON} \tag{11}$$

where t_{ON} = switch ON time (10µs).

Next, the current limit resistor R_{LIM} is selected to give I_{PEAK} from the R_{LIM} Step-Down Mode curve. The addition of this resistor keeps maximum switch current constant as the input voltage is increased.

As an example, suppose 5V at 250mA is to be generated from a 9V to 18V input. Recalling Equation (10),

$$I_{PEAK} = \frac{2\left(250mA\right)}{0.69}\left[\frac{5 + 0.5}{9 - 1.5 + 0.5}\right] = 498mA. \tag{12}$$

Next, inductor value is calculated using Equation (11)

$$L = \frac{9 - 1.5 - 5}{498mA} \bullet 10\mu s = 50\mu H. \tag{13}$$

Use the next lowest standard value (47µH).

Then pick R_{LIM} from the curve. For I_{PEAK} = 500mA, R_{LIM} = 82Ω.

Inductor Selection — Positive-to-Negative Converter

Figure 7 shows hookup for positive-to-negative conversion. All of the output power must come from the inductor. In this case,

$$P_L = \left(|V_{OUT}| + V_D\right)\left(I_{OUT}\right). \tag{14}$$

In this mode the switch is arranged in common collector or step-down mode. The switch drop can be modeled as a 0.75V source in series with a 0.65Ω resistor. When the

APPLICATIONS INFORMATION

switch closes, current in the inductor builds according to

$$I_L(+) = \frac{V_L}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \qquad (15)$$

where $R' = 0.65\Omega + DCR_L$
$V_L = V_{IN} - 0.75V$

As an example, suppose –5V at 75mA is to be generated from a 4.5V to 5.5V input. Recalling Equation (14),

$$P_L = (|-5V| + 0.5V)(75mA) = 413mW. \qquad (16)$$

Energy required from the inductor is

$$\frac{P_L}{f_{OSC}} = \frac{413mW}{70kHz} = 5.9\mu J. \qquad (17)$$

Picking an inductor value of 56µH with 0.2Ω DCR results in a peak switch current of

$$I_{PEAK} = \frac{(4.5V - 0.75V)}{(0.65\Omega + 0.2\Omega)}\left(1 - e^{\frac{-0.85\Omega \bullet 10\mu s}{56\mu H}}\right) = 621mA. \qquad (18)$$

Substituting I_{PEAK} into Equation (04) results in

$$E_L = \frac{1}{2}(56\mu H)(0.621A)^2 = 10.8\mu J. \qquad (19)$$

Since 10.8µJ > 5.9µJ, the 56µH inductor will work.

With this relatively small input range, R_{LIM} is not usually necessary and the I_{LIM} pin can be tied directly to V_{IN}. As in the step-down case, peak switch current should be limited to ~800mA.

Capacitor Selection

Selecting the right output capacitor is almost as important as selecting the right inductor. A poor choice for a filter capacitor can result in poor efficiency and/or high output ripple. Ordinary aluminum electrolytics, while inexpensive and readily available, may have unacceptably poor Equivalent Series Resistance (ESR) and ESL (inductance). There are low ESR aluminum capacitors on the market specifically designed for switch mode DC-DC converters which work much better than general-purpose units. Tantalum capacitors provide still better performance at more expense. We recommend OS-CON capacitors from Sanyo Corporation (San Diego, CA). These units are physically quite small and have extremely low ESR. To illustrate, Figures 1, 2 and 3 show the output voltage of an LT1110 based converter with three 100µF capacitors. The peak switch current is 500mA in all cases. Figure 1 shows a Sprague 501D, 25V aluminum capacitor. V_{OUT} jumps by over 120mV when the switch turns off, followed by a drop in voltage as the inductor dumps into the capacitor. This works out to be an ESR of over 240mΩ. Figure 2 shows the same circuit, but with a Sprague 150D, 20V tantalum capacitor replacing the aluminum unit. Output jump is now about 35mV, corresponding to an ESR of 70mΩ. Figure 3 shows the circuit with a 16V OS-CON unit. ESR is now only 20mΩ.

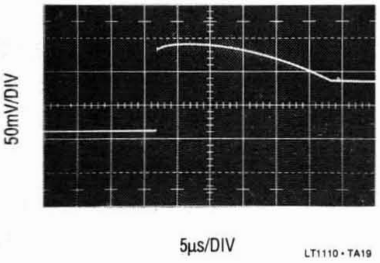


Figure 1. Aluminum

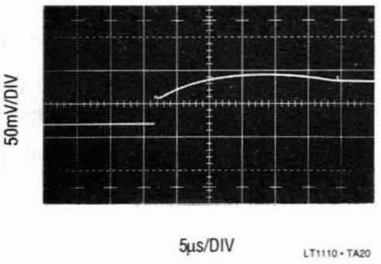


Figure 2. Tantalum

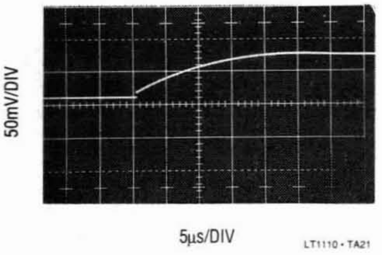


Figure 3. OS-CON

APPLICATIONS INFORMATION

Diode Selection

Speed, forward drop, and leakage current are the three main considerations in selecting a catch diode for LT1110 converters. General purpose rectifiers such as the 1N4001 are *unsuitable* for use in *any* switching regulator application. Although they are rated at 1A, the switching time of a 1N4001 is in the 10µs-50µs range. At best, efficiency will be severely compromised when these diodes are used; at worst, the circuit may not work at all. Most LT1110 circuits will be well served by a 1N5818 Schottky diode, or its surface mount equivalent, the MBRS130T3. The combination of 500mV forward drop at 1A current, fast turn ON and turn OFF time, and 4µA to 10µA leakage current fit nicely with LT1110 requirements. At peak switch currents of 100mA or less, a 1N4148 signal diode may be used. This diode has leakage current in the 1nA-5nA range at 25°C and lower cost than a 1N5818. (You can also use them to get your circuit up and running, but beware of destroying the diode at 1A switch currents.)

Step-Up (Boost Mode) Operation

A step-up DC-DC converter delivers an output voltage higher than the input voltage. Step-up converters are *not* short circuit protected since there is a DC path from input to output.

The usual step-up configuration for the LT1110 is shown in Figure 4. The LT1110 first pulls SW1 low causing $V_{IN} - V_{CESAT}$ to appear across L1. A current then builds up in L1. At the end of the switch ON time the current in L1 is[1]:

$$I_{PEAK} = \frac{V_{IN}}{L} t_{ON} \qquad (20)$$

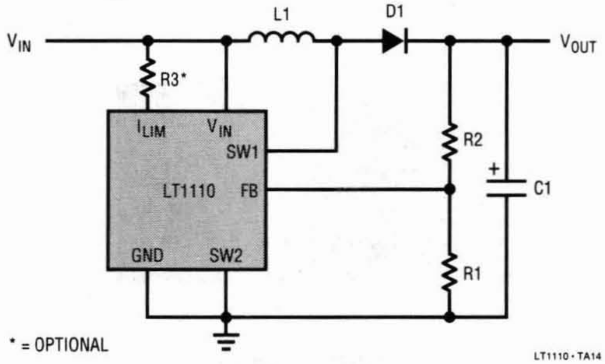


Figure 4. Step-Up Mode Hookup.

Immediately after switch turn off, the SW1 voltage pin starts to rise because current cannot instantaneously stop flowing in L1. When the voltage reaches $V_{OUT} + V_D$, the inductor current flows through D1 into C1, increasing V_{OUT}. This action is repeated as needed by the LT1110 to keep V_{FB} at the internal reference voltage of 220mV. R1 and R2 set the output voltage according to the formula

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(220\text{mV}). \qquad (21)$$

Step-Down (Buck Mode) Operation

A step-down DC-DC converter converts a higher voltage to a lower voltage. The usual hookup for an LT1110 based step-down converter is shown in Figure 5.

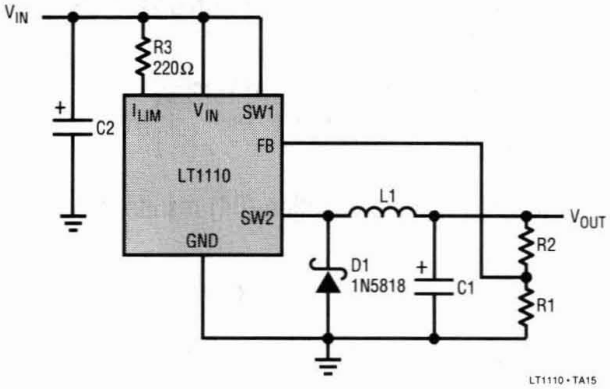


Figure 5. Step-Down Mode Hookup

When the switch turns on, SW2 pulls up to $V_{IN} - V_{SW}$. This puts a voltage across L1 equal to $V_{IN} - V_{SW} - V_{OUT}$, causing a current to build up in L1. At the end of the switch ON time, the current in L1 is equal to

$$I_{PEAK} = \frac{V_{IN} - V_{SW} - V_{OUT}}{L} t_{ON}. \qquad (22)$$

When the switch turns off, the SW2 pin falls rapidly and actually goes below ground. D1 turns on when SW2 reaches 0.4V below ground. *D1 MUST BE A SCHOTTKY DIODE.* The voltage at SW2 must never be allowed to go below –0.5V. A silicon diode such as the 1N4933 will allow SW2 to go to –0.8V, causing potentially destructive power

---

[1] **Note 1**: This simple expression neglects the effects of switch and coil resistance. This is taken into account in the "Inductor Selection" section.

APPLICATIONS INFORMATION

dissipation inside the LT1110. Output voltage is determined by

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(220mV). \tag{23}$$

R3 programs switch current limit. This is especially important in applications where the input varies over a wide range. Without R3, the switch stays on for a fixed time each cycle. Under certain conditions the current in L1 can build up to excessive levels, exceeding the switch rating and/or saturating the inductor. The 220Ω resistor programs the switch to turn off when the current reaches approximately 800mA. When using the LT1110 in step-down mode, output voltage should be limited to 6.2V or less. Higher output voltages can be accommodated by inserting a 1N5818 diode in series with the SW2 pin (anode connected to SW2).

Higher Current Step-Down Operation

Output current can be increased by using a discrete PNP pass transistor as shown in Figure 6. R1 serves as a current limit sense. When the voltage drop across R1 equals a V_{BE}, the switch turns off. For temperature compensation a Schottky diode can be inserted in series with the I_{LIM} pin. This also lowers the maximum drop across R1 to $V_{BE} - V_D$, increasing efficiency. As shown, switch current is limited to 2A. Inductor value can be calculated based on formulas in the “Inductor Selection Step-Down Converter” section with the following conservative expression for V_{SW}:

$$V_{SW} = V_{R1} + V_{SAT} \approx 0.9V. \tag{24}$$

R2 provides a current path to turn off Q1. R3 provides base drive to Q1. R4 and R5 set output voltage.

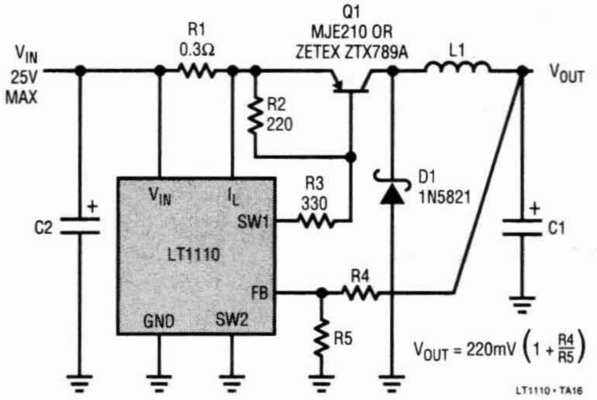

Q1
MJE210 OR
ZETEX ZTX789A
R1
0.3Ω
L1
V_{IN}
25V
MAX
V_{OUT}
R2
220
R3
330
D1
1N5821
C2
C1
V_{IN}
I_L
SW1
LT1110
FB
GND
SW2
R4
R5
$V_{OUT} = 220mV\left(1 + \frac{R4}{R5}\right)$
LT1110 • TA16

Figure 6. Q1 Permits Higher-Current Switching. LT1110 Functions as Controller.

Inverting Configurations

The LT1110 can be configured as a positive-to-negative converter (Figure 7), or a negative-to-positive converter (Figure 8). In Figure 7, the arrangement is very similar to a step-down, except that the high side of the feedback is referred to ground. This level shifts the output negative. As in the step-down mode, D1 must be a Schottky diode, and $|V_{OUT}|$ should be less than 6.2V. More negative output voltages can be accommodated as in the prior section.

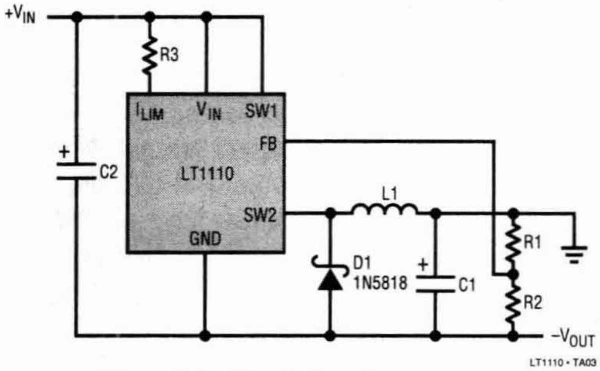

$+V_{IN}$
R3
I_{LIM}
V_{IN}
SW1
FB
C2
LT1110
SW2
GND
L1
D1
1N5818
C1
R1
R2
$-V_{OUT}$
LT1110 • TA03

Figure 7. Positive-to-Negative Converter

In Figure 8, the input is negative while the output is positive. In this configuration, the magnitude of the input voltage can be higher or lower than the output voltage. A level shift, provided by the PNP transistor, supplies proper polarity feedback information to the regulator.

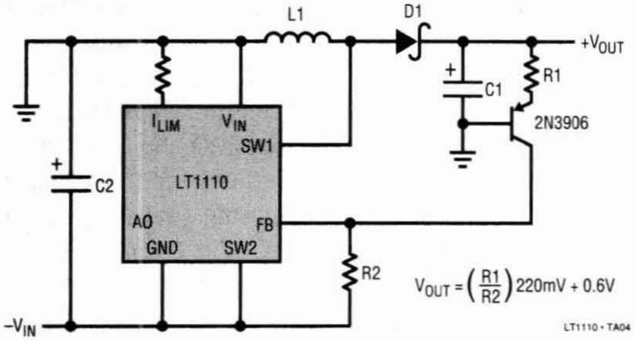

L1
D1
$+V_{OUT}$
C1
R1
2N3906
I_{LIM}
V_{IN}
SW1
C2
LT1110
AO
FB
GND
SW2
R2
$V_{OUT} = \left(\frac{R1}{R2}\right) 220mV + 0.6V$
$-V_{IN}$
LT1110 • TA04

Figure 8. Negative-to-Positive Converter

APPLICATIONS INFORMATION

Using the I_{LIM} Pin

The LT1110 switch can be programmed to turn off at a set switch current, a feature not found on competing devices. This enables the input to vary over a wide range without exceeding the maximum switch rating or saturating the inductor. Consider the case where analysis shows the LT1110 must operate at an 800mA peak switch current with a 2.0V input. If V_{IN} rises to 4V, peak current will rise to 1.6A, exceeding the maximum switch current rating. With the proper resistor selected (see the "Maximum Switch Current vs R_{LIM}" characteristic), the switch current will be limited to 800mA, even if the input voltage increases.

Another situation where the I_{LIM} feature is useful occurs when the device goes into continuous mode operation. This occurs in step-up mode when

$$\frac{V_{OUT}+V_{DIODE}}{V_{IN}-V_{SW}} < \frac{1}{1-DC}. \qquad (25)$$

When the input and output voltages satisfy this relationship, inductor current does not go to zero during the switch OFF time. When the switch turns on again, the current ramp starts from the non-zero current level in the inductor just prior to switch turn on. As shown in Figure 9, the inductor current increases to a high level before the comparator turns off the oscillator. This high current can cause excessive output ripple and requires oversizing the output capacitor and inductor. With the I_{LIM} feature, however, the switch current turns off at a programmed level as shown in Figure 10, keeping output ripple to a minimum.

Figure 11 details current limit circuitry. Sense transistor Q1, whose base and emitter are paralleled with power switch Q2, is ratioed such that approximately 0.5% of Q2's collector current flows in Q1's collector. This current is passed through internal 80Ω resistor R1 and out through the I_{LIM} pin. The value of the external resistor connected between I_{LIM} and V_{IN} set the current limit. When sufficient switch current flows to develop a V_{BE} across R1 + R_{LIM}, Q3 turns on and injects current into the oscillator, turning off the switch. Delay through this circuitry is approximately 800ns. The current trip point becomes less accurate for switch ON times less than 3μs. Resistor values programming switch ON time for 800ns or less will cause spurious response in the switch circuitry although the device will still maintain output regulation.

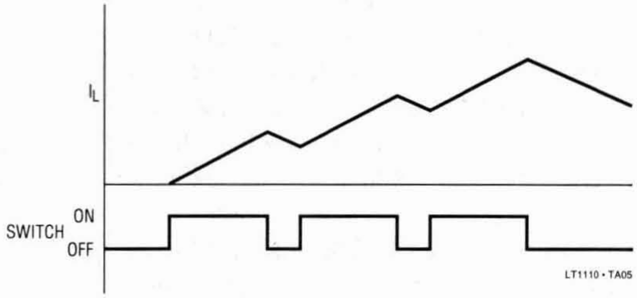


Figure 9. No Current Limit Causes Large Inductor Current Build-Up

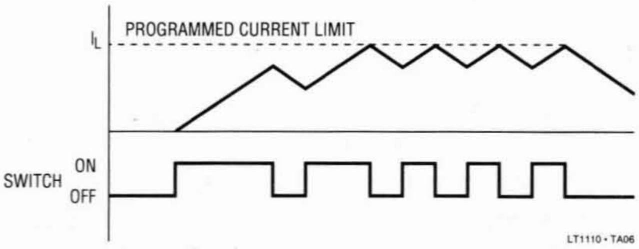


Figure 10. Current Limit Keeps Inductor Current Under Control

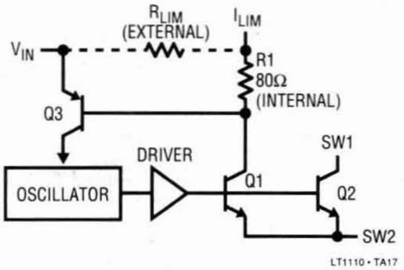


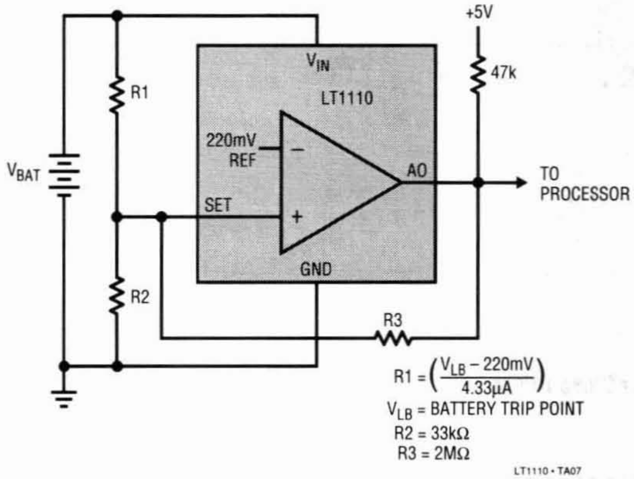
Figure 11. LT1110 Current Limit Circuitry

Using the Gain Block

The gain block (GB) on the LT1110 can be used as an error amplifier, low battery detector or linear post regulator. The gain block itself is a very simple PNP input op amp with an open collector NPN output. The negative input of the gain block is tied internally to the 220mV reference. The positive input comes out on the SET pin.

APPLICATIONS INFORMATION

Arrangement of the gain block as a low battery detector is straightforward. Figure 12 shows hookup. R1 and R2 need only be low enough in value so that the bias current of the SET input does not cause large errors. 33kΩ for R2 is adequate. R3 can be added to introduce a small amount of hysteresis. This will cause the gain block to "snap" when the trip point is reached. Values in the 1M-10M range are optimal. The addition of R3 will change the trip point, however.



$R1 = \left(\frac{V_{LB} - 220mV}{4.33\mu A}\right)$

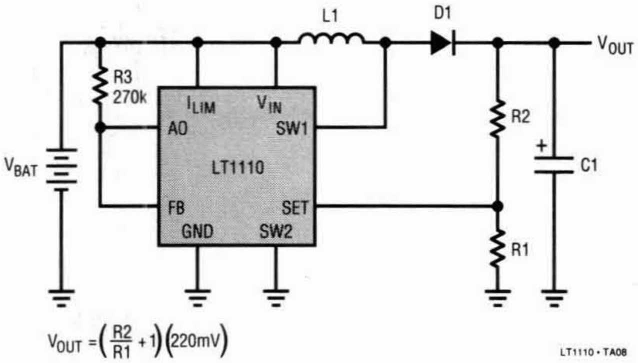
V_{LB} = BATTERY TRIP POINT

R2 = 33kΩ

R3 = 2MΩ

Figure 12. Setting Low Battery Detector Trip Point

Output ripple of the LT1110, normally 90mV at $5V_{OUT}$ can be reduced significantly by placing the gain block in front of the FB input as shown in Figure 13. This effectively reduces the comparator hysteresis by the gain of the gain block. Output ripple can be reduced to just a few millivolts using this technique. Ripple reduction works with step-down or inverting modes as well. For this technique to be effective, output capacitor C1 must be large, so that each switching cycle increases V_{OUT} by only a few millivolts. 1000µF is a good starting value.



$V_{OUT} = \left(\frac{R2}{R1} + 1\right)(220mV)$

Figure 13. Output Ripple Reduction Using Gain Block

Table 1. Inductor Manufacturers

MANUFACTURER	PART NUMBERS
Coiltronics International 984 S.W. 13th Court Pompano Beach, FL 33069 305-781-8900	CTX100-4 Series Surface Mount
Toko America Incorporated 1250 Feehanville Drive Mount Prospect, IL 60056 312-297-0070	Type 8RBS
Sumida Electric Co. USA 708-956-0666	CD54 CDR74 CDR105 Surface Mount

Table 2. Capacitor Manufacturers

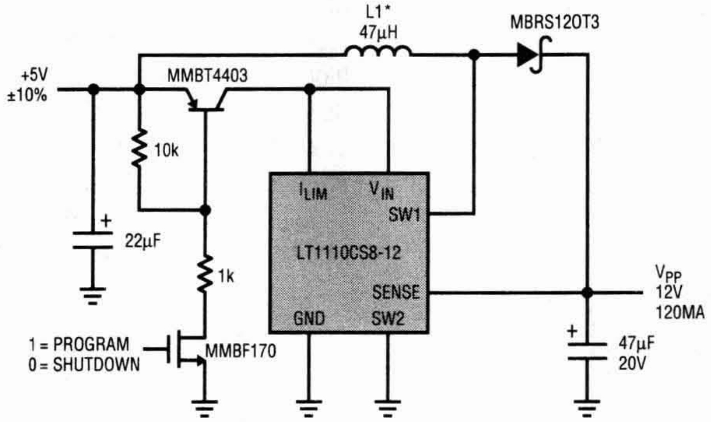
MANUFACTURER	PART NUMBERS
Sanyo Video Components 1201 Sanyo Avenue San Diego, CA 92073 619-661-6322	OS-CON Series
Nichicon America Corporation 927 East State Parkway Schaumberg, IL 60173 708-843-7500	PL Series
Sprague Electric Company Lower Main Street Sanford, ME 04073 207-324-4140	150D Solid Tantalums 550D Tantalex
Matsuo 714-969-2491	267 Series Surface Mount

Table 3. Transistor Manufacturers

MANUFACTURER	PART NUMBERS
Zetex Commack, NY 516-543-7100	ZTX Series FZT Series Surface Mount

TYPICAL APPLICATIONS

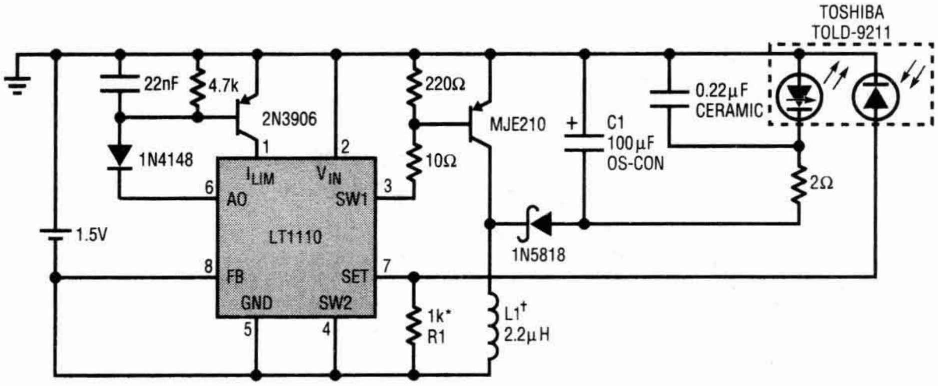
All Surface Mount
Flash Memory V_{PP} Generator


L1*
47μH
MBRS120T3
+5V
±10%
MMBT4403
10k
22μF
1k
I_{LIM}
V_{IN}
SW1
LT1110CS8-12
SENSE
GND
SW2
V_{PP}
12V
120MA
1 = PROGRAM
0 = SHUTDOWN
MMBF170
47μF
20V

*L1= SUMIDA CD105-470M

LT1110 • TA18

1.5V Powered Laser Diode Driver


TOSHIBA
TOLD-9211
22nF
4.7k
2N3906
220Ω
MJE210
0.22μF
CERAMIC
1N4148
1
2
C1
100μF
OS-CON
10Ω
I_{LIM}
V_{IN}
3
6
AO
SW1
2Ω
1.5V
LT1110
1N5818
8
FB
SET
7
GND
SW2
5
4
1k*
R1
L1†
2.2μH

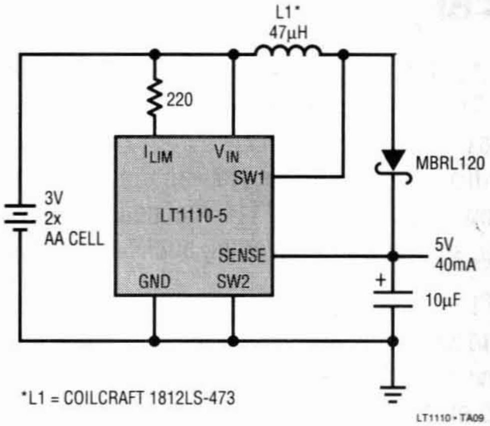
* ADJUST R1 FOR CHANGE IN LASER OUTPUT POWER
† TOKO 262LYF-0076M

- LASER DIODE CASE COMMON TO +BATTERY TERMINAL
- 170mA CURRENT DRAIN FROM 1.5V CELL (50mA DIODE)
- NO OVERSHOOT

LT1110 • TA13

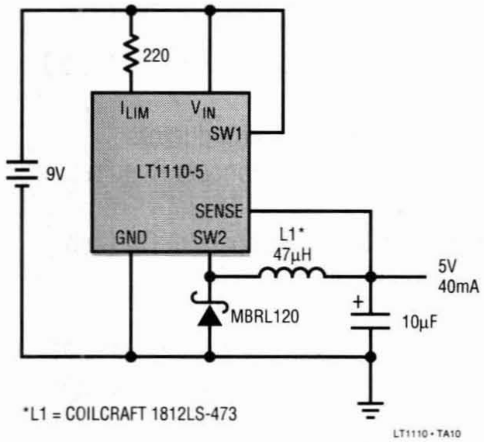
TYPICAL APPLICATIONS

All Surface Mount
3V to 5V Step-Up Converter


L1*
47μH
220
I_{LIM}
V_{IN}
SW1
LT1110-5
SENSE
GND
SW2
MBRL120
3V
2x
AA CELL
5V
40mA
10μF
+
LT1110 • TA09

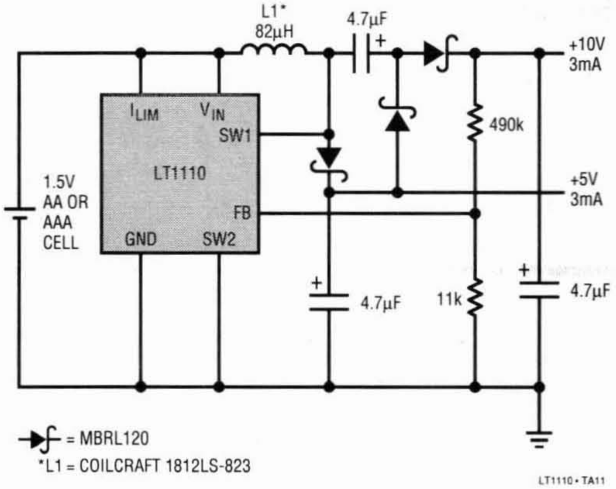
*L1 = COILCRAFT 1812LS-473

All Surface Mount
9V to 5V Step-Down Converter


220
I_{LIM}
V_{IN}
SW1
LT1110-5
SENSE
GND
SW2
9V
L1*
47μH
5V
40mA
MBRL120
10μF
+
LT1110 • TA10

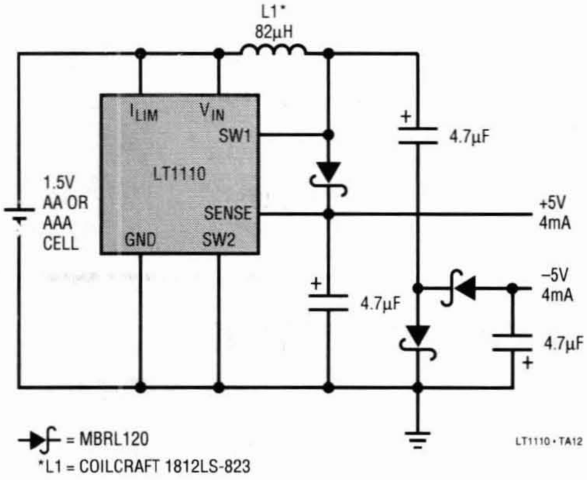
*L1 = COILCRAFT 1812LS-473

All Surface Mount
1.5V to +10V, +5V Dual Output Step-Up Converter


L1*
82μH
4.7μF
+
+10V
3mA
I_{LIM}
V_{IN}
SW1
LT1110
FB
GND
SW2
490k
+5V
3mA
1.5V
AA OR
AAA
CELL
4.7μF
11k
4.7μF
LT1110 • TA11

= MBRL120
*L1 = COILCRAFT 1812LS-823

All Surface Mount
1.5V to ±5V Dual Output Step-Up Converter


L1*
82μH
I_{LIM}
V_{IN}
SW1
LT1110
SENSE
GND
SW2
4.7μF
+
1.5V
AA OR
AAA
CELL
+5V
4mA
–5V
4mA
4.7μF
4.7μF
LT1110 • TA12

= MBRL120
*L1 = COILCRAFT 1812LS-823

LT1111

Micropower DC-to-DC Converter Adjustable and Fixed 5V, 12V

FEATURES

- Operates at Supply Voltages from 2.0V to 30V
- 72kHz Oscillator
- Works with Surface-Mount Inductors
- Only Three External Components Required
- Step-Up or Step-Down Mode
- Low-Battery Detector Comparator On-Chip
- User Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space-Saving 8-Pin MiniDIP or S8 Package

APPLICATIONS

- 3V to 5V, 5V to 12V Converters
- 9V to 5V, 12V to 5V Converters
- Remote Controls
- Peripherals and Add-On Cards
- Battery Backup Supplies
- Uninterruptible Supplies
- Laptop and Palmtop Computers
- Cellular Telephones
- Portable Instruments
- Flash Memory Vpp Generators

DESCRIPTION

The LT1111 is a versatile micropower DC-to-DC converter. The device requires only three external components to deliver a fixed output of 5V or 12V. Supply voltage ranges from 2.0V to 12V in step-up mode and to 30V in step-down mode. The LT1111 functions equally well in step-up, step-down, or inverting applications.

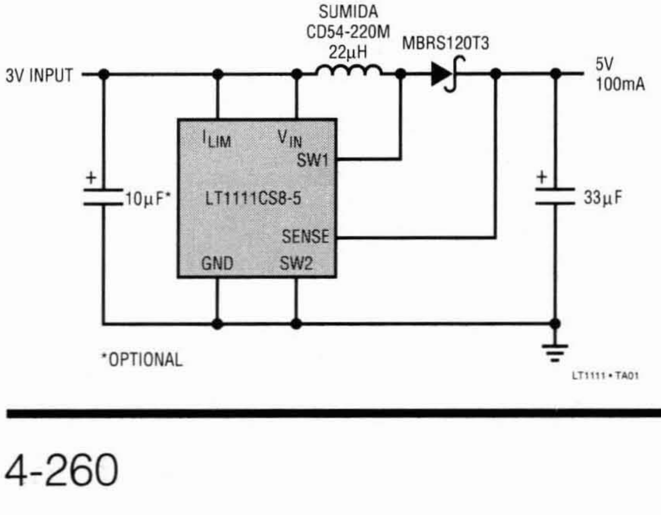
The LT1111 oscillator is set at 72kHz, optimizing the device to work with off-the-shelf surface mount inductors. The device can deliver 5V at 100mA from a 3V input in step-up mode or 5V at 200mA from a 12V input in step-down mode.

Switch current limit can be programmed with a single resistor. An auxiliary open-collector Gain Block can be configured as a low-battery detector, linear post-regulator, undervoltage lock-out circuit, or error amplifier.

For input sources of less than 2V use the LT1110.

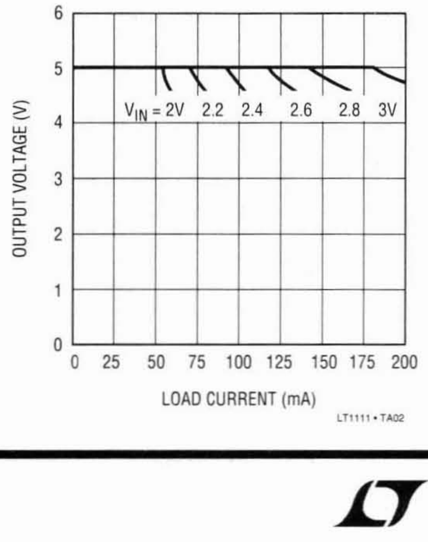
TYPICAL APPLICATION

All Surface-Mount 3V to 5V Step-Up Converter



*OPTIONAL

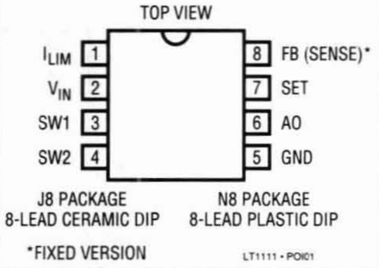
Typical Load Regulation



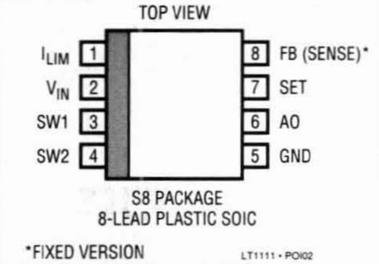
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 36V
SW1 Pin Voltage (V_{SW1}) 50V
SW2 Pin Voltage (V_{SW2})............................$-0.5V$ to V_{IN}
Feedback Pin Voltage (LT1111) 5.5V
Switch Current..1.5A
Maximum Power Dissipation 500mW
Operating Temperature Range
LT1111C ....0°C to 70°C
LT1111M ....-55°C to 125°C
Storage Temperature Range ....-65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ....300°C

PACKAGE/ORDER INFORMATION


TOP VIEW
I_LIM 1
V_IN 2
SW1 3
SW2 4
8 FB (SENSE)*
7 SET
6 AO
5 GND
J8 PACKAGE
8-LEAD CERAMIC DIP
N8 PACKAGE
8-LEAD PLASTIC DIP
LT1111 • POI01

*FIXED VERSION


TOP VIEW
I_LIM 1
V_IN 2
SW1 3
SW2 4
8 FB (SENSE)*
7 SET
6 AO
5 GND
S8 PACKAGE
8-LEAD PLASTIC SOIC
LT1111 • POI02

*FIXED VERSION

ORDER PART NUMBER
LT1111CN8 LT1111CN8-5 LT1111CN8-12 LT1111MJ8 LT1111MJ8-5 LT1111MJ8-12
LT1111CS8 LT1111CS8-5 LT1111CS8-12
S8 PART MARKING
1111 11105 11112

ELECTRICAL CHARACTERISTICS $V_{IN} = 3V$, Military or Commercial Version

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off			300	400	μA
V_{IN}	Input Voltage	Step-Up Mode	●	2.0		12.6	V
		Step-Down Mode	●			30	
	Comparator Trip Point Voltage	LT1111 (Note 1)	●	1.20	1.25	1.30	V
V_{OUT}	Output Sense Voltage	LT1111-5 (Note 2)	●	4.75	5.00	5.25	V
		LT1111-12 (Note 2)	●	11.4	12.00	12.6	
	Comparator Hysteresis	LT1111	●		8	12.5	mV
	Output Hysteresis	LT1111-5	●		32	50	mV
		LT1111-12	●		75	120	
f_{osc}	Oscillator Frequency			54	72	88	kHz
DC	Duty Cycle	Full Load		43	50	59	%
t_{on}	Switch On Time	I_{LIM} Tied to V_{IN}		5	7	9	μs
V_{SAT}	SW Sat Voltage, Step-Up Mode	$V_{IN} = 3.0V$, $I_{SW} = 650mA$			0.5	0.65	V
		$V_{IN} = 5.0V$, $I_{SW} = 1A$			0.8	1.0	
	SW Sat Voltage, Step-Down Mode	$V_{IN} = 12V$, $I_{SW} = 650mA$			1.1	1.5	
I_{fb}	Feedback Pin Bias Current	LT1111, $V_{fb} = 0V$	●		70	120	nA
I_{SET}	Set Pin Bias Current	$V_{SET} = V_{REF}$	●		70	300	nA
V_{OL}	Gain Block Output Low	$I_{SINK} = 300\mu A$, $V_{SET} = 1.00V$	●		0.15	0.4	V
	Reference Line Regulation	$5V \leq V_{IN} \leq 30V$	●		0.02	0.075	%/V
A_V	Gain Block Gain	$R_L = 100k\Omega$ (Note 3)	●	1000	6000		V/V
I_{LIM}	Current Limit	220Ω from I_{LIM} to V_{IN}			400		mA
	Current Limit Temperature Coefficient		●		-0.3		%/°C
	Switch Off Leakage Current	Measured at SW1 Pin, $V_{SW1} = 12V$			1	10	μA
	Maximum Excursion Below GND	$I_{SW1} \leq 10\mu A$, Switch Off			-400	-350	mV

ELECTRICAL CHARACTERISTICS $V_{IN} = 3V$, $-55°C \le T_A \le 125°C$ unless otherwise noted.

					LT1111M			
SYMBOL	**PARAMETER**	**CONDITIONS**			**MIN**	**TYP**	**MAX**	**UNITS**
I_Q	Quiescent Current	Switch Off		●		300	450	μA
f_{osc}	Oscillator Frequency			●	45	72	100	kHz
DC	Duty Cycle	Full Load		●	40	50	62	%
t_{on}	Switch On Time	I_{LIM} Tied to V_{IN}		●	5	7	11	μs
	Reference Line Regulation	$2.0V \le V_{IN} \le 5V$	$0°C \le T_A \le 125°C$			0.2	0.4	%/V
			$T_A = -55°C$				0.8	
V_{SAT}	SW Sat Voltage, Step-Up Mode	$0°C \le T_A \le 125°C$, $I_{SW} = 500mA$ $T_A = -55°C$, $I_{SW} = 400mA$				0.5	0.65	V
	SW Sat Voltage, Step-Down Mode	$V_{IN} = 12V$,	$0°C \le T_A \le 125°C$				1.5	
		$I_{SW} = 500mA$	$T_A = -55°C$				2.0	

ELECTRICAL CHARACTERISTICS $V_{IN} = 3V$, $0°C \le T_A \le 70°C$ unless otherwise noted.

				LT1111C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
I_Q	Quiescent Current	Switch Off	●		300	400	μA
f_{osc}	Oscillator Frequency		●	54	72	95	kHz
DC	Duty Cycle	Full Load	●	43	50	59	%
t_{on}	Switch On Time	I_{LIM} Tied to V_{IN}	●	5	7	9	μs
	Reference Line Regulation	$2.0V \le V_{IN} \le 5V$	●		0.2	0.4	%/V
V_{SAT}	SW Sat Voltage, Step-Up Mode	$V_{IN} = 3V$, $I_{SW} = 650mA$	●		0.5	0.65	V
	SW Sat Voltage, Step-Down Mode	$V_{IN} = 12V$, $I_{SW} = 650mA$	●		1.1	1.5	

The ● denotes specifications which apply over the operating temperature range.

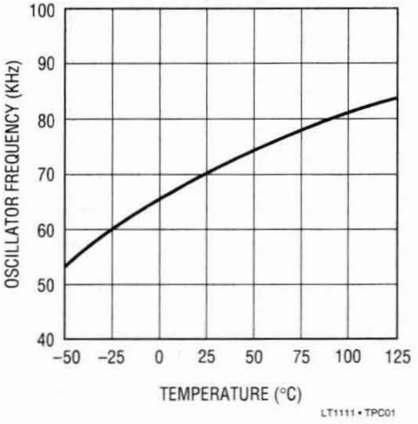
Note 1: This specification guarantees that both the high and low trip points of the comparator fall within the 1.20V to 1.30V range.

Note 2: The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed-output versions will always be within the specified range.

Note 3: 100kΩ resistor connected between a 5V source and the AO pin.

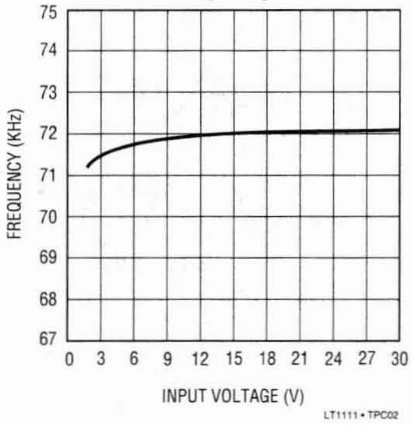
TYPICAL PERFORMANCE CHARACTERISTICS

Oscillator Frequency



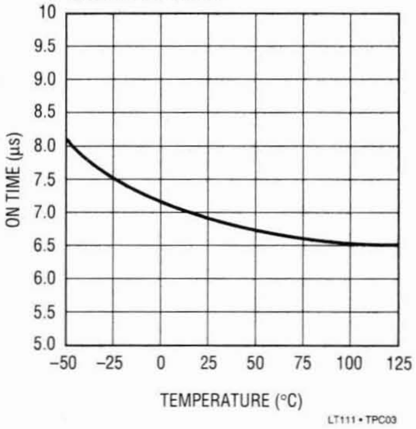
LT1111 • TPC01

Oscillator Frequency



LT1111 • TPC02

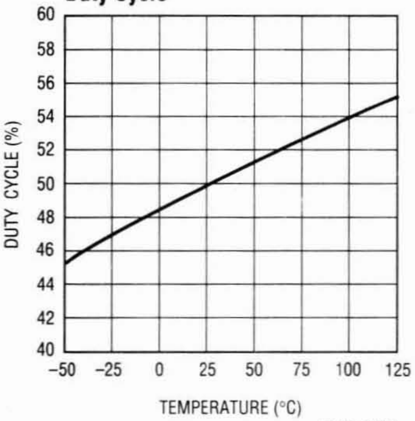
Switch On Time



LT111 • TPC03

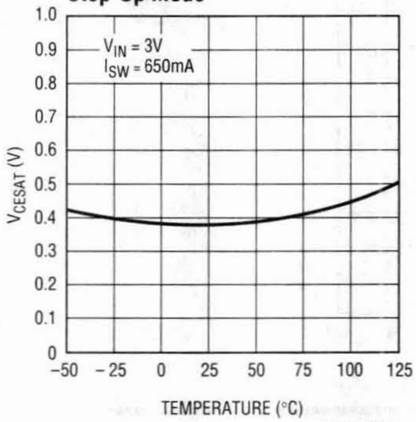
TYPICAL PERFORMANCE CHARACTERISTICS

Duty Cycle



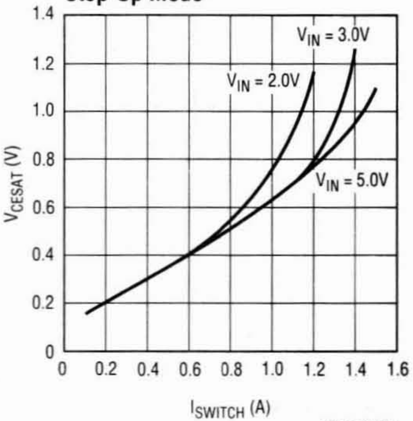
LT1111 • TPC04

Saturation Voltage Step-Up Mode



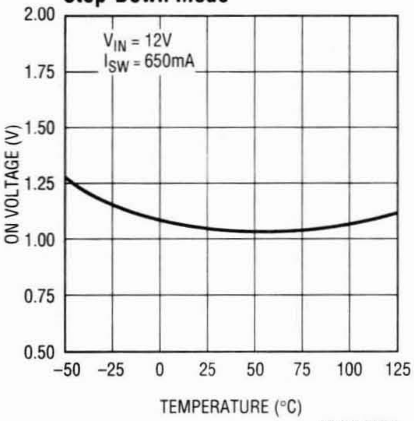
LT1111 • TPC05

Saturation Voltage Step-Up Mode



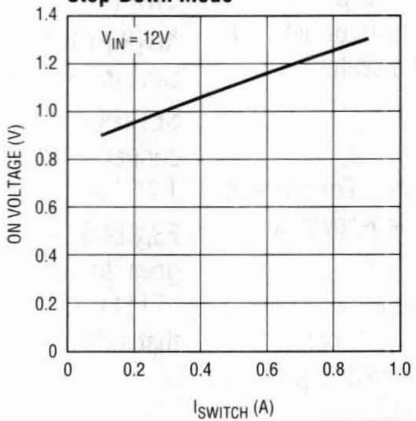
LT1111 • TPC06

Switch On Voltage Step-Down Mode



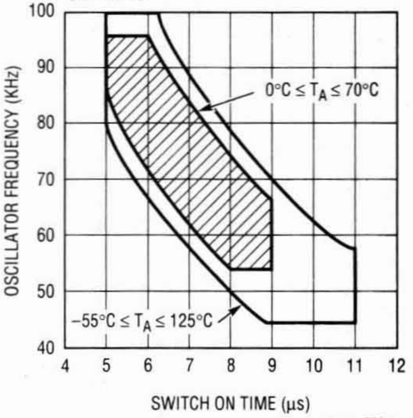
LT1111 • TPC07

Switch On Voltage Step-Down Mode



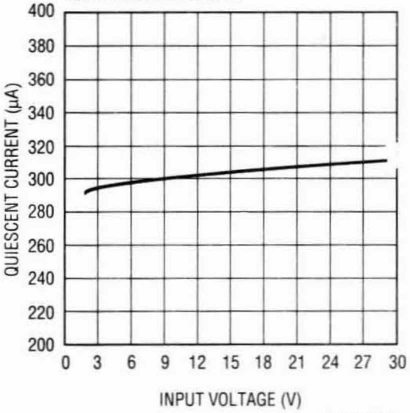
LT1111 • TPC08

Minimum/Maximum Frequency vs On Time



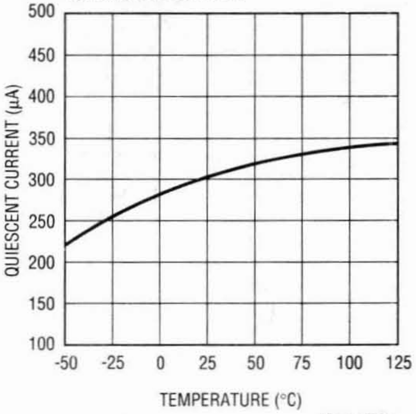
LT1111 • TPC09

Quiescent Current



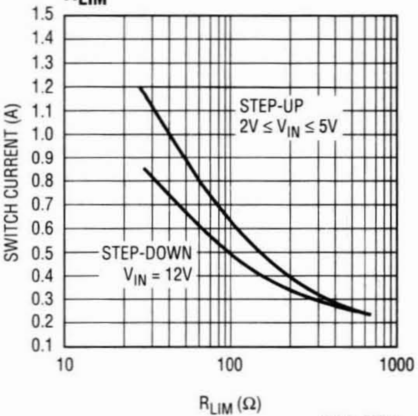
LT1111 • TPC10

Quiescent Current



LT1111 • TPC11

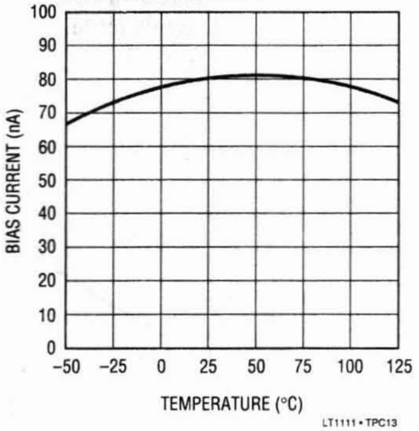
Maximum Switch Current vs R_{LIM}



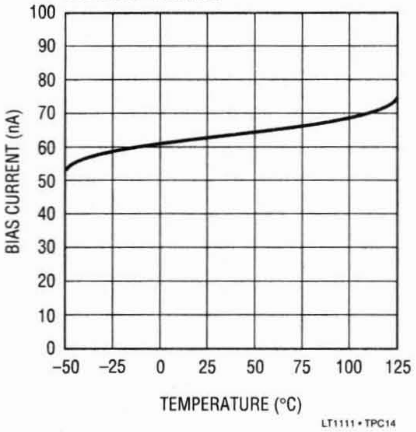
LT1111 • TPC12

TYPICAL PERFORMANCE CHARACTERISTICS

Set Pin Bias Current



FB Bias Current



PIN FUNCTIONS

I_{LIM} (Pin 1): Connect this pin to V_{IN} for normal use. Where lower current limit is desired, connect a resistor between I_{LIM} and V_{IN}. A 220Ω resistor will limit the switch current to approximately 400mA.

V_{IN} (Pin 2): Input supply voltage.

SW1 (Pin 3): Collector of power transistor. For step-up mode connect to inductor/diode. For step-down mode connect to V_{IN}.

SW2 (Pin 4): Emitter of power transistor. For step-up mode connect to ground. For step-down mode connect to inductor/diode. This pin must never be allowed to go more than a Schottky diode drop below ground.

GND (Pin 5): Ground.

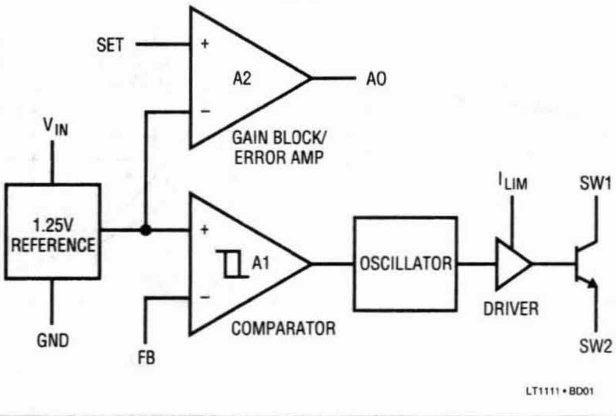
AO (Pin 6): Auxiliary Gain Block (GB) output. Open collector, can sink 300μA.

SET (Pin 7): GB input. GB is an op amp with positive input connected to SET pin and negative input connected to 1.25V reference.

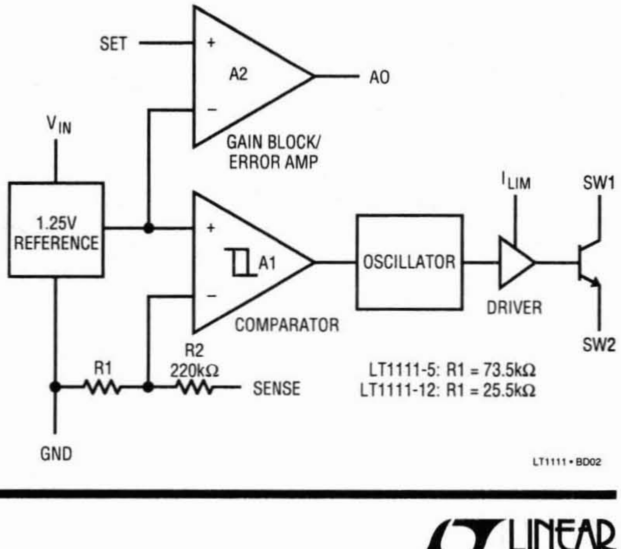
FB/SENSE (Pin 8): On the LT1111 (adjustable) this pin goes to the comparator input. On the LT1111-5 and LT1111-12, this pin goes to the internal application resistor that sets output voltage.

BLOCK DIAGRAMS

LT1111


SET
+
A2
−
AO
GAIN BLOCK/
ERROR AMP
V_{IN}
1.25V
REFERENCE
GND
+
A1
−
COMPARATOR
FB
OSCILLATOR
I_{LIM}
DRIVER
SW1
SW2
LT1111 • BD01

LT1111-5, -12


SET
+
A2
−
AO
GAIN BLOCK/
ERROR AMP
V_{IN}
1.25V
REFERENCE
+
A1
−
COMPARATOR
OSCILLATOR
I_{LIM}
DRIVER
SW1
SW2
R1
R2
220kΩ
SENSE
GND
LT1111-5: R1 = 73.5kΩ
LT1111-12: R1 = 25.5kΩ
LT1111 • BD02

LT1111 OPERATION

The LT1111 is a gated oscillator switcher. This type architecture has very low supply current because the switch is cycled when the feedback pin voltage drops below the reference voltage. Circuit operation can best be understood by referring to the LT1111 block diagram. Comparator A1 compares the feedback (FB) pin voltage with the 1.25V reference signal. When FB drops below 1.25V, A1 switches on the 72kHz oscillator. The driver amplifier boosts the signal level to drive the output NPN power switch. The switch cycling action raises the output voltage and FB pin voltage. When the FB voltage is sufficient to trip A1, the oscillator is gated off. A small amount of hysteresis built into A1 ensures loop stability without external frequency compensation. When the comparator output is low, the oscillator and all high-current circuitry is turned off, lowering device quiescent current to just 300µA.

The oscillator is set internally for 7µs ON time and 7µs OFF time, optimizing the device for circuits where V_{OUT} and V_{IN} differ by roughly a factor of 2. Examples include a 3V to 5V step-up converter or a 9V to 5V step-down converter.

Gain block A2 can serve as a low-battery detector. The negative input of A2 is the 1.25V reference. A resistor divider from V_{IN} to GND, with the mid-point connected to the SET pin provides the trip voltage in a low-battery detector application. AO can sink 300µA (use a 22k resistor pull-up to +5V).

A resistor connected between the I_{LIM} pin and V_{IN} sets maximum switch current. When the switch current exceeds the set value, the switch cycle is prematurely terminated. If current limit is not used, I_{LIM} should be tied directly to V_{IN}. Propagation delay through the current-limit circuitry is approximately 1µs.

In step-up mode the switch emitter (SW2) is connected to ground and the switch collector (SW1) drives the inductor; in step-down mode the collector is connected to V_{IN} and the emitter drives the inductor.

The LT1111-5 and LT1111-12 are functionally identical to the LT1111. The -5 and -12 versions have on-chip voltage setting resistors for fixed 5V or 12V outputs. Pin 8 on the fixed versions should be connected to the output. No external resistors are needed.

APPLICATIONS INFORMATION

Inductor Selection — General

A DC-DC converter operates by storing energy as magnetic flux in an inductor core, and then switching this energy into the load. Since it is flux, not charge, that is stored, the output voltage can be higher, lower, or opposite in polarity to the input voltage by choosing an appropriate switching topology. To operate as an efficient energy transfer element, the inductor must fulfill three requirements. First, the inductance must be low enough for the inductor to store adequate energy under the worst case condition of minimum input voltage and switch ON time. The inductance must also be high enough so maximum current ratings of the LT1111 and inductor are not exceeded at the other worst case condition of maximum input voltage and ON time. Additionally, the inductor core must be able to store the required flux; i.e., it must not *saturate*. At power levels generally encountered with LT1111 based designs, small surface-mount ferrite core units with saturation current ratings in the 300mA to 1A range and DCR less than 0.4Ω (depending on application) are adequate. Lastly, the inductor must have sufficiently low DC resistance so excessive power is not lost as heat in the windings. An additional consideration is Electro-Magnetic Interference (EMI). Toroid and pot core type inductors are recommended in applications where EMI must be kept to a minimum; for example, where there are sensitive analog circuitry or transducers nearby. Rod core types are a less expensive choice where EMI is not a problem. Minimum and maximum input voltage, output voltage and output current must be established before an inductor can be selected.

Inductor Selection — Step-Up Converter

In a step-up, or boost converter (Figure 4), power generated by the inductor makes up the difference between input and output. Power required from the inductor is

APPLICATIONS INFORMATION

determined by

$$P_L = \left(V_{OUT} + V_D - V_{IN\,MIN}\right)\left(I_{OUT}\right) \tag{01}$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky). Energy required by the inductor per cycle must be equal or greater than

$$P_L / f_{OSC} \tag{02}$$

in order for the converter to regulate the output.

When the switch is closed, current in the inductor builds according to

$$I_L(t) = \frac{V_{IN}}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \tag{03}$$

where R' is the sum of the switch equivalent resistance (0.8Ω typical at 25°C) and the inductor DC resistance. When the drop across the switch is small compared to V_{IN}, the simple lossless equation

$$I_L(t) = \frac{V_{IN}}{L}t \tag{04}$$

can be used. These equations assume that at t = 0, inductor current is zero. This situation is called "discontinuous mode operation" in switching regulator parlance. Setting "t" to the switch ON time from the LT1111 specification table (typically 7μs) will yield I_{PEAK} for a specific "L" and V_{IN}. Once I_{PEAK} is known, energy in the inductor at the end of the switch ON time can be calculated as

$$E_L = \frac{1}{2}LI^2_{PEAK} \tag{05}$$

E_L must be greater than P_L/f_{OSC} for the converter to deliver the required power. For best efficiency I_{PEAK} should be kept to 1A or less. Higher switch currents will cause excessive drop across the switch resulting in reduced efficiency. In general, switch current should be held to as low a value as possible in order to keep switch, diode and inductor losses at a minimum.

As an example, suppose 12V at 60mA is to be generated from a 4.5V to 8V input. Recalling equation (01),

$$P_L = \left(12V + 0.5V - 4.5V\right)\left(60mA\right) = 480mW. \tag{06}$$

Energy required from the inductor is

$$\frac{P_L}{f_{OSC}} = \frac{480mW}{72kHz} = 6.7\mu J \tag{07}$$

Picking an inductor value of 47μH with 0.2Ω DCR results in a peak switch current of

$$I_{PEAK} = \frac{4.5V}{1.0\Omega}\left(1 - e^{\frac{-1.0\Omega \bullet 7\mu s}{47\mu H}}\right) = 623mA. \tag{08}$$

Substituting I_{PEAK} into Equation 04 results in

$$E_L = \frac{1}{2}\left(47\mu H\right)\left(0.623A\right)^2 = 9.1\mu J \tag{09}$$

Since 9.1μJ > 6.7μJ, the 47μH inductor will work. This trial-and-error approach can be used to select the optimum inductor. Keep in mind the switch current maximum rating of 1.5A. If the calculated peak current exceeds this, consider using the LT1110. The 70% duty cycle of the LT1110 allows more energy per cycle to be stored in the inductor, resulting in more output power.

A resistor can be added in series with the I_{LIM} pin to invoke switch current limit. The resistor should be picked so the calculated I_{PEAK} at minimum V_{IN} is equal to the Maximum Switch Current (from Typical Performance Characteristic curves). Then, as V_{IN} increases, switch current is held constant, resulting in increasing efficiency.

Inductor Selection — Step-Down Converter

The step-down case (Figure 5) differs from the step-up in that the inductor current flows through the load during both the charge and discharge periods of the inductor. Current through the switch should be limited to ~650mA in this mode. Higher current can be obtained by using an external switch (see Figure 6). The I_{LIM} pin is the key to successful operation over varying inputs.

After establishing output voltage, output current and input voltage range, peak switch current can be calculated by the

APPLICATIONS INFORMATION

formula

$$I_{PEAK} = \frac{2I_{OUT}}{DC}\left[\frac{V_{OUT}+V_D}{V_{IN}-V_{SW}+V_D}\right] \tag{10}$$

where DC = duty cycle (0.50)
V_{SW} = switch drop in step-down mode
V_D = diode drop (0.5V for a 1N5818)
I_{OUT} = output current
V_{OUT} = output voltage
V_{IN} = minimum input voltage

V_{SW} is actually a function of switch current which is in turn a function of V_{IN}, L, time, and V_{OUT}. To simplify, 1.5V can be used for V_{SW} as a very conservative value.

Once I_{PEAK} is known, inductor value can be derived from

$$L = \frac{V_{INMIN}-V_{SW}-V_{OUT}}{I_{PEAK}} \bullet t_{ON} \tag{11}$$

where t_{ON} = switch ON time (7µs).

Next, the current limit resistor R_{LIM} is selected to give I_{PEAK} from the R_{LIM} Step-Down Mode curve. The addition of this resistor keeps maximum switch current constant as the input voltage is increased.

As an example, suppose 5V at 300mA is to be generated from a 12V to 24V input. Recalling Equation (10),

$$I_{PEAK} = \frac{2(300\text{mA})}{0.50}\left[\frac{5+0.5}{12-1.5+0.5}\right] = 600\text{mA} \tag{12}$$

Next, inductor value is calculated using Equation (11)

$$L = \frac{12-1.5-5}{600\text{mA}}\,7\mu\text{s} = 64\mu\text{H}. \tag{13}$$

Use the next lowest standard value (56µH).

Then pick R_{LIM} from the curve. For I_{PEAK} = 600mA, R_{LIM} = 56Ω.

Inductor Selection — Positive-to-Negative Converter

Figure 7 shows hookup for positive-to-negative conversion. All of the output power must come from the inductor. In this case,

$$P_L = \left(|V_{OUT}| + V_D\right)\left(I_{OUT}\right). \tag{14}$$

In this mode the switch is arranged in common collector or step-down mode. The switch drop can be modeled as a 0.75V source in series with a 0.65Ω resistor. When the switch closes, current in the inductor builds according to

$$I_L(t) = \frac{V_L}{R'}\left(1-e^{\frac{-R't}{L}}\right) \tag{15}$$

where R' = 0.65Ω + DCR_L
$V_L = V_{IN} - 0.75V$

As an example, suppose –5V at 50mA is to be generated from a 4.5V to 5.5V input. Recalling Equation (14),

$$P_L = \left(|-5V| + 0.5V\right)\left(50\text{mA}\right) = 275\text{mW}. \tag{16}$$

Energy required from the inductor is

$$\frac{P_L}{f_{OSC}} = \frac{275\text{mW}}{72\text{kHz}} = 3.8\mu\text{J}. \tag{17}$$

Picking an inductor value of 56µH with 0.2Ω DCR results in a peak switch current of

$$I_{PEAK} = \frac{(4.5V-0.75V)}{(0.65\Omega+0.2\Omega)}\left(1-e^{\frac{-0.85\Omega\bullet 7\mu s}{56\mu H}}\right) = 445\text{mA}. \tag{18}$$

Substituting I_{PEAK} into Equation (04) results in

$$E_L = \frac{1}{2}(56\mu\text{H})(0.445\text{A})^2 = 5.54\mu\text{J}. \tag{19}$$

Since 5.54µJ > 3.82µJ, the 56µH inductor will work.

With this relatively small input range, R_{LIM} is not usually necessary and the I_{LIM} pin can be tied directly to V_{IN}. As in the step-down case, peak switch current should be limited to ~650mA.

APPLICATIONS INFORMATION

Capacitor Selection

Selecting the right output capacitor is almost as important as selecting the right inductor. A poor choice for a filter capacitor can result in poor efficiency and/or high output ripple. Ordinary aluminum electrolytics, while inexpensive and readily available, may have unacceptably poor Equivalent Series Resistance (ESR) and ESL (inductance). There are low ESR aluminum capacitors on the market specifically designed for switch mode DC-DC converters which work much better than general-purpose units. Tantalum capacitors provide still better performance at more expense. We recommend OS-CON capacitors from Sanyo Corporation (San Diego, CA). These units are physically quite small and have extremely low ESR. To illustrate, Figures 1, 2, and 3 show the output voltage of an LT1111 based converter with three 100µF capacitors. The peak switch current is 500mA in all cases. Figure 1 shows a Sprague 501D, 25V aluminum capacitor. V_{OUT} jumps by over 120mV when the switch turns off, followed by a drop in voltage as the inductor dumps into the capacitor. This works out to be an ESR of over 240mΩ. Figure 2 shows the same circuit, but with a Sprague 150D, 20V tantalum capacitor replacing the aluminum unit. Output jump is now about 35mV, corresponding to an ESR of 70mΩ. Figure 3 shows the circuit with a 16V OS-CON unit. ESR is now only 20mΩ.

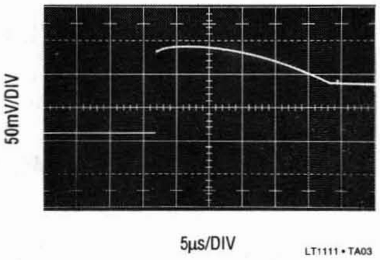


Figure 1. Aluminum

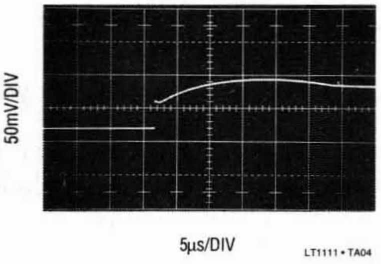


Figure 2. Tantalum

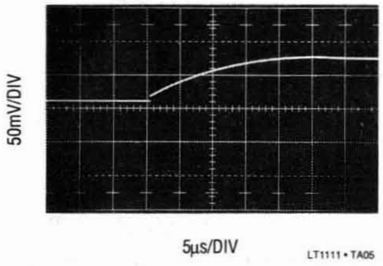


Figure 3. OS-CON

Diode Selection

Speed, forward drop, and leakage current are the three main considerations in selecting a catch diode for LT1111 converters. General purpose rectifiers such as the 1N4001 are *unsuitable* for use in *any* switching regulator application. Although they are rated at 1A, the switching time of a 1N4001 is in the 10µs-50µs range. At best, efficiency will be severely compromised when these diodes are used; at worst, the circuit may not work at all. Most LT1111 circuits will be well served by a 1N5818 Schottky diode, or its surface mount equivalent, the MBRS130T3. The combination of 500mV forward drop at 1A current, fast turn ON and turn OFF time, and 4µA to 10µA leakage current fit nicely with LT1111 requirements. At peak switch currents of 100mA or less, a 1N4148 signal diode may be used. This diode has leakage current in the 1nA-5nA range at 25°C and lower cost than a 1N5818. (You can also use them to get your circuit up and running, but beware of destroying the diode at 1A switch currents.)

Step-Up (Boost Mode) Operation

A step-up DC-DC converter delivers an output voltage higher than the input voltage. Step-up converters are *not* short circuit protected since there is a DC path from input to output.

The usual step-up configuration for the LT1111 is shown in Figure 4. The LT1111 first pulls SW1 low causing $V_{IN} - V_{CESAT}$ to appear across L1. A current then builds up in L1. At the end of the switch ON time the current in L1 is[1]:

$$I_{PEAK} = \frac{V_{IN}}{L} t_{ON} \qquad (20)$$

Note 1: This simple expression neglects the effect of switch and coil resistance. This is taken into account in the "Inductor Selection" section.

APPLICATIONS INFORMATION

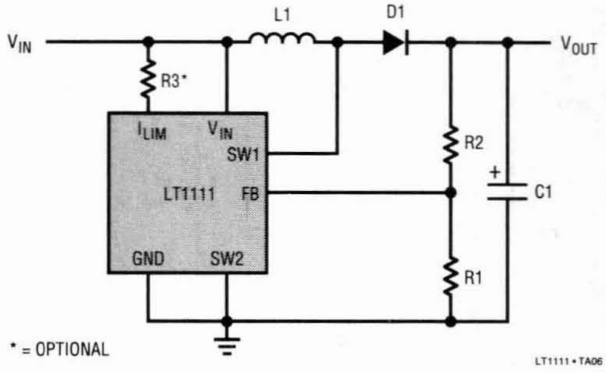


Figure 4. Step-Up Mode Hookup. Refer to Table 1 for Component Values

Immediately after switch turn off, the SW1 voltage pin starts to rise because current cannot instantaneously stop flowing in L1. When the voltage reaches $V_{OUT} + V_D$, the inductor current flows through D1 into C1, increasing V_{OUT}. This action is repeated as needed by the LT1111 to keep V_{FB} at the internal reference voltage of 1.25V. R1 and R2 set the output voltage according to the formula

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.25V). \tag{21}$$

Step-Down (Buck Mode) Operation

A step-down DC-DC converter converts a higher voltage to a lower voltage. The usual hookup for an LT1111 based step-down converter is shown in Figure 5.

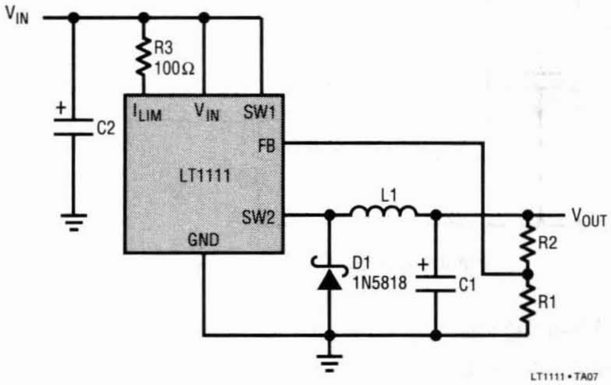


Figure 5. Step-Down Mode Hookup

When the switch turns on, SW2 pulls up to $V_{IN} - V_{SW}$. This puts a voltage across L1 equal to $V_{IN} - V_{SW} - V_{OUT}$, causing a current to build up in L1. At the end of the switch ON time, the current in L1 is equal to

$$I_{PEAK} = \frac{V_{IN} - V_{SW} - V_{OUT}}{L} t_{ON}. \tag{22}$$

When the switch turns off, the SW2 pin falls rapidly and actually goes below ground. D1 turns on when SW2 reaches 0.4V below ground. *D1 MUST BE A SCHOTTKY DIODE.* The voltage at SW2 must never be allowed to go below −0.5V. A silicon diode such as the 1N4933 will allow SW2 to go to −0.8V, causing potentially destructive power dissipation inside the LT1111. Output voltage is determined by

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.25V). \tag{23}$$

R3 programs switch current limit. This is especially important in applications where the input varies over a wide range. Without R3, the switch stays on for a fixed time each cycle. Under certain conditions the current in L1 can build up to excessive levels, exceeding the switch rating and/or saturating the inductor. The 100Ω resistor programs the switch to turn off when the current reaches approximately 700mA. When using the LT1111 in step-down mode, output voltage should be limited to 6.2V or less. Higher output voltages can be accommodated by inserting a 1N5818 diode in series with the SW2 pin (anode connected to SW2).

Higher Current Step-Down Operation

Output current can be increased by using a discrete PNP pass transistor as shown in Figure 6. R1 serves as a current limit sense. When the voltage drop across R1 equals a V_{BE}, the switch turns off. For temperature compensation a Schottky diode can be inserted in series with the I_{LIM} pin. This also lowers the maximum drop across R1 to $V_{BE} - V_D$, increasing efficiency. As shown, switch current is limited to 2A. Inductor value can be calculated based on formulas in the "Inductor Selection Step-Down

APPLICATIONS INFORMATION

Converter" section with the following conservative expression for V_{SW}:

$$V_{SW} = V_{R1} + V_{Q1SAT} \approx 1.0V \qquad (24)$$

R2 provides a current path to turn off Q1. R3 provides base drive to Q1. R4 and R5 set output voltage. A PMOS FET can be used in place of Q1 when V_{IN} is between 10V and 20V.

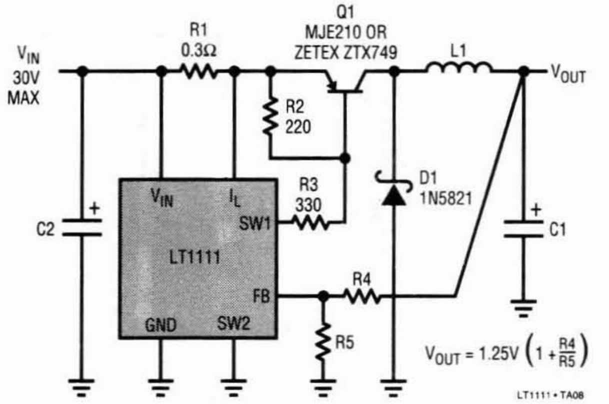
Inverting Configurations

The LT1111 can be configured as a positive-to-negative converter (Figure 7), or a negative-to-positive converter (Figure 8). In Figure 7, the arrangement is very similar to a step-down, except that the high side of the feedback is referred to ground. This level shifts the output negative. As in the step-down mode, D1 must be a Schottky diode, and $|V_{OUT}|$ should be less than 6.2V. More negative output voltages can be accommodated as in the prior section.

In Figure 8, the input is negative while the output is positive. In this configuration, the magnitude of the input voltage can be higher or lower than the output voltage. A level shift, provided by the PNP transistor, supplies proper polarity feedback information to the regulator.

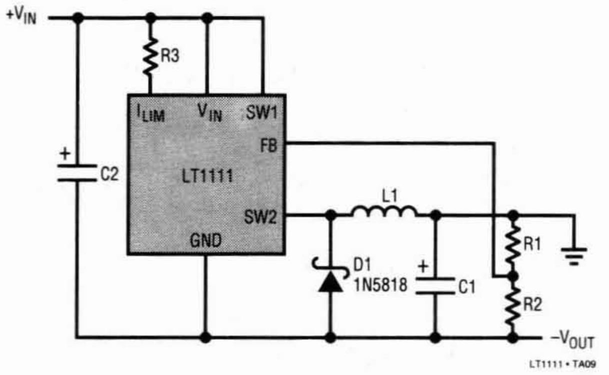
Using the I_{LIM} Pin

The LT1111 switch can be programmed to turn off at a set switch current, a feature not found on competing devices. This enables the input to vary over a wide range without exceeding the maximum switch rating or saturating the inductor. Consider the case where analysis shows the LT1111 must operate at an 800mA peak switch current with a 2.0V input. If V_{IN} rises to 4V, the peak switch current will rise to 1.6A, exceeding the maximum switch current rating. With the proper resistor selected (see the "Maximum Switch Current vs R_{LIM}" characteristic), the switch current will be limited to 800mA, even if the input voltage increases.



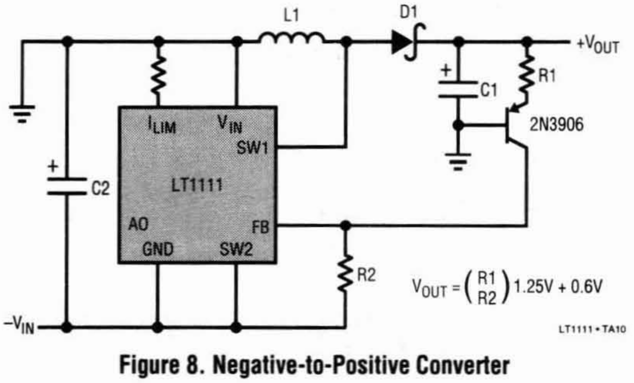
V_IN
30V
MAX
R1
0.3Ω
Q1
MJE210 OR
ZETEX ZTX749
L1
V_OUT
R2
220
R3
330
D1
1N5821
C2
C1
V_IN
I_L
SW1
LT1111
FB
GND
SW2
R4
R5
$V_{OUT} = 1.25V\left(1 + \frac{R4}{R5}\right)$
LT1111 • TA08

Figure 6. Q1 Permits Higher-Current Switching. LT1111 Functions as Controller.



+V_IN
R3
I_LIM
V_IN
SW1
FB
C2
LT1111
SW2
GND
L1
D1
1N5818
C1
R1
R2
−V_OUT
LT1111 • TA09

Figure 7. Positive-to-Negative Converter



L1
D1
+V_OUT
C1
R1
2N3906
I_LIM
V_IN
SW1
C2
LT1111
AO
FB
GND
SW2
R2
$V_{OUT} = \left(\frac{R1}{R2}\right) 1.25V + 0.6V$
−V_IN
LT1111 • TA10

Figure 8. Negative-to-Positive Converter

Another situation where the I_{LIM} feature is useful occurs when the device goes into continuous mode operation. This occurs in step-up mode when

$$\frac{V_{OUT} + V_{DIODE}}{V_{IN} - V_{SW}} < \frac{1}{1 - DC}. \qquad (25)$$

When the input and output voltages satisfy this relationship, inductor current does not go to zero during the switch OFF time. When the switch turns on again, the current ramp starts from the non-zero current level in the inductor just prior to switch turn on. As shown in Figure 9, the inductor current increases to a high level before the

APPLICATIONS INFORMATION

comparator turns off the oscillator. This high current can cause excessive output ripple and requires oversizing the output capacitor and inductor. With the I_{LIM} feature, however, the switch current turns off at a programmed level as shown in Figure 10, keeping output ripple to a minimum.

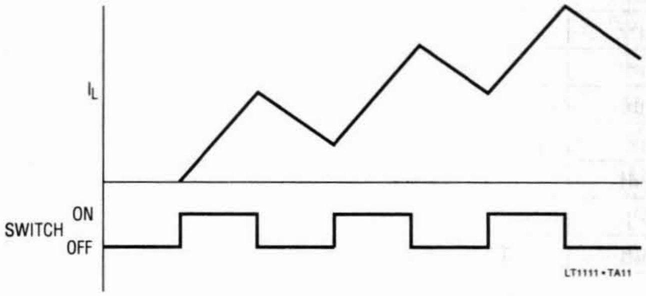


Figure 9. No Current Limit Causes Large Inductor Current Build-Up

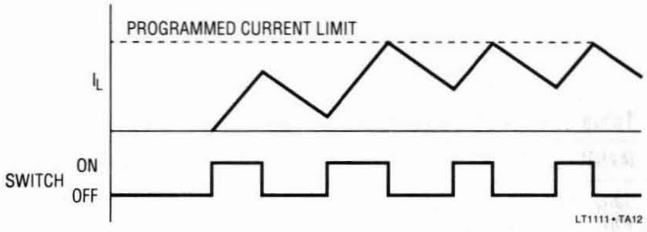


Figure 10. Current Limit Keeps Inductor Current Under Control

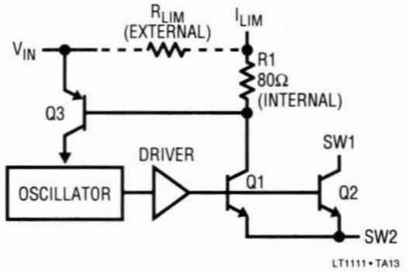


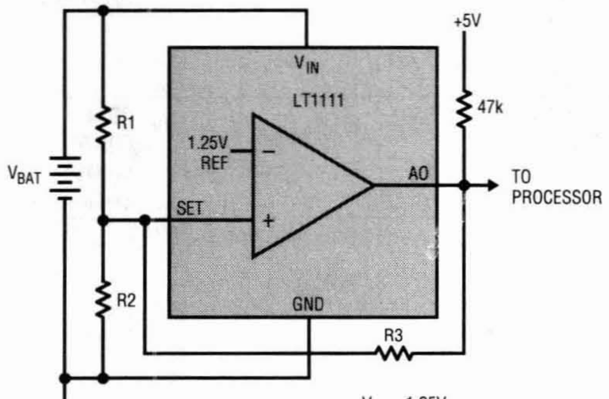
Figure 11. LT1111 Current Limit Circuitry

Figure 11 details current limit circuitry. Sense transistor Q1, whose base and emitter are paralleled with power switch Q2, is ratioed such that approximately 0.5% of Q2's collector current flows in Q1's collector. This current is passed through internal 80Ω resistor R1 and out through the I_{LIM} pin. The value of the external resistor connected between I_{LIM} and V_{IN} sets the current limit. When sufficient switch current flows to develop a V_{BE} across R1 + R_{LIM}, Q3 turns on and injects current into the oscillator, turning off the switch. Delay through this circuitry is approximately 1µs. The current trip point becomes less accurate for switch ON times less than 3µs. Resistor values programming switch ON time for 1µs or less will cause spurious response in the switch circuitry although the device will still maintain output regulation.

Using the Gain Block

The gain block (GB) on the LT1111 can be used as an error amplifier, low battery detector or linear post regulator. The gain block itself is a very simple PNP input op amp with an open collector NPN output. The negative input of the gain block is tied internally to the 1.25V reference. The positive input comes out on the SET pin.

Arrangement of the gain block as a low battery detector is straightforward. Figure 12 shows hookup. R1 and R2 need only be low enough in value so that the bias current of the SET input does not cause large errors. 33kΩ for R2 is adequate. R3 can be added to introduce a small amount of hysteresis. This will cause the gain block to "snap" when the trip point is reached. Values in the 1M-10M range are optimal. The addition of R3 will change the trip point, however.



$$R1 = \frac{V_{LB} - 1.25V}{35.1\mu A}$$

V_{LB} = BATTERY TRIP POINT
R2 = 33kΩ
R3 = 1.6MΩ

LT1111 • TA14

Figure 12. Setting Low Battery Detector Trip Point

APPLICATIONS INFORMATION

Table 1. Component Selection for Common Converters

INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT (MIN)	CIRCUIT FIGURE	INDUCTOR VALUE	INDUCTOR PART NUMBER	CAPACITOR VALUE	NOTES
2.0-3.1	5	90mA	4	15µH	S CD75-750K	33µF	*
2.0-3.1	5	10mA	4	47µH	S CD54-470K, C CTX50-1	10µF	
2.0-3.1	12	30mA	4	15µH	S CD75-150K	22µF	
2.0-3.1	12	10mA	4	47µH	S CD54-470K, C CTX50-1	10µF	
5	12	90mA	4	33µH	S CD75-330K	22µF	
5	12	30mA	4	47µH	S CD75-470K, C CTX50-1	15µF	
6.5-11	5	50mA	5	15µH	S CD54-150K	47µF	**
12-20	5	300mA	5	56µH	S CD105-560K, C CTX50-4	47µF	**
20-30	5	300mA	5	120µH	S CD105-121K, C CTX100-4	47µF	**
5	–5	75mA	6	56µH	S CD75-560K, C CTX50-4	47µF	
12	–5	250mA	6	120µH	S CD105-121K, C CTX100-4	100µF	**

S = Sumida

C = Coiltronics

* Add 47Ω from I_{LIM} to V_{IN}

** Add 220Ω from I_{LIM} to V_{IN}

Table 2. Inductor Manufacturers

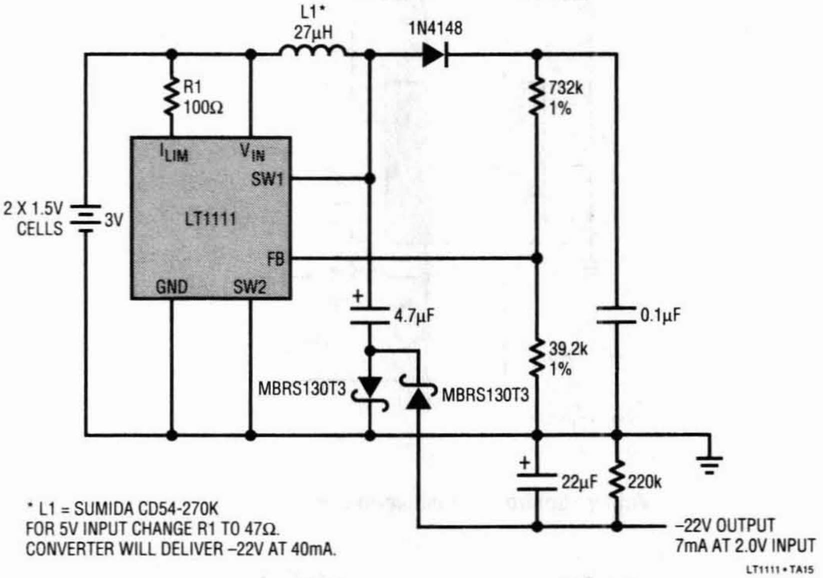
MANUFACTURER	PART NUMBERS
Coiltronics International 984 S.W. 13th Court Pompano Beach, FL 33069 305-781-8900	CTX100-4 Series Surface Mount
Toko America Incorporated 1250 Feehanville Drive Mount Prospect, IL 60056 312-297-0070	Type 8RBS
Sumida Electric Co. USA 708-956-0666	CD54 CDR74 CDR105 Surface Mount

Table 3. Capacitor Manufacturers

MANUFACTURER	PART NUMBERS
Sanyo Video Components 1201 Sanyo Avenue San Diego, CA 92073 619-661-6322	OS-CON Series
Nichicon America Corporation 927 East State Parkway Schaumberg, IL 60173 708-843-7500	PL Series
Sprague Electric Company Lower Main Street Sanford, ME 04073 207-324-4140	150D Solid Tantalums 550D Tantalex
Matsuo 714-969-2491	267 Series Surface Mount

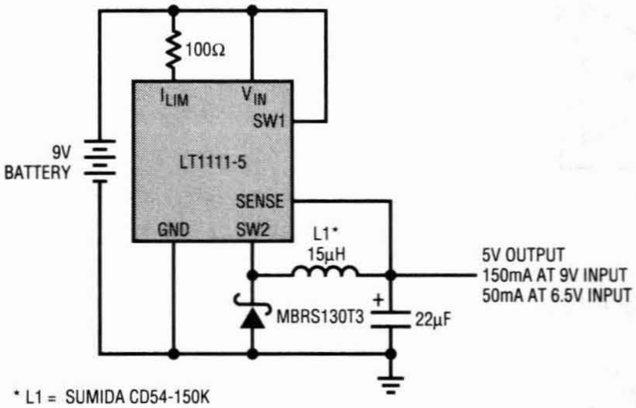
TYPICAL APPLICATIONS

3V to –22V LCD Bias Generator


L1*
27μH
1N4148
R1
100Ω
732k
1%
I_{LIM}
V_{IN}
SW1
2 X 1.5V
CELLS
3V
LT1111
FB
GND
SW2
4.7μF
0.1μF
39.2k
1%
MBRS130T3
MBRS130T3
22μF
220k
–22V OUTPUT
7mA AT 2.0V INPUT
LT1111 • TA15

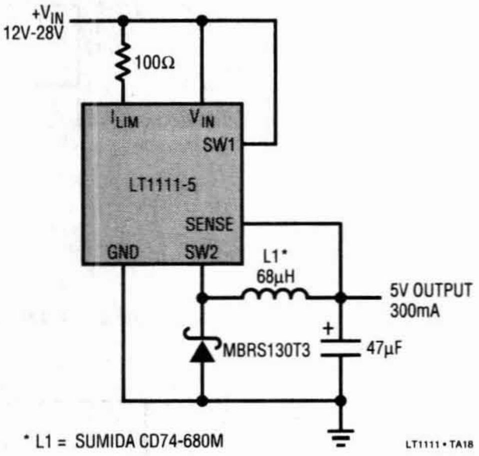
* L1 = SUMIDA CD54-270K
FOR 5V INPUT CHANGE R1 TO 47Ω.
CONVERTER WILL DELIVER –22V AT 40mA.

9V to 5V Step-Down Converter


100Ω
I_{LIM}
V_{IN}
SW1
9V
BATTERY
LT1111-5
SENSE
GND
SW2
L1*
15μH
5V OUTPUT
150mA AT 9V INPUT
50mA AT 6.5V INPUT
MBRS130T3
22μF
LT1111 • TA16

* L1 = SUMIDA CD54-150K

+20V to 5V Step-Down Converter

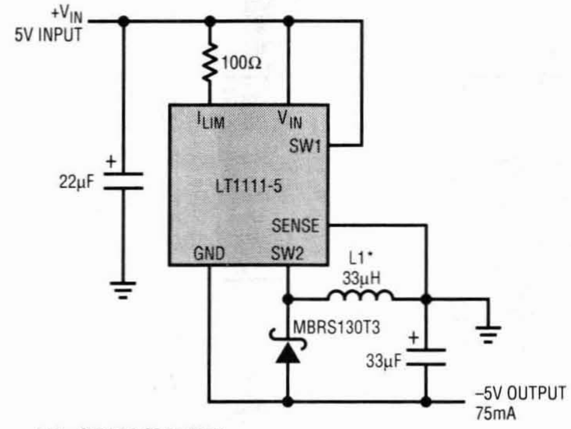

$+V_{IN}$
12V-28V
100Ω
I_{LIM}
V_{IN}
SW1
LT1111-5
SENSE
GND
SW2
L1*
68μH
5V OUTPUT
300mA
MBRS130T3
47μF
LT1111 • TA18

* L1 = SUMIDA CD74-680M

4

TYPICAL APPLICATIONS

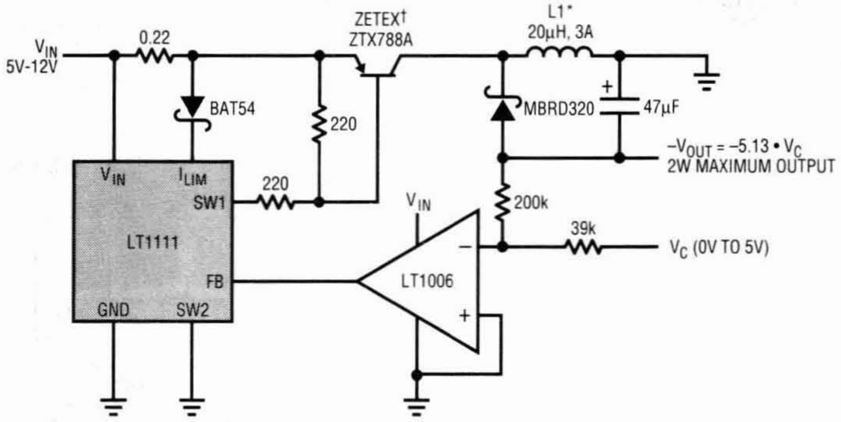
+5V to –5V Converter


+V_{IN}
5V INPUT
100Ω
22µF
I_{LIM}
V_{IN}
SW1
LT1111-5
SENSE
GND
SW2
L1*
33µH
MBRS130T3
33µF
–5V OUTPUT
75mA

* L1= SUMIDA CD54-330K

LT1111 • TA17

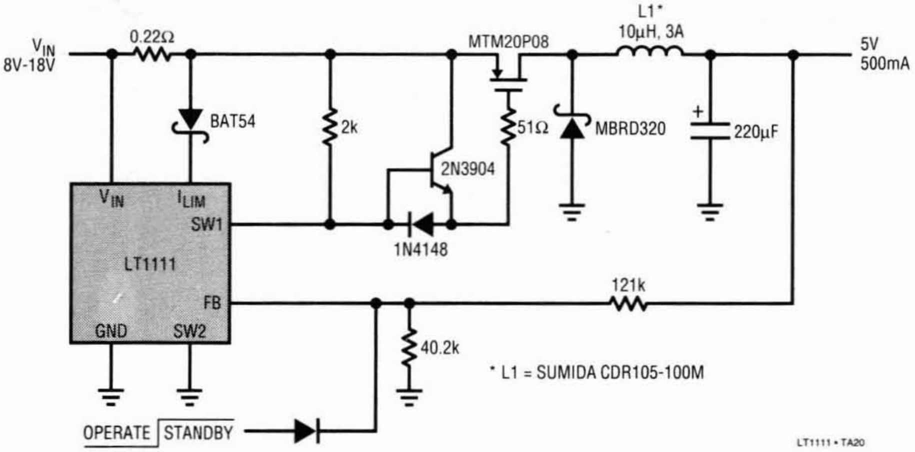
Voltage Controlled Positive-to-Negative Converter


V_{IN}
5V-12V
0.22
BAT54
ZETEX†
ZTX788A
220
L1*
20µH, 3A
MBRD320
47µF
$-V_{OUT} = -5.13 \bullet V_C$
2W MAXIMUM OUTPUT
V_{IN}
I_{LIM}
SW1
220
LT1111
FB
GND
SW2
V_{IN}
200k
39k
V_C (0V TO 5V)
LT1006

* L1 = COILTRONICS CTX20-4
† ZETEX INC. 516-543-7100

LT1111 • TA19

High Power, Low Quiescent Current Step-Down Converter


V_{IN}
8V-18V
0.22Ω
BAT54
2k
MTM20P08
51Ω
2N3904
1N4148
L1*
10µH, 3A
MBRD320
220µF
5V
500mA
V_{IN}
I_{LIM}
SW1
LT1111
FB
GND
SW2
121k
40.2k
OPERATE | STANDBY

* L1 = SUMIDA CDR105-100M

LT1111 • TA20

LT1173

Micropower
DC-DC Converter
Adjustable and Fixed 5V, 12V

FEATURES

- Operates at Supply Voltages From 2.0V to 30V
- Consumes Only 110µA Supply Current
- Works in Step-Up or Step-Down Mode
- Only Three External Components Required
- Low Battery Detector Comparator On-Chip
- User-Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space Saving 8-Pin MiniDIP or SO8 Package

APPLICATIONS

- Flash Memory Vpp Generators
- 3V to 5V, 5V to 12V Converters
- 9V to 5V, 12V to 5V Converters
- LCD Bias Generators
- Peripherals and Add-On Cards
- Battery Backup Supplies
- Laptop and Palmtop Computers
- Cellular Telephones
- Portable Instruments

DESCRIPTION

The LT1173 is a versatile micropower DC-DC converter. The device requires only three external components to deliver a fixed output of 5V or 12V. Supply voltage ranges from 2.0V to 12V in step-up mode and to 30V in step-down mode. The LT1173 functions equally well in step-up, step-down or inverting applications.

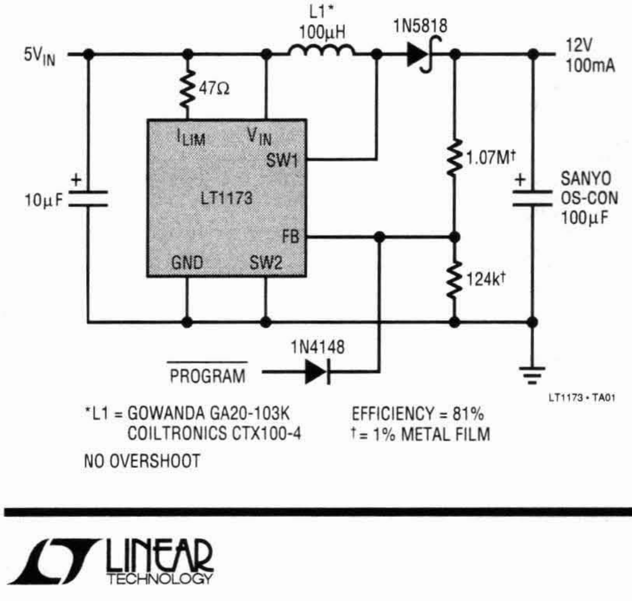
The LT1173 consumes just 110µA supply current at standby, making it ideal for applications where low quiescent current is important. The device can deliver 5V at 80mA from a 3V input in step-up mode or 5V at 200mA from a 12V input in step-down mode.

Switch current limit can be programmed with a single resistor. An auxiliary gain block can be configured as a low battery detector, linear post regulator, under voltage lockout circuit or error amplifier.

For input sources of less than 2V, use the LT1073.

TYPICAL APPLICATIONS

Logic Controlled Flash Memory Vpp Generator

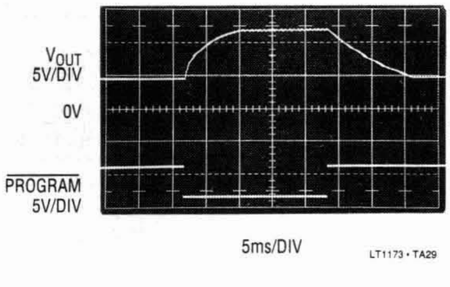


*L1 = GOWANDA GA20-103K
COILTRONICS CTX100-4

NO OVERSHOOT

EFFICIENCY = 81%
† = 1% METAL FILM

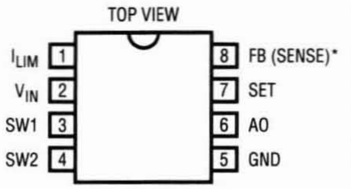
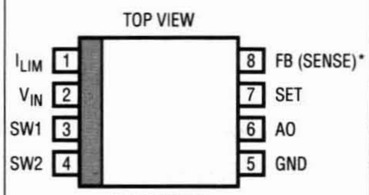
Vpp Output



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN})	36V
SW1 Pin Voltage (V_{SW1})	50V
SW2 Pin Voltage (V_{SW2})	–0.5V to V_{IN}
Feedback Pin Voltage (LT1173)	5V
Sense Pin Voltage (LT1173, -5, -12)	36V
Maximum Power Dissipation	500mW
Maximum Switch Current	1.5A
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature, (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW I_{LIM} 1 V_{IN} 2 SW1 3 SW2 4 8 FB (SENSE)* 7 SET 6 AO 5 GND N8 PACKAGE 8-LEAD PLASTIC DIP *FIXED VERSIONS LT1173 • PI01	LT1173CN8 LT1173CN8-5 LT1173CN8-12
 TOP VIEW I_{LIM} 1 V_{IN} 2 SW1 3 SW2 4 8 FB (SENSE)* 7 SET 6 AO 5 GND S8 PACKAGE 8-LEAD PLASTIC SOIC *FIXED VERSIONS LT1173 • PI02	LT1173CS8 LT1173CS8-5 LT1173CS8-12 **PART MARKING** 1173 17305 17312

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 3V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off		●		110	150	µA
I_Q	Quiescent Current, Boost Mode Configuration	No Load	LT1173-5			135		µA
			LT1173-12			250		µA
V_{IN}	Input Voltage	Step-Up Mode		●	2.0		12.6	V
		Step-Down Mode		●			30	V
	Comparator Trip Point Voltage	LT1173 (Note 1)		●	1.20	1.245	1.30	V
V_{OUT}	Output Sense Voltage	LT1173-5 (Note 2)		●	4.75	5.00	5.25	V
		LT1173-12 (Note 2)		●	11.4	12.0	12.6	V
	Comparator Hysteresis	LT1173		●		5	10	mV
	Output Hysteresis	LT1173-5		●		20	40	mV
		LT1173-12		●		50	100	mV
f_{OSC}	Oscillator Frequency			●	18	24	30	kHz
	Duty Cycle	Full Load		●	47	55	63	%
t_{ON}	Switch ON Time	I_{LIM} tied to V_{IN}		●	17	23	32	µs
	Feedback Pin Bias Current	LT1173, $V_{FB} = 0V$		●		10	50	nA
	Set Pin Bias Current	$V_{SET} = V_{REF}$		●		20	100	nA
V_{OL}	Gain Block Output Low	$I_{SINK} = 100\mu A$, $V_{SET} = 1.00V$		●		0.15	0.4	V
	Reference Line Regulation	$2.0V \le V_{IN} \le 5V$		●		0.2	0.4	%/V
		$5V \le V_{IN} \le 30V$		●		0.02	0.075	%/V
V_{SAT}	SW_{SAT} Voltage, Step-Up Mode	$V_{IN} = 3.0V$, $I_{SW} = 650mA$		●		0.5	0.65	V
		$V_{IN} = 5.0V$, $I_{SW} = 1A$				0.8	1.0	V
				●			1.4	V

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 3V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SAT}	SW_{SAT} Voltage, Step-Down Mode	$V_{IN} = 12V$, $I_{SW} = 650mA$			1.1	1.5	V
			●			1.7	V
A_V	Gain Block Gain	$R_L = 100k\Omega$ (Note 3)	●	400	1000		V/V
	Current Limit	220Ω to I_{LIM} to V_{IN}			400		mA
	Current Limit Temperature Coeff.		●		−0.3		%/°C
	Switch OFF Leakage Current	Measured at SW1 Pin			1	10	μA
V_{SW2}	Maximum Excursion Below GND	$I_{SW1} \leq 10\mu A$, Switch Off			−400	−350	mV

The ● denotes the specifications which apply over the full operating temperature range.

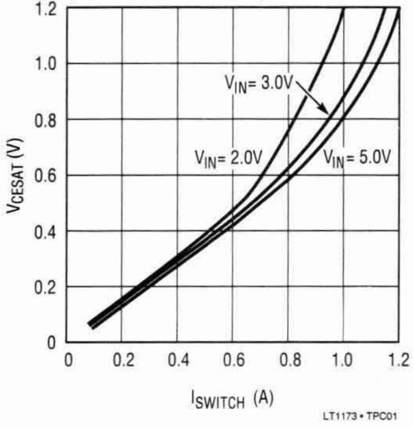
Note 1: This specification guarantees that both the high and low trip points of the comparator fall within the 1.20V to 1.30V range.

Note 2: The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed output versions will always be within the specified range.

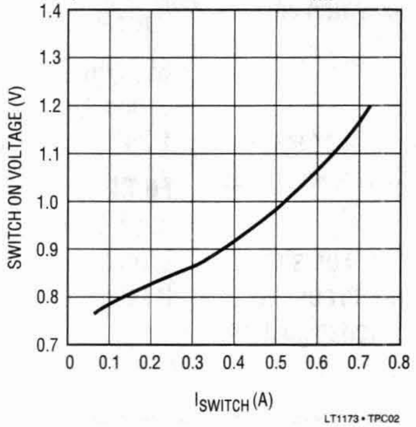
Note 3: 100kΩ resistor connected between a 5V source and the AO pin.

TYPICAL PERFORMANCE CHARACTERISTICS

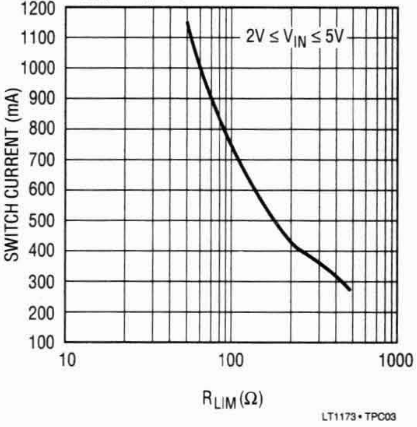
Saturation Voltage Step-Up Mode (SW2 Pin Grounded)



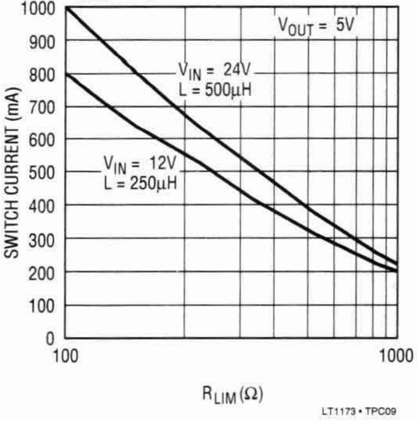
Switch ON Voltage Step-Down Mode (SW1 Pin Connected to V_{IN})



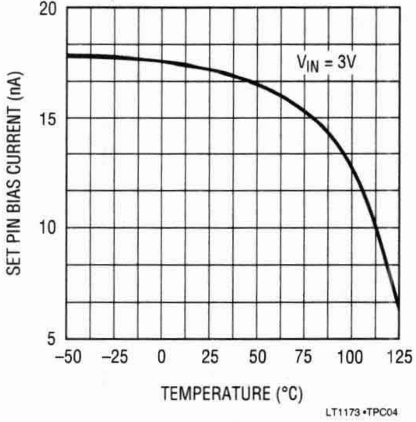
Maximum Switch Current vs R_{LIM} Step-Up Mode



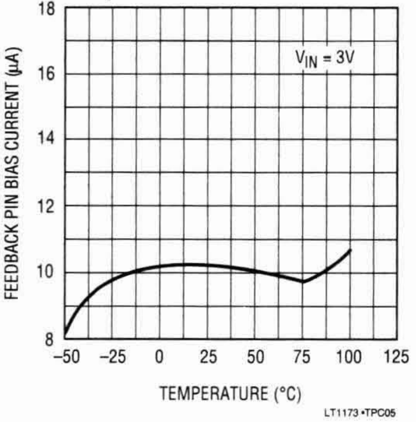
Maximum Switch Current vs R_{LIM} Step-Down Mode



Set Pin Bias Current vs Temperature

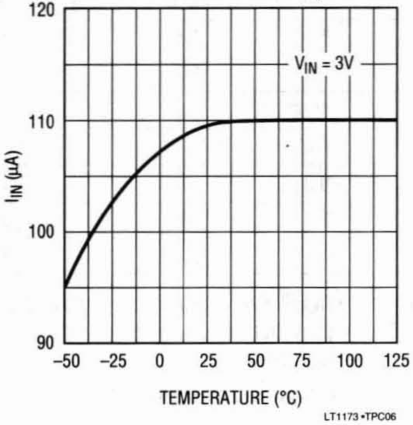


Feedback Pin Bias Current vs Temperature

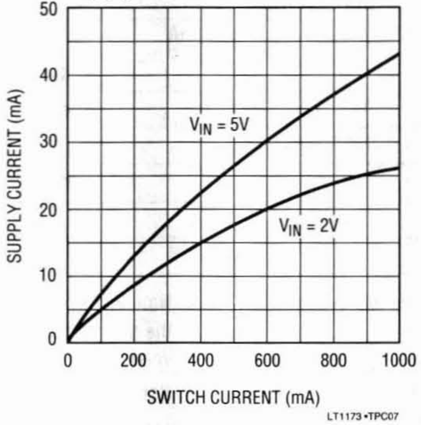


TYPICAL PERFORMANCE CHARACTERISTICS

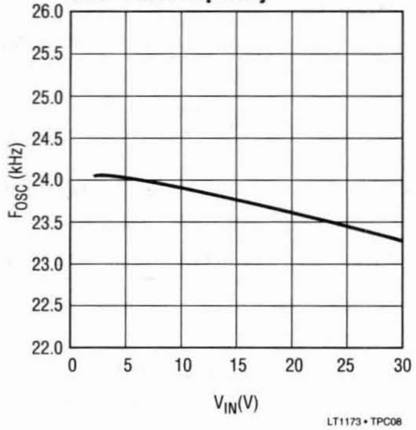
Quiescent Current vs Temperature



Supply Current vs Switch Current



Oscillator Frequency



PIN FUNCTIONS

I_{LIM} (Pin 1): Connect this pin to V_{IN} for normal use. Where lower current limit is desired, connect a resistor between I_{LIM} and V_{IN}. A 220Ω resistor will limit the switch current to approximately 400mA.

V_{IN} (Pin 2): Input supply voltage.

SW1 (Pin 3): Collector of power transistor. For step-up mode connect to inductor/diode. For step-down mode connect to V_{IN}.

SW2 (Pin 4): Emitter of power transistor. For step-up mode connect to ground. For step-down mode connect to inductor/diode. This pin must never be allowed to go more than a Schottky diode drop below ground.

GND (Pin 5): Ground.

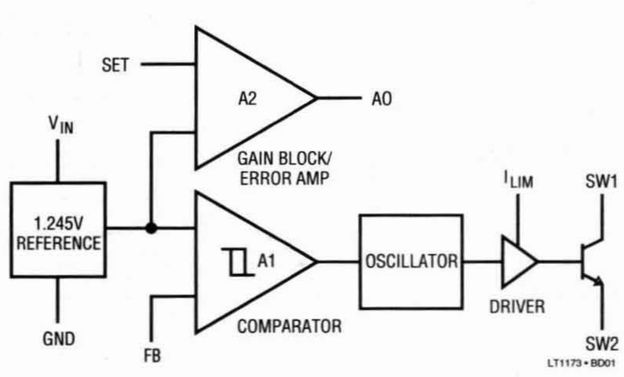
AO (Pin 6): Auxiliary Gain Block (GB) output. Open collector, can sink 100µA.

SET (Pin 7): GB input. GB is an op amp with positive input connected to SET pin and negative input connected to 1.245V reference.

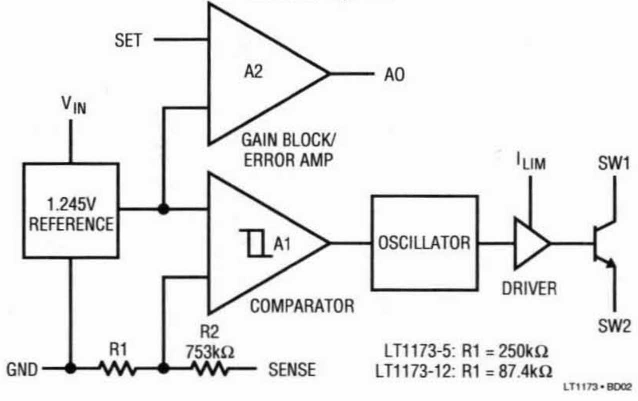
FB/SENSE (Pin 8): On the LT1173 (adjustable) this pin goes to the comparator input. On the LT1173-5 and LT1173-12, this pin goes to the internal application resistor that sets output voltage.

BLOCK DIAGRAMS

LT1173


SET
A2
AO
GAIN BLOCK/
ERROR AMP
V_{IN}
1.245V
REFERENCE
A1
COMPARATOR
OSCILLATOR
I_{LIM}
DRIVER
SW1
SW2
GND
FB
LT1173 • BD01

LT1173-5, -12


SET
A2
AO
GAIN BLOCK/
ERROR AMP
V_{IN}
1.245V
REFERENCE
A1
COMPARATOR
OSCILLATOR
I_{LIM}
DRIVER
SW1
SW2
GND
R1
R2
753kΩ
SENSE
LT1173-5: R1 = 250kΩ
LT1173-12: R1 = 87.4kΩ
LT1173 • BD02

LT1173 OPERATION

The LT1173 is a gated oscillator switcher. This type architecture has very low supply current because the switch is cycled only when the feedback pin voltage drops below the reference voltage. Circuit operation can best be understood by referring to the LT1173 block diagram. Comparator A1 compares the feedback pin voltage with the 1.245V reference voltage. When feedback drops below 1.245V, A1 switches on the 24kHz oscillator. The driver amplifier boosts the signal level to drive the output NPN power switch. An adaptive base drive circuit senses switch current and provides just enough base drive to ensure switch saturation without overdriving the switch, resulting in higher efficiency. The switch cycling action raises the output voltage and feedback pin voltage. When the feedback voltage is sufficient to trip A1, the oscillator is gated off. A small amount of hysteresis built into A1 ensures loop stability without external frequency compensation. When the comparator is low the oscillator and all high current circuitry is turned off, lowering device quiescent current to just 110µA, for the reference, A1 and A2.

The oscillator is set internally for 23µs ON time and 19µs OFF time, optimizing the device for circuits where V_{OUT} and V_{IN} differ by roughly a factor of 2. Examples include a 3V to 5V step-up converter or a 9V to 5V step-down converter.

A2 is a versatile gain block that can serve as a low battery detector, a linear post regulator, or drive an under voltage lockout circuit. The negative input of A2 is internally connected to the 1.245V reference. A resistor divider from V_{IN} to GND, with the mid-point connected to the SET pin provides the trip voltage in a low battery detector application. The gain block output (AO) can sink 100µA (use a 47k resistor pull-up to +5V). This line can signal a microcontroller that the battery voltage has dropped below the preset level.

A resistor connected between the I_{LIM} pin and V_{IN} sets maximum switch current. When the switch current exceeds the set value, the switch cycle is prematurely terminated. If current limit is not used, I_{LIM} should be tied directly to V_{IN}. Propagation delay through the current limit circuitry is approximately 2µs.

In step-up mode the switch emitter (SW2) is connected to ground and the switch collector (SW1) drives the inductor; in step-down mode the collector is connected to V_{IN} and the emitter drives the inductor.

The LT1173-5 and LT1173-12 are functionally identical to the LT1173. The -5 and -12 versions have on-chip voltage setting resistors for fixed 5V or 12V outputs. Pin 8 on the fixed versions should be connected to the output. No external resistors are needed.

APPLICATIONS INFORMATION

Measuring Input Current at Zero or Light Load

Obtaining meaningful numbers for quiescent current and efficiency at low output current involves understanding how the LT1173 operates. At very low or zero load current, the device is idling for seconds at a time. When the output voltage falls enough to trip the comparator, the power switch comes on for a few cycles until the output voltage rises sufficiently to overcome the comparator hysteresis. When the power switch is on, inductor current builds up to hundreds of milliamperes. Ordinary digital multimeters are not capable of measuring average current because of bandwidth and dynamic range limitations. A different approach is required to measure the 100µA off-state and 500mA on-state currents of the circuit.

Quiescent current can be accurately measured using the circuit in Figure 1. V_{SET} is set to the input voltage of the LT1173. The circuit must be "booted" by shorting V2 to V_{SET}. After the LT1173 output voltage has settled, disconnect the short. Input voltage is V2, and average input current can be calculated by this formula:

$$I_{IN} = \frac{V2 - V1}{100\Omega} \qquad (01)$$

APPLICATIONS INFORMATION

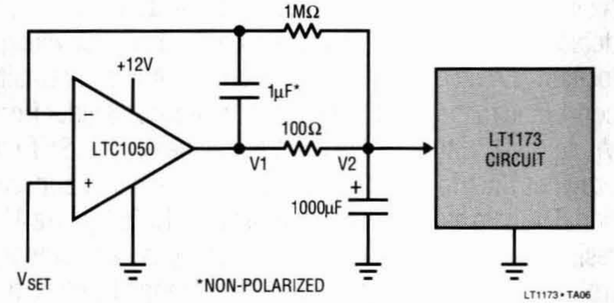


Figure 1. Test Circuit Measures No Load Quiescent Current of LT1073 Converter

Inductor Selection

A DC-DC converter operates by storing energy as magnetic flux in an inductor core, and then switching this energy into the load. Since it is flux, not charge, that is stored, the output voltage can be higher, lower, or opposite in polarity to the input voltage by choosing an appropriate switching topology. To operate as an efficient energy transfer element, the inductor must fulfill three requirements. First, the inductance must be low enough for the inductor to store adequate energy under the worst case condition of minimum input voltage and switch ON time. The inductance must also be high enough so that maximum current ratings of the LT1173 and inductor are not exceeded at the other worst case condition of maximum input voltage and ON time. Additionally, the inductor core must be able to store the required flux; i.e., it must not *saturate*. At power levels generally encountered with LT1173 based designs, small axial leaded units with saturation current ratings in the 300mA to 1A range (depending on application) are adequate. Lastly, the inductor must have sufficiently low DC resistance so that excessive power is not lost as heat in the windings. An additional consideration is Electro-Magnetic Interference (EMI). Toroid and pot core type inductors are recommended in applications where EMI must be kept to a minimum; for example, where there are sensitive analog circuitry or transducers nearby. Rod core types are a less expensive choice where EMI is not a problem.

Specifying a proper inductor for an application requires first establishing minimum and maximum input voltage, output voltage, and output current. In a step-up converter, the inductive events add to the input voltage to produce the output voltage. Power required from the inductor is determined by

$$P_L = (V_{OUT} + V_D - V_{IN})\,(I_{OUT}) \tag{02}$$

where V_D is the diode drop (0.5V for a 1N5818 Schottky). Energy required by the inductor per cycle must be equal or greater than

$$\frac{P_L}{F_{OSC}} \tag{03}$$

in order for the converter to regulate the output.

When the switch is closed, current in the inductor builds according to

$$I_L(t) = \frac{V_{IN}}{R'}\left(1 - e^{\frac{-R't}{L}}\right) \tag{04}$$

where R' is the sum of the switch equivalent resistance (0.8Ω typical at 25°C) and the inductor DC resistance. When the drop across the switch is small compared to V_{IN}, the simple lossless equation

$$I_L(t) = \frac{V_{IN}}{L}t \tag{05}$$

can be used. These equations assume that at t = 0, inductor current is zero. This situation is called "discontinuous mode operation" in switching regulator parlance. Setting "t" to the switch ON time from the LT1173 specification table (typically 23µs) will yield i_{PEAK} for a specific "L" and V_{IN}. Once i_{PEAK} is known, energy in the inductor at the end of the switch ON time can be calculated as

$$E_L = \frac{1}{2}Li_{PEAK}^2 \tag{06}$$

E_L must be greater than P_L/F_{OSC} for the converter to deliver the required power. For best efficiency i_{PEAK} should be kept to 1A or less. Higher switch currents will cause excessive drop across the switch resulting in reduced efficiency. In general, switch current should be held to as low a value as possible in order to keep switch, diode and inductor losses at a minimum.

APPLICATIONS INFORMATION

As an example, suppose 9V at 50mA is to be generated from a 3V input. Recalling Equation 02,

$$P_L = (9V + 0.5V - 3V)\ (50mA) = 325mW. \quad (07)$$

Energy required from the inductor is

$$\frac{P_L}{F_{OSC}} = \frac{325mW}{24kHz} = 13.5\mu J. \quad (08)$$

Picking an inductor value of 100μH with 0.2Ω DCR results in a peak switch current of

$$i_{PEAK} = \frac{3V}{1\Omega}\left(1 - e^{\frac{-1\Omega \bullet 23\mu s}{100\mu H}}\right) = 616mA. \quad (09)$$

Substituting i_{PEAK} into Equation 04 results in

$$E_L = \frac{1}{2}(100\mu H)(0.616A)^2 = 19.0\mu J. \quad (10)$$

Since 19μJ > 13.5μJ the 100μH inductor will work. This trial-and-error approach can be used to select the optimum inductor. Keep in mind the switch current maximum rating of 1.5A. If the calculated peak current exceeds this, consider using the LT1073. The 70% duty cycle of the LT1073 allows more energy per cycle to be stored in the inductor, resulting in more output power.

An inductor's energy storage capability is proportional to its physical size. If the size of the inductor is too large for a particular application, considerable size reduction is possible by using the LT1111. This device is pin compatible with the LT1173 but has a 72kHz oscillator, thereby reducing inductor and capacitor size requirements by a factor of three.

For both positive-to-negative (Figure 7) and negative-to-positive configurations (Figure 8), all the output power must be generated by the inductor. In these cases

$$P_L = (|V_{OUT}| + V_D)\ (I_{OUT}). \quad (11)$$

In the positive-to-negative case, switch drop can be modeled as a 0.75V voltage source in series with a 0.65Ω resistor so that

$$V_L = V_{IN} - 0.75V - I_L\ (0.65\Omega). \quad (12)$$

In the negative-to-positive case, the switch saturates and the 0.8Ω switch ON resistance value given for Equation 04 can be used. In both cases inductor design proceeds from Equation 03.

The step-down case is different than the preceeding three in that the inductor current flows through the load in a step-down topology (Figure 6). Current through the switch should be limited to ~650mA in step-down mode. This can be accomplished by using the I_{LIM} pin. With input voltages in the range of 12V to 25V, a 5V output at 300mA can be generated with a 220μH inductor and 100Ω resistor in series with the I_{LIM} pin. With a 20V to 30V input range, a 470μH inductor should be used along with the 100Ω resistor.

Capacitor Selection

Selecting the right output capacitor is almost as important as selecting the right inductor. A poor choice for a filter capacitor can result in poor efficiency and/or high output ripple. Ordinary aluminum electrolytics, while inexpensive and readily available, may have unacceptably poor equivalent series resistance (ESR) and ESL (inductance). There are low-ESR aluminum capacitors on the market specifically designed for switch mode DC-DC converters which work much better than general-purpose units. Tantalum capacitors provide still better performance at more expense. We recommend OS-CON capacitors from Sanyo Corporation (San Diego, CA). These units are physically quite small and have extremely low ESR. To illustrate, Figures 2, 3, and 4 show the output voltage of an LT1173 based converter with three 100μF capacitors. The peak switch current is 500mA in all cases. Figure 2 shows a Sprague 501D, 25V aluminum capacitor. V_{OUT} jumps by over 120mV when the switch turns off, followed by a drop in voltage as the inductor dumps into the capacitor. This works out to be an ESR of over 240mΩ. Figure 3 shows the same circuit, but with a Sprague 150D, 20V tantalum capacitor replacing the aluminum unit. Output jump is now about 35mV, corresponding to an ESR of 70mΩ. Figure 4 shows the circuit with a 16V OS-CON unit. ESR is now only 20mΩ.

APPLICATIONS INFORMATION

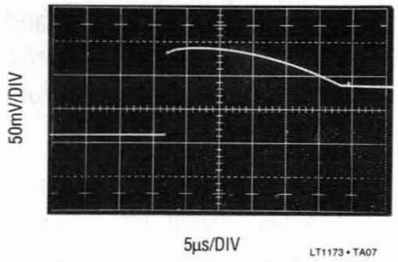


Figure 2. Aluminum

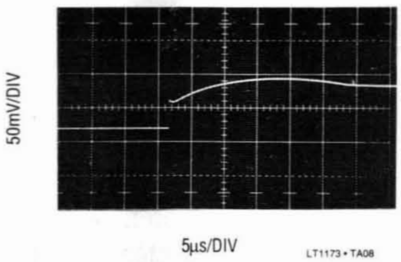


Figure 3. Tantalum

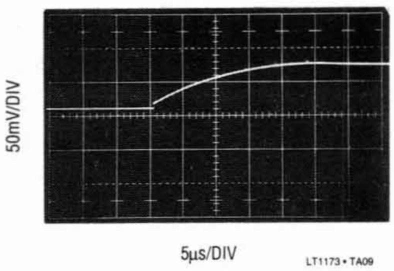


Figure 4. OS-CON

In very low power applications where every microampere is important, leakage current of the capacitor must be considered. The OS-CON units do have leakage current in the 5μA to 10μA range. If the load is also in the microampere range, a leaky capacitor will noticeably decrease efficiency. In this type application tantalum capacitors are the best choice, with typical leakage currents in the 1μA to 5μA range.

Diode Selection

Speed, forward drop, and leakage current are the three main considerations in selecting a catch diode for LT1173 converters. General purpose rectifiers such as the 1N4001 are *unsuitable* for use in *any* switching regulator application. Although they are rated at 1A, the switching time of a 1N4001 is in the 10μs-50μs range. At best, efficiency will be severely compromised when these diodes are used; at worst, the circuit may not work at all. Most LT1173 circuits will be well served by a 1N5818 Schottky diode. The combination of 500mV forward drop at 1A current, fast turn ON and turn OFF time, and 4μA to 10μA leakage current fit nicely with LT1173 requirements. At peak switch currents of 100mA or less, a 1N4148 signal diode may be used. This diode has leakage current in the 1nA-5nA range at 25°C and lower cost than a 1N5818. (You can also use them to get your circuit up and running, but beware of destroying the diode at 1A switch currents.) In situations where the load is intermittent and the LT1173 is idling most of the time, battery life can sometimes be extended by using a silicon diode such as the 1N4933, which can handle 1A but has leakage current of less than 1μA. Efficiency will decrease somewhat compared to a 1N5818 while delivering power, but the lower idle current may be more important.

Step-Up (Boost Mode) Operation

A step-up DC-DC converter delivers an output voltage higher than the input voltage. Step-up converters are *not* short circuit protected since there is a DC path from input to output.

The usual step-up configuration for the LT1173 is shown in Figure 5. The LT1173 first pulls SW1 low causing $V_{IN} - V_{CESAT}$ to appear across L1. A current then builds up in L1. At the end of the switch ON time the current in L1 is[1]:

$$i_{PEAK} = \frac{V_{IN}}{L} t_{ON} \qquad (13)$$

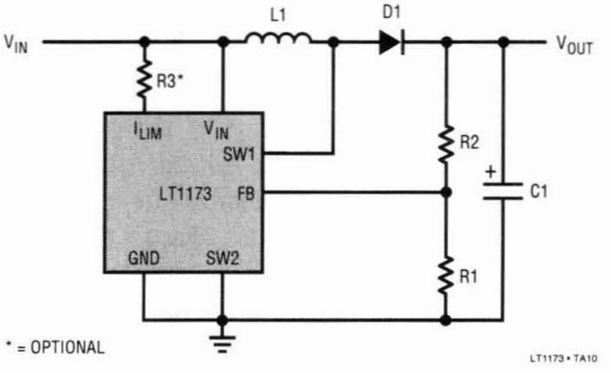


Figure 5. Step-Up Mode Hookup. Refer to Table 1 for Component Values

Immediately after switch turn off, the SW1 voltage pin starts to rise because current cannot instantaneously stop flowing in L1. When the voltage reaches $V_{OUT} + V_D$, the inductor current flows through D1 into C1, increasing V_{OUT}. This action is repeated as needed by the LT1173 to

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Note 1: This simple expression neglects the effect of switch and coil resistance. This is taken into account in the "Inductor Selection" section.

APPLICATIONS INFORMATION

keep V_{FB} at the internal reference voltage of 1.245V. R1 and R2 set the output voltage according to the formula

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.245V). \tag{14}$$

Step-Down (Buck Mode) Operation

A step-down DC-DC converter converts a higher voltage to a lower voltage. The usual hookup for an LT1173 based step-down converter is shown in Figure 6.

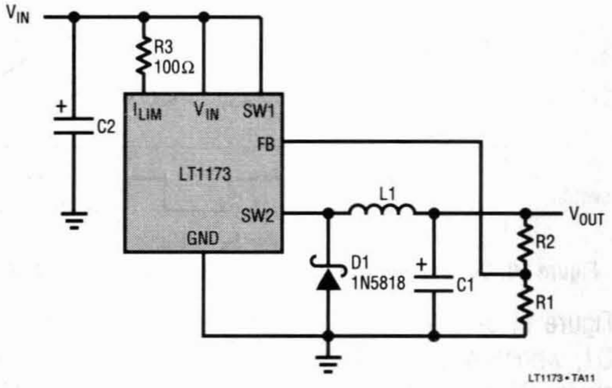


Figure 6. Step-Down Mode Hookup

When the switch turns on, SW2 pulls up to $V_{IN} - V_{SW}$. This puts a voltage across L1 equal to $V_{IN} - V_{SW} - V_{OUT}$, causing a current to build up in L1. At the end of the switch ON time, the current in L1 is equal to

$$i_{PEAK} = \frac{V_{IN} - V_{SW} - V_{OUT}}{L} t_{ON}. \tag{15}$$

When the switch turns off, the SW2 pin falls rapidly and actually goes below ground. D1 turns on when SW2 reaches 0.4V below ground. *D1 MUST BE A SCHOTTKY DIODE.* The voltage at SW2 must never be allowed to go below −0.5V. A silicon diode such as the 1N4933 will allow SW2 to go to −0.8V, causing potentially destructive power dissipation inside the LT1173. Output voltage is determined by

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right)(1.245V). \tag{16}$$

R3 programs switch current limit. This is especially important in applications where the input varies over a wide range. Without R3, the switch stays on for a fixed time each cycle. Under certain conditions the current in L1 can build up to excessive levels, exceeding the switch rating and/or saturating the inductor. The 100Ω resistor programs the switch to turn off when the current reaches approximately 800mA. When using the LT1173 in step-down mode, output voltage should be limited to 6.2V or less. Higher output voltages can be accommodated by inserting a 1N5818 diode in series with the SW2 pin (anode connected to SW2).

Inverting Configurations

The LT1173 can be configured as a positive-to-negative converter (Figure 7), or a negative-to-positive converter (Figure 8). In Figure 7, the arrangement is very similar to a step-down, except that the high side of the feedback is referred to ground. This level shifts the output negative. As in the step-down mode, D1 must be a Schottky diode, and $|V_{OUT}|$ should be less than 6.2V. More negative output voltages can be accomodated as in the prior section.

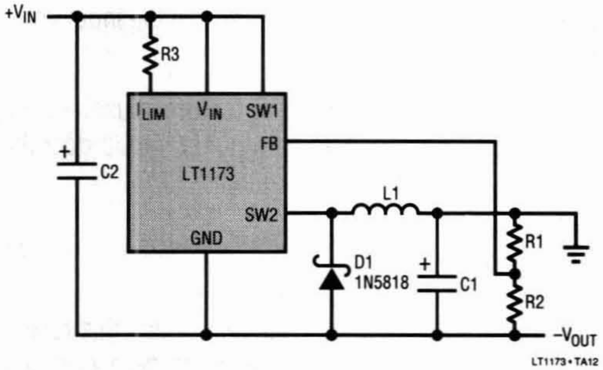


Figure 7. Positive-to-Negative Converter

In Figure 8, the input is negative while the output is positive. In this configuration, the magnitude of the input voltage can be higher or lower than the output voltage. A level shift, provided by the PNP transistor, supplies proper polarity feedback information to the regulator.

APPLICATIONS INFORMATION

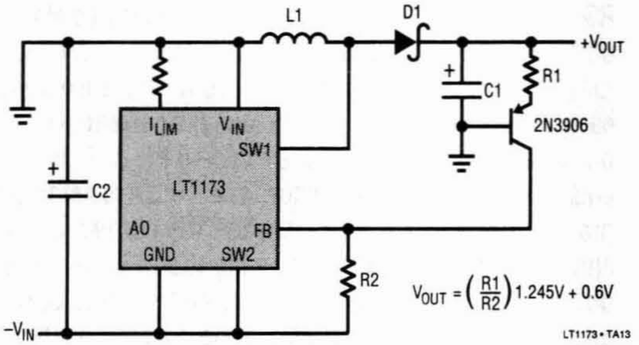


Figure 8. Negative-to-Positive Converter

Using the I_{LIM} Pin

The LT1173 switch can be programmed to turn off at a set switch current, a feature not found on competing devices. This enables the input to vary over a wide range without exceeding the maximum switch rating or saturating the inductor. Consider the case where analysis shows the LT1173 must operate at an 800mA peak switch current with a 2.0V input. If V_{IN} rises to 4V, the peak switch current will rise to 1.6A, exceeding the maximum switch current rating. With the proper resistor selected (see the "Maximum Switch Current vs R_{LIM}" characteristic), the switch current will be limited to 800mA, even if the input voltage increases.

Another situation where the I_{LIM} feature is useful occurs when the device goes into continuous mode operation. This occurs in step-up mode when

$$\frac{V_{OUT} + V_{DIODE}}{V_{IN} - V_{SW}} < \frac{1}{1 - DC}. \tag{17}$$

When the input and output voltages satisfy this relationship, inductor current does not go to zero during the switch OFF time. When the switch turns on again, the current ramp starts from the non-zero current level in the inductor just prior to switch turn on. As shown in Figure 9, the inductor current increases to a high level before the comparator turns off the oscillator. This high current can cause excessive output ripple and requires oversizing the output capacitor and inductor. With the I_{LIM} feature, however, the switch current turns off at a programmed level as shown in Figure 10, keeping output ripple to a minimum.

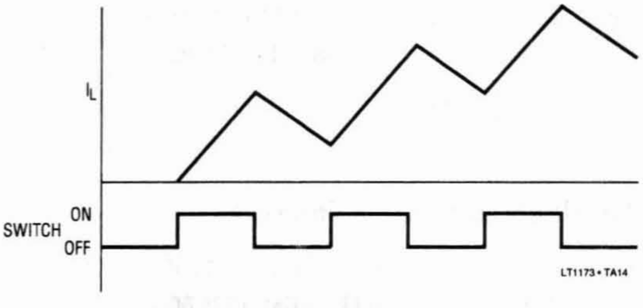


Figure 9. No Current Limit Causes Large Inductor Current Build-Up

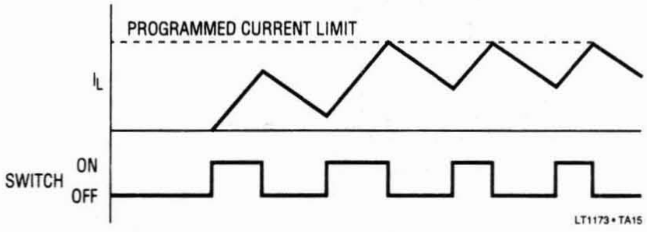


Figure 10. Current Limit Keeps Inductor Current Under Control

Figure 11 details current limit circuitry. Sense transistor Q1, whose base and emitter are paralleled with power switch Q2, is ratioed such that approximately 0.5% of Q2's collector current flows in Q1's collector. This current is passed through internal 80Ω resistor R1 and out through the I_{LIM} pin. The value of the external resistor connected between I_{LIM} and V_{IN} sets the current limit. When sufficient switch current flows to develop a V_{BE} across R1 + R_{LIM}, Q3 turns on and injects current into the oscillator, turning off the switch. Delay through this circuitry is approximately 2μs. The current trip point becomes less accurate for switch ON times less than 4μs. Resistor values programming switch ON time for 2μs or less will cause spurious response in the switch circuitry although the device will still maintain output regulation.

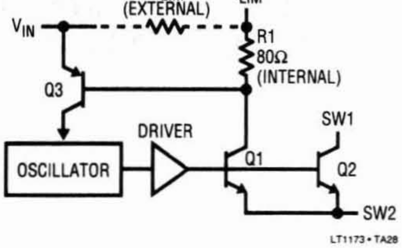


Figure 11. LT1173 Current Limit Circuitry

APPLICATIONS INFORMATION

Using the Gain Block

The gain block (GB) on the LT1173 can be used as an error amplifier, low battery detector or linear post regulator. The gain block itself is a very simple PNP input op amp with an open collector NPN output. The negative input of the gain block is tied internally to the 1.245V reference. The positive input comes out on the SET pin.

Arrangement of the gain block as a low battery detector is straightforward. Figure 12 shows hookup. R1 and R2 need only be low enough in value so that the bias current of the SET input does not cause large errors. 100kΩ for R2 is adequate. R3 can be added to introduce a small amount of hysteresis. This will cause the gain block to "snap" when the trip point is reached. Values in the 1M-10M range are optimal. The addition of R3 will change the trip point, however.

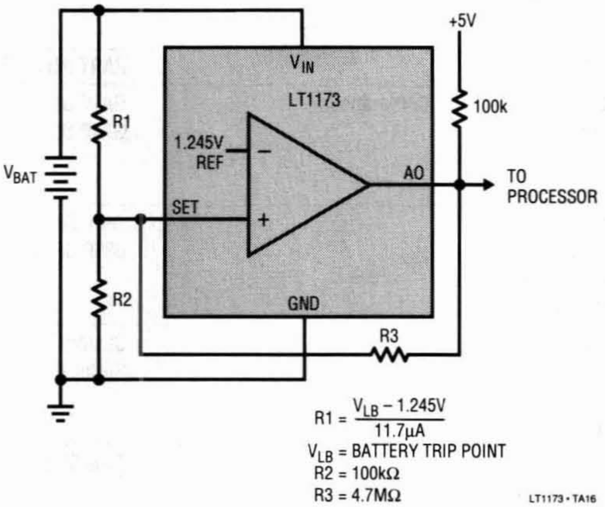


Figure 12. Setting Low Battery Detector Trip Point

Table 1. Component Selection for Common Converters

INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT (MIN)	CIRCUIT FIGURE	INDUCTOR VALUE	INDUCTOR PART NUMBER	CAPACITOR VALUE	NOTES
2.0-3.1	5	90mA	5	47μH	G GA10-472K, C CTX50-1	100μF	*
2.0-3.1	5	10mA	5	220μH	G GA10-223K, C CTX	22μF	
2.0-3.1	12	50mA	5	47μH	G GA10-472K, C CTX50-1	47μF	*
2.0-3.1	12	10mA	5	150μH	G GA10-153K	22μF	
5	12	90mA	5	120μH	G GA10-123K	100μF	
5	12	30mA	5	150μH	G GA10-153K	47μF	**
5	15	50mA	5	120μH	G GA10-123K C CTX100-4	47μF	
5	30	25mA	5	100μH	G GA10-103K, C CTX100-4	10μF, 50V	
6.5-9.5	5	50mA	6	47μH	G GA10-472K, C CTX50-1	100μF	**
12-20	5	300mA	6	220μH	G GA20-223K	220μF	**
20-30	5	300mA	6	470μH	G GA20-473K	470μF	**
5	−5	75mA	7	100μH	G GA10-103K, C CTX100-4	100μF	**
12	−5	250mA	7	470μH	G GA40-473K	220μF	**
−5	5	150mA	8	100μH	G GA10-103K, C CTX100-4	220μF	
−5	12	75mA	8	100μH	G GA10-103K, C CTX100-4	47μF	

G = Gowanda

C = Coiltronics

* Add 68Ω from I_{LIM} to V_{IN}

** Add 100Ω from I_{LIM} to V_{IN}

APPLICATIONS INFORMATION

Table 2. Inductor Manufacturers

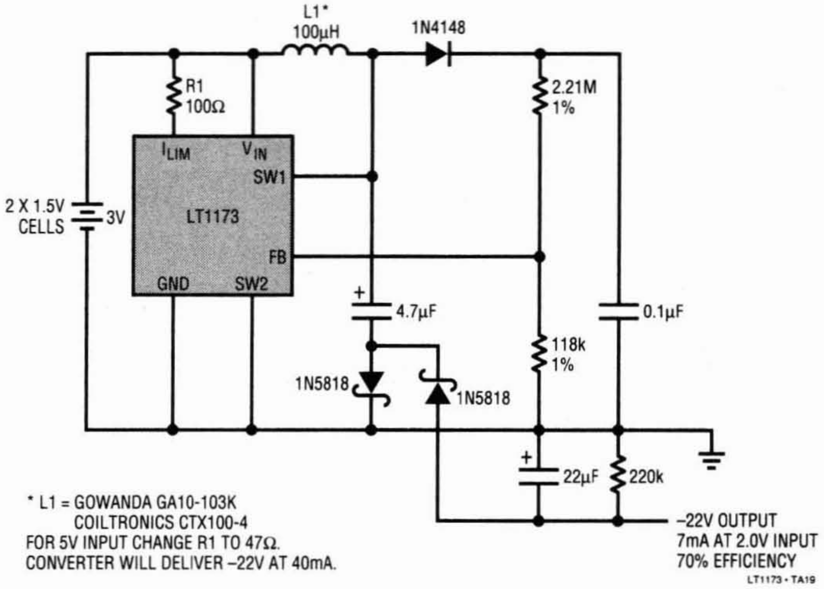
MANUFACTURER	PART NUMBERS
Gowanda Electronics Corporation 1 Industrial Place Gowanda, NY 14070 716-532-2234	GA10 Series GA40 Series
Caddell-Burns 258 East Second Street Mineola, NY 11501 516-746-2310	7300 Series 6860 Series
Coiltronics International 984 S.W. 13th Court Pompano Beach, FL 33069 305-781-8900	Custom Toroids Surface Mount
Toko America Incorporated 1250 Feehanville Drive Mount Prospect, IL 60056 312-297-0070	Type 8RBS
Renco Electronics Incorporated 60 Jefryn Boulevard, East Deer Park, NY 11729 800-645-5828	RL1283 RL1284

Table 3. Capacitor Manufacturers

MANUFACTURER	PART NUMBERS
Sanyo Video Components 1201 Sanyo Avenue San Diego, CA 92073 619-661-6322	OS-CON Series
Nichicon America Corporation 927 East State Parkway Schaumberg, IL 60173 708-843-7500	PL Series
Sprague Electric Company Lower Main Street Sanford, ME 04073 207-324-4140	150D Solid Tantalums 550D Tantalex

TYPICAL APPLICATIONS

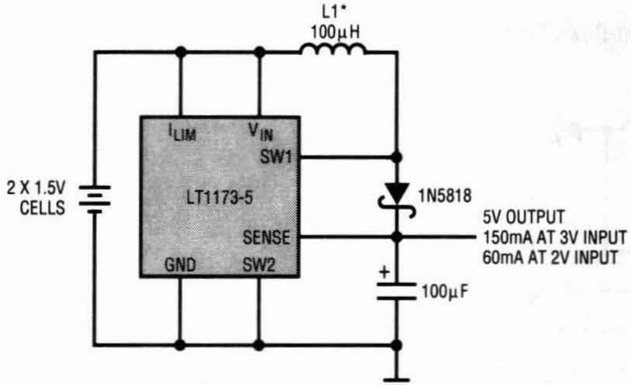
3V to –22V LCD Bias Generator


L1*
100μH
1N4148
R1
100Ω
2.21M
1%
I_{LIM}
V_{IN}
SW1
2 X 1.5V
CELLS
3V
LT1173
FB
GND
SW2
4.7μF
0.1μF
118k
1%
1N5818
1N5818
22μF
220k
–22V OUTPUT
7mA AT 2.0V INPUT
70% EFFICIENCY
LT1173 • TA19

* L1 = GOWANDA GA10-103K
COILTRONICS CTX100-4
FOR 5V INPUT CHANGE R1 TO 47Ω.
CONVERTER WILL DELIVER –22V AT 40mA.

TYPICAL APPLICATIONS

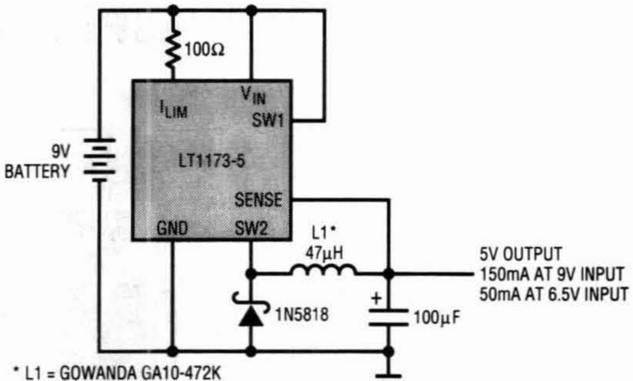
3V to 5V Step-Up Converter


L1*
100μH
2 X 1.5V
CELLS
ILIM
VIN
SW1
LT1173-5
SENSE
GND
SW2
1N5818
5V OUTPUT
150mA AT 3V INPUT
60mA AT 2V INPUT
100μF

* L1 = GOWANDA GA10-103K
COILTRONICS CTX100-1 (SURFACE MOUNT)

LT1173 • TA17

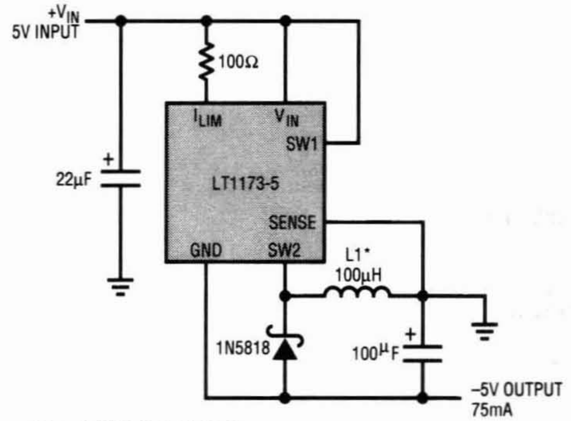
9V to 5V Step-Down Converter


100Ω
9V
BATTERY
ILIM
VIN
SW1
LT1173-5
SENSE
GND
SW2
L1*
47μH
1N5818
100μF
5V OUTPUT
150mA AT 9V INPUT
50mA AT 6.5V INPUT

* L1 = GOWANDA GA10-472K
COILTRONICS CTX50-1
FOR HIGHER OUTPUT CURRENTS SEE LT1073 DATASHEET

LT1173 • TA18

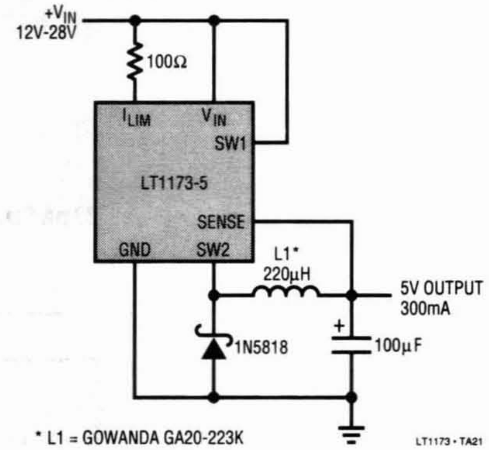
+5V to –5V Converter


+VIN
5V INPUT
100Ω
22μF
ILIM
VIN
SW1
LT1173-5
SENSE
GND
SW2
L1*
100μH
1N5818
100μF
–5V OUTPUT
75mA

* L1= GOWANDA GA10-103K
COILTRONICS CTX100-1

LT1173 • TA20

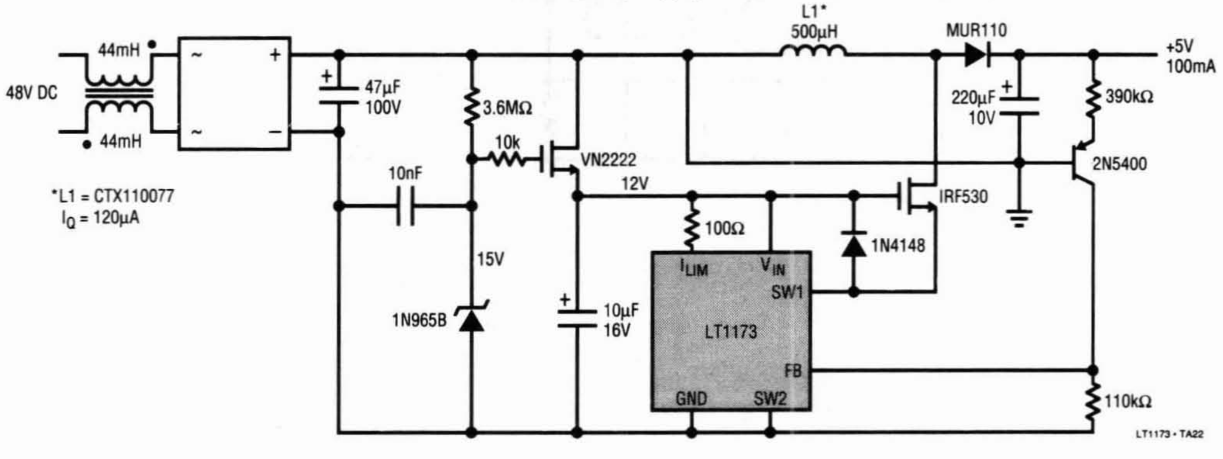
+20V to 5V Step-Down Converter


+VIN
12V-28V
100Ω
ILIM
VIN
SW1
LT1173-5
SENSE
GND
SW2
L1*
220μH
1N5818
100μF
5V OUTPUT
300mA

* L1 = GOWANDA GA20-223K

LT1173 • TA21

Telecom Supply

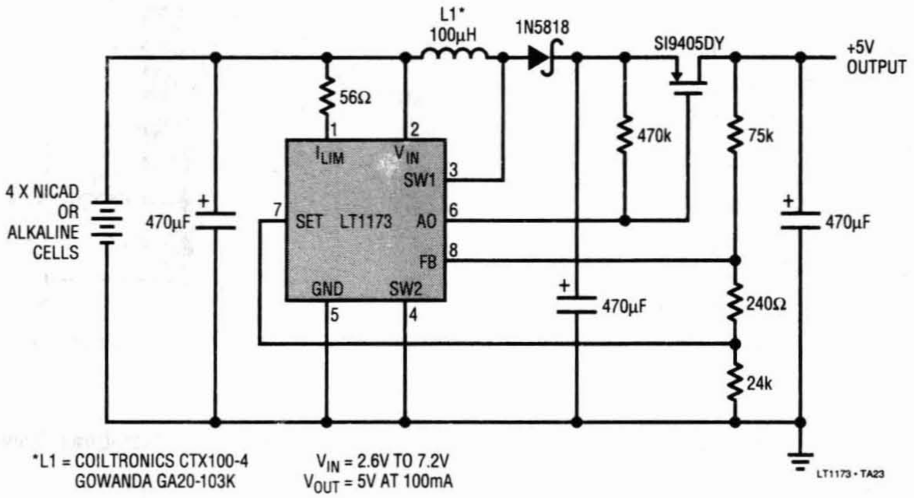

48V DC
44mH
44mH
~
+
~
–
47μF
100V
3.6MΩ
10k
VN2222
10nF
15V
1N965B
10μF
16V
12V
L1*
500μH
MUR110
+5V
100mA
220μF
10V
390kΩ
2N5400
IRF530
100Ω
1N4148
ILIM
VIN
SW1
LT1173
FB
GND
SW2
110kΩ

*L1 = CTX110077
I_Q = 120μA

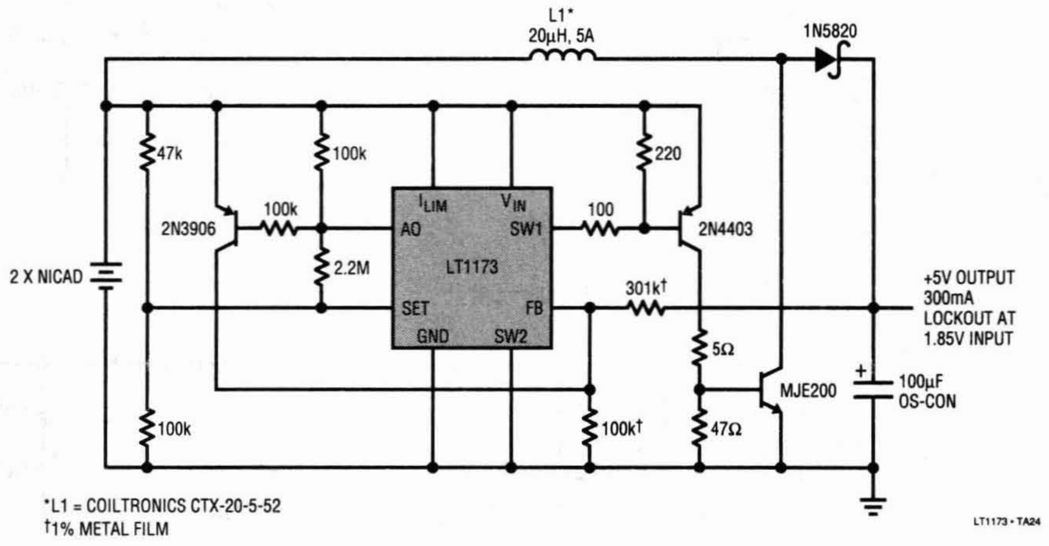
LT1173 • TA22

TYPICAL APPLICATIONS

"5 to 5" Step-Up or Step-Down Converter

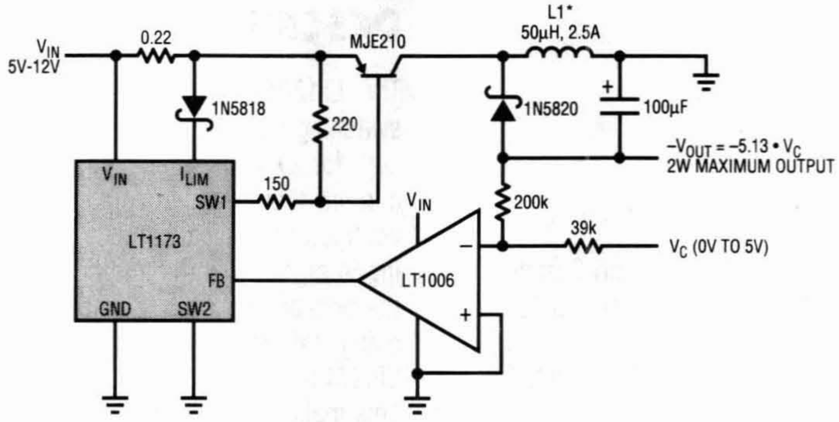

L1*
100μH
1N5818
SI9405DY
+5V
OUTPUT
56Ω
1
2
I_{LIM}
V_{IN}
3
SW1
4 X NICAD
OR
ALKALINE
CELLS
470μF
7
SET
LT1173
AO
6
470k
75k
470μF
FB
8
GND
SW2
5
4
470μF
240Ω
24k
*L1 = COILTRONICS CTX100-4
GOWANDA GA20-103K
V_{IN} = 2.6V TO 7.2V
V_{OUT} = 5V AT 100mA
LT1173 • TA23

2V to 5V at 300mA Step-Up Converter with Under Voltage Lockout


L1*
20μH, 5A
1N5820
47k
100k
220
I_{LIM}
V_{IN}
100k
100
2N3906
AO
SW1
2N4403
2.2M
LT1173
2 X NICAD
301k†
+5V OUTPUT
300mA
LOCKOUT AT
1.85V INPUT
SET
FB
GND
SW2
5Ω
MJE200
100μF
OS-CON
100k
100k†
47Ω
*L1 = COILTRONICS CTX-20-5-52
†1% METAL FILM
LT1173 • TA24

TYPICAL APPLICATIONS

Voltage Controlled Positive-to-Negative Converter

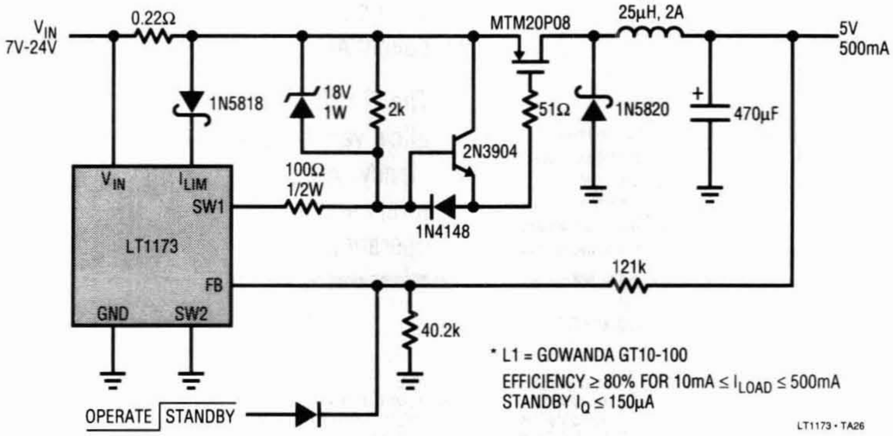


V_{IN}
5V-12V
0.22
1N5818
MJE210
220
L1*
50μH, 2.5A
1N5820
100μF
$-V_{OUT} = -5.13 \cdot V_C$
2W MAXIMUM OUTPUT
V_{IN}
I_{LIM}
SW1
150
LT1173
FB
GND
SW2
V_{IN}
200k
39k
V_C (0V TO 5V)
LT1006

* L1 = GOWANDA GT10-101

LT1173 • TA25

High Power, Low Quiescent Current Step-Down Converter



V_{IN}
7V-24V
0.22Ω
1N5818
18V
1W
2k
MTM20P08
51Ω
L1*
25μH, 2A
1N5820
470μF
5V
500mA
2N3904
100Ω
1/2W
1N4148
V_{IN}
I_{LIM}
SW1
LT1173
FB
GND
SW2
121k
40.2k
OPERATE | STANDBY

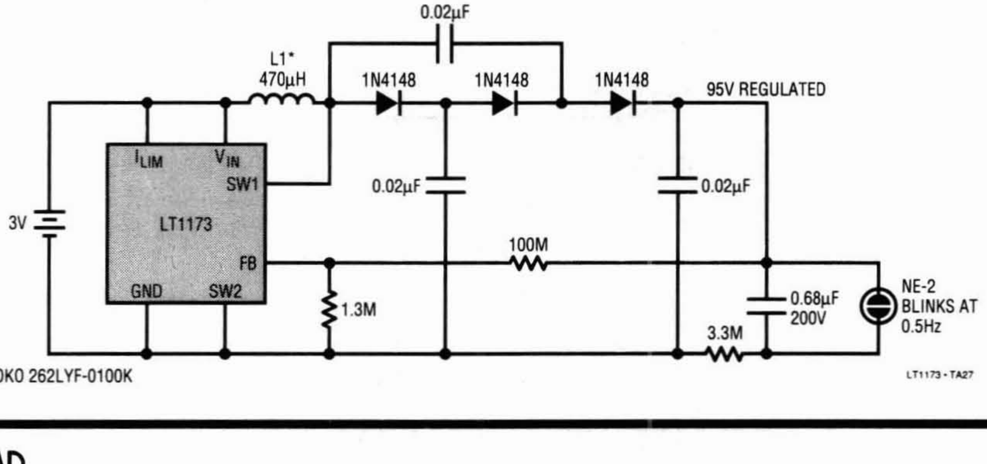
* L1 = GOWANDA GT10-100

EFFICIENCY ≥ 80% FOR 10mA ≤ I_{LOAD} ≤ 500mA

STANDBY I_Q ≤ 150μA

LT1173 • TA26

2 Cell Powered Neon Light Flasher



0.02μF
L1*
470μH
1N4148
1N4148
1N4148
95V REGULATED
I_{LIM}
V_{IN}
SW1
LT1173
FB
GND
SW2
3V
0.02μF
0.02μF
100M
1.3M
0.68μF
200V
3.3M
NE-2
BLINKS AT
0.5Hz

*TOKO 262LYF-0100K

LT1173 • TA27

LT1270/LT1270A

8A and 10A High Efficiency Switching Regulators

FEATURES

- Wide Input Voltage Range 3.5V-30V
- Low Quiescent Current—7mA
- Internal 8A Switch (10A for LT1270A)
- Very Few External Parts Required
- Self-Protected Against Overloads
- Shutdown Mode Draws Only 100µA Supply Current
- Flyback-Regulated Mode has Fully Floating Outputs
- Comes in Standard 5-Pin Package
- Can be Externally Synchronized (See LT1072 Data Sheet)

APPLICATIONS

- High Efficiency Buck Converter
- PC Power Supply with Multiple Outputs
- Battery Upconverter
- Negative to Positive Converter

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1270A/LT1270. Application circuits are included to show the capability of the LT1270A/LT1270. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1270A/LT1270 by factoring in the higher switch current rating and higher operating frequency.

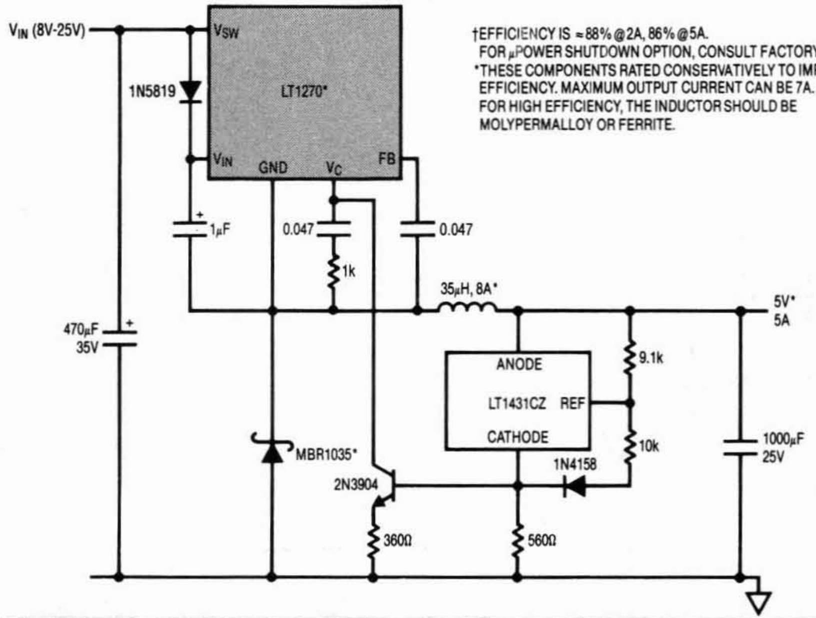
DESCRIPTION

The LT1270 and LT1270A are monolithic high power switching regulators. Identical to the popular LT1070, except for switching frequency (60kHz) and higher switch current, they can be operated in all standard switching configurations including buck, boost, flyback, and inverting. A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1270A/LT1270 to be built in a standard TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1270A/LT1270 operates with supply voltages from 3.5V to 30V, and draws only 7mA quiescent current. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

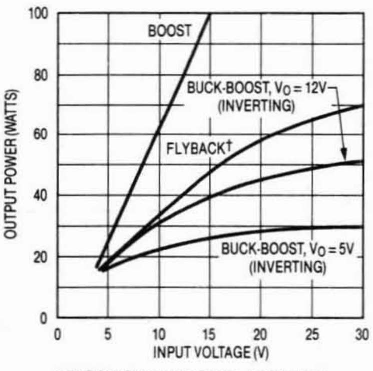
The LT1270A/LT1270 uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 100µA typical for standby operation.

High Efficiency† Buck Converter



†EFFICIENCY IS ≈88% @2A, 86% @5A.
FOR µPOWER SHUTDOWN OPTION, CONSULT FACTORY.
*THESE COMPONENTS RATED CONSERVATIVELY TO IMPROVE EFFICIENCY. MAXIMUM OUTPUT CURRENT CAN BE 7A.
FOR HIGH EFFICIENCY, THE INDUCTOR SHOULD BE MOLYPERMALLOY OR FERRITE.

Maximum Output Power*

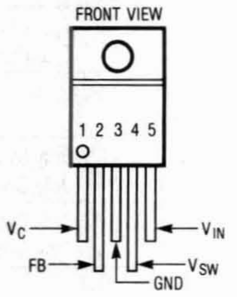


*MULTIPLY BY 1.2 FOR LT1270A. BUCK MODE OUTPUT POWER ≈ (7.5A) (V_{OUT})
†TRANSFORMER TURNS RATIO MUST BE OPTIMUM TO ACHIEVE FULL POWER.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
LT1270A/70 ....30V
Switch Output Voltage
LT1270A/70 ....60V
Feedback Pin Voltage (Transient, 1ms) ....±15V
Operating Junction Temperature Range
LT1270AC/LT1270C (Oper.) ....0°C to +125°C
LT1270AC/LT1270C (Short Ckt.) ....0°C to +140°C
Storage Temperature Range ....– 65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ....300°C

PACKAGE/ORDER INFORMATION



T PACKAGE
5-LEAD TO-220

ORDER PART NUMBER
LT1270CT LT1270ACT

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, $V_{FB} = V_{REF}$, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
		V_C = 0.8V	●	1.214	1.244	1.274	V
I_B	Feedback Input Current	$V_{FB} = V_{REF}$			350	750	nA
			●			1100	nA
gm	Error Amplifier Transconductance	$\Delta I_C = \pm 25\mu A$		3000	4400	6000	μmho
			●	2400		7000	μmho
	Error Amplifier Source or Sink Current	V_C = 1.5V		150	200	350	μA
			●	120		400	μA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V		1.8		2.3	V
		Lo Clamp, V_{FB} = 1.5V		0.25	0.38	0.52	V
	Reference Voltage Line Regulation	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.8V	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	$0.9V \le V_C \le 1.4V$		500	800		V/V
	Minimum Input Voltage		●		2.8	3.0	V
I_Q	Supply Current	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.6V			7	10	mA
	Control Pin Threshold	Duty Cycle = 0		0.8	0.9	1.08	V
			●	0.6		1.25	V
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage	$I_{FB} = 50\mu A$		15	16.3	17.6	V
			●	14		18	V
V_{FB}	Change in Flyback Reference Voltage	$0.05 \le I_{FB} \le 1mA$		4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	$I_{FB} = 50\mu A$ $3V \le V_{IN} \le V_{MAX}$			0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	$\Delta I_C = \pm 10\mu A$		150	300	650	μmho
	Flyback Amplifier Source and Sink Current	V_C = 0.6V Source	●	15	32	70	μA
		$I_{FB} = 50\mu A$ Sink	●	25	40	70	μA
BV	Output Switch Breakdown Voltage	$3V \le V_{IN} \le V_{MAX}$ LT1270A/LT1270 I_{SW} = 5mA	●	60	75		V

ELECTRICAL CHARACTERISTICS V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SAT}	Output Switch ON Resistance (Note 1, 3)	$T_J \leq 100°C$			0.12	0.18	Ω
		$T_J \leq 125°C$				0.22	Ω
	Control Voltage to Switch Current Transconductance				12		A/V
I_{LIM}	Switch Current Limit (LT1270) (Note 3)	Duty Cycle = 50% $T_J \leq 100°C$	●	8		16	A
		Duty Cycle = 80% $T_J \leq 100°C$	●	6		14	A
I_{LIM}	Switch Current Limit (LT1270A) (Note 3)	Duty Cycle = 50% $T_J \leq 100°C$	●	10		16	A
		Duty Cycle = 80% $T_J \leq 100°C$	●	7.5		14	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch ON Time				25	40	mA/A
f	Switching Frequency			50	60	70	kHz
			●	50		70	kHz
DC (max)	Maximum Switch Duty Cycle			80	92	95	%
	Flyback Sense Delay Time				1.5		µs
	Shutdown Mode Supply Current	$3V \leq V_{IN} \leq V_{MAX}$, V_C = 0.05V			100	400	µA
	Shutdown Mode Threshold Voltage	$3V \leq V_{IN} \leq V_{MAX}$		100	150	250	mV
			●	50		300	mV

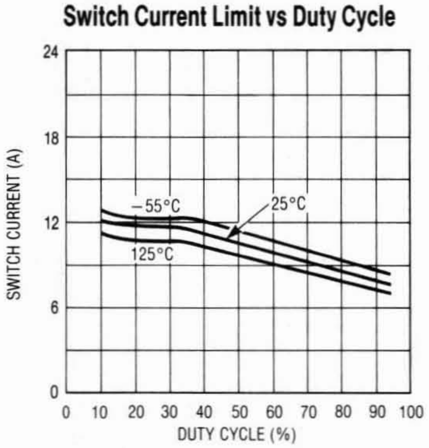
The ● denotes the specifications which apply over the full operating temperature range.

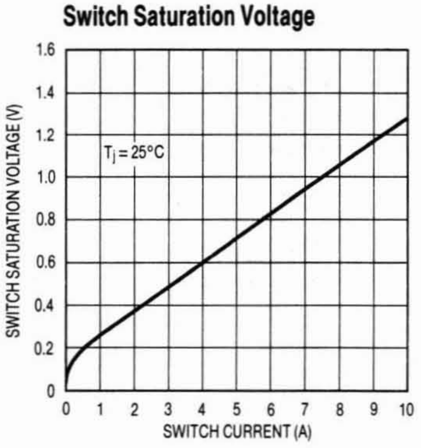
Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by I_{LIM} = 6.67 (1.7 – DC) for the LT1270 and I_{LIM} = 8.33 (1.7 – DC) for the LT1270A.

Note 3: Minimum current limit is reduced by 0.5A at 125°C. 100°C test limits are guaranteed by correlation to 125°C tests.

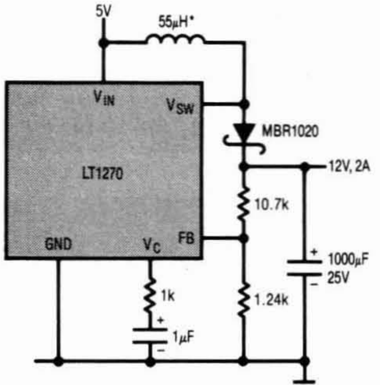
TYPICAL PERFORMANCE CHARACTERISTICS


Switch Current Limit vs Duty Cycle


Switch Saturation Voltage

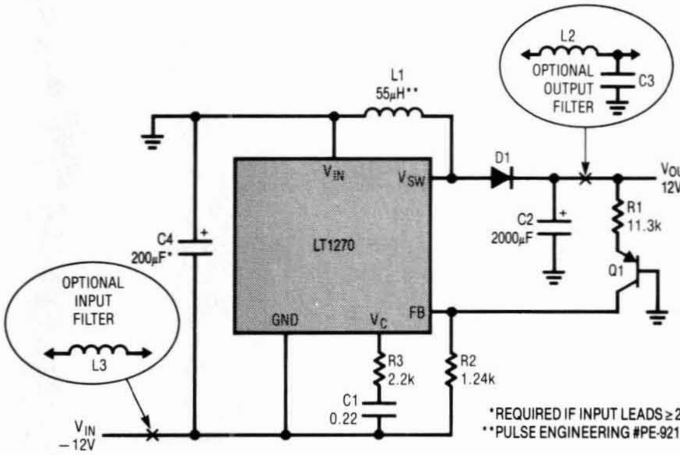
TYPICAL APPLICATIONS

Boost Converter (5V to 12V)


5V
55μH*
V_IN
V_SW
LT1270
MBR1020
12V, 2A
10.7k
GND
V_C
FB
1000μF
25V
1k
1.24k
1μF

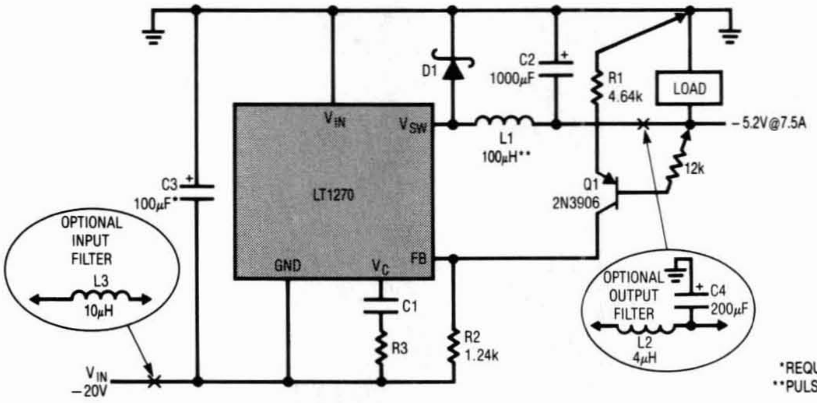
*PULSE ENGINEERING #PE-92116

Negative to Positive Buck-Boost Converter


L2
OPTIONAL
OUTPUT
FILTER
C3
L1
55μH**
V_IN
V_SW
D1
V_OUT
12V, 3A
R1
11.3k
C2
2000μF
Q1
C4
200μF*
LT1270
OPTIONAL
INPUT
FILTER
L3
GND
V_C
FB
R3
2.2k
R2
1.24k
C1
0.22
V_IN
–12V

*REQUIRED IF INPUT LEADS ≥ 2"
**PULSE ENGINEERING #PE-92116

Negative Buck Converter


D1
C2
1000μF
R1
4.64k
LOAD
V_IN
V_SW
–5.2V@7.5A
L1
100μH**
12k
Q1
2N3906
C3
100μF*
LT1270
OPTIONAL
INPUT
FILTER
L3
10μH
GND
V_C
FB
C1
R3
R2
1.24k
OPTIONAL
OUTPUT
FILTER
C4
200μF
L2
4μH
V_IN
–20V

*REQUIRED IF INPUT LEADS ≥ 2"
**PULSE ENGINEERING #PE-92115

NOTES

SECTION 5—INTERFACE

SECTION 5—INTERFACE

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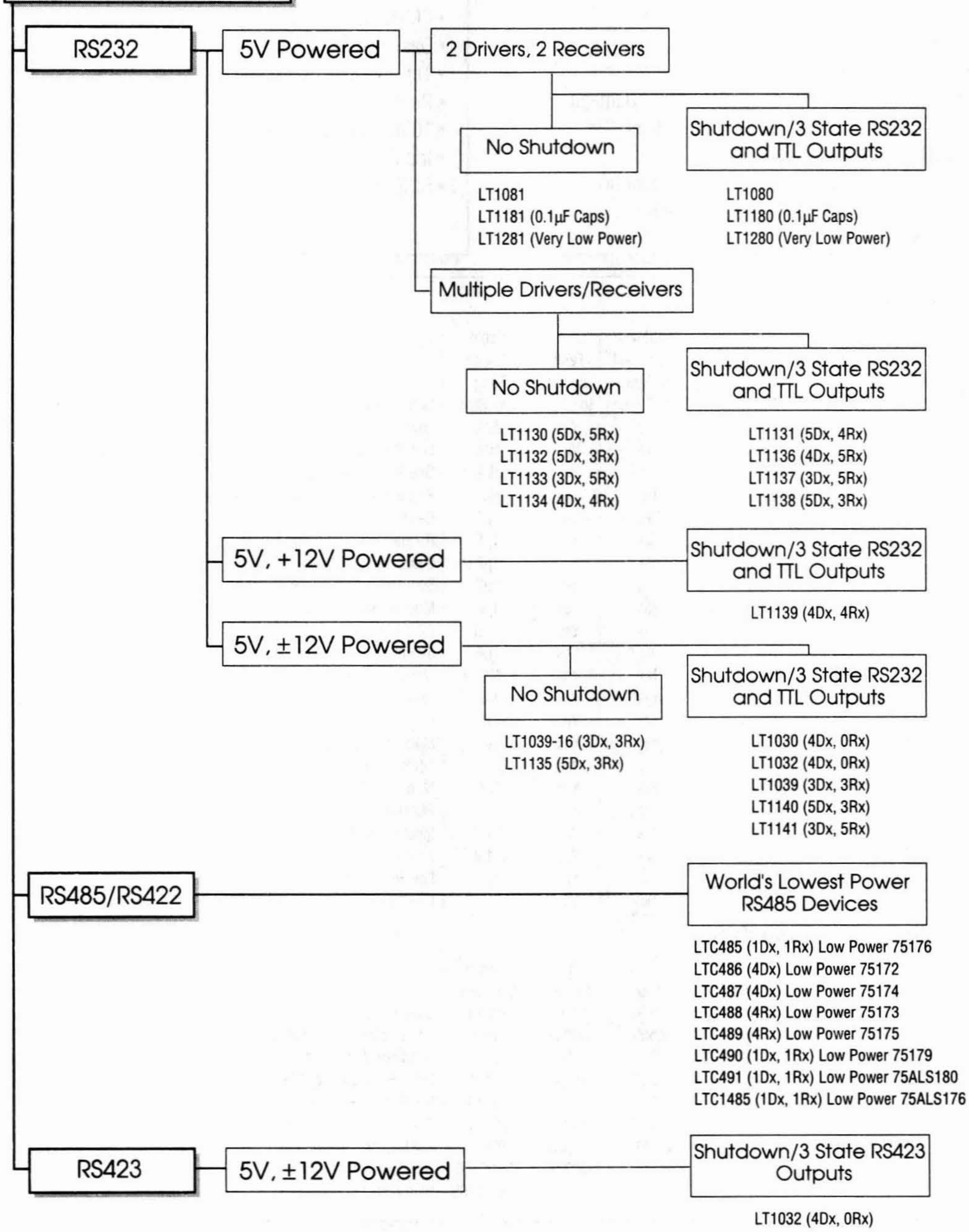
PROPRIETARY PRODUCTS

LTC485, Low Power RS485 Interface Transceiver 5-6
LTC486, Quad Low Power RS485 Driver 5-16
LTC487, Quad Low Power RS485 Driver 5-24
LTC488, Quad RS485 Line Receiver 13-3
LTC489, Quad RS485 Line Receiver 13-12
LTC490, Low Power RS485 Interface Transceiver 5-32
LTC491, Low Power RS485 Interface Transceiver 5-40
LT1137A, Advanced Low Power 5V RS232 Transceiver with Small Capacitors 13-52
LT1237, 5V RS232 Transceiver with Advanced Power Management and One Receiver Active in SHUTDOWN 13-76
LT1330, 5V RS232 Transceiver with 3V Logic Interface and One Receiver Active in SHUTDOWN 13-99
LTC1485, High Speed RS485 Interface Transceiver 13-103

Interface


RS232
5V Powered
2 Drivers, 2 Receivers
No Shutdown
LT1081
LT1181 (0.1μF Caps)
LT1281 (Very Low Power)
Shutdown/3 State RS232 and TTL Outputs
LT1080
LT1180 (0.1μF Caps)
LT1280 (Very Low Power)
Multiple Drivers/Receivers
No Shutdown
LT1130 (5Dx, 5Rx)
LT1132 (5Dx, 3Rx)
LT1133 (3Dx, 5Rx)
LT1134 (4Dx, 4Rx)
Shutdown/3 State RS232 and TTL Outputs
LT1131 (5Dx, 4Rx)
LT1136 (4Dx, 5Rx)
LT1137 (3Dx, 5Rx)
LT1138 (5Dx, 3Rx)
5V, +12V Powered
Shutdown/3 State RS232 and TTL Outputs
LT1139 (4Dx, 4Rx)
5V, ±12V Powered
No Shutdown
LT1039-16 (3Dx, 3Rx)
LT1135 (5Dx, 3Rx)
Shutdown/3 State RS232 and TTL Outputs
LT1030 (4Dx, 0Rx)
LT1032 (4Dx, 0Rx)
LT1039 (3Dx, 3Rx)
LT1140 (5Dx, 3Rx)
LT1141 (3Dx, 5Rx)
RS485/RS422
World's Lowest Power RS485 Devices
LTC485 (1Dx, 1Rx) Low Power 75176
LTC486 (4Dx) Low Power 75172
LTC487 (4Dx) Low Power 75174
LTC488 (4Rx) Low Power 75173
LTC489 (4Rx) Low Power 75175
LTC490 (1Dx, 1Rx) Low Power 75179
LTC491 (1Dx, 1Rx) Low Power 75ALS180
LTC1485 (1Dx, 1Rx) Low Power 75ALS176
RS423
5V, ±12V Powered
Shutdown/3 State RS423 Outputs
LT1032 (4Dx, 0Rx)

RS232 & RS422 INTERFACE SOLUTIONS

RS232 Family Features

- Absolutely No Latch Up
- CMOS Comparable Low Power (80mW)
- Operates From a Single 5V Supply
- Operates Over 64K Baud
- Outputs Can be Forced to ±30V Without Damage
- Three State RS232 and TTL Outputs When Off
- Only Needs 1μF Capacitors
- Easy PC Board Layout (Flow Through Pinout)
- 1μA Supply Current in Shutdown Mode
- SOIC Available

RS485 Family Features

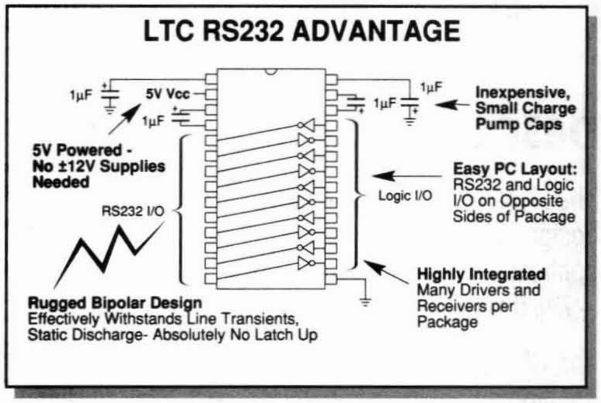
- Ultra Low Power
- CMOS Schottky Process
- Designed for RS485 and RS422 Applications
- Three State RS485 Outputs When Shutdown
- Power Up/Down Glitch Free Outputs
- 10MB Operation (LTC486-489, LTC1485)
- Industry Standard Pinouts
- SOIC Available

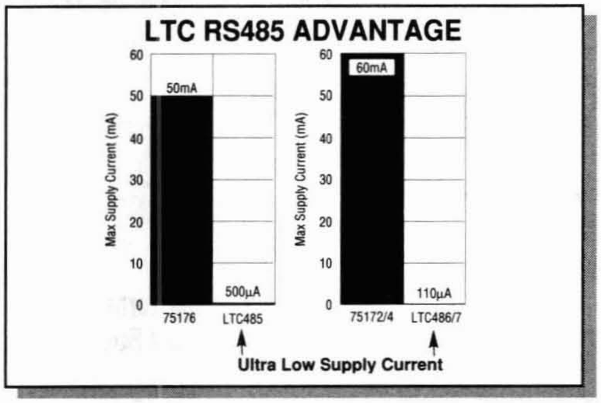
RS232 Interface

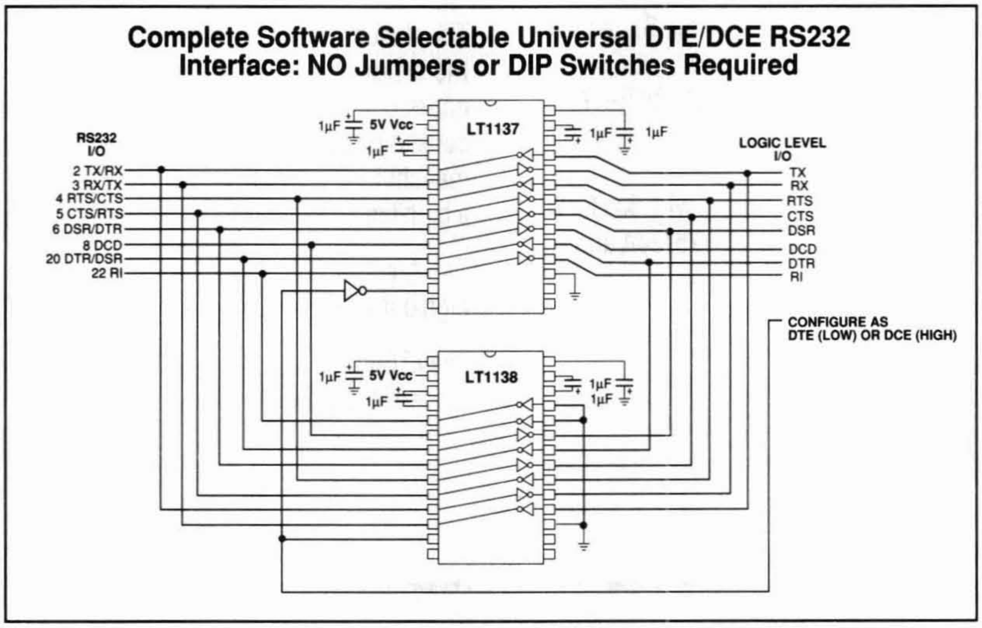
Drivers	Receivers	Supplies Required	Shutdown/ RS232 and TTL Three-State Outputs	Fault Tolerant to ±25V	Req'd Charge Pump Cap Size	Comments	Part Number
4	0	±12 V	Yes	Yes	N/A	Low Pwr 1488 Upgrade	LT1030
4	0	±12 V	Yes	Yes	N/A	Low Pwr 1488 Upgrade Also supports RS423	LT1032
3	3	+5V, ±12 V	Yes	Yes	N/A	One Receiver Active in Shutdown	LT1039
3	3	+5V, ±12 V	No	Yes	N/A	Rugged MC145406 Replacement	LT1039-16
2	2	+5V	Yes	Yes	1μF	General Purpose Interface	LT1080
2	2	+5V	No	Yes	1μF	Rugged MAX232 Replacement	LT1081
5	5	+5V	No	Yes	1μF	Synchronous Communications	LT1130
5	4	+5V	Yes	Yes	1μF	Synchronous Modem/DCE Interface	LT1131
5	3	+5V	No	Yes	1μF	Modem/DCE Interface	LT1132
3	5	+5V	No	Yes	0.1μF	PC/DTE Interface	LT1133
4	4	+5V	No	Yes	1μF	5V only 1488/1489 Replacement	LT1134
5	3	+5V, ±12 V	No	Yes	N/A	Modem/DCE Interface	LT1135
4	5	+5V	Yes	Yes	1μF	Synchronous PC/DTE Interface	LT1136
3	5	+5V	Yes	Yes	0.1μF	PC/ DTE Interface	LT1137
5	3	+5V	Yes	Yes	1μF	Modem/ DCE Interface	LT1138
4	4	+5V, ±12 V	Yes	Yes	1μF	1488/1489 Replacement	LT1139
5	3	+5V, ±12 V	Yes	Yes	N/A	Modem/ DCE Interface	LT1140
3	5	+5V, ±12 V	Yes	Yes	N/A	PC/ DTE Interface	LT1141
2	2	+5V	Yes	Yes	0.1μF	Ideal For Surface Mount	LT1180
2	2	+5V	No	Yes	0.1μF	Ideal For Surface Mount	LT1181
2	2	+5V	Yes	Yes	1μF	Low Power LT1080	LT1280
2	2	+5V	No	Yes	1μF	Low Power LT1081	LT1281

RS485/RS422 Interface

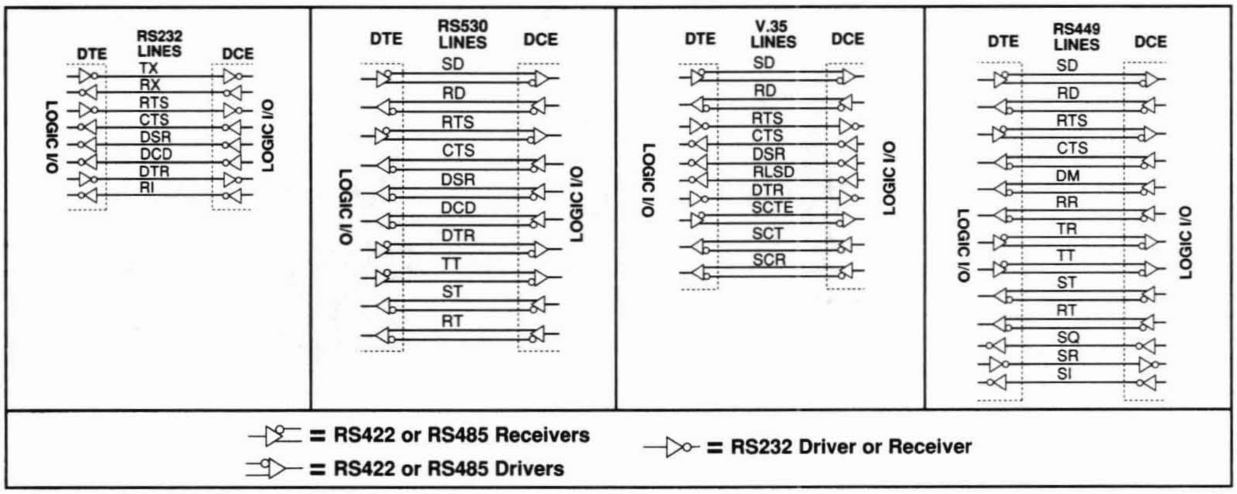
Drivers	Receivers	Supplies Required	Max Data Rate	Max Supply Current	Industry Standard Pinout	Comments	Part Number
1	1	+5V	2.5MB	500μA	75176	Half Duplex 2 Wire RS485	LTC485
4	0	+5V	10MB	150μA	75172	Good For V.35 Interface	LTC486
4	0	+5V	10MB	150μA	75174	Good For V.35 Interface	LTC487
0	4	+5V	10MB	10mA	75173	Good For V.35 Interface	LTC488
0	4	+5V	10MB	10mA	75175	Good For V.35 Interface	LTC489
1	1	+5V	2.5MB	500μA	75179	Full Duplex 4 Wire RS485	LTC490
1	1	+5V	2.5MB	500μA	75ALS180	Full Duplex 4 Wire RS485	LTC491
1	1	+5V	10MB	3.5mA	75ALS176B	High Speed / Half Duplex	LTC1485


LTC RS232 ADVANTAGE
1µF
5V Vcc
1µF
1µF
Inexpensive, Small Charge Pump Caps
5V Powered - No ±12V Supplies Needed
RS232 I/O
Logic I/O
Easy PC Layout: RS232 and Logic I/O on Opposite Sides of Package
Highly Integrated Many Drivers and Receivers per Package
Rugged Bipolar Design Effectively Withstands Line Transients, Static Discharge- Absolutely No Latch Up




Complete Software Selectable Universal DTE/DCE RS232 Interface: NO Jumpers or DIP Switches Required
RS232 I/O
2 TX/RX
3 RX/TX
4 RTS/CTS
5 CTS/RTS
6 DSR/DTR
8 DCD
20 DTR/DSR
22 RI
1µF
5V Vcc
1µF
LT1137
1µF
1µF
LOGIC LEVEL I/O
TX
RX
RTS
CTS
DSR
DCD
DTR
RI
CONFIGURE AS DTE (LOW) OR DCE (HIGH)
1µF
5V Vcc
1µF
LT1138
1µF
1µF

Typical Interconnection Schemes


DTE
RS232 LINES
DCE
TX
RX
RTS
CTS
DSR
DCD
DTR
RI
LOGIC I/O
LOGIC I/O
DTE
RS530 LINES
DCE
SD
RD
RTS
CTS
DSR
DCD
DTR
TT
ST
RT
LOGIC I/O
LOGIC I/O
DTE
V.35 LINES
DCE
SD
RD
RTS
CTS
DSR
RLSD
DTR
SCTE
SCT
SCR
LOGIC I/O
LOGIC I/O
DTE
RS449 LINES
DCE
SD
RD
RTS
CTS
DM
RR
TR
TT
ST
RT
SQ
SR
SI
LOGIC I/O
LOGIC I/O
= RS422 or RS485 Receivers
= RS422 or RS485 Drivers
= RS232 Driver or Receiver

LTC485

Low Power RS485 Interface Transceiver

FEATURES

- Low Power: $I_{CC} = 300\mu A$ Typ
- Designed for RS485 Interface Applications
- Single +5V Supply
- −7V to +12V Bus Common Mode Range Permits ±7V Ground Difference Between Devices on the Bus
- Thermal Shutdown Protection
- Power Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or With the Power Off
- Combined Impedance of a Driver Output and Receiver Allows Up to 32 Transceivers on the Bus
- 70mV Typical Input Hysteresis
- 30ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the SN75176A, DS75176A and µA96176

APPLICATIONS

- Low Power RS485/RS422 Transceiver
- Level Translator

DESCRIPTION

The LTC485 is a low power differential bus/line transceiver designed for multipoint data transmission standard RS485 applications with extended common mode range (+12V to −7V). It also meets the requirements of RS422.

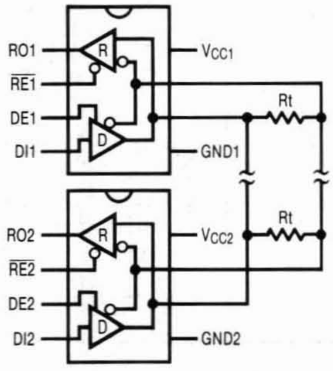
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload of ESD damage.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state.

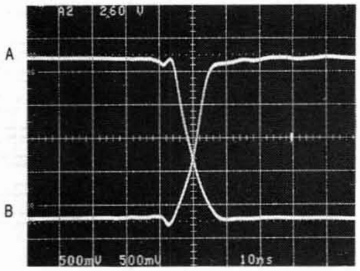
The receiver has a fail safe feature which guarantees a high output state when the inputs are left open.

The LTC485 is fully specified over the commercial and extended industrial temperature range.

TYPICAL APPLICATION



Driver Outputs

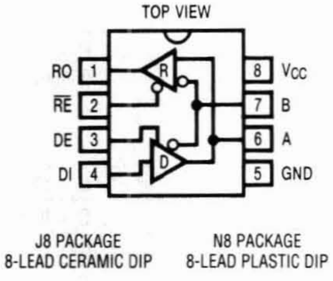


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltages .... −0.5V to V_{CC} + 0.5V
Driver Input Voltage .... −0.5V to V_{CC} + 0.5V
Driver Output Voltages .... ±14V
Receiver Input Voltages........................... ±14V
Receiver Output Voltage .... −0.5V to V_{CC} + 0.5V
Operating Temperature Range
  LTC485I .... $-40°C \le T_A \le 85°C$
  LTC485C .... $0°C \le T_A \le 70°C$
  LTC485M .... $-55°C \le T_A \le 125°C$

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

ORDER PART NUMBER
LTC485CN8
LTC485IN8
LTC485CS8
LTC485IS8
LTC485CJ8
LTC485MJ8
S8 PART MARKING
485
485I

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS		LTC485C, LTC485I MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω; (RS422)	●	2			V
		R = 27Ω; (RS485), Figure 1	●	1.5		5	
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{OC}	Driver Common Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1	●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2.0			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	μA
I_{IN2}	Input Current (A, B)	DE = 0, $V_{CC} = 0$ or 5.25; $V_{IN} = 12V$	●			+1.0	mA
		$V_{IN} = -7V$	●			−0.8	
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le +12V$	●	−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis	$V_{CM} = 0V$	●		70		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, $V_{ID} = +200mV$	●	3.5			V
V_{OL}	Receiver Output Low Voltage	$I_O = +4mA$, $V_{ID} = -200mV$	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, $0.4 \le V_O \le 2.4$	●			±1	μA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le +12V$	●	12			kΩ
I_{CC}	Supply Current	No Load, Pins 2, 3, 4 = 0V or 5V; Outputs Enabled	●		500	900	μA
		Outputs Disabled	●		300	500	
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	$-7V \le V_O \le +12V$	●	35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	$-7V \le V_O \le +10V$	●	35		250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

SWITCHING CHARACTERISTICS $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS		LTC485C, LTC485I MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	$R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$, (Figures 3 and 5)	●	10	30	60	ns
t_{PHL}	Driver Input to Output		●	10	30	60	
t_{SKEW}	Driver Output to Output		●		5	10	
t_R, t_F	Driver Rise or Fall Time		●	3	15	40	
t_{ZH}	Driver Enable to Output High	$C_L = 100pF$ (Figures 4 and 6) S2 Closed	●		40	70	ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100pF$ (Figures 4 and 6) S1 Closed	●		40	70	ns
t_{LZ}	Driver Disable Time from Low	$C_L = 15pF$ (Figures 4 and 6) S1 Closed	●		40	70	ns
t_{HZ}	Driver Disable Time from High	$C_L = 15pF$ (Figures 4 and 6) S2 Closed	●		40	70	ns
t_{PLH}	Receiver Input to Output	$R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$, (Figures 3 and 7)	●	30	90	200	ns
t_{PHL}	Receiver Input to Output		●	30	90	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
t_{ZL}	Receiver Enable to Output Low	$C_{RL} = 15pF$ (Figures 2 and 8) S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	$C_{RL} = 15pF$ (Figures 2 and 8) S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	$C_{RL} = 15pF$ (Figures 2 and 8) S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	$C_{RL} = 15pF$ (Figures 2 and 8) S2 Closed	●		20	50	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

TEST CIRCUITS

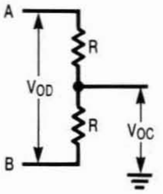


Figure 1. Driver DC Test Load

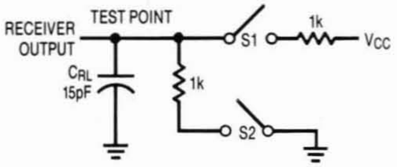


Figure 2. Receiver Timing Test Load

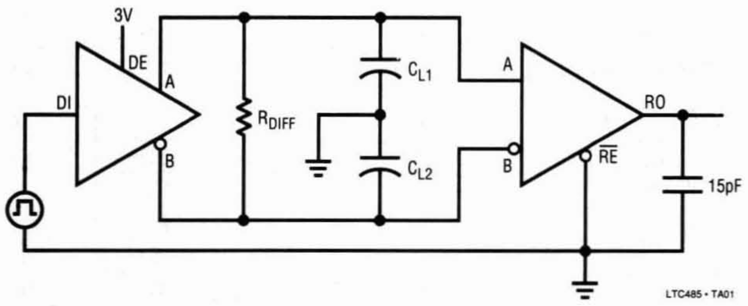


Figure 3. Driver/Receiver Timing Test Circuit

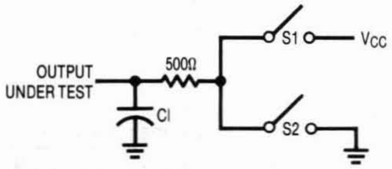


Figure 4. Driver Timing Test Load #2

SWITCHING TIME WAVEFORMS

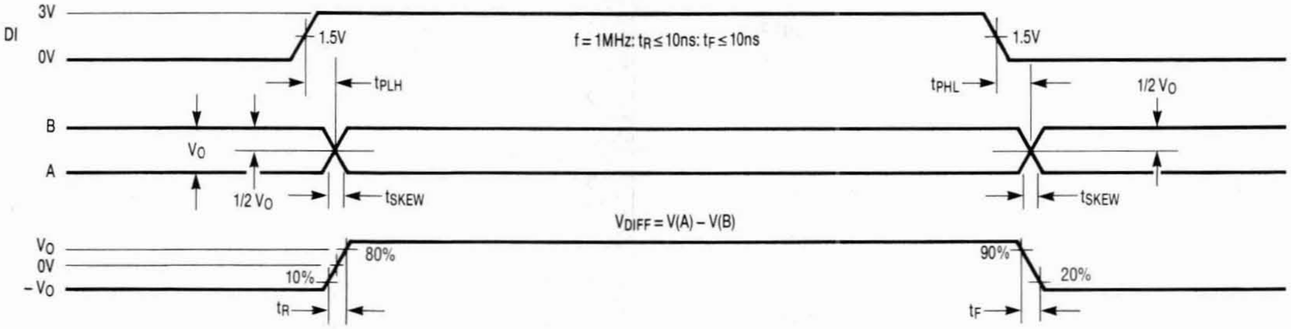

DI
3V
0V
1.5V
f = 1MHz: $t_R \leq$ 10ns: $t_F \leq$ 10ns
1.5V
t_{PLH}
t_{PHL}
1/2 V_O
B
A
V_O
1/2 V_O
t_{SKEW}
t_{SKEW}
V_{DIFF} = V(A) – V(B)
V_O
0V
–V_O
80%
10%
90%
20%
t_R
t_F

Figure 5. Driver Propagation Delays

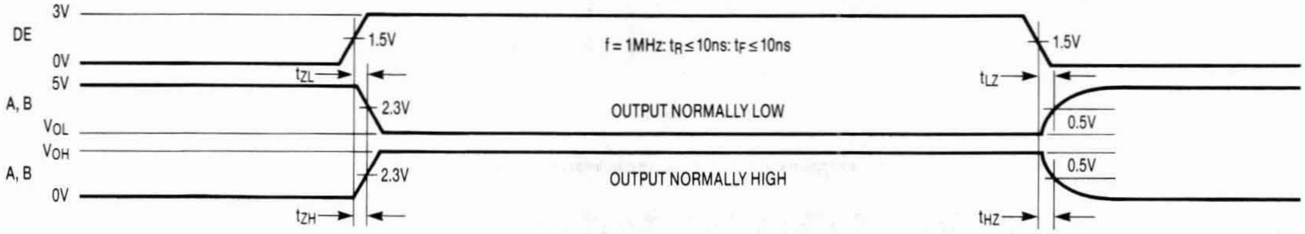

DE
3V
0V
1.5V
f = 1MHz: $t_R \leq$ 10ns: $t_F \leq$ 10ns
1.5V
t_{ZL}
t_{LZ}
A, B
5V
V_{OL}
2.3V
OUTPUT NORMALLY LOW
0.5V
A, B
V_{OH}
0V
2.3V
OUTPUT NORMALLY HIGH
0.5V
t_{ZH}
t_{HZ}

Figure 6. Driver Enable and Disable Times

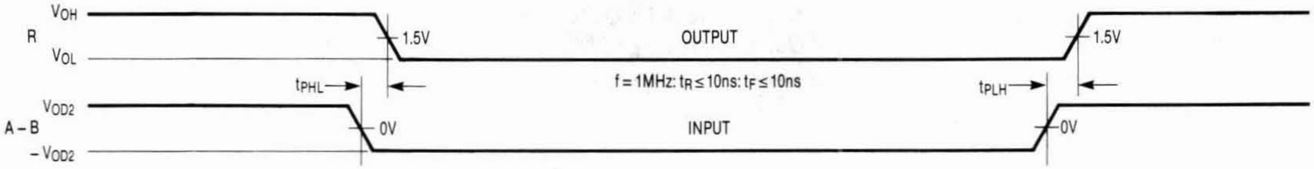

R
V_{OH}
V_{OL}
1.5V
OUTPUT
1.5V
t_{PHL}
f = 1MHz: $t_R \leq$ 10ns: $t_F \leq$ 10ns
t_{PLH}
A – B
V_{OD2}
–V_{OD2}
0V
INPUT
0V

Figure 7. Receiver Propagation Delays

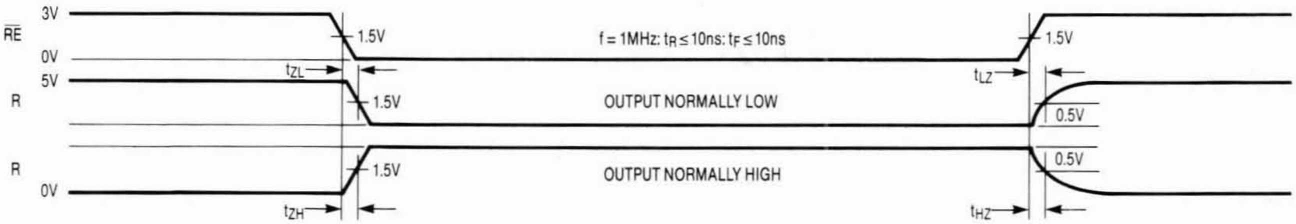

$\overline{RE}$
3V
0V
1.5V
f = 1MHz: $t_R \leq$ 10ns: $t_F \leq$ 10ns
1.5V
t_{ZL}
t_{LZ}
R
5V
1.5V
OUTPUT NORMALLY LOW
0.5V
R
0V
1.5V
OUTPUT NORMALLY HIGH
0.5V
t_{ZH}
t_{HZ}

Figure 8. Receiver Enable and Disable Times

FUNCTION TABLES

LTC485 Transmitting

INPUTS			LINE CONDITION	OUTPUTS	
$\overline{RE}$	DE	DI		B	A
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

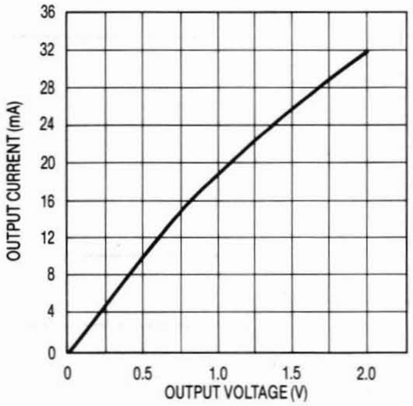
LTC485 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	R
0	0	$\geq +0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Inputs Open	1
1	0	X	Z

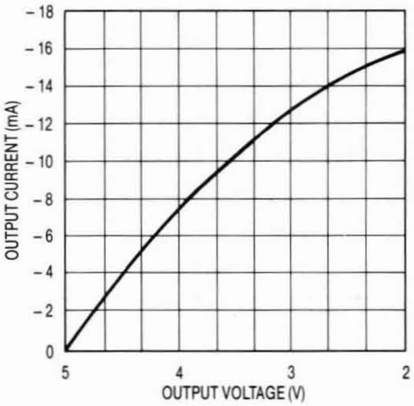
PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1	RO	Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if A > B by 200mV, RO will be high. If A < B by 200mV, then RO will be low.
2	$\overline{RE}$	Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.
3	DE	Driver Outputs Enable. A high on DE enables the driver output. A and B, and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver.
4	DI	Driver Input. If the driver outputs are enabled (DE high), then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.
5	GND	Ground Connection.
6	A	Driver Output/Receiver Input.
7	B	Driver Output/Receiver Input.
8	V_{CC}	Positive Supply; $4.75 < V_{CC} < 5.25$

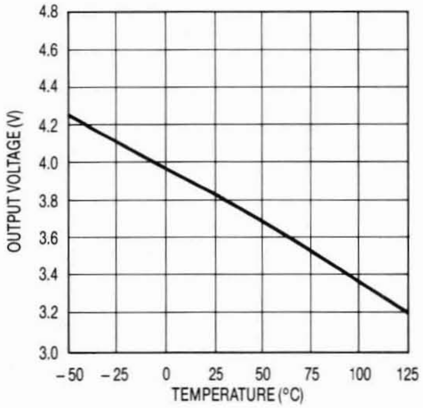
TYPICAL PERFORMANCE CHARACTERISTICS



Receiver Output Low Voltage vs Output Current $T_A = 25°C$



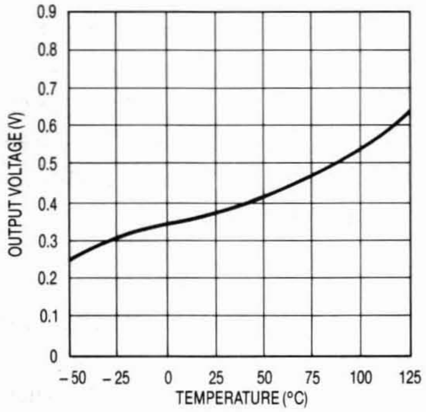
Receiver Output High Voltage vs Output Current $T_A = 25°C$



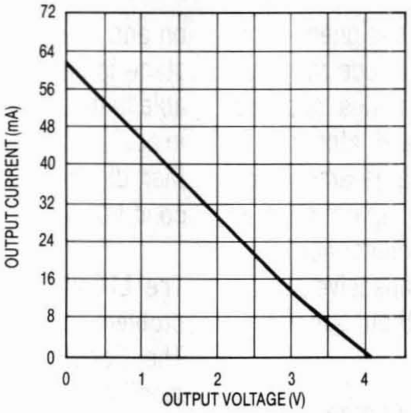
Receiver Output High Voltage vs Temperature @I = 8mA

TYPICAL PERFORMANCE CHARACTERISTICS

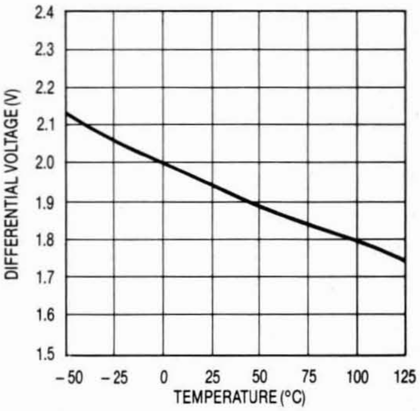
Receiver Output Low Voltage vs Temperature @I = 8mA



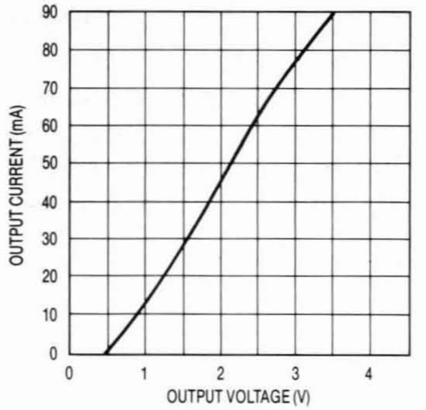
Driver Differential Output Voltage vs Output Current $T_A = 25°C$



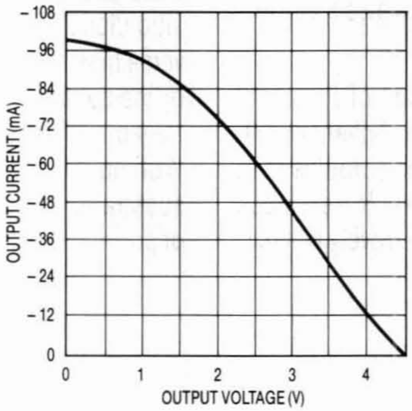
Driver Differential Output Voltage vs Temperature RI = 54Ω



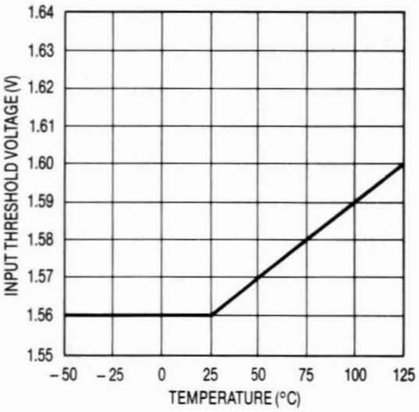
Driver Output Low Voltage vs Output Current $T_A = 25°C$



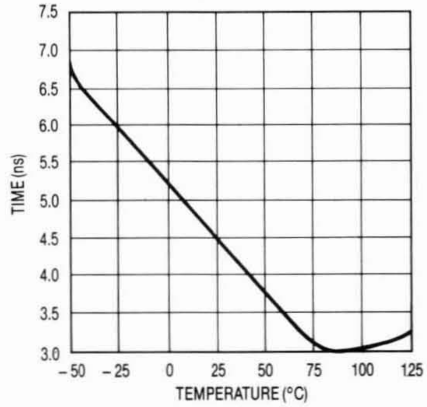
Driver Output High Voltage vs Output Current $T_A = 25°C$



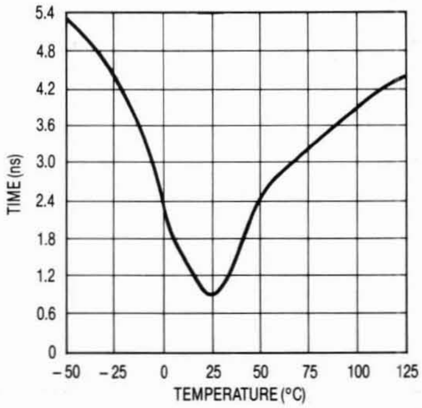
TTL Input Threshold vs Temperature



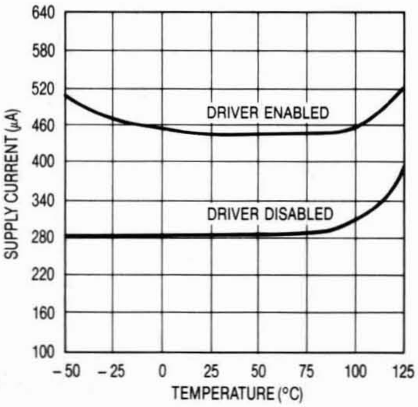
Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



Driver Skew vs Temperature



Supply Current vs Temperature



APPLICATIONS INFORMATION

Basic Theory of Operation

Previous RS485 transceivers have been designed using bipolar technology because the common mode range of the device must extend beyond the supplies and the device must be immune to ESD damage and latchup. Unfortunately, the bipolar devices draw a large amount of supply current, which is unacceptable for the numerous applications that require low power consumption. The LTC485 is the first CMOS RS485/RS422 transceiver which features ultra low power consumption without sacrificing ESD and latchup immunity.

The LTC485 uses a proprietary driver output stage, which allows a common mode range that extends beyond the power supplies while virtually eliminating latchup and providing excellent ESD protection. Figure 9 below shows the LTC485 output stage while Figure 10 shows a conventional CMOS output stage.

When the conventional CMOS output stage of Figure 10 enters a high impedance state, both the P-channel (P1) and the N-channel (N1) are turned off. If the output is then driven above V_{CC} or below ground, the P+/N-well diode (D1) or the N+/P-substrate diode (D2) respectively will turn on and clamp the output to the supply. Thus, the output stage is no longer in a high impedance state and is not able to meet the RS485 common mode range requirement. In addition, the large amount of current flowing through either diode will induce the well known CMOS latchup condition, which could destroy the device.

The LTC485 output stage of Figure 9 eliminates these problems by adding two Schottky diodes, SD3 and SD4. The Schottky diodes are fabricated by a proprietary modification to the standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground, the parasitic diodes D1 or D2 still turn on, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or the substrate. Thus, the high impedance state is maintained even with the output voltage beyond the supplies. With no minority carrier current flowing into the N-well or substrate, latchup is virtually eliminated under power-up or power-down conditions.

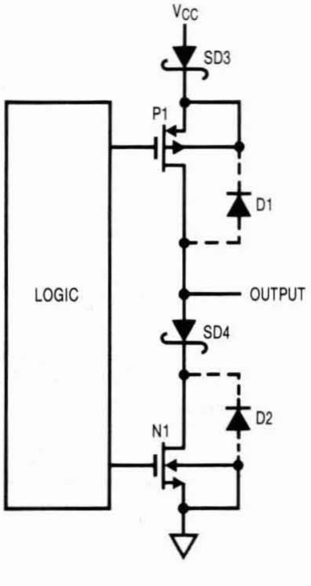


Figure 9. LTC485 Output Stage

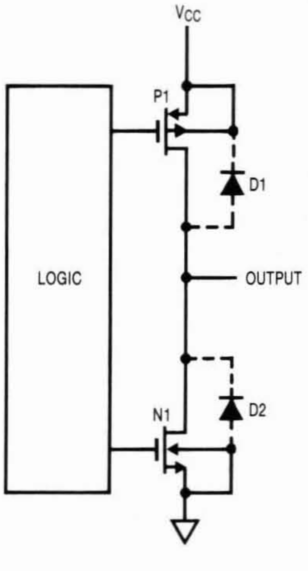


Figure 10. Conventional CMOS Output Stage

APPLICATIONS INFORMATION

The LTC485 output stage will maintain a high impedance state until the breakdown of the N-channel or P-channel is reached when going positive or negative respectively. The output will be clamped to either V_{CC} or ground by a zener voltage plus a Schottky diode drop, but this voltage is way beyond the RS485 operating range. This clamp protects the MOS gates from ESD voltages well over 2000V. Because the ESD injected current in the N-well or substrate consists of majority carriers, latchup is prevented by careful layout techniques.

Propagation Delay

Many digital encoding schemes are dependent upon the difference in the propagation delay times of the driver and the receiver. Using the test circuit of Figure 13, Figures 11 and 12 show the typical LTC485 receiver propagation delay.

The receiver delay times are:

$|t_{PLH} - t_{PHL}| = 9\text{ns}$ Typ, $V_{CC} = 5V$

The driver skew times are:

Skew = 5ns Typ, $V_{CC} = 5V$

10ns Max, $V_{CC} = 5V$, $T_A = -40°C$ to 85°C

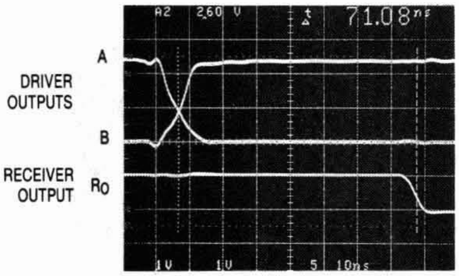


Figure 11. Receiver t_{PHL}

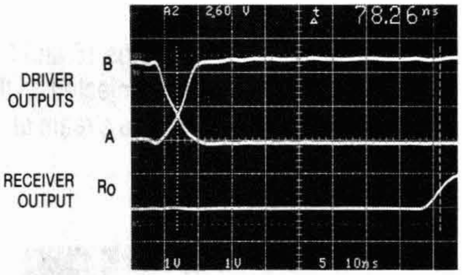


Figure 12. Receiver t_{PLH}

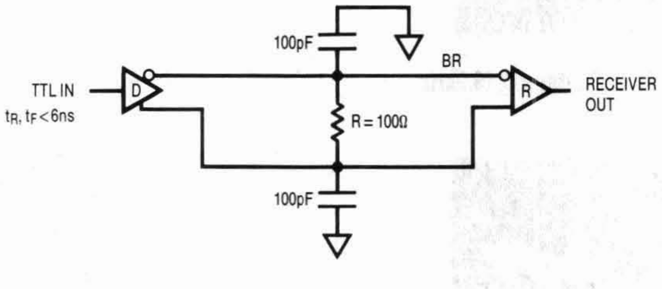


Figure 13. Receiver Propagation Delay Test Circuit

APPLICATIONS INFORMATION

LTC485 Line Length vs Data Rate

The maximum line length allowable for the RS422/RS485 standard is 4000 feet.

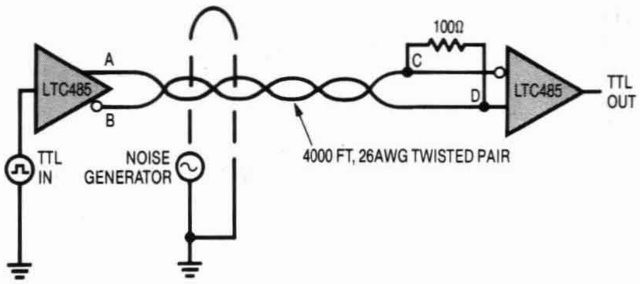


Figure 14. Line Length Test Circuit

Using the test circuit of Figure 14, Figures 15 and 16 show that with ~20Vp-p common mode noise injected on the line, the LTC485 is able to reconstruct the data stream at the end of 4000 feet of twisted pair wire.

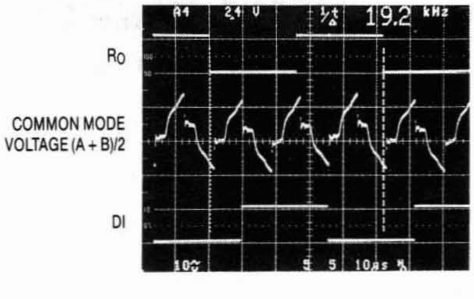


Figure 15. System Common Mode Voltage @19.2kHz

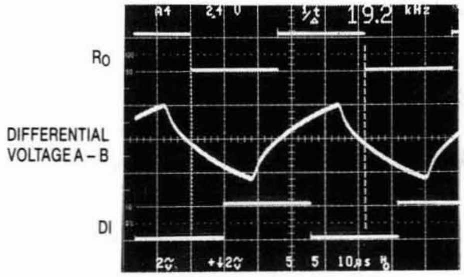


Figure 16. System Differential Voltage @19.2kHz

Figures 17 and 18 show that the LTC485 is able to comfortably drive 4000 feet of wire at 110kHz.

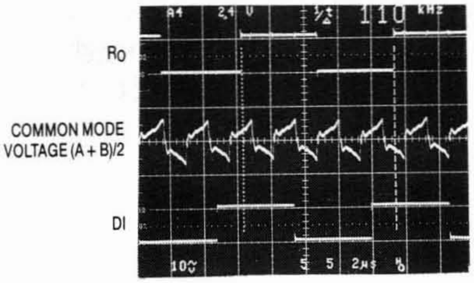


Figure 17. System Common Mode Voltage @110kHz

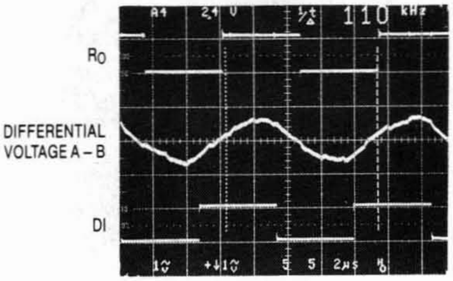


Figure 18. System Differential Voltage @110kHz

When specifying line length vs maximum data rate the curve in Figure 19 should be used:

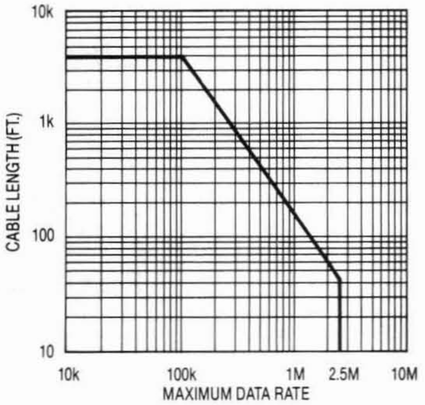
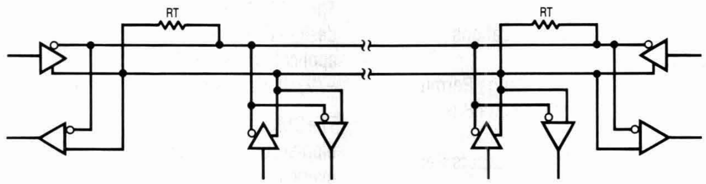


Figure 19. Cable Length vs Maximum Data Rate

TYPICAL APPLICATION

Typical RS485 Network



LTC486

Quad Low Power RS485 Driver

FEATURES

- Very Low Power: I_{CC} = 110µA Typ.
- Designed for RS485 or RS422 Applications
- Single +5V Supply
- –7V to +12V Bus Common Mode Range Permits ±7V GND Difference Between Devices on the Bus
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Driver Outputs Permit Live Insertion/Removal of Package
- Driver Maintains High Impedance in Three-State or with the Power Off
- 28ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the SN75172, DS96172, µA96172, and DS96F172

APPLICATIONS

- Low Power RS485/RS422 Drivers
- Level Translator

DESCRIPTION

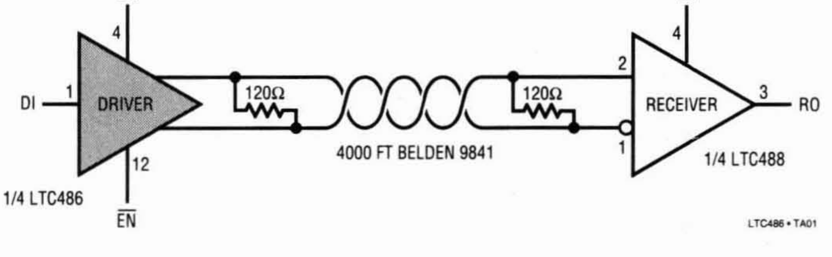
The LTC486 is a low power differential bus/line driver designed for multipoint data transmission standard RS485 applications with extended common mode range (+12V to –7V). It also meets RS422 requirements.

The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

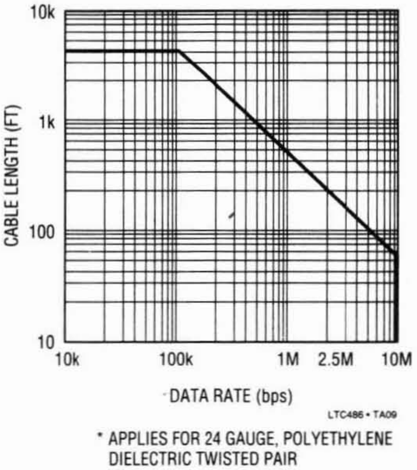
The driver features three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state.

Both AC and DC specifications are guaranteed from 0°C to 70°C and over the 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION



RS485 Cable Length Specification*



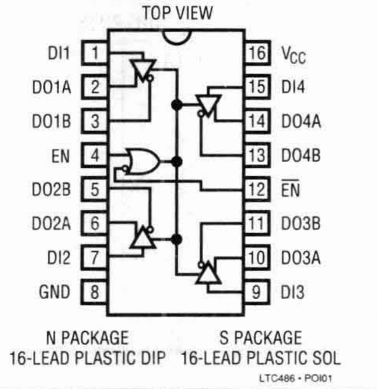
* APPLIES FOR 24 GAUGE, POLYETHYLENE DIELECTRIC TWISTED PAIR

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltages .... −0.5V to V_{CC} + 0.5V
Driver Input Voltages .... −0.5V to V_{CC} + 0.5V
Driver Output Voltages .... ±14V
Control Input Currents .... ±25mA
Driver Input Currents .... ±25mA
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 16-LEAD PLASTIC DIP S PACKAGE 16-LEAD PLASTIC SOL

LTC486 • POI01

ORDER PART NUMBER
LTC486CN LTC486CS

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%, 0°C ≤ Temperature ≤ 70°C (Note 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	I_O = 0				5	V
V_{OD2}	Differential Driver Output Voltage (With Load)	R = 50Ω; (RS422)		2			V
		R = 27Ω; (RS485) (Figure 1)		1.5		5	V
V_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)				0.2	V
V_{OC}	Driver Common Mode Output Voltage					3	
$\|V_{OC}\|$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States					0.2	
V_{IH}	Input High Voltage	DI, EN, $\overline{EN}$		2.0			V
V_{IL}	Input Low Voltage					0.8	V
I_{IN1}	Input Current					±2	μA
I_{CC}	Supply Current	No Load	Output Enabled		110	200	μA
			Output Disabled		110	200	
I_{OSD1}	Driver Short Circuit Current, V_{OUT} = High	−7V ≤ V_O ≤ +12V				250	mA
I_{OSD2}	Driver Short Circuit Current, V_{OUT} = Low	−7V ≤ V_O ≤ +12V				250	mA
I_{OZ}	High Impedance State Output Current	V_O = −7V to 12V			±2	±200	μA

SWITCHING CHARACTERISTICS V_{CC} = 5V ±5%, 0°C ≤ Temperature ≤ 70°C (Note 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF (Figures 2, 4)	20	28	60	ns
t_{PHL}	Driver Input to Output		20	28	60	
t_{SKEW}	Driver Output to Output			5	15	
t_r, t_f	Driver Rise or Fall Time		5	15	71	
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 3, 5) S2 Closed		35	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 3, 5) S1 Closed		44	75	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 3, 5) S1 Closed		55	92	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 3, 5) S2 Closed		45	75	ns

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and Temperature = 25°C.

FUNCTION TABLE

INPUT	ENABLES		OUTPUTS	
DI	EN	$\overline{EN}$	OUTA	OUTB
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H: High Level
L: Low Level
X: Irrelevant
Z: High Impedance (Off)

PIN FUNCTIONS

DI1 (Pin 1): Driver 1 input. If Driver 1 is enabled, then a low on DI1 forces the driver outputs DO1A low and DO1B high. A high on DI1 with the driver outputs enabled will force DO1A high and DO1B low.

DO1A (Pin 2): Driver 1 output.

DO1B (Pin 3): Driver 1 output.

EN (Pin 4): Driver outputs enabled. See Function Table for details.

DO2B (Pin 5): Driver 2 output.

DO2A (Pin 6): Driver 2 output.

DI2 (Pin 7): Driver 2 input. Refer to DI1.

GND (Pin 8): Ground connection.

DI3 (Pin 9): Driver 3 input. Refer to DI1.

DO3A (Pin 10): Driver 3 output.

DO3B (Pin 11): Driver 3 output.

$\overline{EN}$ (Pin 12): Driver outputs disenabled. See Function Table for details.

DO4B (Pin 13): Driver 4 output.

DO4A (Pin 14): Driver 4 output.

DI4 (Pin 15): Driver 4 input. Refer to DI1.

V_{CC} (Pin 16): Positive supply; $4.75 < V_{CC} < 5.25$.

TEST CIRCUITS

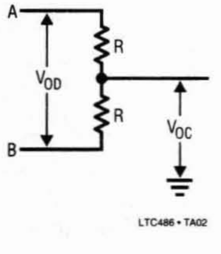

A
R
V_{OD}
R
V_{OC}
B
LTC486 • TA02

Figure 1. Driver DC Test Load

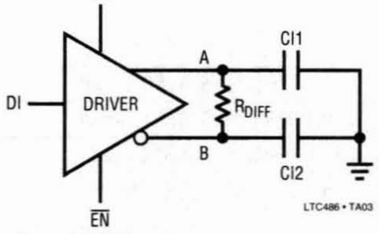

EN
CI1
A
DI
DRIVER
R_{DIFF}
B
CI2
$\overline{EN}$
LTC486 • TA03

Figure 2. Driver Timing Test Circuit

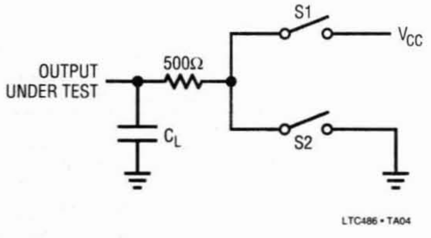

S1
V_{CC}
OUTPUT UNDER TEST
500Ω
C_L
S2
LTC486 • TA04

Figure 3. Driver Timing Test Load #2

SWITCHING TIME WAVEFORMS

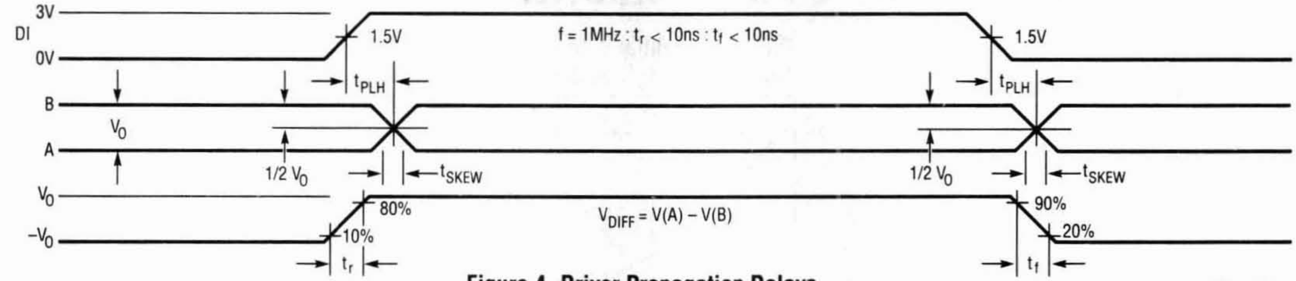

3V
DI
0V
1.5V
f = 1MHz : t_r < 10ns : t_f < 10ns
1.5V
t_{PLH}
t_{PLH}
B
V_O
A
1/2 V_O
t_{SKEW}
1/2 V_O
t_{SKEW}
V_O
80%
V_{DIFF} = V(A) – V(B)
90%
$–V_O$
10%
20%
t_r
t_f
LTC486 • TA05

Figure 4. Driver Propagation Delays

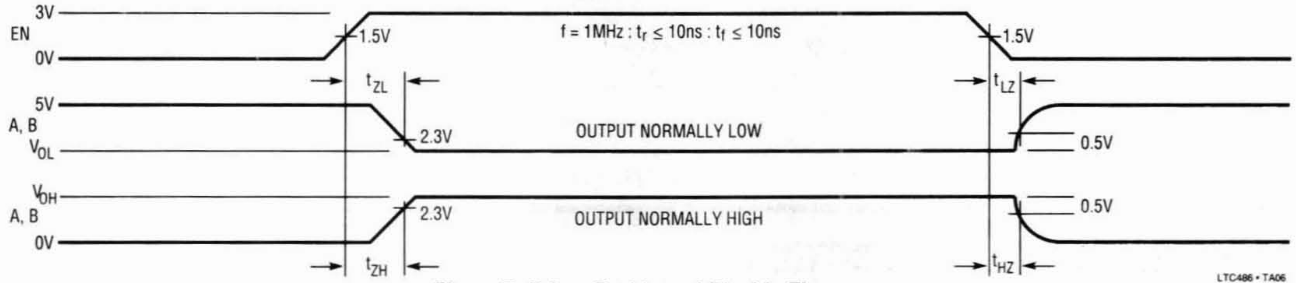
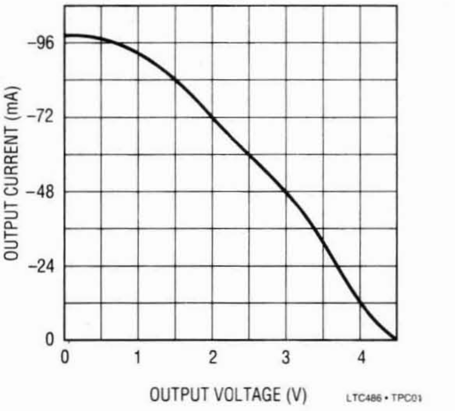

3V
EN
0V
1.5V
f = 1MHz : $t_r \le$ 10ns : $t_f \le$ 10ns
1.5V
t_{ZL}
t_{LZ}
5V
A, B
V_{OL}
2.3V
OUTPUT NORMALLY LOW
0.5V
V_{OH}
A, B
0V
2.3V
OUTPUT NORMALLY HIGH
0.5V
t_{ZH}
t_{HZ}
LTC486 • TA06

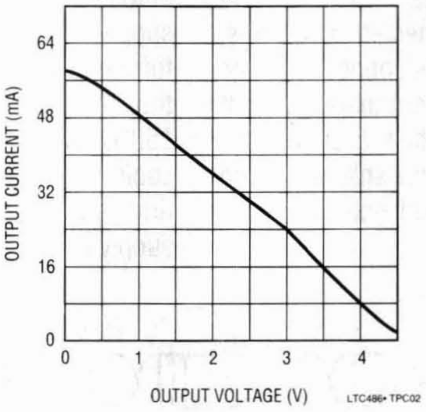
Figure 5. Driver Enable and Disable Times

TYPICAL PERFORMANCE CHARACTERISTICS

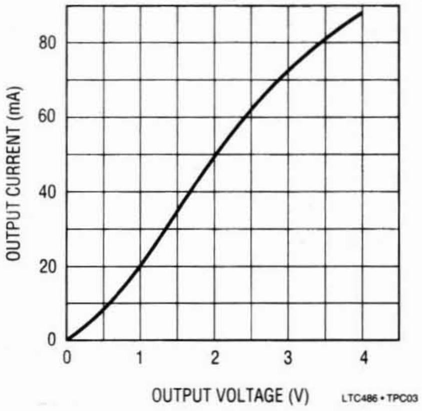
Driver Output High Voltage vs Output Current T_A = 25°C



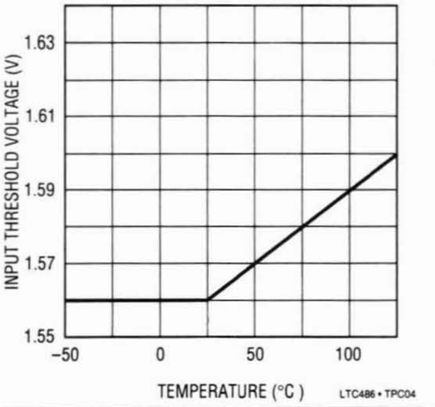
Driver Differential Output Voltage vs Output Current T_A = 25°C



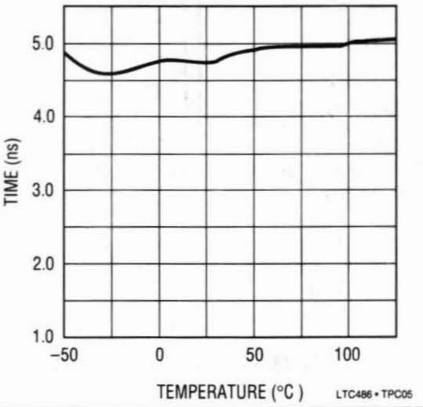
Driver Output Low Voltage vs Output Current T_A = 25°C



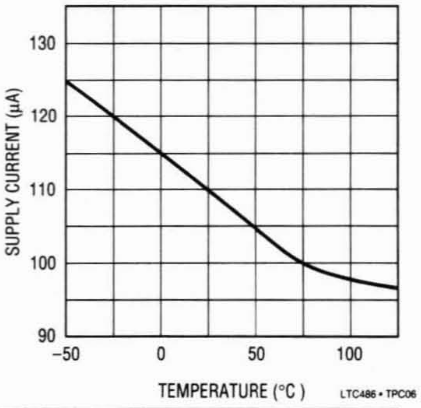
TTL Input Threshold vs Temperature



Driver Skew vs Temperature

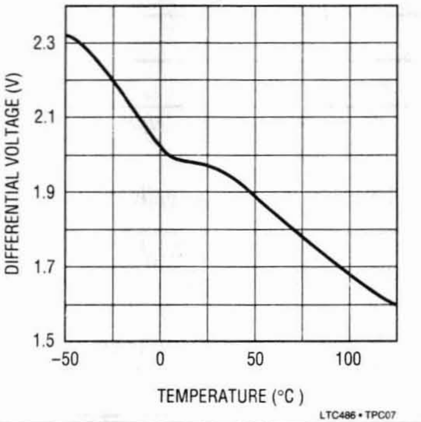


Supply Current vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Driver Differential Output Voltage vs Temperature $R_O = 54\Omega$



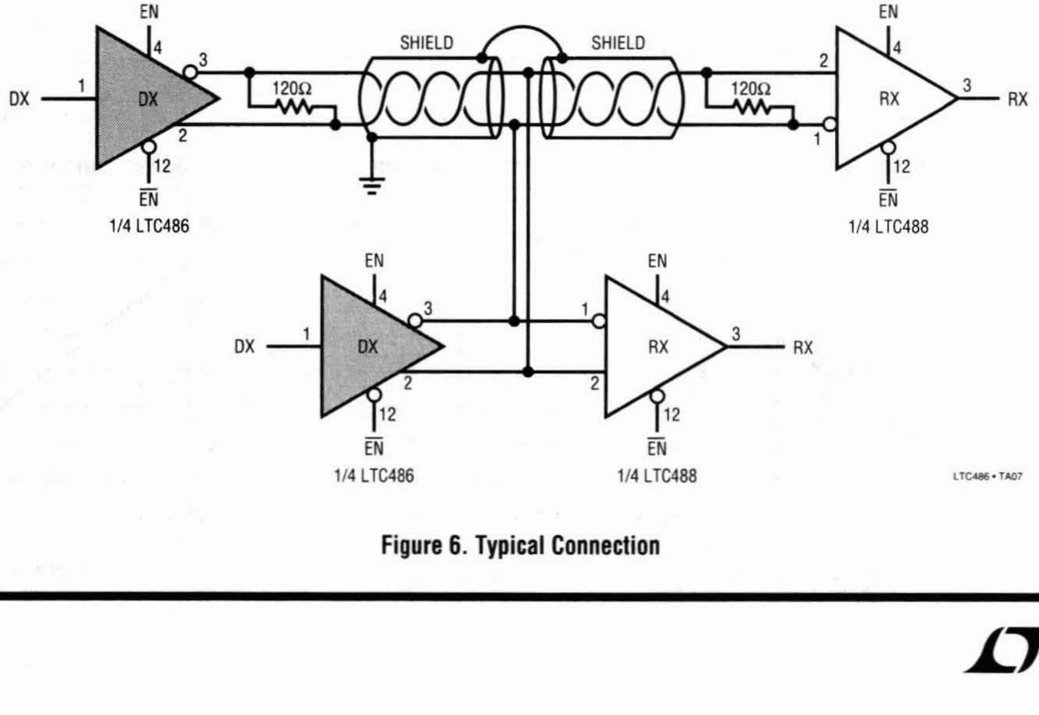
APPLICATIONS INFORMATION

Typical Application

A typical connection of the LTC486 is shown in Figure 6. A twisted pair of wires connect up to 32 drivers and receivers for half duplex data transmission. There are no restrictions on where the chips are connected to the wires, and it isn't necessary to have the chips connected at the ends. However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120Ω. The optional shields around the twisted pair help reduce unwanted noise, and are connected to GND at one end.

Thermal Shutdown

The LTC486 has a thermal shutdown feature which protects the part from excessive power dissipation. If the outputs of the driver are accidently shorted to a power supply or low impedance source, up to 250mA can flow through the part. The thermal shutdown circuit disables the driver outputs when the internal temperature reaches 150°C and turns them back on when the temperature cools to 130°C. If the outputs of two or more LTC486 drivers are shorted directly, the driver outputs can not supply enough current to activate the thermal shutdown.



EN
4
3
DX
1
DX
2
12
$\overline{EN}$
1/4 LTC486
SHIELD
120Ω
SHIELD
120Ω
EN
2
4
RX
3
RX
1
12
$\overline{EN}$
1/4 LTC488
EN
4
3
DX
1
DX
2
12
$\overline{EN}$
1/4 LTC486
EN
1
4
RX
3
RX
2
12
$\overline{EN}$
1/4 LTC488
LTC486 • TA07

Figure 6. Typical Connection

APPLICATIONS INFORMATION

Thus, the thermal shutdown circuit will not prevent contention faults when two drivers are active on the bus at the same time.

Cable and Data Rate

The transmission line of choice for RS-485 applications is a twisted pair. There are coaxial cables (twinaxial) made for this purpose that contain straight pairs, but these are less flexible, more bulky, and more costly than twisted pairs. Many cable manufacturers offer a broad range of 120Ω cables designed for RS-485 applications.

Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage, and AC losses in the dielectric. In good polyethylene cables such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low overall loss (Figure 7).

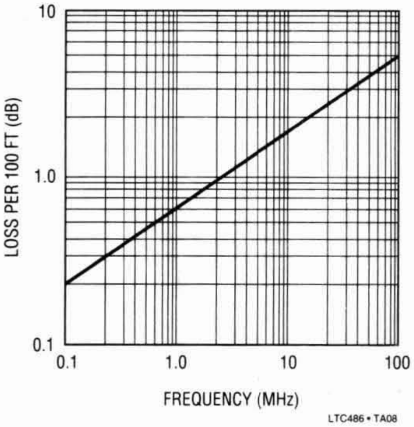


Figure 7. Attenuation vs Frequency for Belden 9841

When using low loss cables, Figure 8 can be used as a guideline for choosing the maximum line length for a given data rate. With lower quality PVC cables, the dielectric loss factor can be 1000 times worse. PVC twisted pairs have terrible losses at high data rates (> 100kbs) and greatly reduce the maximum cable length. At low data rates however, they are acceptable and much more economical.

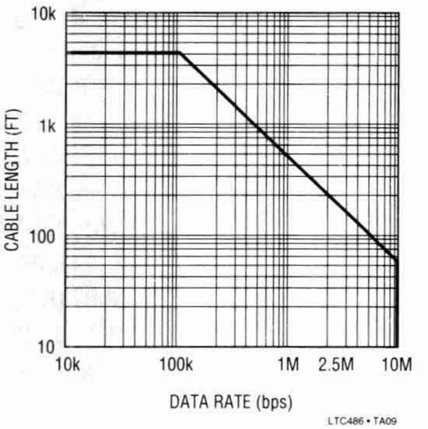


Figure 8. Cable Length vs Data Rate

Cable Termination

The proper termination of the cable is very important. If the cable is not terminated with its characteristic impedance, distorted waveforms will result. In severe cases, distorted (false) data and nulls will occur. A quick look at the output of the driver will tell how well the cable is terminated. It is best to look at a driver connected to the end of the cable, since this eliminates the possibility of getting reflections from two directions. Simply look at the driver output while transmitting square wave data. If the cable is terminated properly, the waveform will look like a square wave (Figure 9).

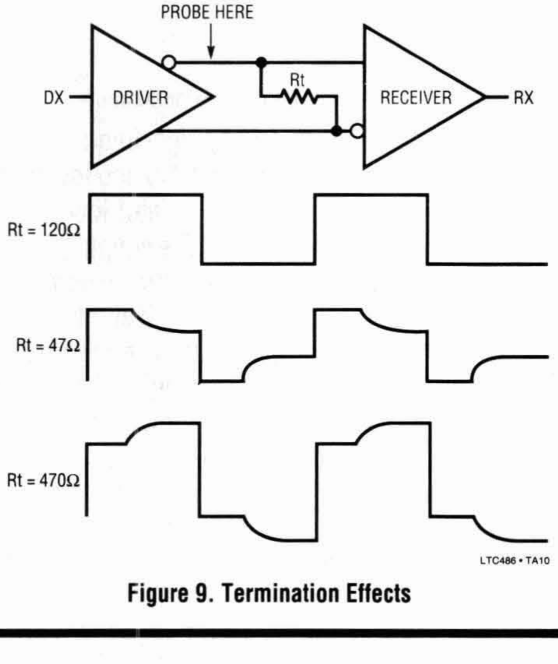


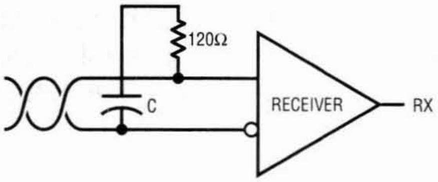
Figure 9. Termination Effects

APPLICATIONS INFORMATION

If the cable is loaded excessively (47Ω), the signal initially sees the surge impedance of the cable and jumps to an initial amplitude. The signal travels down the cable and is reflected back out of phase because of the mistermination. When the reflected signal returns to the driver, the amplitude will be lowered. The width of the pedestal is equal to twice the electrical length of the cable (about 1.5ns/foot). If the cable is lightly loaded (470Ω), the signal reflects in phase and increases the amplitude at the driver output. An input frequency of 30kHz is adequate for tests out to 4000 ft. of cable.

AC Cable Termination

Cable termination resistors are necessary to prevent unwanted reflections, but they consume power. The typical differential output voltage of the driver is 2V when the cable is terminated with two 120Ω resistors, causing 33mA of DC current to flow in the cable when no data is being sent. This DC current is about 220 times greater than the supply current of the LTC486. One way to eliminate the unwanted current is by AC coupling the termination resistors as shown in Figure 10.



C = LINE LENGTH (FT) x 16.3pF

Figure 10. AC Coupled Termination

The coupling capacitor must allow high-frequency energy to flow to the termination, but block DC and low frequencies. The dividing line between high and low frequency depends on the length of the cable. The coupling capacitor must pass frequencies above the point where the line represents an electrical one-tenth wavelength. The value of the coupling capacitor should therefore be set at 16.3pF per foot of cable length for 120Ω cables. With the coupling capacitors in place, power is consumed only on the signal edges, and not when the driver output is idling at a 1 or 0 state. A 100nF capacitor is adequate for lines up to 4000 feet in length. Be aware that the power savings start to decrease once the data rate surpasses 1/(120Ω x C).

Receiver Open-Circuit Fail-Safe

Some data encoding schemes require that the output of the receiver maintains a known state (usually a logic 1) when the data is finished transmitting and all drivers on the line are forced into three-state. All LTC RS485 receivers have a fail-safe feature which guarantees the output to be in a logic 1 state when the receiver inputs are left floating (open-circuit). However, when the cable is terminated with 120Ω, the differential inputs to the receiver are shorted together, not left floating. Because the receiver has about 70mV of hysteresis, the receiver output will maintain the last data bit received.

If the receiver output must be forced to a known state, the circuits of Figure 11 can be used.

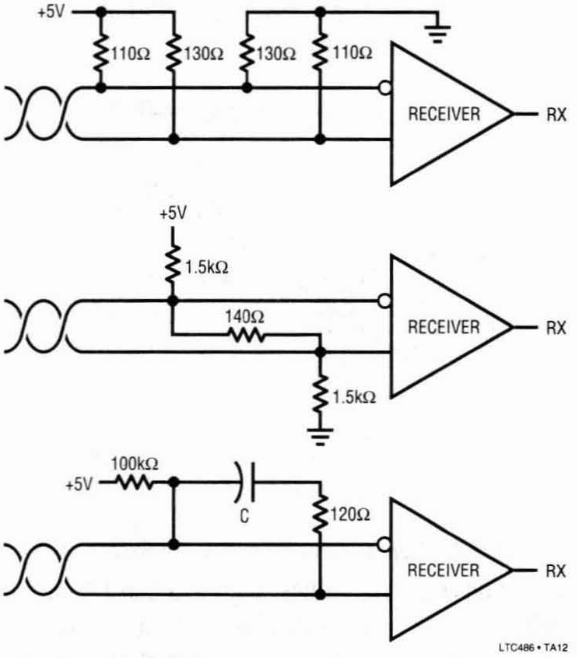


Figure 11. Forcing '0' When All Drivers Are Off

The termination resistors are used to generate a DC bias which forces the receiver output to a known state, in this case a logic 0. The first method consumes about 208mW and the second about 8mW. The lowest power solution is to use an AC termination with a pull-up resistor. Simply swap the receiver inputs for data protocols ending in logic 1.

APPLICATIONS INFORMATION

Fault Protection

All of LTC's RS-485 products are protected against ESD transients up to 2kV using the human body model (100pF, 1.5kΩ). However, some applications need more protection. The best protection method is to connect a bidirectional TransZorb from each line side pin to ground (Figure 12).

A TransZorb is a silicon transient voltage suppressor that has exceptional surge handling capabilities, fast response time, and low series resistance. They are available from General Semiconductor Industries and come in a variety of breakdown voltages and prices. Be sure to pick a breakdown voltage higher than the common mode voltage required for your application (typically 12V). Also, don't forget to check how much the added parasitic capacitance will load down the bus.

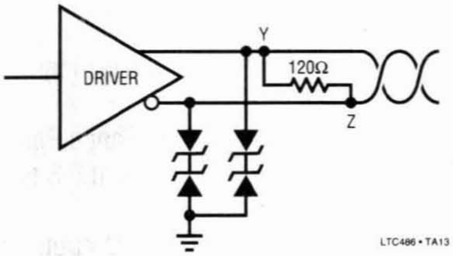
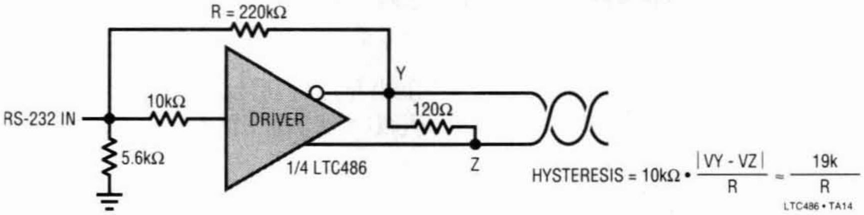

Y
DRIVER
120Ω
Z
LTC486 • TA13

Figure 12. ESD Protection with TransZorbs

TYPICAL APPLICATION

RS232 to RS485 Level Translator with Hysteresis


R = 220kΩ
Y
10kΩ
RS-232 IN
DRIVER
120Ω
5.6kΩ
1/4 LTC486
Z
HYSTERESIS = 10kΩ • |VY - VZ| / R ≈ 19k / R
LTC486 • TA14

LINEAR TECHNOLOGY

LTC487

Quad Low Power RS485 Driver

FEATURES

- Very Low Power: I_{CC} = 110μA Typ.
- Designed for RS485 or RS422 Applications
- Single +5V Supply
- –7V to +12V Bus Common Mode Range Permits ±7V GND Difference Between Devices on the Bus
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Driver Outputs Permit Live Insertion/Removal of Package
- Driver Maintains High Impedance in Three-State or with the Power Off
- 28ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the SN75174, DS96174, μA96174, and DS96F174

APPLICATIONS

- Low Power RS485/RS422 Drivers
- Level Translator

DESCRIPTION

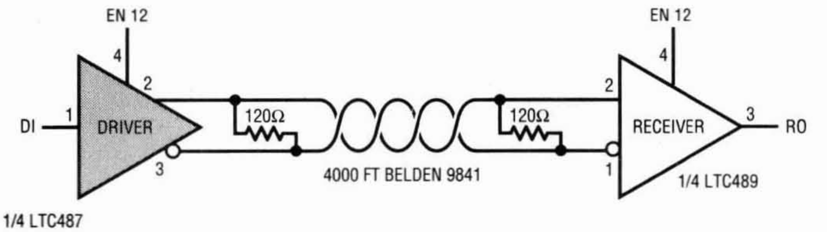
The LTC487 is a low power differential bus/line driver designed for multipoint data transmission standard RS485 applications with extended common mode range (+12V to –7V). It also meets RS422 requirements.

The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

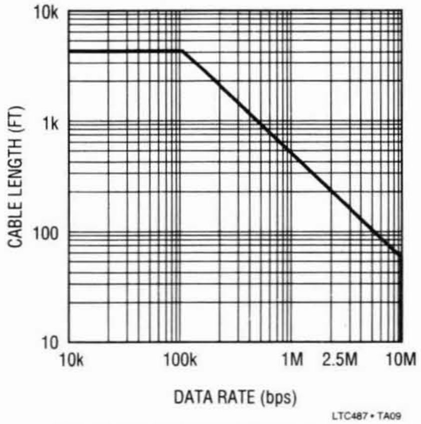
The driver features three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state.

Both AC and DC specifications are guaranteed from 0°C to 70°C and over the 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION



RS485 Cable Length Specification*



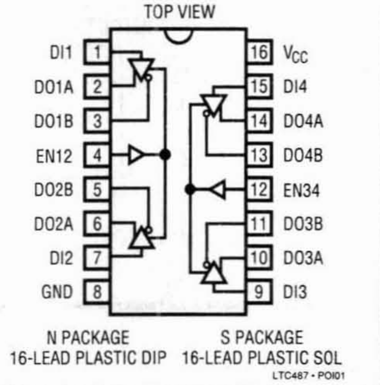
* APPLIES FOR 24 GAUGE, POLYETHYLENE DIELECTRIC TWISTED PAIR

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC})	12V
Control Input Voltages	–0.5V to V_{CC} + 0.5V
Driver Input Voltages	–0.5V to V_{CC} + 0.5V
Driver Output Voltages	±14V
Control Input Currents	±25mA
Driver Input Currents	±25mA
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 16-LEAD PLASTIC DIP
S PACKAGE 16-LEAD PLASTIC SOL

ORDER PART NUMBER
LTC487CN LTC487CS

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±5%, 0°C ≤ Temperature ≤ 70°C (Note 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (With Load)	R = 50Ω; (RS422)		2			V
		R = 27Ω; (RS485) (Figure 1)		1.5		5	V
V_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)				0.2	V
V_{OC}	Driver Common Mode Output Voltage					3	
$\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States					0.2	
V_{IH}	Input High Voltage	DI, EN12, EN34		2.0			V
V_{IL}	Input Low Voltage					0.8	V
I_{IN1}	Input Current					±2	µA
I_{CC}	Supply Current	No Load	Output Enabled		110	200	µA
			Output Disabled		110	200	
I_{OSD1}	Driver Short Circuit Current, V_{OUT} = High	$-7V \le V_O \le +12V$				250	mA
I_{OSD2}	Driver Short Circuit Current, V_{OUT} = Low	$-7V \le V_O \le +12V$				250	mA
I_{OZ}	High Impedance State Output Current	V_O = –7V to 12V			±2	±200	µA

SWITCHING CHARACTERISTICS V_{CC} = 5V ±5%, 0°C ≤ Temperature ≤ 70°C (Note 2, 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF (Figures 2, 4)	20	28	60	ns
t_{PHL}	Driver Input to Output		20	28	60	
t_{SKEW}	Driver Output to Output			5	15	
t_r, t_f	Driver Rise or Fall Time		5	20	71	
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 3, 5) S2 Closed		35	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 3, 5) S1 Closed		44	75	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 3, 5) S1 Closed		55	92	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 3, 5) S2 Closed		45	75	ns

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device GND unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and Temperature = 25°C.

FUNCTION TABLE

INPUT	ENABLES	OUTPUTS	
DI	EN12 or EN34	OUTA	OUTB
H	H	H	L
L	H	L	H
X	L	Z	Z

H: High Level
L: Low Level
X: Irrelevant
Z: High Impedance (Off)

PIN FUNCTIONS

DI1 (Pin 1): Driver 1 input. If Driver 1 is enabled, then a low on DI1 forces the driver outputs DO1A low and DO1B high. A high on DI1 with the driver outputs enabled will force DO1A high and DO1B low.

DO1A (Pin 2): Driver 1 output.

DO1B (Pin 3): Driver 1 output.

EN12 (Pin 4): Driver 1 and 2 outputs enabled. See Function Table for details.

DO2B (Pin 5): Driver 2 output.

DO2A (Pin 6): Driver 2 output.

DI2 (Pin 7): Driver 2 input. Refer to DI1.

GND (Pin 8): GND connection.

DI3 (Pin 9): Driver 3 input. Refer to DI1.

DO3A (Pin 10): Driver 3 output.

DO3B (Pin 11): Driver 3 output.

EN34 (Pin 12): Driver 3 and 4 outputs enabled. See Function Table for details.

DO4B (Pin 13): Driver 4 output.

DO4A (Pin 14): Driver 4 output.

DI4 (Pin 15): Driver 4 input. Refer to DI1.

V_{CC} (Pin 16): Positive supply; $4.75 < V_{CC} < 5.25$.

TEST CIRCUITS

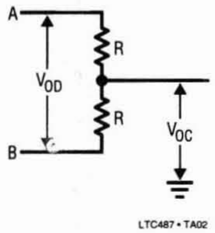

A
B
R
R
V_OD
V_OC
LTC487 • TA02

Figure 1. Driver DC Test Load

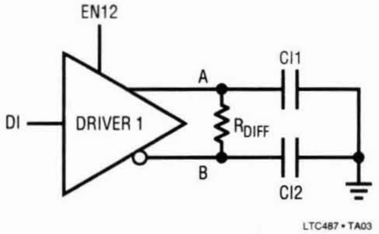

EN12
DI
DRIVER 1
A
B
R_DIFF
CI1
CI2
LTC487 • TA03

Figure 2. Driver Timing Test Circuit

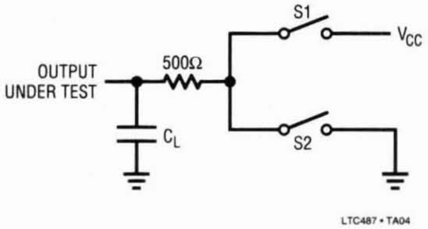

OUTPUT UNDER TEST
500Ω
C_L
S1
S2
V_CC
LTC487 • TA04

Figure 3. Driver Timing Test Load #2

SWITCHING TIME WAVEFORMS

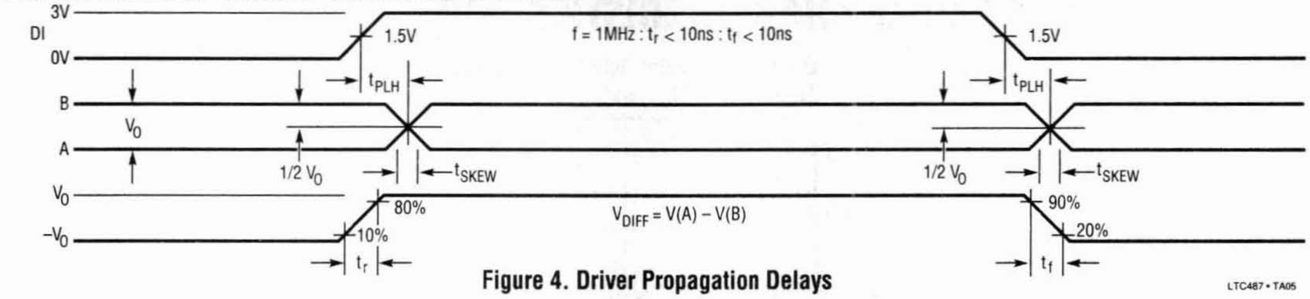

3V
DI
0V
1.5V
f = 1MHz : t_r < 10ns : t_f < 10ns
1.5V
t_{PLH}
t_{PLH}
B
V_O
A
1/2 V_O
t_{SKEW}
1/2 V_O
t_{SKEW}
V_O
80%
V_{DIFF} = V(A) – V(B)
90%
$-V_O$
10%
20%
t_r
t_f
LTC487 • TA05

Figure 4. Driver Propagation Delays

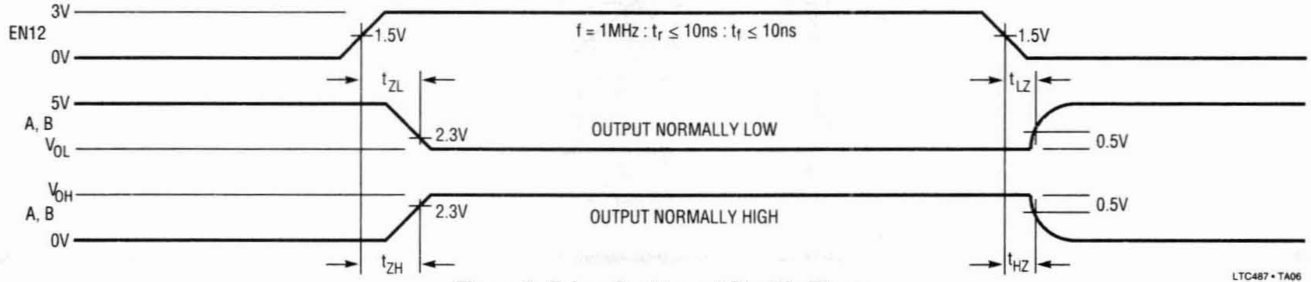
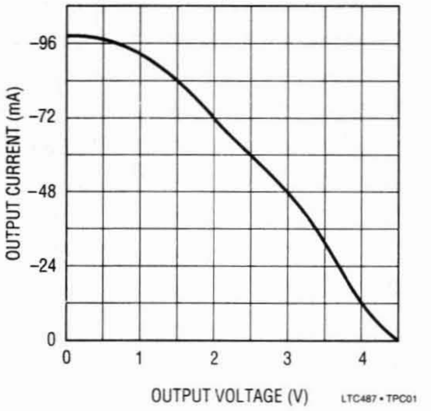

3V
EN12
0V
1.5V
f = 1MHz : t_r ≤ 10ns : t_f ≤ 10ns
1.5V
t_{ZL}
t_{LZ}
5V
A, B
V_{OL}
2.3V
OUTPUT NORMALLY LOW
0.5V
V_{OH}
A, B
0V
2.3V
OUTPUT NORMALLY HIGH
0.5V
t_{ZH}
t_{HZ}
LTC487 • TA06

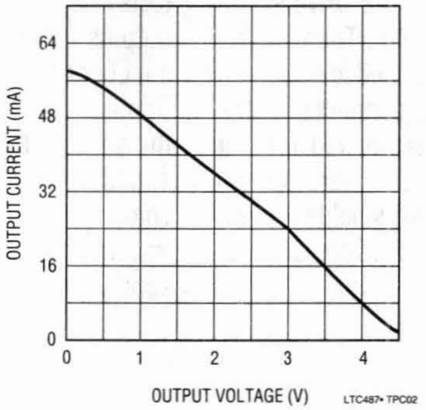
Figure 5. Driver Enable and Disable Times

TYPICAL PERFORMANCE CHARACTERISTICS

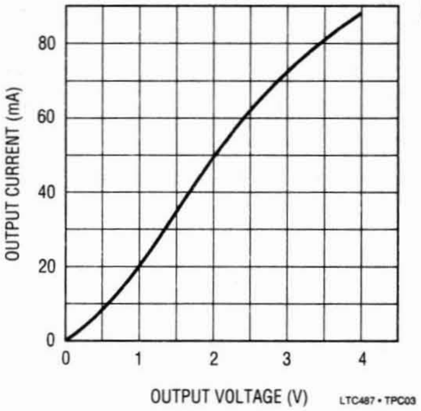
Driver Output High Voltage vs Output Current T_A = 25°C



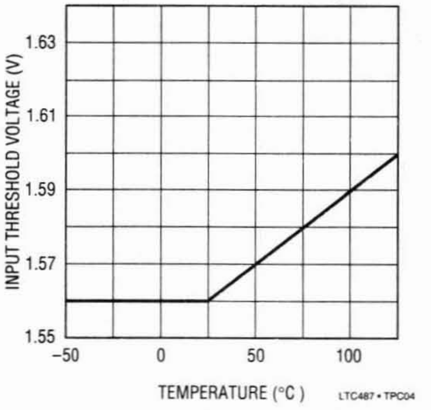
Driver Differential Output Voltage vs Output Current T_A = 25°C



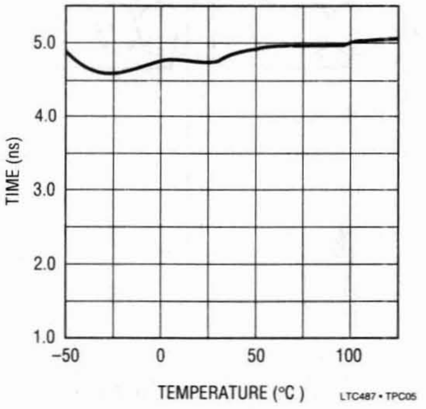
Driver Output Low Voltage vs Output Current T_A = 25°C



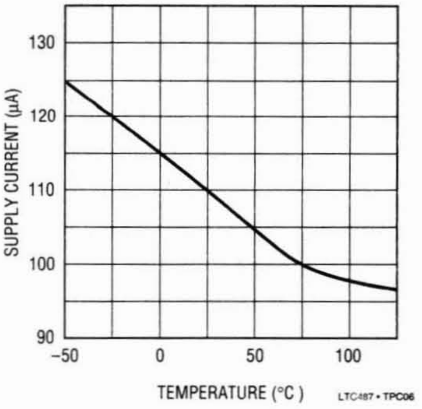
TTL Input Threshold vs Temperature



Driver Skew vs Temperature

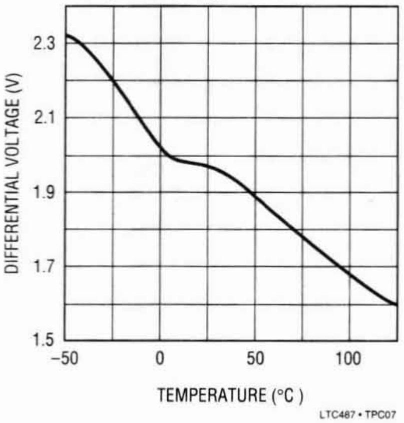


Supply Current vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Driver Differential Output Voltage vs Temperature $R_O = 54\Omega$



APPLICATIONS INFORMATION

Typical Application

A typical connection of the LTC487 is shown in Figure 6. A twisted pair of wires connect up to 32 drivers and receivers for half duplex data transmission. There are no restrictions on where the chips are connected to the wires, and it isn't necessary to have the chips connected at the ends. However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120Ω. The optional shields around the twisted pair help reduce unwanted noise, and are connected to GND at one end.

Thermal Shutdown

The LTC487 has a thermal shutdown feature which protects the part from excessive power dissipation. If the outputs of the driver are accidently shorted to a power supply or low impedance source, up to 250mA can flow through the part. The thermal shutdown circuit disables the driver outputs when the internal temperature reaches 150°C and turns them back on when the temperature cools to 130°C. If the outputs of two or more LTC487 drivers are shorted directly, the driver outputs can not supply enough current to activate the thermal shutdown.

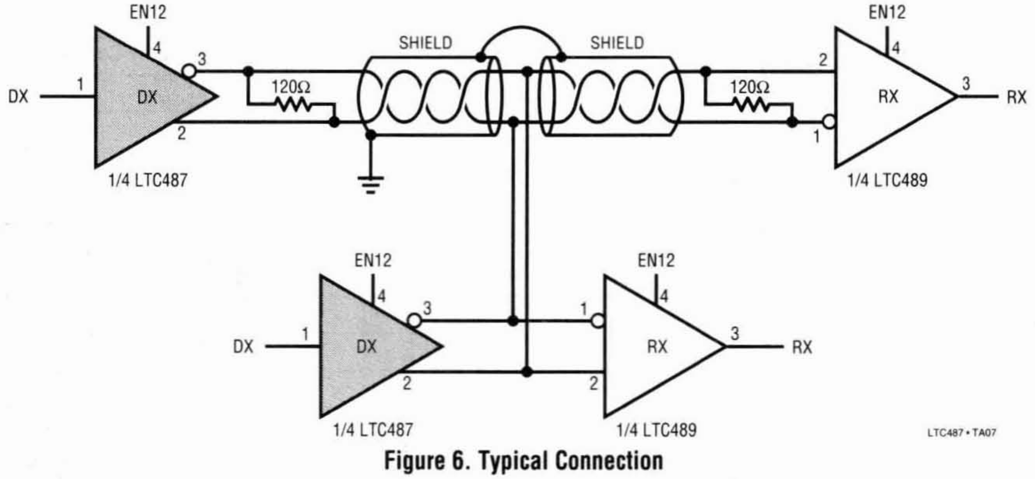


Figure 6. Typical Connection

APPLICATIONS INFORMATION

Thus, the thermal shutdown circuit will not prevent contention faults when two drivers are active on the bus at the same time.

Cable and Data Rate

The transmission line of choice for RS-485 applications is a twisted pair. There are coaxial cables (twinaxial) made for this purpose that contain straight pairs, but these are less flexible, more bulky, and more costly than twisted pairs. Many cable manufacturers offer a broad range of 120Ω cables designed for RS-485 applications.

Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage, and AC losses in the dielectric. In good polyethylene cables such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low overall loss (Figure 7).

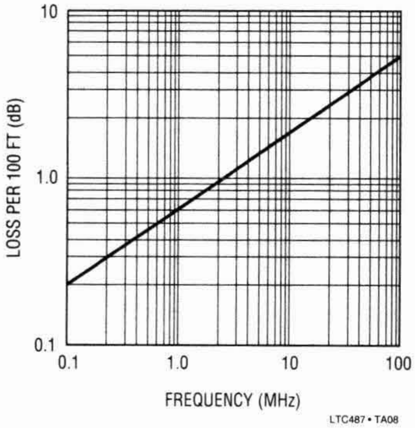


Figure 7. Attenuation vs Frequency for Belden 9841

When using low loss cables, Figure 8 can be used as a guideline for choosing the maximum line length for a given data rate. With lower quality PVC cables, the dielectric loss factor can be 1000 times worse. PVC twisted pairs have terrible losses at high data rates (> 100kbs) and greatly reduce the maximum cable length. At low data rates however, they are acceptable and much more economical.

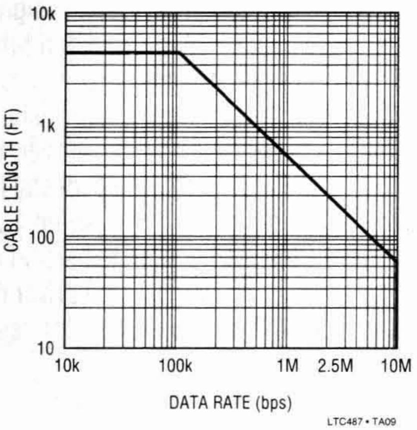


Figure 8. Cable Length vs Data Rate

Cable Termination

The proper termination of the cable is very important. If the cable is not terminated with its characteristic impedance, distorted waveforms will result. In severe cases, distorted (false) data and nulls will occur. A quick look at the output of the driver will tell how well the cable is terminated. It is best to look at a driver connected to the end of the cable, since this eliminates the possibility of getting reflections from two directions. Simply look at the driver output while transmitting square wave data. If the cable is terminated properly, the waveform will look like a square wave (Figure 9).

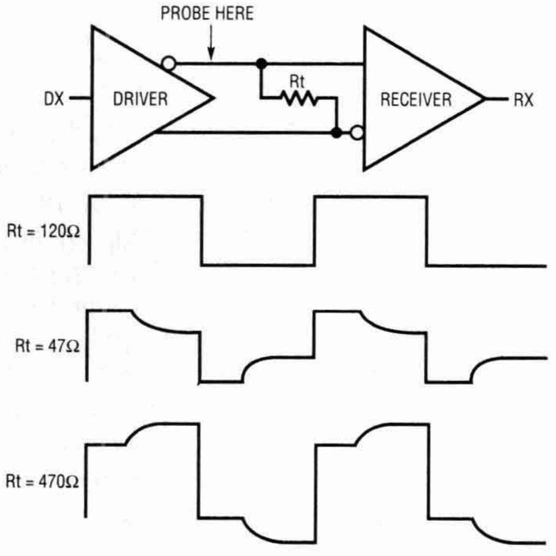


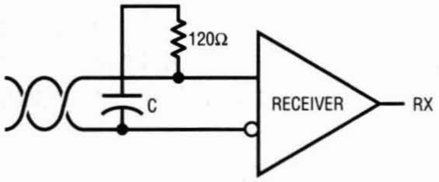
Figure 9. Termination Effects

APPLICATIONS INFORMATION

If the cable is loaded excessively (47Ω), the signal initially sees the surge impedance of the cable and jumps to an initial amplitude. The signal travels down the cable and is reflected back out of phase because of the mistermination. When the reflected signal returns to the driver, the amplitude will be lowered. The width of the pedestal is equal to twice the electrical length of the cable (about 1.5ns/foot). If the cable is lightly loaded (470Ω), the signal reflects in phase and increases the amplitude at the driver output. An input frequency of 30kHz is adequate for tests out to 4000 ft. of cable.

AC Cable Termination

Cable termination resistors are necessary to prevent unwanted reflections, but they consume power. The typical differential output voltage of the driver is 2V when the cable is terminated with two 120Ω resistors, causing 33mA of DC current to flow in the cable when no data is being sent. This DC current is about 220 times greater than the supply current of the LTC487. One way to eliminate the unwanted current is by AC coupling the termination resistors as shown in Figure 10.



C = LINE LENGTH (FT) x 16.3pF

Figure 10. AC Coupled Termination

The coupling capacitor must allow high-frequency energy to flow to the termination, but block DC and low frequencies. The dividing line between high and low frequency depends on the length of the cable. The coupling capacitor must pass frequencies above the point where the line represents an electrical one-tenth wavelength. The value of the coupling capacitor should therefore be set at 16.3pF per foot of cable length for 120Ω cables. With the coupling capacitors in place, power is consumed only on the signal edges, and not when the driver output is idling at a 1 or 0 state. A 100nF capacitor is adequate for lines up to 4000 feet in length. Be aware that the power savings start to decrease once the data rate surpasses 1/(120Ω x C).

Receiver Open-Circuit Fail-Safe

Some data encoding schemes require that the output of the receiver maintains a known state (usually a logic 1) when the data is finished transmitting and all drivers on the line are forced into three-state. All LTC RS485 receivers have a fail-safe feature which guarantees the output to be in a logic 1 state when the receiver inputs are left floating (open-circuit). However, when the cable is terminated with 120Ω, the differential inputs to the receiver are shorted together, not left floating. Because the receiver has about 70mV of hysteresis, the receiver output will maintain the last data bit received.

If the receiver output must be forced to a known state, the circuits of Figure 11 can be used.

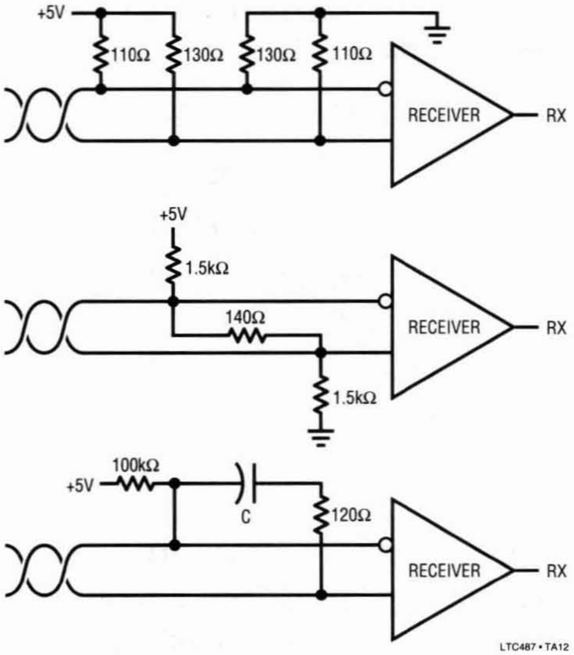


Figure 11. Forcing '0' When All Drivers Are Off

The termination resistors are used to generate a DC bias which forces the receiver output to a known state, in this case a logic 0. The first method consumes about 208mW and the second about 8mW. The lowest power solution is to use an AC termination with a pull-up resistor. Simply swap the receiver inputs for data protocols ending in logic 1.

APPLICATIONS INFORMATION

Fault Protection

All of LTC's RS-485 products are protected against ESD transients up to 2kV using the human body model (100pF, 1.5kΩ). However, some applications need more protection. The best protection method is to connect a bidirectional TransZorb from each line side pin to ground (Figure 12).

A TransZorb is a silicon transient voltage suppressor that has exceptional surge handling capabilities, fast response time, and low series resistance. They are available from General Semiconductor Industries and come in a variety of breakdown voltages and prices. Be sure to pick a breakdown voltage higher than the common mode voltage required for your application (typically 12V). Also, don't forget to check how much the added parasitic capacitance will load down the bus.

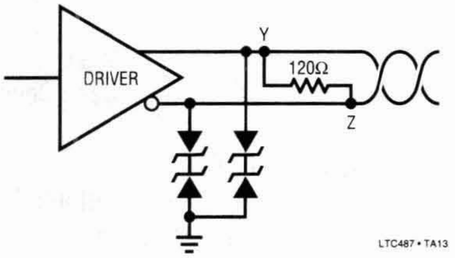
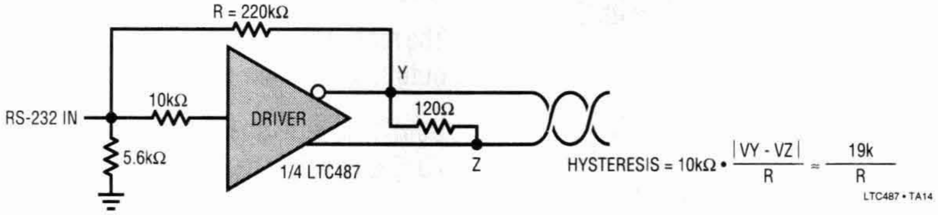

DRIVER
Y
Z
120Ω
LTC487 • TA13

Figure 12. ESD Protection with TransZorbs

TYPICAL APPLICATION

RS232 to RS485 Level Translator with Hysteresis


R = 220kΩ
Y
RS-232 IN
10kΩ
DRIVER
120Ω
5.6kΩ
1/4 LTC487
Z
HYSTERESIS = 10kΩ • |VY - VZ| / R ≈ 19k / R
LTC487 • TA14

LTC490

Differential Driver and Receiver Pair

FEATURES

- Low Power: I_{CC} = 300μA Typical
- Designed for RS485 or RS422 Applications
- Single +5V Supply
- –7V to +12V Bus Common Mode Range Permits ±7V Ground Difference Between Devices on the Bus
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Package
- Driver Maintains High Impedance in Three-State or with the Power Off
- Combined Impedance of a Driver Output and Receiver Allows up to 32 Transceivers on the Bus
- 70mV Typical Input Hysteresis
- 28ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the SN75179

APPLICATIONS

- Low Power RS485/RS422 Transceiver
- Level Translator

DESCRIPTION

The LTC490 is a low power differential bus/line transceiver designed for multipoint data transmission standard RS485 applications with extended common mode range (+12V to –7V). It also meets the requirements of RS422.

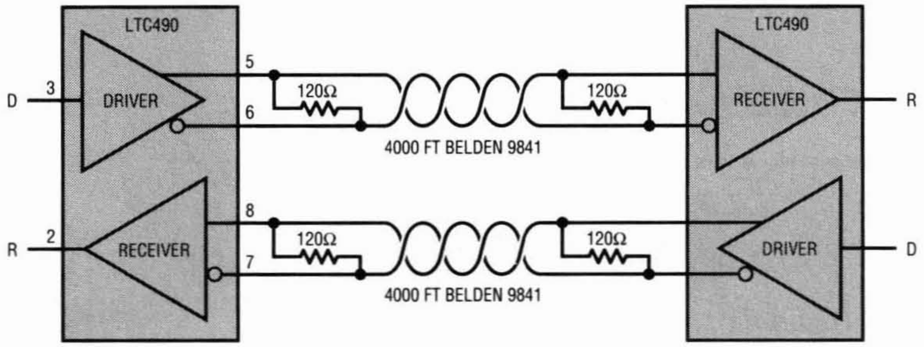
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state.

The receiver has a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed from 0°C to 70°C and 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION



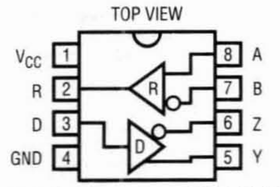
LTC490 • TA01

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Driver Input Currents .... −25mA to 25mA
Driver Input Voltages .... −0.5V to V_{CC} +0.5V
Driver Output Voltages .... ±14V
Receiver Input Voltages .... ±14V
Receiver Output Voltages .... −0.5V to V_{CC} +0.5V
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC

LT490 • POI01

ORDER PART NUMBER
LTC490CN8 LTC490CS8 LTC490IN8 LTC490IS8
S8 PART MARKING
490 490I

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, 0°C ≤ Temperature ≤ 70°C (Notes 2 and 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	I_O = 0				5	V
V_{OD2}	Differential Driver Output Voltage (With load)	R = 50Ω; (RS422)		2			V
		R = 27Ω; (RS485) (Figure 1)		1.5		5	V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)				0.2	V
V_{OC}	Driver Common Mode Output Voltage					3	V
$\Delta \vert V_{OC} \vert$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States					0.2	V
V_{IH}	Input High Voltage (D)			2.0			V
V_{IL}	Input Low Voltage (D)					0.8	V
I_{IN1}	Input Current (D)					±2	µA
I_{IN2}	Input Current (A, B)	V_{CC} = 0V or 5.25V	V_{IN} = 12V			+1.0	mA
			V_{IN} = −7V			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver	−7V ≤ V_{CM} ≤ 12V		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V			70		mV
V_{OH}	Receiver Output High Voltage	I_O = −4mA, V_{ID} = +0.2V		3.5			V
V_{OL}	Receiver Output Low Voltage	I_O = +4mA, V_{ID} = −0.2V				0.4	V
I_{OZR}	Three-State Output Current at Receiver	V_{CC} = Max 0.4V ≤ V_O ≤ 2.4V				±1	µA
I_{CC}	Supply Current	No Load; D = GND, or V_{CC}			300	500	µA
R_{IN}	Receiver Input Resistance	−7V ≤ V_{CM} ≤ +12V		12			kΩ
I_{OSD1}	Driver Short Circuit Current, V_{OUT} = High	−7V ≤ V_O ≤ +12V				250	mA
I_{OSD2}	Driver Short Circuit Current, V_{OUT} = Low	−7V ≤ V_O ≤ +12V				250	mA
I_{OSR}	Receiver Short-Circuit Current	0V ≤ V_O ≤ V_{CC}		7		85	mA
I_{OZ}	Driver Three-State Output Current	V_O = −7V to 12V			±2	±200	µA

SWITCHING CHARACTERISTICS

V_{CC} = 5V ±5%, 0°C ≤ Temperature ≤ 70°C (Notes 2 and 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	$R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$ (Figures 2, 3)	10	28	60	ns
t_{PHL}	Driver Input to Output		10	28	60	ns
t_{SKEW}	Driver Output to Output			5		ns
t_r, t_f	Driver Rise or Fall Time		5	15	25	ns
t_{PLH}	Receiver Input to Output	$R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$ (Figures 2, 4)	40	70	150	ns
t_{PHL}	Receiver Input to Output		40	70	150	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew			13		ns

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and Temperature = 25°C.

PIN FUNCTIONS

V_{CC} (Pin 1): Positive supply; 4.75V ≤ V_{CC} ≤ 5.25V.

R (Pin 2): Receiver output. If A > B by 200mV, R will be high. If A < B by 200mV, then R will be low.

D (Pin 3): Driver input. A low on D forces the driver outputs A low and B high. A high on D will force A high and B low.

GND (Pin 4): Ground Connection.

Y (Pin 5): Driver output.

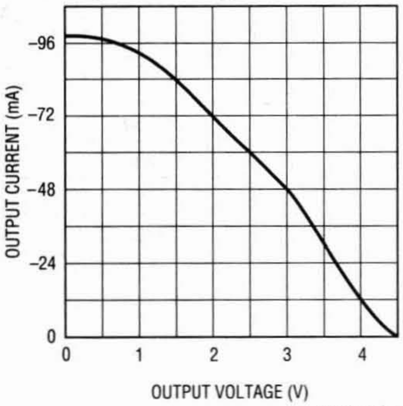
Z (Pin 6): Driver output.

B (Pin 7): Receiver input.

A (Pin 8): Receiver input.

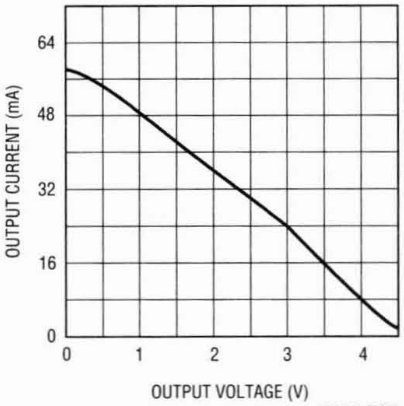
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Output High Voltage vs Output Current T_A = 25°C



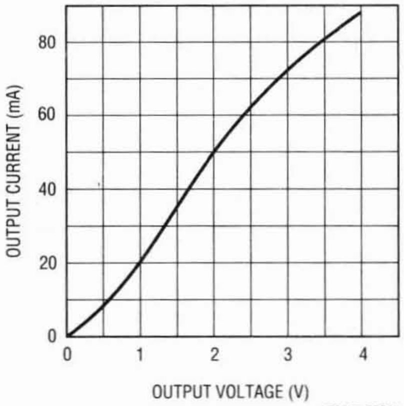
LTC490 • TPC01

Driver Differential Output Voltage vs Output Current T_A = 25°C



LTC490 • TPC02

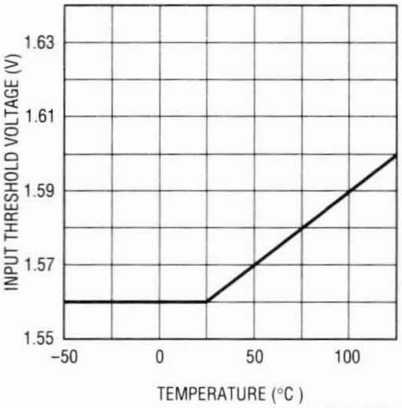
Driver Output Low Voltage vs Output Current T_A = 25°C



LTC490 • TPC03

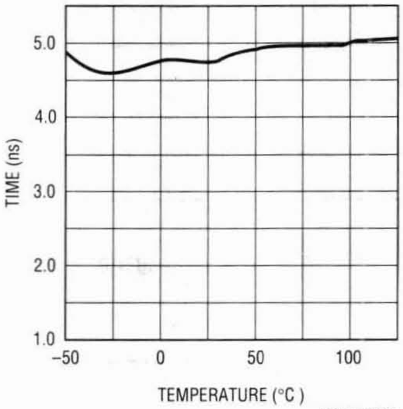
TYPICAL PERFORMANCE CHARACTERISTICS

TTL Input Threshold vs Temperature



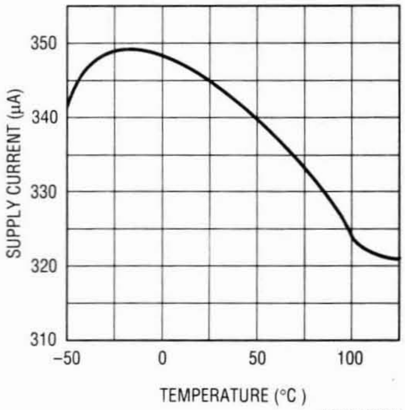
LTC490 • TPC04

Driver Skew vs Temperature



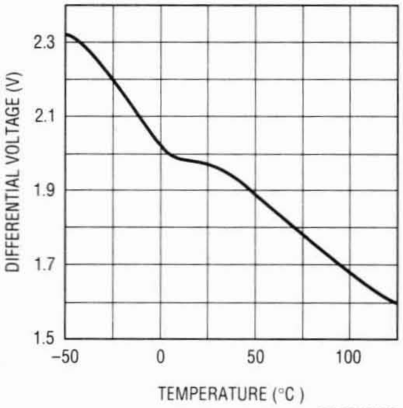
LTC490 • TPC05

Supply Current vs Temperature



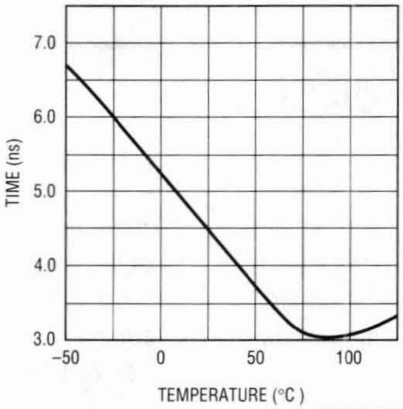
LTC490 • TPC06

Driver Differential Output Voltage vs Temperature $R_O = 54\Omega$



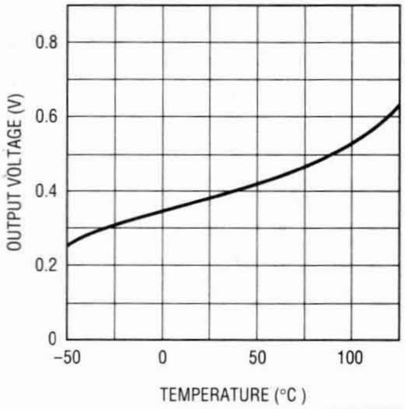
LTC490 • TPC07

Receiver $|t_{PLH}\text{-}t_{PHL}|$ vs Temperature



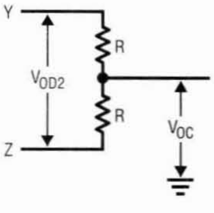
LTC490 • TPC08

Receiver Output Low Voltage vs Temperature at I = 8mA



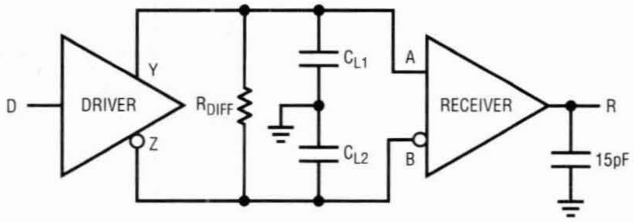
LTC490 • TPC09

TEST CIRCUITS



LTC490 • TA02

Figure 1. Driver DC Test Load



LTC490 • TA03

Figure 2. Driver/Receiver Timing Test Circuit

SWITCHING TIME WAVEFORMS

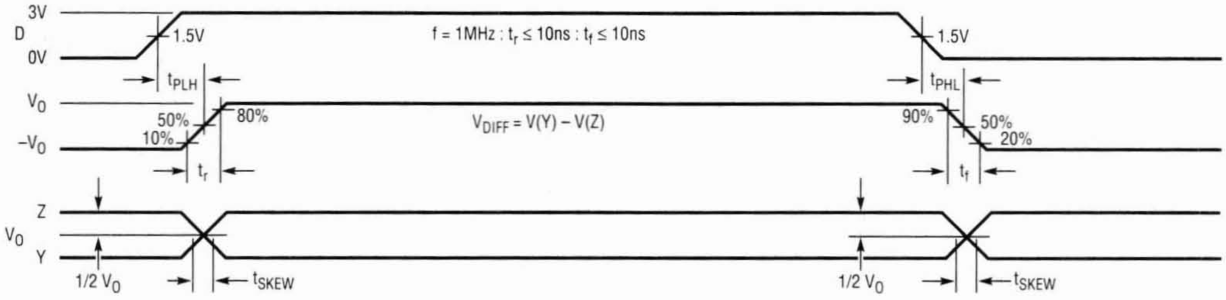

3V
D
0V
1.5V
f = 1MHz : $t_r \leq 10ns$: $t_f \leq 10ns$
1.5V
t_{PLH}
t_{PHL}
V_O
$-V_O$
50%
10%
80%
$V_{DIFF} = V(Y) - V(Z)$
90%
50%
20%
t_r
t_f
Z
V_O
Y
1/2 V_O
t_{SKEW}
1/2 V_O
t_{SKEW}

Figure 3. Driver Propagation Delays

LTC490 • TA04

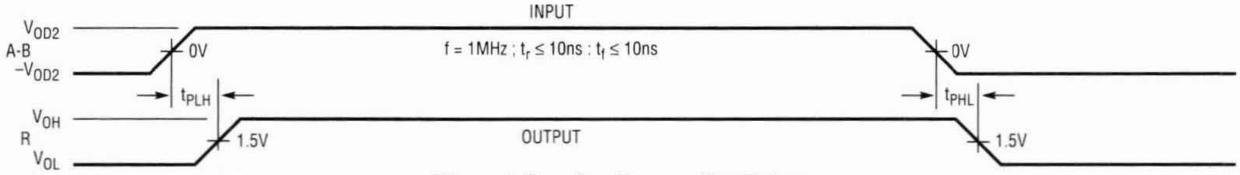

INPUT
V_{OD2}
A-B
$-V_{OD2}$
0V
f = 1MHz ; $t_r \leq 10ns$: $t_f \leq 10ns$
0V
t_{PLH}
t_{PHL}
V_{OH}
R
V_{OL}
1.5V
OUTPUT
1.5V

Figure 4. Receiver Propagation Delays

LTC490 • TA05

APPLICATIONS INFORMATION

Typical Application

A typical connection of the LTC490 is shown in Figure 5. Two twisted pair wires connect two driver/receiver pairs for full duplex data transmission. Note that the driver and receiver outputs are always enabled. If the outputs must be disabled, use the LTC491.

There are no restrictions on where the chips are connected, and it isn't necessary to have the chips connected at the ends of the wire. However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120Ω. Because only

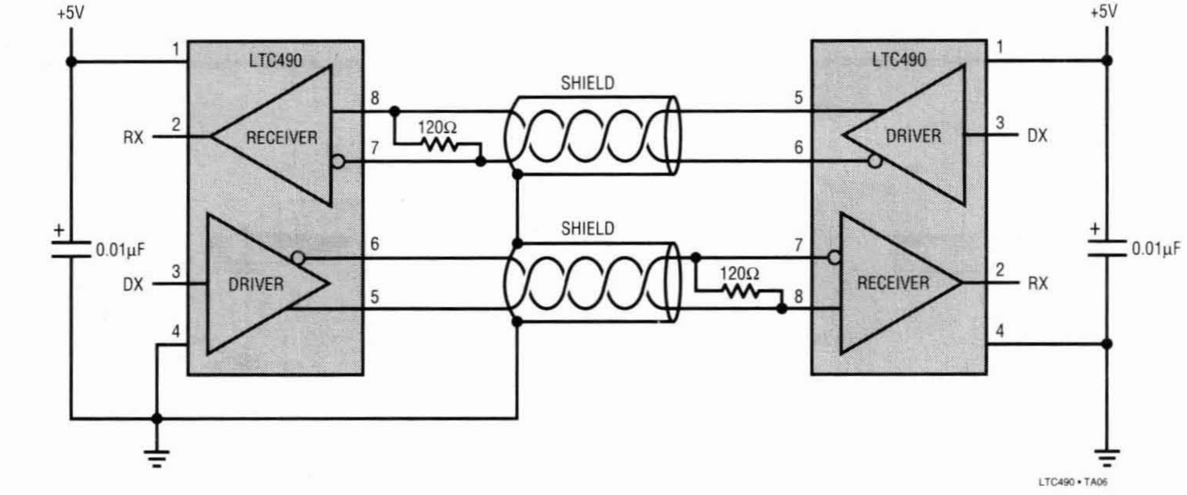

+5V
1
LTC490
RX
2
RECEIVER
8
7
120Ω
SHIELD
0.01µF
DX
3
DRIVER
6
5
4
SHIELD
+5V
1
LTC490
5
6
DRIVER
3
DX
0.01µF
7
120Ω
8
RECEIVER
2
RX
4
LTC490 • TA06

Figure 5. Typical Connection

APPLICATIONS INFORMATION

one driver can be connected on the bus, the cable can be terminated only at the receiving end. The optional shields around the twisted pair help reduce unwanted noise, and are connected to GND at one end.

The LTC490 can also be used as a line repeater as shown in Figure 6. If the cable length is longer than 4000 feet, the LTC490 is inserted in the middle of the cable with the receiver output connected back to the driver input.

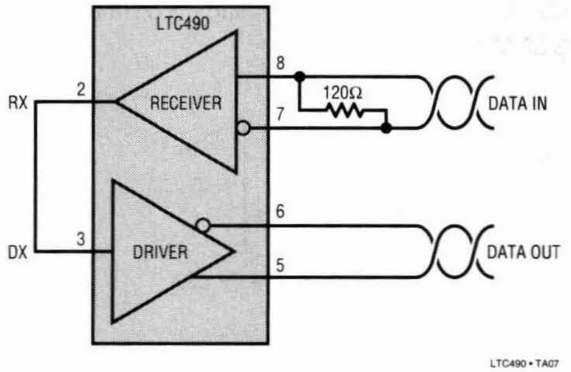


Figure 6. Line Repeater

Thermal Shutdown

The LTC490 has a thermal shutdown feature which protects the part from excessive power dissipation. If the outputs of the driver are accidently shorted to a power supply or low impedance, source, up to 250mA can flow through the part. The thermal shutdown circuit disables the driver outputs when the internal temperature reaches 150°C and turns them back on when the temperature cools to 130°C. If the outputs of two or more LTC490 drivers are shorted directly, the driver outputs can not supply enough current to activate the thermal shutdown. Thus, the thermal shutdown circuit will not prevent contention faults when two drivers are active on the bus at the same time.

Cables and Data Rate

The transmission line of choice for RS485 applications is a twisted pair. There are coaxial cables (twinaxial) made for this purpose that contain straight pairs, but these are less flexible, more bulky, and more costly than twisted pairs. Many cable manufacturers offer a broad range of 120Ω cables designed for RS485 applications.

Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage and AC losses in the dielectric. In good polyethylene cables such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low overall loss (Figure 7).

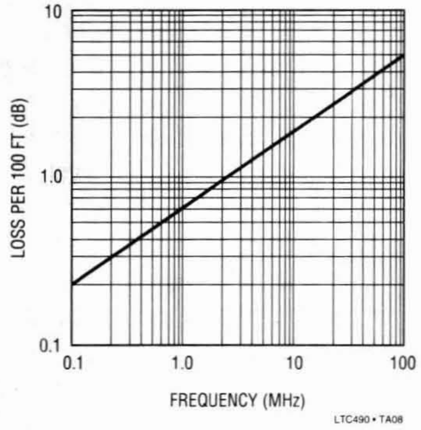


Figure 7. Attenuation vs Frequency for Belden 9841

When using low loss cables, Figure 8 can be used as a guideline for choosing the maximum line length for a given data rate. With lower quality PVC cables, the dielectric loss factor can be 1000 times worse. PVC twisted pairs have terrible losses at high data rates (>100kbs), and greatly reduce the maximum cable length. At low data rates however, they are acceptable and much more economical.

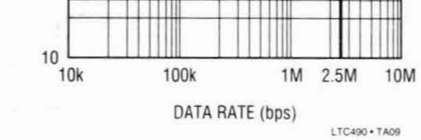


Figure 8. RS485 Cable Length Specification. Applies for 24 Gauge, Polyethylene Dielectric Twisted Pair.

APPLICATIONS INFORMATION

Cable Termination

The proper termination of the cable is very important. If the cable is not terminated with its characteristic impedance, distorted waveforms will result. In severe cases, distorted (false) data and nulls will occur.

A quick look at the output of the driver will tell how well the cable is terminated. It is best to look at a driver connected to the end of the cable, since this eliminates the possibility of getting reflections from two directions. Simply look at the driver output while transmitting square wave data. If the cable is terminated properly, the waveform will look like a square wave (Figure 9). If the cable is loaded excessively (47Ω), the signal initially sees the surge impedance of the cable and jumps to an initial amplitude. The signal travels down the cable and is reflected back out of phase because of the mistermination. When the reflected signal returns to the driver, the amplitude will be lowered. The width of the pedestal is equal to twice the electrical length of the cable (about 1.5ns/foot). If the cable is lightly loaded (470Ω), the signal reflects in phase and increases the amplitude at the driver output. An input frequency of 30kHz is adequate for tests out to 4000 feet of cable.

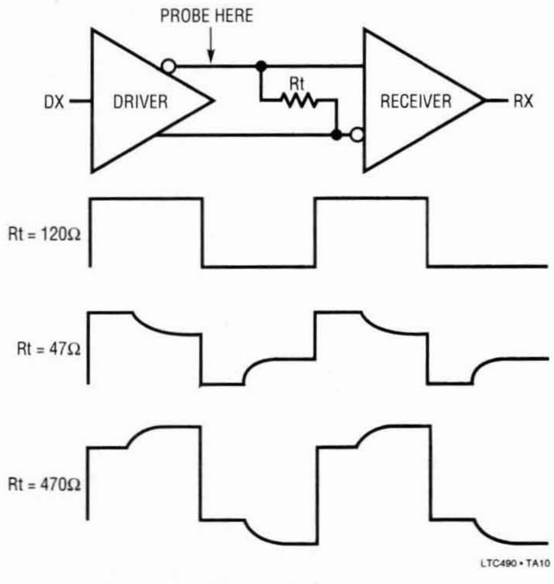


Figure 9. Termination Effects

AC Cable Termination

Cable termination resistors are necessary to prevent unwanted reflections, but they consume power. The typical differential output voltage of the driver is 2V when the cable is terminated with two 120Ω resistors, causing 33mA of DC current to flow in the cable when no data is being sent. This DC current is about 60 times greater than the supply current of the LTC490. One way to eliminate the unwanted current is by AC coupling the termination resistors as shown in Figure 10.

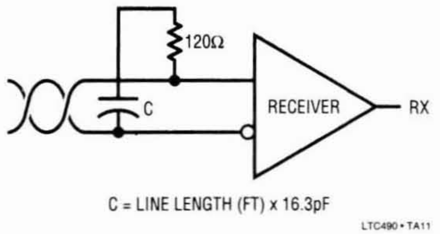


Figure 10. AC Coupled Termination

The coupling capacitor must allow high-frequency energy to flow to the termination, but block DC and low frequencies. The dividing line between high and low frequency depends on the length of the cable. The coupling capacitor must pass frequencies above the point where the line represents an electrical one-tenth wavelength. The value of the coupling capacitor should therefore be set at 16.3pF per foot of cable length for 120Ω cables.

With the coupling capacitors in place, power is consumed only on the signal edges, and not when the driver output is idling at a 1 or 0 state. A 100nF capacitor is adequate for lines up to 4000 feet in length. Be aware that the power savings start to decrease once the data rate surpasses 1/(120Ω × C).

Fault Protection

All of LTC's RS485 products are protected against ESD transients up to 2kV using the human body model (100pF, 1.5kΩ). However, some applications need more protection. The best protection method is to connect a bidirectional TransZorb from each line side pin to ground (Figure 11). A TransZorb is a silicon transient voltage

APPLICATIONS INFORMATION

suppressor that has exceptional surge handling capabilities, fast response time, and low series resistance. They are available from General Semiconductor Industries and come in a variety of breakdown voltages and prices. Be sure to pick a breakdown voltage higher than the common mode voltage required for your application (typically 12V). Also, don't forget to check how much the added parasitic capacitance will load down the bus.

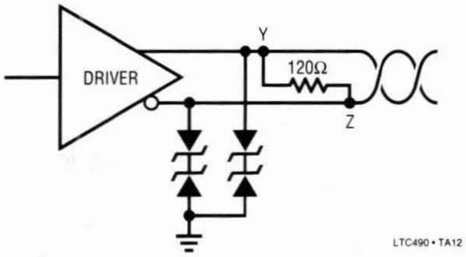
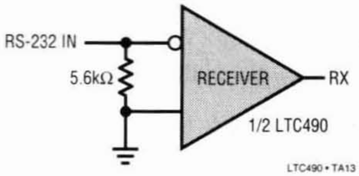

DRIVER
Y
120Ω
Z
LTC490 • TA12

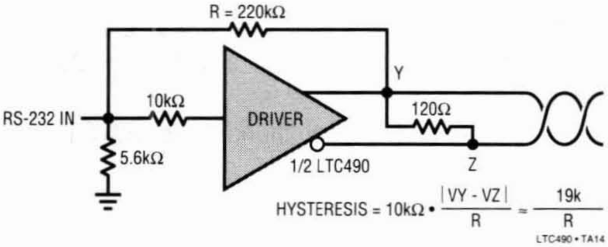
Figure 11. ESD Protection with TransZorbs

TYPICAL APPLICATIONS

RS232 Receiver


RS-232 IN
5.6kΩ
RECEIVER
RX
1/2 LTC490
LTC490 • TA13

RS232 to RS485 Level Transistor with Hysteresis


R = 220kΩ
RS-232 IN
10kΩ
5.6kΩ
DRIVER
Y
120Ω
Z
1/2 LTC490
HYSTERESIS = 10kΩ • |VY - VZ| / R ≈ 19k / R
LTC490 • TA14

LTC491

Differential Driver and Receiver Pair

FEATURES

- Low Power: I_{CC} = 300µA Typical
- Designed for RS485 or RS422 Applications
- Single +5V Supply
- –7V to +12V Bus Common Mode Range Permits ±7V Ground Difference Between Devices on the Bus
- Thermal Shutdown Protection
- Power-Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Package
- Driver Maintains High Impedance in Three-State or with the Power Off
- Combined Impedance of a Driver Output and Receiver Allows up to 32 Transceivers on the Bus
- 70mV Typical Input Hysteresis
- 28ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the SN75180

APPLICATIONS

- Low Power RS485/RS422 Transceiver
- Level Translator

DESCRIPTION

The LTC491 is a low power differential bus/line transceiver designed for multipoint data transmission standard RS485 applications with extended common mode range (+12V to –7V). It also meets the requirements of RS422.

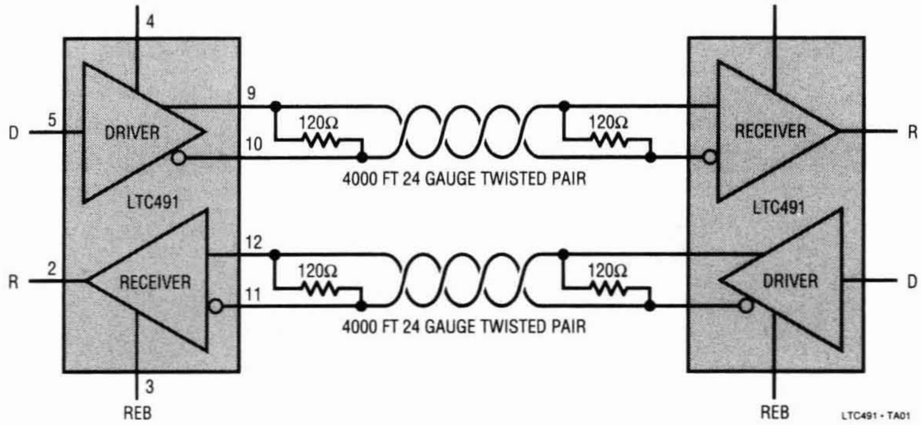
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state.

The receiver has a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed from 0°C to 70°C and 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION

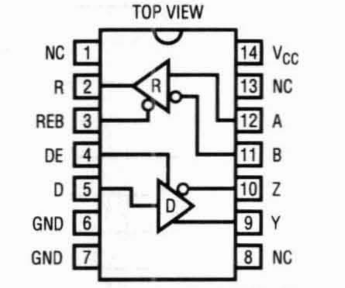


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltages .... −0.5V to V_{CC} +0.5V
Control Input Currents .... −50mA to 50mA
Driver Input Voltages .... −0.5V to V_{CC} +0.5V
Driver Input Currents .... −25mA to 25mA
Driver Output Voltages .... ±14V
Receiver Input Voltages .... ±14V
Receiver Output Voltages .... −0.5V to V_{CC} +0.5V
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 14-LEAD PLASTIC DIP
S PACKAGE 14-LEAD PLASTIC SOIC

LTC491 • POI01

ORDER PART NUMBER
LTC491CN LTC491CS LTC491IN LTC491IS

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, 0°C ≤ Temperature ≤ 70°C (Notes 2 and 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	I_O = 0				5	V
V_{OD2}	Differential Driver Output Voltage (With load)	R = 50Ω; (RS422)		2			V
		R = 27Ω; (RS485) (Figure 1)		1.5		5	V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω (Figure 1)				0.2	V
V_{OC}	Driver Common Mode Output Voltage					3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States					0.2	V
V_{IH}	Input High Voltage	D, DE, REB		2.0			V
V_{IL}	Input Low Voltage					0.8	V
I_{IN1}	Input Current					±2	μA
I_{IN2}	Input Current (A, B)	V_{CC} = 0V or 5.25V	V_{IN} = 12V			+1.0	mA
			V_{IN} = −7V			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver	−7V ≤ V_{CM} ≤ 12V		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V			70		mV
V_{OH}	Receiver Output High Voltage	I_O = −4mA, V_{ID} = +0.2V		3.5			V
V_{OL}	Receiver Output Low Voltage	I_O = +4mA, V_{ID} = −0.2V				0.4	V
I_{OZR}	Three-State Output Current at Receiver	V_{CC} = Max 0.4V ≤ V_O ≤ 2.4V				±1	μA
I_{CC}	Supply Current	No Load; D = GND, or V_{CC}	Outputs Enabled		300	500	μA
			Outputs Disabled		300	500	μA
R_{IN}	Receiver Input Resistance	−7V ≤ V_{CM} ≤ +12V		12			kΩ
I_{OSD1}	Driver Short Circuit Current, V_{OUT} = High	−7V ≤ V_O ≤ +12V				250	mA
I_{OSD2}	Driver Short Circuit Current, V_{OUT} = Low	−7V ≤ V_O ≤ +12V				250	mA
I_{OSR}	Receiver Short Circuit Current	0V ≤ V_O ≤ V_{CC}		7		85	mA
I_{OZ}	Driver Three-State Output Current	V_O = −7V to 12V			±2	±200	μA

SWITCHING CHARACTERISTICS

V_{CC} = 5V ±5%, 0°C ≤ Temperature ≤ 70°C (Notes 2 and 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF (Figures 2, 5)	10	28	60	ns
t_{PHL}	Driver Input to Output		10	28	60	ns
t_{SKEW}	Driver Output to Output			5		ns
t_r, t_f	Driver Rise or Fall Time		5	15	25	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 4, 6) S2 Closed		40	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 4, 6) S1 Closed		40	70	ns
t_{LZ}	Driver Disable Time From Low	C_L = 15pF (Figures 4, 6) S1 Closed		40	70	ns
t_{HZ}	Driver Disable Time From High	C_L = 15pF (Figures 4, 6) S2 Closed		40	70	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, $C_{L1} = C_{L2}$ = 100pF (Figures 2, 7)	40	70	150	ns
t_{PHL}	Receiver Input to Output		40	70	150	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew			13		ns
t_{ZL}	Receiver Enable to Output Low	C_L = 15pF (Figures 3, 8) S1 Closed		20	50	ns
t_{ZH}	Receiver Enable to Output High	C_L = 15pF (Figures 3, 8) S2 Closed		20	50	ns
t_{LZ}	Receiver Disable From Low	C_L = 15pF (Figures 3, 8) S1 Closed		20	50	ns
t_{HZ}	Receiver Disable From High	C_L = 15pF (Figures 3, 8) S2 Closed		20	50	ns

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and Temperature = 25°C.

PIN FUNCTIONS

NC (Pin 1): Not Connected.

R (Pin 2): Receiver output. If the receiver output is enabled (REB low), then if A > B by 200mV, R will be high. If A < B by 200mV, then R will be low.

REB (Pin 3): Receiver output enable. A low enables the receiver output, R. A high input forces the receiver output into a high impedance state.

DE (Pin 4): Driver output enable. A high on DE enables the driver outputs, A and B. A low input forces the driver outputs into a high impedance state.

D (Pin 5): Driver input. If the driver outputs are enabled (DE high), then A low on D forces the driver outputs A low and B high. A high on D will force A high and B low.

GND (Pin 6): Ground Connection.

GND (Pin 7): Ground Connection.

NC (Pin 8): Not Connected.

Y (Pin 9): Driver output.

Z (Pin 10): Driver output.

B (Pin 11): Receiver input.

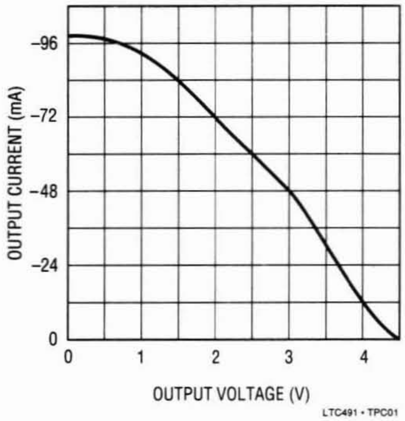
A (Pin 12): Receiver input.

NC (Pin 13): Not Connected.

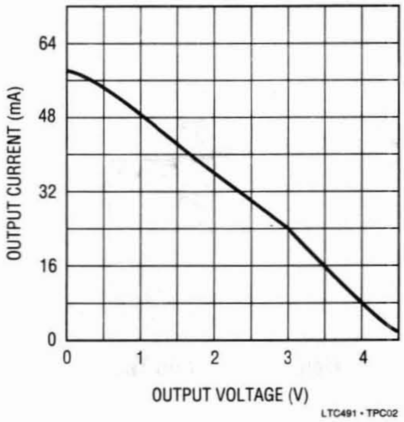
V_{CC} (Pin 14): Positive supply; 4.75V ≤ V_{CC} ≤ 5.25V.

TYPICAL PERFORMANCE CHARACTERISTICS

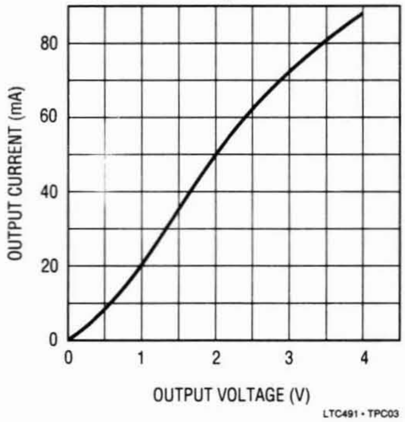
Driver Output High Voltage vs Output Current $T_A = 25°C$



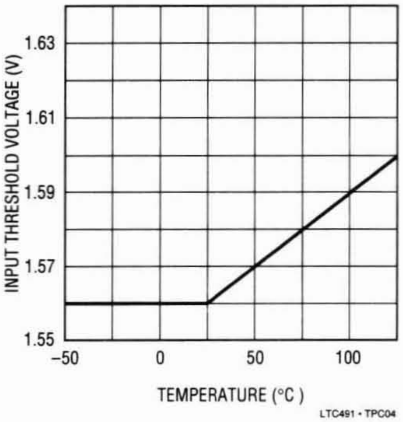
Driver Differential Output Voltage vs Output Current $T_A = 25°C$



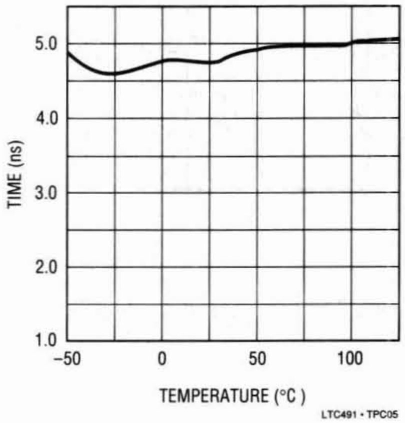
Driver Output Low Voltage vs Output Current $T_A = 25°C$



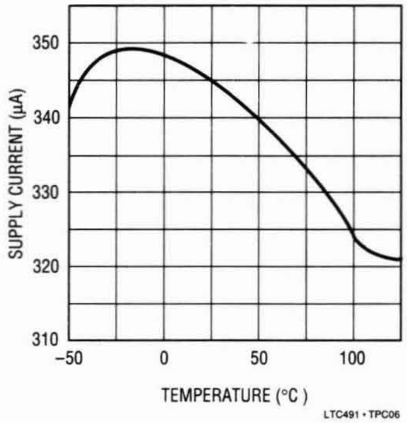
TTL Input Threshold vs Temperature



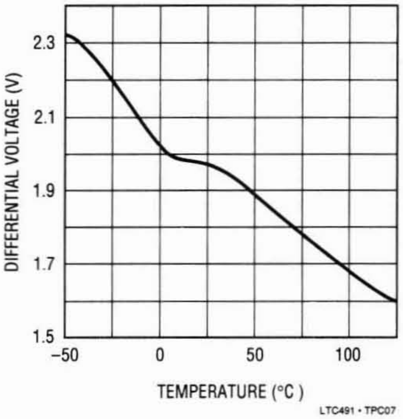
Driver Skew vs Temperature



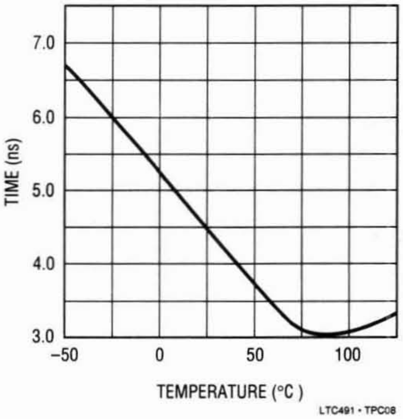
Supply Current vs Temperature



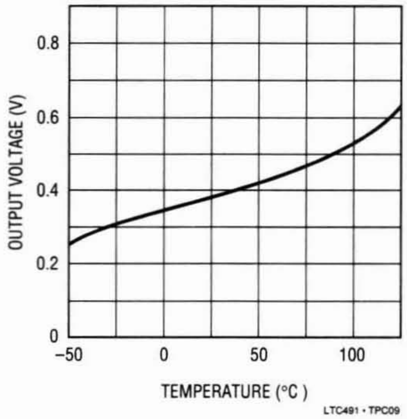
Driver Differential Output Voltage vs Temperature $R_O = 54Ω$



Receiver $|t_{PLH}\ t_{PHL}|$ vs Temperature



Receiver Output Low Voltage vs Temperature at I = 8mA



TEST CIRCUITS

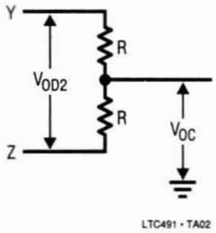

Y
R
V_{OD2}
R
V_{OC}
Z
LTC491 • TA02

Figure 1. Driver DC Test Load

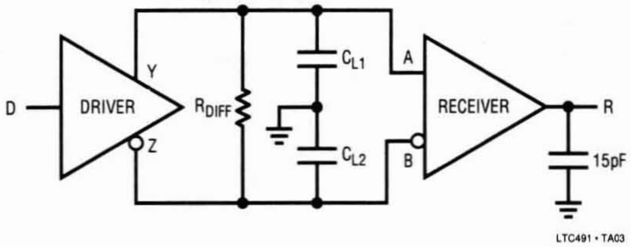

D
DRIVER
Y
Z
R_{DIFF}
C_{L1}
C_{L2}
A
B
RECEIVER
R
15pF
LTC491 • TA03

Figure 2. Driver/Receiver Timing Test Circuit

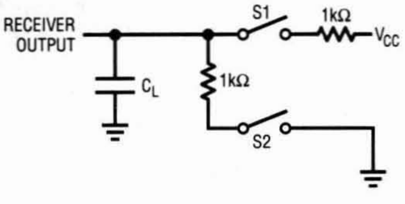

RECEIVER OUTPUT
C_L
1kΩ
S1
1kΩ
V_{CC}
S2
LTC491 • TA04

Figure 3. Receiver Timing Test Load

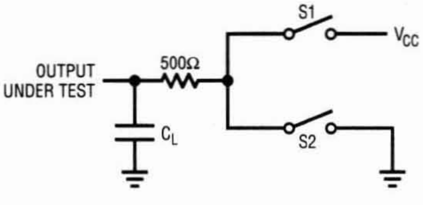

OUTPUT UNDER TEST
500Ω
C_L
S1
V_{CC}
S2
LTC491 • TA05

Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

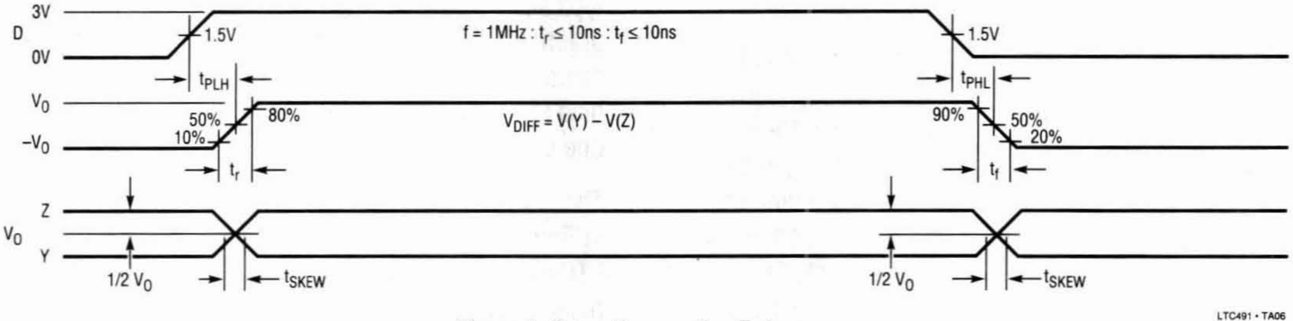

3V
D
0V
1.5V
f = 1MHz : $t_r \leq$ 10ns : $t_f \leq$ 10ns
1.5V
t_{PLH}
t_{PHL}
V_O
$-V_O$
50%
10%
80%
V_{DIFF} = V(Y) – V(Z)
90%
50%
20%
t_r
t_f
Z
V_O
Y
1/2 V_O
t_{SKEW}
1/2 V_O
t_{SKEW}
LTC491 • TA06

Figure 5. Driver Propagation Delays

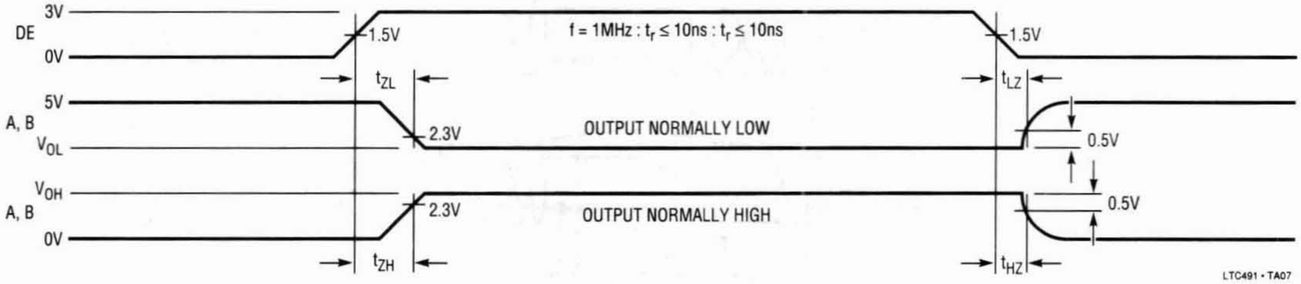

3V
DE
0V
1.5V
f = 1MHz : $t_r \leq$ 10ns : $t_f \leq$ 10ns
1.5V
t_{ZL}
t_{LZ}
5V
A, B
V_{OL}
2.3V
OUTPUT NORMALLY LOW
0.5V
V_{OH}
A, B
0V
2.3V
OUTPUT NORMALLY HIGH
0.5V
t_{ZH}
t_{HZ}
LTC491 • TA07

Figure 6. Driver Enable and Disable Times

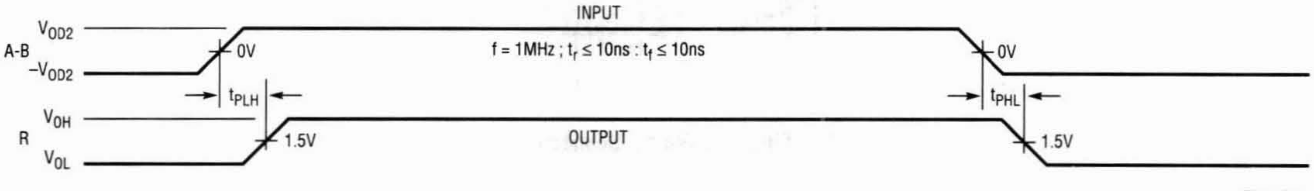

INPUT
V_{OD2}
A-B
$-V_{OD2}$
0V
f = 1MHz ; $t_r \leq$ 10ns : $t_f \leq$ 10ns
0V
t_{PLH}
t_{PHL}
V_{OH}
R
V_{OL}
1.5V
OUTPUT
1.5V
LTC491 • TA08

Figure 7. Receiver Propagation Delays

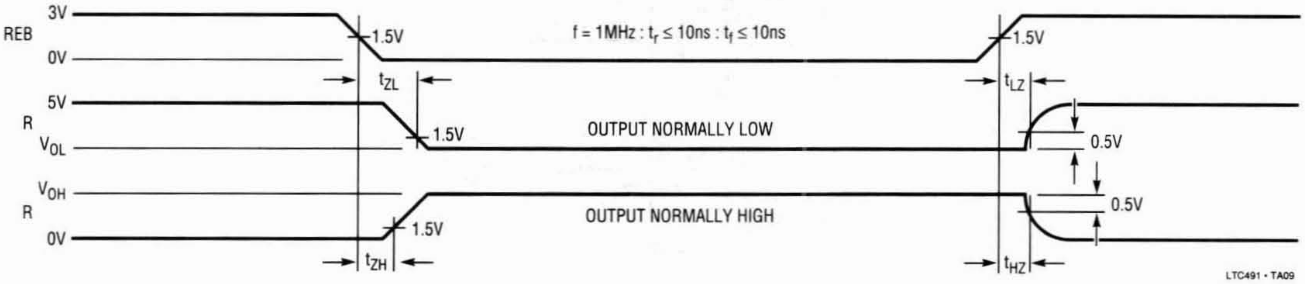

3V
REB
0V
1.5V
f = 1MHz : $t_r \leq$ 10ns : $t_f \leq$ 10ns
1.5V
t_{ZL}
t_{LZ}
5V
R
V_{OL}
1.5V
OUTPUT NORMALLY LOW
0.5V
V_{OH}
R
0V
1.5V
OUTPUT NORMALLY HIGH
0.5V
t_{ZH}
t_{HZ}
LTC491 • TA09

Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Typical Application

A typical connection of the LTC491 is shown in Figure 9. Two twisted pair wires connect up to 32 driver/receiver pairs for full duplex data transmission. There are no restrictions on where the chips are connected to the wires, and it isn't necessary to have the chips connected at the ends. However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120Ω. The input impedance of a receiver is typically 20kΩ to GND, or 0.6 unit RS-485 load, so in practice 50 to 60 transceivers can be connected to the same wires. The optional shields around the twisted pair help reduce unwanted noise, and are connected to GND at one end.

The LTC491 can also be used as a line repeater as shown in Figure 10. If the cable length is longer than 4000 feet, the LTC491 is inserted in the middle of the cable with the receiver output connected back to the driver input.

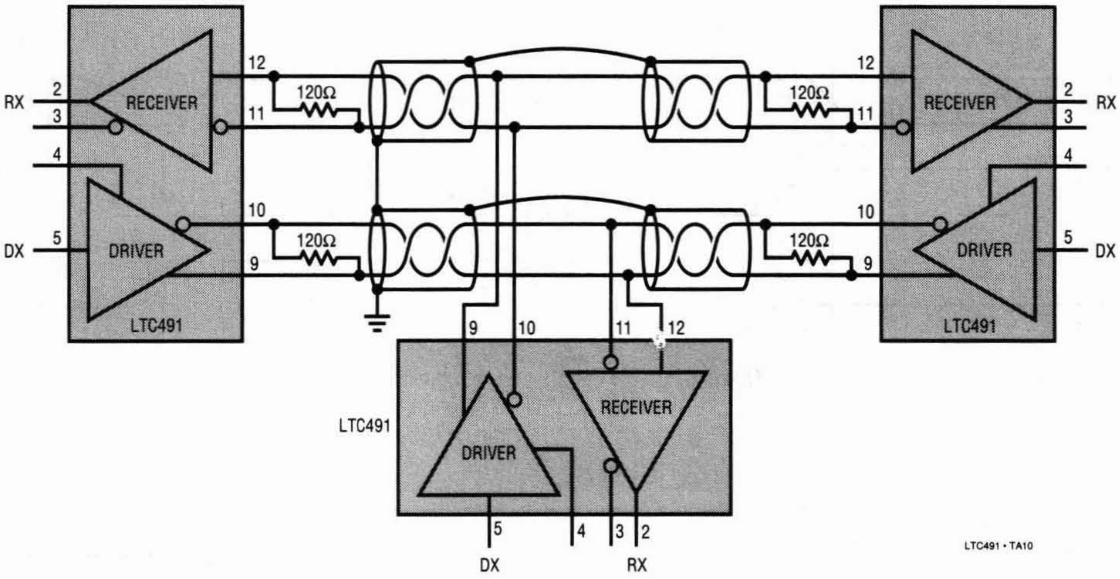

RX
2
3
4
DX
5
RECEIVER
DRIVER
LTC491
12
11
10
9
120Ω
120Ω
120Ω
120Ω
RECEIVER
DRIVER
LTC491
12
11
10
9
2
3
4
5
RX
DX
9
10
11
12
LTC491
DRIVER
RECEIVER
5
4
3
2
DX
RX
LTC491 • TA10

Figure 9. Typical Connection

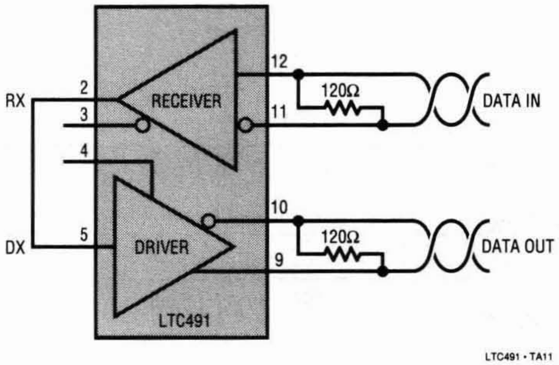

RX
DX
2
3
4
5
RECEIVER
DRIVER
LTC491
12
11
10
9
120Ω
120Ω
DATA IN
DATA OUT
LTC491 • TA11

Figure 10. Line Repeater

APPLICATIONS INFORMATION

Thermal Shutdown

The LTC491 has a thermal shutdown feature which protects the part from excessive power dissipation. If the outputs of the driver are accidently shorted to a power supply or low impedance source, up to 250mA can flow through the part. The thermal shutdown circuit disables the driver outputs when the internal temperature reaches 150°C and turns them back on when the temperature cools to 130°C. If the outputs of two or more LTC491 drivers are shorted directly, the driver outputs can not supply enough current to activate the thermal shutdown. Thus, the thermal shutdown circuit will not prevent contention faults when two drivers are active on the bus at the same time.

Cables and Data Rate

The transmission line of choice for RS485 applications is a twisted pair. There are coaxial cables (twinaxial) made for this purpose that contain straight pairs, but these are less flexible, more bulky, and more costly than twisted pairs. Many cable manufacturers offer a broad range of 120Ω cables designed for RS485 applications.

Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage and AC losses in the dielectric. In good polyethylene cables such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low over all loss (Figure 11).

When using low loss cables, Figure 12 can be used as a guideline for choosing the maximum line length for a given data rate. With lower quality PVC cables, the dielectric loss factor can be 1000 times worse. PVC twisted pairs have terrible losses at high data rates (>100kBs), and greatly reduce the maximum cable length. At low data rates however, they are acceptable and much more economical.

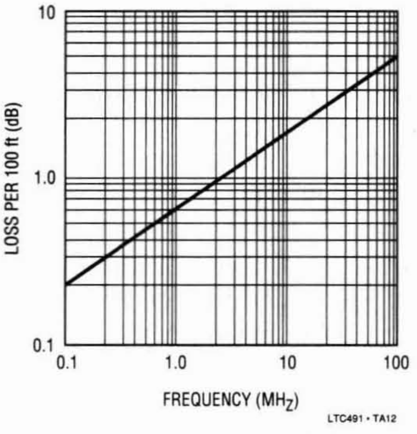


Figure 11. Attenuation vs Frequency for Belden 9481

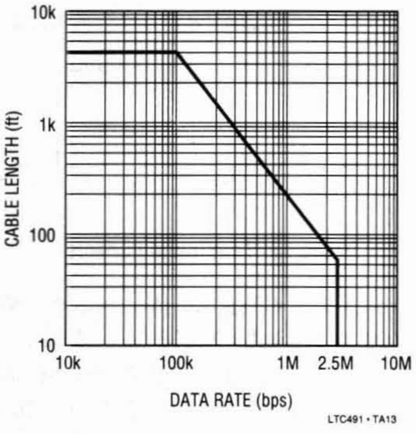


Figure 12. Cable Length vs Data Rate

APPLICATIONS INFORMATION

Cable Termination

The proper termination of the cable is very important. If the cable is not terminated with it's characteristic impedance, distorted waveforms will result. In severe cases, distorted (false) data and nulls will occur. A quick look at the output of the driver will tell how well the cable is terminated. It is best to look at a driver connected to the end of the cable, since this eliminates the possibility of getting reflections from two directions. Simply look at the driver output while transmitting square wave data. If the cable is terminated properly, the waveform will look like a square wave (Figure 13).

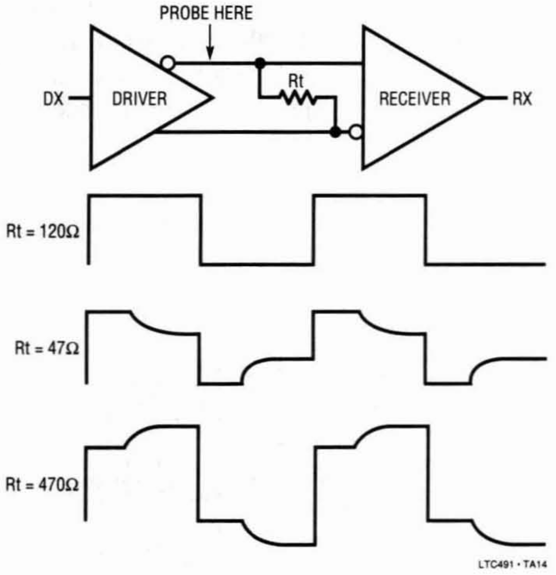


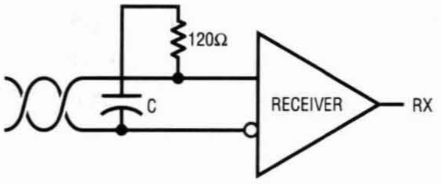
Figure 13. Termination Effects

If the cable is loaded excessively (47Ω), the signal initially sees the surge impedance of the cable and jumps to an initial amplitude. The signal travels down the cable and is reflected back out of phase because of the mistermination. When the reflected signal returns to the driver, the amplitude will be lowered. The width of the pedestal is equal to twice the electrical length of the cable (about 1.5ns/foot).

If the cable is lightly loaded (470Ω), the signal reflects in phase and increases the amplitude at the driver output. An input frequency of 30kHz is adequate for tests out to 4000 feet of cable.

AC Cable Termination

Cable termination resistors are necessary to prevent unwanted reflections, but they consume power. The typical differential output voltage of the driver is 2V when the cable is terminated with two 120Ω resistors, causing 33mA of DC current to flow in the cable when no data is being sent. This DC current is about 60 times greater than the supply current of the LTC491. One way to eliminate the unwanted current is by AC coupling the termination resistors as shown in Figure 14.



C = LINE LENGTH (ft) x 16.3pF

LTC491 • TA15

Figure 14. AC Coupled Termination

The coupling capacitor must allow high-frequency energy to flow to the termination, but block DC and low frequencies. The dividing line between high and low frequency depends on the length of the cable. The coupling capacitor must pass frequencies above the point where the line represents an electrical one-tenth wavelength. The value of the coupling capacitor should therefore be set at 16.3pF per foot of cable length for 120Ω cables. With the coupling capacitors in place, power is consumed only on the signal edges, and not when the driver output is idling at a 1 or 0 state. A 100nF capacitor is adequate for lines up to 4000 feet in length. Be aware that the power savings start to decrease once the data rate surpasses 1/(120Ω × C).

APPLICATIONS INFORMATION

Receiver Open-Circuit Fail-Safe

Some data encoding schemes require that the output of the receiver maintains a known state (usually a logic 1) when the data is finished transmitting and all drivers on the line are forced into three-state. The receiver of the LTC491 has a fail-safe feature which guarantees the output to be in a logic 1 state when the receiver inputs are left floating (open-circuit). However, when the cable is terminated with 120Ω, the differential inputs to the receiver are shorted together, not left floating. Because the receiver has about 70mV of hysteresis, the receiver output will maintain the last data bit received.

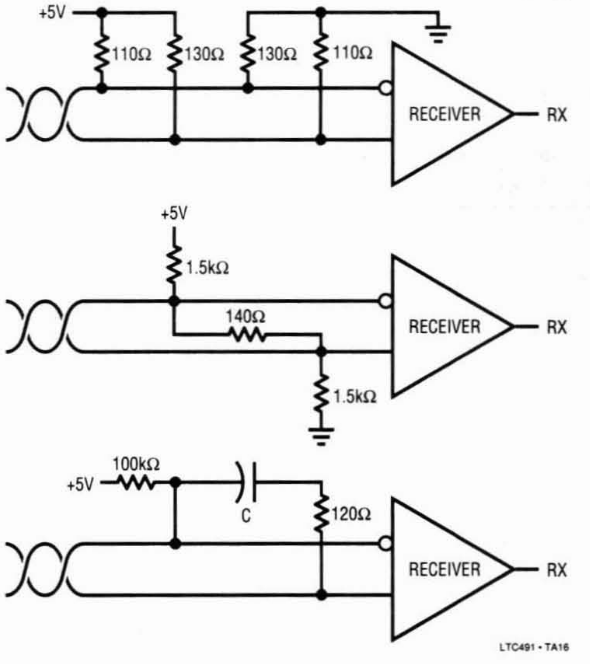


Figure 15. Forcing "0" When All Drivers are Off

The termination resistors are used to generate a DC bias which forces the receiver output to a known state, in this case a logic 0. The first method consumes about 208mW and the second about 8mW. The lowest power solution is to use an AC termination with a pull-up resistor. Simply swap the receiver inputs for data protocols ending in logic 1.

Fault Protection

All of LTC's RS485 products are protected against ESD transients up to 2kV using the human body model (100pF, 1.5kΩ). However, some applications need more protection. The best protection method is to connect a bidirectional TransZorb from each line side pin to ground (Figure 16).

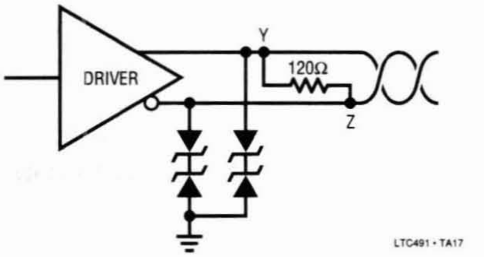
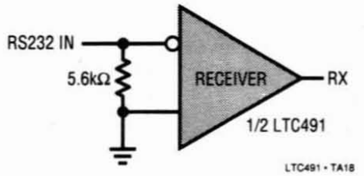


Figure 16. ESD Protection with TransZorbs

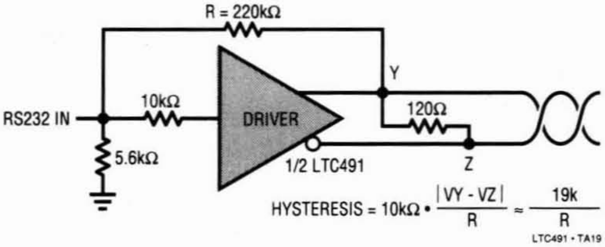
A TransZorb is a silicon transient voltage suppressor that has exceptional surge handling capabilities, fast response time, and low series resistance. They are available from General Semiconductor Industries and come in a variety of breakdown voltages and prices. Be sure to pick a breakdown voltage higher than the common mode voltage required for your application (typically 12V). Also, don't forget to check how much the added parasitic capacitance will load down the bus.

TYPICAL APPLICATIONS

RS232 Receiver


RS232 IN
5.6kΩ
RECEIVER
RX
1/2 LTC491
LTC491 • TA18

RS232 to RS485 Level Transistor with Hysteresis


R = 220kΩ
Y
10kΩ
120Ω
RS232 IN
DRIVER
5.6kΩ
1/2 LTC491
Z
HYSTERESIS = 10kΩ • |VY - VZ| / R ≈ 19k / R
LTC491 • TA19

SECTION 6—DATA CONVERSION

SECTION 6—DATA CONVERSION

INDEX 6-2
SELECTION GUIDES 6-3
PROPRIETARY PRODUCTS
LTC1096/LTC1098, Micropower, Sampling 8-Bit Serial I/O A/D Converters 13-33
LTC1196/LTC1198, 8-Bit, 600ns, 1.3MHz Sampling A/D Converters 13-64
LTC1272, 12-Bit, 3μs, 250kHz Sampling A/D Converter 6-6
LTC1287, 3V Single Chip 12-Bit Data Acquisition System 6-25
LTC1289, 3V Single Chip 12-Bit Data Acquisition System 6-40
LTC1290, Single Chip 12-Bit Data Acquisition System 6-67
LTC1291, Single Chip 12-Bit Data Acquisition System 13-92
LTC1292, Single Chip 12-Bit Data Acquisition System 6-94
LTC1293/LTC1294/LTC1296, Single Chip 12-Bit Data Acquisition System 6-113

ANALOG TO DIGITAL CONVERTERS

- Serial Output 8-Bit Micropower SO-8
  - Single Input
    - LTC1096 (16µs)
  - 2 Channel MUX
    - LTC1098 (16µs)
- Parallel Output 8-Bit High Speed
  - LTC1099 (2.5µs)
- 12-Bit High Speed
  - LTC1272 (3µs, 5µs, 8µs Sampling)
- 10-Bit with MUX
  - Single Input
    - LTC1092 (20µs)
  - 2 Channel MUX
    - LTC1091 (20µs)
  - 6 Channel MUX
    - LTC1093 (20µs)
    - LTC1095 (20µs, Reference)
  - 8 Channel MUX
    - LTC1090 (20µs)
    - LTC1094 (20µs)
- 12-Bit with MUX
  - Single Input
    - LTC1292 (13µs)
  - 2 Channel MUX
    - LTC1291 (13µs)
  - 6 Channel MUX
    - LTC1293 (13µs)
  - 8 Channel MUX
    - LTC1290 (13µs)
    - LTC1294 (13µs)
    - LTC1289 (3.3V Operation, 26µs)

DATA ACQUISITION SELECTION GUIDE

MILITARY AND COMMERCIAL

PART NUMBER	DESCRIPTION	RESOLU-TION	TOTAL UNADJUSTED ERROR	CONV. TIME	VOLTAGE SUPPLY	MAXIMUM SUPPLY CURRENT	PKGS. AVAIL.	IMPORTANT FEATURES
LTC1090C, M	10-Bit, Serial I/O, Analog to Digital Converter with 8 Channel Multiplexer. Full Duplex Serial Interface.	10 Bits	±1/2LSB (LTC1090A) Over Full Temperature Range	22µs	5V, 10V, or ±5V	2.5mA	J, N, S	10-Bit A to D with Built in 8 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Full Duplex Serial I/O.
LTC1091C, M	10-Bit, 8-Pin Serial I/O, Analog to Digital Converter with 2 Channel Analog Multiplexer.	10 Bits	±1/2LSB (LTC1091A) Over Full Temperature Range	20µs	5V or 10V	3.5mA	J8, N8	10-Bit A to D with Built in 2 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Unipolar Operation.
LTC1092C, M	10-Bit, 8-Pin, Analog to Digital Converter with Serial Output.	10 Bits	±1/2LSB (LTC1092A) Over Full Temperature Range	20µs	5V or 10V	2.5mA	J8, N8	Separate Reference Pin Allows Reduced Span (Down to 200mV) Operation. Unipolar A to D Conversions are Performed on a Differential Input Pair. Compatible with All Microprocessors with Serial Ports.
LTC1093C, M	10-Bit, Serial I/O, Analog to Digital Converter with 6 Channel Multiplexer.	10 Bits	±1/2LSB (LTC1093A) Over Full Temperature Range	20µs	5V, 10V, or ±5V	2.5mA	J, N, S	10-Bit A to D with Built in 6 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.
LTC1094C, M	10-Bit, Serial I/O, Analog to Digital Converter System with 8 Channel Multiplexer.	10 Bits	±1/2LSB (LTC1094A) Over Full Temperature Range	20µs	5V, 10V, or ±5V	2.5mA	J, N	10-Bit A to D with Built in 8 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.
LTC1095C, M	10-Bit, Serial I/O, Analog to Digital Converter with 6 Channel Multiplexer and 5V Buried Zener Reference.	10 Bits	±0.15% FSR	20µs	7.2V to 10V	3.7mA	J	10-Bit ADC with Built in 6 Channel Analog MUX, Sample/Hold, and 5V Buried Zener Reference. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.
LTC1096	8-Bit, 16µs, Micropower, Sampling A/D Converter with Serial I/O and Differential Input.	8 Bits	±1/2LSB (LTC1096A) Over Full Temperature Range	16µs	3V to 9V	80µA	N8, S8	Single Differential Input, S/H with Single Ended Inputs. Ultra-Low Power. Automatic Power-Down Mode.
LTC1098	8-Bit, 16µs, Micropower, Sampling A/D Converter with Serial I/O and 2 Channel MUX	8 Bits	±1/2LSB (LTC1098A) Over Full Temperature Range	16µs	3V to 9V	80µA	N8, S8	2 Channel Multiplexer, Sampling ADC. Ultra-Low Power, Automatic Power-Down Mode.
LTC1099C, M	8-Bit, 2µs Analog to Digital Converter with Built in Sample-and-Hold. Parallel Output.	8 Bits	±1LSB Over Full Temperature Range	2µs	5V	15mA	J, N, S	Built in S/H Allows Direct Conversion of 5Vp-p Signals up to 167kHz. Pin Compatible with ADC0820 and AD7820.
LTC1272C, M	12-Bit, 3µs, Sampling A/D Converter with Parallel Output.	12 Bits	±1/2LSB Linearity, ±3LSB Offset, ±10LSB Full/Scale Error	3µs	5V	20mA	J, N, S	Single Supply, Sampling Plug in Upgrade for AD7572. 250kHz Sample Rate. Operates with or without –15V Supply Required by AD7572.

MILITARY AND COMMERCIAL

PART NUMBER	DESCRIPTION	RESOLU-TION	TOTAL UNADJUSTED ERROR	CONV. TIME	VOLTAGE SUPPLY	MAXIMUM SUPPLY CURRENT	PKGS. AVAIL.	IMPORTANT FEATURES
LTC1290C, M	12-Bit, Serial I/O, Analog to Digital Converter with 8 Channel Multiplexer. Full Duplex Serial Interface.	12 Bits	±2.5LSB Over Full Temperature Range (LTC1290B)	13µs	5V, or ±5V	5mA	J, N, S	12-Bit ADC with Built in 8 Channel Analog MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Full Duplex Serial I/O.
LTC1292C	12-Bit, 8-Pin Analog to Digital Converter with Serial Output.	12 Bits	±2.5LSB Over Full Temperature Range (LTC1292B)	13µs	5V	5mA	J, N	12-Bit ADC, Unipolar Conversion of Single Differential Input. Separate Reference Pin Allows Reduced Span. Compatible with All Microprocessors with Serial Ports.
LTC1293C	12-Bit, Serial I/O, Analog to Digital Converter System with 6 Channel Multiplexer.	12 Bits	±2.5LSB Over Full Temperature Range (LTC1293B)	13µs	5V, or ±5V	5mA	J, N	12-Bit ADC with Built in 8 Channel MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Full Duplex Serial I/O.
LTC1294C	12-Bit, Serial I/O, Analog to Digital Converter System with 8 Channel Multiplexer.	12 Bits	±2.5LSB Over Full Temperature Range (LTC1294B)	13µs	5V, or ±5V	5mA	J, N	12-Bit ADC with Built in 8 Channel MUX and Sample/Hold. Compatible with All Microprocessors with Serial Ports. Software Configurable Bipolar or Unipolar Operation. Half Duplex Serial I/O.

LTC1272

12-Bit, 3µs, 250kHz Sampling A/D Converter

FEATURES

- AD7572 Pin Out
- 12-Bit Resolution
- 3µs, 5µs, 8µs Conversion Times
- On-Chip Sample-and-Hold
- Up to 250kHz Sample Rates
- +5V Single Supply Operation
- No Negative Supply Required
- On-Chip 25ppm/°C Reference
- 75mW (Typ) Power Consumption
- 24-Pin Narrow DIP and SO Packages
- ESD Protected on all Pins

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing (DSP)
- Multiplexed Data Acquisition Systems
- Single Supply Systems

DESCRIPTION

The LTC1272 is a 3µs, 12-bit, successive approximation sampling A/D converter. It has the same pinout as the industry standard AD7572 and offers faster conversion time, on-chip sample-and-hold, and single supply operation. It uses LTBiCMOS™ switched capacitor technology to combine a high speed 12-bit ADC with a fast, accurate sample-and-hold and a precision reference.

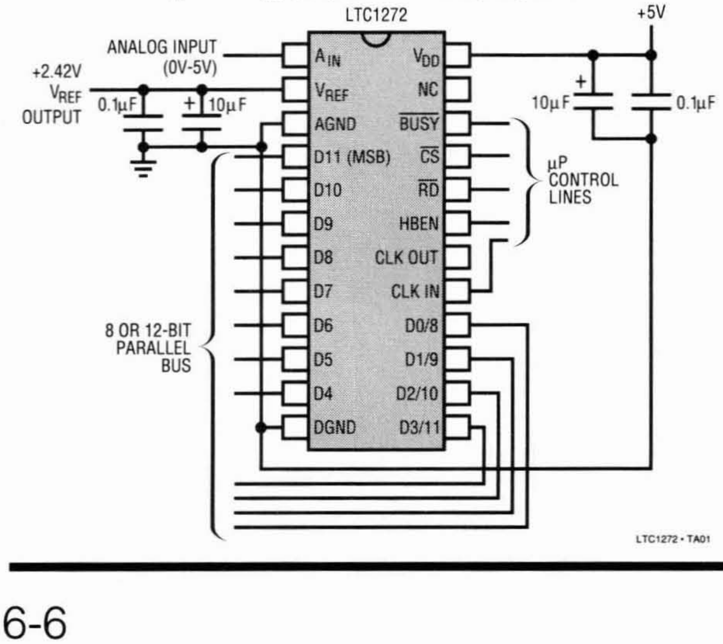
The LTC1272 operates with a single +5V supply but can also accept the +5V/–15V supplies required by the AD7572 (Pin 23, the negative supply pin of the AD7572, is not connected on the LTC1272). The LTC1272 has the same 0V to 5V input range as the AD7572 but, to achieve single supply operation, it provides a +2.42V reference output instead of the –5.25V of the AD7572. It plugs in for the AD7572 if the reference capacitor polarity is reversed and a 1µs sample-and-hold acquisition time is allowed between conversions.

The output data can be read as a 12-bit word or as two 8-bit bytes. This allows easy interface to both 8-bit and higher processors. The LTC1272 can be used with a crystal or an external clock and comes in speed grades of 3µs, 5µs, and 8µs.

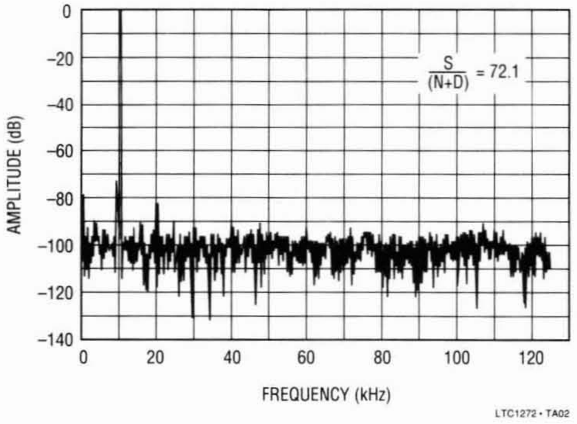
LTBiCMOS™ is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

Single 5V Supply, 3µs, 12-Bit Sampling ADC


LTC1272
+5V
ANALOG INPUT (0V-5V)
+2.42V V_REF OUTPUT
0.1µF
10µF
A_IN
V_REF
AGND
D11 (MSB)
D10
D9
D8
D7
D6
D5
D4
DGND
V_DD
NC
BUSY
CS
RD
HBEN
CLK OUT
CLK IN
D0/8
D1/9
D2/10
D3/11
10µF
0.1µF
µP CONTROL LINES
8 OR 12-BIT PARALLEL BUS
LTC1272 • TA01

1024 Point FFT, f_S = 250kHz, f_{IN} = 10kHz

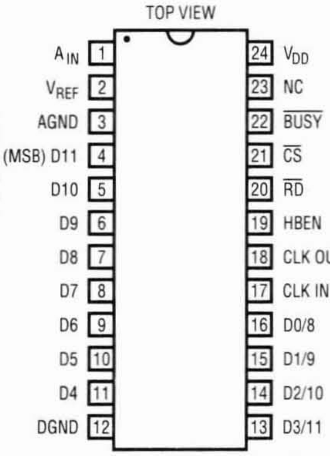


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

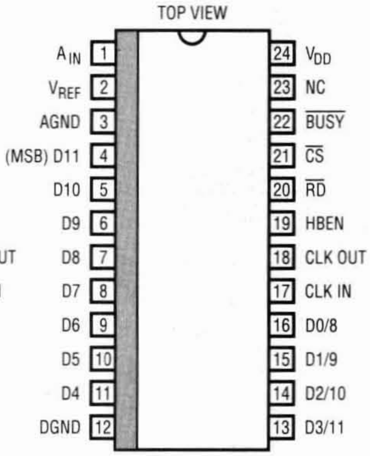
Supply Voltage (V_{DD})	6V
Analog Input Voltage (Note 3)	−0.3V to +15V
Digital Input Voltage	−0.3V to 12V
Digital Output Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation	500mW
Operating Temperature Range	
LTC1272-XAC, BC, CC	0°C to 70°C
LTC1272-XAM, BM, CM	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION


TOP VIEW
A IN 1
VREF 2
AGND 3
(MSB) D11 4
D10 5
D9 6
D8 7
D7 8
D6 9
D5 10
D4 11
DGND 12
24 VDD
23 NC
22 BUSY
21 CS
20 RD
19 HBEN
18 CLK OUT
17 CLK IN
16 D0/8
15 D1/9
14 D2/10
13 D3/11

J PACKAGE 24-LEAD CERAMIC DIP N PACKAGE 24-LEAD PLASTIC DIP

LTC1272 • POI01


TOP VIEW
A IN 1
VREF 2
AGND 3
(MSB) D11 4
D10 5
D9 6
D8 7
D7 8
D6 9
D5 10
D4 11
DGND 12
24 VDD
23 NC
22 BUSY
21 CS
20 RD
19 HBEN
18 CLK OUT
17 CLK IN
16 D0/8
15 D1/9
14 D2/10
13 D3/11

S PACKAGE 24-LEAD PLASTIC SOIC

LTC1272 • POI02

ORDER PART NUMBER		
CONVERSION TIME = 3µs	CONVERSION TIME = 5µs	CONVERSION TIME = 8µs
LTC1272-3AMJ LTC1272-3BMJ LTC1272-3CMJ	LTC1272-5AMJ LTC1272-5BMJ LTC1272-5CMJ	LTC1272-8AMJ LTC1272-8BMJ LTC1272-8CMJ
LTC1272-3ACJ LTC1272-3BCJ LTC1272-3CCJ	LTC1272-5ACJ LTC1272-5BCJ LTC1272-5CCJ	LTC1272-8ACJ LTC1272-8BCJ LTC1272-8CCJ
LTC1272-3ACN LTC1272-3BCN LTC1272-3CCN	LTC1272-5ACN LTC1272-5BCN LTC1272-5CCN	LTC1272-8ACN LTC1272-8BCN LTC1272-8CCN
S PACKAGE ONLY		
LTC1272-3ACS LTC1272-3BCS LTC1272-3CCS	LTC1272-5ACS LTC1272-5BCS LTC1272-5CCS	LTC1272-8ACS LTC1272-8BCS LTC1272-8CCS

CONVERTER CHARACTERISTICS With Internal Reference (Note 4)

				LTC1272-XA			LTC1272-XB			LTC1272-XC			
PARAMETER	**CONDITIONS**			**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Resolution (No Missing Codes)			●	12			12			12			Bits
Integral Linearity Error	(Note 5)					±1/2			±1			±1	LSB
		Com	●			±1/2			±1			±1	
		Mil	●			±3/4			±1			±1	
Differential Linearity Error			●			±1			±1			±1	LSB
Offset Error						±3			±3			±4	LSB
			●			±4			±5			±6	
Gain Error						±10			±10			±15	LSB
Full Scale Tempco	I_{OUT} (Reference) = 0		●		±5	±25		±10	±25		±10	±45	ppm/°C

INTERNAL REFERENCE CHARACTERISTICS (Note 4)

			LTC1272-XA/B			LTC1272-XC			
PARAMETER	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{REF} Output Voltage (Note 6)	I_{OUT} = 0		2.400	2.420	2.440	2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		5	25		10	45	ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V, I_{OUT} = 0			0.01			0.01		LSB/V
V_{REF} Load Regulation (Sourcing Current)	0 ≤ $\lvert I_{OUT}\rvert$ ≤ 1mA			2			2		LSB/mA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 4)

				LTC1272-XA/B/C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{IH}	High Level Input Voltage $\overline{CS}$, $\overline{RD}$, HBEN, CLK_{IN}	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage $\overline{CS}$, $\overline{RD}$, HBEN, CLK_{IN}	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Input Current $\overline{CS}$, $\overline{RD}$, HBEN	V_{IN} = 0V to V_{DD}	●			±10	µA
I_{IN}	Input Current CLK_{IN}	V_{IN} = 0V to V_{DD}	●			±20	µA
V_{OH}	High Level Output Voltage All Logic Outputs	V_{DD} = 4.75V, I_{OUT} = −10µA			4.7		V
		I_{OUT} = −200µA	●	4.0			
V_{OL}	Low Level Output Voltage All Logic Outputs	V_{DD} = 4.75V, I_{OUT} = 1.6mA	●			0.4	V
I_{OZ}	High-Z Output Leakage D11-D0/8	V_{OUT} = 0V to V_{DD}	●			±10	µA
C_{OZ}	High-Z Output Capacitance (Note 7)		●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA
I_{DD}	Positive Supply Current	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, A_{IN} = 5V	●		15	30	mA
PD	Power Dissipation				75		mW

DYNAMIC ACCURACY (Note 4) f_{SAMPLE} = 250kHz (LTC1272-3), 166kHz (LTC1272-5), 111kHz (LTC1272-8)

			LTC1272-XA/B/C			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
S/(N + D)	Signal to Noise Plus Distortion Ratio	10kHz Input Signal		72		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	10kHz Input Signal		−82		dB
	Peak Harmonic or Spurious Noise	10kHz Input Signal		−82		dB

ANALOG INPUT (Note 4)

				LTC1272-XA/B/C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input Voltage Range	4.75V ≤ V_{DD} ≤ 5.25V	●	0		+5	V
I_{IN}	Input Current		●			3.5	mA
C_{IN}	Input Capacitance				50		pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		0.45	1	µs

TIMING CHARACTERISTICS (Note 8)

SYMBOL	PARAMETER	CONDITIONS			LTC1272-XA/B/C MIN	TYP	MAX	UNITS
t_1	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Setup Time			●	0			ns
t_2	$\overline{\text{RD}}$ to $\overline{\text{BUSY}}$ Delay	$C_L = 50pF$				80	190	ns
			COM Grade	●			230	
			MIL Grade	●			270	
t_3	Data Access Time After $\overline{\text{RD}}$↓	$C_L = 20pF$				50	90	ns
			COM Grade	●			110	
			MIL Grade	●			120	
		$C_L = 100pF$				70	125	ns
			COM Grade	●			150	
			MIL Grade	●			170	
t_4	$\overline{\text{RD}}$ Pulse Width				t_3			ns
			COM Grade	●	t_3			
			MIL Grade	●	t_3			
t_5	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ Hold Time			●	0			ns
t_6	Data Setup Time After $\overline{\text{BUSY}}$					40	70	ns
			COM Grade	●			90	
			MIL Grade	●			100	
t_7	Bus Relinquish Time				20	30	75	ns
			COM Grade	●	20		85	
			MIL Grade	●	20		90	
t_8	HBEN to $\overline{\text{RD}}$ Setup Time			●	0			ns
t_9	HBEN to $\overline{\text{RD}}$ Hold Time			●	0			ns
t_{10}	Delay Between $\overline{\text{RD}}$ Operations			●	200			ns
t_{11}	Delay Between Conversions				1			µs
t_{12}	Aperture Delay of Sample and Hold	Jitter < 50ps				25		ns
t_{13}	CLK to $\overline{\text{BUSY}}$ Delay					80	170	ns
			COM Grade	●			220	
			MIL Grade	●			260	
t_{CONV}	Conversion Time			●	12		13	CLK Cycles

The ● indicates specs which apply over the full operating temperature range; all other limits and typicals $T_A = 25°C$.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When the analog input voltage is taken below ground it will be clamped by an internal diode. This product can handle, with no external diode, input currents of greater than 60mA below ground without latch-up.

Note 4: $V_{DD} = 5V$, $f_{CLK} = 4MHz$ for LTC1272-3, 2.5MHz for LTC1272-5 and 1.6MHz for LTC1272-8, $t_r = t_f = 5ns$ unless otherwise specified. For best analog performance, the LTC1272 clock should be synchronized to the $\overline{\text{RD}}$ and $\overline{\text{CS}}$ control inputs with at least 40ns separating convert start from the nearest clock edge.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 6: The LTC1272 has the same 0V to 5V input range as the AD7572 but, to achieve single supply operation, it provides a +2.42V reference output instead of the –5.25V of the AD7572. This requires that the polarity of the reference bypass capacitor be reversed when plugging an LTC1272 into an AD7572 socket.

Note 7: Guaranteed by design, not subject to test.

Note 8: $V_{DD} = 5V$. Timing specifications are sample tested at 25°C to ensure compliance. All input control signals are specified with $t_r = t_f = 5ns$ (10% to 90% of +5V) and timed from a voltage level of +1.6V. See Figures 13 through 17.

PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input, 0V to +5V unipolar input.

V_{REF} (Pin 2): +2.42V Reference Output. When plugging into an AD7572 socket, reverse the reference bypass capacitor polarity and short the 10Ω series resistor.

AGND (Pin 3): Analog Ground

D11-D4 (Pins 4-11): Three-State Data Outputs

DGND (Pin 12): Digital Ground

D3/11-D0/8 (Pins 13-16): Three-State Data Outputs

CLK IN (Pin 17): Clock Input. An external TTL/CMOS compatible clock may be applied to this pin or a crystal can be connected between CLK IN and CLK OUT.

CLK OUT (Pin 18): Clock Output. An inverted CLK IN signal appears at this pin.

HBEN (Pin 19): High Byte Enable Input. This pin is used to multiplex the internal 12-bit conversion result into the lower bit outputs (D7-D0/8). See table below. HBEN also disables conversion starts when HIGH.

$\overline{RD}$ (Pin 20): READ Input. This active low signal starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 21): The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ Output is low when a conversion is in progress.

NC (Pin 23): Not connected internally. The LTC1272 does not require negative supply. This pin can accommodate the –15V required by the AD7572 without problems.

V_{DD} (Pin 24): Positive Supply, +5V.

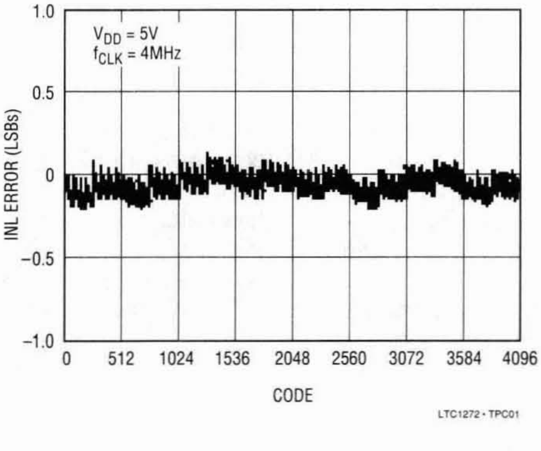
Data Bus Output, $\overline{CS}$ and $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

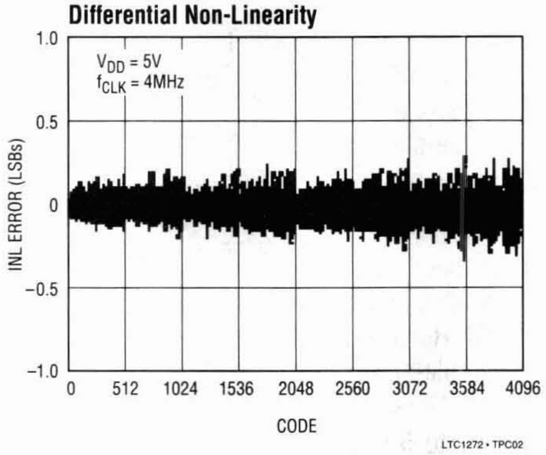
*D11...D0/8 are the ADC data output pins.
DB11...DB0 are the 12-bit conversion results, DB11 is the MSB.

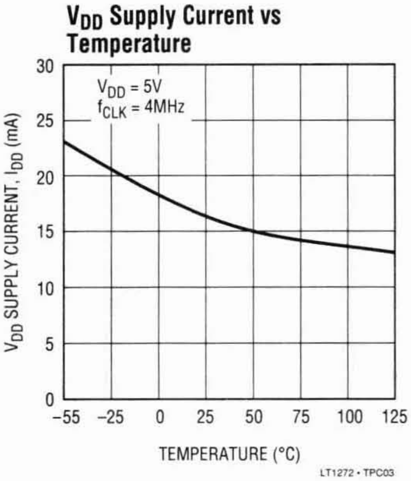
TYPICAL PERFORMANCE CHARACTERISTICS

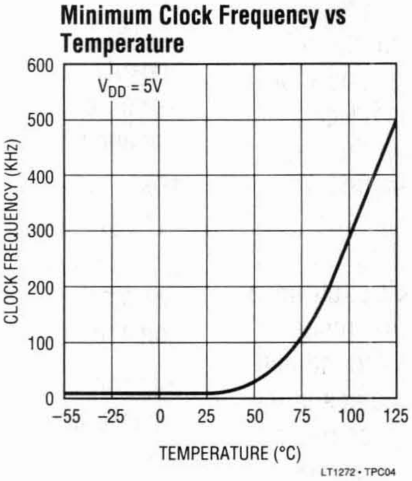
Integral Non-Linearity

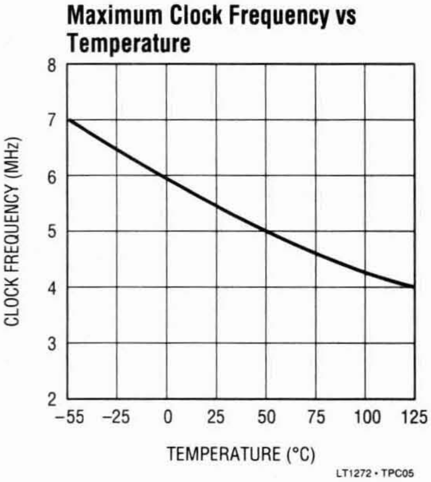


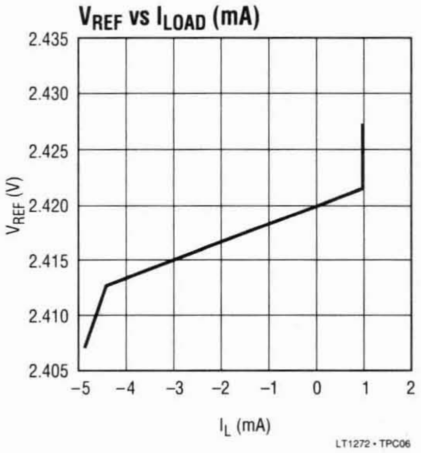
TYPICAL PERFORMANCE CHARACTERISTICS

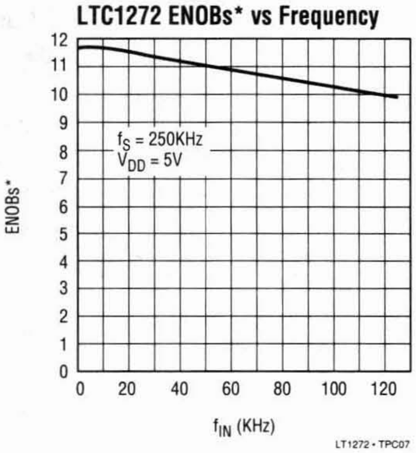












*EFFECTIVE NUMBER OF BITS, ENOBs = $\frac{S/(N + D) - 1.76dB}{6.02}$

APPLICATIONS INFORMATION

Conversion Details

Conversion start is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor through a 300Ω/2.7kΩ divider. The voltage divider allows the LTC1272 to convert 0V to 5V input signals while operating from a 4.5V supply. The conversion has two phases: the sample phase and the convert phase. During the sample phase, the comparator offset is nulled by the feedback switch and the analog input is stored as a charge on the sample-and-hold capacitor, C_{SAMPLE}. This phase lasts from the end of the previous conversion until the next conversion is started. A minimum delay between conversions (t_{10}) of 1µs allows enough time for the analog input to be acquired. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The sample-and-hold capacitor is switched to ground injecting the analog input charge onto the comparator summing junction. This input charge is successively compared to binary weighted charges supplied by the capacitive DAC. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output. The MSB decision is made 50ns (typically) after the second falling edge of CLK IN following a conversion start. Similarly, the succeeding bit decisions are made approximately 50ns after a CLK IN edge until the conversion is finished. At the end of a conversion, the DAC output balances the A_{IN} output charge. The SAR contents (12-bit data word) which represent the A_{IN} input signal are loaded into a 12-bit latch.

Sample-and-Hold and Dynamic Performance

Traditionally A/D converters have been characterized by such specs as offset and full-scale errors, integral non-linearity and differential non-linearity. These specs are useful for characterizing an ADC's DC or low frequency signal performance.

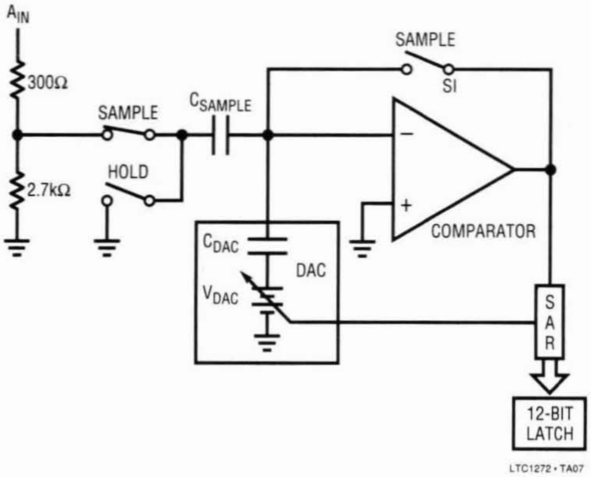


Figure 1. A_{IN} Input

These specs alone are not adequate to fully specify the LTC1272 because of its high speed sampling ability. FFT (Fast Fourrier Transform) test techniques are used to characterize the LTC1272's frequency response, distortion and noise at the rated throughput.

By applying a low distortion sine-wave and analyzing the digital output using a FFT algorithm, the LTC1272's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1272 FFT plot.

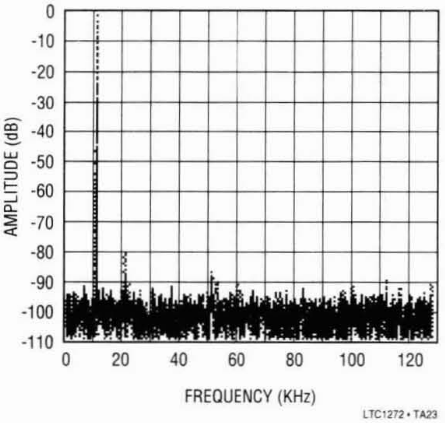


Figure 2. LTC1272 Non-Averaged, 1024 Point FFT Plot. f_S = 250kHz, f_{IN} = 10kHz

APPLICATIONS INFORMATION

Signal to Noise Ratio

The Signal to Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. This includes distortion as well as noise products and for this reason it is sometimes referred to as Signal to Noise + Distortion [S/(N + D)]. The output is band limited to frequencies from DC to one half the sampling frequency. Figure 2 shows spectral content from DC to 125kHz which is 1/2 the 250kHz sampling rate.

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an A/D and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02,$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 250kHz the LTC1272 maintains 11.5 ENOBs or better to 20kHz. Above 20kHz the ENOBs gradually decline, as shown in Figure 3, due to increasing second harmonic distortion. The noise floor remains approximately 90dB. The dynamic differential non-linearity remains good out to 120kHz as shown in Figure 4.

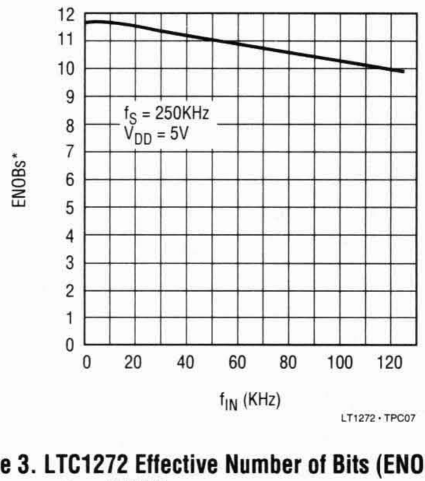


Figure 3. LTC1272 Effective Number of Bits (ENOBs) vs Input Frequency. f_S = 250kHz

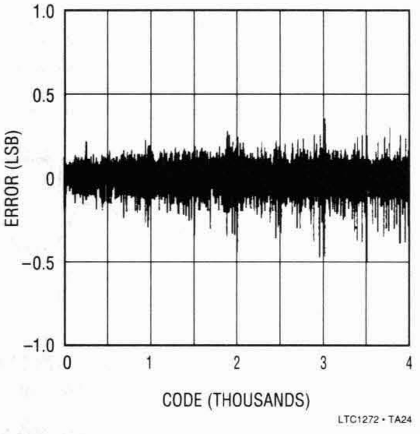


Figure 4. LTC1272 Dynamic DNL. f_{CLK} = 4MHz, f_S = 250kHz, f_{IN} = 122.25342kHz, V_{CC} = 5V

Total Harmonic Distortion

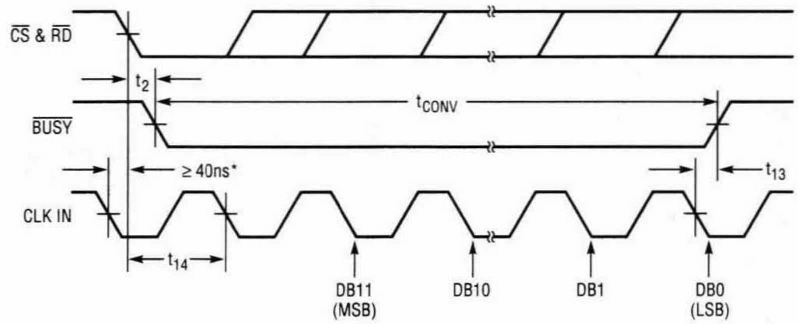
Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The harmonics are limited to the frequency band between DC and one half the sampling frequency. THD is expressed as: $20\ \mathrm{LOG}\ [\sqrt{V_2^2 + V_3^2 + V_N^2} / V_1]$ where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics.

Clock and Control Synchronization

For best analog performance, the LTC1272 clock should be synchronized to the $\overline{CS}$ and $\overline{RD}$ control inputs as shown in Figure 5, with at least 40ns separating convert start from the nearest CLK IN edge. This ensures that transitions at CLK IN and CLK OUT do not couple to the analog input and get sampled by the sample-and-hold. The magnitude of this feedthrough is only a few millivolts, but if CLK and convert start ($\overline{CS}$ and $\overline{RD}$) are asynchronous, frequency components caused by mixing the clock and convert signals may increase the apparent input noise.

When the clock and convert signals are synchronized, small endpoint errors (offset and full scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be eliminated by ensuring that the start of a conversion ($\overline{CS}$ and $\overline{RD}$ falling edge) does not occur within 40ns of a clock edge, as in

APPLICATIONS INFORMATION



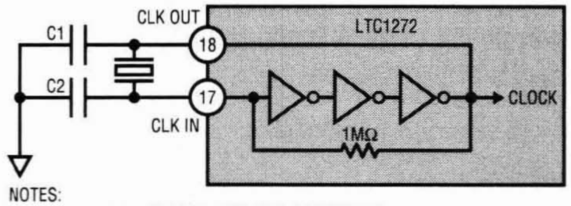
UNCERTAIN CONVERSION TIME FOR 30ns < t_{14} < 180ns

*THE LTC1272 IS ALSO COMPATIBLE WITH THE AD7572 SYNCHRONIZATION MODES.

LTC1272 • TA06

Figure 5. $\overline{\text{RD}}$ and CLK IN for Synchronous Operation

Figure 5. Nevertheless, even without observing this guideline, the LTC1272 is still compatible with AD7572 synchronization modes, with no increase in linearity error. This means that either the falling or rising edge of CLK IN may be near $\overline{\text{RD}}$'s falling edge.



NOTES:
LTC1272-3 – 4MHz CRYSTAL/CERAMIC RESONATOR
LTC1272-5 – 2.5MHz CRYSTAL/CERAMIC RESONATOR
LTC1272-8 – 1.6MHz CRYSTAL/CERAMIC RESONATOR

LTC1272 • TA09

Figure 6. LTC1272 Internal Clock Circuit

Driving the Analog Input

The analog input of the LTC1272 is much easier to drive than that of the AD7572. The input current is not modulated by the DAC as in the AD7572. It has only one small current spike from charging the sample-and-hold capacitor at the end of the conversion. During the conversion the analog input draws only DC Current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion is started. Any op amp that settles in 1µs to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the LTC1272 A_{IN} input include the LT1006 and LT1007 op amps.

Internal Clock Oscillator

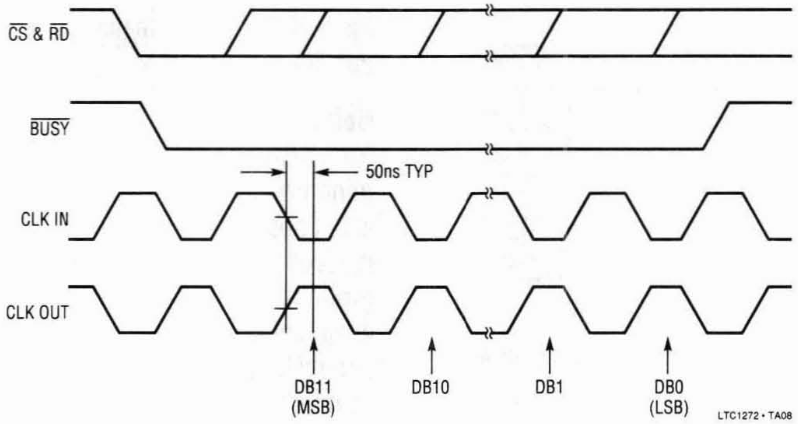
Figure 6 shows the LTC1272 internal clock circuit. A crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18) to provide a clock oscillator for ADC timing. Alternatively the crystal/resonator may be omitted and an external clock source may be connected to CLK IN. For an external clock the duty cycle is not critical. An inverted CLK IN signal will appear at the CLK OUT pin as shown in the operating waveforms of Figure 7. Capacitance on the CLK OUT pin should be minimized for best analog performance.

Internal Reference

The LTC1272 has an on-chip, temperature-compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.42V ±1%. It is internally connected to the DAC and is also available at Pin 2 to provide up to 1mA current to an external load.

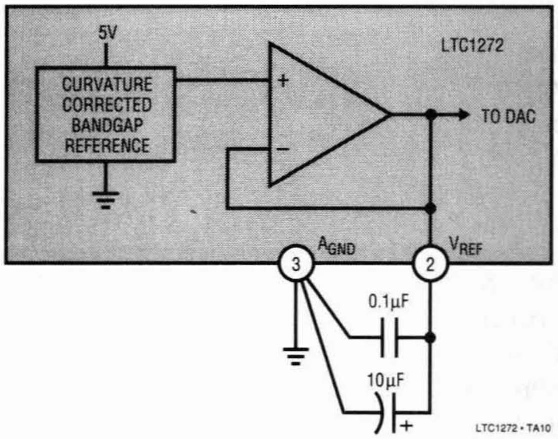
For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic). A simplified schematic of the reference with its recommended decoupling is shown in Figure 8.

APPLICATIONS INFORMATION



CS & RD
BUSY
50ns TYP
CLK IN
CLK OUT
DB11
(MSB)
DB10
DB1
DB0
(LSB)
LTC1272 • TA08

Figure 7. Operating Waveforms Using an External Clock Source for CLK IN



5V
LTC1272
CURVATURE CORRECTED BANDGAP REFERENCE
+
–
TO DAC
A_{GND}
V_{REF}
3
2
0.1µF
10µF
+
LTC1272 • TA10

Figure 8. LTC1272 Internal 2.42V Reference

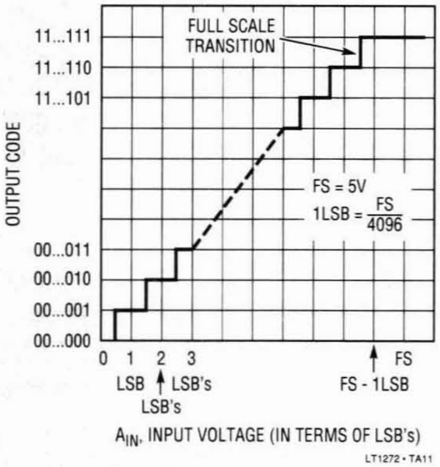


Figure 9. LTC1272 Ideal Input/Output Transfer Characteristic

Unipolar Operation

Figure 9 shows the ideal input/output characteristic for the 0V to 5V input range of the LTC1272. The code transitions occur midway between successive integer LSB values (i.e., 1/2 LSB, 3/2 LSBs, 5/2 LSBs . . . FS-3/2 LSBs). The output code is natural binary with 1 LSB = FS/4096 = (5/4096)V = 1.22mV.

Unipolar Offset and Full-Scale Error Adjustment

In applications where absolute accuracy is important, then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 10 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving A_{IN} (i.e., A1 in Figure 10). For zero offset error apply 0.61mV (i.e., 1/2 LBS) at V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

For zero full-scale error apply an analog input of 4.99817V (i.e., FS-3/2 LSBs or last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

APPLICATIONS INFORMATION

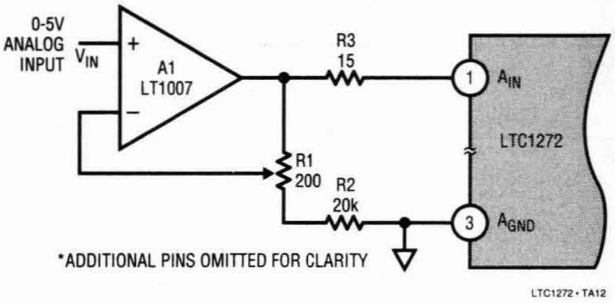


Figure 10. Unipolar 0V to +5V Operation with Gain Error Adjust

Application Hints

Wire wrap boards are not recommended for high resolution or high-speed A/D converters. To obtain the best performance from the LTC1272 a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the LTC1272. The analog input should be screened by AGND.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at Pin 3 (AGND) or as close as possible to the LTC1272, as shown in Figure 11. Pin 12 (LTC1272 DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to A_{IN} and signal return leads from AGND (Pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potiential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the LTC1272 data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the LTC1272 data bus.

Timing and Control

Conversion start and data read operations are controlled by three LTC1272 digital inputs; HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 12 shows the logic structure associated with these inputs. The three signals are internally gated so that a logic "0" is required on all three inputs to initiate a conversion. Once initiated it cannot be restarted until conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

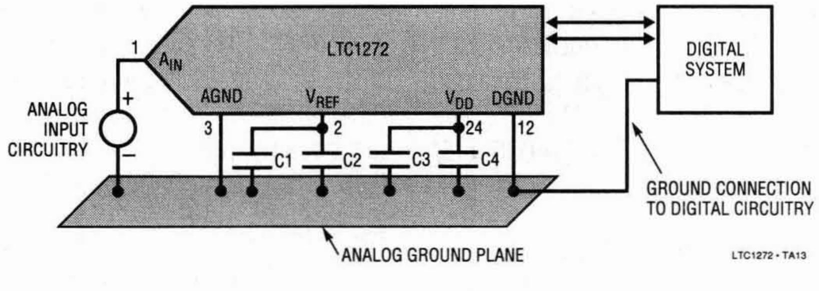
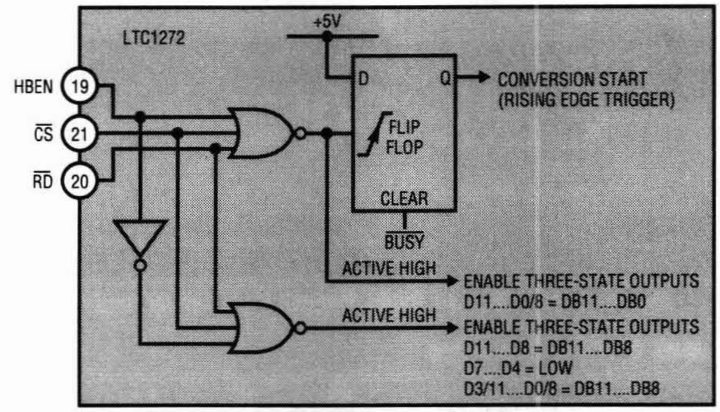


Figure 11. Power Supply Grounding Practice

APPLICATIONS INFORMATION

There are two modes of operation as outlined by the timing diagrams of Figures 13 to 17. Slow Memory Mode is designed for microprocessors which can be driven into a WAIT state, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and data is read when conversion is complete.

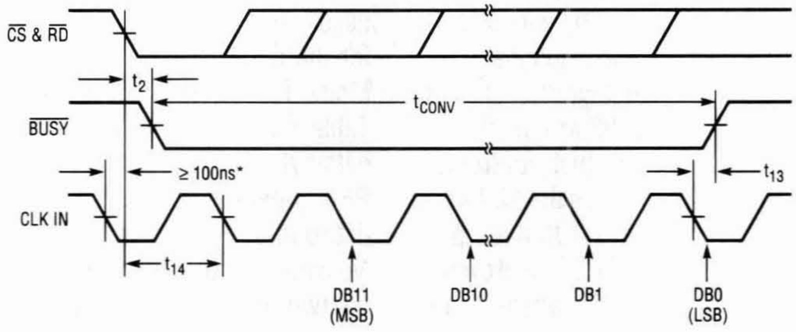
The second is the ROM Mode which does not require microprocessor WAIT states. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result.


LTC1272
+5V
HBEN 19
$\overline{CS}$ 21
$\overline{RD}$ 20
D
Q
FLIP FLOP
CLEAR
$\overline{BUSY}$
CONVERSION START (RISING EDGE TRIGGER)
ACTIVE HIGH
ENABLE THREE-STATE OUTPUTS D11....D0/8 = DB11....DB0
ACTIVE HIGH
ENABLE THREE-STATE OUTPUTS D11....D8 = DB11....DB8 D7....D4 = LOW D3/11....D0/8 = DB11....DB8

* D11....D0/8 ARE THE ADC DATA OUTPUT PINS
DB11....DB0 ARE THE 12-BIT CONVERSION RESULTS

LTC1272 • TA14

Figure 12. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$ and HBEN


$\overline{CS}$ & $\overline{RD}$
t_2
t_{CONV}
$\overline{BUSY}$
≥ 100ns*
t_{13}
CLK IN
t_{14}
DB11 (MSB)
DB10
DB1
DB0 (LSB)

UNCERTAIN CONVERSION TIME FOR 30ns < t_{14} < 180ns
*THE LTC1272 IS ALSO COMPATIBLE WITH THE AD7572 SYNCHRONIZATION MODES.
SEE "DIGITAL INTERFACE" TEXT.

LTC1272 • TA15

Figure 13. $\overline{RD}$ and CLK IN for Synchronous Operation

Table 1. Data Bus Output, $\overline{CS}$ and $\overline{RD}$ = Low

	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8	PIN 9	PIN 10	PIN 11	PIN 13	PIN 14	PIN 15	PIN 16
Data Outputs*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = Low	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = High	DB11	DB10	DB9	DB8	Low	Low	Low	Low	DB11	DB10	DB9	DB8

Note: *D11 . . . D0/8 are the ADC data output pins
DB11 . . . DB0 are the 12-bit conversion results, DB11 is the MSB

APPLICATIONS INFORMATION

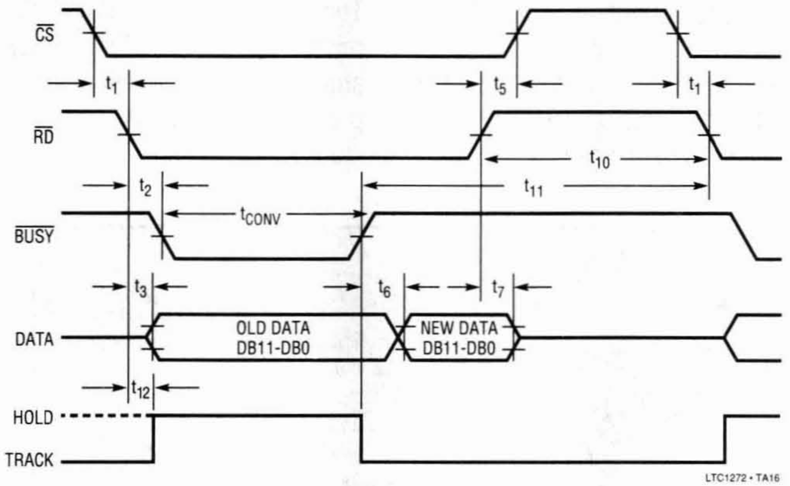


Figure 14. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3/11**	**D2/10**	**D1/9**	**D0/8**
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Data Format

The output data format can be either a complete parallel load for 16-bit microprocessors or a two byte load for 8-bit microprocessors. Data is always right justified (i.e., LSB is the most right-hand bit in a 16-bit word). For a two byte read, only data outputs D7. . . D0/8 are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12-bits of conversion data onto the lower D7. . . D0/8 outputs (4 MSBs or 8 LSBs) where it can be read in two read cycles. The 4 MSB's always appear on D11 . . . D8 whenever the three-state output drives are turned on.

Slow Memory Mode, Parallel Read (HBEN = Low)

Figure 14 and Table 2 show the timing diagram and data bus status for Slow Memory Mode, Parallel Read. $\overline{\text{CS}}$ and $\overline{\text{RD}}$ going low triggers a conversion and the LTC1272 acknowledges by taking $\overline{\text{BUSY}}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{\text{BUSY}}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on data outputs D11 . . . D0/8.

Slow Memory Mode, Two Byte Read

For a two byte read only 8 data outputs D7 . . . D0/8 are used. Conversion start procedure and data output status for the first read operation is identical to Slow Memory Mode, Parallel Read. See Figure 15 timing diagram and Table 3 data bus status. At the end of conversion the low data byte (DB7 . . . DB0) is read from the ADC. A second READ operation with HBEN high, places the high byte on data outputs D3/11 . . . D0/8 and disables conversion start. Note the 4 MSB's appear on data outputs D11 . . . D8 during the two READ operations above.

ROM Mode, Parallel READ (HBEN = Low)

The ROM Mode avoids placing a microprocessor into a WAIT state. A conversion is started with a READ operation and the 12 bits of data from the previous conversion is available on data outputs D11 . . . D0/8 (see Figure 16 and Table 4). This data may be disregarded if not required. A second READ operation reads the new data (DB11 . . . DB0) and starts another conversion. A delay at least as long as the LTC1272 conversion time plus the 1μs minimum delay between conversions must be allowed between READ operations.

APPLICATIONS INFORMATION

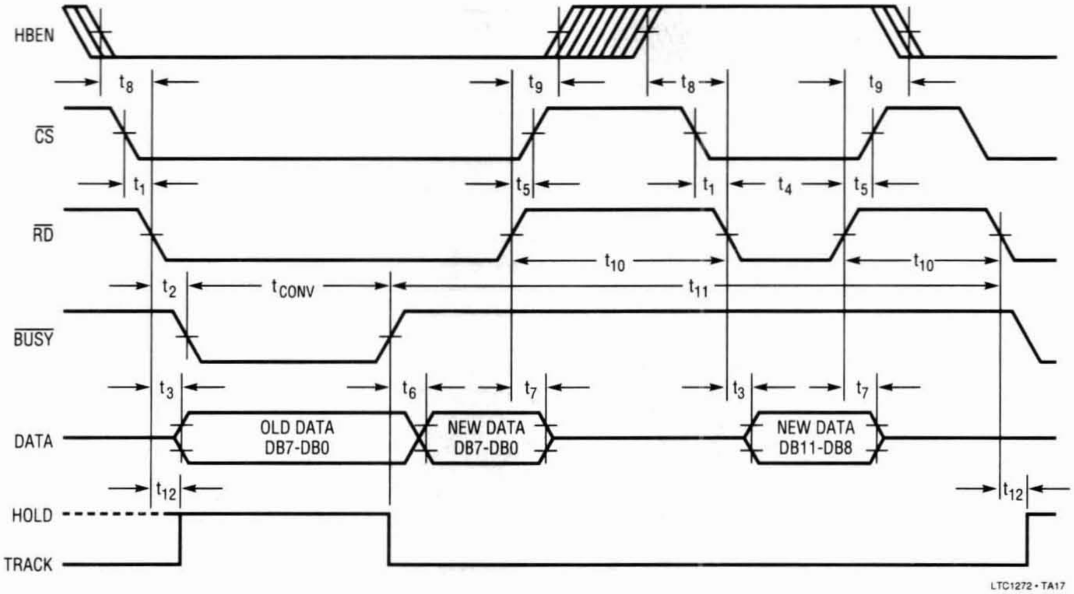

HBEN
$\overline{CS}$
$\overline{RD}$
$\overline{BUSY}$
DATA
HOLD
TRACK
t_8
t_9
t_1
t_4
t_5
t_2
t_{CONV}
t_{10}
t_{11}
t_3
t_6
t_7
t_{12}
OLD DATA DB7-DB0
NEW DATA DB7-DB0
NEW DATA DB11-DB8
LTC1272 • TA17

Figure 15. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8

6

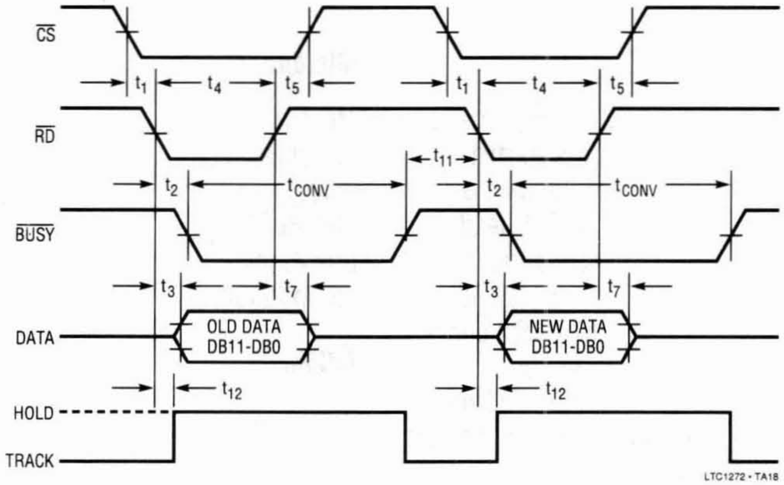

$\overline{CS}$
$\overline{RD}$
$\overline{BUSY}$
DATA
HOLD
TRACK
t_1
t_4
t_5
t_{11}
t_2
t_{CONV}
t_3
t_7
t_{12}
OLD DATA DB11-DB0
NEW DATA DB11-DB0
LTC1272 • TA18

Figure 16. ROM Mode, Parallel Read Timing Diagram

Table 4. ROM Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

APPLICATIONS INFORMATION

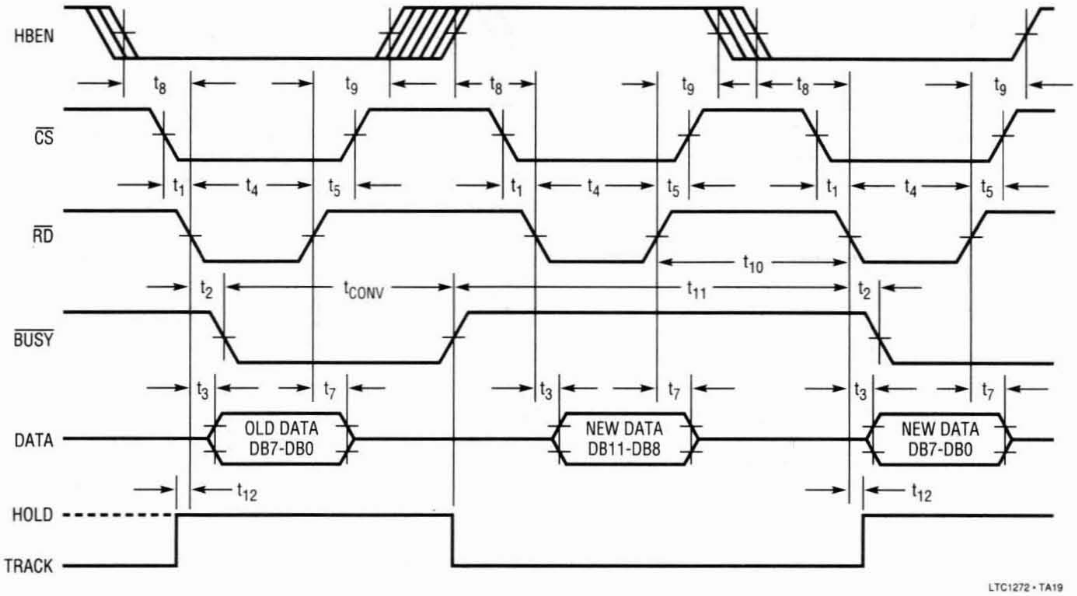


Figure 17. ROM Mode, Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	Low	Low	Low	Low	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

ROM Mode, Two Byte READ

As previously mentioned for a two byte read, only data outputs D7 . . . D0/8 are used. Conversion is started in the normal way with a READ operation and the data output status is the same as the ROM Mode, Parallel Read. See Figure 17 timing diagram and Table 5 data bus status. Two more READ operations are required to access the new conversion result. A delay equal to the LTC1272 conversion time must be allowed between conversion start and the second data READ operation. The second READ operation, with HBEN high, disables conversion start and places the high byte (4 MSBs) on data outputs D3/11 . . . D018. A third read operation accesses the low data byte (DB7 . . . DB0) and starts another conversion. The 4 MSB's appear on data outputs D11 . . . D8 during all three read operations above.

Microprocessor Interfacing

The LTC1272 is designed to interface with microprocessors as a memory mapped device. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ control inputs are common to all peripheral memory interfacing. The HBEN input serves as a data byte select for 8-bit processors and is normally connected to the microprocessor address bus.

MC68000 Microprocessor

Figure 18 shows a typical interface for the MC68000. The LTC1272 is operating in the Slow Memory Mode. Assuming the LTC1272 is located at address C000, then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result:

```
Move.W $C000,D0
```

APPLICATIONS INFORMATION

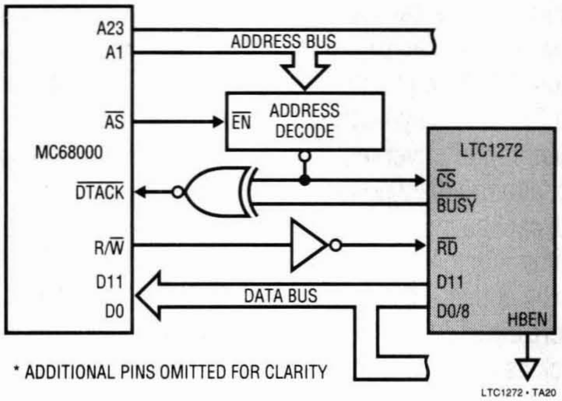

A23
A1
ADDRESS BUS
AS
EN
ADDRESS DECODE
MC68000
LTC1272
DTACK
CS
BUSY
R/W
RD
D11
D0
DATA BUS
D11
D0/8
HBEN
* ADDITIONAL PINS OMITTED FOR CLARITY
LTC1272 • TA20

Figure 18. LTC1272 MC68000 Interface

At the beginning of the instruction cycle when the ADC address is selected, $\overline{\text{BUSY}}$ and $\overline{\text{CS}}$ assert $\overline{\text{DTACK}}$, so that the MC68000 is forced into a WAIT state. At the end of conversion $\overline{\text{BUSY}}$ returns high and the conversion result is placed in the D0 register of the microprocessor.

8085A, Z80 Microprocessor

Figure 19 shows a LTC1272 interface for the Z80 and 8085A. The LTC1272 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. A0 is used to assert HBEN, so that an even address (HBEN = LOW) to the LTC1272 will start a conversion and read the low data byte. An odd address (HBEN = HIGH) will read the high data byte. This is accomplished with the single 16-bit LOAD instruction below.

For the 8085A	LHLD (B000)
For the Z80	LDHL, (B000)

This is a two byte read instruction which loads the ADC data (address B000) into the HL register pair. During the first read operation, $\overline{\text{BUSY}}$ forces the microprocessor to WAIT for the LTC1272 conversion. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

TMS32010 Microcomputer

Figure 20 shows an LTC1272 TMS32010 interface. The LTC1272 is operating in the ROM Mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The LTC1272 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into memory and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

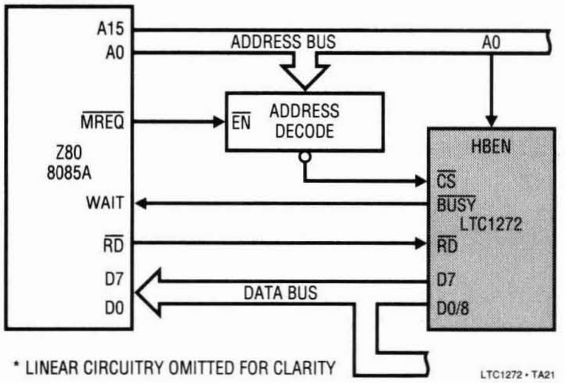

A15
A0
ADDRESS BUS
A0
MREQ
EN
ADDRESS DECODE
HBEN
Z80
8085A
CS
WAIT
BUSY
LTC1272
RD
RD
D7
D0
DATA BUS
D7
D0/8
* LINEAR CIRCUITRY OMITTED FOR CLARITY
LTC1272 • TA21

Figure 19. LTC1272 8085A/Z80 Interface

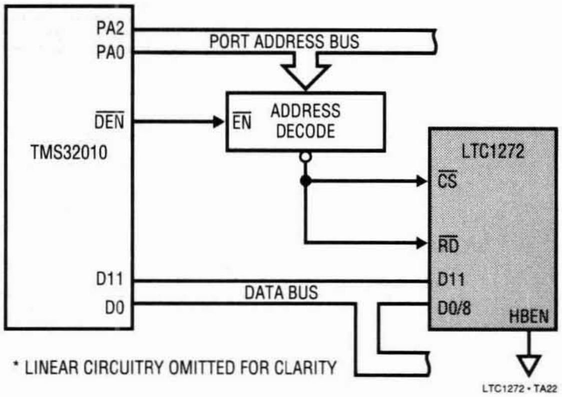

PA2
PA0
PORT ADDRESS BUS
DEN
EN
ADDRESS DECODE
TMS32010
LTC1272
CS
RD
D11
D0
DATA BUS
D11
D0/8
HBEN
* LINEAR CIRCUITRY OMITTED FOR CLARITY
LTC1272 • TA22

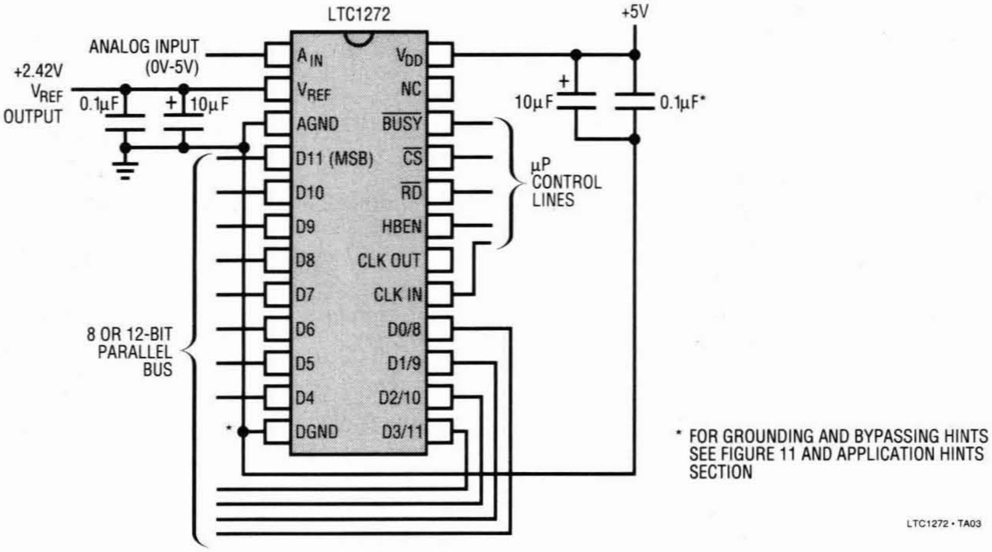
Figure 20. LTC1272 TMS32010 Interface

APPLICATIONS INFORMATION

Compatibility with the AD7572

Figure 21 shows the simple, single 5V configuration recommended for new designs with the LTC1272. If an AD7572 replacement or upgrade is desired, the LTC1272 can be plugged into an AD7572 socket with minor modifications. It can be used as a replacement or to upgrade with sample-and-hold, single supply operation and reduced power consumption.

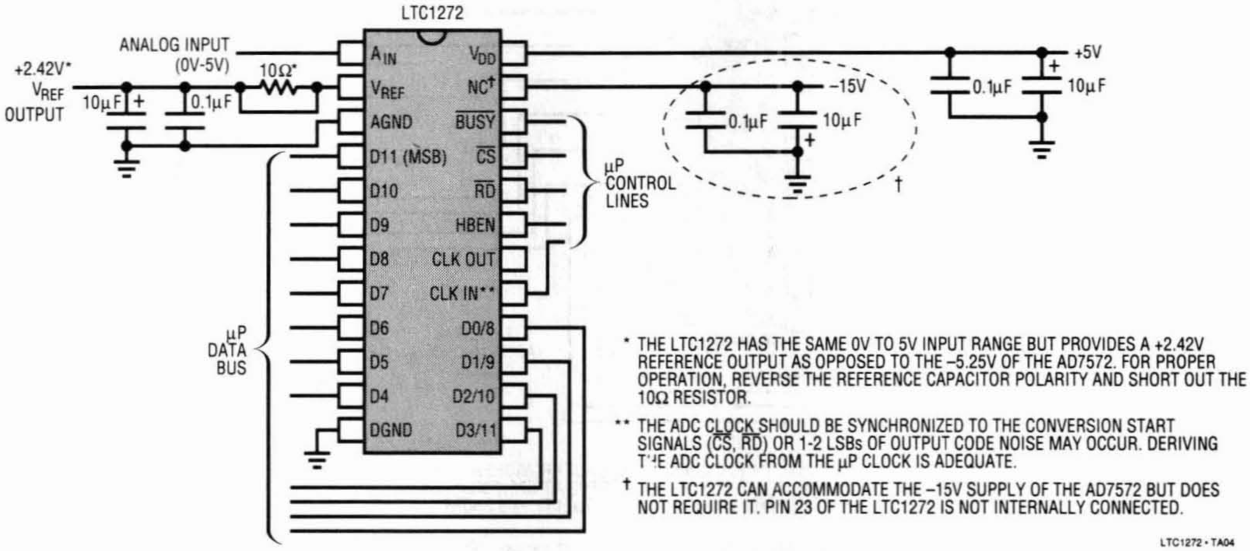
The LTC1272, while consuming less power overall than the AD7572, draws more current from the +5V supply (it draws no power from the –15V supply). Also, a 1μs minimum time between conversions must be provided to allow the sample-and-hold to reacquire the analog input. Figure 22 shows that if the clock is synchronous with $\overline{CS}$ and $\overline{RD}$, it is only necessary to short out the 10Ω series resistor and reverse the polarity of the 10μF bypass capacitor on the V_{REF} pin. The –15V supply is not required and can be removed, or, because there is no internal connection to Pin 23, it can remain unmodified. The clock can be considered synchronous with $\overline{CS}$ and $\overline{RD}$ in cases where the LTC1272 CLK IN signal is derived from the same clock as the microprocessor reading the LTC1272.


LTC1272
+5V
ANALOG INPUT
(0V-5V)
+2.42V
VREF
OUTPUT
0.1μF
10μF
10μF
0.1μF*
AIN
VREF
AGND
D11 (MSB)
D10
D9
D8
D7
D6
D5
D4
DGND
VDD
NC
BUSY
CS
RD
HBEN
CLK OUT
CLK IN
D0/8
D1/9
D2/10
D3/11
μP
CONTROL
LINES
8 OR 12-BIT
PARALLEL
BUS
*
LTC1272 • TA03

* FOR GROUNDING AND BYPASSING HINTS SEE FIGURE 11 AND APPLICATION HINTS SECTION

Figure 21. Single 5V Supply, 3μs, 12-Bit Sampling ADC

APPLICATIONS INFORMATION


LTC1272
ANALOG INPUT
(0V-5V)
+2.42V*
V_{REF}
OUTPUT
10µF
0.1µF
10Ω*
A_{IN}
V_{REF}
AGND
D11 (MSB)
D10
D9
D8
D7
D6
D5
D4
DGND
V_{DD}
NC†
$\overline{BUSY}$
$\overline{CS}$
$\overline{RD}$
HBEN
CLK OUT
CLK IN**
D0/8
D1/9
D2/10
D3/11
µP
CONTROL
LINES
µP
DATA
BUS
–15V
0.1µF
10µF
†
+5V
0.1µF
10µF

* THE LTC1272 HAS THE SAME 0V TO 5V INPUT RANGE BUT PROVIDES A +2.42V REFERENCE OUTPUT AS OPPOSED TO THE –5.25V OF THE AD7572. FOR PROPER OPERATION, REVERSE THE REFERENCE CAPACITOR POLARITY AND SHORT OUT THE 10Ω RESISTOR.

** THE ADC CLOCK SHOULD BE SYNCHRONIZED TO THE CONVERSION START SIGNALS ($\overline{CS}$, $\overline{RD}$) OR 1-2 LSBs OF OUTPUT CODE NOISE MAY OCCUR. DERIVING THE ADC CLOCK FROM THE µP CLOCK IS ADEQUATE.

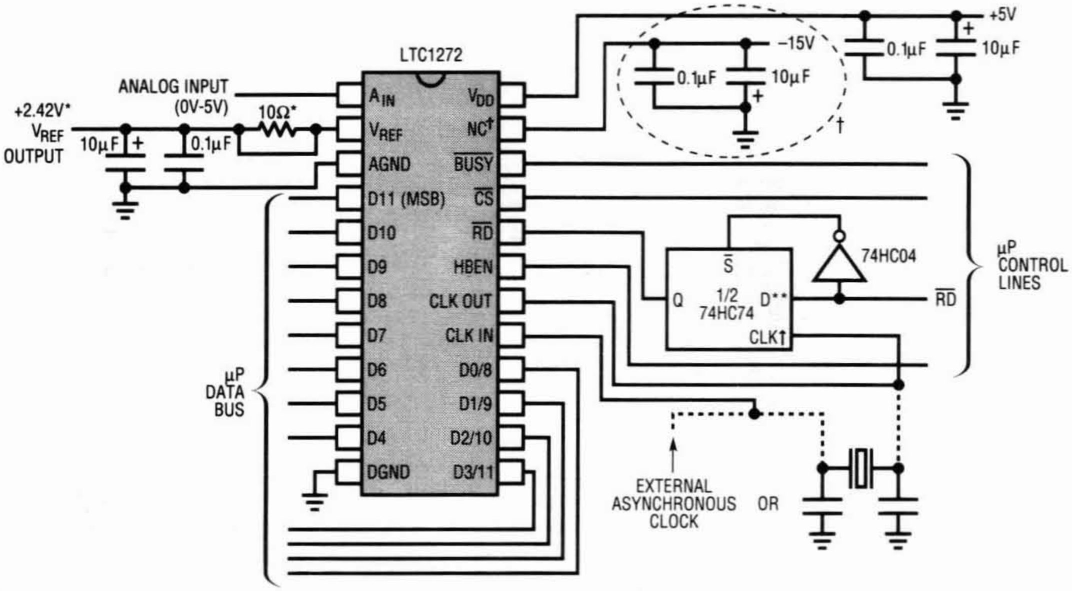
† THE LTC1272 CAN ACCOMMODATE THE –15V SUPPLY OF THE AD7572 BUT DOES NOT REQUIRE IT. PIN 23 OF THE LTC1272 IS NOT INTERNALLY CONNECTED.

LTC1272 • TA04

Figure 22. Plugging the LTC1272 into an AD7572 Socket Case 1: Clock Synchronous with $\overline{CS}$ and $\overline{RD}$

If the clock signal for the AD7572 is derived from a separate crystal or other signal which is not synchronous with the microprocessor clock, then the signals need to be synchronized for the LTC1272 to achieve best analog performance (see Clock and Control Synchronization). The best way to synchronize these signals is to drive the CLK IN pin of the LTC1272 with a derivative of the processor clock, as mentioned above and shown in Figure 22. Another way, shown in Figure 23, is to use a flip-flop to synchronize the $\overline{RD}$ to the LTC1272 with the CLK IN signal. This method will work but has two disavantages over the first: Because the $\overline{RD}$ is delayed by the flip-flop, the actual conversion start and the enabling of the LTC1272's $\overline{BUSY}$ and data outputs can take up to one CLK IN cycle to respond to a $\overline{RD}$↓ convert command from the processor. The sampling of the analog input no longer occurs at the processor's falling $\overline{RD}$ edge but may be delayed as much as one CLK IN cycle. Although the LTC1272 will still exhibit excellent DC performance, the flip-flop will introduce jitter into the sampling which may reduce the usefulness of this method for AC systems.

APPLICATIONS INFORMATION


LTC1272
+5V
–15V
0.1µF
10µF
0.1µF
10µF
†
ANALOG INPUT
(0V-5V)
+2.42V*
VREF
OUTPUT
10µF
0.1µF
10Ω*
AIN
VREF
AGND
D11 (MSB)
D10
D9
D8
D7
D6
D5
D4
DGND
VDD
NC†
BUSY
CS
RD
HBEN
CLK OUT
CLK IN
D0/8
D1/9
D2/10
D3/11
74HC04
S
Q
1/2
74HC74
D**
CLK↑
RD
µP
CONTROL
LINES
µP
DATA
BUS
EXTERNAL
ASYNCHRONOUS
CLOCK
OR

* THE LTC1272 HAS THE SAME 0V TO 5V INPUT RANGE BUT PROVIDES A +2.42V REFERENCE OUTPUT AS OPPOSED TO THE –5.25V OF THE AD7572. FOR PROPER OPERATION, REVERSE THE REFERENCE CAPACITOR POLARITY AND SHORT OUT THE 10Ω RESISTOR.

** THE D FLIP-FLOP SYNCHRONIZES THE CONVERSION START SIGNAL (RD↓) TO THE ADC CLK_{OUT} SIGNAL TO PREVENT OUTPUT CODE NOISE WHICH OCCURS WITH AN ASYNCHRONOUS CLOCK.

† THE LTC1272 CAN ACCOMMODATE THE –15V SUPPLY OF THE AD7572 BUT DOES NOT REQUIRE IT. PIN 23 OF THE LTC1272 IS NOT INTERNALLY CONNECTED.

LTC1272 • TA05

**Figure 23. Plugging the LTC1272 into an AD7572 Socket
Case 2: Clock Not Synchronous with $\overline{\text{CS}}$ and $\overline{\text{RD}}$**

LINEAR TECHNOLOGY

LTC1287

3V Single Chip 12-Bit Data Acquisition System

FEATURES

- Single Supply 3.3V or ±3.3V Operation
- Built-In Sample-and-Hold
- Direct 3-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 30kHz Maximum Throughput Rate

KEY SPECIFICATIONS

- Minimum Guaranteed Supply Voltage: 2.7V
- Resolution: 12 Bits
- Fast Conversion Time: 24µs Max Over Temp.
- Low Supply Current: 1.0mA

TYPICAL APPLICATION

- Battery-Powered Instruments
- Data Logger
- Data Acquisition Modules

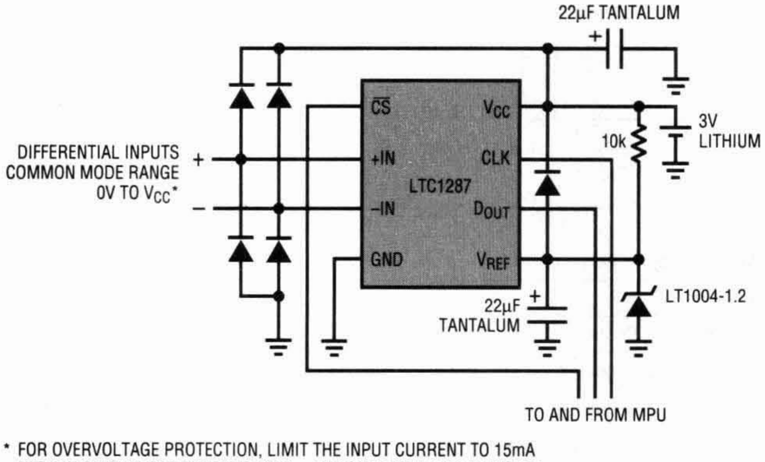
DESCRIPTION

The LTC1287 is a 3V data acquisition component which contains a serial I/O successive approximation A/D converter. The device specifications are guaranteed at a supply voltage of 2.7V. It uses LTCMOS™ switched capacitor technology to perform a 12-bit unipolar, A/D conversion. The differential input has an on-chip sample-and-hold on the (+) input.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing data to be transmitted and received over three wires. The low voltage operating capability and the low power consumption of this device make it ideally suited for battery applications. Given the ease of use, small package size and the minimum number of interconnects for I/O, the LTC1287 can be used for remote sensing applications.

LTCMOS is a trademark of Linear Technology Corporation

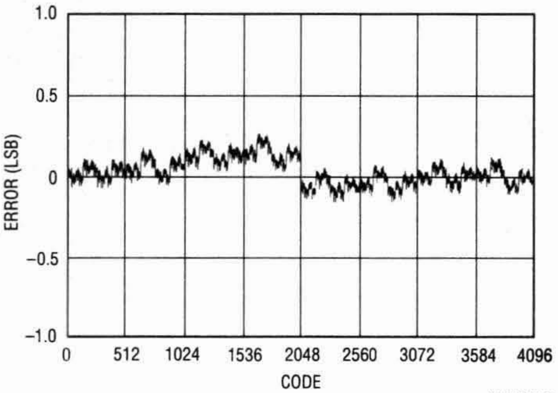
3V Differential Input Data Acquisition System



* FOR OVERVOLTAGE PROTECTION, LIMIT THE INPUT CURRENT TO 15mA PER PIN OR CLAMP THE INPUTS TO V_{CC} AND GND WITH 1N4148 DIODES. CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED CHANNEL OR OTHER CHANNEL IS OVERVOLTAGED (V_{IN} < GND OR V_{IN} > V_{CC}). SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION.

1287 TA01/DB

INL with V_{REF} = 1.2V



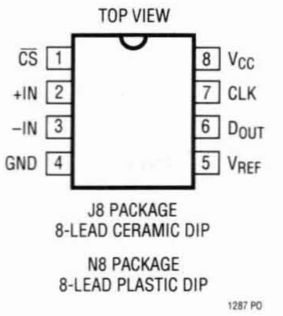
LTC1287 TA02

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog and Reference Inputs ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs .... −0.3V to 12V
  Digital Outputs .... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1287BI, LTC1287CI .... −40°C TO 85°C
  LTC1287BC, LTC1287CC........................ 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1287BIJ
LTC1287CIJ
LTC1287BIN
LTC1287CIN
LTC1287BCJ
LTC1287CCJ
LTC1287BCN
LTC1287CCN

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1287B MIN	LTC1287B TYP	LTC1287B MAX	LTC1287C MIN	LTC1287C TYP	LTC1287C MAX	UNITS
Offset Error	V_{CC} = 2.7V (Note 4)	●			±3.0			±3.0	LSB
Linearity Error (INL)	V_{CC} = 2.7V (Notes 4 & 5)	●			±0.5			±0.5	LSB
Gain Error	V_{CC} = 2.7V (Note 4)	●			±0.5			±1.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed		●			12			12	Bits
Analog and REF Input Range	(Note 7)		(V^-) − 0.05V to V_{CC} + 0.05V						V
On Channel Leakage Current (Note 8)	On Channel = 3V Off Channel = 0V	●			±1			±1	μA
	On Channel = 0V Off Channel = 3V	●			±1			±1	μA
Off Channel Leakage Current (Note 8)	On Channel = 3V Off Channel = 0V	●			±1			±1	μA
	On Channel = 0V Off Channel = 3V	●			±1			±1	μA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1287B/LTC1287C MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	(Note 6)		(Note 9)		0.5	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		14 CLK+ 5.0μs			Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		250	450	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		80	160	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		130	250	ns

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1287B/LTC1287C MIN	 TYP	 MAX	UNITS
t_{hDO}	Time Output Data Remains Valid After CLK↓				50		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		40	100	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		40	100	ns
t_{WHCLK}	CLK High Time	V_{CC} = 3V (Note 6)		600			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 3V (Note 6)		800			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ Before CLK↑	V_{CC} = 3V (Note 6)		100			ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 3V (Note 6)		5.0			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 3V (Note 6)		14			CLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs			100 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1287B/LTC1287C MIN	 TYP	 MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2.1			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.0V	●			0.45	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 3.0V, I_O = 20µA I_O = 400µA	 ●	 2.7	2.90 2.85		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0V, I_O = 20µA I_O = 400µA	 ●		0.05 0.10	 0.3	V V
I_{OZ}	High Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 −3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			9		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High	●		1.5	5	mA
I_{REF}	Reference Current	V_{REF} = 2.5V	●		10	50	µA

The ● denotes specifications which apply over the operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 3V, V_{REF} = 2.5V, CLK = 500kHz unless otherwise specified.

Note 4: One LSB is equal to V_{REF} divided by 4096. For example, when V_{REF} = 2.5V, 1LSB = 2.5V/4096 = 0.61mV.

Note 5: Integral nonlinearity error is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

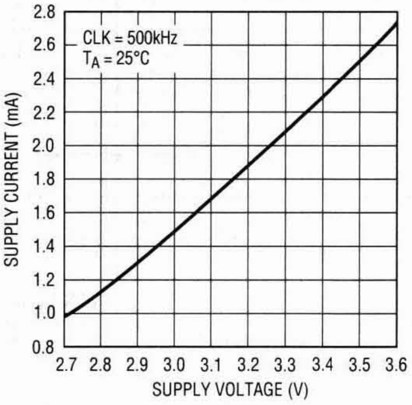
Note 7: Two on-chip diodes are tied to each analog input which will conduct for analog voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels, as high level analog inputs can cause this input diode to conduct, especially at elevated temperature, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

Note 8: Channel leakage current is measured after the channel selection.

Note 9: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that f_{CLK} ≥ 30kHz at 85°C and f_{CLK} ≥ 3kHz at 25°C.

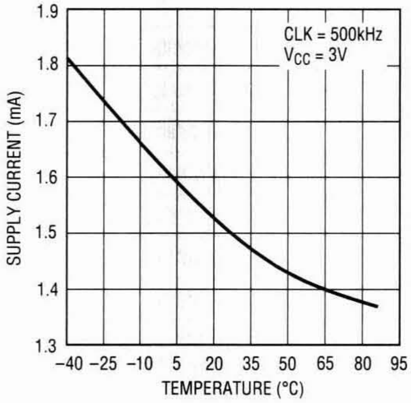
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



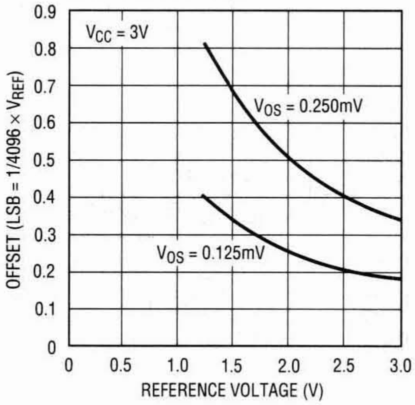
LTC1287 G1

Supply Current vs Temperature



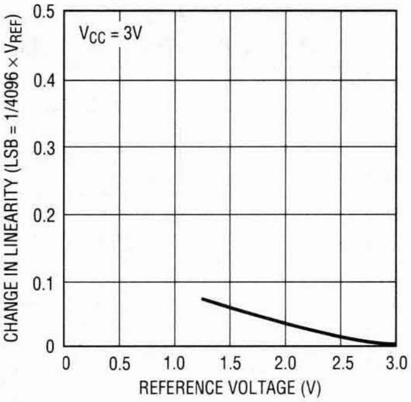
LTC1287 G2

Unadjusted Offset Voltage vs Reference Voltage



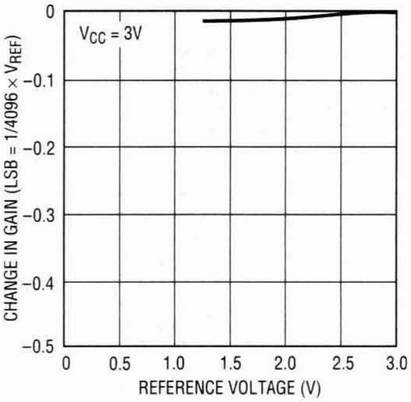
LTC1287 G3

Change in Linearity vs Reference Voltage



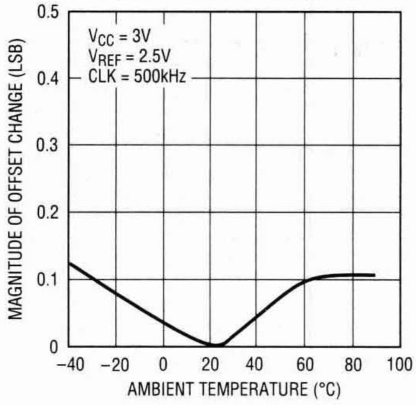
LTC1287 G4

Change in Gain vs Reference Voltage



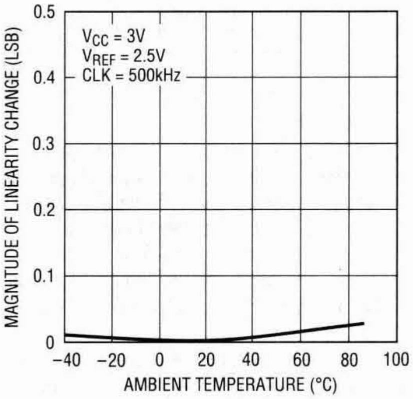
LTC1287 G5

Change in Offset vs Temperature



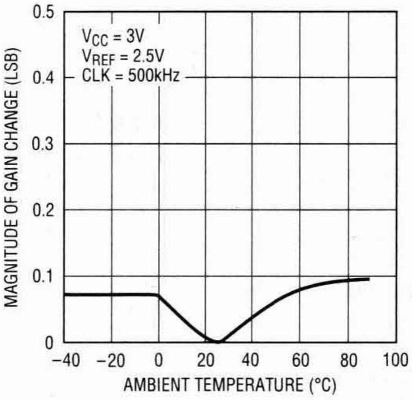
LTC1287 G6

Change in Linearity vs Temperature



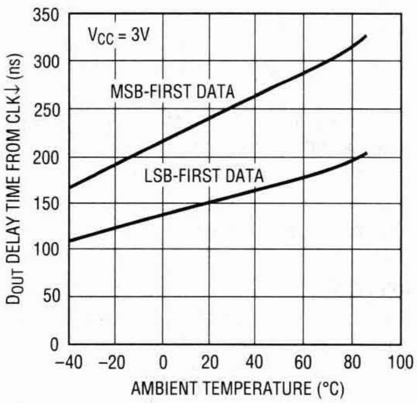
LTC1287 G7

Change in Gain vs Temperature



LTC1287 G8

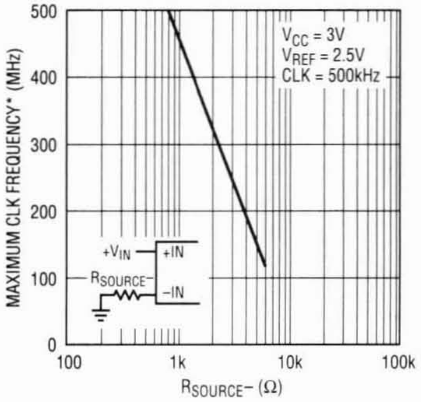
D_{OUT} Delay Time vs Temperature



LTC1287 G9

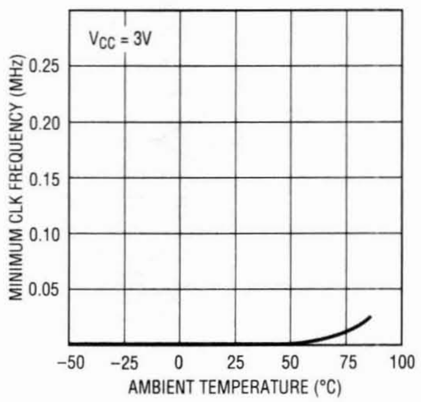
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Clock Rate vs Source Resistance



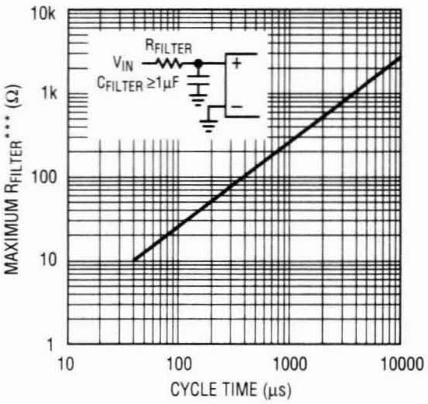
LTC G10

Minimum Clock Rate for 0.1LSB Error**



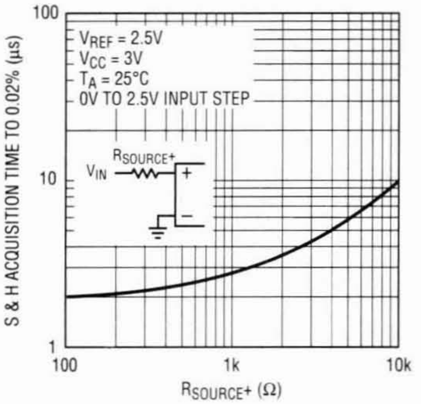
LTC1287 G11

Maximum Filter Resistor vs Cycle Time



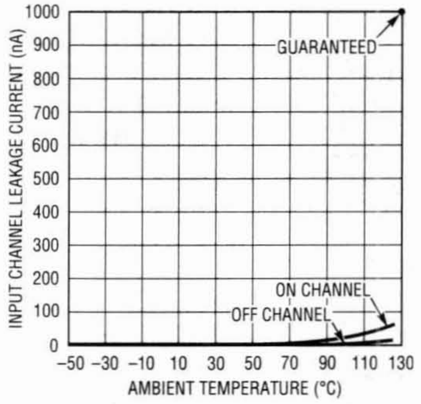
LTC1287 G12

Sample-and-Hold Acquisition Time vs Source Resistance



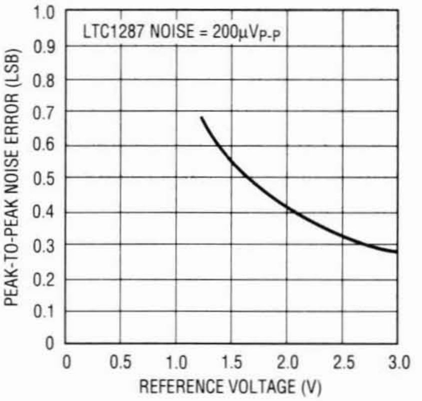
LTC1287 G13

Input Channel Leakage Current vs Temperature



LTC1287 G14

Noise Error vs Reference Voltage



LTC1287 G15

* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

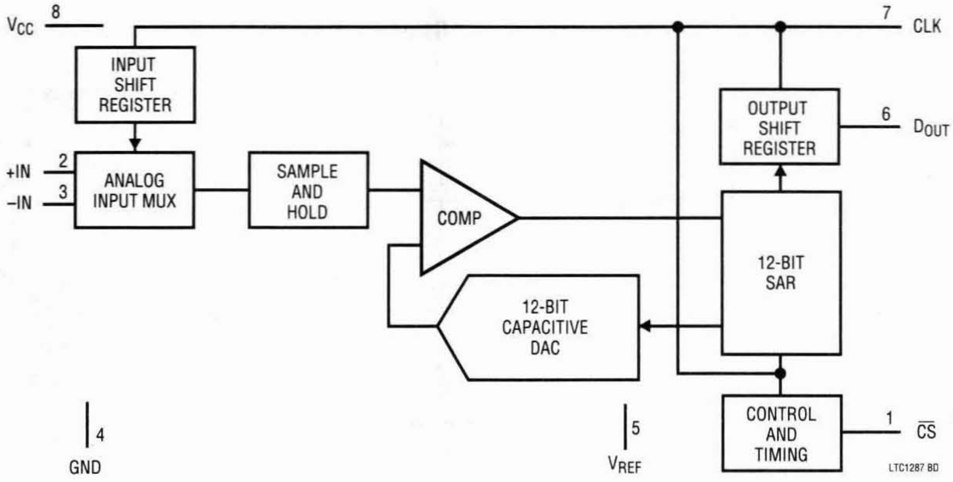
** AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 500kHz VALUE IS FIRST DETECTED.

*** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0Ω IS FIRST DETECTED.

PIN FUNCTIONS

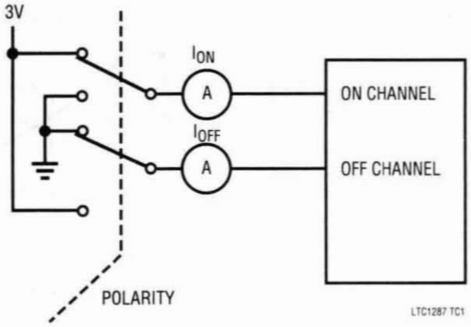
#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1287.
2, 3	+IN, –IN	Analog Inputs	These inputs must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	V_{REF}	Reference Input	The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

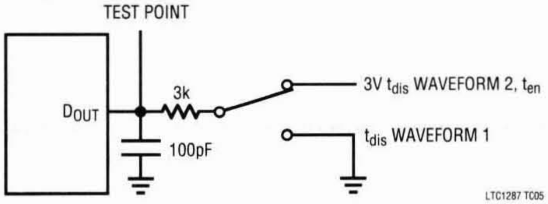

VCC
8
7
CLK
INPUT SHIFT REGISTER
OUTPUT SHIFT REGISTER
6
DOUT
+IN
–IN
2
3
ANALOG INPUT MUX
SAMPLE AND HOLD
COMP
12-BIT SAR
12-BIT CAPACITIVE DAC
4
GND
5
VREF
CONTROL AND TIMING
1
CS
LTC1287 BD

TEST CIRCUITS

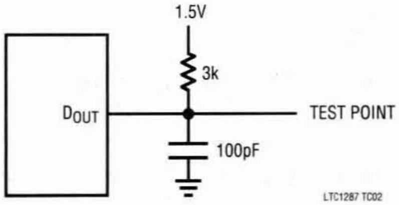
On and Off Channel Leakage Current


3V
ION
A
IOFF
A
ON CHANNEL
OFF CHANNEL
POLARITY
LTC1287 TC1

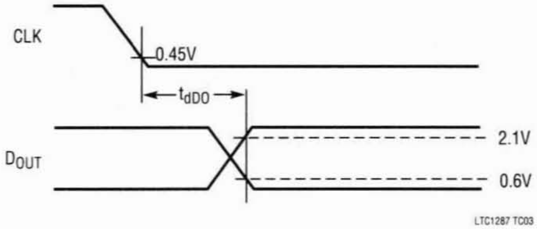
Load Circuit for t_{dis} and t_{en}


TEST POINT
DOUT
3k
100pF
3V tdis WAVEFORM 2, ten
tdis WAVEFORM 1
LTC1287 TC05

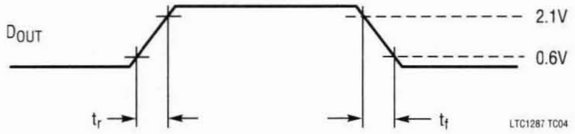
Load Circuit for t_{dDO}, t_r and t_f


1.5V
3k
DOUT
TEST POINT
100pF
LTC1287 TC02

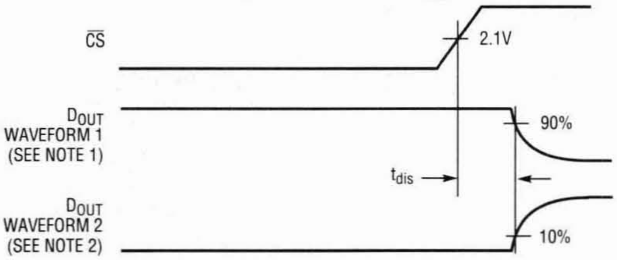
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}


CLK
0.45V
tdDO
DOUT
2.1V
0.6V
LTC1287 TC03

Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f


DOUT
2.1V
0.6V
tr
tf
LTC1287 TC04

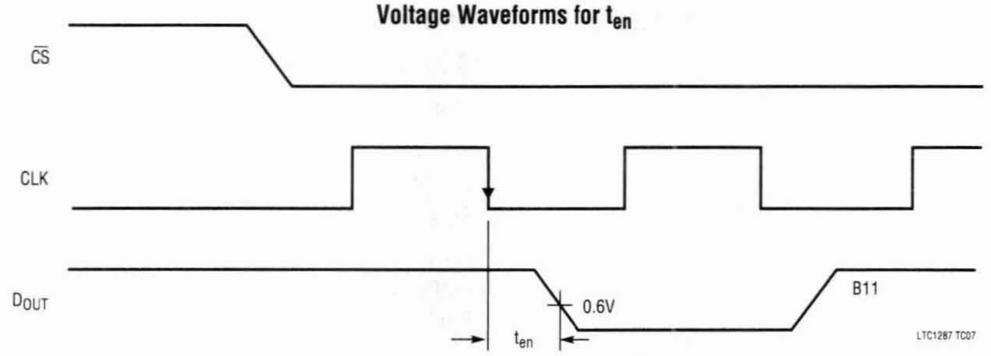
Voltage Waveforms for t_{dis}


CS
2.1V
DOUT WAVEFORM 1 (SEE NOTE 1)
90%
tdis
DOUT WAVEFORM 2 (SEE NOTE 2)
10%
LTC1287 TC06

NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS

Voltage Waveforms for t_{en}



APPLICATIONS INFORMATION

The LTC1287 is a data acquisition component which contains the following functional blocks:

1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample-and-hold (S/H)
4. Synchronous, half-duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

The LTC1287 communicates with microprocessors and other external circuitry via a synchronous, half-duplex, three-wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge. The LTC1287 does not require a configuration input word and has no D_{IN} pin. It is permanently configured to have a single differential input and to operate in unipolar mode. A falling $\overline{CS}$ initiates data transfer. The first CLK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line with a MSB-first sequence followed by a LSB-first sequence. With the half duplex serial interface the D_{OUT} data is from the current conversion. This provides easy interface to MSB- or LSB-first serial ports. Bringing $\overline{CS}$ high resets the LTC1287 for the next data exchange.

Logic Levels

The logic level standards for this supply range have not been well defined. What standards that do exist are not universally accepted. The trip point on the logic inputs of the LTC1287 is 0.28 × V_{CC}. This makes the logic inputs compatible with HC-type levels and processors that are

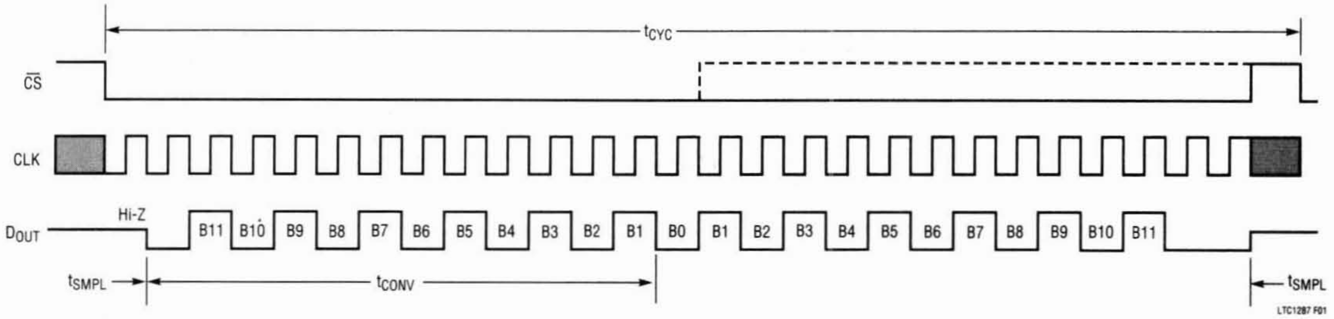


Figure 1. LTC1287 Operating Sequence

APPLICATIONS INFORMATION

specified at 3.3V. The output D_{OUT} is also compatible with the above standards. The following summarizes such levels.

V_{OH} (no load)	$V_{CC} - 0.1V$
V_{OL} (no load)	0.1V
V_{OH}	$0.9 \times V_{CC}$
V_{OL}	$0.1 \times V_{CC}$
V_{IH}	$0.7 \times V_{CC}$
V_{IL}	$0.2 \times V_{CC}$

The LTC1287 can be driven with 5V logic even when V_{CC} is at 3.3V. This is due to a unique input protection device that is found on the LTC1287.

Microprocessor Interfaces

The LTC1287 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats. If an MPU without a serial interface is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1287. Many of the popular MPUs can operate with 3V supplies. For example the MC68HC11 is an MPU with a serial format (SPI). Likewise parallel MPUs that have the 8051 type architecture are also capable of operating at this voltage range. The code for these processors remains the same and can be found in the LTC1292 data sheet.

Sharing the Serial Interface

The LTC1287 can share the same two-wire serial interface with other peripheral components or other LTC1287s (Figure 2). In this case, the $\overline{CS}$ signals decide which LTC1287 is being addressed by the MPU.

ANALOG CONSIDERATIONS

Grounding

The LTC1287 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a PC board. The ground pin (Pin 4) should be tied directly to the ground plane with minimum lead length (a low profile socket is fine). Pin 7 (V_{CC}) should be bypassed to the ground plane with a 22μF (minimum value) tantalum with leads as short as possible and as close as possible to the pin. A 0.1μF ceramic disk also should be placed in parallel with the 22μF and again with leads as short as possible and as close to V_{CC} as possible. Figure 3 shows an example of an ideal LTC1287 ground plane design for a two-sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog plane with a minimum of 22μF tantalum capacitor and with leads as short as possible. The lead from the device to the V_{CC} supply also should be kept to a minimum and the V_{CC} supply should have a low output impedance

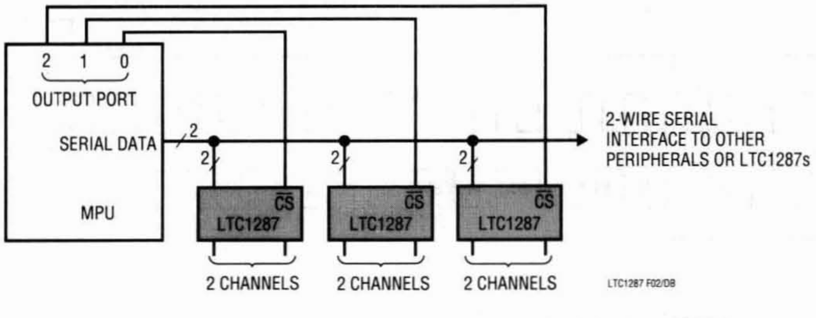


Figure 2. Several LTC1287s Sharing One 2-Wire Serial Interface

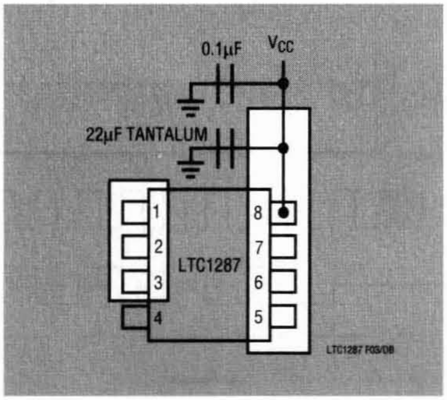


Figure 3. Example Ground Plane for the LTC1287

APPLICATIONS INFORMATION

such as obtained from a voltage regulator (e.g., LT1117). For high frequency bypassing a 0.1μF ceramic disk placed in parallel with the 22μF is recommended. Again the leads should be kept to a minimum. Using a battery to power the LTC1287 will help reduce the amount of bypass capacitance required on the V_{CC} pin. A battery placed close to the device will only require 10μF to adequately bypass the supply pin. Figure 4 shows the effect of poor V_{CC} bypassing. Figure 5 shows the settling of a LT1117 low dropout regulator with a 22μF bypass capacitor. The noise and ripple is kept around 0.5mV. Figure 6 shows the response of a lithium battery with a 10μF bypass capacitor. The noise and ripple is kept below 0.5mV.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1287 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure the transients caused by the current spikes settle completely before the conversion begins.

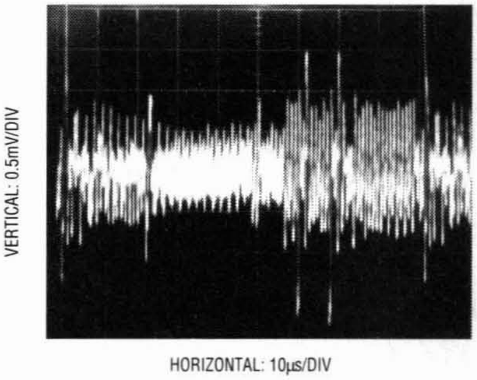


Figure 4. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

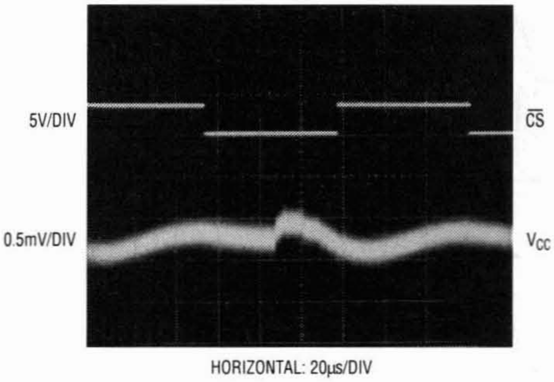


Figure 5. LT1117 Regulator with 22μF Bypassing on V_{CC}

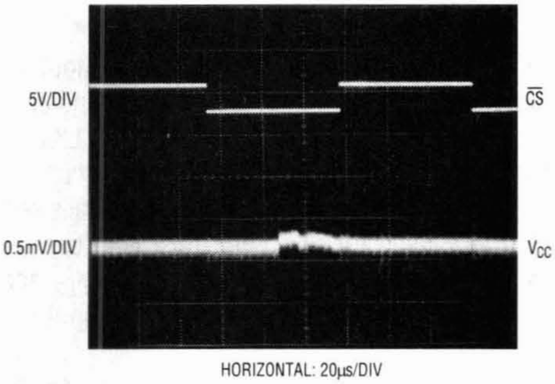


Figure 6. Lithium Battery with 10μF Bypassing on V_{CC}

Source Resistance

The analog inputs of the LTC1287 look like a 100pF capacitor (C_{IN}) in series with a 1.5k resistor (R_{ON}). This value for R_{ON} is for V_{CC} = 2.7V. With larger supply voltages R_{ON} will be reduced. For example, with V_{CC} = 2.7V and V^- = −2.7V, R_{ON} becomes 500Ω. C_{IN} gets switched between (+) and (−) inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

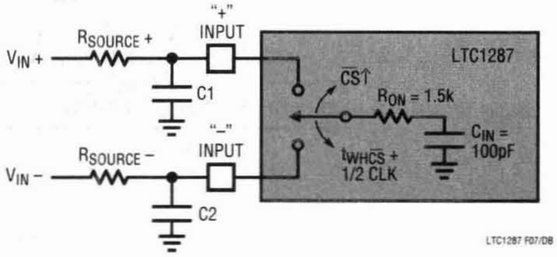


Figure 7. Analog Input Equivalent Circuit

APPLICATIONS INFORMATION

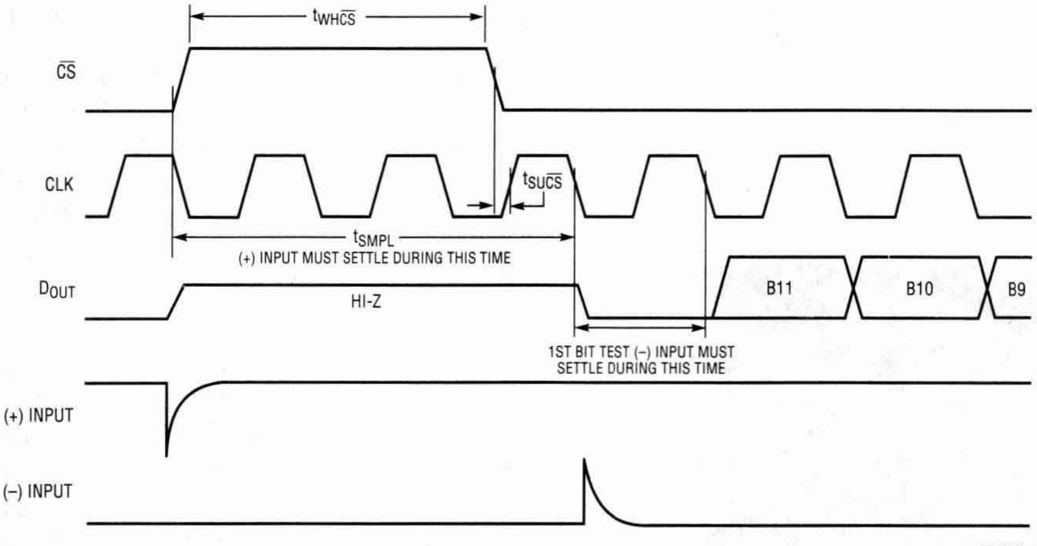
“+” Input Settling

The input capacitor is switched onto the “+” input during the sample phase (t_{SMPL}, see Figures 8a, 8b and 8c). The sample period can be as short as $t_{WH\overline{CS}}$ + 0.5 CLK cycle or as long as $t_{WH\overline{CS}}$ + 1.5 CLK cycles before a conversion starts. This variability depends on where $\overline{CS}$ falls relative to CLK. The voltage on the “+” input must settle completely within the sample period. Minimizing $R_{SOURCE}+$ and C1 will improve the settling time. If large “+” input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 6.0μs, **$R_{SOURCE}+$ < 4.0k and C1 < 20pF will provide adequate settle time.**

“–” Input Settling

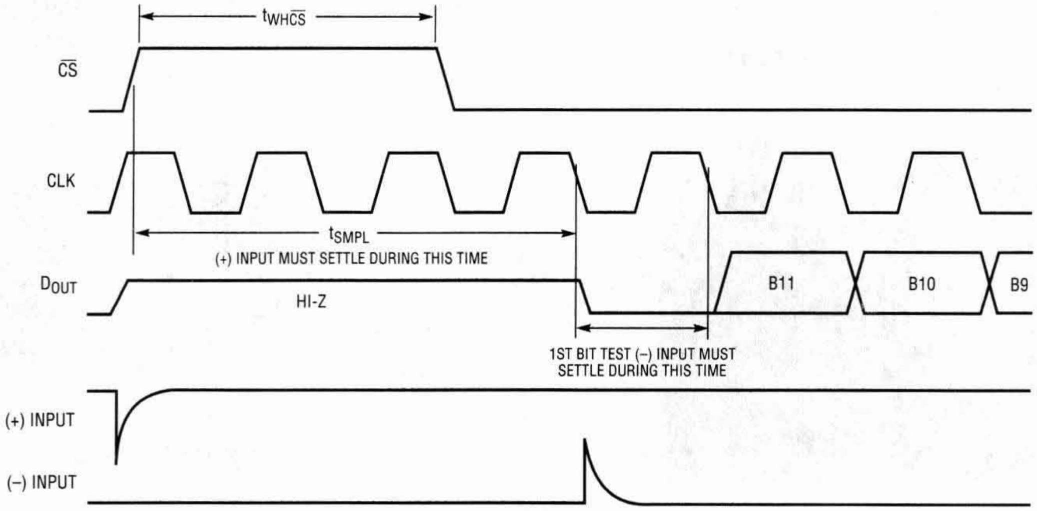
At the end of the sample phase the input capacitor switches to the “–” input and the conversion starts (see Figures 8a, 8b and 8c). During the conversion, the “+” input voltage is

“+” and “–” Input Settling Windows



$t_{WH\overline{CS}}$
$\overline{CS}$
CLK
$t_{SU\overline{CS}}$
t_{SMPL}
(+) INPUT MUST SETTLE DURING THIS TIME
D_{OUT}
HI-Z
B11
B10
B9
1ST BIT TEST (–) INPUT MUST SETTLE DURING THIS TIME
(+) INPUT
(–) INPUT
LTC1287 F8a

Figure 8a. Setup Time ($t_{SU\overline{CS}}$) is Met



$t_{WH\overline{CS}}$
$\overline{CS}$
CLK
t_{SMPL}
(+) INPUT MUST SETTLE DURING THIS TIME
D_{OUT}
HI-Z
B11
B10
B9
1ST BIT TEST (–) INPUT MUST SETTLE DURING THIS TIME
(+) INPUT
(–) INPUT
LTC1287 F8b

Figure 8b. Setup Time ($t_{SU\overline{CS}}$) is Met

APPLICATIONS INFORMATION

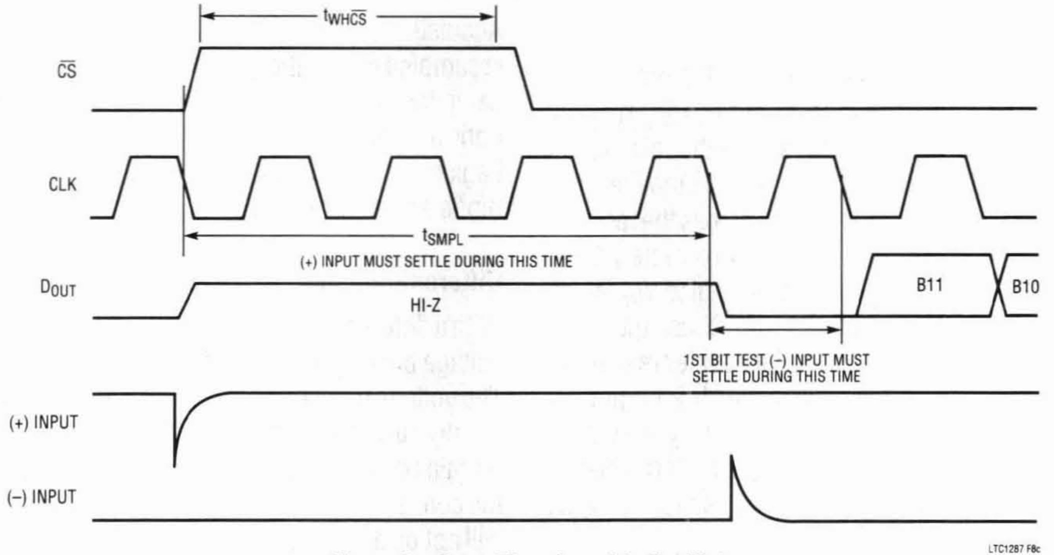

$t_{WH\overline{CS}}$
$\overline{CS}$
CLK
t_{SMPL}
(+) INPUT MUST SETTLE DURING THIS TIME
D_{OUT}
HI-Z
B11
B10
1ST BIT TEST (–) INPUT MUST SETTLE DURING THIS TIME
(+) INPUT
(–) INPUT
LTC1287 F8c

Figure 8c. Setup Time ($t_{SU\overline{CS}}$) is Not Met

effectively "held" by the sample and hold and will not affect the conversion result. It is critical that the "–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing R_{SOURCE}– and C2 will improve settling time. If large "–" input source resistance must be used the time can be extended by using a slower CLK frequency. At the maximum CLK frequency of 500kHz, **R_{SOURCE}– < 200Ω and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settles within the allowed time (see Figures 8a, 8b and 8c). Again the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. For single supply low voltage application the LT1006, LT1013 and LT1014 can be made to settle well even with the minimum settling windows of 6μs ("+" input) and 2μs ("–" input) which occur at the maximum clock rates (CLK = 500kHz). Figures 9 and 10 show examples of adequate and poor op amp settling. The LT1077, LT1078 or LT1079 can be used here to reduce power consumption. Placing an RC network at the output of the op amps will inprove the settling response and also reduce the broadband noise.

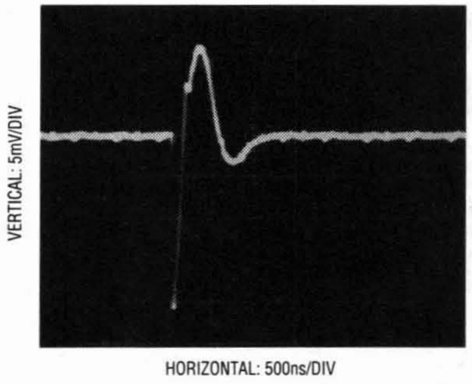


Figure 9. Adequate Settling of Op Amp Driving Analog Input

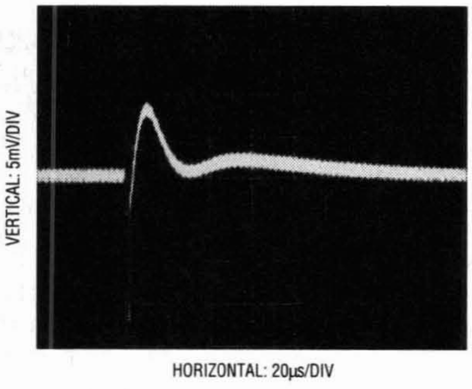


Figure 10. Poor Op Amp Settling Can Cause A/D Errors

APPLICATIONS INFORMATION

RC Input filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., 1µF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately I_{DC} = 100pF × V_{IN}/t_{CYC} and is roughly proportional to V_{IN}. When running at the minimum cycle time of 33µs, the input current equals 7.6µA at V_{IN} = 2.5V. Here a filter resistor of 8Ω will cause 0.1LSB of full-scale error. If a large filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the Typical Performance Characteristics curve Maximum Filter Resistor vs Cycle Time.

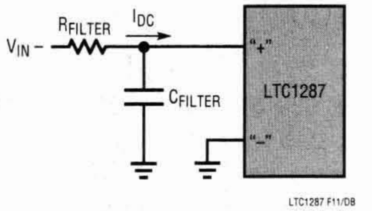


Figure 11. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1µA (at 85°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 1.6LSB with V_{REF} = 2.5V. This error will be much reduced at lower temperatures because leakage drops rapidly (see Typical Performance Characteristics curve Input Channel Leakage Current vs Temperature).

SAMPLE-AND-HOLD

Single-Ended Input

The LTC1287 provides a built-in sample and hold (S&H) function on the +IN input for signals acquired in the single ended mode (–IN pin grounded). The sample and hold allows the LTC1287 to convert rapidly varying signals (see Typical Performance Characteristics curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval begins at rising edge of $\overline{CS}$ and continues until the falling edge of the CLK before the conversion begins. On this falling edge the S&H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the +IN pin is sampled and held and can be rapidly time varying. The voltage on the –IN pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR(MAX)} = \left(2\pi f_{(-IN)} V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right)$$

Where $f_{(-IN)}$ is the frequency of the –IN input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. Usually V_{ERROR} will not be significant. For a 60Hz signal on the –IN input to generate a 0.25LSB error (150µV) with the converter running at CLK = 500kHz, its peak value would have to be 16mV. Rearranging the above equation, the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-IN)MAX} = \left(\frac{V_{ERROR(MAX)}}{2\pi V_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right)$$

For 0.25LSB error (150µV) the maximum input sinusoid with a 2.5V peak amplitude that can be digitized is 0.4Hz.

Reference Input

The voltage on the reference input of the LTC1287 determines the voltage span of the A/D converter. The reference input has transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the

APPLICATIONS INFORMATION

conversion (every CLK cycle) a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. If slow settling circuitry is used to drive the reference input, take care to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

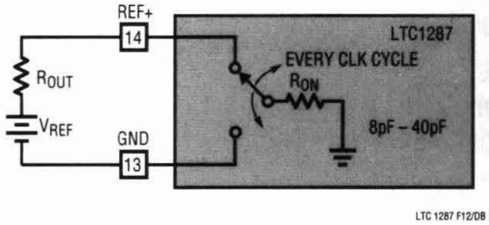


Figure 12. Reference Input Equivalent Circuit

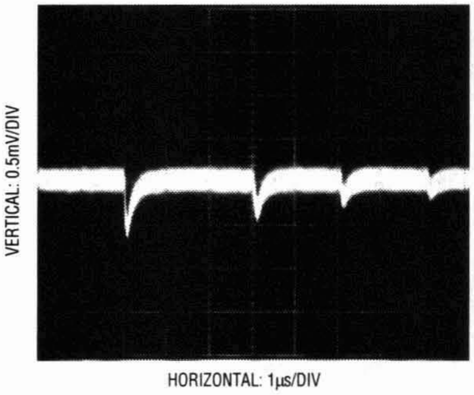


Figure 13. Adequate Reference Settling

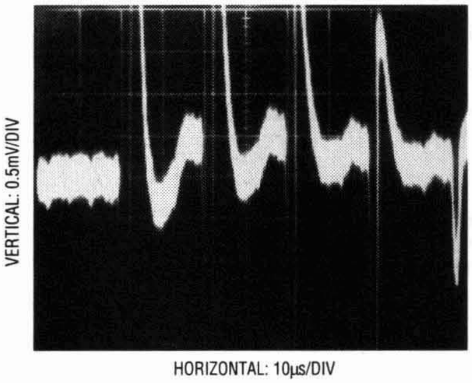


Figure 14. Poor Reference Settling Can Cause A/D Errors

Figures 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 500kHz most references and op amps can be made to settle within the 2μs bit time. For example an LT1019 used in the shunt mode with a 10μF bypass capacitor will settle adequately. To minimize power an LT1004-2.5 can be used with a 10μF bypass capacitor. For lower value references the LT1004-1.2 with a 10μF bypass capacitor can be used.

Reduced Reference Operation

The effective resolution of the LTC1287 can be increased by reducing the input span of the converter. The LTC1287 exhibits good linearity over a range of reference voltages (seeTypical Performance Characteristics curves of Change in Linearity vs Reference Voltage). Care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. Offset and Noise are factors that must be considered when operating at low V_{REF} values.

Offset with Reduced V_{REF}

The offset of the LTC1287 has a larger effect on the output code when the A/D is operated with a reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The Typical Performance Characteristics curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example a V_{OS} of 0.1mV, which is 0.2LSB with a 2.5V reference becomes 0.4LSB with a 1.25 reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the –IN input to the LTC1287.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1287 can be reduced to approximately 200μV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This

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noise is insignificant with a 2.5V reference input but will become a larger fraction of an LSB as the size of the LSB is reduced. The Typical Performance Characteristics curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

For operation with a 2.5V reference, the 200µV noise is only 0.32LSB peak-to-peak. Here the LTC1287 noise will contribute virtually no uncertainty to the output code. For reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this 200µV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. Now averaging readings may be necessary.

This noise data was taken in a very clean test fixture. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage used, the more critical it becomes to have a noise-free setup.

Overvoltage Protection

Applying signals to the LTC1287's analog inputs that exceed the positive supply or that go below ground will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog inputs before power is applied to the LTC1287. Another example is the input source operating from different supplies of larger value than the LTC1287. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. There are two ways to protect the inputs. In Figure 15 diode clamps from the inputs to V_{CC} and GND are used. The second method is to put resistors in series with the analog inputs for current limiting. Limit the current to 15mA per channel. The +IN input can accept a resistor value of 1k but the –IN input cannot accept more than 200Ω when clocked at its maximum clock frequency of 500kHz. If the LTC1287 is clocked at the maximum clock frequency and 200Ω is not enough to current limit the input source then the clamp diodes are recommended (Figures 16 and 17). The reason for the limit on the resistor value is the MSB bit test is affected by the value of the resistor placed at the –IN input (see discussion on Analog Inputs and the Typical Performance Characteristics curve of Maximum CLK Frequency vs Source Resistance).

If V_{CC} and V_{REF} are not tied together, then V_{CC} should be turned on first, then V_{REF}. If this sequence cannot be met, connecting a diode from V_{REF} to V_{CC} is recommended (see Figure 18).

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

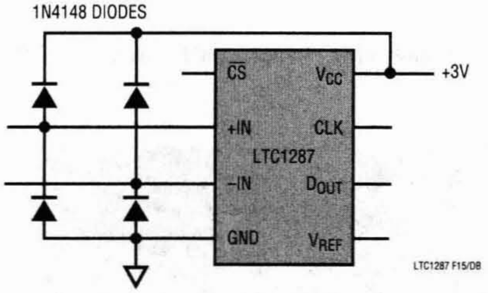

Figure 15. Overvoltage Protection for Inputs

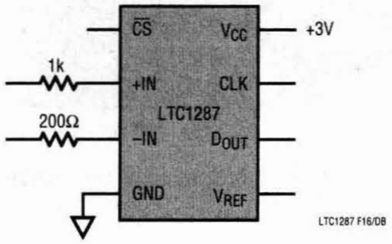

Figure 16. Overvoltage Protection for Inputs

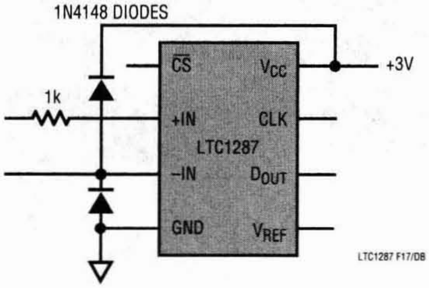

Figure 17. Overvoltage Protection for Inputs

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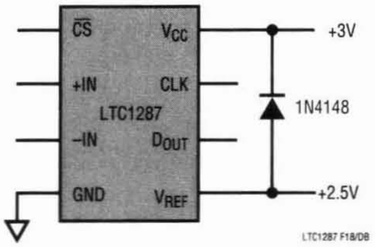
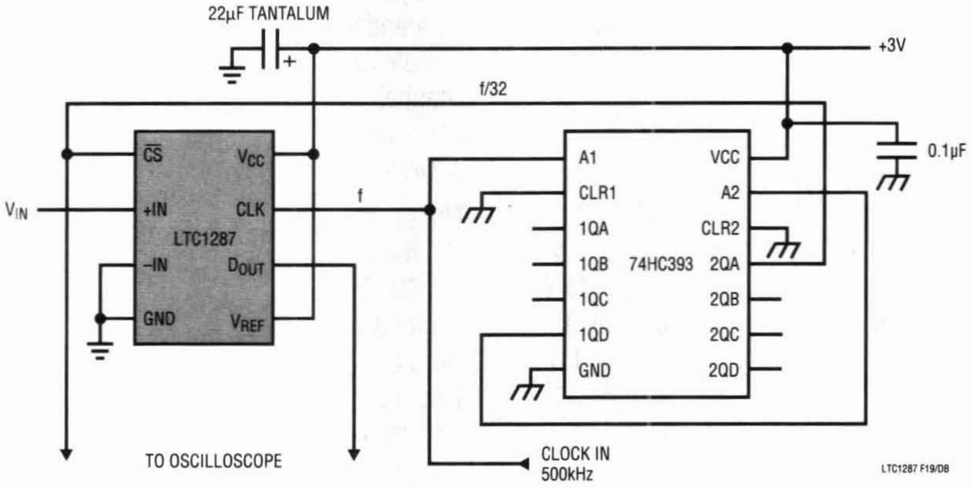


$\overline{CS}$
V_{CC}
+3V
+IN
CLK
LTC1287
1N4148
–IN
D_{OUT}
GND
V_{REF}
+2.5V
LTC1287 F18/D8

Figure 18

A "Quick Look" Circuit for the LTC1287

Users can get a quick look at the function and timing of the LTC1287 by using the following simple circuit (Figure 19). V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground plane. $\overline{CS}$ is driven at 1/32 the clock rate by the 74HC393 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 20). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.



22µF TANTALUM
+3V
f/32
0.1µF
$\overline{CS}$
V_{CC}
V_{IN}
+IN
CLK
f
LTC1287
–IN
D_{OUT}
GND
V_{REF}
A1
VCC
CLR1
A2
1QA
CLR2
1QB
74HC393
2QA
1QC
2QB
1QD
2QC
GND
2QD
TO OSCILLOSCOPE
CLOCK IN
500kHz
LTC1287 F19/D8

Figure 19. "Quick Look" Circuit for the LTC1287

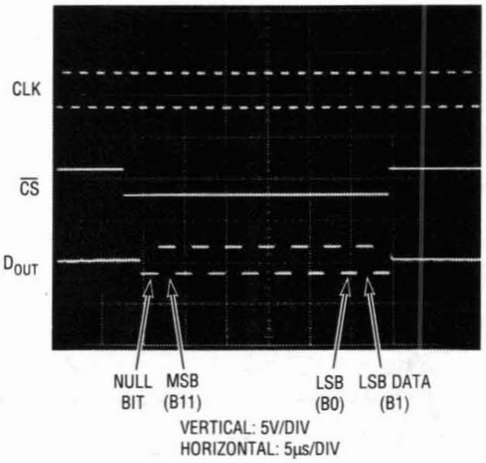


Figure 20. Scope Trace of the LTC1287 "Quick Look" Circuit Showing A/D Output 1010101010 (AAA_{HEX})

3 Volt Single Chip 12-Bit Data Acquisition System

FEATURES

- Single Supply 3.3V or ±3.3V Operation
- Software Programmable Features
  - Unipolar/Bipolar Conversions
  - 4 Differential/8 Single-Ended Inputs
  - Variable Data Word Length
  - Power Shutdown
- Built-In Sample and Hold
- Direct 4-Wire Interface to Most MPU Serial Ports and all MPU Parallel Ports
- 25kHz Maximum Throughput Rate

KEY SPECIFICATIONS

- Minimum Guaranteed Supply Voltage 2.7V
- Resolution .... 12 Bits
- Fast Conversion Time .... 26µs Max Over Temp
- Low Supply Currents....................................... 1.0mA

DESCRIPTION

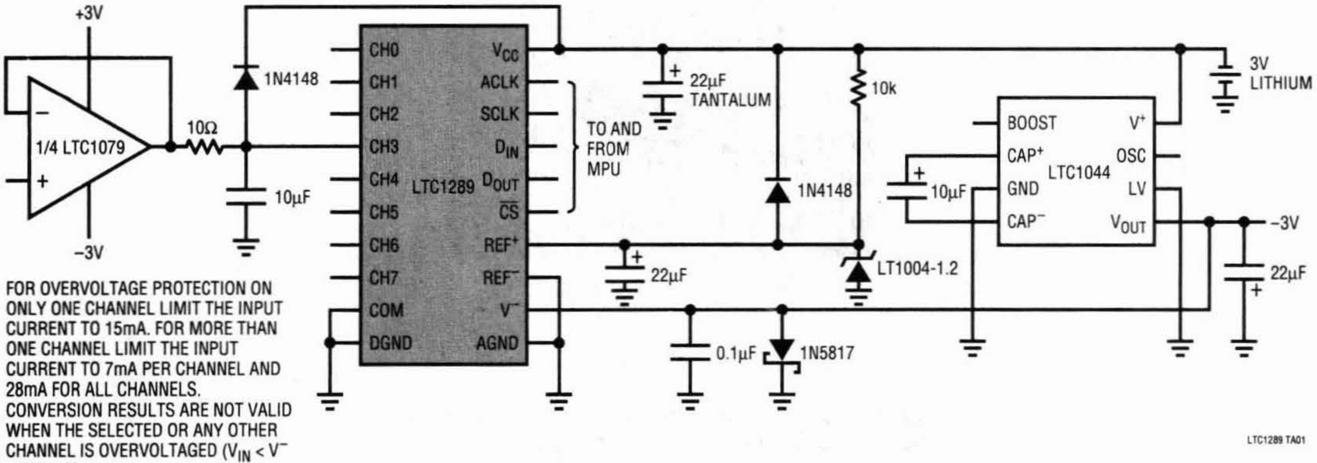
The LTC1289 is a 3V data acquisition component which contains a serial I/O successive approximation A/D converter. The device specifications are guaranteed at a supply voltage of 2.7V. It uses LTCMOS™ switched capacitor technology to perform a 12-bit unipolar, or 11-bit plus sign bipolar A/D conversion. The 8 channel input multiplexer can be configured for either single-ended or differential inputs (or combinations thereof). An on-chip sample and hold is included for all single-ended input channels. When the LTC1289 is idle it can be powered down in applications where low power consumption is desired.

The serial I/O is designed to be compatible with industry standard full duplex serial interfaces. It allows either MSB- or LSB- first data and automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8, 12 or 16 bits. This allows easy interface to shift registers and a variety of processors.

LTCMOS™ is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

Single Cell 3V 12-Bit Data Acquisition System

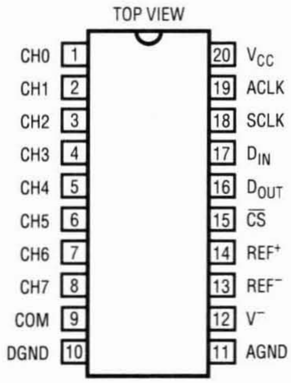
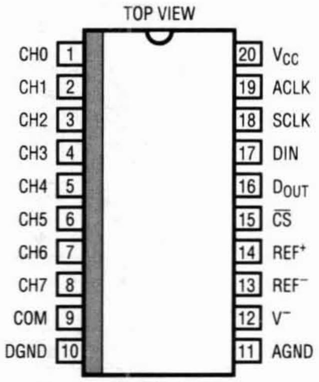

+3V
-3V
1/4 LTC1079
10Ω
1N4148
10µF
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
LTC1289
V_{CC}
ACLK
SCLK
D_{IN}
D_{OUT}
$\overline{CS}$
REF^+
REF^-
V^-
AGND
TO AND FROM MPU
22µF TANTALUM
22µF
0.1µF
1N4148
10k
LT1004-1.2
1N5817
BOOST
CAP^+
GND
CAP^-
LTC1044
V^+
OSC
LV
V_{OUT}
10µF
3V LITHIUM
-3V
22µF
LTC1289 TA01

FOR OVERVOLTAGE PROTECTION ON ONLY ONE CHANNEL LIMIT THE INPUT CURRENT TO 15mA. FOR MORE THAN ONE CHANNEL LIMIT THE INPUT CURRENT TO 7mA PER CHANNEL AND 28mA FOR ALL CHANNELS. CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED OR ANY OTHER CHANNEL IS OVERVOLTAGED ($V_{IN} < V^-$ or $V_{IN} > V_{CC}$).

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage V_{CC} to GND or V^-	12V
Negative Supply Voltage (V^-)	−6V to GND
Voltage	
Analog and Reference Inputs	(V^-) −0.3V to V_{CC} + 0.3V
Digital Inputs	−0.3V to 12V
Digital Outputs	−0.3V to V_{CC} + 0.3V
Power Dissipation	500mW
Operating Temperature Range	
LTC1289BI, LTC1289CI	−40°C TO 85°C
LTC1289BC, LTC1289CC	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
 TOP VIEW CH0 1 CH1 2 CH2 3 CH3 4 CH4 5 CH5 6 CH6 7 CH7 8 COM 9 DGND 10 20 V_{CC} 19 ACLK 18 SCLK 17 D_{IN} 16 D_{OUT} 15 $\overline{CS}$ 14 REF^+ 13 REF^- 12 V^- 11 AGND J PACKAGE 20-LEAD CERAMIC DIP N PACKAGE 20-LEAD PLASTIC DIP 1289 P001	LTC1289BIJ LTC1289CIJ LTC1289BIN LTC1289CIN LTC1289BCJ LTC1289CCJ LTC1289BCN LTC1289CCN	 TOP VIEW CH0 1 CH1 2 CH2 3 CH3 4 CH4 5 CH5 6 CH6 7 CH7 8 COM 9 DGND 10 20 V_{CC} 19 ACLK 18 SCLK 17 DIN 16 D_{OUT} 15 $\overline{CS}$ 14 REF^+ 13 REF^- 12 V^- 11 AGND S PACKAGE 20-LEAD PLASTIC SOL LTC1289 P002	LTC1289BCS LTC1289CCS

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

			LTC1289B			LTC1289C			
PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Offset Error	V_{CC} = 2.7V (Note 4)	●			±1.5			±1.5	LSB
Linearity Error (INL)	V_{CC} = 2.7V (Notes 4 and 5)	●			±0.5			±0.5	LSB
Gain Error	V_{CC} = 2.7V (Note 4)	●			±0.5			±1.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed		●			12			12	BITS
Analog and REF Input Range	(Note 7)		(V^-) − 0.05V to V_{CC} + 0.05V			(V^-) − 0.05V to V_{CC} + 0.05V			V
On Channel Leakage Current (Note 8)	On Channel = 3V Off Channel = 0V	●			±1			±1	μA
	On Channel = 0V Off Channel = 3V	●			±1			±1	μA
Off Channel Leakage Current (Note 8)	On Channel = 3V Off Channel = 0V	●			±1			±1	μA
	On Channel = 0V Off Channel = 3V	●			±1			±1	μA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1289B LTC1289C MIN	 TYP	 MAX	UNITS
f_{SCLK}	Shift Clock Frequency	(Note 6)		0		1.0	MHz
f_{ACLK}	A/D Clock Frequency	(Note 6)		(Note 10)		2.0	MHz
t_{ACC}	Delay time from $\overline{CS}$↓ to D_{OUT} Data Valid	(Note 9)			2		ACLK Cycles
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			7		SCLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			52		ACLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		12 SCLK + 56 ACLK			Cycles
t_{dDO}	Delay Time, SCLK↓ to D_{OUT} Data Valid	See Test Circuits	●		200	350	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		70	150	ns
t_{en}	Delay Time, 2nd ACLK↓ to D_{OUT} Enabled	See Test Circuits	●		130	250	ns
$t_{h\overline{CS}}$	Hold Time, $\overline{CS}$ After Last SCLK↓	(Note 6)		0			ns
t_{hDI}	Hold Time, D_{IN} After SCLK↑	(Note 6)		50			ns
t_{hDO}	Time Output Data Remains Valid After SCLK↓				50		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		40	100	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		40	100	ns
t_{suDI}	Setup Time, D_{IN} Stable Before SCLK↑	(Note 6 and 9)		50			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ Before Clocking in First Address Bit	(Note 6 and 9)		2 ACLK Cycles + 180ns			
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	(Note 6)		52			ACLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs			100 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1289B LTC1289C MIN	 TYP	 MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2.1			V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.0V	●			0.45	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 3.0V I_O = 20µA I_O = 400µA	 ● 	 2.7	 2.90 2.85		V
V_{OL}	Low Level Output Voltage	V_{CC} = 3.0V I_O = 20µA I_O = 400µA	 ● 		 0.05 0.10	 0.3	V
I_{OZ}	High Z Output Leakage	V_{OUT} = V_{CC}, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 −3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			9		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High $\overline{CS}$ High, Power Shutdown, ACLK Off	● ●		1.5 1.0	5 10	mA µA
I_{REF}	Reference Current	V_{REF} = 2.5V	●		10	50	µA
I^-	Negative Supply Current	$\overline{CS}$ High	●		1	50	µA

The ● denotes specifications which apply over the operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impared.

Note 2: All voltage values are with respect to ground with DGND, AGND and REF^- wired together (unless otherwise noted).

Note 3: V_{CC} = 3V, $V_{REF}+$ = 2.5V, $V_{REF}-$ = 0V, V^- = 0V for unipolar mode and −3V for bipolar mode, ACLK = 2.0MHz unless otherwise specified.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 4096. For example, when V_{REF} = 2.5V, 1LSB(bipolar) = 2(2.5)/4096 = 1.22mV. V^- = −2.7V for bipolar mode.

Note 5: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

Note 7: Two on-chip diodes are tied to each analog input which will conduct for analog voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels, as high level analog inputs can cause this input diode to conduct, especially at elevated temperature, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

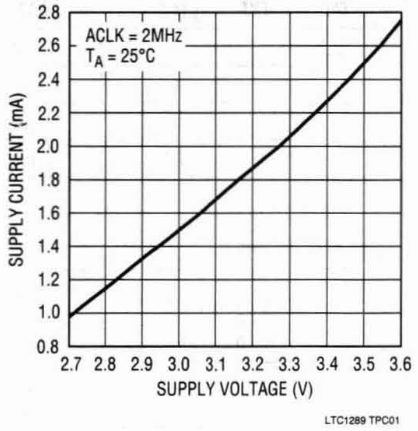
Note 8: Channel leakage current is measured after the channel selection.

Note 9: To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edges after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select set-up time has elasped. See Typical Peformance Characteristics curves for additional information ($t_{su\overline{CS}}$ vs V_{CC}).

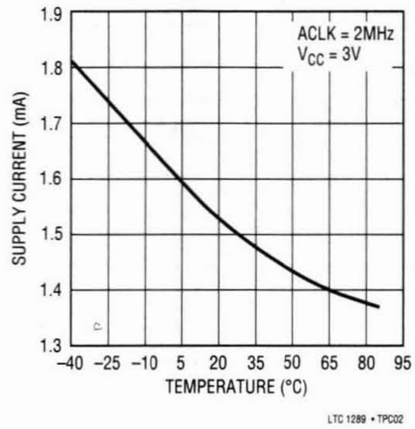
Note 10: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it's recommended that $f_{ACLK} \geq$ 125kHz at 85°C and $f_{ACLK} \geq$ 15kHz at 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

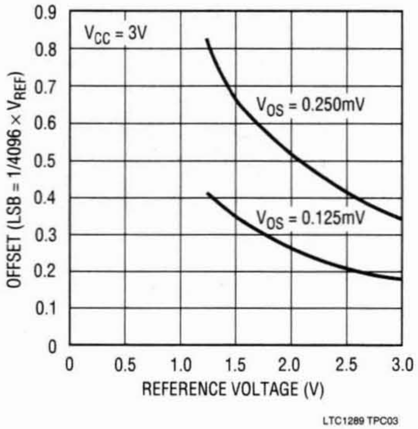
Supply Current vs Supply Voltage



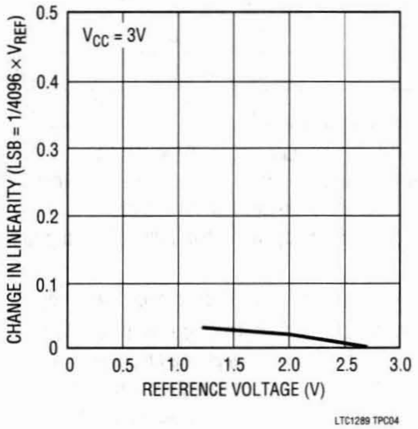
Supply Current vs Temperature



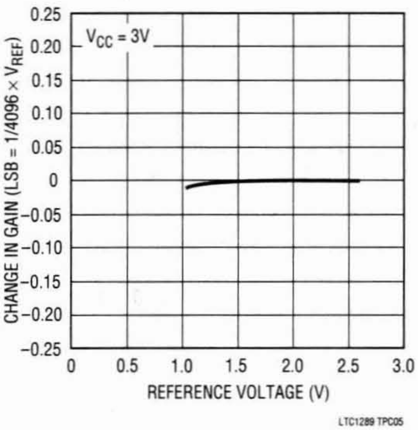
Unadjusted Offset Voltage vs Reference Voltage



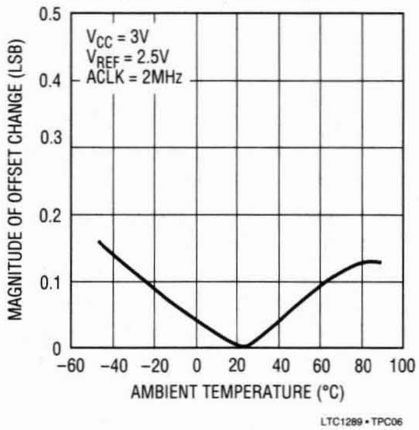
Change in Linearity vs Reference Voltage



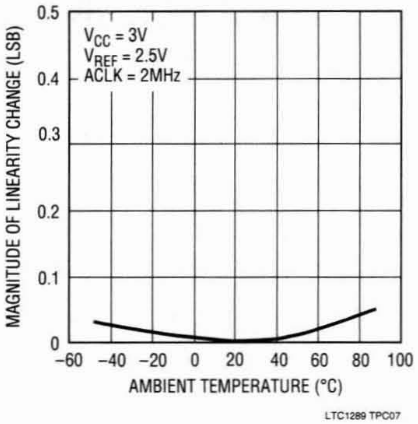
Change in Gain vs Reference Voltage



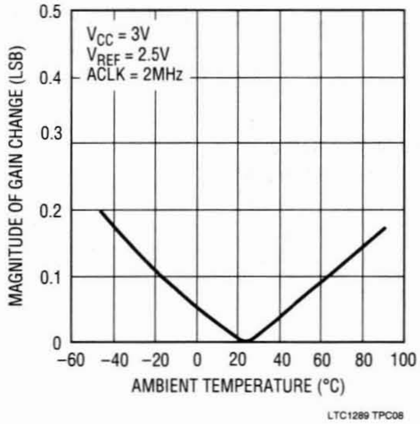
Change in Offset vs Temperature



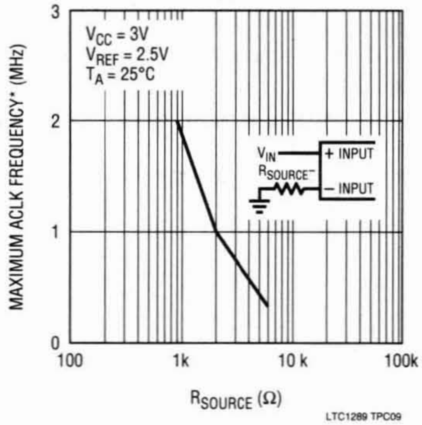
Change in Linearity vs Temperature



Change in Gain vs Temperature



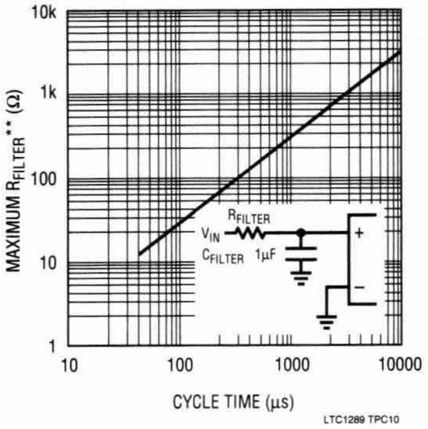
Maximum ACLK Frequency vs Source Resistance



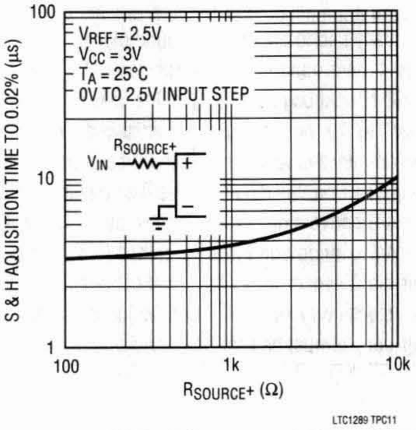
* MAXIMUM ACLK FREQUENCY REPRESENTS THE ACLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 2MHZ VALUE IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

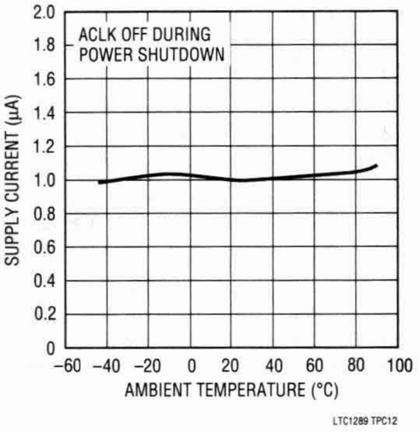
Maximum Filter Resistor vs Cycle Time



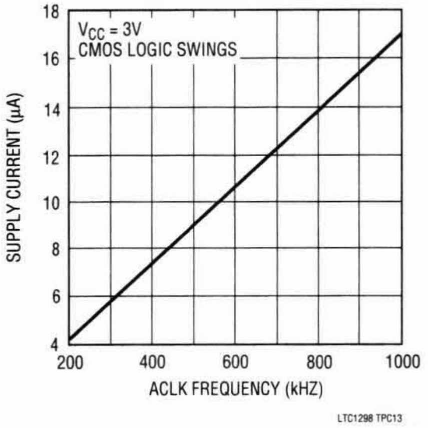
Sample and Hold Acquisition Time vs Source Resistance



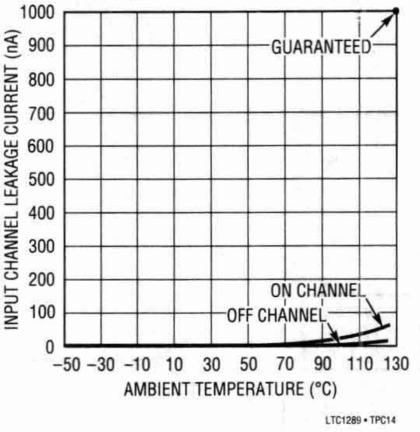
Supply Current (Power Shutdown) vs Temperature



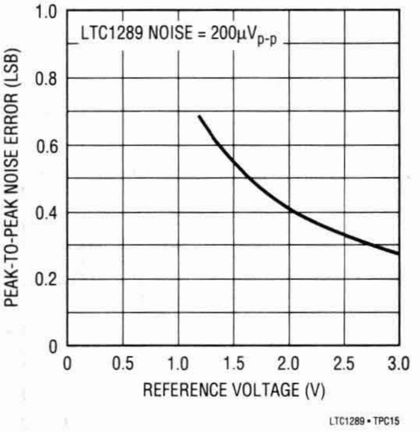
Supply Current (Power Shutdown) vs ACLK



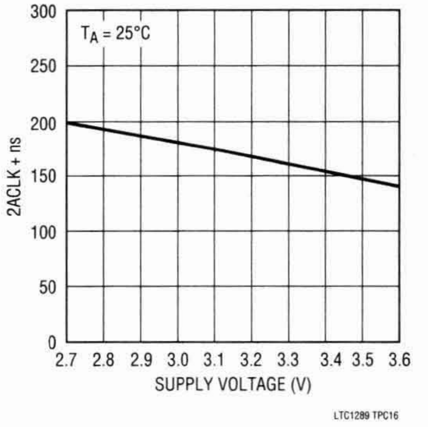
Input Channel Leakage Current vs Temperature



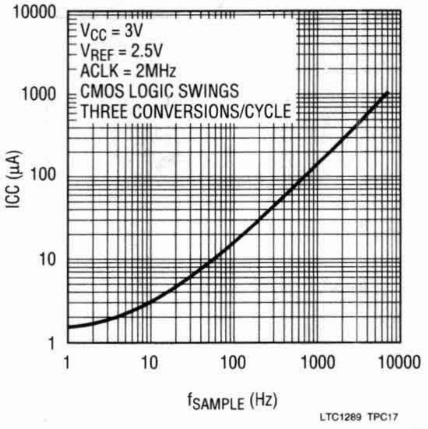
Noise Error vs Reference Voltage



$t_{su\overline{CS}}$ vs Supply Voltage



Power Consumption with Power Shutdown vs f_{SAMPLE}

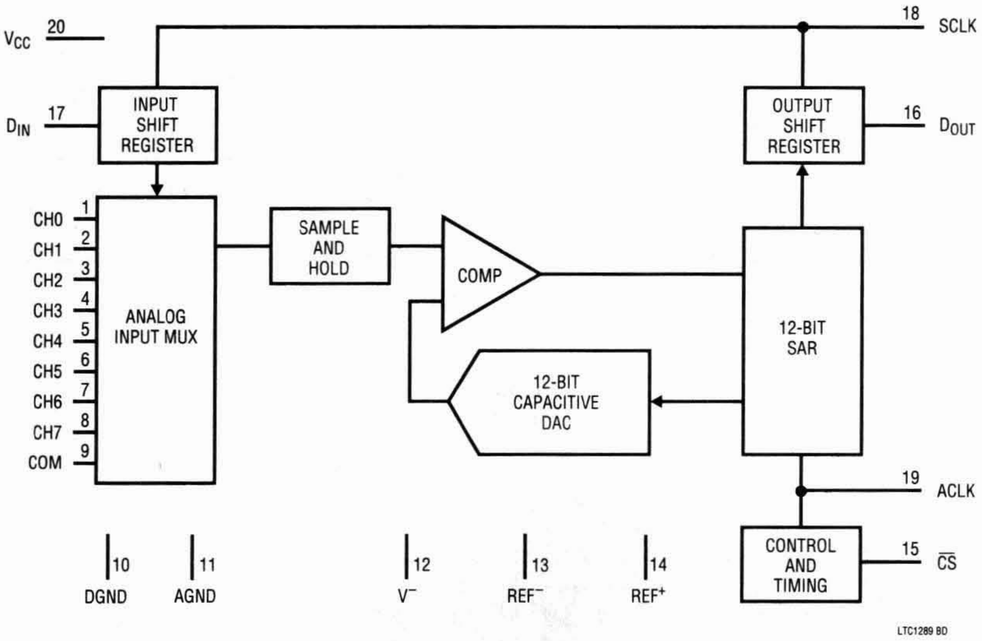


** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0 IS FIRST DETECTED.

PIN FUNCTIONS

#	PIN	FUNCTION	DESCRIPTION
1 – 8	CH0 – CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single-ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
12	V^-	Negative Supply	Tie V^- to the most negative potential in the circuit. (Ground in single supply applications.)
13,14	REF^-, REF^+	Reference Inputs	The reference inputs must be kept free of noise with respect to AGND.
15	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	D_{IN}	Digital Input	The A/D configuration word is shifted into this input.
18	SCLK	Shift Clock	This clock synchronizes the serial data transfer.
19	ACLK	A/D Conversion Clock	This clock controls the A/D conversion process.
20	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

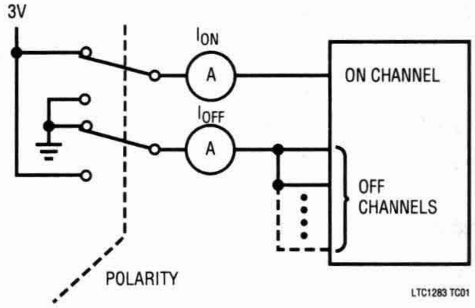
BLOCK DIAGRAM



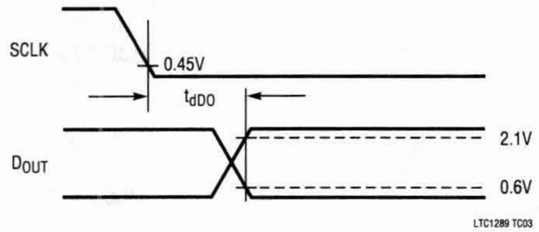
V_{CC}
20
D_{IN}
17
INPUT SHIFT REGISTER
18
SCLK
OUTPUT SHIFT REGISTER
16
D_{OUT}
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
ANALOG INPUT MUX
SAMPLE AND HOLD
COMP
12-BIT CAPACITIVE DAC
12-BIT SAR
19
ACLK
CONTROL AND TIMING
15
$\overline{CS}$
10 DGND
11 AGND
12 V^-
13 REF^-
14 REF^+
LTC1289 BD

TEST CIRCUITS

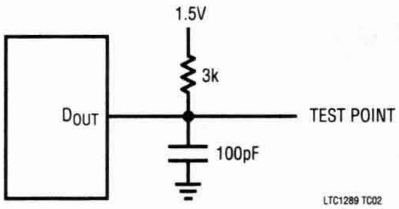
On and Off Channel Leakage Current


3V
I_{ON}
A
ON CHANNEL
I_{OFF}
A
OFF CHANNELS
POLARITY
LTC1283 TC01

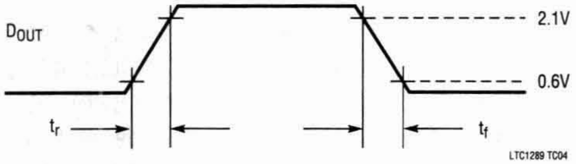
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}


SCLK
0.45V
t_{dDO}
D_{OUT}
2.1V
0.6V
LTC1289 TC03

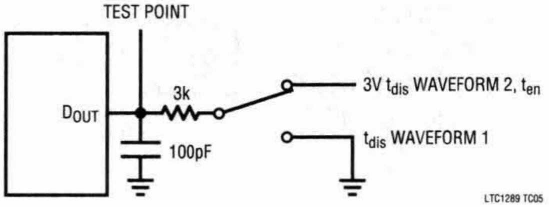
Load Circuit for t_{dDO}, t_r and t_f


1.5V
3k
D_{OUT}
TEST POINT
100pF
LTC1289 TC02

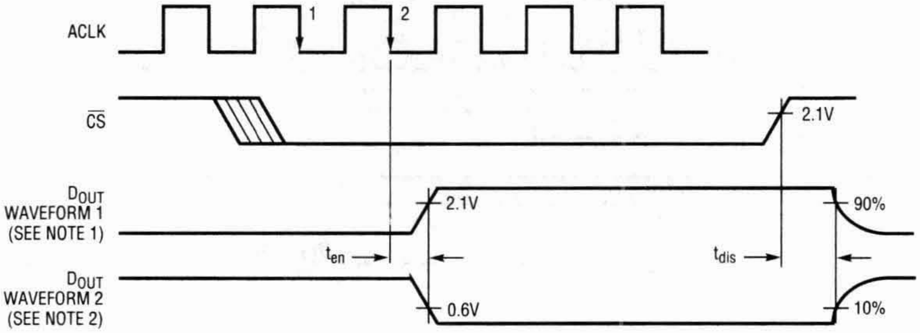
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r,t_f


D_{OUT}
2.1V
0.6V
t_r
t_f
LTC1289 TC04

Load Circuit for t_{dis} and t_{en}


TEST POINT
D_{OUT}
3k
100pF
3V t_{dis} WAVEFORM 2, t_{en}
t_{dis} WAVEFORM 1
LTC1289 TC05

Voltage Waveforms for t_{en} and t_{dis}


ACLK
1
2
$\overline{CS}$
2.1V
D_{OUT} WAVEFORM 1 (SEE NOTE 1)
2.1V
90%
t_{en}
t_{dis}
D_{OUT} WAVEFORM 2 (SEE NOTE 2)
0.6V
10%

NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

LTC1289 TC06

APPLICATIONS INFORMATION

The LTC1289 is a data acquisition component which contains the following functional blocks:

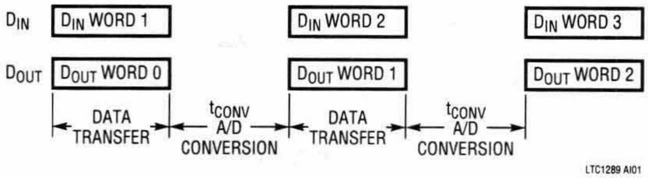
1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, full duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

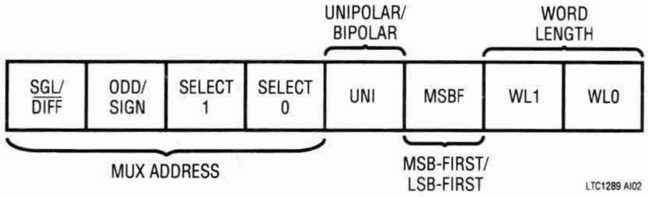
The LTC1289 communicates with microprocessors and other external circuitry via a synchronous, full duplex, four wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After the falling $\overline{CS}$ is recognized, an 8-bit input word is shifted into the D_{IN} input which configures the LTC1289 for the next conversion. Simultaneously, the result of the previous conversion is output on the D_{OUT} line. At the end of the data exchange the requested conversion begins and $\overline{CS}$ should be brought high. After t_{CONV}, the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one $\overline{CS}$ cycle from the input word requesting it.

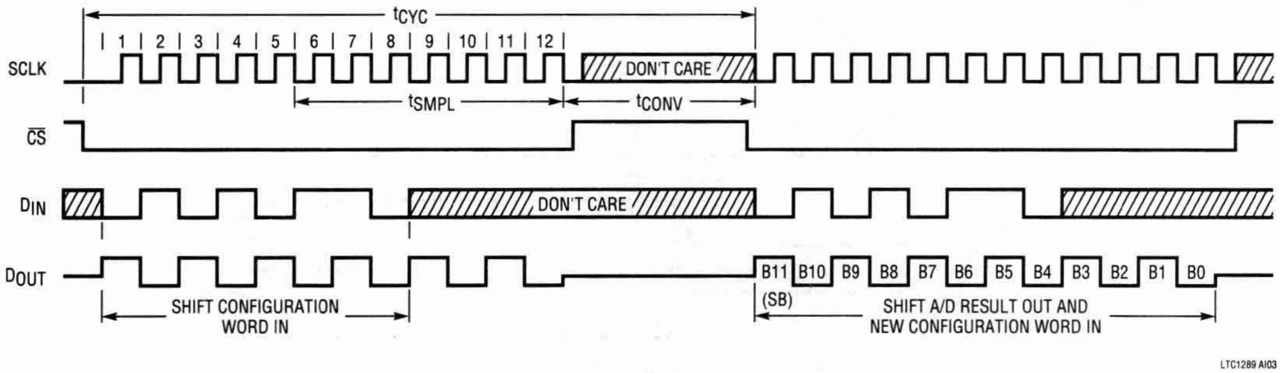

DIN
DIN WORD 1
DIN WORD 2
DIN WORD 3
DOUT
DOUT WORD 0
DOUT WORD 1
DOUT WORD 2
DATA TRANSFER
tCONV A/D CONVERSION
DATA TRANSFER
tCONV A/D CONVERSION
LTC1289 AI01

Input Data Word

The LTC1289 8-bit data word is clocked into the D_{IN} input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The eight bits of the input word are defined as follows:


UNIPOLAR/ BIPOLAR
WORD LENGTH
SGL/ DIFF
ODD/ SIGN
SELECT 1
SELECT 0
UNI
MSBF
WL1
WL0
MUX ADDRESS
MSB-FIRST/ LSB-FIRST
LTC1289 AI02

Operating Sequence
(Example: Differential Inputs (CH3-CH2), Bipolar, MSB-First and 12-Bit Word Length)


tCYC
1
2
3
4
5
6
7
8
9
10
11
12
SCLK
DON'T CARE
tSMPL
tCONV
CS
DIN
DON'T CARE
DOUT
B11
B10
B9
B8
B7
B6
B5
B4
B3
B2
B1
B0
(SB)
SHIFT CONFIGURATION WORD IN
SHIFT A/D RESULT OUT AND NEW CONFIGURATION WORD IN
LTC1289 AI03

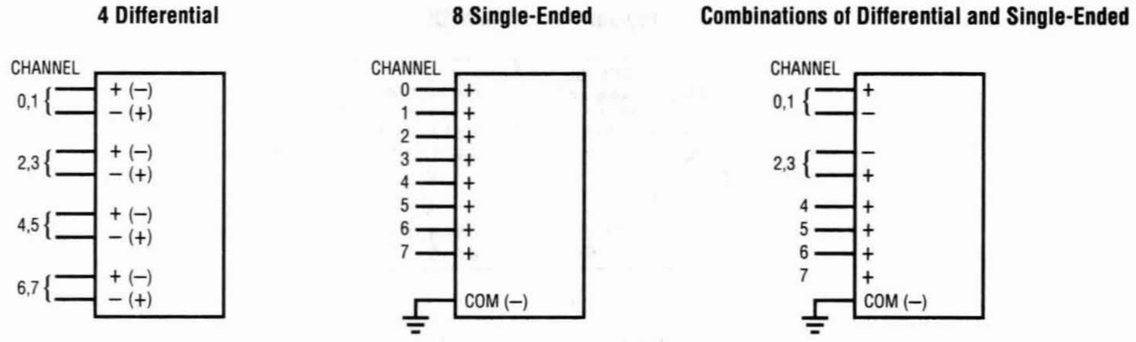
APPLICATIONS INFORMATION

MUX Address

The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of Table 1. Note that in differential mode (SGL/$\overline{\text{DIFF}}$ = 0) measurements are limited to four adjacent input pairs with either polarity. In single-ended mode, all input channels are measured with respect to COM.

Table 1. Multiplexer Channel Selection

MUX ADDRESS			DIFFERENTIAL CHANNEL SELECTION								MUX ADDRESS			SINGLE-ENDED CHANNEL SELECTION								
SGL/ $\overline{\text{DIFF}}$	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	6	7	SGL/ $\overline{\text{DIFF}}$	ODD SIGN	SELECT 1 0	0	1	2	3	4	5	6	7	COM
0	0	0 0	+	–							1	0	0 0	+								–
0	0	0 1			+	–					1	0	0 1			+						–
0	0	1 0					+	–			1	0	1 0					+				–
0	0	1 1							+	–	1	0	1 1							+		–
0	1	0 0	–	+							1	1	0 0		+							–
0	1	0 1			–	+					1	1	0 1				+					–
0	1	1 0					–	+			1	1	1 0						+			–
0	1	1 1							–	+	1	1	1 1								+	–



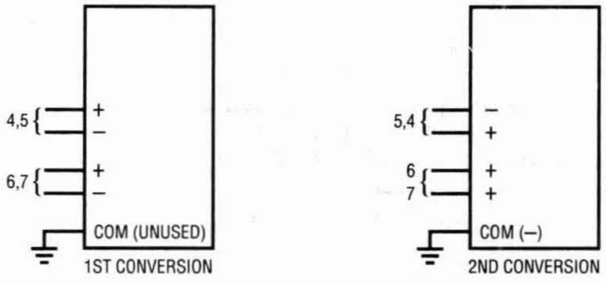
4 Differential

8 Single-Ended

Combinations of Differential and Single-Ended

CHANNEL
0,1
+ (–)
– (+)
2,3
+ (–)
– (+)
4,5
+ (–)
– (+)
6,7
+ (–)
– (+)
CHANNEL
0
1
2
3
4
5
6
7
COM (–)
CHANNEL
0,1
2,3
4
5
6
7
COM (–)

Changing the MUX Assignment "On the Fly"



4,5
6,7
COM (UNUSED)
1ST CONVERSION
5,4
6
7
COM (–)
2ND CONVERSION
LTC1289 AIF01

Figure 1. Examples of Multiplexer Options on the LTC1289

APPLICATIONS INFORMATION

Unipolar/Bipolar (UNI)

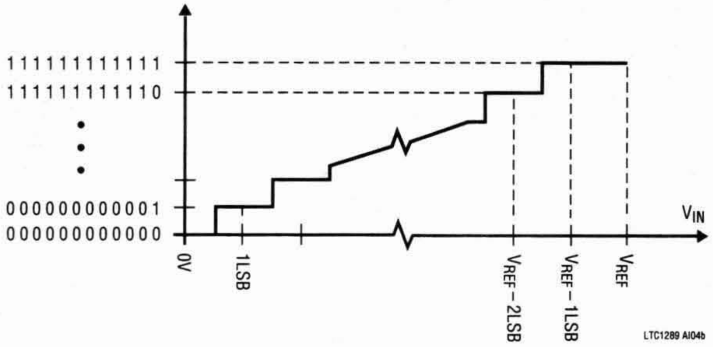
The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.5V)
111111111111	V_{REF} – 1LSB	2.4994V
111111111110	V_{REF} – 2LSB	2.4988V
•	•	•
•	•	•
•	•	•
000000000001	1LSB	0.0006V
000000000000	0V	0V

LTC1289 AI04a

Unipolar Transfer Curve (UNI = 1)



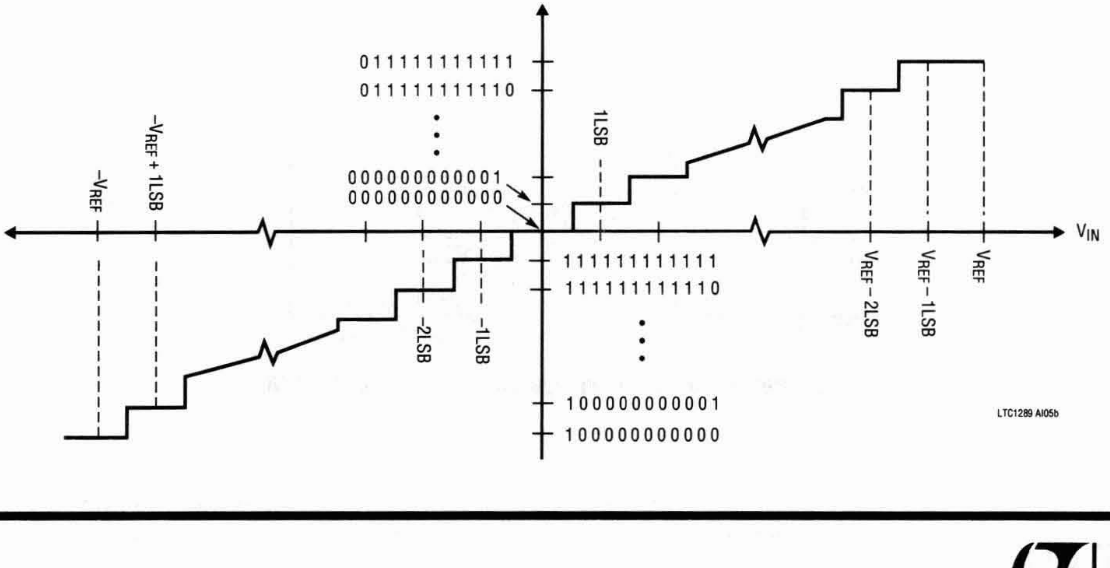
LTC1289 AI04b

Bipolar Output Code (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.5V)	OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 2.5V)
011111111111	V_{REF} – 1LSB	2.4988V	111111111111	–1LSB	–0.0012V
011111111110	V_{REF} – 2LSB	2.4976V	111111111110	–2LSB	–0.0024V
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
000000000001	1LSB	0.0012V	100000000001	–(V_{REF}) + 1LSB	–2.4988V
000000000000	0V	0V	100000000000	– (V_{REF})	–2.5000V

LTC1289 AI05a

Bipolar Transfer Curve (UNI = 0)



LTC1289 AI05b

APPLICATIONS INFORMATION

The following discussion will demonstrate how the two reference pins are to be used in conjunction with the analog input multiplexer. In unipolar mode the input span of the A/D is set by the difference in voltage on the REF^+ pin and the REF^- pin. In the bipolar mode the input span is twice the difference in voltage on the REF^+ pin and the REF^- pin. In the unipolar mode the lower value of the input span is set by the voltage on the COM pin for single-ended inputs and by the voltage on the minus input pin for differential inputs. For the bipolar mode of operation the voltage on the COM pin or the minus input pin sets the center of the input span.

The upper and lower value of the input span can now be summarized in the following table:

INPUT CONFIGURATION		UNIPOLAR MODE	BIPOLAR MODE
Single-Ended	Lower Value	COM	$-(REF^+ - REF^-) + COM$
	Upper Value	$(REF^+ - REF^-) + COM$	$(REF^+ - REF^-) + COM$
Differential	Lower Value	IN^-	$-(REF^+ - REF^-) + IN^-$
	Upper Value	$(REF^+ - REF^-) + IN^-$	$(REF^+ - REF^-) + IN^-$

The reference voltages REF^+ and REF^- can fall between V_{CC} and V^-, but the difference ($REF^+ - REF^-$) must be less than or equal to V_{CC}. The input voltages must be less than or equal to V_{CC} and greater than or equal to V^-.

The following examples are for a single-ended input configuration.

Example 1: Let $V_{CC} = 3.3V$, $V^- = 0V$, $REF^+ = 3V$, $REF^- = 1V$ and COM = 0V. Unipolar mode of operation. The resulting input span is $0V \leq IN^+ \leq 2V$.

Example 2: The same conditions as Example 1 except COM = 1V. The resulting input span is $1V \leq IN^+ \leq 3V$. Note if $IN^+ \geq 3V$ the resulting D_{OUT} word is all 1's. If $IN^+ \leq 1V$ then the resulting D_{OUT} word is all 0's.

Example 3: Let $V_{CC} = 3.3V$, $V^- = -3.3V$, $REF^+ = 3V$, $REF^- = 1V$ and COM = 1V. Bipolar mode of operation. The resulting input span is $-1V \leq IN+ \leq 3V$.

For differential input configurations with the same conditions as in the above three examples the resulting input spans are as follows:

Example 1 (Diff.): $IN^- \leq IN^+ \leq IN^- + 2V$

Example 2 (Diff.): $IN^- \leq IN^+ \leq IN^- + 2V$

Example 3 (Diff.): $IN^- - 2V \leq IN^+ \leq IN^- + 2V$.

MSB-First/LSB-First Format (MSBF)

The output data of the LTC1289 is programmed for MSB-first or LSB-first sequence using the MSBF bit. For MSB-first output data, the input word clocked to the LTC1289 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB-first output data the input word clocked to the LTC1289 should always contain a zero in the MSBF bit location. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

MSBF	OUTPUT FORMAT
0	LSB-First
1	MSB-First

LTC1289 AI06

Word Length (WL1, WL0) and Power Shutdown

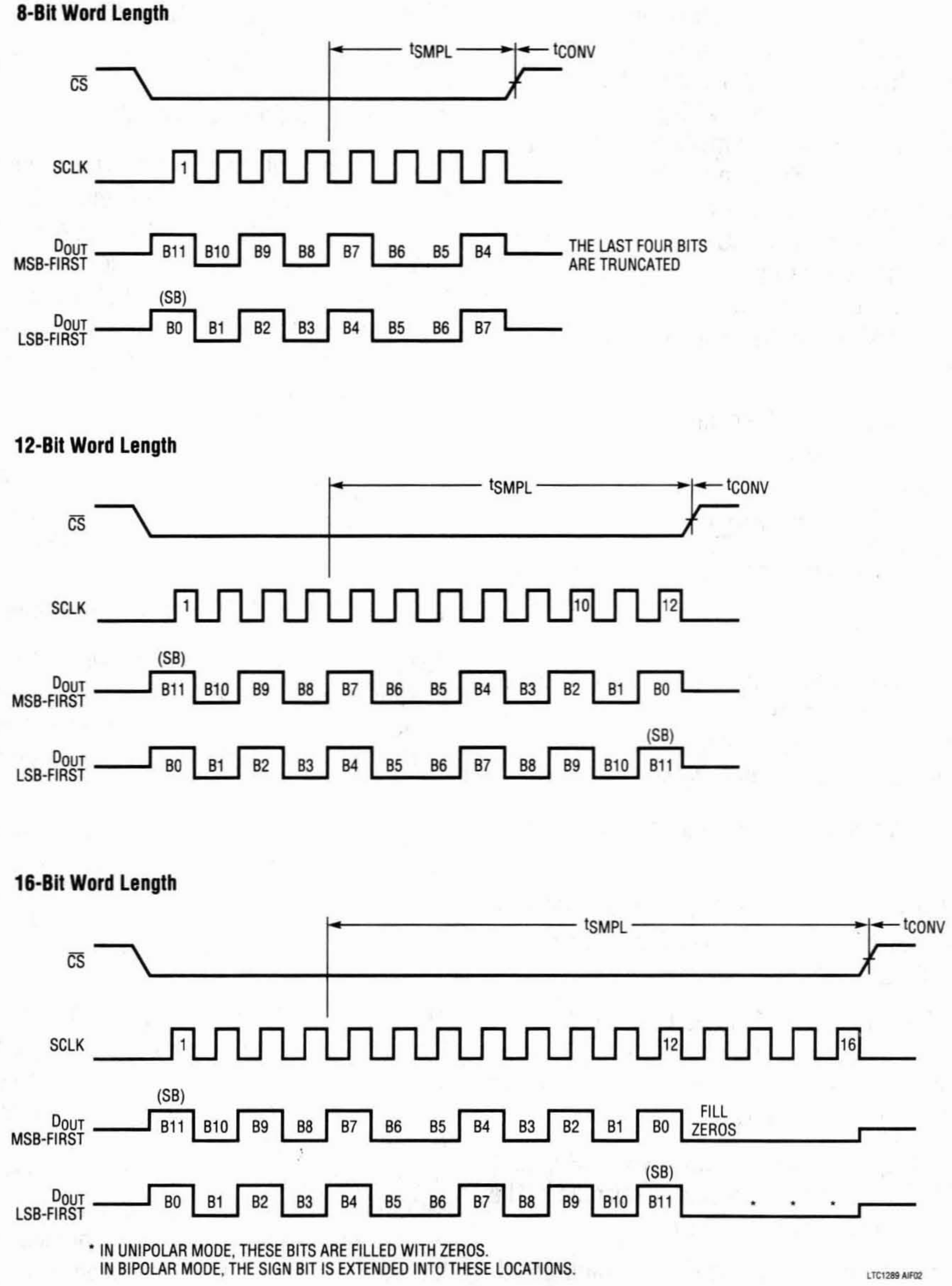
The last two bits of the input word (WL1 and WL0) program the output data word length and the power shutdown feature of the LTC1289. Word lengths of 8, 12 or 16 bits can be selected according to the following table.

WL1	WL0	OUTPUT WORD LENGTH
0	0	8 Bits
0	1	Power Shutdown
1	0	12 Bits
1	1	16 Bits

LTC1289 AI07

The WL1 and WL0 bits in a given D_{IN} word control the length of the present, not the next, D_{OUT} word. WL1 and WL0 are never "don't cares" and must be set for the correct D_{OUT} word length even when a "dummy" D_{IN} word is sent. On any transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU. Power down will occur when WL1 = 0 and WL0 = 1 is selected. The previous result will be clocked out as a 10 bit word so a "dummy"conversion is required before powering down the LTC1289. Conversions are resumed once $\overline{CS}$ goes low or an SCLK is applied, if $\overline{CS}$ is already low.

APPLICATIONS INFORMATION



8-Bit Word Length

12-Bit Word Length

16-Bit Word Length

tSMPL
tCONV
CS
SCLK
1
10
12
16
DOUT MSB-FIRST
DOUT LSB-FIRST
(SB)
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11
THE LAST FOUR BITS ARE TRUNCATED
FILL ZEROS
* * *
LTC1289 AIF02

* IN UNIPOLAR MODE, THESE BITS ARE FILLED WITH ZEROS.
IN BIPOLAR MODE, THE SIGN BIT IS EXTENDED INTO THESE LOCATIONS.

Figure 2. Data Output (D_{OUT}) Timing with Different Word Lengths

APPLICATIONS INFORMATION

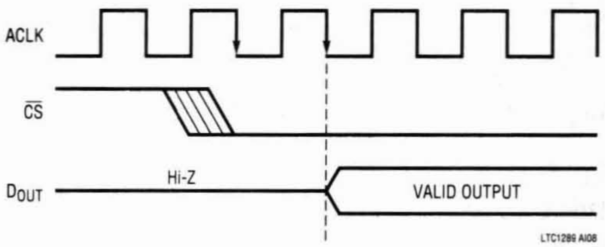
Deglitcher

A deglitching circuit has been added to the Chip Select input of the LTC1289 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the $\overline{CS}$ input that are shorter in duration than one ACLK cycle. After a change of state on the $\overline{CS}$ input, the LTC1289 waits for two falling edge of the ACLK before recognizing a valid chip select. One indication of $\overline{CS}$ recognition is the D_{OUT} line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling $\overline{CS}$ edges.

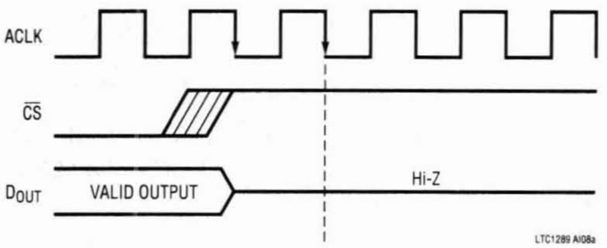
$\overline{CS}$ Low During Conversion

In the normal mode of operation, $\overline{CS}$ is brought high during the conversion time. The serial port ignores any SCLK activity while $\overline{CS}$ is high. The LTC1289 will also operate with $\overline{CS}$ low during the conversion. In this mode, SCLK must remain low during the conversion as shown in the following figure. After the conversion is complete, the D_{OUT} line will become active with the first output bit. Then the data transfer can begin as normal.

Low $\overline{CS}$ Recognized Internally


ACLK
CS
DOUT
Hi-Z
VALID OUTPUT
LTC1289 AI08

High $\overline{CS}$ Recognized Internally


ACLK
CS
DOUT
VALID OUTPUT
Hi-Z
LTC1289 AI08a

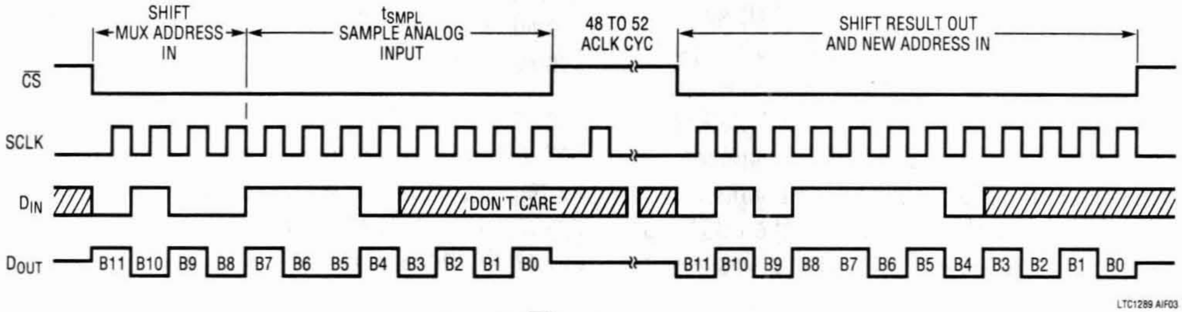

SHIFT
MUX ADDRESS
IN
tSMPL
SAMPLE ANALOG
INPUT
48 TO 52
ACLK CYC
SHIFT RESULT OUT
AND NEW ADDRESS IN
CS
SCLK
DIN
DON'T CARE
DOUT
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
LTC1289 AIF03

Figure 3. $\overline{CS}$ High During Conversion

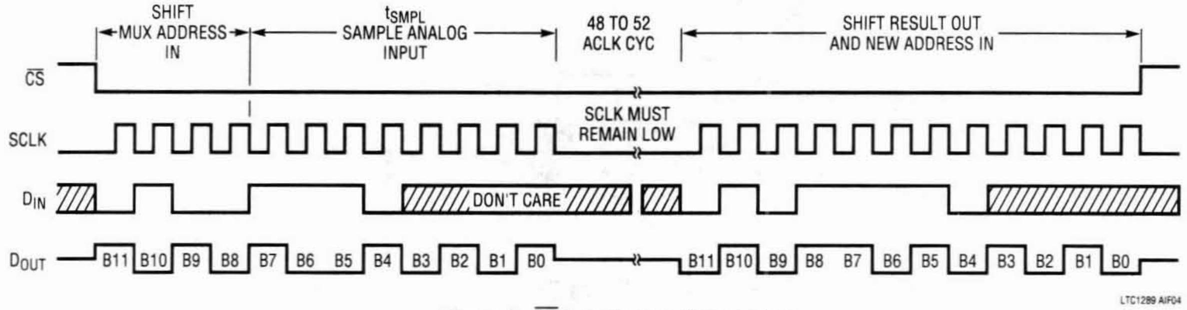

SHIFT
MUX ADDRESS
IN
tSMPL
SAMPLE ANALOG
INPUT
48 TO 52
ACLK CYC
SHIFT RESULT OUT
AND NEW ADDRESS IN
CS
SCLK
SCLK MUST
REMAIN LOW
DIN
DON'T CARE
DOUT
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
LTC1289 AIF04

Figure 4. $\overline{CS}$ Low During Conversion

APPLICATIONS INFORMATION

Logic Levels

The logic level standards for this supply range have not been well defined. What standards that do exist are not universally accepted. The trip point on the logic inputs of the LTC1289 is 0.28 × V_{CC}. This makes the logic inputs compatible with HC type logic levels and processors that are specified at 3.3V. The output D_{OUT} is also compatible with the above standards. The following summarizes such levels.

V_{OH} (no load)	V_{CC} - 0.1V
V_{OL} (no load)	0.1V
V_{OH}	0.9 × V_{CC}
V_{OL}	0.1 × V_{CC}
V_{IH}	0.7 × V_{CC}
V_{IL}	0.2 × V_{CC}

The LTC1289 can be driven with 5V logic even when V_{CC} is at 3.3V. This is due to a unique input protection device that is found on the LTC1289.

Microprocessor Interfaces

The LTC1289 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats. If an MPU without a serial interface is used, then four of the MPU's parallel port lines can be programmed to form the serial link to the LTC1289. Many of the popular MPU's can operate with 3V supplies. For example the MC68HC11 is an MPU with a serial format (SPI). Likewise parallel MPU's that have the 8051 type architecture are also capable of operating at this voltage range. The code for these processors remains the same and can be found in the LTC1290 datasheet or application notes AN36A and AN36B.

Sharing the Serial Interface

The LTC1289 can share 3-wire serial interface with other peripheral components or other LTC1289s (See Figure 5). In this case, the $\overline{CS}$ signals decide which LTC1289 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1289 should be used with an analog ground plane and single point grounding techniques.

Pin 11 (AGND) should be tied directly to this ground plane.

Pin 10 (DGND) can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

Pin 20 (V_{CC}) should be bypassed to the ground plane with a 22µF tantalum with leads as short as possible. Pin 12 (V^-) should be bypassed with a 0.1µF ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that pin 13 (REF^-) and pin 9 (COM) be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

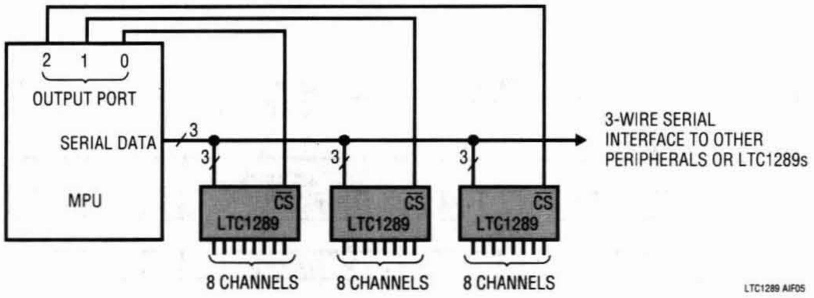


Figure 5. Several LTC1289s Sharing One 3-Wire Serial Interface

APPLICATIONS INFORMATION

Figure 6 shows an example of an ideal ground plane design for a two-sided board. Of course, this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a 22µF tantalum capacitor and leads as short as possible. The lead from the device to the V_{CC} supply should also be kept to a minimum and the V_{CC} supply should have a low output impedance such as that obtained from a voltage regulator (e.g., LT1117). Using a battery to power the LTC1289 will help reduce the amount of bypass capacitance required on the V_{CC} pin. A battery placed close to the device will only require 10µF to adequately bypass the supply pin. Figure 7 shows the effect of poor V_{CC} bypassing. Figure 8a shows the settling of a LT1117 low dropout regulator with a 22µF bypass capacitor. The noise and ripple is approximately 0.5mV. Figure 8b shows the response of a lithium battery with a 10µF bypass capacitor. The noise and ripple is kept below 0.5mV.

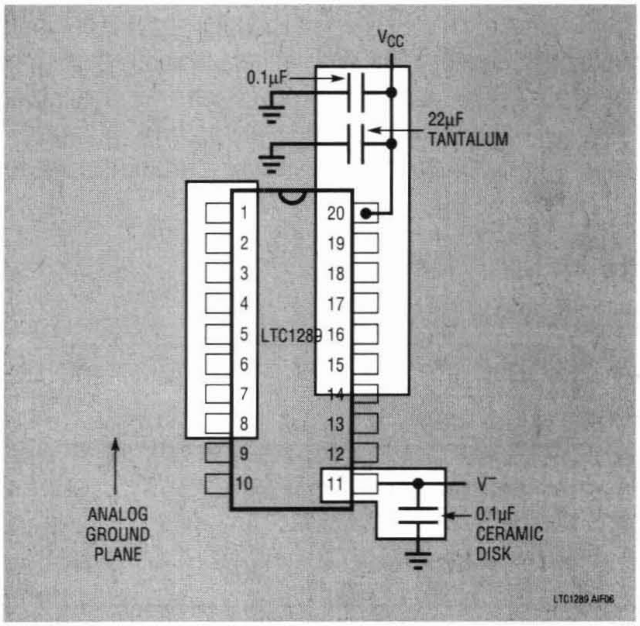


Figure 6. Example Ground Plane for the LTC1289

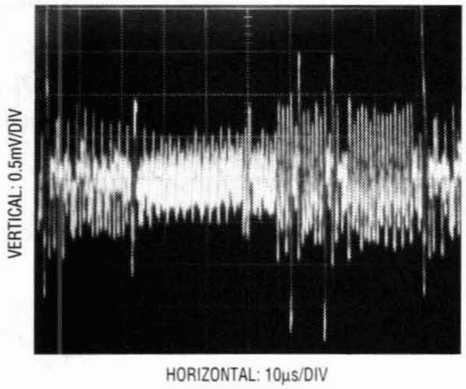


Figure 7. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors.

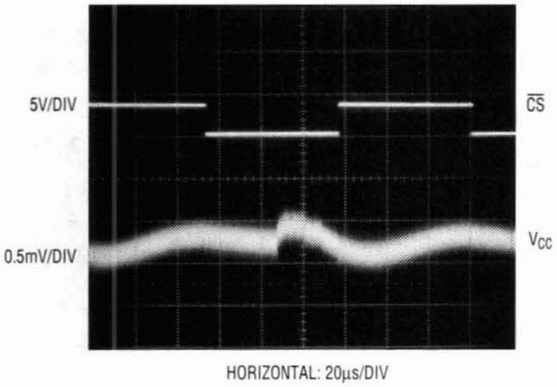


Figure 8a. LT1117 Regulator with 22µF Bypassing on V_{CC}

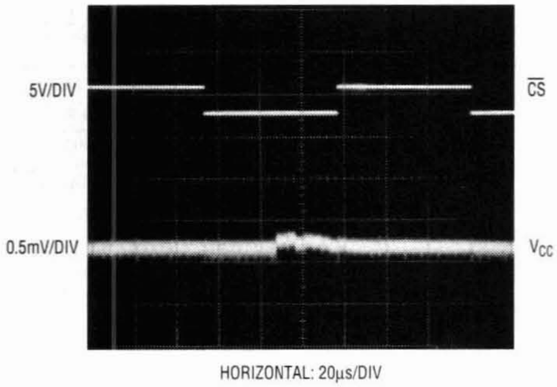


Figure 8b. Lithium Battery with 10µF Bypassing on V_{CC}

APPLICATIONS INFORMATION

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1289 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1289 look like a 100pF capacitor (C_{IN}) is series with a 1500Ω resistor (R_{ON}) as shown in Figure 9. This value for R_{ON} is for V_{CC} = 2.7V. With larger supply voltages R_{ON} will be reduced. For example with V_{CC} = 2.7V and V^-= −2.7V R_{ON} becomes 500Ω. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allotted time.

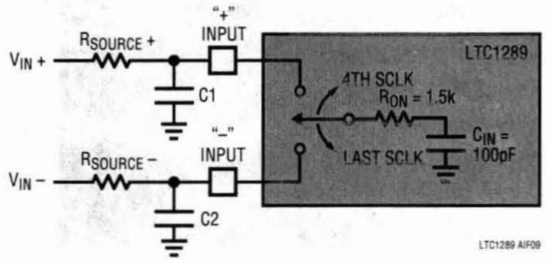

"+"
INPUT
R_{SOURCE} +
V_{IN} +
C1
"–"
INPUT
R_{SOURCE} –
V_{IN} –
C2
LTC1289
4TH SCLK
R_{ON} = 1.5k
C_{IN} = 100pF
LAST SCLK
LTC1289 AIF09

Figure 9. Analog Input Equivalent Circuit

"+" Input Settling

This input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 10). The sample phase starts at the 4th SCLK cycle and lasts until the falling edge of the last SCLK (the 8th, 12th or 16th SCLK cycle depending on the selected word length). The voltage on the "+" input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower SCLK frequency or selecting a longer word length. With the minimum possible sample time of 4μs, **R_{SOURCE}^+ < 2k and C1 < 20pF will provide adequate settling**.

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 10). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. However, it is critical that the "–" input voltage be free of noise and settle completely during the first four ACLK cycles of the conversion time. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large "–" input source resistance must be used, the time allowed for

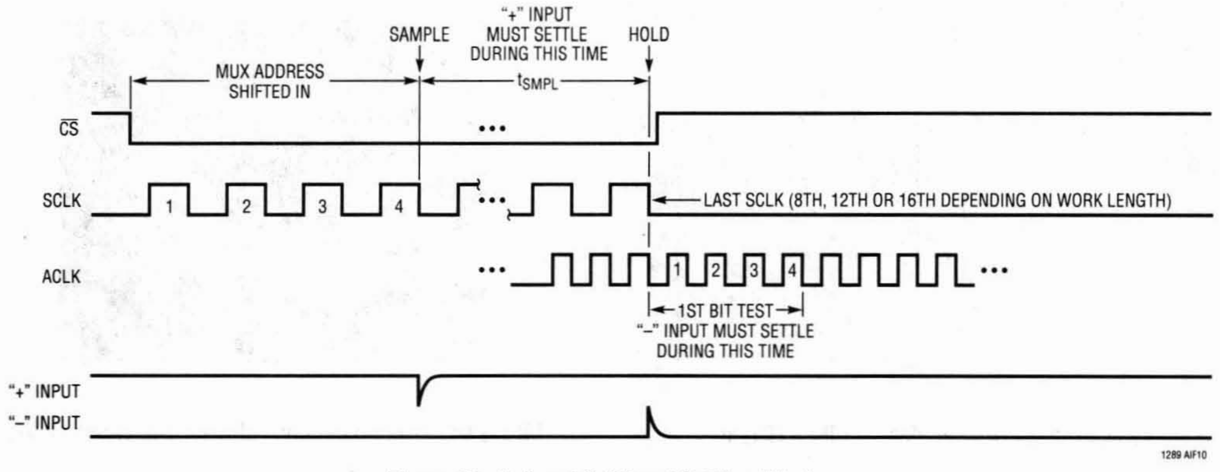

"+" INPUT
MUST SETTLE
DURING THIS TIME
SAMPLE
HOLD
MUX ADDRESS
SHIFTED IN
t_{SMPL}
CS
SCLK
1
2
3
4
LAST SCLK (8TH, 12TH OR 16TH DEPENDING ON WORK LENGTH)
ACLK
1
2
3
4
1ST BIT TEST
"–" INPUT MUST SETTLE
DURING THIS TIME
"+" INPUT
"–" INPUT
1289 AIF10

Figure 10. "+" and "–" Input Settling Windows

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settling can be extended by using a slower ACLK frequency. At the maximum ACLK rate of 2MHz, **$R_{SOURCE}^- < 200\Omega$ and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 10). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. For single supply low voltage applications the LT1006, LT1013 and LT1014 can be made to settle well even with the minimum settling windows of 4µs ("+" input) and 2µs ("–" input) which occur at the maximum clock rates (ACLK = 2MHz and SCLK = 1MHz). Figures 11 and 12 show examples of adequate and poor op amp settling. The LT1077, LT1078 or LT1079 can be used here to reduce power consumption. Placing an RC network at the output of the op amps will improve the settling response and also reduce the broadband noise.

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 13. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 40µs, the input current equals 6.3µA at $V_{IN} = 2.5V$. In this case, a filter resistor of 10Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 85°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 1.6LSB with $V_{REF} = 2.5V$. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

Noise Coupling Into Inputs

High source resistance input signals (>500Ω) are more sensitive to coupling from external sources. It is preferable to use channels near the center of the package (i.e., CH2-CH7) for signals which have the highest output resistance because they are essentially shielded by the

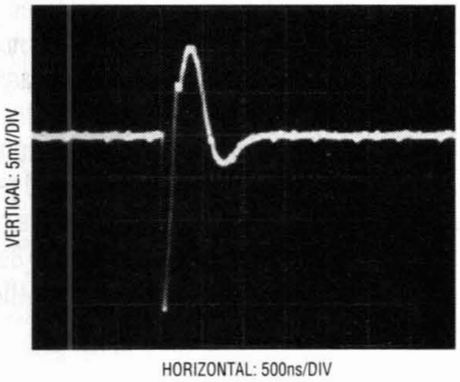


Figure 11. Adequate Settling of Op Amps Driving Analog Input

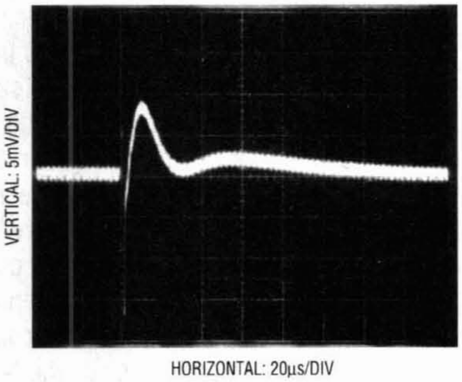


Figure 12. Poor Op Amp Settling Can Cause A/D Errors

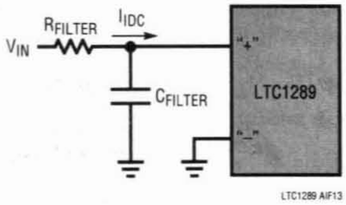


Figure 13. RC Input Filtering

APPLICATIONS INFORMATION

pins on the package ends (DGND and CH0). Grounding any unused inputs (especially the end pin, CH0) will also reduce outside coupling into high source resistances.

4. Sample and Hold

Single-Ended Inputs

The LTC1289 provides a built-in sample and hold (S&H) function for all signals acquired in the single-ended mode (COM pin grounded). This sample and hold allows the LTC1289 to convert rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 10. The sampling interval begins after the fourth MUX address bit is shifted in and continues during the remainder of the data transfer. On the falling edge of the final SCLK, the S&H goes into hold mode and the conversion begins. The voltage will be held on either the 8th, 12th or 16th falling edge of the SCLK depending on the word length selected.

Differential Inputs

With differential inputs or when the COM pin is not tied to ground, the A/D no longer converts just a single voltage but rather the difference between two voltages. In these cases, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varing just as in single ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 52 ACLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f(\text{“}-\text{”}) \times \frac{52}{f_{ACLK}}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{ACLK} is the frequency of the ACLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (150µV) with the converter running at ACLK = 2MHz, its peak value would have to be 15mV.

5. Reference Inputs

The voltage between the reference inputs of the LTC1289 defines the voltage span of the A/D converter. The reference inputs will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 14). During each bit test of the conversion (every 4 ACLK cycles), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

When driving the reference inputs, two things should be kept in mind:

1. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each 4 ACLK cycles). Figures 15 and 16 show examples of both adequate and poor settling. Using a slower ACLK will allow more time for the reference to settle. However, even at the maximum ACLK rate of 2MHz most references and op amps can be made to settle within the 2µs bit time. For example an LT1019 used in the shunt mode with a 10µF bypass capacitor will settle adequately. To minimize power an LT1004-2.5 can be used with a 10µF bypass capacitor. For lower value references the LT1004-1.2 with a 1µF bypass capacitor can be used.

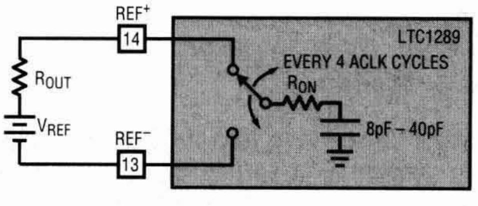


Figure 14. Reference Input Equivalent Circuit

APPLICATIONS INFORMATION

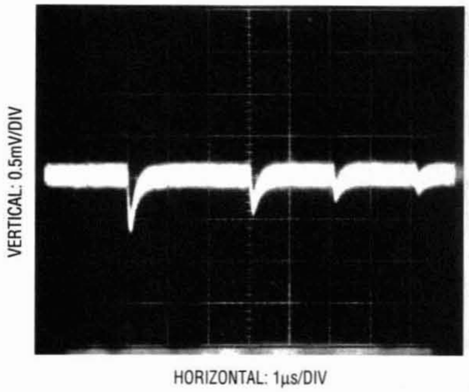


Figure 15. Adequate Reference Settling

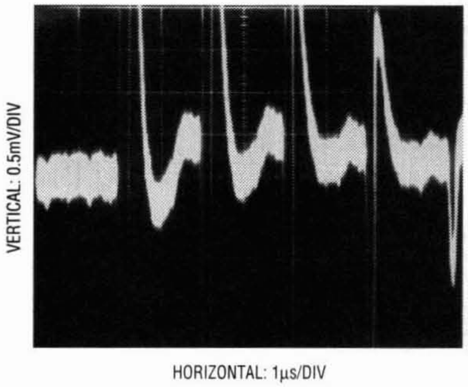


Figure 16. Poor Reference Settling Can Cause A/D Errors

2. It is recommended that REF^- input be tied directly to the analog ground plane. If REF^- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

6. Reduced Reference Operation

The effective resolution of the LTC1289 can be increased by reducing the input span of the converter. The LTC1289 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Gain Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values:

1. Offset
2. Noise

Offset with Reduced V_{REF}

The offset of the LTC1289 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 0.1mV which is 0.2LSB with a 2.5V reference becomes 0.4LSB with a 1.25V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1289.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1289 can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 2.5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

For operation with a 2.5 reference, the 200µV noise is only 0.32LSB peak-to-peak. In this case, the LTC1289 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this same 200µV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF}, V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

APPLICATIONS INFORMATION

7. LTC1289 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/D's in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "effective number of bits (ENOB)." SNR is defined as the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the nonfundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by:

$$SNR = (6.02N + 1.76dB)$$

where N is the number of bits. Thus the SNR is a function of the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. A Fast Fourier Transform(FFT) plot of the output spectrum of the LTC1289 is shown in Figures 17a and 17b. The input (f_{IN}) frequencies are 1kHz and 12kHz with the sampling frequency (f_S) at 25kHz. The SNR obtained from the plot are 72.92dB and 72.23dB.

Rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = \frac{SNR - 1.76dB}{6.02}$$

This is the so-called effective number of bits (ENOB). For the example shown in Figures 17a and 17b, N = 11.8 bits and 11.7 bits, respectively. Figure 18 shows a plot of ENOB as a function of input frequency. The curve shows the A/D's ENOB remain in the range of 11.8 to 11.7 for input frequencies up to $f_S/2$

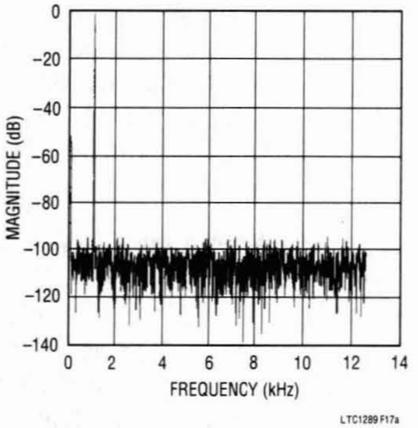


Figure 17a. f_{IN} = 1kHz, f_S = 25kHz, SNR = 72.92dB

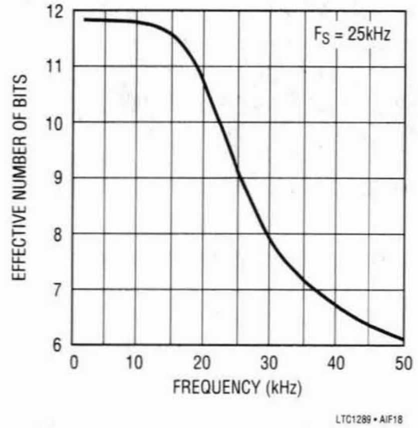


Figure 18. LTC1289 ENOB vs Input Frequency

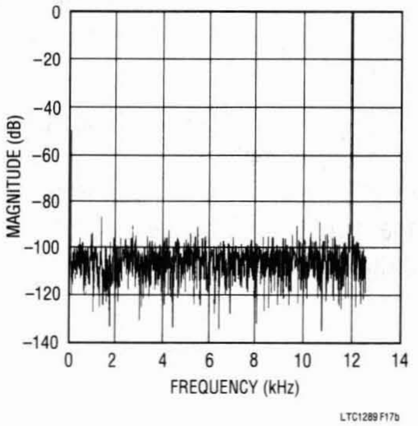


Figure 17b. f_{IN} = 12kHz, f_S = 25kHz, SNR = 72.23dB

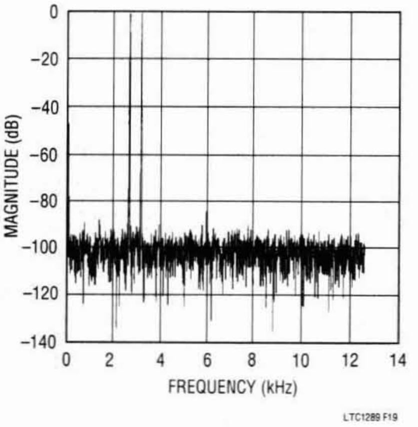


Figure 19. $f_{IN}1$ = 2.6kHz, $f_{IN}2$ = 3.1kHz, f_S = 25kHz

APPLICATIONS INFORMATION

Figure 19 shows an FFT plot of the output spectrum for two tones applied to the input of the A/D. Nonlinearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

8. Overvoltage Protection

Applying signals to the analog MUX that exceed the positive or negative supply of the device will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog MUX before power is applied to the LTC1289. Another example is the input source is operating from different supplies of larger value than the LTC1289. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. As shown in Figure 20, a 1kΩ resistor is enough to stand off ±15V (15mA for one only channel). If more than one channel exceeds the supplies than the following guidelines can be used. Limit the current to 7mA per channel and 28mA for all channels. This means four channels can handle 7mA of input current each. Reducing the ACLK and SCLK frequencies from the maximum of 2MHz and 1MHz, respectively (see Typical Peformance Characteristics curves Maximum ACLK Frequency vs Source Resistance and Sample and Hold Acquisition Time vs Source Resistance) allows the use of larger current limiting resistors. Use 1N4148 diode clamps from the MUX inputs to V_{CC} and V^- if the value of the series resistor will not allow the maximum clock speeds to be used or if an unknown source is used to drive the LTC1289 MUX inputs.

How the various power supplies to the LTC1289 are applied can also lead to overvoltage conditions. For single supply operation (i.e., unipolar mode), if V_{CC} and REF^+ are not tied together, then V_{CC} should be turned on first, then REF^+. If this sequence cannot be met, connecting a diode from REF^+ to V_{CC} is recommended (see Figure 21).

For dual supplies (bipolar mode) placing two Schottky diodes from V_{CC} and V^- to ground (Figure 22) will prevent power supply reversal from occuring when an input source is applied to the analog MUX before power is applied to the device. Power supply reversal occurs, for example, if the input is pulled below V^- then V_{CC} will pull a diode drop below ground which could cause the device not to power up properly. Likewise, if the input is pulled above V_{CC} then V^- will be pulled a diode drop above ground. If no inputs are present on the MUX, the Schottky diodes are not required if V^- is applied first, then V_{CC}.

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

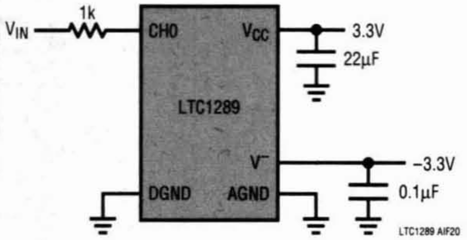


Figure 20. Overvoltage Protection for MUX

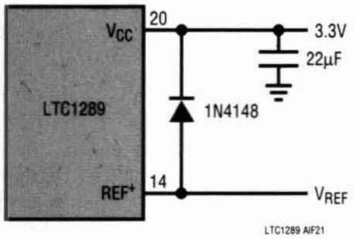


Figure 21.

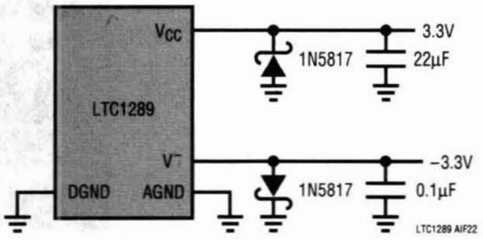


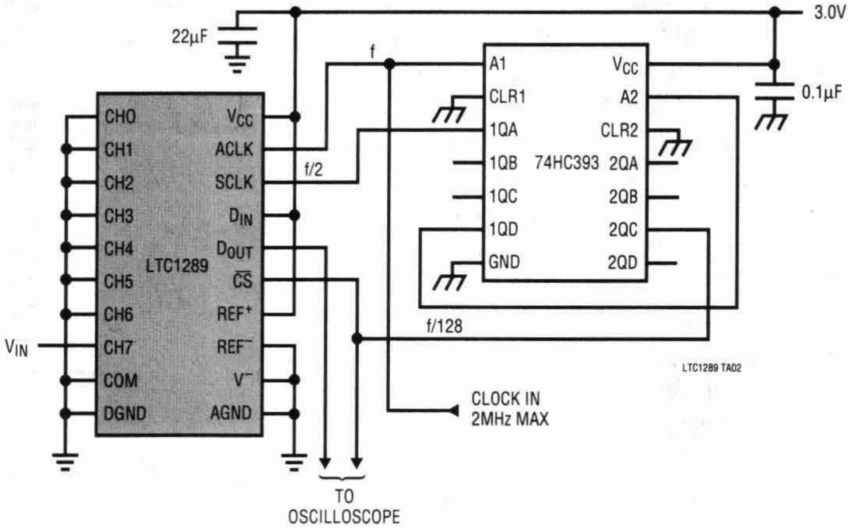
Figure 22. Power Supply Reversal

TYPICAL APPLICATIONS

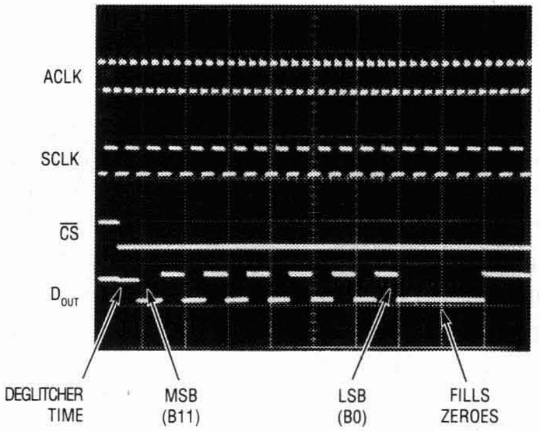
A "Quick Look" Circuit for the LTC1289

Users can get a quick look at the function and timing of the LTC1289 by using the following simple circuit. REF^+ and D_{IN} are tied to V_{CC} selecting a 3V input span, CH7 as a single-ended input, unipolar mode, MSB-first format and 16-bit word length. ACLK is driven by an external clock and SCLK is driven by one half the clock rate. $\overline{CS}$ is driven at 1/128 the clock rate by the 74HC393 and D_{OUT} outputs the data. All other pins are tied to a ground plane. The output data from the D_{OUT} pin can be viewed on an oscilloscope which is set up to trigger on the falling edge of $\overline{CS}$.

A "Quick Look" Circuit for the LTC1289


3.0V
22µF
f
0.1µF
A1
VCC
CLR1
A2
1QA
CLR2
1QB
74HC393
2QA
1QC
2QB
1QD
2QC
GND
2QD
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
LTC1289
VCC
ACLK
SCLK
DIN
DOUT
CS
REF+
REF−
V−
AGND
f/2
f/128
VIN
LTC1289 TA02
CLOCK IN
2MHz MAX
TO
OSCILLOSCOPE

Scope Trace of LTC1289 "Quick Look" Circuit Showing A/D Output of 010101010101 (555_{HEX})



VERTICAL: 5V/DIV
HORIZONTAL: 2µs/DIV

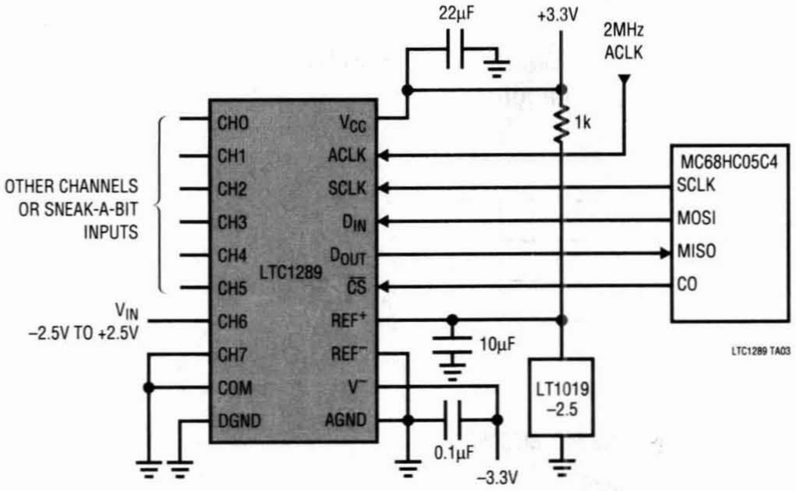
TYPICAL APPLICATIONS

SNEAK-A-BIT™

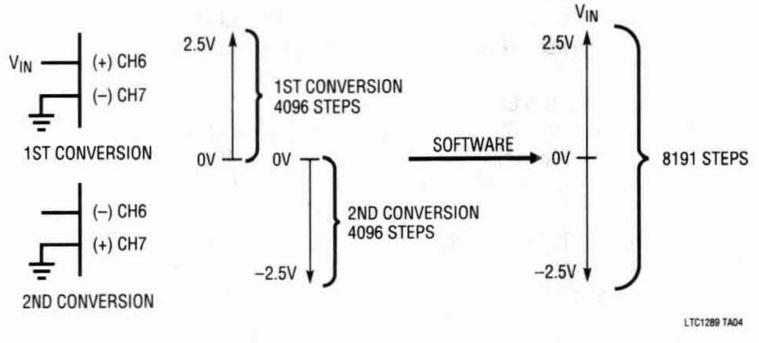
The LTC1289's unique ability to software select the polarity of the differential inputs and the output word length is used to achieve one more bit of resolution. Using the circuit below with two conversions and some software, a 2's complement 12-bit + sign word is returned to memory inside the MPU. The MC68HC05C4 was chosen as an example, however, any processor that operates at 3.3V could be used.

Two 12-bit unipolar conversions are performed: the first over a 0V to 2.5V span and the second over a 0V to −2.5V span (by reversing the polarity of the inputs). The sign of the input is determined by which of the two spans contained it. Then the resulting number (ranging from −4095 to +4095 decimal) is converted to 2's complement notation and stored in RAM.

SNEAK-A-BIT Circuit


22µF
+3.3V
2MHz
ACLK
1k
MC68HC05C4
SCLK
MOSI
MISO
CO
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
V_CC
ACLK
SCLK
D_IN
D_OUT
CS
REF+
REF−
V−
AGND
LTC1289
OTHER CHANNELS
OR SNEAK-A-BIT
INPUTS
V_IN
−2.5V TO +2.5V
10µF
LT1019
−2.5
0.1µF
−3.3V
LTC1289 TA03

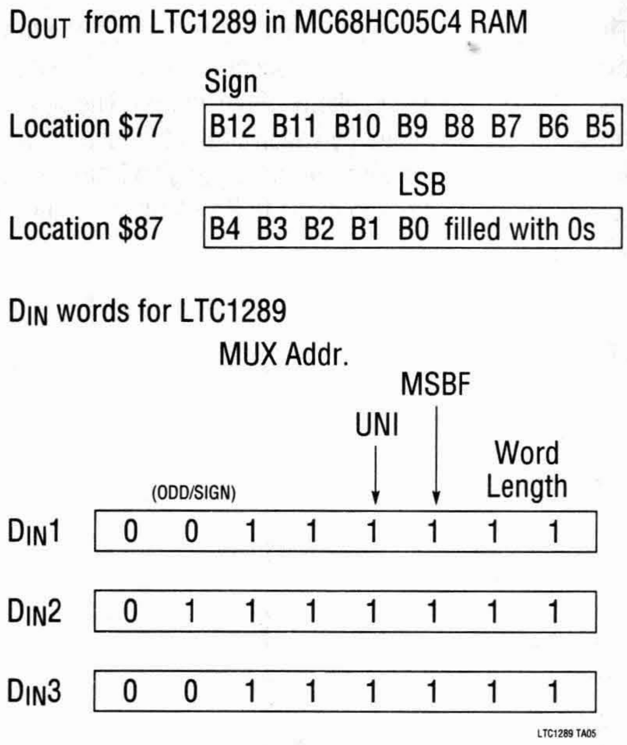
SNEAK-A-BIT


V_IN
(+) CH6
(−) CH7
1ST CONVERSION
(−) CH6
(+) CH7
2ND CONVERSION
2.5V
0V
1ST CONVERSION
4096 STEPS
0V
−2.5V
2ND CONVERSION
4096 STEPS
SOFTWARE
V_IN
2.5V
0V
−2.5V
8191 STEPS
LTC1289 TA04

SNEAK-A-BIT is a trademark of Linear Technology Corp.

TYPICAL APPLICATIONS

SNEAK-A-BIT Code



SNEAK-A-BIT Code for the LTC1289 Using the MC68HC05C4

MNEMONIC	DESCRIPTION
LDA #$50	Configuration data for SPCR
STA $0A	Load configuration data into $0A
LDA #$FF	Configuration data for port C DDR
STA $06	Load configuration data into port C DDR
BSET 0, $02	Make sure $\overline{CS}$ is high
JSR READ −/+	Dummy read configures LTC1289 for next read
JSR READ +/−	Read CH6 with respect to CH7
JSR READ −/+	Read CH7 with respect to CH6
JSR CHK SIGN	Determines which reading has valid data, converts to 2's complement and stores in RAM
READ −/+: LDA #$3F	Load D_{IN} word for LTC1289 into ACC
JSR TRANSFER	Read LTC1289 routine
LDA $60	Load MSBs from LTC1289 in ACC
STA $71	Store MSBs in $71
LDA $61	Load LSBs from LTC1289 in ACC
STA $72	Store LSBs in $72
RTS	Return
READ +/−: LDA #$7F	Load D_{IN} word for LTC1289 into ACC
JSR TRANSFER	Read LTC1289 routine
LDA $60	Load MSBs from LTC1289 into ACC
STA $73	Store MSBs in $73
LDA $61	Load LSBs from LTC1289 into ACC
STA $74	Store LSBs in $74
RTS	Return
TRANSFER: BCLR 0, $02	$\overline{CS}$ goes low
STA $0C	Load D_{IN} into SPI. Start transfer
LOOP 1: TST $0B	Test status of SPIF
BPL LOOP 1	Loop to previous instruction if not done
LDA $0C	Load contents of SPI data reg into ACC
STA $0C	Start next cycle
STA $60	Store MSBs in $60
LOOP 2: TST $0B	Test status of SPIF
BPL LOOP 2	Loop to previous instruction if not done
BSET 0, $02	$\overline{CS}$ goes high
LDA $0C	Load contents of SPI data reg into ACC
STA $61	Store LSBs in $61
RTS	Return
CHK SIGN: LDA $73	Load MSBs of +/− read into ACC
ORA $74	Or ACC (MSBs) with LSBs of +/− read
BEQ MINUS	If result is 0 goto minus
CLC	Clear carry
ROR $73	Rotate right $73 through carry
ROR $74	Rotate right $74 through carry
LDA $73	Load MSBs of +/− read into ACC
STA $77	Store MSBs in RAM locations $77
LDA $74	Load LSBs of +/− read into ACC
STA $87	Store LSBs in RAM location $87
BRA END	Goto end of routine
MINUS: CLC	Clear carry
ROR $71	Shift MSBs of −/+ read right
ROR $72	Shift LSBs of −/+ read right
COM $71	1's complement of MSBs
COM $72	1's complement of LSBs
LDA $72	Load LSBs into ACC
ADD #$01	Add 1 to LSBs
STA $72	Store ACC in $72
CLRA	Clear ACC
ADC $71	Add with carry to MSBs. Result in ACC
STA $71	Store ACC in $71
STA $77	Store MSBs in RAM locations $77
LDA $72	Load LSBs in ACC
STA $87	Store LSBs in RAM location $87
END: RTS	Return

TYPICAL APPLICATIONS

Power Shutdown

For battery-powered applications it is desirable to keep power dissipation at a minimum. The LTC1289 can be powered down when not in use reducing the supply current from a nominal value of 1mA to typically 1μA (with ACLK turned off). See the Curve for Supply Current (Power Shutdown) vs ACLK if ACLK cannot be turned off when the LTC1289 is powered down. In this case the supply current is proportional to the ACLK frequency and is independent of temperature until it reaches the magnitude of the supply current attained with ACLK turned off.

As an example of how to use this feature let's add this to the previous application, SNEAK-A-BIT. After the CHK SIGN subroutine call insert the following:

```
                •
                •
JSR CHK SIGN    Determines which reading has valid
                data, converts to 2's complement
                and stores in RAM
JSR SHUTDOWN    LTC1289 power shutdown routine
```

The actual subroutine is:

```
SHUTDOWN:  LDA  #$3D       Load DIN word for
                           LTC1289 into ACC
           JSR TRANSFER    Read LTC1289 routine
           RTS             Return
```

To place the device in power shutdown the word length bits are set to WL1 = 0 and WL0 = 1. The LTC1289 is powered up on the next request for conversion and it's ready to digitize an input signal immediately.

Power Shutdown Timing Considerations

After power shutdown has been requested, the LTC1289 is powered up on the next request for a conversion. This request can be initiated either by bringing $\overline{CS}$ low or by starting the next cycle of SCLKs if $\overline{CS}$ is kept low (see Figures 3 and 4). When the SCLK frequency is much slower than the ACLK frequency a situation can arise where the LTC1289 could power down and then prematurely power back up. Power shutdown begins at the negative going edge of the 10th SCLK once it has been requested. A dummy conversion is executed and the LTC1289 waits for the next request for conversion. If the SCLKs have not finished once the LTC1289 has finished its dummy conversion, it will recognize the next remaining SCLKs as a request to start a conversion and power up the LTC1289 (see Figure 23). To prevent this, bring either $\overline{CS}$ high at the 19th SCLK (Figure 24) or clock out only 10 SCLKs (Figure 25) when power shutdown is requested.

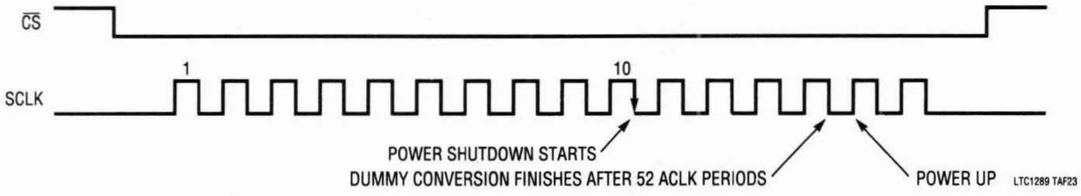


Figure 23. Power Shutdown Timing Problem

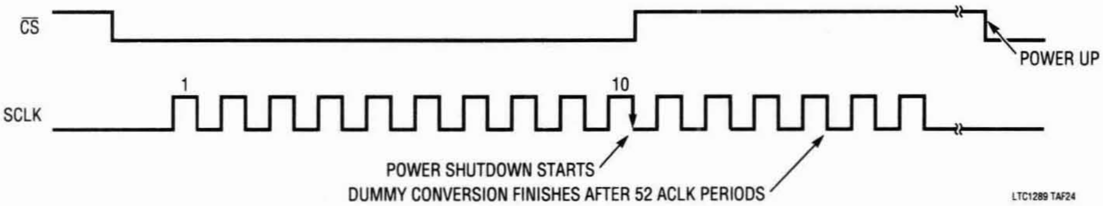


Figure 24. Power Shutdown Timing

TYPICAL APPLICATIONS

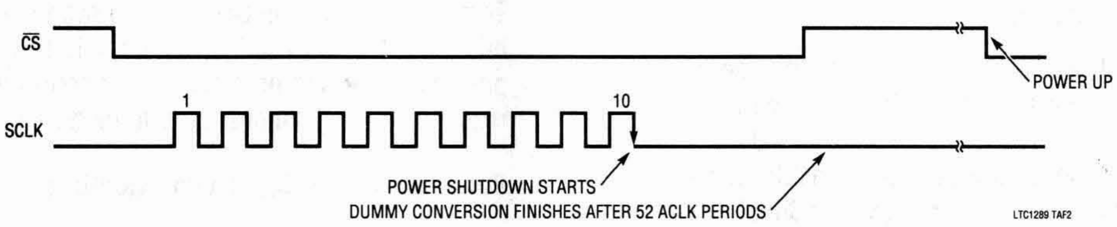

$\overline{CS}$
POWER UP
SCLK
1
10
POWER SHUTDOWN STARTS
DUMMY CONVERSION FINISHES AFTER 52 ACLK PERIODS
LTC1289 TAF2

Figure 25. Power Shutdown Timing

LTC1290

Single Chip 12-Bit Data Acquisition System

FEATURES

- Software Programmable Features
  - -Unipolar/Bipolar Conversion
  - -4 Differential/8 Single Ended Inputs
  - -MSB or LSB First Data Sequence
  - -Variable Data Word Length
  - -Power Shutdown
- Built-In Sample and Hold
- Single Supply 5V or ± 5V Operation
- Direct 4 Wire Interface to Most MPU Serial Ports and all MPU Parallel Ports
- 50kHz Maximum Throughput Rate

KEY SPECIFICATIONS

■ Resolution	12 Bits
■ Fast Conversion Time	13μs Max. Over Temp.
■ Low Supply Current	6.0mA

LTCMOS is a trademark of Linear Technology Corporation.

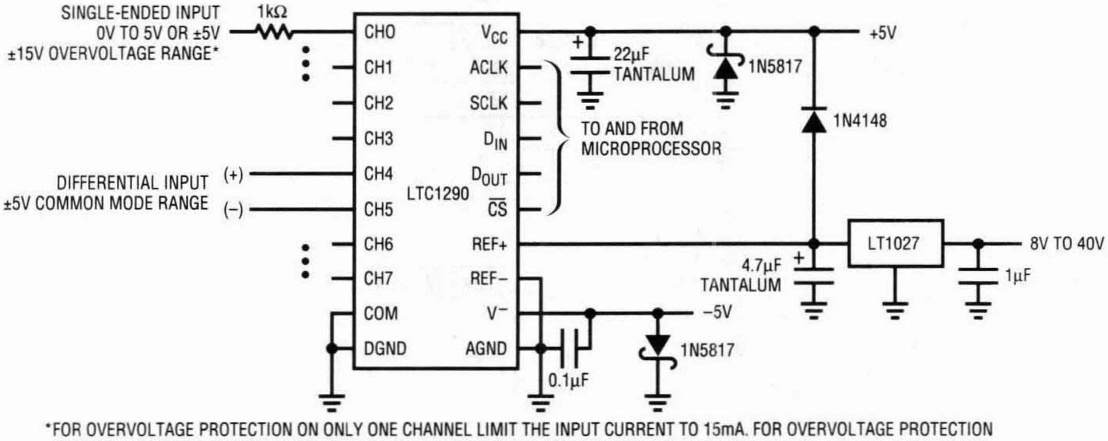
DESCRIPTION

The LTC1290 is a data acquisition component which contains a serial I/O successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform either 12-bit unipolar, or 11-bit plus sign bipolar A/D conversions. The 8-channel input multiplexer can be configured for either single ended or differential inputs (or combinations thereof). An on-chip sample and hold is included for all single ended input channels. When the LTC1290 is idle it can be powered down with a serial word in applications where low power consumption is desired.

The serial I/O is designed to be compatible with industry standard full duplex serial interfaces. It allows either MSB or LSB first data and automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8, 12 or 16-bits. This allows easy interface to shift registers and a variety of processors.

TYPICAL APPLICATION

12-Bit 8-Channel Sampling Data Acquisition System


SINGLE-ENDED INPUT
0V TO 5V OR ±5V
±15V OVERVOLTAGE RANGE*
1kΩ
DIFFERENTIAL INPUT
±5V COMMON MODE RANGE
(+)
(–)
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
LTC1290
V_{CC}
ACLK
SCLK
D_{IN}
D_{OUT}
CS
REF+
REF–
V–
AGND
22μF
TANTALUM
1N5817
+5V
1N4148
TO AND FROM
MICROPROCESSOR
LT1027
8V TO 40V
1μF
4.7μF
TANTALUM
–5V
1N5817
0.1μF

*FOR OVERVOLTAGE PROTECTION ON ONLY ONE CHANNEL LIMIT THE INPUT CURRENT TO 15mA. FOR OVERVOLTAGE PROTECTION ON MORE THAN ONE CHANNEL LIMIT THE INPUT CURRENT TO 7mA PER CHANNEL AND 28mA FOR ALL CHANNELS. (SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION.) CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED OR ANY OTHER CHANNEL IS OVERVOLTAGED ($V_{IN} < V^-$ OR $V_{IN} > V_{CC}$).

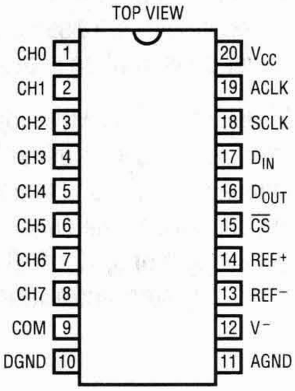
LTC1290 • TA07

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND or V^- 12V
Negative Supply Voltage (V^-) .... – 6V to GND
Voltage
  Analog and Reference Inputs .. (V^-) – 0.3V to V_{CC} + 0.3V
  Digital Inputs .... – 0.3V to 12V
  Digital Outputs .... – 0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1290BC, LTC1290CC, LTC1290DC ...... 0°C to 70°C
  LTC1290BI, LTC1290CI, LTC1290DI ...... – 40°C to 85°C
  LTC1290BM, LTC1290CM, LTC1290DM . – 55°C to 125°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION


TOP VIEW
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
DGND 10
20 V_{CC}
19 ACLK
18 SCLK
17 D_{IN}
16 D_{OUT}
15 $\overline{CS}$
14 REF+
13 REF–
12 V–
11 AGND

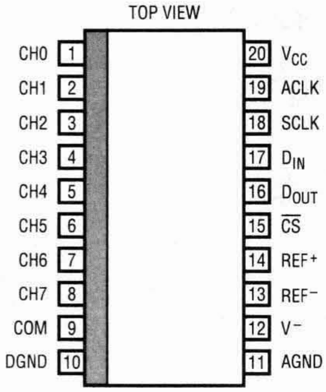
J PACKAGE
20-LEAD CERAMIC DIP

N PACKAGE
20-LEAD PLASTIC DIP

LTC1290 • POI02

ORDER PART NUMBER

LTC1290BMJ
LTC1290CMJ
LTC1290DMJ
LTC1290BIJ
LTC1290CIJ
LTC1290DIJ
LTC1290BIN
LTC1290CIN
LTC1290DIN
LTC1290BCN
LTC1290CCN
LTC1290DCN


TOP VIEW
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
DGND 10
20 V_{CC}
19 ACLK
18 SCLK
17 D_{IN}
16 D_{OUT}
15 $\overline{CS}$
14 REF+
13 REF–
12 V–
11 AGND

S PACKAGE
20-LEAD PLASTIC SOL

LTC1290 • POI01

ORDER PART NUMBER

LTC1290BCS
LTC1290CCS
LTC1290DCS

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1290B MIN	LTC1290B TYP	LTC1290B MAX	LTC1290C MIN	LTC1290C TYP	LTC1290C MAX	LTC1290D MIN	LTC1290D TYP	LTC1290D MAX	UNITS
Offset Error	(Note 4)	●			± 1.5			± 1.5			± 1.5	LSB
Linearity Error (INL)	(Notes 4 and 5)	●			± 0.5			± 0.5			± 0.75	LSB
Gain Error	(Note 4)	●			± 0.5			± 1.0			± 4.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed		●			12			12			12	Bits
Analog and REF Input Range	(Note 7)		(V^-) – 0.05V to V_{CC} + 0.05V			(V^-) – 0.05V to V_{CC} + 0.05V			(V^-) – 0.05V to V_{CC} + 0.05V			V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			± 1			± 1			± 1	μA
	On Channel = 0V Off Channel = 5V	●			± 1			± 1			± 1	μA
Off Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			± 1			± 1			± 1	μA
	On Channel = 0V Off Channel = 5V	●			± 1			± 1			± 1	μA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS			LTC1290B LTC1290C LTC1290D MIN	TYP	MAX	UNITS
f_{SCLK}	Shift Clock Frequency	$V_{CC} = 5V$ (Note 6)			0		2.0	MHz
f_{ACLK}	A/D Clock Frequency	$V_{CC} = 5V$ (Note 6)			(Note 10)		4.0	MHz
t_{ACC}	Delay Time from $\overline{CS}$ ↓ to D_{OUT} Data Valid	(Note 9)				2		ACLK Cycles
t_{SMPL}	Analog Input Sample Time	See Operating Sequence				7		SCLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence				52		ACLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)			12 SCLK + 56 ACLK			Cycles
t_{dDO}	Delay Time, SCLK ↓ to D_{OUT} Data Valid	See Test Circuits	LTC1290BC, LTC1290CC, LTC1290DC, LTC1290BI, LTC1290CI, LTC1290DI	●		130	220	ns
			LTC1290BM, LTC1290CM, LTC1290DM	●		180	270	ns
t_{dis}	Delay Time, $\overline{CS}$ ↑ to D_{OUT} Hi-Z	See Test Circuits		●		70	100	ns
t_{en}	Delay Time, 2nd ACLK ↓ to D_{OUT} Enabled	See Test Circuits		●		130	200	ns
t_{hCS}	Hold Time, $\overline{CS}$ After Last SCLK ↓	$V_{CC} = 5V$ (Note 6)			0			ns
t_{hDI}	Hold Time, D_{IN} After SCLK ↑	$V_{CC} = 5V$ (Note 6)			50			ns
t_{hDO}	Time Output Data Remains Valid After SCLK ↓					50		ns
t_f	D_{OUT} Fall Time	See Test Circuits		●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits		●		25	50	ns
t_{suDI}	Setup Time, D_{IN} Stable Before SCLK ↑	$V_{CC} = 5V$ (Note 6)			50			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$ ↓ Before Clocking in First Address Bit	(Note 6 and 9)			2 ACLK Cycles + 100ns			
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	$V_{CC} = 5V$ (Note 6)			52			ACLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel Off Channel				100 5		pF pF
		Digital Inputs				5		pF

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, AGND, and REF^- wired together (unless otherwise noted).

Note 3: $V_{CC} = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, $V^- = 0V$ for unipolar mode and $-5V$ for bipolar mode, ACLK = 4.0MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals $T_A = 25°C$.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 4096. For example, when $V_{REF} = 5V$, 1LSB (bipolar) = 2(5V)/4096 = 2.44mV.

Note 5: Integral non-linearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

Note 8: Channel leakage current is measured after the channel selection.

Note 9: To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edge after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select setup time has elapsed.

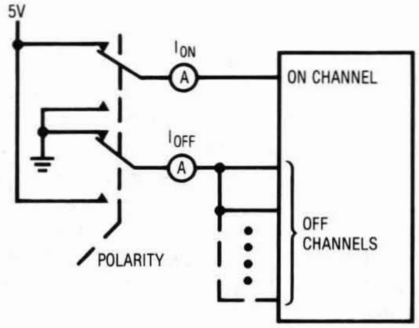
Note 10: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it's recommended that $f_{ACLK} \geq 500kHz$ at 125°C, $f_{ACLK} \geq 125kHz$ at 85°C, and $f_{ACLK} \geq 15kHz$ at 25°C.

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

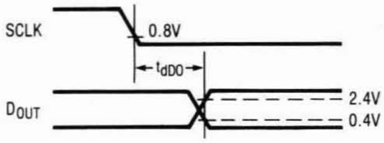
					LTC1290B LTC1290C LTC1290D		
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10µA			4.7		V
		I_O = 360µA	●	2.4	4.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High	●			3	µA
		V_{OUT} = 0V, $\overline{CS}$ High	●			−3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−20		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			20		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High	●		6	12	mA
		$\overline{CS}$ High, Power Shutdown, ACLK off: LTC1290BC, LTC1290CC, LTC1290DC, LTC1290BI, LTC1290CI, LTC1290DI	●		5	10	µA
		LTC1290BM, LTC1290CM, LTC1290DM	●		5	15	µA
I_{REF}	Reference Current	V_{REF} = 5V	●		10	50	µA
I^-	Negative Supply Current	$\overline{CS}$ High	●		1	50	µA

TEST CIRCUITS

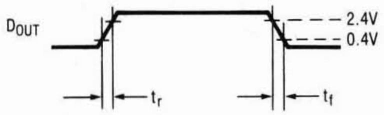
On and Off Channel Leakage Current


5V
I_{ON}
A
ON CHANNEL
I_{OFF}
A
OFF CHANNELS
POLARITY

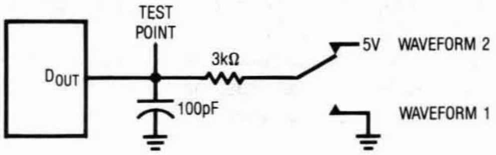
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}


SCLK
0.8V
t_{dDO}
D_{OUT}
2.4V
0.4V

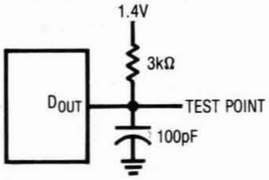
Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f


D_{OUT}
2.4V
0.4V
t_r
t_f

Load Circuit for t_{dis} and t_{en}

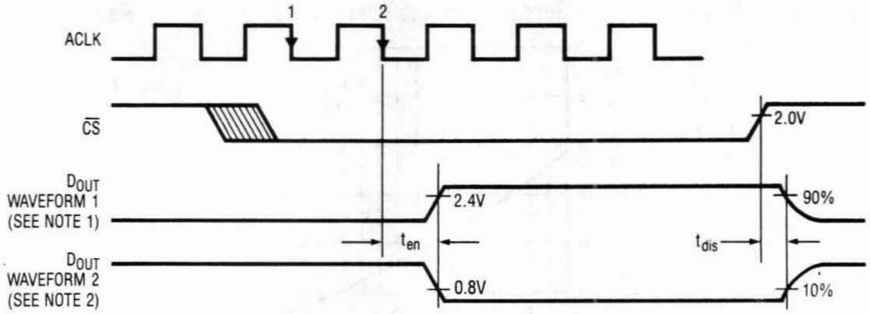

TEST POINT
D_{OUT}
3kΩ
5V
WAVEFORM 2
100pF
WAVEFORM 1

Load Circuit for t_{dDO}, t_r, and t_f


1.4V
3kΩ
D_{OUT}
TEST POINT
100pF

TEST CIRCUITS

Voltage Waveforms for t_{en} and t_{dis}


ACLK
1
2
$\overline{CS}$
2.0V
D_{OUT} WAVEFORM 1 (SEE NOTE 1)
2.4V
90%
t_{en}
t_{dis}
D_{OUT} WAVEFORM 2 (SEE NOTE 2)
0.8V
10%

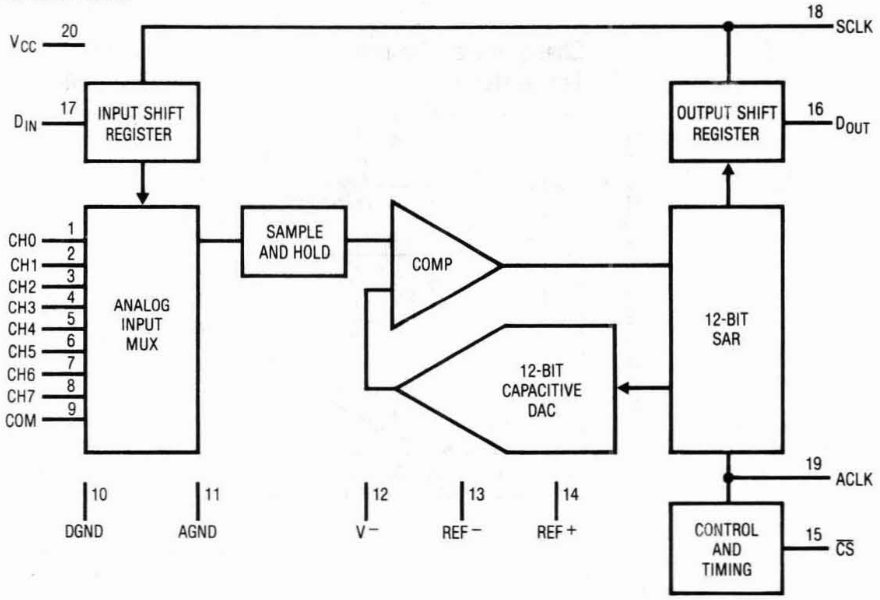
NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

PIN FUNCTIONS

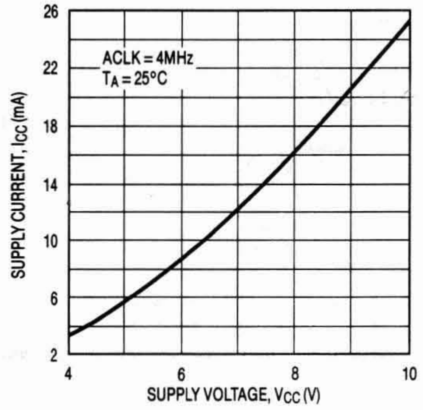
#	PIN	FUNCTION	DESCRIPTION
1-8	CH0-CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
12	V^-	Negative Supply	Tie V^- to most negative potential in the circuit. (Ground in single supply applications.)
13, 14	REF^-, REF^+	Reference Inputs	The reference inputs must be kept free of noise with respect to AGND.
15	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
18	SCLK	Shift Clock	This clock synchronizes the serial data transfer.
19	ACLK	A/D Conversion Clock	This clock controls the A/D conversion process.
20	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

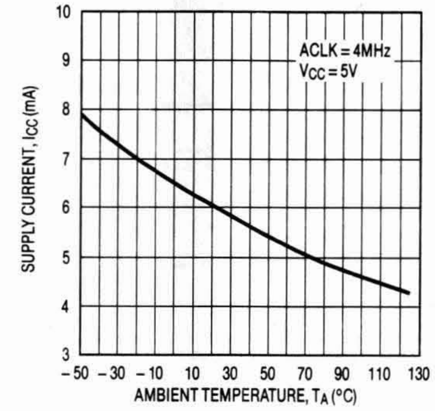

V_{CC}
20
18
SCLK
D_{IN}
17
INPUT SHIFT REGISTER
OUTPUT SHIFT REGISTER
16
D_{OUT}
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
1
2
3
4
5
6
7
8
9
ANALOG INPUT MUX
SAMPLE AND HOLD
COMP
12-BIT CAPACITIVE DAC
12-BIT SAR
19
ACLK
10
DGND
11
AGND
12
V−
13
REF−
14
REF+
CONTROL AND TIMING
15
$\overline{CS}$

TYPICAL PERFORMANCE CHARACTERISTICS

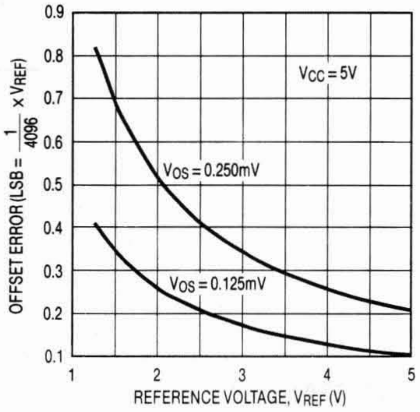
Supply Current vs Supply Voltage



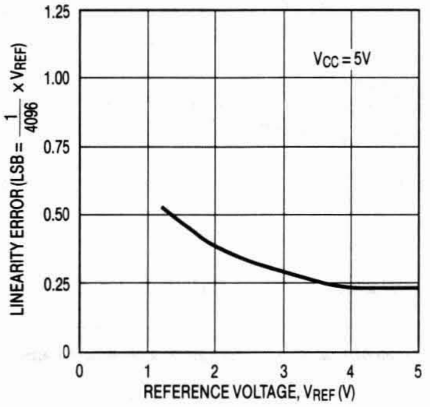
Supply Current vs Temperature



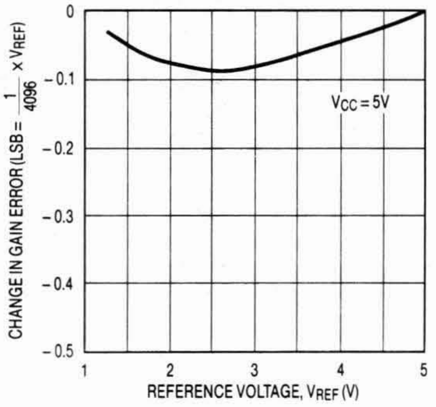
Unadjusted Offset Voltage vs Reference Voltage



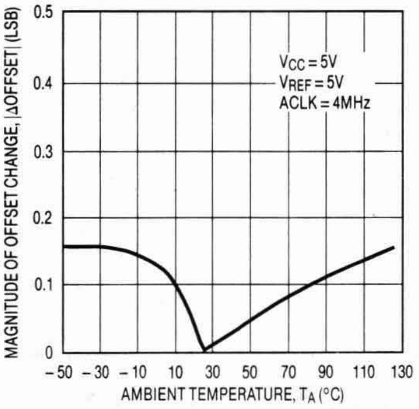
Change in Linearity vs Reference Voltage



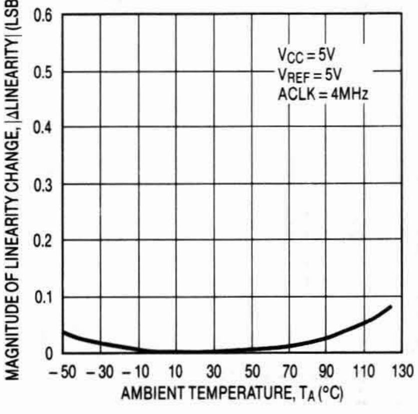
Change in Gain Error vs Reference Voltage



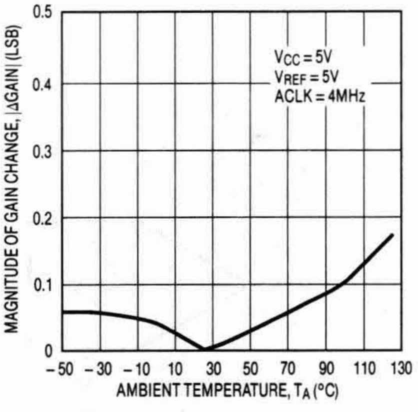
Change in Offset Error vs Temperature



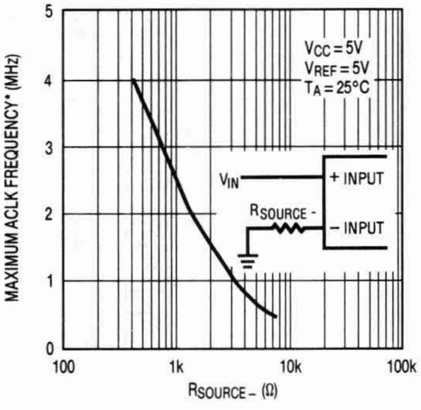
Change in Linearity Error vs Temperature



Change in Gain Error vs Temperature



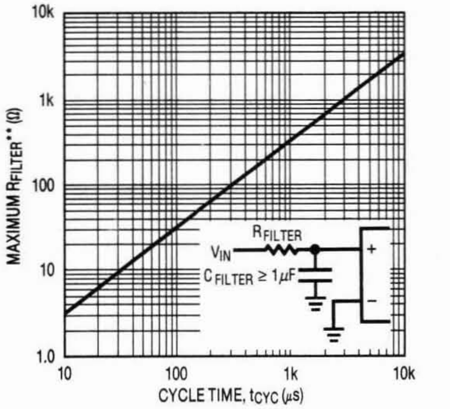
Maximum ACLK Frequency vs Source Resistance



*MAXIMUM ACLK FREQUENCY REPRESENTS THE ACLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 4MHz VALUE IS FIRST DETECTED.

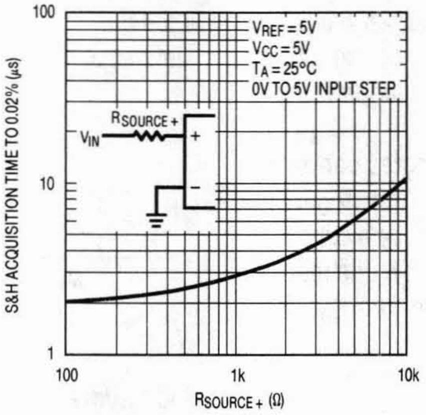
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Filter Resistor vs Cycle Time

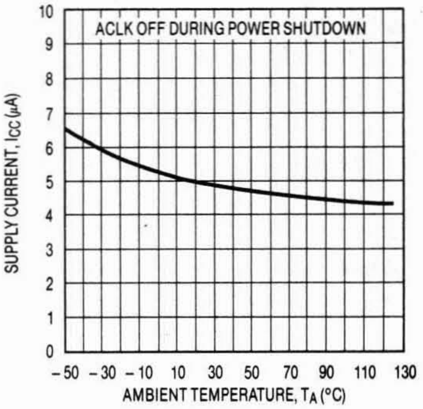


**MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0 IS FIRST DETECTED.

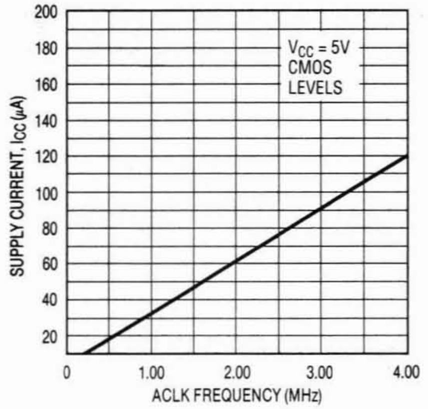
Sample and Hold Acquisition Time vs Source Resistance



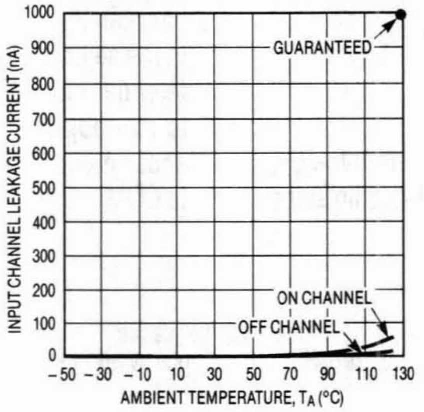
Supply Current (Power Shutdown) vs Temperature



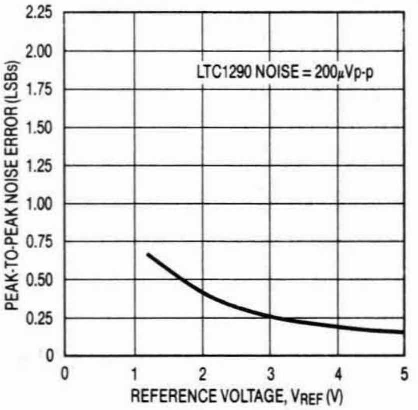
Supply Current (Power Shutdown) vs ACLK



Input Channel Leakage Current vs Temperature



Noise Error vs Reference Voltage



APPLICATIONS INFORMATION

The LTC1290 is a data acquisition component which contains the following functional blocks:

1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, full duplex serial interface
5. Control and timing logic

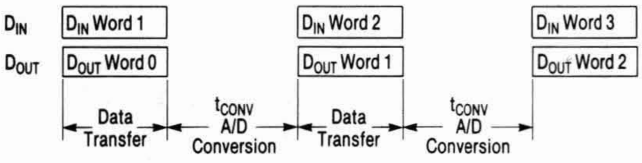
DIGITAL CONSIDERATIONS

Serial Interface

The LTC1290 communicates with microprocessors and other external circuitry via a synchronous, full duplex, four wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

APPLICATIONS INFORMATION

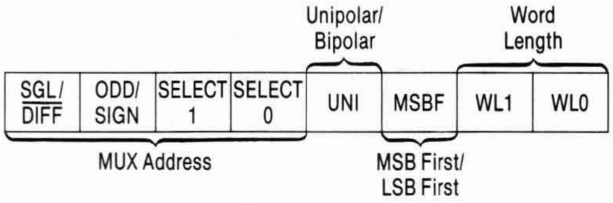
Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After the falling $\overline{CS}$ is recognized, an 8-bit input word is shifted into the D_{IN} input which configures the LTC1290 for the next conversion. Simultaneously, the result of the previous conversion is output on the D_{OUT} line. At the end of the data exchange the requested conversion begins and $\overline{CS}$ should be brought high. After t_{CONV}, the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one $\overline{CS}$ cycle from the input word requesting it.



D_{IN}
D_{OUT}
D_{IN} Word 1
D_{OUT} Word 0
D_{IN} Word 2
D_{OUT} Word 1
D_{IN} Word 3
D_{OUT} Word 2
Data Transfer
t_{CONV} A/D Conversion
Data Transfer
t_{CONV} A/D Conversion

Input Data Word

The LTC1290 eight bit data word is clocked into the D_{IN} input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The eight bits of the input word are defined as follows:

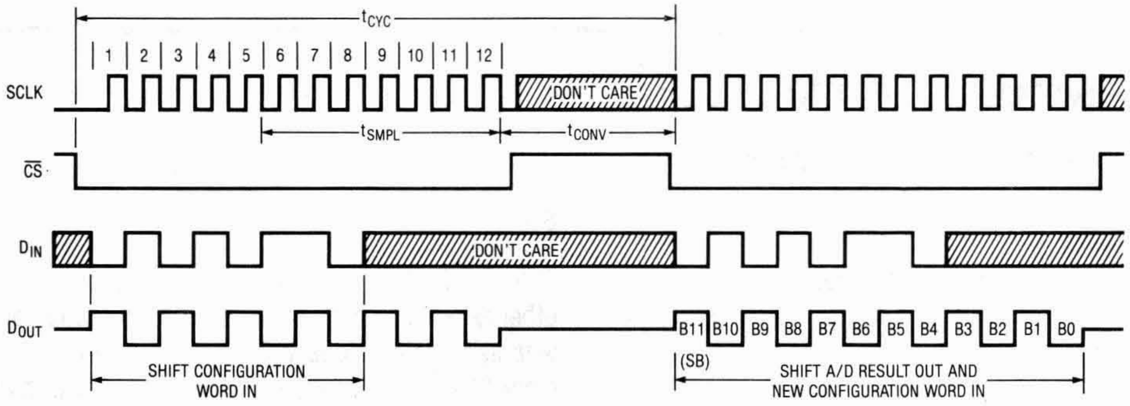


Unipolar/ Bipolar
Word Length
SGL/ DIFF
ODD/ SIGN
SELECT 1
SELECT 0
UNI
MSBF
WL1
WL0
MUX Address
MSB First/ LSB First

MUX Address

The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and − signs in the selected row of the following table. Note that in differential mode (SGL/$\overline{DIFF}$ = 0) measurements are limited to four adjacent input pairs with either polarity. In single ended mode, all input channels are measured with respect to COM.

Operating Sequence
(Example: Differential Inputs (CH3-CH2), Bipolar, MSB First and 12-Bit Word Length)



t_{CYC}
1
2
3
4
5
6
7
8
9
10
11
12
SCLK
DON'T CARE
t_{SMPL}
t_{CONV}
CS
D_{IN}
DON'T CARE
D_{OUT}
B11
B10
B9
B8
B7
B6
B5
B4
B3
B2
B1
B0
(SB)
SHIFT CONFIGURATION WORD IN
SHIFT A/D RESULT OUT AND NEW CONFIGURATION WORD IN

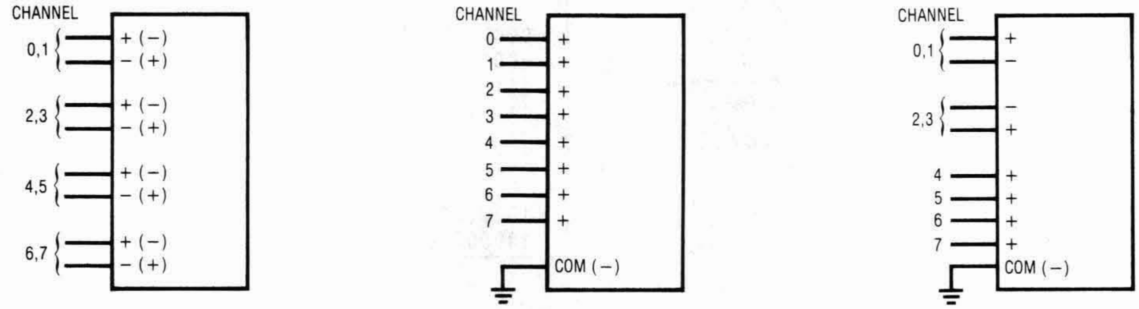
APPLICATIONS INFORMATION

Table 1. Multiplexer Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION							
SGL/$\overline{\text{DIFF}}$	ODD/ SIGN	SELECT 1	0	0	1	2	3	4	5	6	7
0	0	0	0	+	−						
0	0	0	1			+	−				
0	0	1	0					+	−		
0	0	1	1							+	−
0	1	0	0	−	+						
0	1	0	1			−	+				
0	1	1	0					−	+		
0	1	1	1							−	+

MUX ADDRESS				SINGLE ENDED CHANNEL SELECTION								
SGL/$\overline{\text{DIFF}}$	ODD/ SIGN	SELECT 1	0	0	1	2	3	4	5	6	7	COM
1	0	0	0	+								−
1	0	0	1			+						−
1	0	1	0					+				−
1	0	1	1							+		−
1	1	0	0		+							−
1	1	0	1				+					−
1	1	1	0						+			−
1	1	1	1								+	−

4 Differential **8 Single Ended** **Combinations of Differential and Single Ended**


CHANNEL
0,1
+ (−)
− (+)
2,3
+ (−)
− (+)
4,5
+ (−)
− (+)
6,7
+ (−)
− (+)
CHANNEL
0
1
2
3
4
5
6
7
+
+
+
+
+
+
+
+
COM (−)
CHANNEL
0,1
+
−
2,3
−
+
4
5
6
7
+
+
+
+
COM (−)

Changing the MUX Assignment "On the Fly"

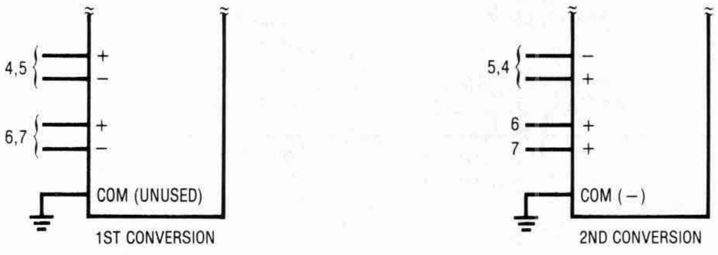

4,5
+
−
6,7
+
−
COM (UNUSED)
1ST CONVERSION
5,4
−
+
6
7
+
+
COM (−)
2ND CONVERSION

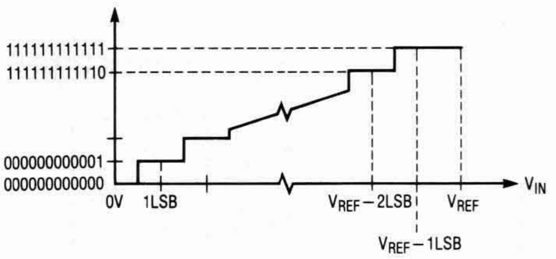
Figure 1. Examples of Multiplexer Options on the LTC1290

APPLICATIONS INFORMATION

Unipolar/Bipolar (UNI)

The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

Unipolar Transfer Curve (UNI = 1)



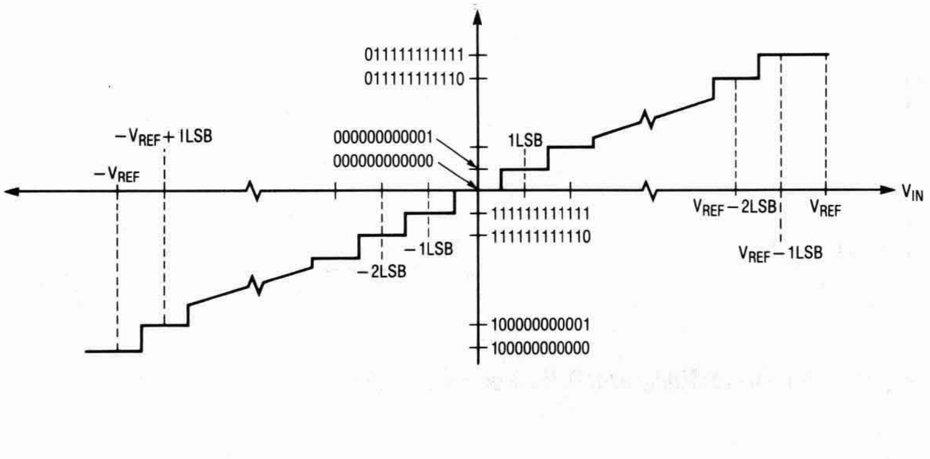
Unipolar Output Code (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
111111111111	V_{REF} − 1LSB	4.9988V
111111111110	V_{REF} − 2LSB	4.9976V
•	•	•
•	•	•
•	•	•
000000000001	1LSB	0.0012V
000000000000	0V	0V

Bipolar Output Code (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
011111111111	V_{REF} − 1LSB	4.9976V
011111111110	V_{REF} − 2LSB	4.9851V
•	•	•
•	•	•
•	•	•
000000000001	1LSB	0.0024V
000000000000	0V	0V
111111111111	− 1LSB	− 0.0024V
111111111110	− 2LSB	− 0.0048V
•	•	•
•	•	•
•	•	•
100000000001	− (V_{REF}) + 1LSB	− 4.9976V
100000000000	− (V_{REF})	− 5.0000V

Bipolar Transfer Curve (UNI = 0)



APPLICATIONS INFORMATION

MSB First/LSB First Format (MSBF)

The output data of the LTC1290 is programmed for MSB first or LSB first sequence using the MSBF bit. For MSBF first output data the input word clocked to the LTC1290 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB first output data the input word clocked to the LTC1290 should always contain a zero in the MSBF bit location. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

MSBF	OUTPUT FORMAT
0	LSB First
1	MSB First

Word Length (WL1, WL0) and Power Shutdown

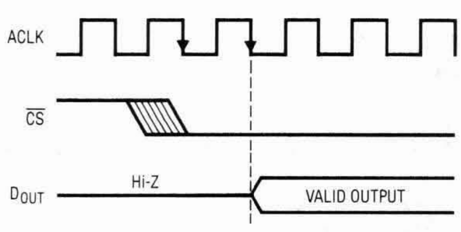
The last two bits of the input word (WL1 and WL0) program the output data word length and the power shutdown feature of the LTC1290. Word lengths of 8, 12 or 16-bits can be selected according to the following table. The WL1 and WL0 bits in a given D_{IN} word control the length of the present, not the next, D_{OUT} word. WL1 and WL0 are never "don't cares" and must be set for the correct D_{OUT} word length even when a "dummy" D_{IN} word is sent. On any transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU. Power down will occur when WL1 = 0 and WL0 = 1 is selected. The previous conversion result will be clocked out as a 10-bit word so a "dummy" conversion is required before powering down the LTC1290. Conversions are resumed once $\overline{CS}$ goes low or an SCLK is applied, if $\overline{CS}$ is already low.

WL1	WL0	OUTPUT WORD LENGTH
0	0	8-Bits
0	1	Power Shutdown
1	0	12-Bits
1	1	16-Bits

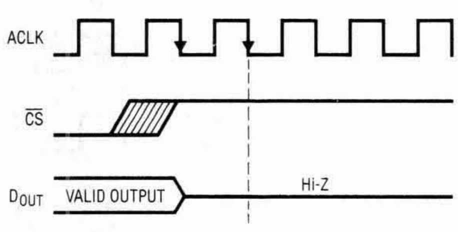
Deglitcher

A deglitching circuit has been added to the Chip Select input of the LTC1290 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the $\overline{CS}$ input that are shorter in duration than one ACLK cycle. After a change of state on the $\overline{CS}$ input, the LTC1290 waits for two falling edge of the ACLK before recognizing a valid chip select. One indication of $\overline{CS}$ recognition is the D_{OUT} line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling $\overline{CS}$ edges.

Low $\overline{CS}$ Recognized Internally

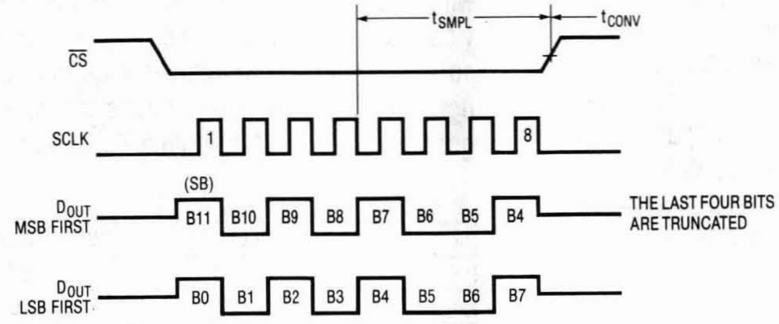


High $\overline{CS}$ Recognized Internally

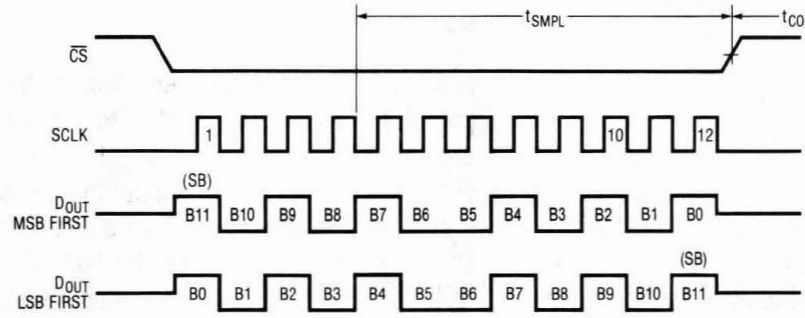


APPLICATIONS INFORMATION

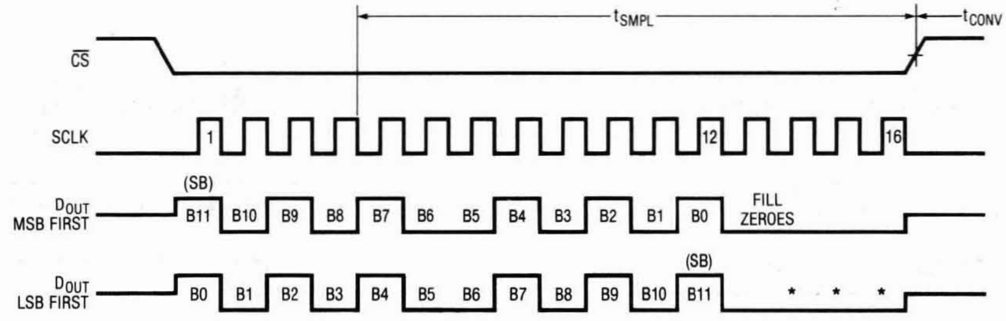
8-Bit Word Length


CS
SCLK
D_OUT MSB FIRST
D_OUT LSB FIRST
t_SMPL
t_CONV
1
8
(SB)
B11 B10 B9 B8 B7 B6 B5 B4
B0 B1 B2 B3 B4 B5 B6 B7
THE LAST FOUR BITS ARE TRUNCATED

12-Bit Word Length


CS
SCLK
D_OUT MSB FIRST
D_OUT LSB FIRST
t_SMPL
t_CONV
1
10
12
(SB)
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
(SB)
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11

16-Bit Word Length


CS
SCLK
D_OUT MSB FIRST
D_OUT LSB FIRST
t_SMPL
t_CONV
1
12
16
(SB)
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
FILL ZEROES
(SB)
B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11
* * *

*IN UNIPOLAR MODE, THESE BITS ARE FILLED WITH ZEROES.
IN BIPOLAR MODE, THE SIGN BIT IS EXTENDED INTO THESE LOCATIONS.

Figure 2. Data Output (D_{OUT}) Timing with Different Word Lengths

APPLICATIONS INFORMATION

$\overline{CS}$ Low During Conversion

In the normal mode of operation, $\overline{CS}$ is brought high during the conversion time. The serial port ignores any SCLK activity while $\overline{CS}$ is high. The LTC1290 will also operate with $\overline{CS}$ low during the conversion. In this mode, SCLK must remain low during the conversion as shown in the following figure. After the conversion is complete, the D_{OUT} line will become active with the first output bit. Then the data transfer can begin as normal.

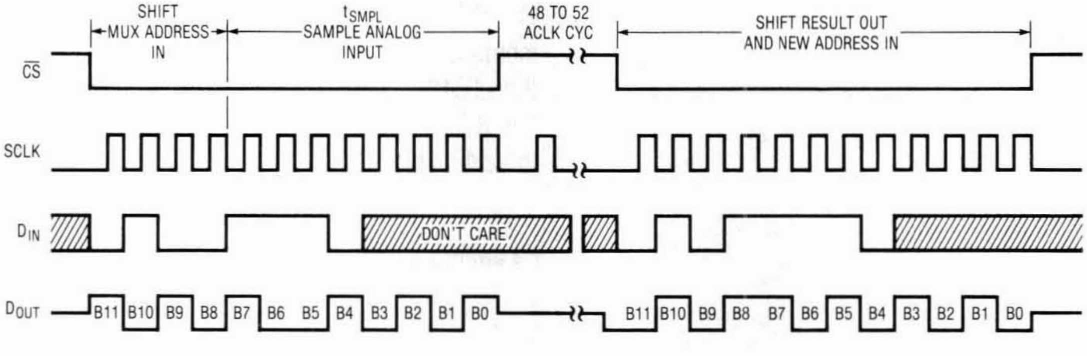

SHIFT MUX ADDRESS IN
tSMPL SAMPLE ANALOG INPUT
48 TO 52 ACLK CYC
SHIFT RESULT OUT AND NEW ADDRESS IN
CS
SCLK
DIN
DON'T CARE
DOUT
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0

Figure 3. $\overline{CS}$ High During Conversion

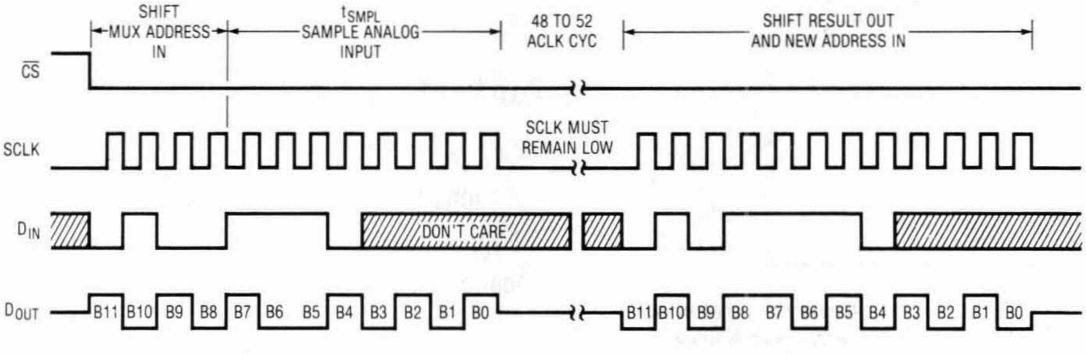

SHIFT MUX ADDRESS IN
tSMPL SAMPLE ANALOG INPUT
48 TO 52 ACLK CYC
SHIFT RESULT OUT AND NEW ADDRESS IN
CS
SCLK
SCLK MUST REMAIN LOW
DIN
DON'T CARE
DOUT
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0

Figure 4. $\overline{CS}$ Low During Conversion

APPLICATIONS INFORMATION

Microprocessor Interfaces

The LTC1290 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 2). If an MPU without a serial interface is used, then 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1290. Included here are two serial interface examples and one example showing a parallel port programmed to form the serial interface.

Table 2. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1290**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

*Requires external hardware

**Contact factory for interface information for processors not on this list

†MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

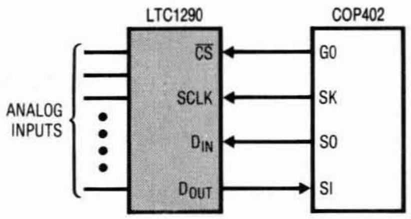
Serial Port Microprocessors

Most synchronous serial formats contain a shift clock (SCLK) and two data lines, one for transmitting and one for receiving. In most cases data bits are transmitted on the falling edge of the clock (SCLK) and captured on the rising edge. However, serial port formats vary among MPU manufacturers as to the smallest number of bits that can be sent in one group (e.g., 4-bit, 8-bit or 16-bit transfers). They also vary as to the order in which the bits are transmitted (LSB or MSB first). The following examples show how the LTC1290 accommodates these differences.

National MICROWIRE (COP402)

The COP402 transfers data MSB first and in 4-bit increments (nibbles). This is easily accommodated by setting the LTC1290 to MSB first format and 12-bit word length. The data output word is then received by the COP402 in three 4-bit blocks.

Hardware and Software Interface to COP402 Processor



D_{OUT} from LTC1290 stored in COP402 RAM

	MSB‡	
Location $13	B11 B10 B9 B8	first 4 bits
Location $14	B7 B6 B5 B4	second 4 bits
	LSB	
Location $15	B3 B2 B1 B0	third 4 bits

‡B11 is MSB in unipolar or sign bit in bipolar

APPLICATIONS INFORMATION

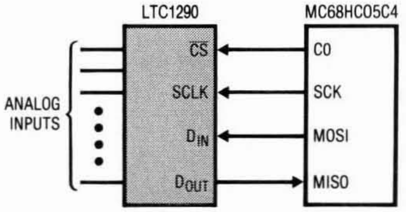
COP402 Code

	MNEMONIC		COMMENTS
	CLRA		MUST BE FIRST INSTRUCTION
	LBI	1,0	BR = 1 BD = 0 INITIALIZE B REG.
	STII	8	FIRST D_{IN} NIBBLE IN $10
	STII	E	SECOND D_{IN} NIBBLE IN $11
	STII	0	NULL DATA IN $12, B = $13
	LEI	C	SET EN TO (1100) BIN
LOOP	SC		CARRY SET
	LDD	1,0	LOAD FIRST D_{IN} NIBBLE IN ACC
	OGI	0	G0 ($\overline{CS}$) CLEARED
	XAS		ACC TO SHIFT REG. BEGIN SHIFT
	LDD	1,1	LOAD NEXT D_{IN} NIBBLE IN ACC
	NOP		TIMING
	XAS		NEXT NIBBLE, SHIFT CONTINUES
	XIS	0	FIRST NIBBLE D_{OUT} TO $13
	LDD	1,2	PUT NULL DATA IN ACC
	XAS		SHIFT CONTINUES, D_{OUT} TO ACC
	XIS	0	NEXT NIBBLE D_{OUT} TO $14
	RC		CLEAR CARRY
	CLRA		CLEAR ACC
	XAS		THIRD NIBBLE D_{OUT} TO ACC
	OGI	1	G0 ($\overline{CS}$) SET
	XIS	0	THIRD NIBBLE D_{OUT} TO $15
	LBI	1,3	SET B REG. FOR NEXT LOOP

Motorola SPI (MC68HC05C4)

The MC68HC05C4 transfers data MSB first and in 8-bit increments. Programming the LTC1290 for MSB first format and 16-bit word length allows the 12-bit data output to be received by the MPU as two 8-bit bytes with the final 4 unused bits filled with zeroes by the LTC1290.

Hardware and Software Interface to Motorola MC68HC05C4 Processor



D_{OUT} from LTC1290 stored in MC68HC05C4 RAM

	MSB*	
Location $61	B11 B10 B9 B8 B7 B6 B5 B4	byte 1
	LSB	
Location $62	B3 B2 B1 B0 0 0 0 0	byte 2

*B11 is MSB in unipolar or sign bit in bipolar

MC68HC05C4 Code

	MNEMONIC		COMMENTS
	LDA	#$50	CONFIGURATION DATA FOR SPCR
	STA	$0A	LOAD DATA INTO SPCR ($0A)
	LDA	#$FF	CONFIG. DATA FOR PORT C DDR
	STA	$06	LOAD DATA INTO PORT C DDR
	LDA	#$0F	LOAD LTC1290 D_{IN} DATA INTO ACC
	STA	$50	LOAD LTC1290 D_{IN} DATA INTO $50
START	BCLR	0,$02	CO GOES LOW ($\overline{CS}$ GOES LOW)
	LDA	$50	LOAD D_{IN} INTO ACC FROM $50
	STA	$0C	LOAD D_{IN} INTO SPI. START SCK
	NOP		8 NOPs FOR TIMING
	LDA	$0B	CHECK SPI STATUS REG
	LDA	$0C	LOAD LTC1290 MSBs INTO ACC
	STA	$61	STORE MSBs IN $61
	STA	$0C	START NEXT SPI CYCLE
	NOP		6 NOPs FOR TIMING
	BSET	0,$02	CO GOES HIGH ($\overline{CS}$ GOES HIGH)
	LDA	$0B	CHECK SPI STATUS REGISTER
	LDA	$0C	LOAD LTC1290 LSBs INTO ACC
	STA	$62	STORE LSBs IN $62

Parallel Port Microprocessors

When interfacing the LTC1290 to an MPU which has a parallel port, the serial signals are created on the port with software. Three MPU port lines are programmed to create the $\overline{CS}$, SCLK and D_{IN} signals for the LTC1290. A fourth port line reads the D_{OUT} line. An example is made of the Intel 8051/8052/80C252 family.

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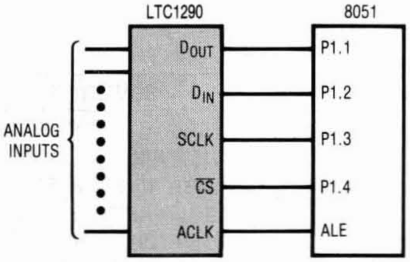
Intel 8051

To interface to the 8051, the LTC1290 is programmed for MSB first format and 12-bit word length. The 8051 generates $\overline{CS}$, SCLK and D_{IN} on three port lines and reads D_{OUT} on the fourth.

Hardware and Software Interface to Intel 8051 Processor



D_{OUT} from LTC1290 stored in 8051 RAM

	MSB*							
R2	B11	B10	B9	B8	B7	B6	B5	54
				LSB				
R3	B3	B2	B1	B0	0	0	0	0

*B11 is MSB in unipolar or sign bit in bipolar

8051 Code

MNEMONIC			COMMENTS
	MOV	P1, #02H	BIT 1 PORT 1 SET AS INPUT
	CLR	P1.3	SCLK GOES LOW
	SETB	P1.4	$\overline{CS}$ GOES HIGH
CONT	MOV	A, #0EH	D_{IN} WORD FOR LTC1290
	CLR	P1.4	$\overline{CS}$ GOES LOW
	MOV	R4, #08H	LOAD COUNTER
	NOP		DELAY FOR DEGLITCHER
LOOP	MOV	C, P1.1	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT INTO ACC
	MOV	P1.2, C	OUTPUT D_{IN} BIT TO LTC1290
	SETB	P1.3	SCLK GOES HIGH
	CLR	P1.3	SCLK GOES LOW
	DJNZ	R4, LOOP	NEXT BIT
	MOV	R2, A	STORE MSBs IN R2
	MOV	C, P1.1	READ DATA BIT INTO CARRY
	CLR	A	CLEAR ACC
	RLC	A	ROTATE DATA BIT INTO ACC
	SETB	P1.3	SCLK GOES HIGH
	CLR	P1.3	SCLK GOES LOW
	MOV	C, P1.1	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT INTO ACC
	SETB	P1.3	SCLK GOES HIGH
	CLR	P1.3	SCLK GOES LOW
	MOV	C, P1.1	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT INTO ACC
	SETB	P1.3	SCLK GOES HIGH
	CLR	P1.3	SCLK GOES LOW
	MOV	C, P1.1	READ DATA BIT INTO CARRY
	RRC	A	ROTATE RIGHT INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	MOV	R3, A	STORE LSBs IN R3
	SETB	P1.3	SCLK GOES HIGH
	CLR	P1.3	SCLK GOES LOW
	SETB	P1.4	$\overline{CS}$ GOES HIGH
	MOV	R5, #0BH	LOAD COUNTER
DELAY	DJNZ	R5, DELAY	GO TO DELAY IF NOT DONE

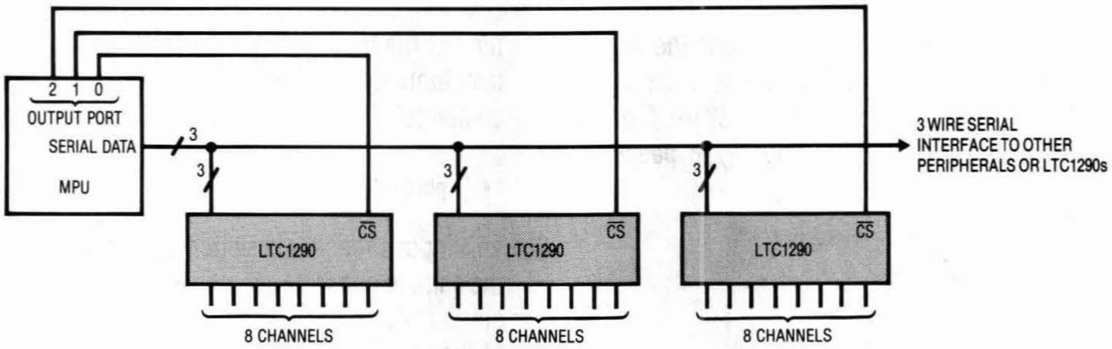

2 1 0
OUTPUT PORT
SERIAL DATA
MPU
3
3
3
3
LTC1290
$\overline{CS}$
LTC1290
$\overline{CS}$
LTC1290
$\overline{CS}$
8 CHANNELS
8 CHANNELS
8 CHANNELS
3 WIRE SERIAL INTERFACE TO OTHER PERIPHERALS OR LTC1290s

Figure 5. Several LTC1290s Sharing One 3 Wire Serial Interface

Sharing the Serial Interface

The LTC1290 can share the same 3 wire serial interface with other peripheral components or other LTC1290s (see Figure 5). In this case, the $\overline{CS}$ signals decide which LTC1290 is being addressed by the MPU.

ANALOG CONSIDERATIONS

1. Grounding

The LTC1290 should be used with an analog ground plane and single point grounding techniques.

Pin 11 (AGND) should be tied directly to this ground plane.

Pin 10 (DGND) can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

Pin 20 (V_{CC}) should be bypassed to the ground plane with a 22µF tantalum with leads as short as possible. Pin 12 (V^-) should be bypassed with a 0.1µF ceramic disk. For single supply applications, V^- can be tied to the ground plane.

It is also recommended that pin 13 (REF^-) and pin 9 (COM) be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

Figure 6 shows an example of an ideal ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

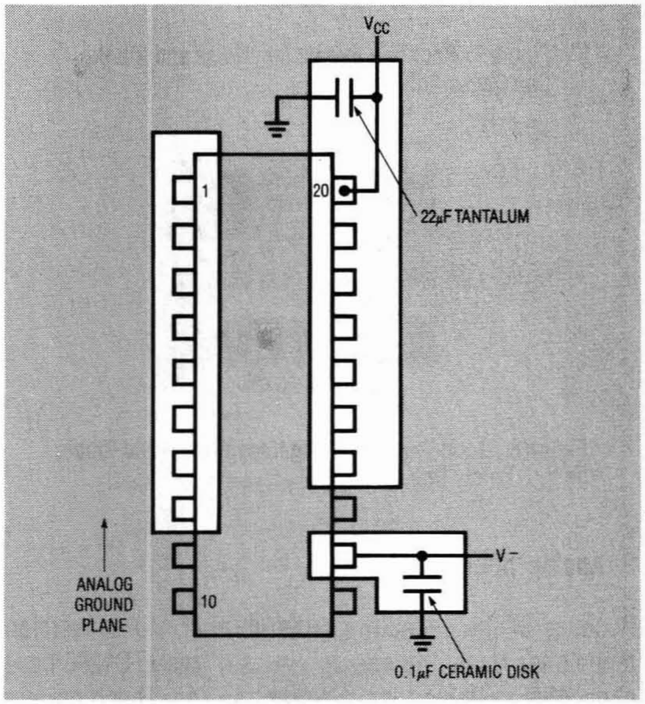

V_{CC}
1
20
22µF TANTALUM
ANALOG GROUND PLANE
10
V⁻
0.1µF CERAMIC DISK

Figure 6. Example Ground Plane for the LTC1290

2. Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a 22µF tantalum capacitor and leads as short as possible. The lead from the device to the V_{CC}

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supply should also be kept to a minimum and the V_{CC} supply should have a low output impedance such as that obtained from a voltage regulator (e.g. LT323A). Figures 7 and 8 show the effects of good and poor V_{CC} bypassing.

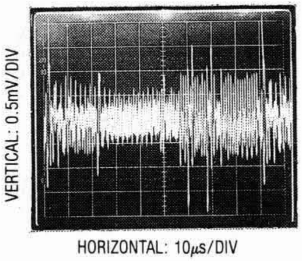

Figure 7. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

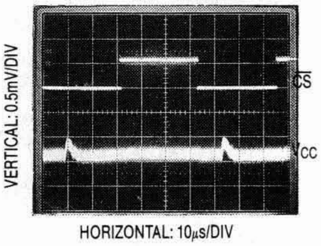

Figure 8. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1290 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

Source Resistance

The analog inputs of the LTC1290 look like a 100pF capacitor (C_{IN}) is series with a 500Ω resistor (R_{ON}) as shown in Figure 9. C_{IN} gets switched between the selected " + " and " – " inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

" + " Input Settling

This input capacitor is switched onto the " + " input during the sample phase (t_{SMPL}, see Figure 10). The sample phase starts at the 4th SCLK cycle and lasts until the falling edge of the last SCLK (the 8th, 12th or 16th SCLK cycle depending on the selected word length). The voltage on the " + " input must settle completely within this sample time. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If large " + " input source resistance must be used, the sample time can be increased by using a slower SCLK frequency or selecting a longer word length. With the minimum possible sample time of 2μs, **$R_{SOURCE}^+ < 1k$ and $C1 < 20pF$ will provide adequate settling.**

" – " Input Settling

At the end of the sample phase the input capacitor switches to the " – " input and the conversion starts (see Figure 10). During the conversion, the " + " input voltage is effectively "held" by the sample and hold and will not affect the conversion result. However, it is critical that the " – " input voltage be free of noise and settle completely during the first four ACLK cycles of the conversion time. Minimizing R_{SOURCE}^- and C2 will improve settling time. If large " – " input source resistance must be used, the time allowed for settling can be extended by using a slower ACLK frequency. At the maximum ACLK rate of 4MHz, **$R_{SOURCE}^- < 250\Omega$ and $C2 < 20pF$ will provide adequate settling.**

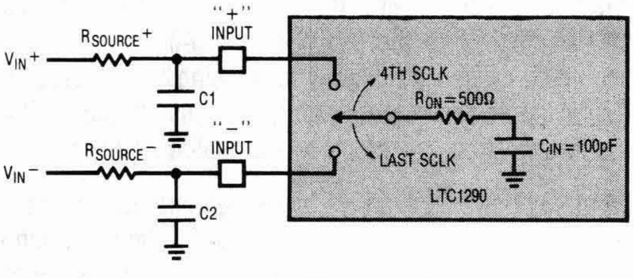

Figure 9. Analog Input Equivalent Circuit

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Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 10). Again, the "+" and "−" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 2μs ("+" input) and 1μs ("−" input) which occur at the maximum clock rates (ACLK = 4MHz and SCLK = 2MHz). Figures 11 and 12 show examples of adequate and poor op amp settling.

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 13. For large values of C_F (e.g., 1μF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 20μs, the input current equals 25μA at $V_{IN} = 5V$. In this case, a filter resistor of 5Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

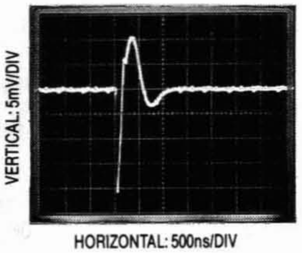

Figure 11. Adequate Settling of Op Amps Driving Analog Input

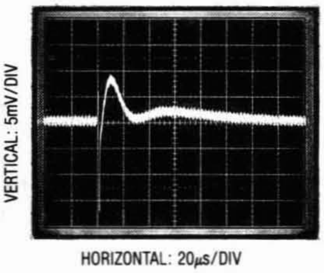

Figure 12. Poor Op Amp Settling Can Cause A/D Errors

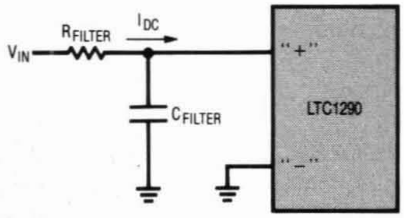
V_{IN}
R_{FILTER}
I_{DC}
C_{FILTER}
"+"
LTC1290
"−"

Figure 13. RC Input Filtering

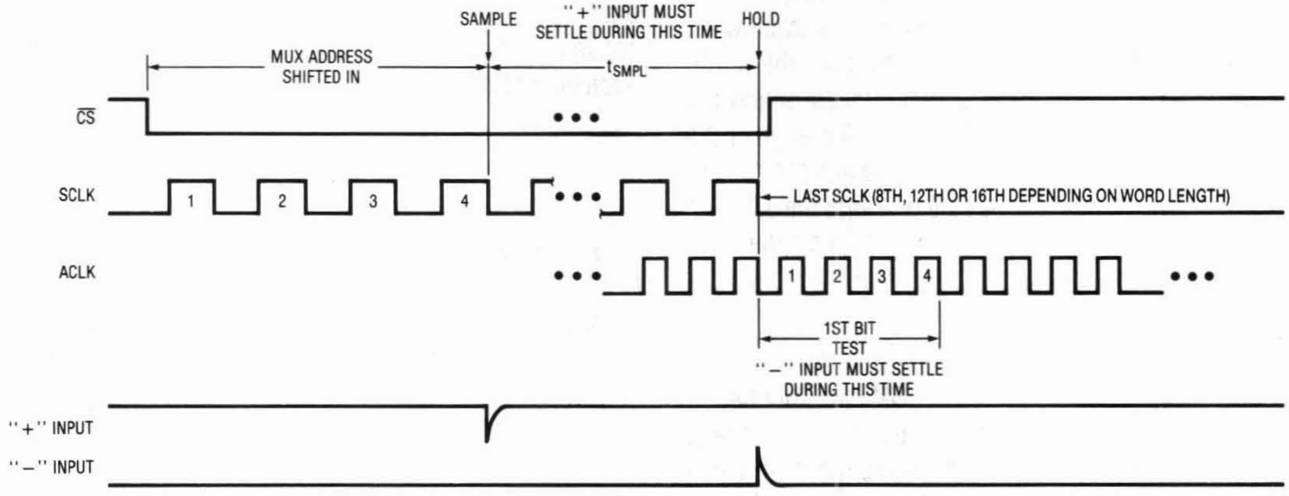
SAMPLE
"+" INPUT MUST SETTLE DURING THIS TIME
HOLD
MUX ADDRESS SHIFTED IN
t_{SMPL}
CS
SCLK
1
2
3
4
LAST SCLK (8TH, 12TH OR 16TH DEPENDING ON WORD LENGTH)
ACLK
1
2
3
4
1ST BIT TEST
"−" INPUT MUST SETTLE DURING THIS TIME
"+" INPUT
"−" INPUT

Figure 10. "+" and "−" Input Settling Windows

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Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1μA (at 125°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

Noise Coupling into Inputs

High source resistance input signals (>500Ω) are more sensitive to coupling from external sources. It is preferable to use channels near the center of the package (i.e., CH2-CH7) for signals which have the highest output resistance because they are essentially shielded by the pins on the package ends (DGND and CH0). Grounding any unused inputs (especially the end pin, CH0) will also reduce outside coupling into high source resistances.

4. Sample and Hold

Single Ended Inputs

The LTC1290 provides a built-in sample and hold (S&H) function for all signals acquired in the single ended mode (COM pin grounded). This sample and hold allows the LTC1290 to convert rapidly varying signals (see typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 10. The sampling interval begins after the fourth MUX address bit is shifted in and continues during the remainder of the data transfer. On the falling edge of the final SCLK, the S&H goes into hold mode and the conversion begins. The voltage will be held on either the 8th, 12th or 16th falling edge of the SCLK depending on the word length selected.

Differential Inputs

With differential inputs or when the COM pin is not tied to ground, the A/D no longer converts just a single voltage but rather the difference between two voltages. In these cases, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single ended mode. However, the voltage on the selected "−" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 52 ACLK cycles. Therefore, a change in the "−" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "−" input this error would be:

$$V_{ERROR\,(MAX)} = V_{PEAK} \times 2 \times \pi \times f(\text{"}-\text{"}) \times 52/f_{ACLK}$$

Where f("−") is the frequency of the "−" input voltage, V_{PEAK} is its peak amplitude and f_{ACLK} is the frequency of the ACLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "−" input to generate a 1/4LSB error (300μV) with the converter running at ACLK = 4MHz, its peak value would have to be 61mV.

5. Reference Inputs

The voltage between the reference inputs of the LTC1290 defines the voltage span of the A/D converter. The reference inputs will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 14). During each bit test of the conversion (every 4 ACLK cycles), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

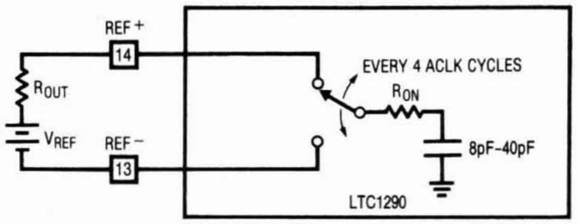

Figure 14. Reference Input Equivalent Circuit

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When driving the reference inputs, two things should be kept in mind:

1. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each 4 ACLK cycles). Figures 15 and 16 show examples of both adequate and poor settling. Using a slower ACLK will allow more time for the reference to settle. However, even at the maximum ACLK rate of 4MHz most references and op amps can be made to settle within the 1µs bit time. For example the LT1027 will settle adequately or with a 10µF bypass capacitor at REF^+ the LT1021 can also be used.
2. It is recommended that the REF^- input be tied directly to the analog ground plane. If REF^- is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

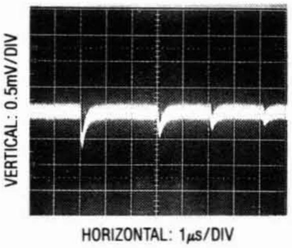

Figure 15. Adequate Reference Settling

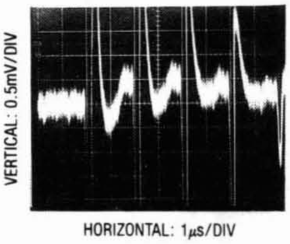

Figure 16. Poor Reference Settling Can Cause A/D Errors

6. Reduced Reference Operation

The effective resolution of the LTC1290 can be increased by reducing the input span of the converter. The LTC1290 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Gain Error vs Reference Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Offset
2. Noise

Offset with Reduced V_{REF}

The offset of the LTC1290 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 0.1mV which is 0.1LSB with a 5V reference becomes 0.4LSB with a 1.25V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the " – " input to the LTC1290.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1290 can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

For operation with a 5V reference, the 200µV noise is only 0.16LSB peak-to-peak. In this case, the LTC1290 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter

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in the output code. For example, with a 1.25V reference, this same 200μV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF}, V_{IN} or V^-) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

7. LTC1290 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/D's in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "effective number of bits (ENOB)." SNR is defined as the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the nonfundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by

$$SNR = (6.02N + 1.76dB)$$

where N is the number of bits. Thus the SNR is a function of the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. A Fast Fourier Transform (FFT) plot of the output spectrum of the LTC1290 is shown in Figures 17A and 17B. The input (F_{IN}) frequencies are 1kHz and 25kHz with the sampling frequency (F_S) at 50.6kHz. The SNR obtained from the plot are 73.25dB and 72.54dB.

Rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = (SNR - 1.76dB)/6.02$$

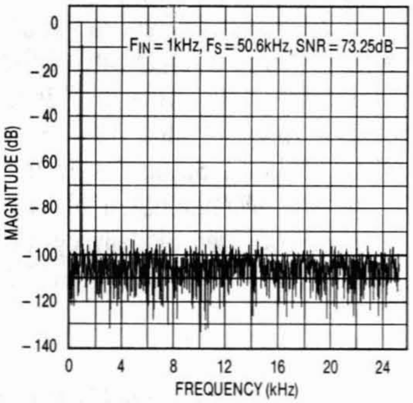

Figure 17A. LTC1290 FFT Plot

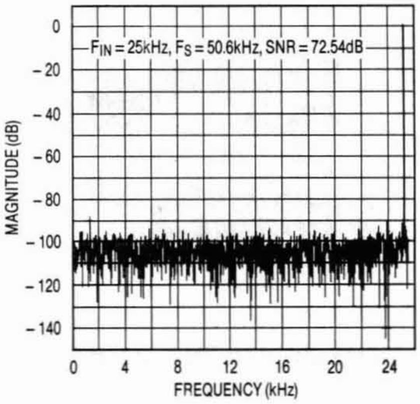

Figure 17B. LTC1290 FFT Plot

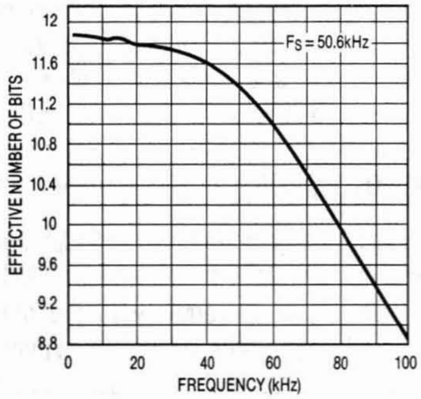

Figure 18. LTC1290 ENOB vs Input Frequency

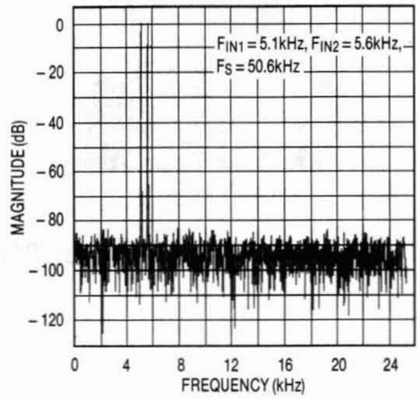

Figure 19. LTC1290 FFT Plot

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This is the so-called effective number of bits (ENOB). For the example shown in Figures 17A and 17B, N = 11.9 bits and 11.8 bits, respectively. Figure 18 shows a plot of ENOB as a function of input frequency. The curve shows the A/D's ENOB remain in the range of 11.9 to 11.8 for input frequencies up to $F_S/2$.

Figure 19 shows an FFT plot of the output spectrum for two tones applied to the input of the A/D. Non-linearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

8. Overvoltage Protection

Applying signals to the analog MUX that exceed the positive or negative supply of the device will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog MUX before power is applied to the LTC1290. Another example, is the input source is operating from different supplies of larger value than the LTC1290. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. As shown in Figure 20, a 1kΩ resistor is enough to stand off ±15V (15mA for one only channel). If more than one channel exceeds the supplies than the following guidelines can be used. Limit the current to 7mA per channel and 28mA for all channels. This means four channels can handle 7mA of input current each. Reducing the ACLK and SCLK frequencies from the maximum of 4MHz and 2MHz, respectively (See Typical Performance Characteristics Curves Maximum ACLK Frequency vs Source Resistance and Sample and Hold Acquisition Time vs Source Resistance.) allows the use of larger current limiting resistors. Use 1N4148 diode clamps from the MUX inputs to V_{CC} and V^- if the value of the series resistor will not allow the maximum clock speeds to be used or if an unknown source is used to drive the LTC1290 MUX inputs.

How the various power supplies to the LTC1290 are applied can also lead to overvoltage conditions. For single supply operation (i.e. unipolar mode), if V_{CC} and REF^+ are not tied together, then V_{CC} should be turned on first, then REF^+. If this sequence cannot be met connecting a diode from REF^+ to V_{CC} is recommended (see Figure 21).

For dual supplies (bipolar mode) placing two Schottky diodes from V_{CC} and V^- to ground (Figure 23) will prevent power supply reversal from occuring when an input source is applied to the analog MUX before power is applied to the device. Power supply reversal occurs, for example, if the input is pulled below V^- then V_{CC} will pull a diode drop below ground which could cause the device not to power up properly. Likewise, if the input is pulled above V_{CC} then V^- will be pulled a diode drop above ground. If no inputs are present on the MUX, the Schottky diodes are not required if V^- is applied first, then V_{CC}.

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

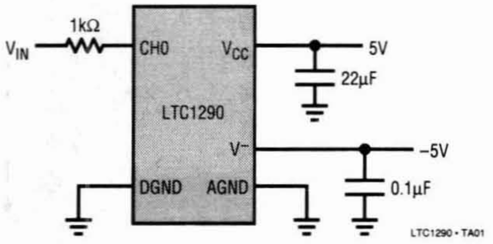


Figure 20. Overvoltage Protection for MUX

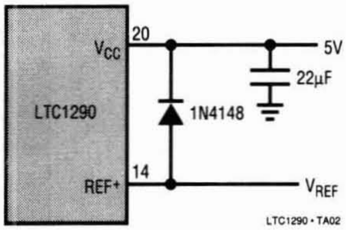


Figure 21.

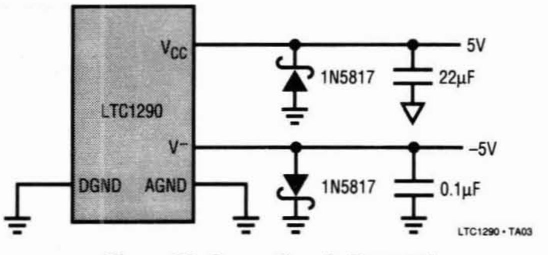


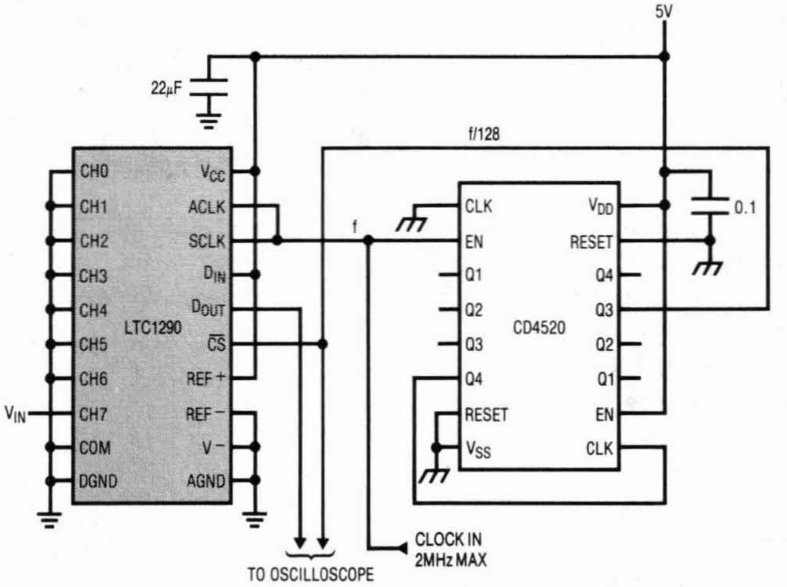
Figure 22. Power Supply Reversal

TYPICAL APPLICATIONS

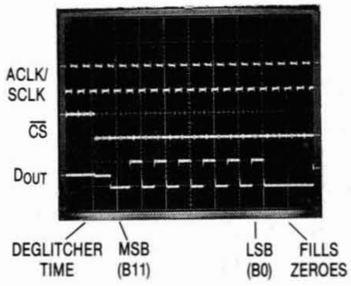
A "Quick Look" Circuit for the LTC1290

Users can get a quick look at the function and timing of the LTC1290 by using the following simple circuit. REF^+ and D_{IN} are tied to V_{CC} selecting a 5V input span, CH7 as a single ended input, unipolar mode, MSB first format and 16-bit word length. ACLK and SCLK are tied together and driven by an external clock. $\overline{CS}$ is driven at 1/128 the clock rate by the CD4520 and D_{OUT} outputs the data. All other pins are tied to a ground plane. The output data from the D_{OUT} pin can be viewed on an oscilloscope which is set up to trigger on the falling edge of $\overline{CS}$.

A "Quick Look" Circuit for the LTC1290


5V
22µF
f/128
0.1
f
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
VCC
ACLK
SCLK
DIN
DOUT
CS
REF+
REF−
V−
AGND
LTC1290
VIN
CLK
EN
Q1
Q2
Q3
Q4
RESET
VSS
VDD
RESET
Q4
Q3
Q2
Q1
EN
CLK
CD4520
TO OSCILLOSCOPE
CLOCK IN
2MHz MAX

Scope Trace of LTC1290 "Quick Look" Circuit Showing A/D Output of 010101010101 (555_{HEX})



VERTICAL: 5V/DIV
HORIZONTAL: 1µs/DIV

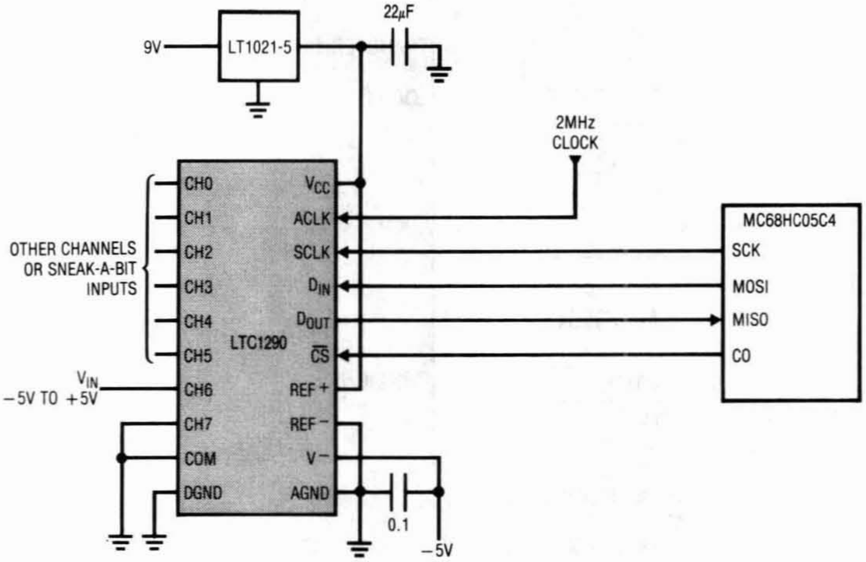
TYPICAL APPLICATIONS

SNEAK-A-BIT™

The LTC1290's unique ability to software select the polarity of the differential inputs and the output word length is used to achieve one more bit of resolution. Using the circuit below with two conversions and some software, a 2's complement 12-bit + sign word is returned to memory inside the MPU. The MC68HC05C4 was chosen as an example; however, any processor could be used.

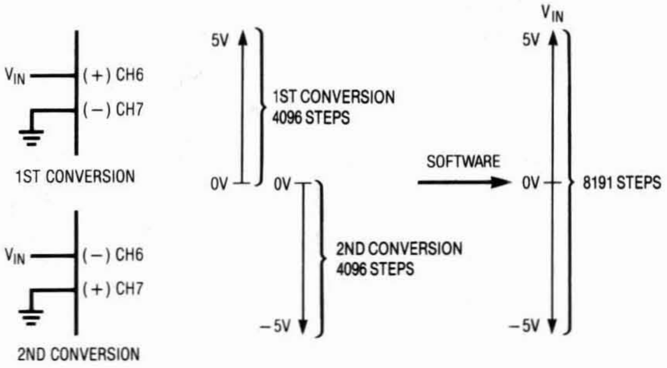
Two 12-bit unipolar conversions are performed: the first over a 0V to 5V span and the second over a 0V to −5V span (by reversing the polarity of the inputs). The sign of the input is determined by which of the two spans contained it. Then the resulting number (ranging from −4095 to +4095 decimal) is converted to 2's complement notation and stored in RAM.

SNEAK-A-BIT Circuit



9V
LT1021-5
22μF
2MHz CLOCK
OTHER CHANNELS OR SNEAK-A-BIT INPUTS
V_{IN} −5V TO +5V
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
LTC1290
V_{CC}
ACLK
SCLK
D_{IN}
D_{OUT}
$\overline{CS}$
REF+
REF−
V−
AGND
0.1
−5V
MC68HC05C4
SCK
MOSI
MISO
CO

SNEAK-A-BIT



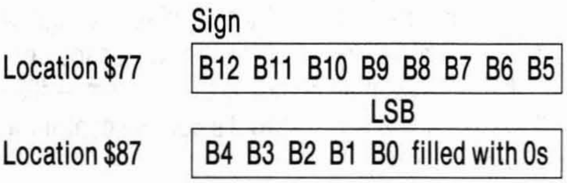
V_{IN}
(+) CH6
(−) CH7
1ST CONVERSION
V_{IN}
(−) CH6
(+) CH7
2ND CONVERSION
5V
0V
1ST CONVERSION 4096 STEPS
0V
−5V
2ND CONVERSION 4096 STEPS
SOFTWARE
V_{IN}
5V
0V
−5V
8191 STEPS

SNEAK-A-BIT is a trademark of Linear Technology Corp.

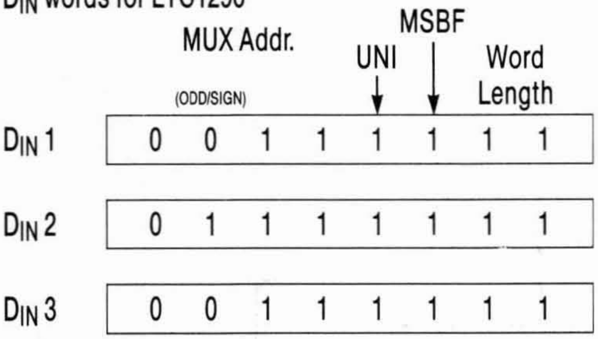
TYPICAL APPLICATIONS

SNEAK-A-BIT Code

D_{OUT} from LTC1290 in MC68HC05C4 RAM



D_{IN} words for LTC1290



Sneak-A-Bit Code for the LTC1290 Using the MC68HC05C4

MNEMONIC	DESCRIPTION
LDA #$50	Configuration data for SPCR
STA $0A	Load configuration data into $0A
LDA #$FF	Configuration data for port C DDR
STA $06	Load configuration data into port C DDR
BSET 0, $02	Make sure $\overline{CS}$ is high
JSR READ −/+	Dummy read configures LTC1290 for next read
JSR READ +/−	Read CH6 with respect to CH7
JSR READ −/+	Read CH7 with respect to CH6
JSR CHK SIGN	Determines which reading has valid data, converts to 2's complement and stores in RAM

Sneak-A-Bit Code for the LTC1290 Using the MC68HC05C4

MNEMONIC	DESCRIPTION
READ −/+: LDA #$3F	Load D_{IN} word for LTC1290 into ACC
JSR TRANSFER	Read LTC1290 routine
LDA $60	Load MSBs from LTC1290 into ACC
STA $71	Store MSBs in $71
LDA $61	Load LSBs from LTC1290 into ACC
STA $72	Store LSBs in $72
RTS	Return
READ +/−: LDA #$7F	Load D_{IN} word for LTC1290 into ACC
JSR TRANSFER	Read LTC1290 routine
LDA $60	Load MSBs from LTC1290 into ACC
STA $73	Store MSBs in $73
LDA $61	Load LSBs from LTC1290 into ACC
STA $74	Store LSBs in $74
RTS	Return
TRANSFER: BCLR 0, $02	$\overline{CS}$ goes low
STA $0C	Load D_{IN} into SPI. Start transfer
LOOP 1: TST $0B	Test status of SPIF
BPL LOOP 1	Loop to previous instruction if not done
LDA $0C	Load contents of SPI data reg into ACC
STA $0C	Start next cycle
STA $60	Store MSBs in $60
LOOP 2: TST $0B	Test status of SPIF
BPL LOOP 2	Loop to previous instruction if not done
BSET 0, $02	$\overline{CS}$ goes high
LDA $0C	Load contents of SPI data reg into ACC
STA $61	Store LSBs in $61
RTS	Return
CHK SIGN: LDA $73	Load MSBs of +/− read into ACC
ORA $74	Or ACC (MSBs) with LSBs of +/− read
BEQ MINUS	If result is 0 goto minus
CLC	Clear carry
ROR $73	Rotate right $73 through carry
ROR $74	Rotate right $74 through carry
LDA $73	Load MSBs of +/− read into ACC
STA $77	Store MSBs in RAM location $77
LDA $74	Load LSBs of +/− read into ACC
STA $87	Store LSBs in RAM location $87
BRA END	Goto end of routine
MINUS: CLC	Clear carry
ROR $71	Shift MSBs of −/+ read right
ROR $72	Shift LSBs of −/+ read right
COM $71	1's complement of MSBs
COM $72	1's complement of LSBs
LDA $72	Load LSBs into ACC
ADD #$01	Add 1 to LSBs
STA $72	Store ACC in $72
CLRA	Clear ACC
ADC $71	Add with carry to MSBs. Result in ACC
STA $71	Store ACC in $71
STA $77	Store MSBs in RAM location $77
LDA $72	Load LSBs in ACC
STA $87	Store LSBs in RAM location $87
END: RTS	Return

TYPICAL APPLICATIONS

Power Shutdown

For battery powered applications it is desirable to keep power dissipation at a minimum. The LTC1290 can be powered down when not in use reducing the supply current from a nominal value of 5mA to typically 5μA (with ACLK turned off). See the curve for Supply Current (Power Shutdown) vs ACLK if ACLK cannot be turned off when the LTC1290 is powered down. In this case the supply current is proportional to the ACLK frequency and is independent of temperature until it reaches the magnitude of the supply current attained with ACLK turned off.

As an example of how to use this feature let's add this to the previous application, SNEAK-A-BIT. After the CHK SIGN subroutine call insert the following:

```
                   •
                   •
JSR CHK SIGN       Determines which reading has valid
                   data, converts to 2's complement
                   and stores in RAM
JSR SHUTDOWN       LTC1290 power shutdown routine
```

The actual subroutine is:

```
SHUTDOWN:  LDA   #$3D       Load DIN word for
                            LTC1290 into ACC
           JSR TRANSFER     Read LTC1290 routine
           RTS              Return
```

To place the device in power shutdown the word length bits are set to WL1 = 0 and WL0 = 1. The LTC1290 is powered up on the next request for a conversion and it's ready to digitize an input signal immediately.

Power Shutdown Timing Considerations

After power shutdown has been requested, the LTC1290 is powered up on the next request for a conversion. This request can be initiated either by bring $\overline{CS}$ low or by starting the next cycle of SCLKs if $\overline{CS}$ is kept low (see Figures 3 and 4). When the SCLK frequency is much slower than the ACLK frequency a situation can arise where the LTC1290 could power down and then prematurely power back up. Power shutdown begins at the negative going edge of the 10th SCLK once it has been requested. A dummy conversion is executed and the LTC1290 waits for the next request for conversion. If the SCLKs have not finished once the LTC1290 has finished its dummy conversion it will recognize the next remaining SCLKs as a request to start a conversion and power up the LTC1290 (see Figure 23). To prevent this bring either $\overline{CS}$ high at the 10th SCLK (Figure 24) or clock out only 10 SCLKs (Figure 25) when power shutdown is requested.

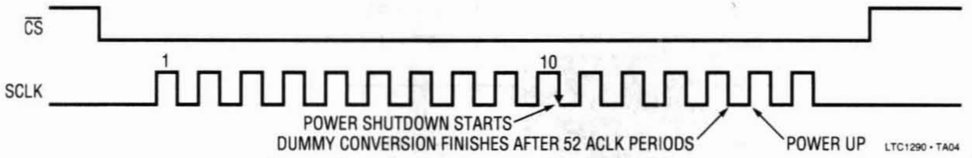

CS
SCLK
1
10
POWER SHUTDOWN STARTS
DUMMY CONVERSION FINISHES AFTER 52 ACLK PERIODS
POWER UP
LTC1290 • TA04

Figure 23. Power Shutdown Timing Problem

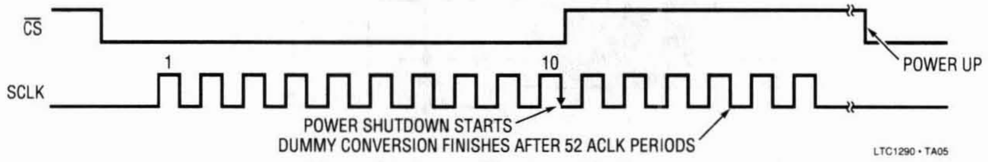

CS
SCLK
1
10
POWER UP
POWER SHUTDOWN STARTS
DUMMY CONVERSION FINISHES AFTER 52 ACLK PERIODS
LTC1290 • TA05

Figure 24. Power Shutdown Timing

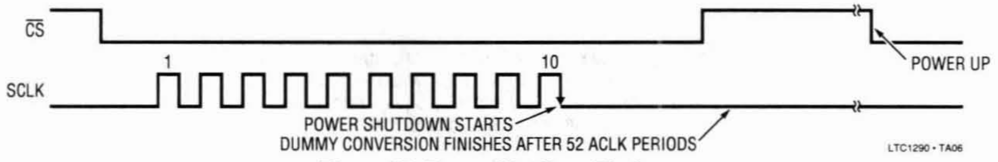

CS
SCLK
1
10
POWER UP
POWER SHUTDOWN STARTS
DUMMY CONVERSION FINISHES AFTER 52 ACLK PERIODS
LTC1290 • TA06

Figure 25. Power Shutdown Timing

LINEAR TECHNOLOGY

LTC1292

Single Chip 12-Bit Data Acquisition System

FEATURES

- Built-In Sample and Hold
- Single Supply 5V Operation
- Direct 3-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 60kHz Maximum Throughput Rate
- Analog Inputs Common Mode to Supply Rails

KEY SPECIFICATIONS

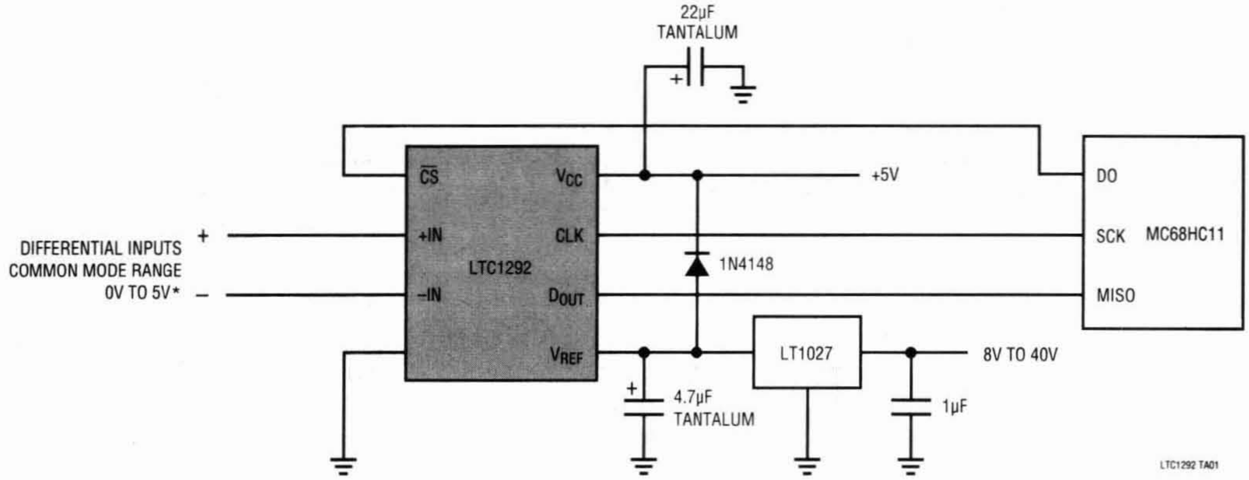
- Resolution .... 12 Bits
- Fast Conversion Time .... 12μs Max Over Temp
- Low Supply Current 6.0mA

DESCRIPTION

The LTC1292 is a 12-bit data acquisition system that contains a 12-bit, switched capacitor successive approximation A/D, a differential input, sample and hold on the (+) input, and serial I/O. All these features are packaged in an 8-pin DIP. The LTC1292 is capable of digitizing signals at a 60kHz rate and with the device's excellent AC characteristics, it can be used for DSP applications. The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing data to be transmitted over three wires. Given the accuracy, ease of use and small package size these devices are well suited for digitizing analog signals in remote applications where minimum number of interconnects and power consumption are important.

TYPICAL APPLICATION

12-Bit Differential Input Data Acquisition System

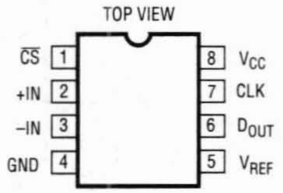

22μF
TANTALUM
+
$\overline{CS}$
V_{CC}
+IN
CLK
LTC1292
–IN
D_{OUT}
V_{REF}
+5V
1N4148
DO
SCK
MC68HC11
MISO
LT1027
8V TO 40V
+
4.7μF
TANTALUM
1μF
DIFFERENTIAL INPUTS
COMMON MODE RANGE
0V TO 5V*
+
–
LTC1292 TA01

*FOR OVERVOLTAGE PROTECTION LIMIT THE INPUT CURRENT TO 15mA PER PIN OR CLAMP THE INPUTS TO V_{CC} AND GND WITH 1N4148 DIODES. CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED CHANNEL OR THE OTHER CHANNEL IS OVERVOLTAGED (V_{IN} < GND OR V_{IN} > V_{CC}). SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) to GND or V^-	12V
Voltage	
Analog and Reference Inputs	$-0.3V$ to $V_{CC} + 0.3V$
Digital Inputs	$-0.3V$ to 12V
Digital Outputs	$-0.3V$ to $V_{CC} + 0.3V$
Power Dissipation	500mW
Operating Temperature Range	
LTC1292BC, LTC1292CC, LTC1292DC	0°C to 70°C
LTC1292BI, LTC1292CI, LTC1292DI	−40°C to 85°C
LTC1292BM, LTC1292CM, LTC1292DM	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

ORDER PART NUMBER
LTC1292BMJ8
LTC1292CMJ8
LTC1292DMJ8
LTC1292BIJ8
LTC1292CIJ8
LTC1292DIJ8
LTC1292BIN8
LTC1292CIN8
LTC1292DIN8
LTC1292BCJ8
LTC1292CCJ8
LTC1292DCJ8
LTC1292BCN8
LTC1292CCN8
LTC1292DCN8

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1292B			LTC1292C			LTC1292D			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Error	(Note 4)	●			±3.0			±3.0			±3.0	LSB
Linearity Error (INL)	(Note 4 & 5)	●			±0.5			±0.5			±0.75	LSB
Gain Error	(Note 4)	●			±0.5			±1.0			±4.0	LSB
Minimum Resolution for which No Missing Codes are Guaranteed					12			12			12	Bits
Analog and REF Input Range	(Note 7)	●	$(V^-)-0.05V$ to $V_{CC} + 0.05V$									V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	μA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	μA
Off Channel Lekage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	μA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	μA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1292B/LTC1292C/LTC1292D			UNITS
				MIN	TYP	MAX	
f_{CLK}	Clock Frequency	V_{CC} = 5V (Note 6)		0.1		1.0	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1292B/LTC1292C/LTC1292D MIN	TYP	MAX	UNITS
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		14CLK 2.5µs			Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		160	300	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		80	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		80	200	ns
t_{hDO}	Time Output Data Remains Valid after CLK↓				130		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	50	ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V (Note 6)		300			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 5V (Note 6)		400			ns
$t_{su\overline{CS}}$	Set-up Time, $\overline{CS}$↓ before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time between Data Transfer Cycles	V_{CC} = 5V (Note 6)		2.5			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V (Note 6)		14			CLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs			100 5 5		pF pF pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1292B/LTC1292C/LTC1292D MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = –10µA I_O = 360µA	 ●	 2.4	4.7 4.0		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	High Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High	● ●			3 –3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–20		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			20		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High	●		6.0	12	mA
I_{REF}	Reference Current	$\overline{CS}$ High	●		10	50	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 5V, V_{REF+} = 5V, CLK = 1.0MHz unless otherwise specified. The ● denotes specifications which apply over the operating temperature range; all other limits and typicals T_A = 25°C.

Note 4: One LSB is equal to V_{REF} divided by 4096. For example, when V_{REF} = 5V, 1LSB = 5V/4096 = 1.22mV.

Note 5: Linearity error is specified between the actual and points of the A/D transfer curve. The deviation is measured from the center of the quantization band.

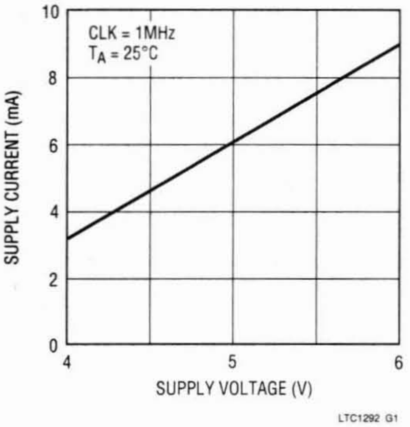
Note 6: Recommended operating conditions.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

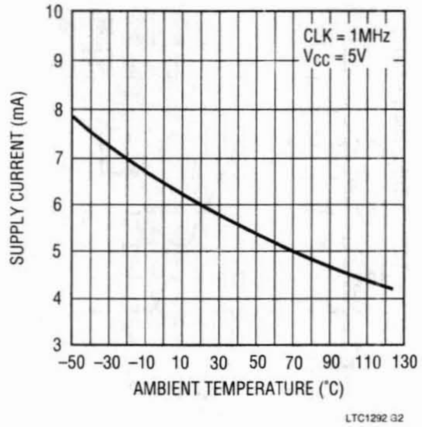
Note 8: Channel leakage current is measured after the channel selection.

TYPICAL PERFORMANCE CHARACTERISTICS

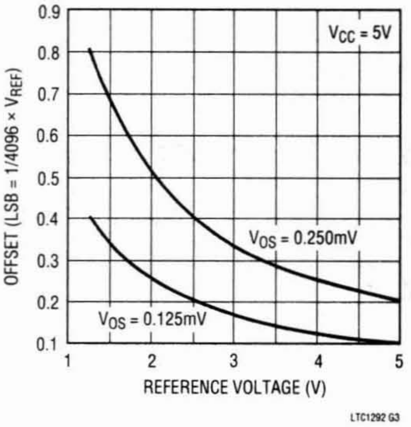
Supply Current vs Supply Voltage



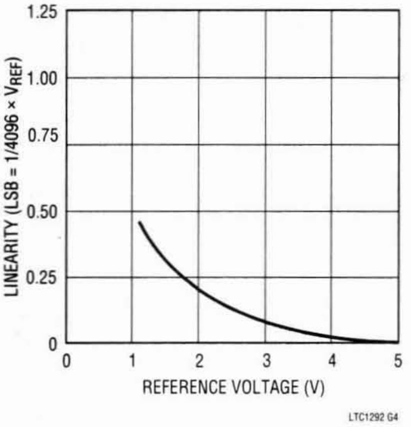
Supply Current vs Temperature



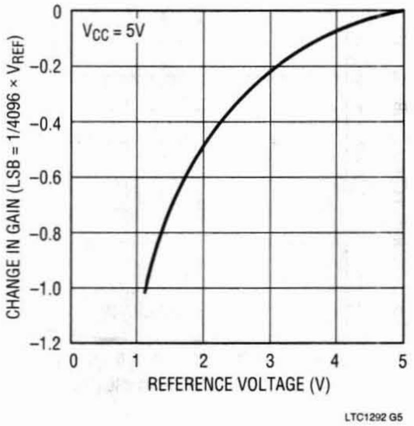
Unadjusted Offset Voltage vs Reference Voltage



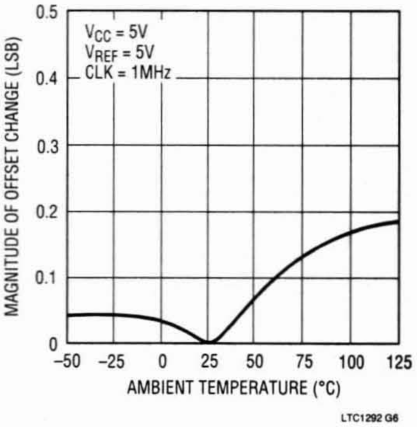
Change in Linearity vs Reference Voltage



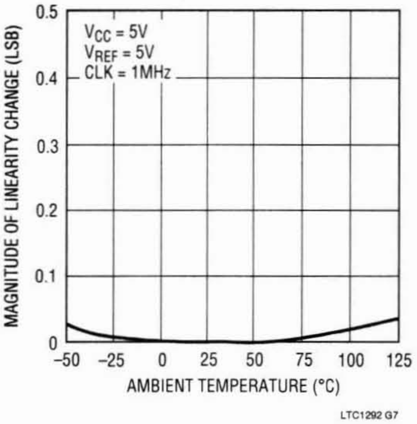
Change in Gain vs Reference Voltage



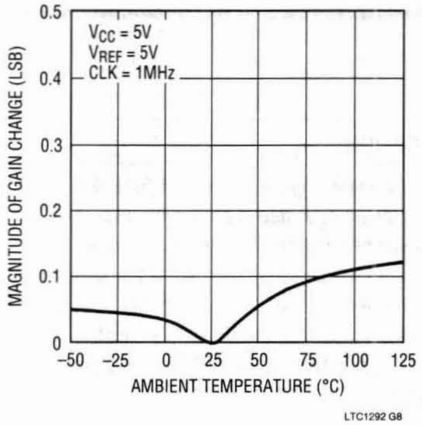
Change in Offset vs Temperature



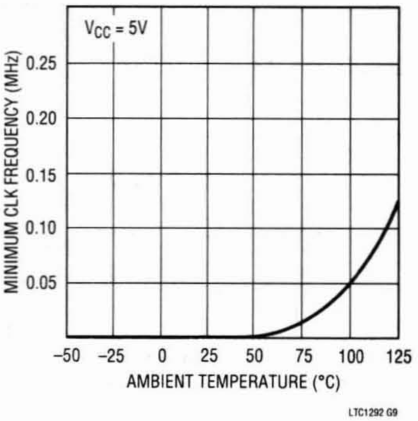
Change in Linearity vs Temperature



Change in Gain vs Temperature



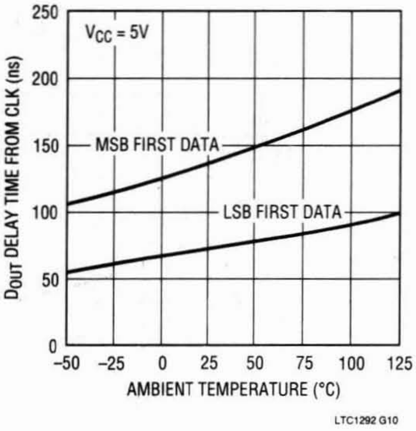
Minimum Clock Rate for 0.1 LSB Error*



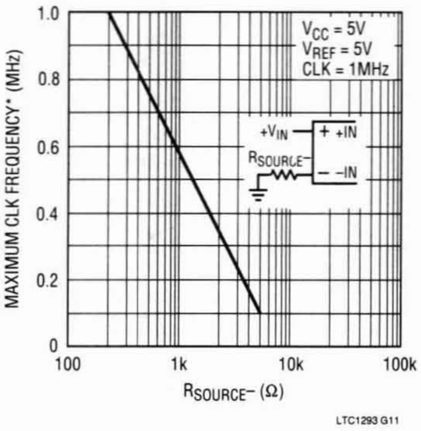
* AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

TYPICAL PERFORMANCE CHARACTERISTICS

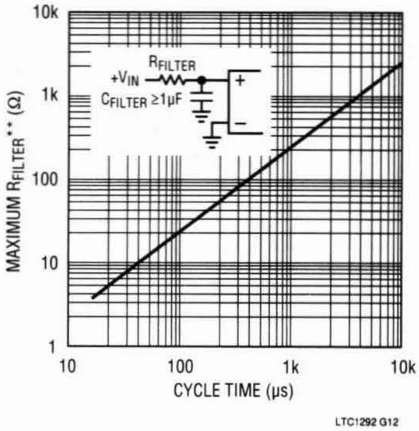
D_{OUT} Delay Time vs Temperature



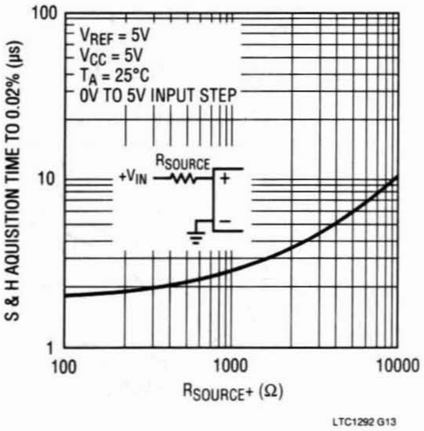
Maximum Clock Rate vs Source Resistance



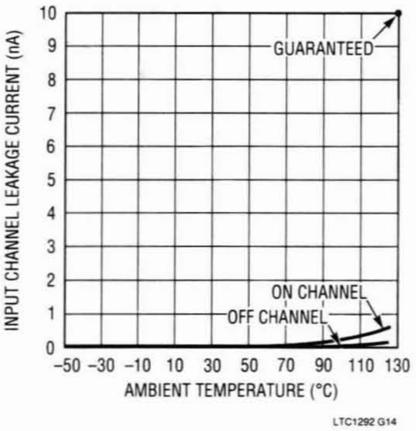
Maximum Filter Resistor vs Cycle Time



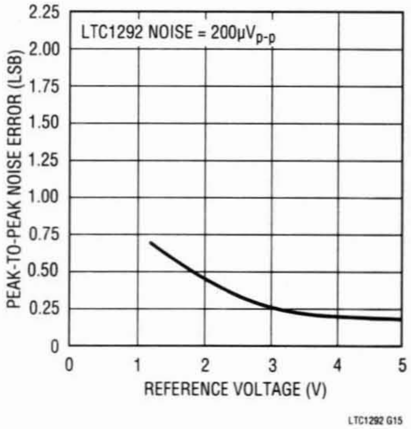
Sample and Hold Acquisition Time vs Source Resistance



Input Channel Leakage Current vs Temperature



Noise Error vs Reference Voltage



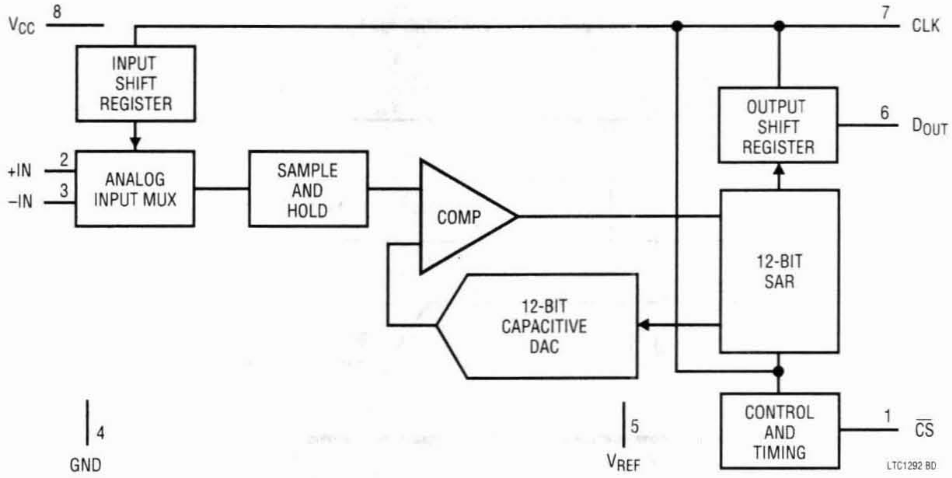
* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

**MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0Ω IS FIRST DETECTED.

PIN FUNCTIONS

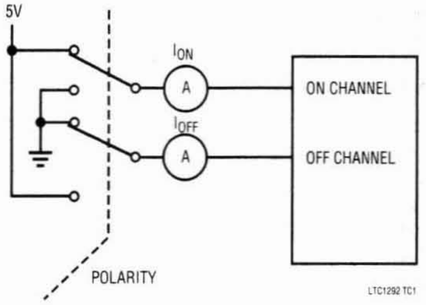
#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1292.
2, 3	+IN, –IN	Analog Inputs	These inputs must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	V_{REF}	Reference Input	The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

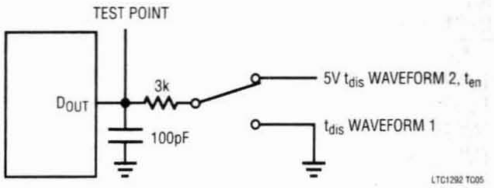

VCC
8
7
CLK
INPUT SHIFT REGISTER
OUTPUT SHIFT REGISTER
6
DOUT
+IN
2
–IN
3
ANALOG INPUT MUX
SAMPLE AND HOLD
COMP
12-BIT SAR
12-BIT CAPACITIVE DAC
4
GND
5
VREF
CONTROL AND TIMING
1
CS
LTC1292 BD

TEST CIRCUITS

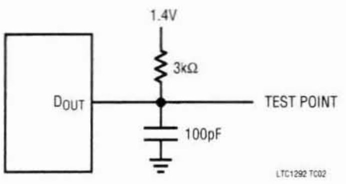
On and Off Channel Leakage Current


5V
ION
A
IOFF
A
ON CHANNEL
OFF CHANNEL
POLARITY
LTC1292 TC1

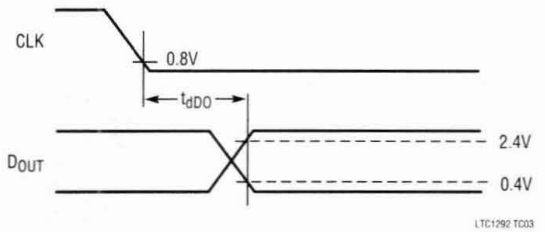
Load Circuit for t_{dis} and t_{en}


TEST POINT
DOUT
3k
100pF
5V tdis WAVEFORM 2, ten
tdis WAVEFORM 1
LTC1292 TC05

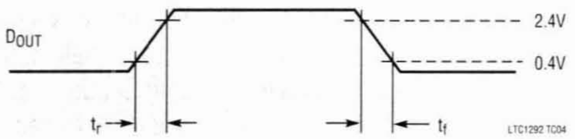
Load Circuit for t_{dDO}, t_r and t_f


1.4V
3kΩ
DOUT
TEST POINT
100pF
LTC1292 TC02

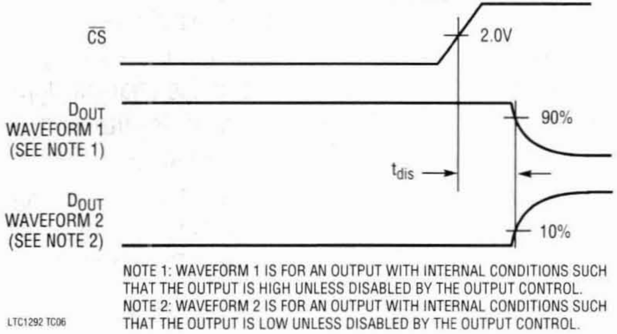
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}


CLK
0.8V
tdDO
DOUT
2.4V
0.4V
LTC1292 TC03

Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f


DOUT
2.4V
0.4V
tr
tf
LTC1292 TC04

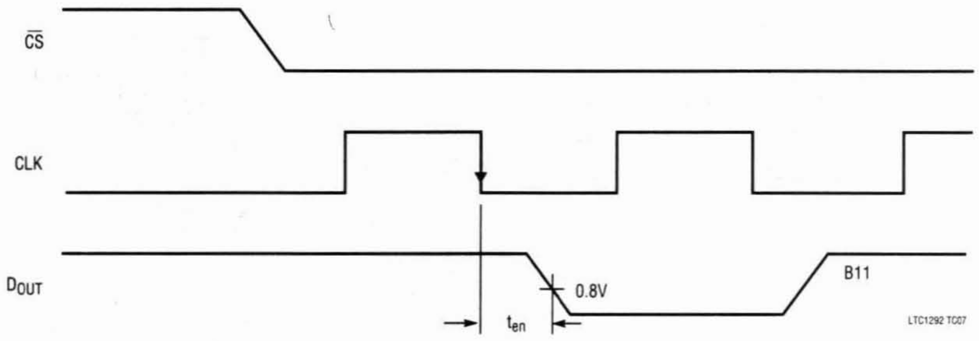
Voltage Waveforms for t_{dis}


CS
2.0V
DOUT WAVEFORM 1 (SEE NOTE 1)
90%
tdis
DOUT WAVEFORM 2 (SEE NOTE 2)
10%
LTC1292 TC06

NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS

Voltage Waveforms for t_{en}



APPLICATIONS INFORMATION

The LTC1292 is a data acquisition component which contains the following functional blocks:

1. 12-bit succesive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, half duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

The LTC1292 communicates with microprocessors and other external circuitry via a synchronous, half duplex, three wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge. The LTC1292 does not require a configuration input word and has no D_{IN} pin. It is permanently configured to have a single differential input and to operate in unipolar mode. A falling $\overline{CS}$ initiates data transfer. The first CLK pulse enables D_{OUT}. After one null bit, the A/D conversion result is output on the D_{OUT} line with a MSB first sequence followed by a LSB first sequence. With the half duplex serial interface the D_{OUT} data is from the current conversion. This provides easy interface to MSB or LSB first serial ports. Bringing $\overline{CS}$ high resets the LTC1292 for the next data exchange.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1292**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MCROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

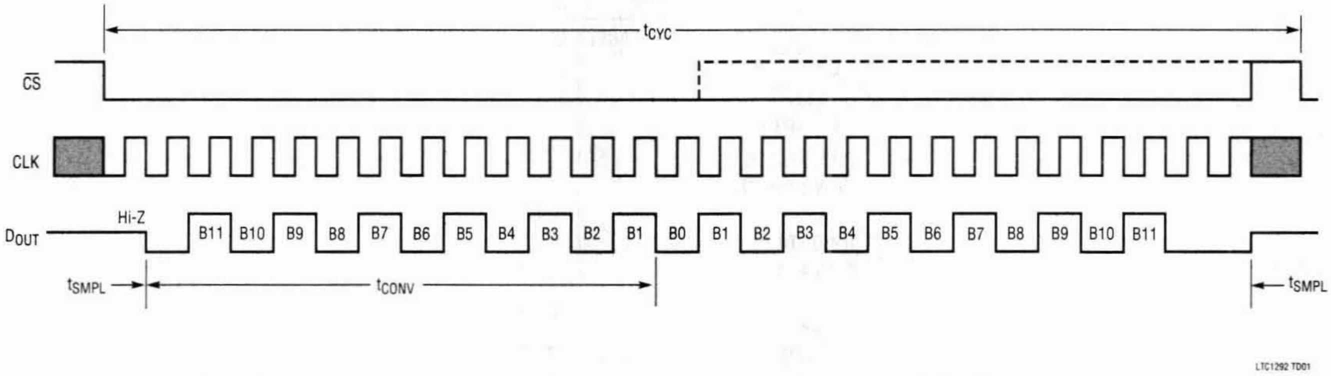
* Requires external hardware

** Contact factory for interface information for processors not on this list

† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

APPLICATIONS INFORMATION

LTC1292 Operating Sequence


tCYC
CS
CLK
DOUT
Hi-Z
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11
tSMPL
tCONV
tSMPL
LTC1292 TD01

Microprocessor Interfaces

The LTC1292 can interface directly (without external hardware) to most popular microprocessors(MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1292. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. A dummy D_{IN} word sent to the data register starts the SPI process. With two 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The second 8-bit transfer clocks the remaining bits B7 through B0 into the MPU. The data is

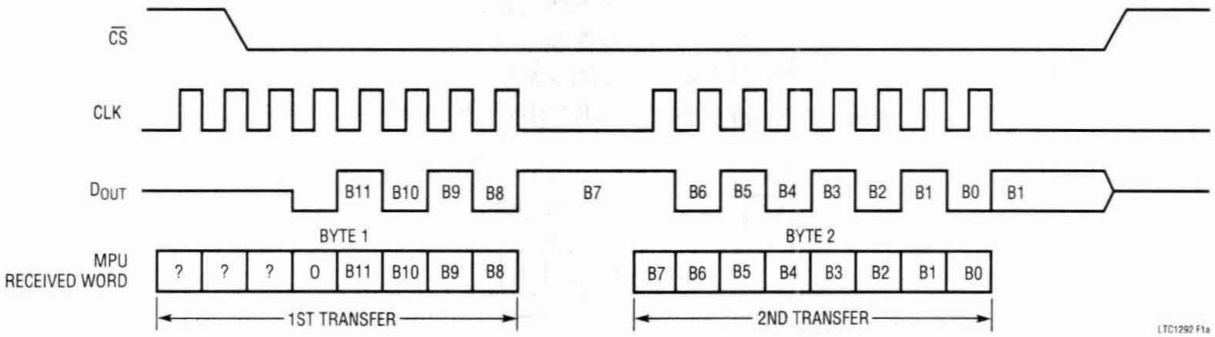

CS
CLK
DOUT
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0 B1
BYTE 1
BYTE 2
MPU RECEIVED WORD
? ? ? 0 B11 B10 B9 B8
B7 B6 B5 B4 B3 B2 B1 B0
1ST TRANSFER
2ND TRANSFER
LTC1292 F1a

Figure 1a. Data Exchange Between LTC1292 and MC68HC11

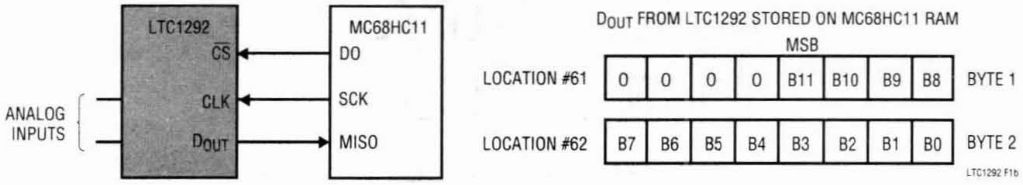

LTC1292
CS
CLK
DOUT
ANALOG INPUTS
MC68HC11
DO
SCK
MISO
DOUT FROM LTC1292 STORED ON MC68HC11 RAM
MSB
LOCATION #61
0 0 0 0 B11 B10 B9 B8
BYTE 1
LOCATION #62
B7 B6 B5 B4 B3 B2 B1 B0
BYTE 2
LTC1292 F1b

Figure 1b. Hardware and Software Interface to Motorola MC68HC11 Microcontroller

APPLICATIONS INFORMATION

MC68HC11 CODE

LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR
	STAA	$1028	LOAD DATA INTO SPCR ($1028)
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR
	STAA	$1009	LOAD DATA INTO PORT D DDR
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A
	STAA	$50	LOAD DUMMY DIN DATA INTO $50
LOOP	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000
	LDAB	#$00	LOAD ACC B WITH $00
	LDAA	$50	LOAD DUMMY DIN INTO ACC A FROM $50
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	NOP		DELAY $\overline{CS}$ FALL TIME TO RIGHT JUSTIFY DATA
	STAB	$08, X	D0 GOES LOW ($\overline{CS}$ GOES LOW)
	NOP		6 NOPS FOR TIMING
	LDAA	$1029	CHECK SPI STATUS REG
	LDAA	$102A	LOAD LTC1292 MSBs INTO ACC A
	STAA	$61	STORE MSBs IN $61
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	NOPS		6 NOPS FOR TIMING
	BSET	$08,X,$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	LDAA	$1029	CHECK SPI STATUS REGISTER
	LDAA	$102A	LOAD LTC1292 LSBs IN ACC
	STAA	$62	STORE LSBs IN $62
	JMP	LOOP	START NEXT CONVERSION

right justified in the two memory locations. This was made possible by delaying the falling edge of $\overline{CS}$ till after the second CLK. ANDing the first byte with OD$_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to show the interface between the LTC1292 and parallel port microprocessors. The signals $\overline{CS}$ and CLK are generated on two port lines and the D_{OUT} signal is read on a third port line. After a falling CLK edge each data bit is loaded into the carry bit and then rotated into the accumulator. Once the first 8 MSBs have been shifted into the accumulator they are loaded into register R2. The last four bits are shifted in the same way and loaded into register R3. The output data is left justified in registers R2 and R3.

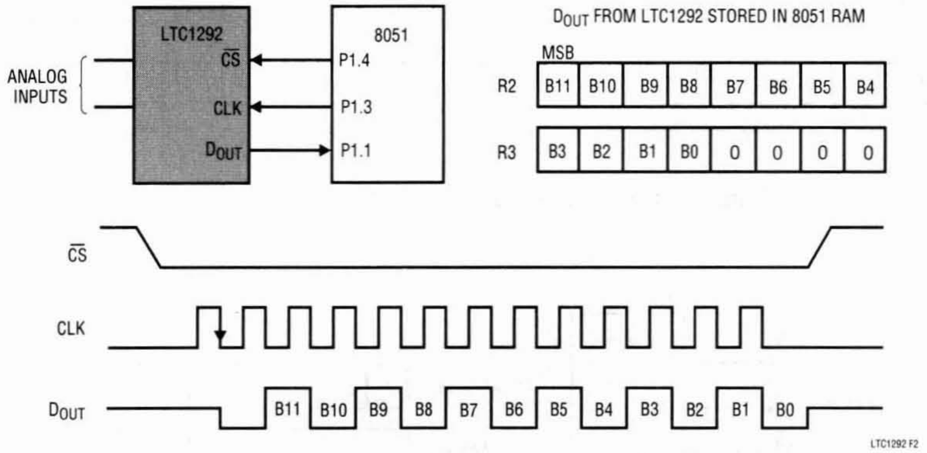

ANALOG INPUTS
LTC1292
CS
CLK
DOUT
8051
P1.4
P1.3
P1.1
DOUT FROM LTC1292 STORED IN 8051 RAM
MSB
R2
B11 B10 B9 B8 B7 B6 B5 B4
R3
B3 B2 B1 B0 0 0 0 0
CS
CLK
DOUT
B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0
LTC1292 F2

Figure 2. Hardware and Software Interface to Intel 8051 Processor

APPLICATIONS INFORMATION

8051 CODE

LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	P1,#02h	BIT 1 PORT 1 SET AS INPUT
	CLR	P1.3	CLK GOES LOW
	SETB	P1.4	$\overline{CS}$ GOES HIGH
CONT	CLR	P1.4	$\overline{CS}$ GOES LO
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	MOV	R4,#08H	LOAD COUNTER
LOOP	MOV	C,P1.1	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT INTO ACC
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	DJNZ	R4,LOOP	NEXT BIT
	MOV	R2,A	STORE MSBs IN R2
	MOV	C,P1.1	READ DATA BIT INTO CARRY
	CLR	A	CLEAR ACC
	RLC	A	ROTATE DATA BIT (B3) INTO ACC
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	MOV	C,P1.1	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT (B2) INTO ACC
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	MOV	C,P1.1	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT (B1) INTO ACC
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	MOV	C,P1.1	READ DATA BIT INTO CARRY
	SETB	P1.4	$\overline{CS}$ GOES HIGH
	RRC	A	ROTATE DATA BIT (B0) INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	MOV	R3,A	STORE LSBs IN R3
	AJMP	CONT	START NEXT CONVERSION

Sharing the Serial Interface

The LTC1292 can share the same two-wire serial interface with other peripheral components or other LTC1292s (Figure 3). In this case, the $\overline{CS}$ signals decide which LTC1292 is being addressed by the MPU.

ANALOG CONSIDERATIONS

Grounding

The LTC1292 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a PC board. The ground pin (Pin 4) should be tied directly to the ground plane with minimum lead length (a low profile socket is fine). Pin 7 (V_{CC}) should be bypassed to the ground plane with a 22µF (minimum value) tantalum with leads as short as possible and as close as possible to the pin. A 0.1µF ceramic disk also should be placed in parallel with the 22µF and again with leads as short as possible and as close to V_{CC} as possible. Figure 4 shows an example of an ideal LTC1292 ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

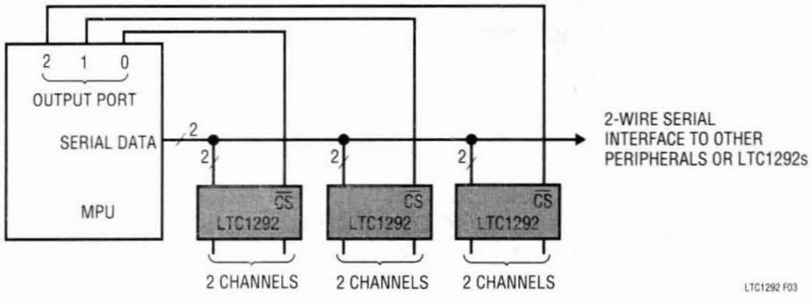


Figure 3. Several LTC1292s Sharing One 2-Wire Serial Interface

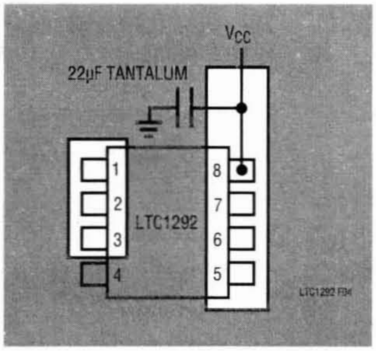


Figure 4. Example Ground Plane for the LTC1292

APPLICATIONS INFORMATION

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog plane with a minimum of 22µF tantalum capacitor and with leads as short as possible. The lead from the device to the V_{CC} supply also should be kept to a minimum and the V_{CC} supply should have a low output impedance such as obtained from a voltage regulator (e.g., LT323A). For high frequency bypassing a 0.1µF ceramic disk placed in parallel with the 22µF is recommended. Again the leads should be kept to a minimum. Figures 5 and 6 show the effects of good and poor V_{CC} bypassing.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1292 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure the transients caused by the current spikes settle completely before the conversion begins.

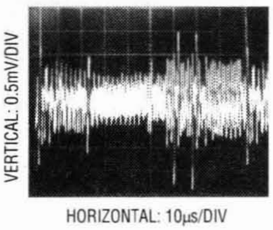


Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

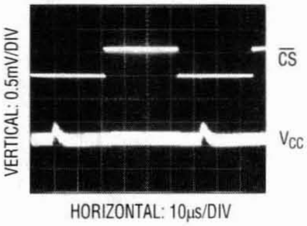


Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

Source Resistance

The analog inputs of the LTC1292 look like a 100pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}). C_{IN} gets switched between (+) and (–) inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

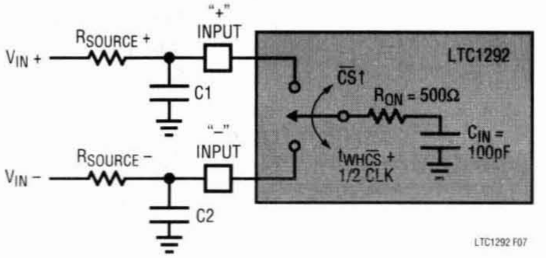


Figure 7. Analog Input Equivalent Circuit

"+" Input Settling

The input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figures 8a, 8b and 8c). The sample period can be as short as $t_{WH\overline{CS}}$ + 1/2 CLK cycle or as long as $t_{WH\overline{CS}}$ + 1 1/2 CLK cycles before a conversion starts. This variability depends on where $\overline{CS}$ falls relative to CLK. The voltage on the "+" input must settle completely within the sample period. Minimizing R_{SOURCE}+ and C1 will improve the settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 3.0µs, **R_{SOURCE}+ < 2.0kΩ and C1 < 20pF will provide adequate settle time.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figures 8a, 8b and 8c). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. It is critical that the "–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing R_{SOURCE}– and C2 will improve settling time. If large "–" input source resistance must be used the time can be extended by using a slower

APPLICATIONS INFORMATION

“+” and “–” Input Settling Windows

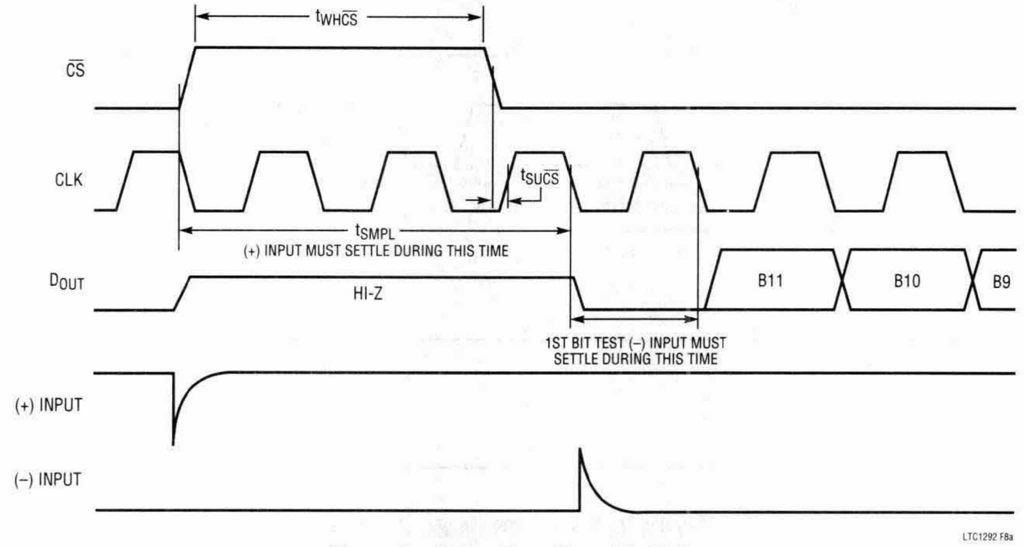

$t_{WH\overline{CS}}$
$\overline{CS}$
CLK
$t_{SU\overline{CS}}$
t_{SMPL}
(+) INPUT MUST SETTLE DURING THIS TIME
D_{OUT}
HI-Z
B11
B10
B9
1ST BIT TEST (–) INPUT MUST SETTLE DURING THIS TIME
(+) INPUT
(–) INPUT
LTC1292 F8a

Figure 8a. Setup Time ($t_{SU\overline{CS}}$) is Met

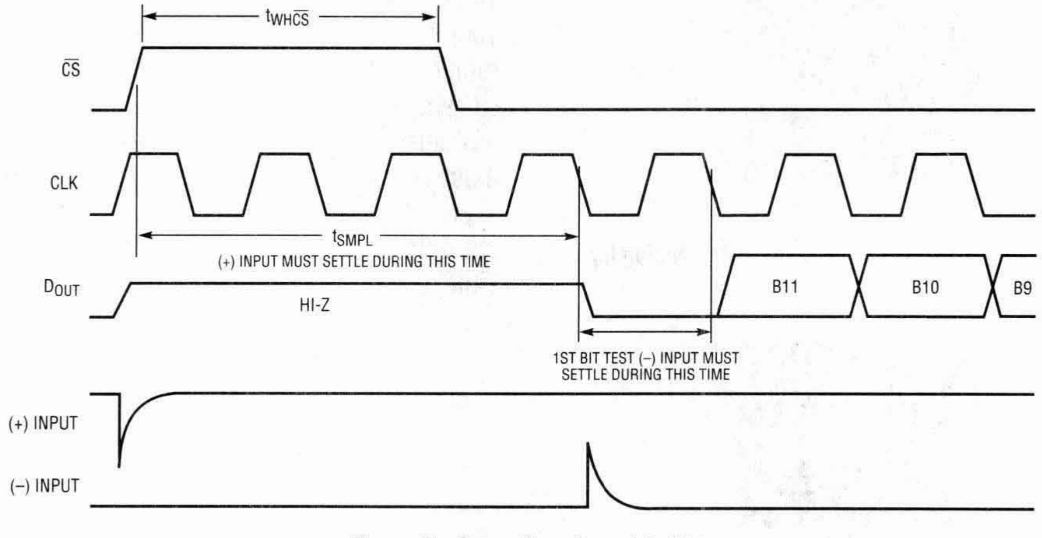

$t_{WH\overline{CS}}$
$\overline{CS}$
CLK
t_{SMPL}
(+) INPUT MUST SETTLE DURING THIS TIME
D_{OUT}
HI-Z
B11
B10
B9
1ST BIT TEST (–) INPUT MUST SETTLE DURING THIS TIME
(+) INPUT
(–) INPUT
LTC1292 F8b

Figure 8b. Setup Time ($t_{SU\overline{CS}}$) is Met

CLK frequency. At the maximum CLK frequency of 1MHz, **R_{SOURCE}– < 250Ω and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settles within the allowed time (see Figures 8a, 8b and 8c). Again the “+” and “–” input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 3.0μs (“+” input) and 1μs (“–” input) that occurs at the maximum clock rate of 1MHz. Figures 9 and 10 show examples adequate and poor op amp settling.

APPLICATIONS INFORMATION

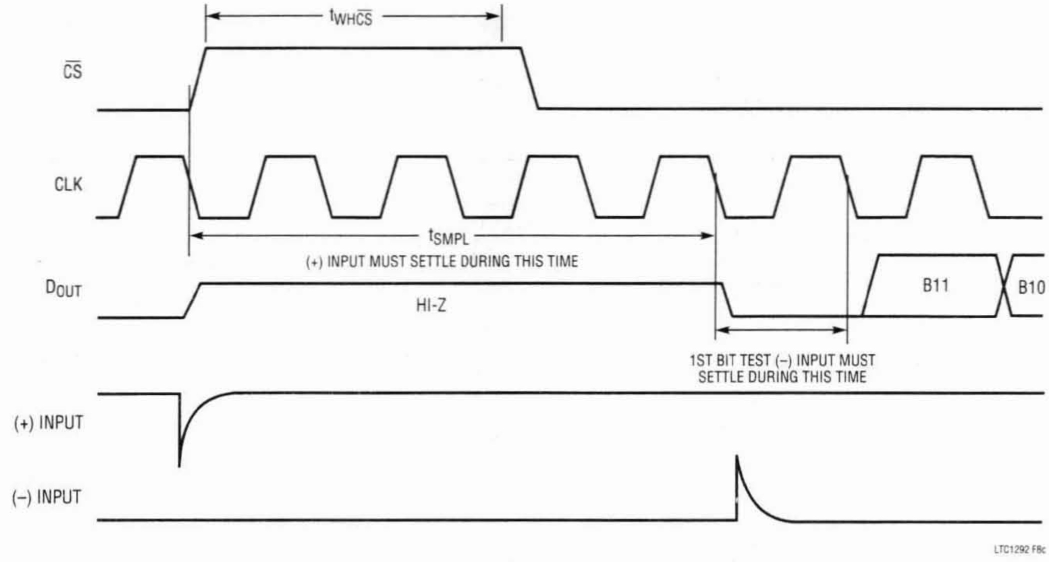

$t_{WH\overline{CS}}$
$\overline{CS}$
CLK
t_{SMPL}
(+) INPUT MUST SETTLE DURING THIS TIME
D_{OUT}
HI-Z
B11
B10
1ST BIT TEST (–) INPUT MUST SETTLE DURING THIS TIME
(+) INPUT
(–) INPUT
LTC1292 F8c

Figure 8c. Setup Time ($t_{SU\overline{CS}}$) is Not Met

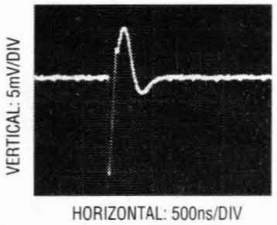


Figure 9. Adequate Settling of Op Amp Driving Analog Input

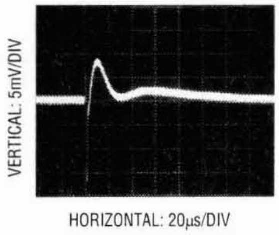


Figure 10. Poor Op Amp Settling Can Cause A/D Errors

RC Input filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., 1μF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor.

The magnitude of the DC current is approximately I_{DC} = 100pF × V_{IN}/t_{CYC} and is roughly proportional to V_{IN}. When running at the minimum cycle time of 16.5μs, the input current equals 30μA at V_{IN} = 5V. Here a filter resistor of 4Ω will cause 0.1LSB of full-scale error. If a large filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the typical performance characteristics curve Maximum Filter Resistor vs Cycle Time.

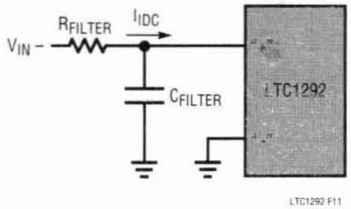

R_{FILTER}
I_{DC}
V_{IN}
C_{FILTER}
LTC1292
LTC1292 F11

Figure 11. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1μA (at 125°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical

APPLICATIONS INFORMATION

performance characteristics curve Input Channel Leakage Current vs Temperature).

SAMPLE AND HOLD

Single Ended Input

The LTC1292 provides a built-in sample and hold (S&H) function on the +IN input for signals acquired in the single ended mode (–IN pin grounded). The sample and hold allows the LTC1292 to convert rapidly varying signals (see typical performance characteristics curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval begins at rising edge of $\overline{CS}$ and continues until the falling edge of the CLK before the conversion begins. On this falling edge the S&H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the +IN pin is sampled and held and can be rapidly time varying. The voltage on the –IN pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR(MAX)} = \left(2\pi f_{(-IN)} V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right)$$

Where $f_{(-IN)}$ is the frequency of the –IN input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. Usually V_{ERROR} will not be significant. For a 60Hz signal on the –IN input to generate a 0.25LSB error (300μV) with the converter running at CLK = 1MHz, its peak value would have to be 66mV. Rearranging the above equation the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-IN)MAX} = \left(\frac{V_{ERROR(MAX)}}{2\pi V_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right)$$

For 0.25LSB error (300μV) the maximum input sinusoid with a 5V peak amplitude that can be digitized is 0.8Hz.

Reference Input

The voltage on the reference input of the LTC1292 determines the voltage span of the A/D converter. The reference input has transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the conversion (every CLK cycle) a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. If slow settling circuitry is used to drive the reference input, take care to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

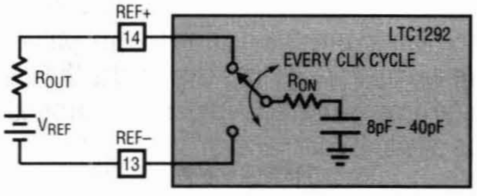


Figure 12. Reference Input Equivalent Circuit

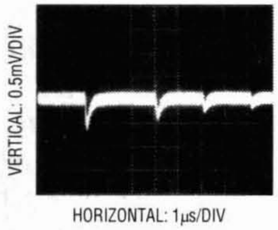


Figure 13. Adequate Reference Settling (LT1027)

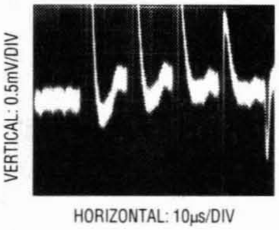


Figure 14. Poor Reference Settling Can Cause A/D Errors

APPLICATIONS INFORMATION

Figures 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 1MHz most references and op amps can be made to settle within the 1μs bit time. For example the LT1027 will settle adequately or with a 10μF bypass capacitor at V_{REF} the LT1021 also can be used.

Reduced Reference Operation

The effective resolution of the LTC1292 can be increased by reducing the input span of the converter. The LTC1292 exhibits good linearity over a range of reference voltages (see typical performance characteristics curves of Change in Linearity vs Reference Voltage). Care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. Offset and Noise are factors that must be considered when operating at low V_{REF} values. The internal reference for V_{REF} has been tied to the GND pin. Any voltage drop from the GND pin to the ground plane will cause a gain error.

Offset with Reduced V_{REF}

The offset of the LTC1292 has a larger effect on the output code when the A/D is operated with a reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristics curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example a V_{OS} of 0.1mV, which is 0.1LSB with a 5V reference becomes 0.4LSB with a 1.25 reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the –IN input to the LTC1292.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1292 can be reduced to approximately 200μV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference input but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristics curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200μV of noise.

For operation with a 5V reference, the 200μV noise is only 0.16LSB peak-to-peak. Here the LTC1292 noise will contribute virtually no uncertainty to the output code. For reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this 200μV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. Now averaging readings may be necessary.

This noise data was taken in a very clean test fixture. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage used, the more critical it becomes to have a noise-free setup.

Gain Error due to Reduced V_{REF}

The gain error of the LTC1292 is very good over a wide range of reference voltages. The error component that is seen in the typical performance characteristics curve Change in Gain Error vs Reference Voltage is due to the voltage drop on the GND pin from the device to the ground plane. To minimize this error the LTC1292 should be soldered directly onto the PC board. The internal reference point for V_{REF} is tied to GND. Any voltage drop in the GND pin will make the reference voltage, internal to the device, less than what is applied externally (Figure 15). This drop is typically 420μV due to the product of the pin resistance (R_{PIN}) and the

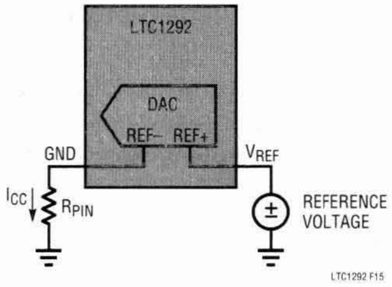


Figure 15. Parasitic Resistance in GND Pin

APPLICATIONS INFORMATION

LTC1292 supply current. For example, with V_{REF} = 1.25V this will result in a gain error change of –1.0LSB from the gain error measured with V_{REF} = 5V.

LTC1292 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/Ds in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "effective number of bits (ENOB)." SNR is the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the non-fundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by:

$$SNR = (6.02N + 1.76dB)$$

where N is the number of bits. Thus the SNR depends on the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. A Fast Fourier Transform (FFT) plot of the output spectrum of the LTC1292 is shown in Figures 16a and 16b. The input (f_{IN}) frequencies are 1kHz and 28kHz with the sampling frequency (f_S) at 58.8 kHz. The SNR obtained from the plot are 73.0dB and 61.5dB.

Rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = \left(\frac{SNR - 1.76dB}{6.02}\right)$$

This is the so-called effective number of bits (ENOB). For the example shown in Figures 16a and 16b, N = 11.8 bits and 9.9 bits, respectively. Figure 17 shows a plot of ENOB as a function of input frequency. The 2nd harmonic distortion term accounts for the degradation of the ENOB as f_{IN} approaches $f_S/2$.

Figure 18 shows a FFT plot of the output spectrum for two tones applied to the input of the A/D. Nonlinearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

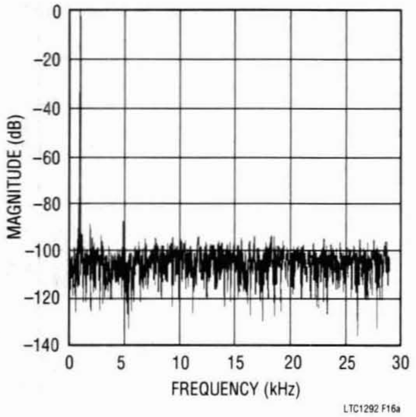


Figure 16a. f_{IN} = 1kHz, f_S = 58.8kHz, SNR = 73.0dB

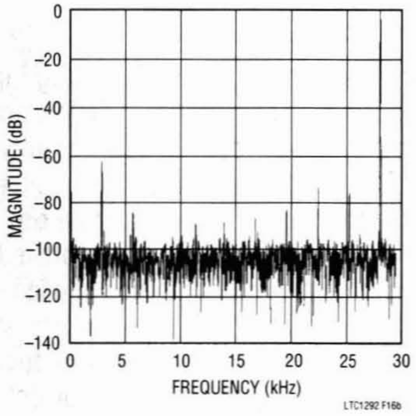


Figure 16b. f_{IN} = 28kHz, f_S = 58.8kHz, SNR = 61.5dB

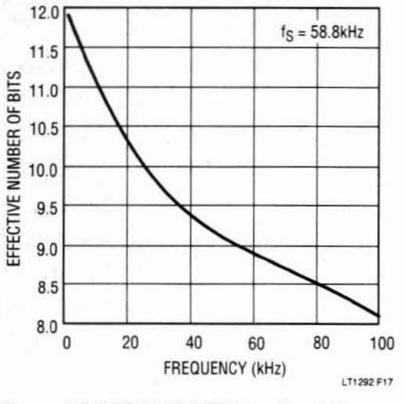


Figure 17. LTC1292 ENOB vs Input Frequency

APPLICATIONS INFORMATION

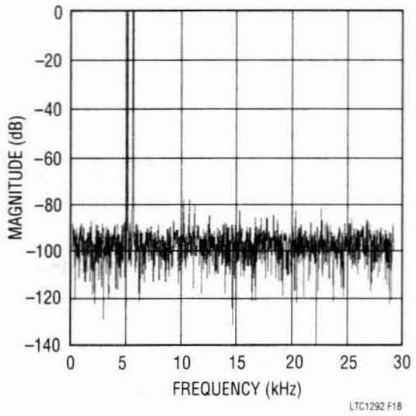


Figure 18. $f_{IN1} = 5.1kHz$, $f_{IN2} = 5.6kHz$, $f_S = 58.8kHz$

Overvoltage Protection

Applying signals to the LTC1292's analog inputs that exceed the positive supply or that go below ground will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog inputs before power is applied to the LTC1292. Another example is the input source is operating from different supplies of larger value than the LTC1292. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. There are two ways to protect the inputs. In Figure 19 diode clamps from the inputs to V_{CC} and GND are used. The second method is to put resistors in series with the analog inputs for current limiting. Limit the current to 15mA per channel. The +IN input can accept a resistor value of 1kΩ but the –IN input cannot accept more than 250Ω when clocked at its maximum clock frequency of 1MHz. If the LTC1292 is clocked at the maximum clock frequency and 250Ω is not enough to current limit the input source then the clamp diodes are recommended (Figures 20a and 20b). The reason for the limit on the resistor value is the MSB bit test is affected by the value of the resistor placed at the –IN input (see discussion on Analog Inputs and the typical performance characteristics Maximum CLK Frequency vs Source Resistance).

If V_{CC} and V_{REF} are not tied together, then V_{CC} should be turned on first, then V_{REF}. If this sequence cannot be met, connecting a diode from V_{REF} to V_{CC} is recommended (see Figure 21).

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

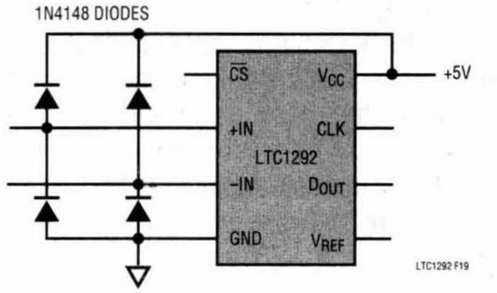


Figure 19. Overvoltage Protection for Inputs

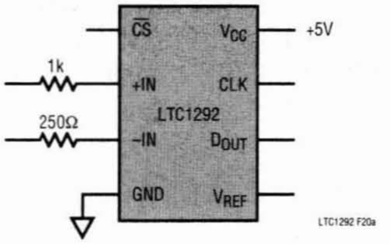


Figure 20a. Overvoltage Protection for Inputs

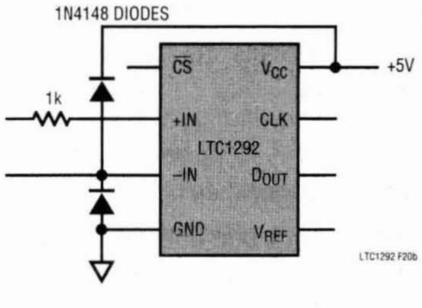


Figure 20b. Overvoltage Protection for Inputs

APPLICATIONS INFORMATION

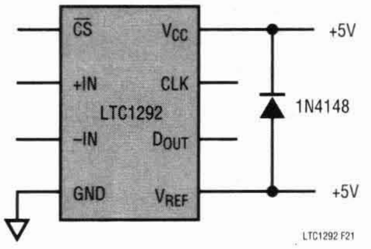

$\overline{CS}$
V_{CC}
+IN
CLK
LTC1292
–IN
D_{OUT}
GND
V_{REF}
+5V
1N4148
+5V
LTC1292 F21

Figure 21

A "Quick Look" Circuit for the LTC1292

Users can get a quick look at the function and timing of the LTC1292 by using the following simple circuit (Figure 22). V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground plane. $\overline{CS}$ is driven at 1/32 the clock rate by the CD4520 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 23). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

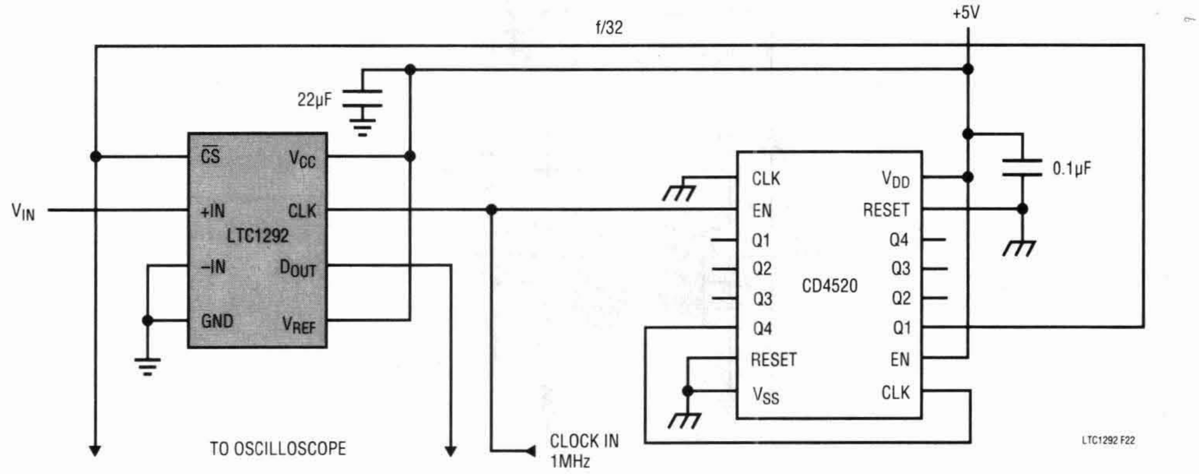

f/32
+5V
22µF
$\overline{CS}$
V_{CC}
V_{IN}
+IN
CLK
LTC1292
–IN
D_{OUT}
GND
V_{REF}
0.1µF
CLK
EN
Q1
Q2
Q3
Q4
RESET
V_{SS}
V_{DD}
RESET
Q4
Q3
Q2
Q1
EN
CLK
CD4520
TO OSCILLOSCOPE
CLOCK IN
1MHz
LTC1292 F22

Figure 22. "Quick Look" Circuit for the LTC1292

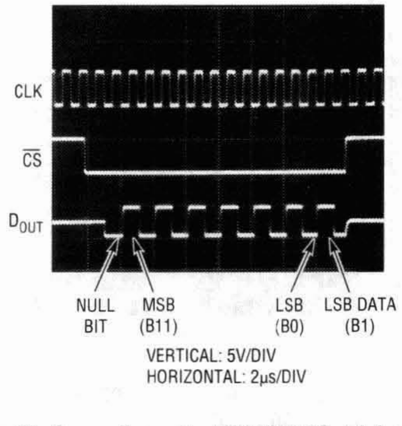


Figure 23. Scope Trace the LTC1292 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

APPLICATIONS INFORMATION

Opto-Isolated Temperature Monitor

Amplification of sensor outputs is often required to generate a signal large enough that can be properly digitized. For example, a J type thermocouple provides only 52µV/°C. The 5µV offset of the LTC1050 chopper op amp generates less than 0.1°C error. Cold junction compensation is provided by the LT1025A. (For more detail see LTC Design Note 5).

In the opto-isolated interface two signals are generated from one. This allows a two-wire interface to the LTC1292. A long high signal (>1ms) on the CLK IN input allows the 0.1µF capacitor to discharge taking $\overline{CS}$ high. This resets the A/D for the next conversion. When CLK IN starts toggling, $\overline{CS}$ goes low and stays there until the next extended CLK IN high time. See Figure 25.

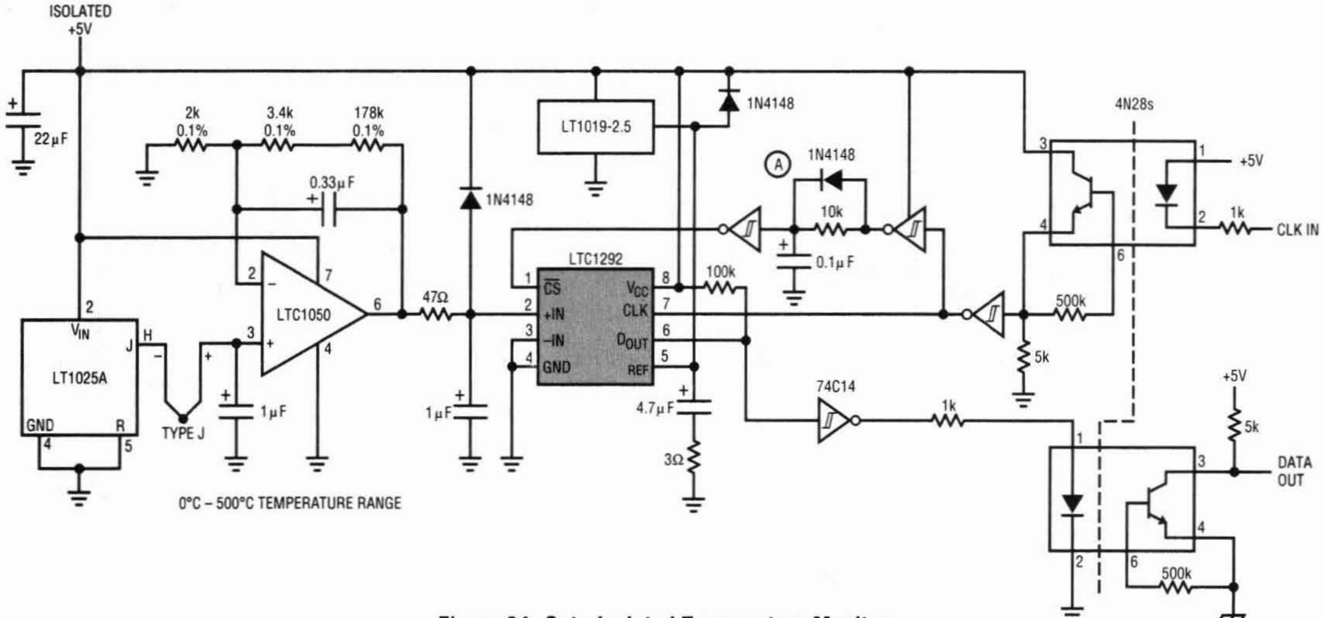

ISOLATED
+5V
22µF
2k
0.1%
3.4k
0.1%
178k
0.1%
0.33µF
LTC1050
47Ω
1N4148
LT1019-2.5
1N4148
Ⓐ
1N4148
10k
0.1µF
LTC1292
$\overline{CS}$
+IN
–IN
GND
V_{CC}
CLK
D_{OUT}
REF
100k
500k
5k
4.7µF
3Ω
74C14
1k
4N28s
+5V
1k
CLK IN
+5V
5k
DATA
OUT
500k
LT1025A
V_{IN}
J
H
GND
R
TYPE J
1µF
1µF
0°C – 500°C TEMPERATURE RANGE
LTC1292 F24

Figure 24. Opto-Isolated Temperature Monitor

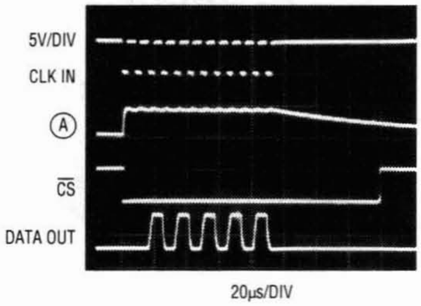


Figure 25. Opto-Isolated Temperature Monitor Digital Waveforms

LTC1293/LTC1294/LTC1296

Single Chip 12-Bit Data Acquisition System

FEATURES

- Software Programmable Features
  - Unipolar/Bipolar Conversion
  - Differential/Single Ended Inputs
  - MSB-First or MSB/LSB Data Sequence
  - Power Shutdown
- Built-In Sample and Hold
- Single Supply 5V or ±5V Operation
- Direct 4-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 46.5kHz Maximum Throughput Rate
- System Shutdown Output (LTC1296)

KEY SPECIFICATIONS

Resolution	12 Bits
Fast Conversion Time	12μs Max Over Temp.
Low Supply Current	6.0mA

DESCRIPTION

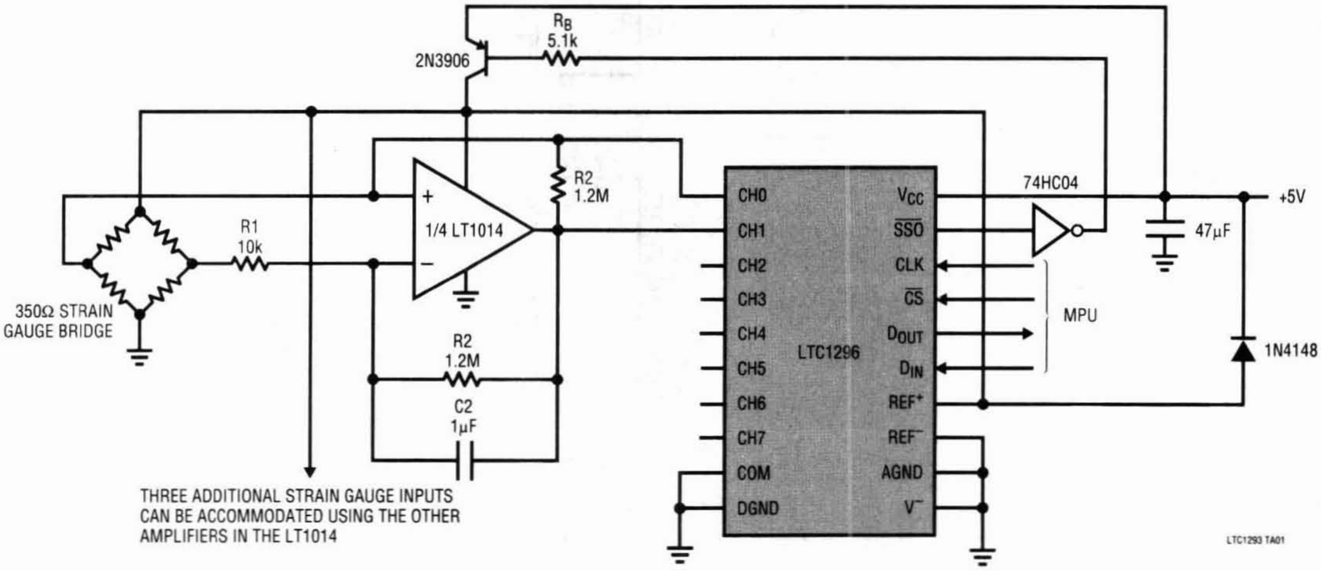
The LTC1293/4/6 is a family of data acquisition systems which contain a serial I/O successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform either 12-bit unipolar, or 11-bit plus sign bipolar A/D conversions. The input multiplexer can be configured for either single ended or differential inputs (or combinations thereof). An on-chip sample and hold is included for all single ended input channels. When the LTC1293/4/6 is idle it can be powered down in applications where low power consumption is desired. The LTC1296 includes a System Shutdown Output pin which can be used to power down external circuitry, such as signal conditioning circuitry prior to the input mux.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing up to eight channels of data to be transmitted over as few as three wires.

LTCMOS™ is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

12-Bit Data Acquisition System with Power Shutdown


R$_B$ 5.1k
2N3906
R2 1.2M
1/4 LT1014
R1 10k
350Ω STRAIN GAUGE BRIDGE
R2 1.2M
C2 1μF
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
LTC1296
V$_{CC}$
$\overline{SSO}$
CLK
$\overline{CS}$
D$_{OUT}$
D$_{IN}$
REF$^+$
REF$^-$
AGND
V$^-$
74HC04
MPU
47μF
+5V
1N4148
LTC1293 TA01

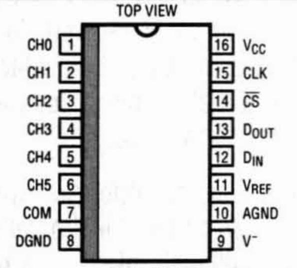
THREE ADDITIONAL STRAIN GAUGE INPUTS CAN BE ACCOMMODATED USING THE OTHER AMPLIFIERS IN THE LT1014

ABSOLUTE MAXIMUM RATINGS (Note 1 and 2)

Supply Voltage (V_{CC}) to GND or V^- 12V
Negative Supply Voltage (V^-) .... −6V to GND
Voltage
  Analog and Reference
    Inputs .... (V^-) −0.3V to V_{CC} + 0.3V
  Digital Inputs .... −0.3V to 12V
  Digital Outputs .... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW

Operating Temperature Range
  LTC1293/4/6BC, LTC1293/4/6CC,
  LTC1293/4/6DC .... 0°C to 70°C
  LTC1293/4/6BI, LTC1293/4/6CI,
  LTC1293/4/6DI .... −40°C to 85°C
  LTC1293/4/6BM, LTC1293/4/6CM,
  LTC1293/4/6DM .... −55°C to 125°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

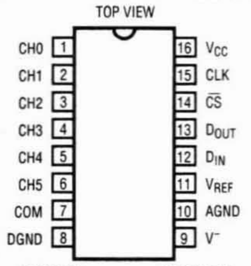
PACKAGE/ORDER INFORMATION


TOP VIEW
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
COM 7
DGND 8
16 V_{CC}
15 CLK
14 $\overline{CS}$
13 D_{OUT}
12 D_{IN}
11 V_{REF}
10 AGND
9 V^-

S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER

LTC1293BCS
LTC1293CCS
LTC1293DCS

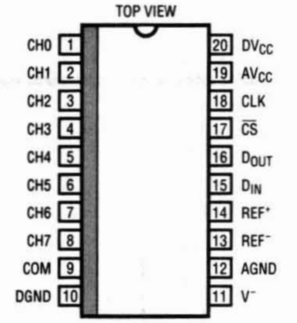

TOP VIEW
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
COM 7
DGND 8
16 V_{CC}
15 CLK
14 $\overline{CS}$
13 D_{OUT}
12 D_{IN}
11 V_{REF}
10 AGND
9 V^-

J PACKAGE
16-LEAD CERAMIC DIP

N PACKAGE
16-LEAD PLASTIC DIP

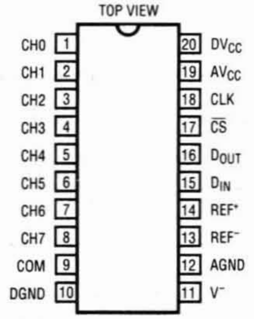
ORDER PART NUMBER

LTC1293BMJ	LTC1293BIN
LTC1293CMJ	LTC1293CIN
LTC1293DMJ	LTC1293DIN
LTC1293BIJ	LTC1293BCN
LTC1293CIJ	LTC1293CCN
LTC1293DIJ	LTC1293DCN


TOP VIEW
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
DGND 10
20 DV_{CC}
19 AV_{CC}
18 CLK
17 $\overline{CS}$
16 D_{OUT}
15 D_{IN}
14 REF^+
13 REF^-
12 AGND
11 V^-

S PACKAGE
20-LEAD PLASTIC SO

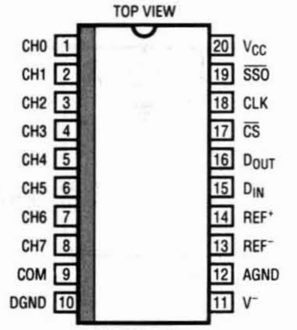
LTC1294BCS
LTC1294CCS
LTC1294DCS


TOP VIEW
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
DGND 10
20 DV_{CC}
19 AV_{CC}
18 CLK
17 $\overline{CS}$
16 D_{OUT}
15 D_{IN}
14 REF^+
13 REF^-
12 AGND
11 V^-

J PACKAGE
20-LEAD CERAMIC DIP

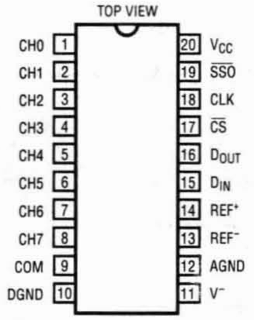
N PACKAGE
20-LEAD PLASTIC DIP

LTC1294BMJ	LTC1294BIN
LTC1294CMJ	LTC1294CIN
LTC1294DMJ	LTC1294DIN
LTC1294BIJ	LTC1294BCN
LTC1294CIJ	LTC1294CCN
LTC1294DIJ	LTC1294DCN


TOP VIEW
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
DGND 10
20 V_{CC}
19 $\overline{SSO}$
18 CLK
17 $\overline{CS}$
16 D_{OUT}
15 D_{IN}
14 REF^+
13 REF^-
12 AGND
11 V^-

S PACKAGE
20-LEAD PLASTIC SO

LTC1296BCS
LTC1296CCS
LTC1296DCS


TOP VIEW
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
DGND 10
20 V_{CC}
19 $\overline{SSO}$
18 CLK
17 $\overline{CS}$
16 D_{OUT}
15 D_{IN}
14 REF^+
13 REF^-
12 AGND
11 V^-

J PACKAGE
20-LEAD CERAMIC DIP

N PACKAGE
20-LEAD PLASTIC DIP

LTC1296BMJ	LTC1296BIN
LTC1296CMJ	LTC1296CIN
LTC1296DMJ	LTC1296DIN
LTC1296BIJ	LTC1296BCN
LTC1296CIJ	LTC1296CCN
LTC1296DIJ	LTC1296DCN

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1293/4/6B MIN	 TYP	 MAX	LTC1293/4/6C MIN	 TYP	 MAX	LTC1293/4/6D MIN	 TYP	 MAX	UNITS
Offset Error	(Note 4)	●			±3.0			±3.0			±3.0	LSB
Linearity Error (INL)	(Notes 4, 5)	●			±0.5			±0.5			±0.75	LSB
Gain Error	(Note 4)	●			±0.5			±1.0			±4.0	LSB
Minimum Resolution for which No Missing Codes are Guaranteed		●			12			12			12	Bits
Analog and REF Input Range	(Note 7)		(V^-)–0.05V to V_{CC} + 0.05V									V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA
Off Channel Lekage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA

AC CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1293/4/6B LTC1293/4/6C LTC1293/4/6D MIN	 TYP	 MAX	UNITS
f_{CLK}	Clock Frequency	V_{CC} = 5V (Note 6)		0.1		1.0	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			2.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		21 CLK +500ns			Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		160	300	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		80	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		80	200	ns
t_{hDI}	Hold Time, D_{IN} after CLK↑	V_{CC} = 5V (Note 6)		50			ns
t_{hDO}	Time Output Data Remains Valid After CLK↓				130		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	50	ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V (Note 6)		300			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 5V (Note 6)		400			ns
t_{suDI}	Set-up Time, D_{IN} Stable Before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{su\overline{CS}}$	Set-up Time, $\overline{CS}$↓ before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{wH\overline{CS}}$	CS High Time During Conversion	V_{CC} = 5V (Note 6)		500			ns
$t_{wL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V (Note 6)		21			CLK Cycles
$t_{en\overline{SSO}}$	Delay Time, CLK↓ to $\overline{SSO}$↓	See Test Circuits	●		750	1500	ns
$t_{dis\overline{SSO}}$	Delay Time, $\overline{CS}$↓ to $\overline{SSO}$↑	See Test Circuits	●		250	500	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Analog Inputs Off Channel Digital Inputs			100 5 5		pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 3)

					LTC1293/4/6B LTC1293/4/6C LTC1293/4/6D			
SYMBOL	**PARAMETER**	**CONDITIONS**			**MIN**	**TYP**	**MAX**	**UNITS**
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V		●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V		●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$		●			2.5	μA
I_{IL}	Low Level Input Current	V_{IN} = 0V		●			−2.5	μA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = −10mA I_O = 360μA		 ●	 2.4	4.7 4.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA		●			0.4	V
I_{OZ}	High Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High		● ●			3 −3	μA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V				−20		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$				20		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High		●		6	12	mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High, Power Shutdown	LTC1294BC, LTC1294CC, LTC1294DC, LTC1294BI, LTC1294CI, LTC1294DI,	●		5	10	μA
		CLK Off	LTC1294BM, LTC1294CM, LTC1294DM	●		5	15	μA
I_{REF}	Reference Current	$\overline{CS}$ High		●		10	50	μA
I^-	Negative Supply Current	$\overline{CS}$ High		●		1	50	μA
$I_{SOURCEs}$	$\overline{SSO}$ Source Current	$V_{\overline{SSO}}$ = 0V		●	0.8	1.5		mA
I_{SINKs}	$\overline{SSO}$ Sink Current	$V_{\overline{SSO}} = V_{CC}$		●	0.5	1.0		mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to DGND, AGND and REF^- wired together (unless otherwise noted).

Note 3: V_{CC} = 5V, V_{REF+} = 5V, V_{REF-} = 0V, V^- = 0V for unipolar mode and −5V for bipolar mode, CLK = 1.0MHz unless otherwise specified. The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 4: These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ($2V_{REF}$) divided by 4096. For example, when V_{REF} = 5V, 1LSB (bipolar) = 2 (5V)/4096 = 2.44mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve. The deviation is measured from the center of the quantization band.

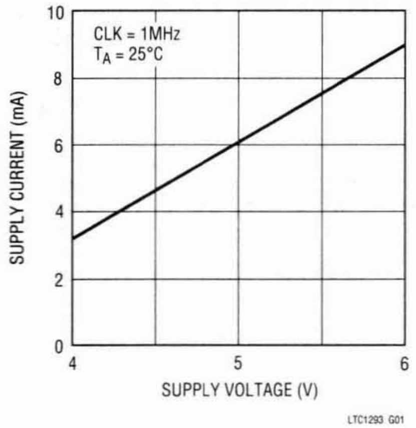
Note 6: Recommended operating conditions.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below V^- or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

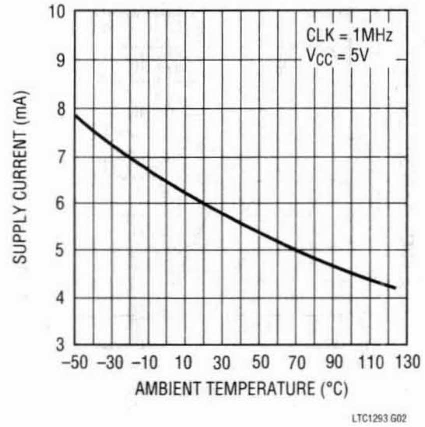
Note 8: Channel leakage current is measured after the channel selection.

TYPICAL PERFORMANCE CHARACTERISTICS

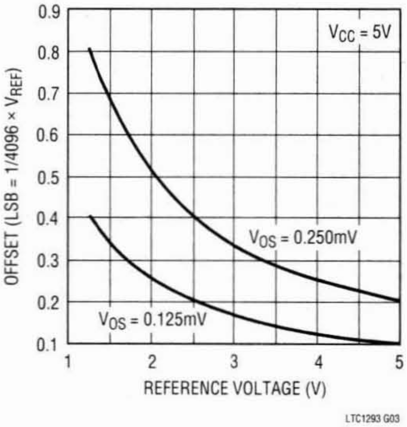
Supply Current vs Supply Voltage



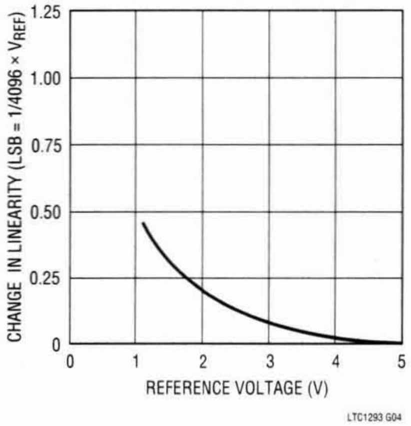
Supply Current vs Temperature



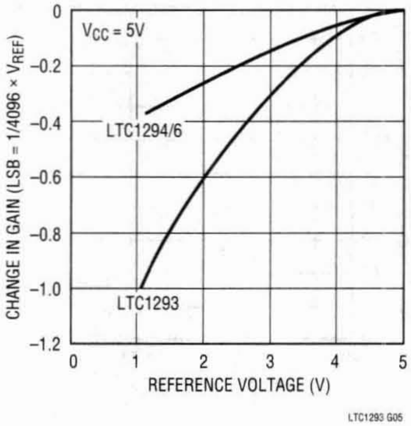
Unadjusted Offset Voltage vs Reference Voltage



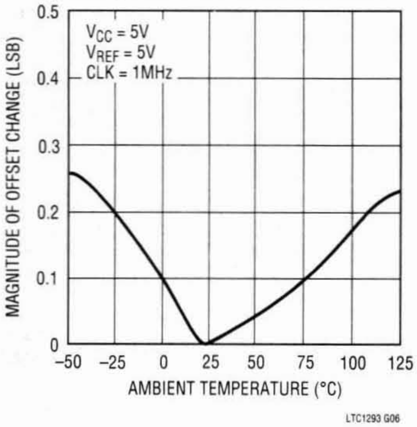
Change in Linearity vs Reference Voltage



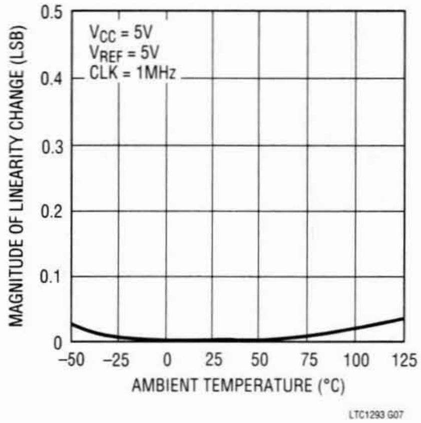
Change in Gain vs Reference Voltage



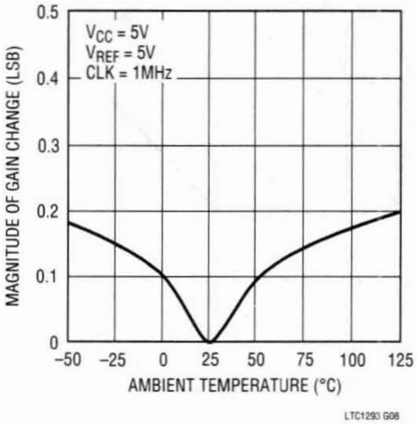
Change in Offset vs Temperature



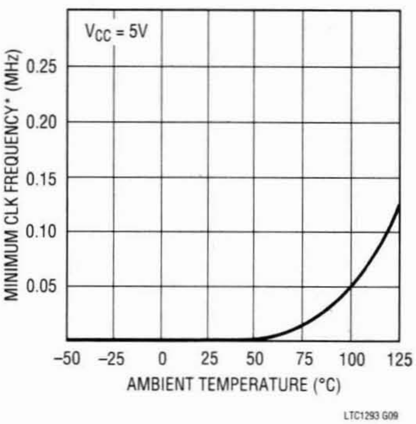
Change in Linearity vs Temperature



Change in Gain vs Temperature

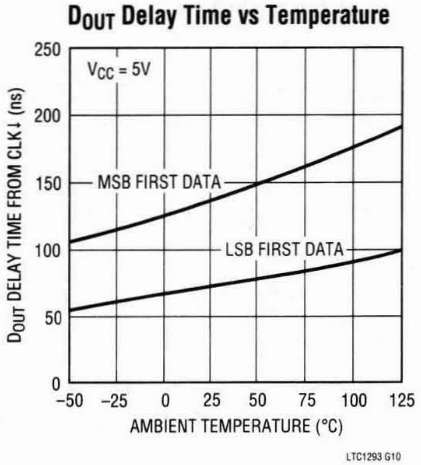


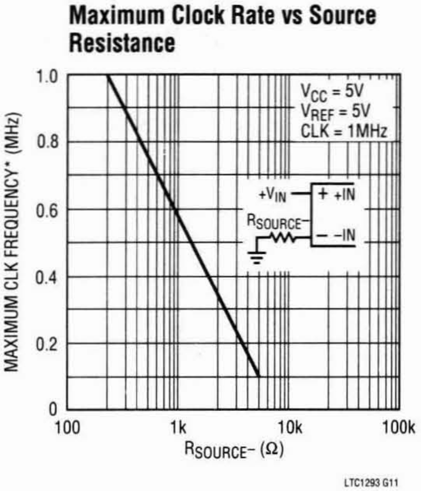
Minimum Clock Rate for 0.1LSB Error

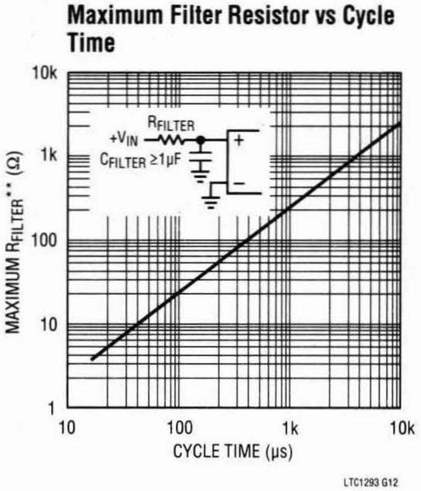


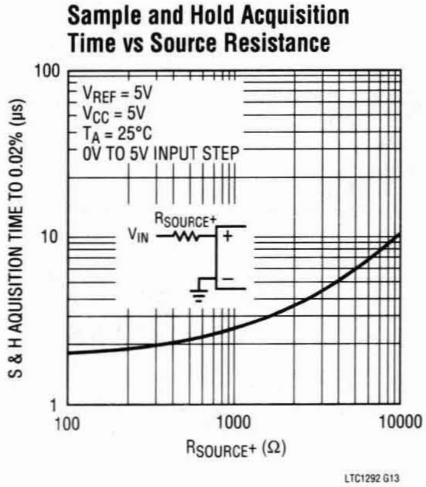
* AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

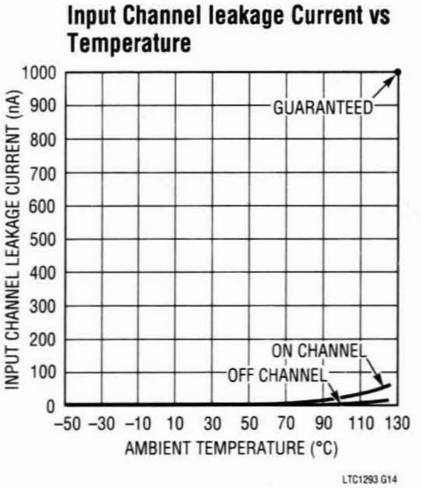
TYPICAL PERFORMANCE CHARACTERISTICS

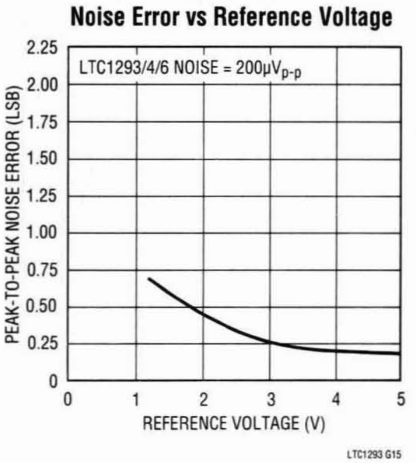

D_{OUT} Delay Time vs Temperature

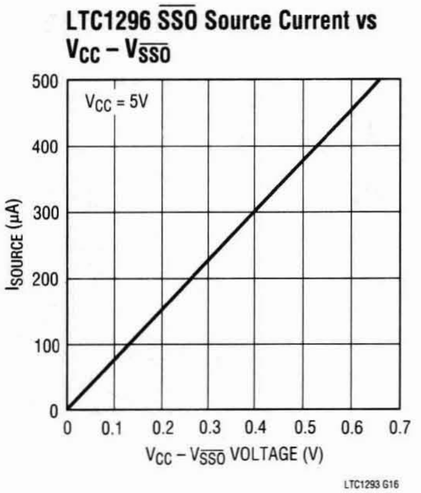

Maximum Clock Rate vs Source Resistance

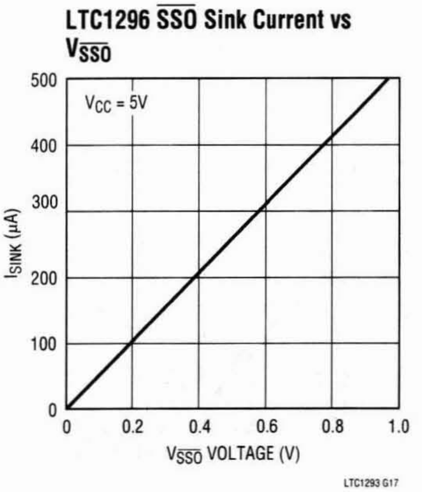

Maximum Filter Resistor vs Cycle Time


Sample and Hold Acquisition Time vs Source Resistance


Input Channel leakage Current vs Temperature


Noise Error vs Reference Voltage


LTC1296 $\overline{SSO}$ Source Current vs $V_{CC} - V_{\overline{SSO}}$


LTC1296 $\overline{SSO}$ Sink Current vs $V_{\overline{SSO}}$

* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED.

** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0Ω IS FIRST DETECTED.

PIN FUNCTIONS

LTC1293

#	PIN	FUNCTION	DESCRIPTION
1 – 6	CH0 – CH5	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
7	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
8	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
9	V^-	Negative Supply	Tie V^- to most negative potential in the circuit (Ground in single supply applications).
10	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
11	V_{REF}	Ref. Input	The reference inputs must be kept free of noise with respect to AGND.
12	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
13	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
14	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
15	CLK	Clock	This clock synchronizes the serial data transfer and controls A/D conversion rate.
16	V_{CC}	Positive supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

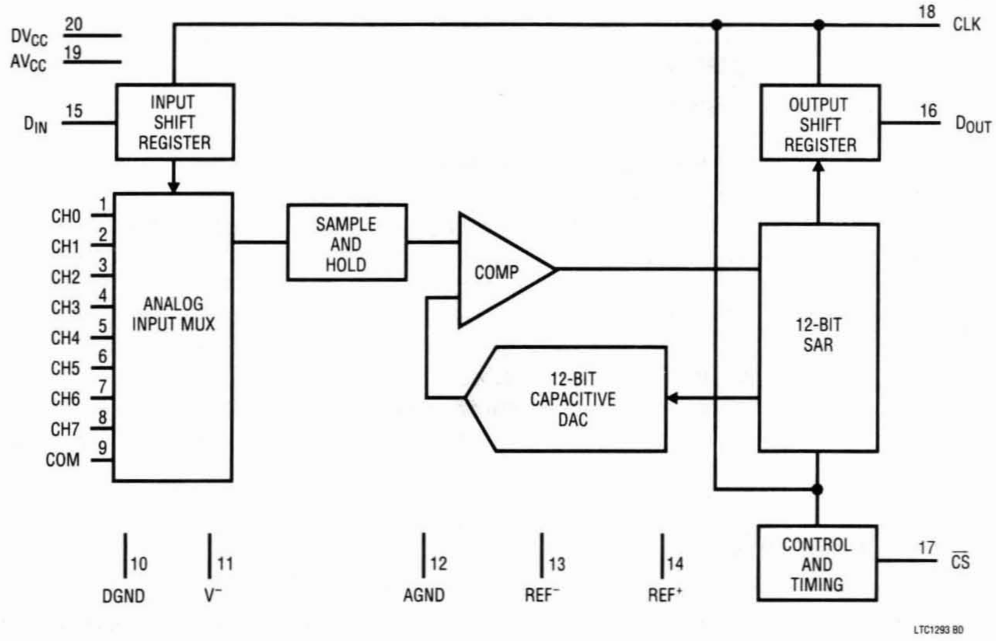
LTC1294

#	PIN	FUNCTION	DESCRIPTION
1 –8	CH0 – CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	V^-	Negative Supply	Tie V^- to most negative potential in the circuit (Ground in single supply applications).
12	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
13, 14	REF^-, REF^+	Ref. Inputs	The reference inputs must be kept free of noise with respect to AGND. The A/D sees a reference voltage equal to the difference between REF^+ and REF^-.
15	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
18	CLK	Clock	This clock synchronizes the serial data transfer and controls A/D converion rate.
19, 20	AV_{CC}, DV_{CC}	Positive Supplies	These supplies must be kept free of noise and ripple by bypassing directly to the analog ground plane. AV_{CC} and DV_{CC} must be tied together.

LTC1296

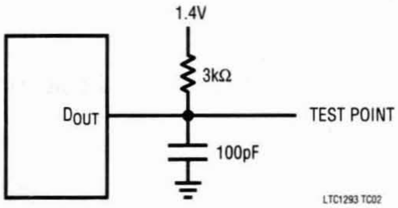
#	PIN	FUNCTION	DESCRIPTION
1 –8	CH0 – CH7	Analog Inputs	The analog inputs must be free of noise with respect to AGND.
9	COM	Common	The common pin defines the zero reference point for all single ended inputs. It must be free of noise and is usually tied to the analog ground plane.
10	DGND	Digital Ground	This is the ground for the internal logic. Tie to the ground plane.
11	V^-	Negative Supply	Tie V^- to most negative potential in the circuit (Ground in single supply applications).
12	AGND	Analog Ground	AGND should be tied directly to the analog ground plane.
13, 14	REF^-, REF^+	Ref. Inputs	The reference inputs must be kept free of noise with respect to AGND. The A/D sees a reference voltage equal to the difference between REF^+ and REF^-.
15	D_{IN}	Data Input	The A/D configuration word is shifted into this input.
16	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
17	$\overline{CS}$	Chip Select Input	A logic low on this input enables data transfer.
18	CLK	Clock	This clock synchronizes the serial data transfer and controls A/D conversion rate.
19	$\overline{SSO}$	System Shutdown Output	System Shutdown Output pin will go low when power shutdown is requested.
20	V_{CC}	Positive Supply	This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM (Pin numbers refer to LTC1294)

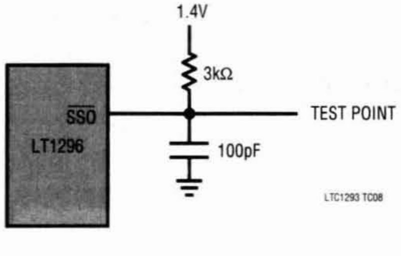

DVCC 20
AVCC 19
DIN 15
INPUT SHIFT REGISTER
CH0 1
CH1 2
CH2 3
CH3 4
CH4 5
CH5 6
CH6 7
CH7 8
COM 9
ANALOG INPUT MUX
SAMPLE AND HOLD
COMP
12-BIT CAPACITIVE DAC
12-BIT SAR
OUTPUT SHIFT REGISTER
18 CLK
16 DOUT
CONTROL AND TIMING
17 CS̅
10 DGND
11 V⁻
12 AGND
13 REF⁻
14 REF⁺
LTC1293 BD

TEST CIRCUITS

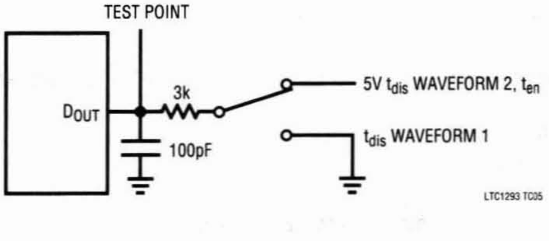
Load Circuit for t_{dDO}, t_r and t_f


1.4V
3kΩ
DOUT
TEST POINT
100pF
LTC1293 TC02

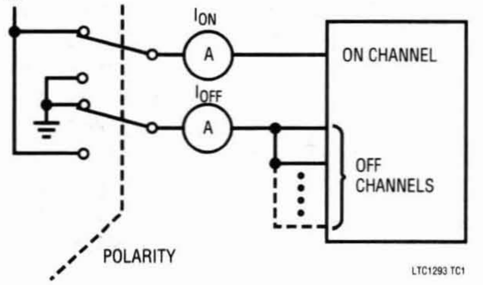
Load Circuit for t_{enSSO} and $t_{dis\overline{SSO}}$


1.4V
3kΩ
SSO̅
LT1296
TEST POINT
100pF
LTC1293 TC08

Load Circuit for t_{dis} and t_{en}

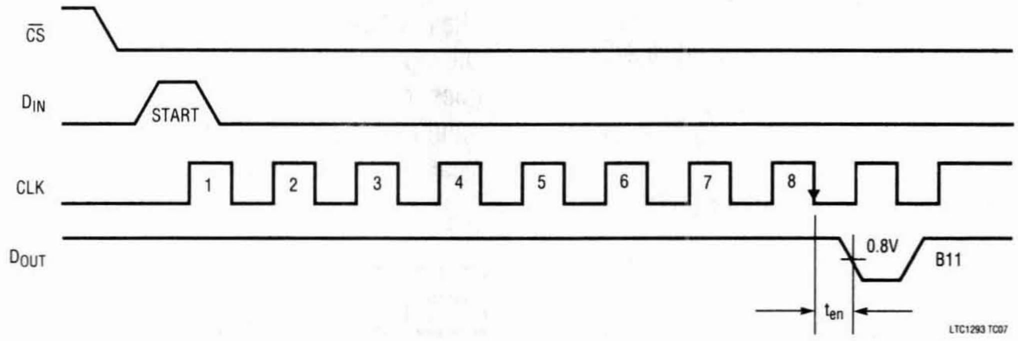

TEST POINT
DOUT
3k
100pF
5V tdis WAVEFORM 2, ten
tdis WAVEFORM 1
LTC1293 TC05

On and Off Channel Leakage Current


5V
ION
A
IOFF
A
ON CHANNEL
OFF CHANNELS
POLARITY
LTC1293 TC1

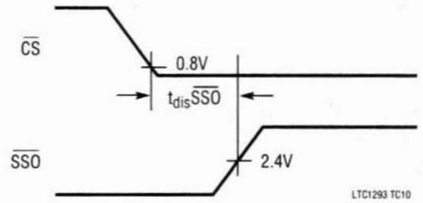
TEST CIRCUITS

Voltage Waveforms for t_{en}



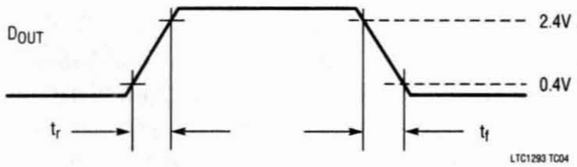
$\overline{CS}$
D_{IN}
START
CLK
1
2
3
4
5
6
7
8
D_{OUT}
0.8V
B11
t_{en}
LTC1293 TC07

Voltage Waveform for $t_{dis\overline{SSO}}$



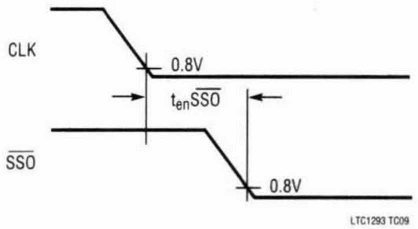
$\overline{CS}$
0.8V
$t_{dis}\overline{SSO}$
$\overline{SSO}$
2.4V
LTC1293 TC10

Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f



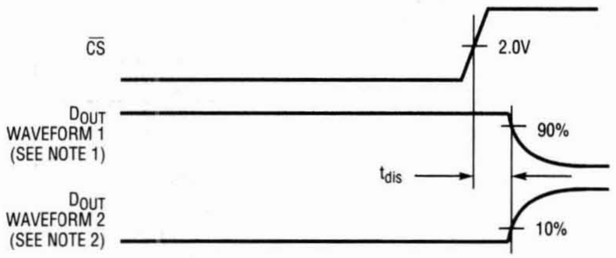
D_{OUT}
2.4V
0.4V
t_r
t_f
LTC1293 TC04

Voltage Waveform for for $t_{en\overline{SSO}}$



CLK
0.8V
$t_{en}\overline{SSO}$
$\overline{SSO}$
0.8V
LTC1293 TC09

Voltage Waveform for t_{dis}

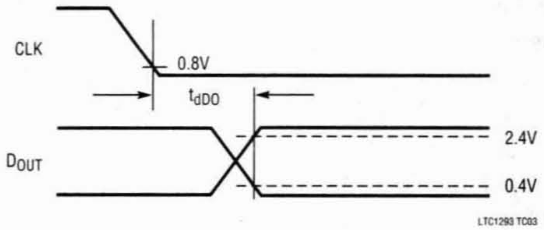


$\overline{CS}$
2.0V
D_{OUT} WAVEFORM 1 (SEE NOTE 1)
90%
t_{dis}
D_{OUT} WAVEFORM 2 (SEE NOTE 2)
10%

NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

LTC1293 TC06

Voltage Waveform for D_{OUT} Delay Time, t_{dDO}



CLK
0.8V
t_{dDO}
D_{OUT}
2.4V
0.4V
LTC1293 TC03

APPLICATIONS INFORMATION

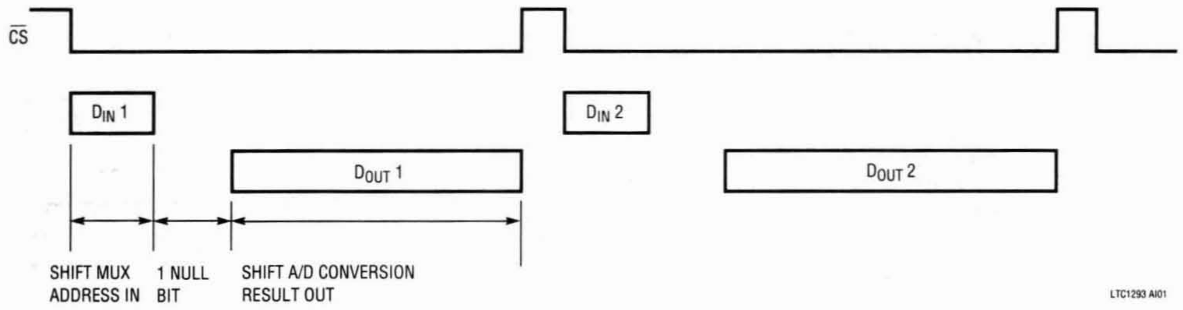
The LTC 1293/4/6 is a data acquisition component which contains the following functional blocks:

1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample and hold (S/H)
4. Synchronous, half duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

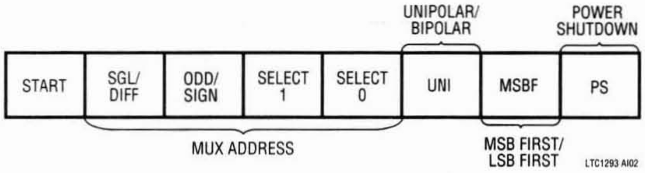
Serial Interface

The LTC1293/4/6 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four-wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The input data is first received and then the A/D conversion result is transmitted (half duplex). Because of the half duplex operation D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wired: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}). Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1293/4/6 looks for a start bit. After the start bit is received a 7-bit input word is shifted into the D_{IN} input which configures the LTC1293/4/6 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. With the half duplex serial interface the D_{OUT} data is from the current conversion. After the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1293/4/6 in preparation for the next data exchange.



INPUT DATA WORD

The LTC1293/4/6 seven-bit data word is clocked into the D_{IN} input on the rising edge of the clock after chip select goes low and the start bit has been recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The input word is defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeroes which precede this logical one will be ignored. After the start bit is received the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

MUX Address

The four bits of the input word following the START BIT assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of the following table. Note that in differential mode (SGL/DIFF = 0) measurements are limited to four adjacent input pairs with either polarity. In single ended mode, all input channels are measured with respect to COM. Only the +inputs have sample and holds. Signals applied at the –inputs must not change more than the required accuracy during the conversion.

APPLICATIONS INFORMATION

Table 1a. LTC1294/6 Multiplexer Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION								MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION								
SGL/ DIFF	ODD SIGN	SELECT		0	1	2	3	4	5	6	7	SGL/ DIFF	ODD SIGN	SELECT		0	1	2	3	4	5	6	7	COM
		1	0											1	0									
0	0	0	0	+	−							1	0	0	0	+								−
0	0	0	1			+	−					1	0	0	1			+						−
0	0	1	0					+	−			1	0	1	0					+				−
0	0	1	1							+	−	1	0	1	1							+		−
0	1	0	0	−	+							1	1	0	0		+							−
0	1	0	1			−	+					1	1	0	1				+					−
0	1	1	0					−	+			1	1	1	0						+			−
0	1	1	1							−	+	1	1	1	1								+	−

Table 1b. LTC1293 Channel Selection

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION						MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION						
SGL/ DIFF	ODD SIGN	SELECT		0	1	2	3	4	5	SGL/ DIFF	ODD SIGN	SELECT		0	1	2	3	4	5	COM
		1	0									1	0							
0	0	0	0	+	−					1	0	0	0	+						−
0	0	0	1			+	−			1	0	0	1			+				−
0	0	1	0					+	−	1	0	1	0					+		−
0	0	1	1	Not Used						1	0	1	1	Not Used						
0	1	0	0	−	+					1	1	0	0		+					−
0	1	0	1			−	+			1	1	0	1				+			−
0	1	1	0					−	+	1	1	1	0						+	−
0	1	1	1	Not Used						1	1	1	1	Not Used						

Unipolar/Bipolar (UNI)

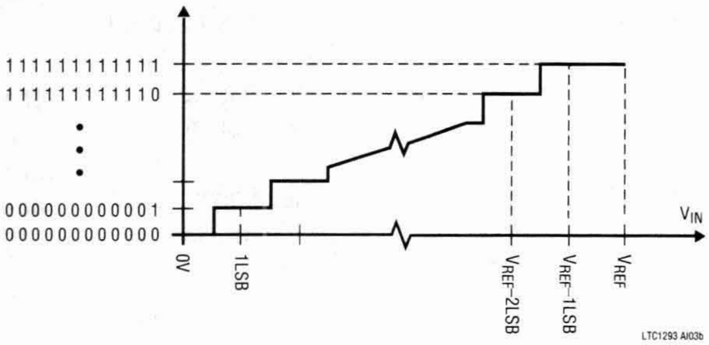
The UNI bit determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below:

Unipolar Transfer Curve (UNI = 1)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (VREF = 5V)
111111111111	V_{REF} − 1LSB	4.9988V
111111111110	V_{REF} − 2LSB	4.9976V
•	•	•
•	•	•
•	•	•
000000000001	1LSB	0.0012V
000000000000	0V	0V

LTC1293 AI03a

Unipolar Output Code (UNI = 1)



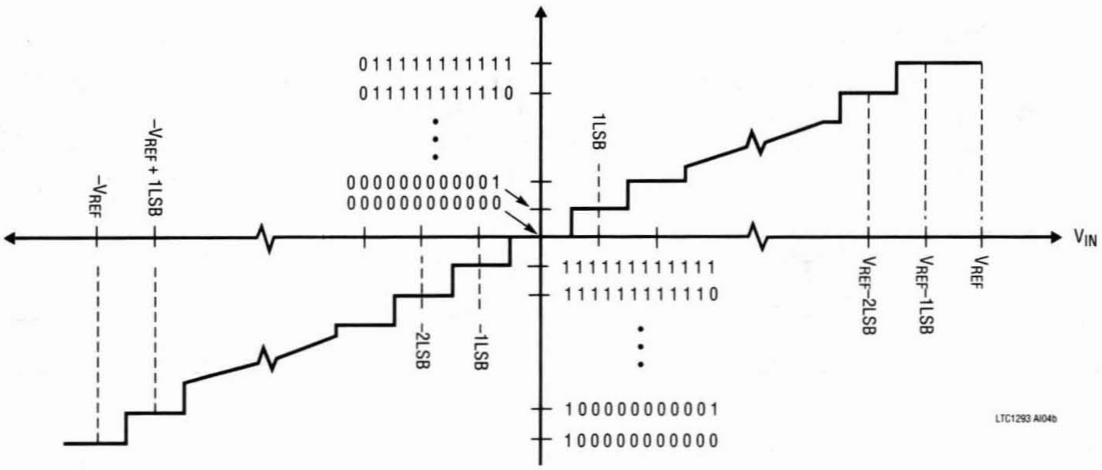
APPLICATIONS INFORMATION

Bipolar Transfer Curve (UNI = 0)

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)	OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
011111111111	V_{REF} – 1LSB	4.9976V	111111111111	–1LSB	–0.0024V
011111111110	V_{REF} – 2LSB	4.9851V	111111111110	–2LSB	–0.0048V
•	•	•	•	•	•
•	•	•	•	•	•
•	•	•	•	•	•
000000000001	1LSB	0.0024V	100000000001	–(V_{REF}) + 1LSB	–4.9976V
000000000000	0V	0V	100000000000	– (V_{REF})	–5.00000V

LTC1293 AI04a

Bipolar Output Code (UNI = 0)



The following discussion will demonstrate how the two reference pins are to be used in conjunction with the analog input multiplexer. In unipolar mode the input span of the A/D is set by the difference in voltage on the REF^+ pin and the REF^- pin. In the bipolar mode the input span is twice the difference in voltage on the REF^+ pin and the REF^- pin. In the unipolar mode the lower value of the input span is set by the voltage on the COM pin for single-ended inputs and by the voltage on the minus input pin for differential inputs. For the bipolar mode of operation the voltage on the COM pin or the minus input pin set the center of the input span.

The upper and lower value of the input span can now be summarized in the following table:

INPUT CONFIGURATION		UNIPOLAR MODE	BIPOLAR MODE
Single-Ended	Lower Value	COM	$-(REF^+ - REF^-) + COM$
	Upper Value	$(REF^+ - REF^-) + COM$	$(REF^+ - REF^-) + COM$
Differential	Lower Value	IN^-	$-(REF^+ - REF^-) + IN^-$
	Upper Value	$(REF^+ - REF^-) + IN^-$	$(REF^+ - REF^-) + IN^-$

The reference voltages REF^+ and REF^- can fall between V_{CC} and V^-, but the difference $(REF^+ - REF^-)$ must be less than or equal to V_{CC}. The input voltages must be less than or equal to V_{CC} and greater than or equal to V^-. For the LTC1293 REF^- = 0V.

The following examples are for a single-ended input configuration.

Example 1: Let V_{CC} = 5V, V^- = 0V, REF^+ = 4V, REF^- = 1V and COM = 0V. Unipolar mode of operation. The resulting input span is $0V \le IN^+ \le 3V$.

APPLICATIONS INFORMATION

Example 2: The same conditions as Example 1 except COM = 1V. The resulting input span is $1V \leq IN^+ \leq 4V$. Note if $IN^+ \geq 4V$ the resulting D_{OUT} word is all 1's. If $IN^+ \leq 1V$ then the resulting D_{OUT} word is all 0's.

Example 3: Let $V_{CC} = 5V$, $V^- = -5V$, $REF^+ = 4V$, $REF^- = 1V$ and COM = 1V. Bipolar mode of operation. The resulting input span is $-2V \leq IN^+ \leq 4V$.

For differential input configurations with the same conditions as in the above three examples the resulting input spans are as follows:

Example 1 (Diff.): $IN^- \leq IN^+ \leq IN^- + 3V$.
Example 2 (Diff.): $IN^- \leq IN^+ \leq IN^- + 3V$.
Example 3 (Diff.): $IN^- - 3V \leq IN^+ \leq IN^- + 3V$.

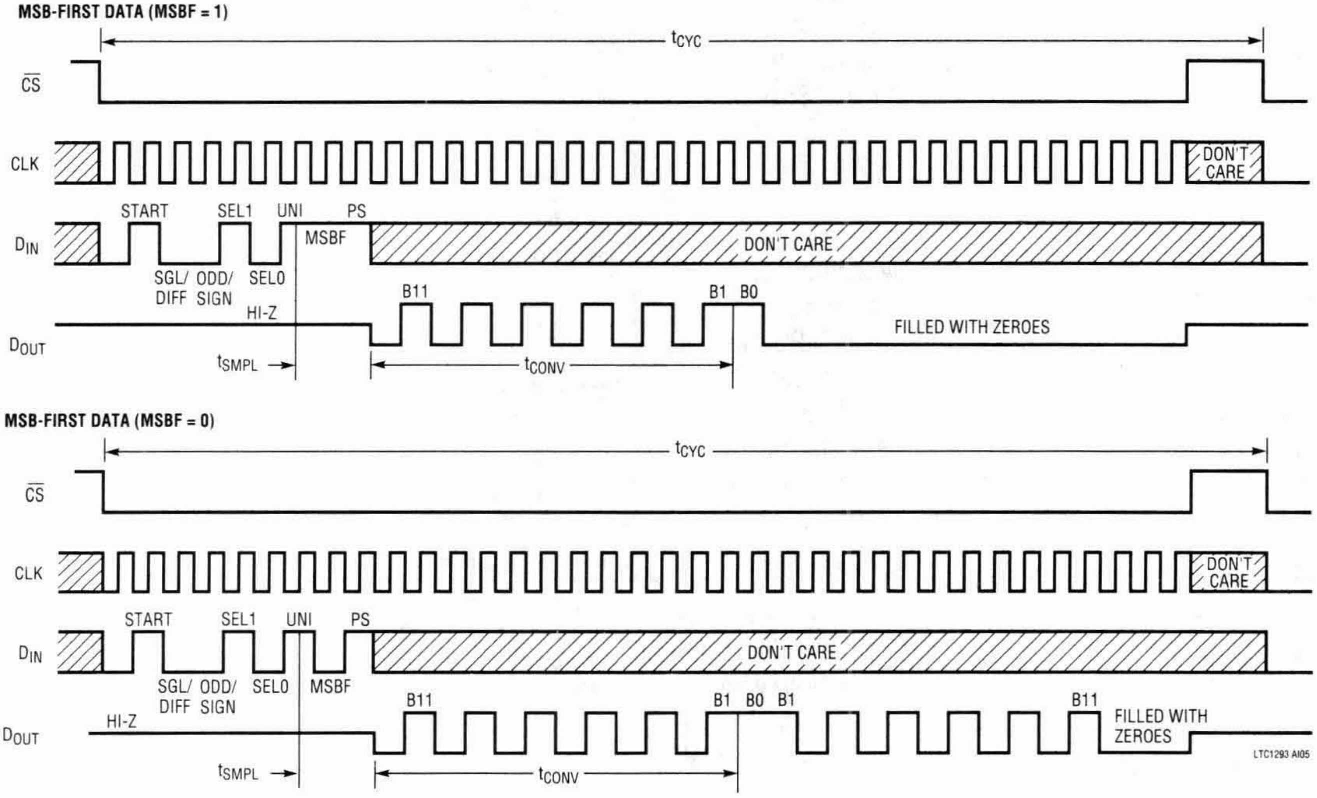
MSB-First/LSB-First (MSBF)

The output data of the LTC1293/4/6 is programmed for MSB-first or LSB-first sequence using the MSB bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB-first format. Logical zeroes will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line. In the bipolar mode the sign bit will fill in after the MSB bit for MSBF = 0 (see Operating Sequence).

Power Shutdowns (PS)

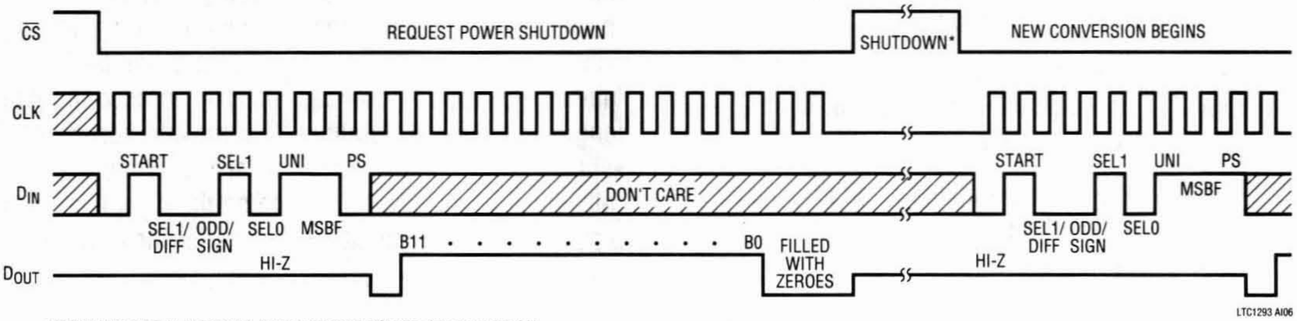
The power shutdown feature of the LTC1293/4/6 is activated by making the PS bit a logical zero. If $\overline{CS}$ remains low after the PS bit has been received, a 12-bit D_{OUT} word with

Operating Sequence
Example: Differential Inputs ($CH4^+$, $CH5^-$), Unipolar Mode


MSB-FIRST DATA (MSBF = 1)
tCYC
CS
CLK
DON'T CARE
START
SEL1
UNI
PS
DIN
MSBF
DON'T CARE
SGL/ DIFF
ODD/ SIGN
SEL0
HI-Z
B11
B1
B0
DOUT
FILLED WITH ZEROES
tSMPL
tCONV
MSB-FIRST DATA (MSBF = 0)
tCYC
CS
CLK
DON'T CARE
START
SEL1
UNI
PS
DIN
DON'T CARE
SGL/ DIFF
ODD/ SIGN
SEL0
MSBF
HI-Z
B11
B1
B0
B1
B11
DOUT
FILLED WITH ZEROES
tSMPL
tCONV
LTC1293 AI05

APPLICATIONS INFORMATION

Power Shutdown Operating Sequence
Example: Differential Inputs ($CH4^+$, $CH5^-$), Unipolar Mode and MSB-First Data



*STOPPING THE CLOCK WILL HELP REDUCE POWER CONSUMPTION.
$\overline{CS}$ CAN BE BROUGHT HIGH ONCE THE DIN WORD HAS BEEN CLOCKED IN.

all logical ones will be shifted out followed by logical zeroes till $\overline{CS}$ goes high. Then the D_{OUT} line will go into its high impedance state. The LTC 1293/4/6 will remain in the shutdown mode till the next $\overline{CS}$ cycle. There is no warm-up or wait period required after coming out of the power shutdown cycle so a conversion can commence after $\overline{CS}$ goes low (see Power Shutdown Operating Sequence). The LTC1296 has a System Shutdown Output pin ($\overline{SSO}$) which will go low when power shutdown is activated. The pin will stay low till next $\overline{CS}$ cycle.

Microprocessor Interfaces

The LTC1293/4/6 can interface directly (without external hardware) to most popular microprocessors (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1293/4/6. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Microprocessor Interfaces

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Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1293/4/6**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MCROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

* Requires external hardware
** Contact factory for interface information for processors not on this list
† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

APPLICATIONS INFORMATION

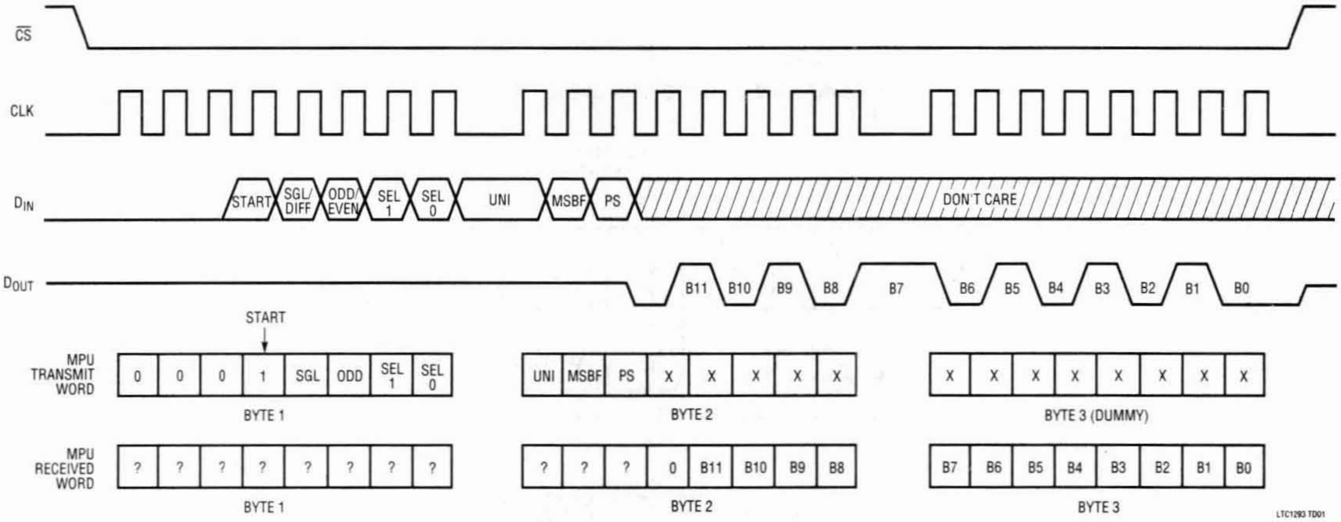
Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts the SPI process. With three 8-bit transfers, the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits B7 through B0 into the MPU. The data is right justified in the two memory locations. ANDing the second byte with $0D_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to show the interface between the LTC1293/4/6 and parallel port microprocessors. Usually the signals $\overline{CS}$, D_{IN} and CLK are generated on three port lines and the D_{OUT} signal is read on a fourth port line. This works very well. One can save a line by tying the D_{IN} and D_{OUT} lines together. The 8051 first sends the start bit and D_{IN} to the LTC1294 over the line connected to P1.2. Then P1.2 is reconfigured as an input and the 8051 reads back the 12-bit A/D result over the same data line.

Data Exchange Between LTC1294 and MC68HC11


CS
CLK
DIN
START
SGL/DIFF
ODD/EVEN
SEL 1
SEL 0
UNI
MSBF
PS
DON'T CARE
DOUT
B11
B10
B9
B8
B7
B6
B5
B4
B3
B2
B1
B0
START
MPU TRANSMIT WORD
MPU RECEIVED WORD
LTC1293 TD01

MPU TRANSMIT WORD

BYTE 1							
0	0	0	1	SGL	ODD	SEL 1	SEL 0

BYTE 2							
UNI	MSBF	PS	X	X	X	X	X

BYTE 3 (DUMMY)							
X	X	X	X	X	X	X	X

MPU RECEIVED WORD

BYTE 1							
?	?	?	?	?	?	?	?

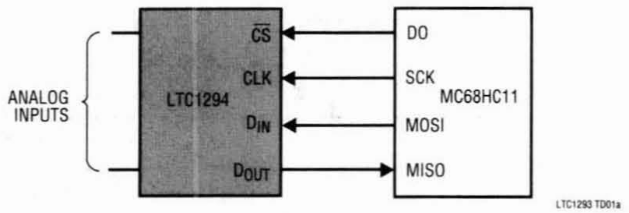
BYTE 2							
?	?	?	0	B11	B10	B9	B8

BYTE 3							
B7	B6	B5	B4	B3	B2	B1	B0

Hardware and Software Interface to Motorola MC68HC11

D_{OUT} FROM LTC1294 STORED ON MC68HC11 RAM

	MSB							LSB	
#62	0	0	0	0	B11	B10	B9	B8	BYTE 1
#63	B7	B6	B5	B4	B3	B2	B1	B0	BYTE 2

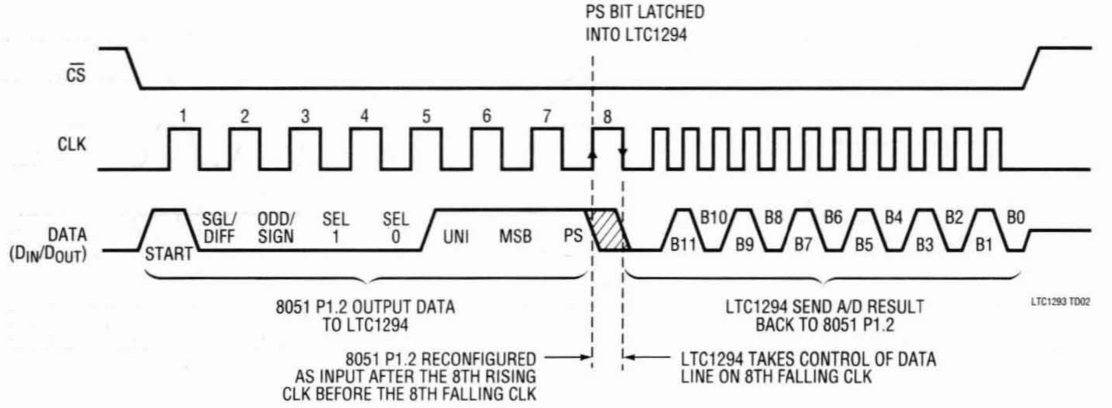

ANALOG INPUTS
LTC1294
CS
CLK
DIN
DOUT
DO
SCK
MOSI
MISO
MC68HC11
LTC1293 TD01a

APPLICATIONS INFORMATION

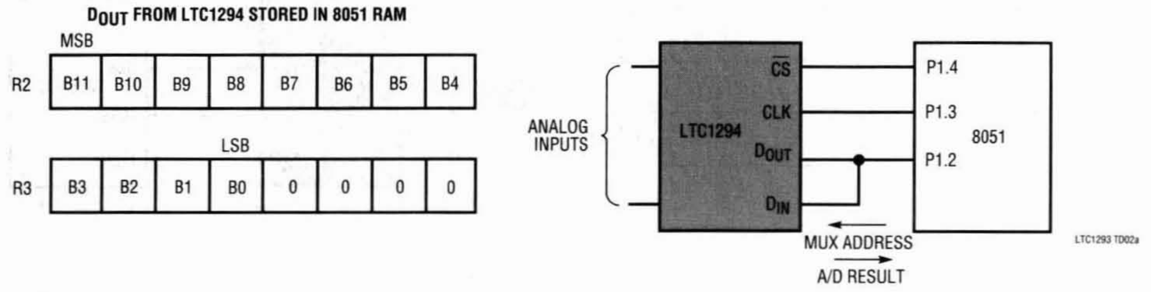
MC68HC11 CODE

LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR
	STAA	$1028	LOAD DATA INTO SPCR ($1028)
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR
	STAA	$1009	LOAD DATA INTO PORT D DDR
	LDAA	#$10	LOAD DIN WORD INTO ACC A
	STAA	$50	LOAD DIN DATA INTO $50
	LDAA	#$E0	LOAD DIN WORD INTO ACC A
	STAA	$51	LOAD DIN DATA INTO $51
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A
	STAA	$52	LOAD DUMMY DIN DATA INTO $52
	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000
LOOP	BCLR	$08,X,$01	D0 GOES LOW ($\overline{CS}$ GOES LOW)
	LDAA	$50	LOAD DIN INTO ACC A FROM $50
	STAA	$102A	LOAD DIN INTO SPI, START SCK
	LDAA	$1029	CHECK SPI STATUS REG
WAIT1	BPL	WAIT1	CHECK IF TRANSFER IS DONE
	LDAA	$51	LOAD DIN INTO ACC A FROM $51
	STAA	$102A	LOAD DIN INTO SPI, START SCK
WAIT2	LDAA	$1029	CHECK SPI STATUS REG
	BPL	WAIT2	CHECK IF TRANSFER IS DONE
	LDAA	$102A	LOAD LTC1294 MSBs INTO ACC A
	STAA	$62	STORE MSBs IN $62
	LDAA	$52	LOAD DUMMY DIN INTO ACC A FROM $52
	STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
WAIT3	LDAA	$1029	CHECK SPI STATUS REG
	BPL	WAIT3	CHECK IF TRANSFER IS DONE
	BSET	$08,X,$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	LDAA	$102A	LOAD LTC1294 LSBs IN ACC
	STAA	$63	STORE LSBs IN $63
	JMP	LOOP	START NEXT CONVERSION

Hardware and Software Interface to Intel 8051


PS BIT LATCHED INTO LTC1294
$\overline{CS}$
CLK
1
2
3
4
5
6
7
8
DATA (D_{IN}/D_{OUT})
START
SGL/ DIFF
ODD/ SIGN
SEL 1
SEL 0
UNI
MSB
PS
B11
B10
B9
B8
B7
B6
B5
B4
B3
B2
B1
B0
8051 P1.2 OUTPUT DATA TO LTC1294
LTC1294 SEND A/D RESULT BACK TO 8051 P1.2
8051 P1.2 RECONFIGURED AS INPUT AFTER THE 8TH RISING CLK BEFORE THE 8TH FALLING CLK
LTC1294 TAKES CONTROL OF DATA LINE ON 8TH FALLING CLK
LTC1293 TD02

Hardware and Software Interface to Intel 8051


D_{OUT} FROM LTC1294 STORED IN 8051 RAM
MSB
R2
B11
B10
B9
B8
B7
B6
B5
B4
LSB
R3
B3
B2
B1
B0
0
0
0
0
ANALOG INPUTS
LTC1294
$\overline{CS}$
CLK
D_{OUT}
D_{IN}
P1.4
P1.3
P1.2
8051
MUX ADDRESS
A/D RESULT
LTC1293 TD02a

APPLICATIONS INFORMATION

8051 CODE

LABEL	MNEMONIC	OPERAND	COMMENTS
	SETB	P1.4	$\overline{CS}$ GOES HIGH
CONT	MOV	A,#87H	DIN WORD FOR LTC1294
	CLR	P1.4	$\overline{CS}$ GOES LOW
	MOV	R4,#08H	LOAD COUNTER
LOOP1	RLC	A	ROTATE DIN BIT INTO CARRY
	CLR	P1.3	CLK GOES LOW
	MOV	P1.2,C	OUTPUT DIN BIT TO LTC1294
	SETB	P1.3	CLK GOES HIGH
	DJNZ	R4,LOOP1	NEXT DIN BIT
	MOV	P1,#04H	P1.2 BECOMES AN INPUT
	CLR	P1.3	CLK GOES LOW
	MOV	R4,#09H	LOAD COUNTER
LOOP	MOV	C,P1.2	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT (B3) INTO ACC
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	DJNZ	R4,LOOP	NEXT DOUT BIT
	MOV	R2,A	STORE MSBs IN R2
	MOV	C,P1.2	READ DATA BIT INTO CARRY
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	CLR	A	CLEAR ACC
	RLC	A	ROTATE DATA BIT (B3) INTO ACC
	MOV	C,P1.2	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT (B2) INTO ACC
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	MOV	C,P1.2	READ DATA BIT INTO CARRY
	RLC	A	ROTATE DATA BIT (B1) INTO ACC
	SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW
	MOV	C,P1.2	READ DATA BIT INTO CARRY
	SETB	P1.4	$\overline{CS}$ GOES HIGH
	RRC	A	ROTATE DATA BIT (B0) INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	RRC	A	ROTATE RIGHT INTO ACC
	MOV	R3,A	STORE LSBs IN R3
	AJMP	CONT	START NEXT CONVERSION

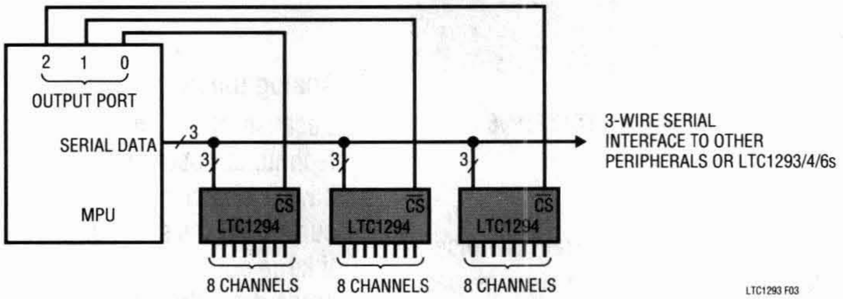


Figure 3. Several LTC1294 Sharing One 3-Wire Serial Interface

Sharing the Serial Interface

The LTC1293/4/6 can share the same 3-wire serial interface with other peripheral components or other LTC1293/4/6's (Figure 3). Now, the $\overline{CS}$ signals decide which LTC1293/4/6 is being addressed by the MPU.

ANALOG CONSIDERATIONS

Grounding

The LTC1293/4/6 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a PC board. The analog ground pin (AGND) should be tied directly to the ground plane with minimum lead length (a low profile socket is fine). The digital ground pin (DGND) also can be tied directly to this ground pin because minimal digital noise is generated within the chip itself. V_{CC} should be bypassed to the ground plane with a 22μF (minimum value) tantalum with leads as short as possible and as close as possible to the pin. A 0.1μF ceramic disk also should be placed in parallel with the 22μF and again with leads as short as possible and as close to V_{CC} as possible. AV_{CC} and DV_{CC} should be tied together on the

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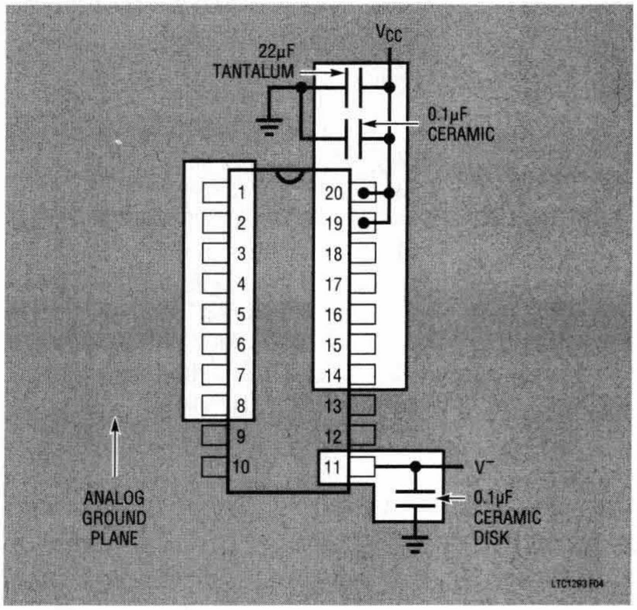
LTC1294. Figure 4 shows an example of an ideal LTC1293/4/6 ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.



V_{CC}
22µF
TANTALUM
0.1µF
CERAMIC
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
V^-
0.1µF
CERAMIC
DISK
ANALOG
GROUND
PLANE
LTC1293 F04

Figure 4. Ground Plane for the LTC1293/4/6

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during a conversion cycle can induce errors or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a minimum of 22µF tantalum capacitor and with leads as short as possible. The lead from the device to the V_{CC} supply also should be kept to a minimum and the V_{CC} supply should have a low output impedance such as obtained from a voltage regulator (e.g., LT323A). For high frequency bypassing a 0.1µF ceramic disk placed in parallel with the 22µF is recommended. Again the leads should be kept to a minimum. Figure 5 and 6 show the effects of good and poor V_{CC} bypassing.

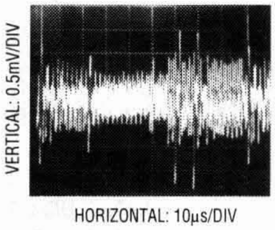


Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors.

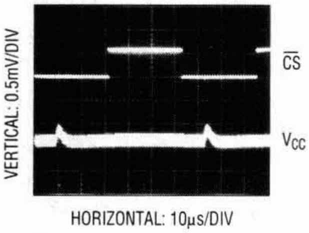
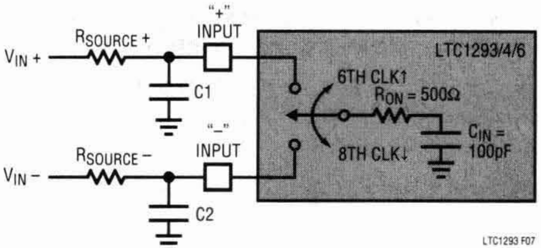


Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1293/4/6 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure the transients caused by the current spikes settle completely before the conversion begins.



V_{IN} +
R_{SOURCE} +
"+"
INPUT
C1
V_{IN} –
R_{SOURCE} –
"–"
INPUT
C2
LTC1293/4/6
6TH CLK↑
R_{ON} = 500Ω
8TH CLK↓
C_{IN} = 100pF
LTC1293 F07

Figure 7. Analog Input Equivalent Circuit

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Source Resistance

The analog inputs of the LTC1293/4/6 look like a 100pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}). C_{IN} gets switched between (+) and (–) inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

"+" Input Settling

The input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 8). The sample period 2 1/2 CLK cycles before a conversion starts. The voltage on the "+" input must settle completely within the sample period. Minimizing $R_{SOURCE}+$ and C1 will improve the settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 2.5μs **$R_{SOURCE}+ < 1.5k\Omega$ and C1 < 20pF will provide adequate settling time.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "-" input and the conversion starts (see Figure 8). During the conversion, the "+" input voltage is effectively "held" by the sample and hold and will not affect the conversion result. It is critical that the "–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing $R_{SOURCE}-$ and C2 will improve settling time. If large "–" input source resistance must be used the time can be extended by using a slower CLK frequency. At the maximum CLK frequency of 1MHz, **$R_{SOURCE}- < 250\Omega$ and C2 < 20pF will provide adequate settling**.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settles within the allowed time (see Figure 8). Again the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle

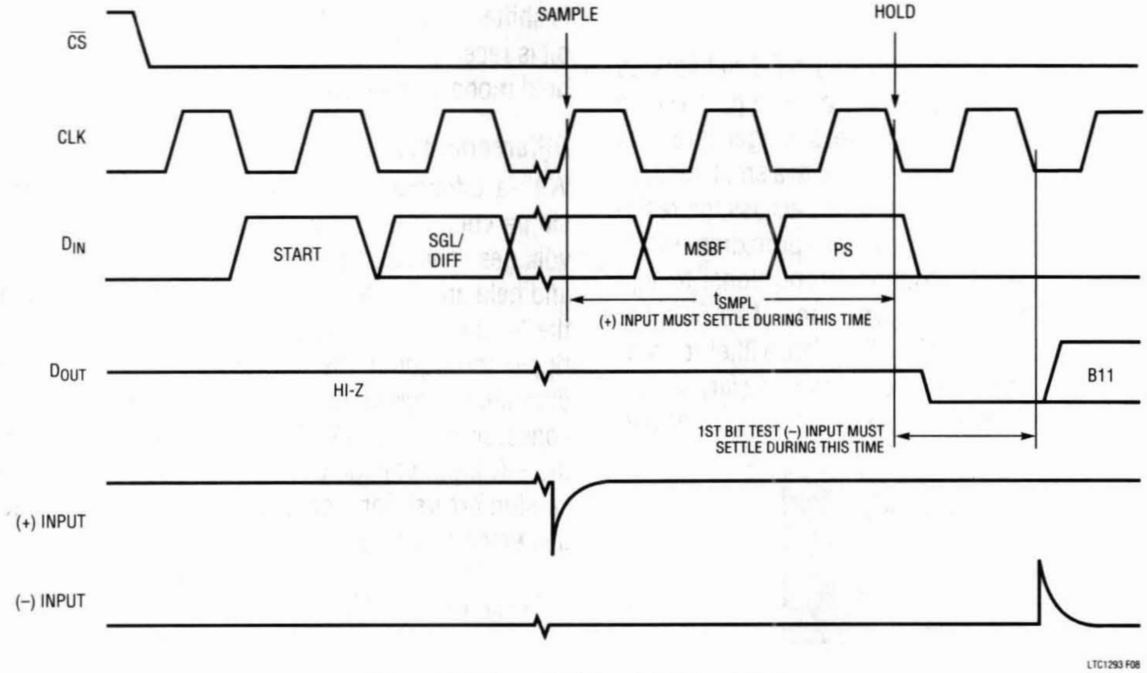

Figure 8. "+" and "–" Input Settling Windows

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within the minimum settling windows of 2.5μs ("+" input) and 1μs("–" input) that occurs at the maximum clock rate of 1MHz. Figures 9 and 10 show examples of adequate and poor op amp settling.

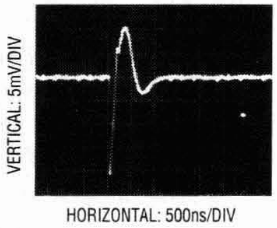

Figure 9. Adequate Settling of Op Amp Driving Analog Input

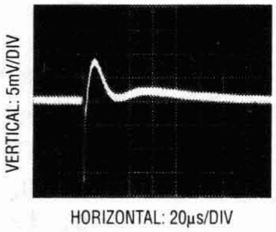

Figure 10. Poor Op Amp Settling Can Cause A/D Errors

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 11. For large values of C_F (e.g., 1μF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 21.5μs, the input current equals 23μA at $V_{IN} = 5V$. Here a filter resistor of 5Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the typical performance characteristic curve Maximum Filter Resistor vs Cycle Time.

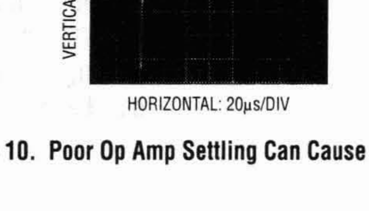

Figure 11. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1μA (at 125°C) flowing through a source resistance of 1kΩ will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical performance characteristic curve Input Channel Leakage Current vs Temperature).

SAMPLE AND HOLD

Single-Ended Input

The LTC1293/4/6 provides a built-in sample and hold (S&H) function for all signals acquired in the single-ended mode (COM pin grounded). The sample and hold allows the LTC1293/4/6 to convert rapidly varying signals (see typical performance characteristic curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 8. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling edge of the PS bit is received. On this falling edge the S&H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the selected "+" input is sampled and held and can be rapidly time varying. The voltage on the "–" pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR\,(MAX)} = \left(2\pi f_{(-)} V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right)$$

Where $f_{(-)}$ is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK.

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Usually V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 0.25LSB error (300μV) with the converter running at CLK = 1MHz, its peak value would have to be 66mV. Rearranging the above equation the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-)MAX} = \left(\frac{V_{ERROR\,(MAX)}}{2\pi V_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right)$$

For 0.25LSB error (300μV) the maximum input sinusoid with a 5V peak amplitude that can be digitized is 0.8Hz. **Unused inputs should be tied to the ground plane.**

Reference Input

The voltage on the reference input of the LTC1293/4/6 determines the voltage span of the A/D converter. The reference input has transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 12). During each bit test of the conversion (every CLK cycle) a capacitive current spike will be generated on the reference pin by the A/D. These current spikes settle quickly and do not cause a problem. If slow settling circuitry is used to drive the reference input, take care to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

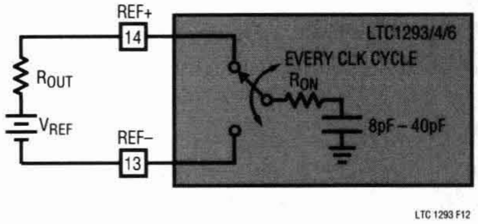

Figure 12. Reference Input Equivalent Circuit

Figure 13 and 14 show examples of both adequate and poor settling. Using a slower CLK will allow more time for the reference to settle. Even at the maximum CLK rate of 1MHz most references and op amps can be made to settle within the 1μs bit time. For example the LT1027 will settle adequately or with a 10μF bypass capacitor at V_{REF} the LT1021 also can be used.

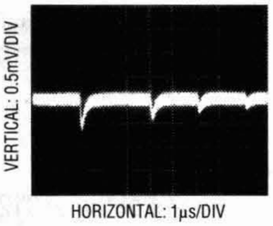

Figure 13. Adequate Reference Settling (LT1027)

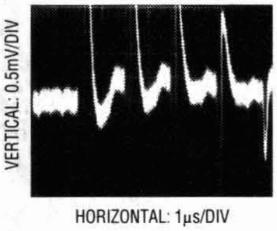

Figure 14. Poor Reference Settling Can Cause A/D Errors

Reduced Reference Operation

The effective resolution of the LTC1293/4/6 can be increased by reducing the input span of the converter. The LTC1293/4/6 exhibits good linearity over a range of reference voltages (see typical performance characteristics curves of Change in Linearity vs Reference Voltage and Change in Gain Error vs Reference Voltage). Care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. Offset and Noise are factors that must be considered when operating at low V_{REF} values. For the LTC1293 REF^- has been tied to the AGND pin. Any voltage drop from the AGND pin to the ground plane will cause a gain error.

Offset with Reduced V_{REF}

The offset of the LTC1293/4/6 has a larger effect on the output code when the A/D is operated with a reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristic curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSB's is related to reference voltage for a typical value of V_{OS}. For example a V_{OS} of 0.1mV, which is 0.1LSB with a 5V reference becomes 0.4LSB with

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a 1.25 reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input to the LTC1293/4/6.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1293/4/6 can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference input but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical performance characteristic curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200µV of noise.

For operation with a 5V reference, the 200µV noise is only 0.16LSB peak-to-peak. Here the LTC1293/4/6 noise will contribute virtually no uncertainty to the output code. For reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this 200µV noise is 0.64LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. Now averaging readings may be necessary.

This noise data was taken in a very clean test fixture. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage used, the more critical it becomes to have a noise-free setup.

Gain Error due to Reduced V_{REF}

The gain error of the LTC1294/6 is very good over a wide range of reference voltages. The error component that is seen in the typical performance characteristics curve Change in Gain Error vs Reference Voltage for the LTC1293 is due the voltage drop on the AGND pin from the device to the ground plane. To minimize this error the LTC1293 should be soldered directly onto the PC board. The internal reference point for V_{REF} is tied to AGND. Any voltage drop in the AGND pin will make the reference voltage, internal to the device, less than what is applied externally (Figure 15). This drop is typically 400µV due to the product of the pin resistance (R_{PIN}) and the LTC1293 supply current. For example, with V_{REF} = 1.25V this will result in a gain error change of –1.0LSB from the gain error measured with V_{REF} = 5V.

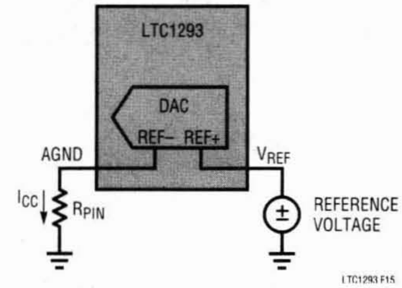

Figure 15. Parasitic Pin Resistance (R_{PIN})

LTC1293/4/6 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/Ds in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the "effective number of bits"(ENOB). SNR is the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the non-fundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by:

$$SNR = (6.02N + 1.76dB)$$

where N is the number of bits. Thus the SNR depends on the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. A Fast Fourier Transform (FFT) plot of the output spectrum of the LTC1294 is shown in Figures 16a and 16b. The input (f_{IN}) frequencies are 1kHz and 22kHz with the sampling frequency (f_S) at 45.4kHz. The SNR obtained from the plot are 72.7dB and 72.5dB.

Rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = \left(\frac{SNR - 1.76dB}{6.02} \right)$$

This is the so-called effective number of bits (ENOB). For the example shown in Figures 16a and 16b, N = 11.8 bits. Figure 17 shows a plot of ENOB as a function of input frequency. The top curve shows the A/D's ENOB remains at 11.8 for input frequencies up to $f_S/2$ with ±5V supplies.

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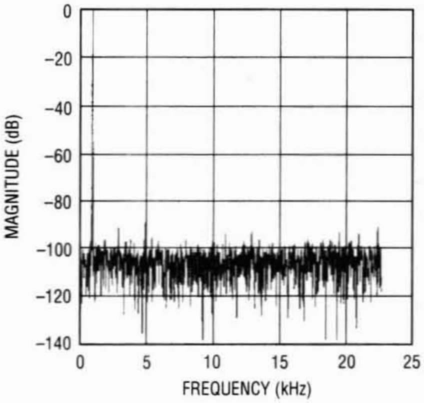

Figure 16a. LTC1294 FFT Plot
f_{IN} = 1kHz, f_S = 45.4kHz,
SNR = 72.7dB with ±5V Supplies

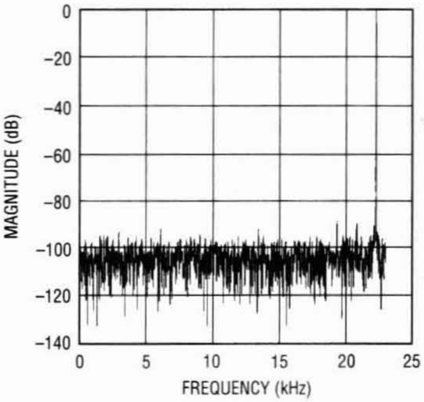

Figure 16b. LTC1294 FFT Plot
f_{IN} = 22kHz, f_S = 45.4kHz,
SNR = 72.5dB with ±5V Supplies

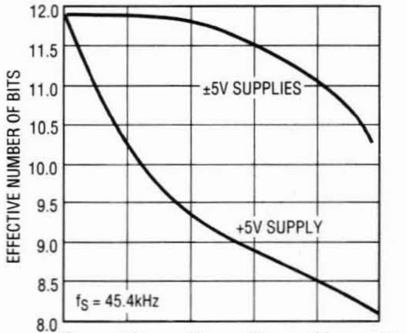

Figure 17. LTC1294 ENOB vs Input Frequency

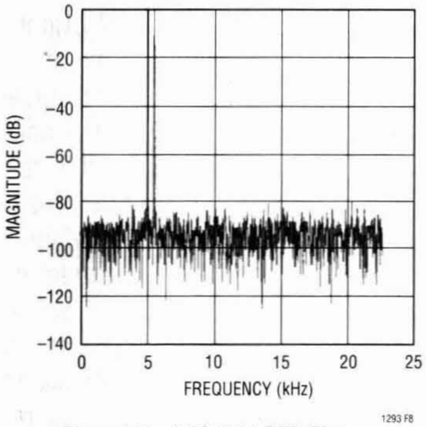

Figure 18. LTC1294 FFT Plot
$f_{IN}1$ = 5.1kHz, $f_{IN}2$ = 5.6kHz, f_S = 45.4kHz
with ±5V Supplies

For +5V supplies the ENOB decreases more rapidly. This is due predominantly to the 2nd harmonic distortion term.

Figure 18 shows a FFT plot of the output spectrum for two tones applied to the input of the A/D. Nonlinearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

Overvoltage Protection

Applying signals to the LTC1293/4/6's analog inputs that exceed the positive supply or that go below V^- will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog inputs before power is applied to the LTC1293/4/6. Another example is the input source is operating from different supplies of larger value than the LTC1293/4/6. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. There are two ways to protect the inputs. In Figure 19 diode clamps from the inputs to V_{CC} and V^- are used. The second method is to put resistors in series with the analog inputs for current limiting. As shown in Figure 20a, a 1kΩ resistor is enough to stand off ±15V (15mA for only one channel). If more than one channel exceeds the supplies than the following guidelines can be used. Limit the current to 7mA per channel and 28mA for all channels.

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This means four channels can handle 7mA of input current each. Reducing CLK frequency from a maximum of 1MHz (See typical performance characteristics curves Maximum CLK Frequency vs Source Resistance and Sample and Hold Acquisition Time vs Source Resistance) allows the use of larger current limiting resistors. The "+" input can accept a resistor value of 1kΩ but the "–" input cannot accept more than 250Ω when the maximum clock frequency of 1MHz is used. If the LTC1293/4/6 is clocked at the maximum clock frequency and 250Ω is not enough to current limit the "–" input source then the clamp diodes are recommended (Figures 20a and 20b). The reason for the limit on the resistor value is the MSB bit test is affected by the value of the resistor placed at the "–" input (see discussion on Analog Inputs and the typical performance characteristics curve Maximum CLK Frequency vs Source Resistance).

If V_{CC} and V_{REF} are not tied together, then V_{CC} should be turned on first, then V_{REF}. If this sequence cannot be met connecting a diode from V_{REF} to V_{CC} is recommended (see Figure 21).

For dual supplies (bipolar mode) placing two Schottky diodes from V_{CC} and V^- to ground (Figure 22) will prevent power supply reversal from occuring when an input source is applied to the analog MUX before power is applied to the device. Power supply reversal occurs, for example, if the input is pulled below V^-. V_{CC} will then pull a diode drop below ground which could cause the device not to power up properly. Likewise, if the input is pulled above V_{CC}, V^- will be pulled a diode drop above ground. If no inputs are present on the MUX, the Schottky diodes are not required if V^- is applied first then V_{CC}.

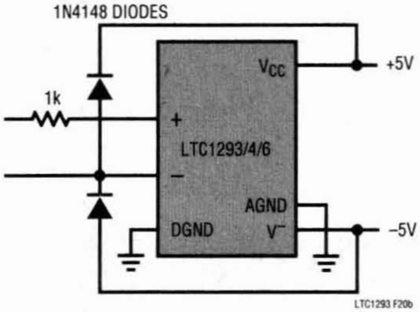
1N4148 DIODES
1k
VCC
+5V
+
LTC1293/4/6
–
AGND
DGND
V–
–5V
LTC1293 F20b

Figure 20b. Overvoltage Protection for Inputs

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

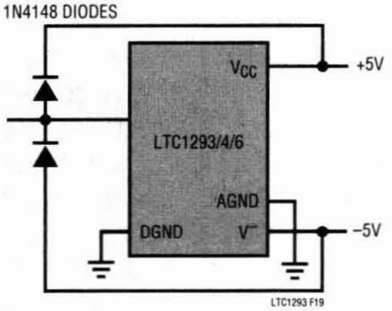
1N4148 DIODES
VCC
+5V
LTC1293/4/6
AGND
DGND
V–
–5V
LTC1293 F19

Figure 19. Overvoltage Protection for Inputs

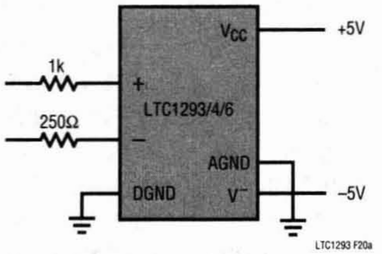
VCC
+5V
1k
+
LTC1293/4/6
250Ω
–
AGND
DGND
V–
–5V
LTC1293 F20a

Figure 20a. Overvoltage Protection for Inputs

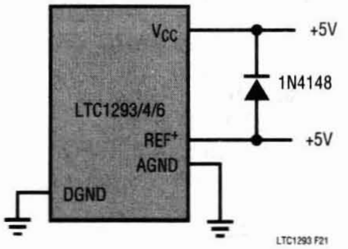
VCC
+5V
1N4148
LTC1293/4/6
REF+
+5V
AGND
DGND
LTC1293 F21

Figure 21

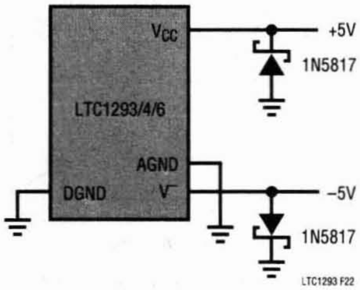
VCC
+5V
1N5817
LTC1293/4/6
AGND
DGND
V–
–5V
1N5817
LTC1293 F22

Figure 22. Power Supply Reversal

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A "Quick Look" Circuit for the LTC1294/6

Users can get a quick look at the function and timing of the LTC1294/6 by using the following simple circuit (Figure 23). V_{REF} is tied to V_{CC}. D_{IN} is tied high which means V_{IN} should be applied to the CH7 with respect to COM. A Unipolar conversion is requested and the data is output MSB first. $\overline{CS}$ is driven at 1/64 the clock rate by the CD4520 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 24).

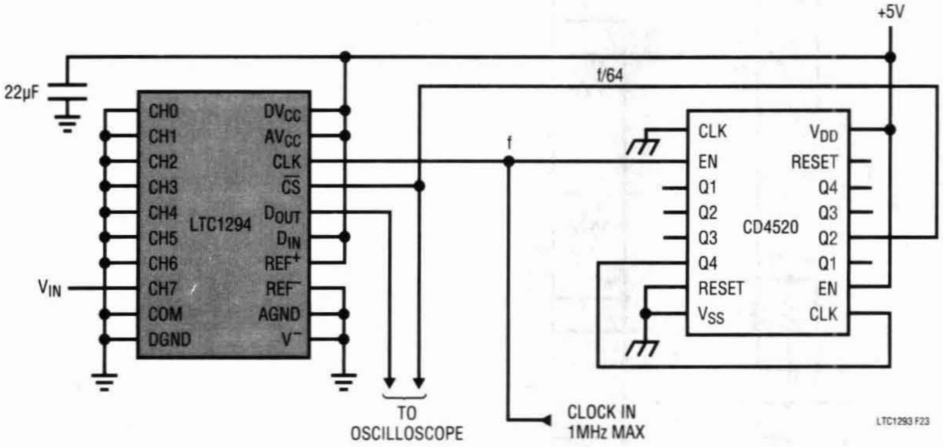

+5V
22µF
f/64
f
LTC1294
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
DVCC
AVCC
CLK
CS
DOUT
DIN
REF+
REF−
AGND
V−
VIN
CD4520
CLK
EN
Q1
Q2
Q3
Q4
RESET
VSS
VDD
RESET
Q4
Q3
Q2
Q1
EN
CLK
TO OSCILLOSCOPE
CLOCK IN 1MHz MAX
LTC1293 F23

Figure 23. "Quick Look" Circuit for the LTC1294/6

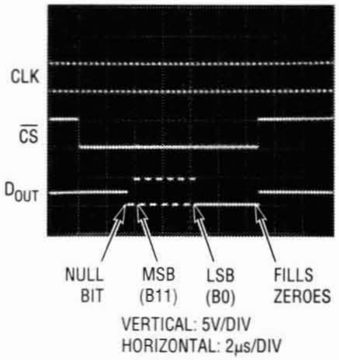
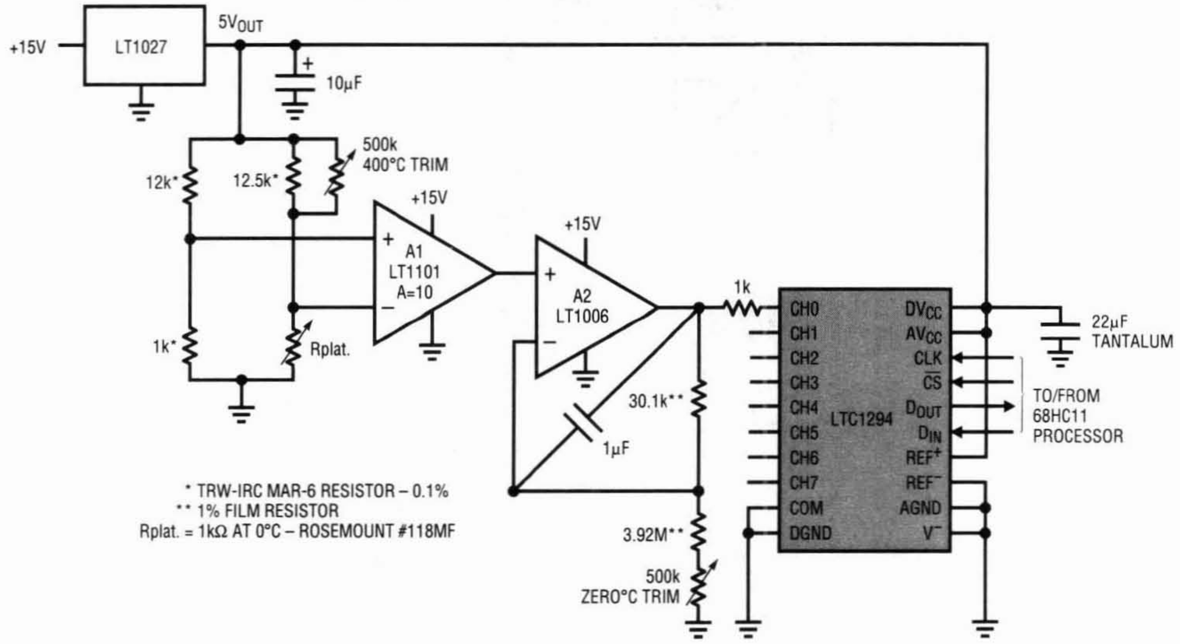


Figure 24. Scope Trace of the LTC1294/6 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

TYPICAL APPLICATIONS

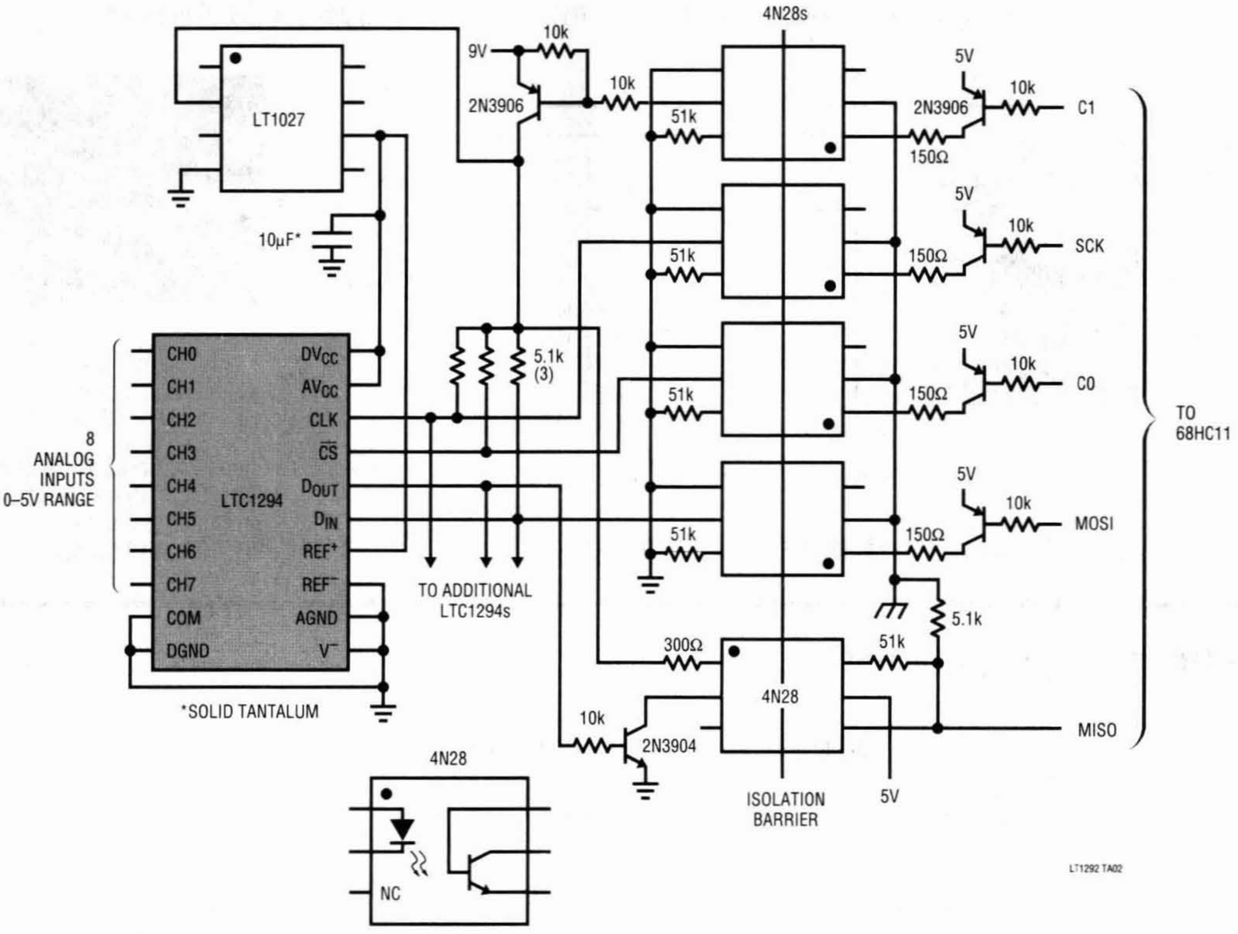
Digitally Linearized Platinum RTD Signal Conditioner


+15V
LT1027
5VOUT
10µF
12k*
12.5k*
500k 400°C TRIM
+15V
A1 LT1101 A=10
1k*
Rplat.
+15V
A2 LT1006
1µF
1k
30.1k**
3.92M**
500k ZERO°C TRIM
LTC1294
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
DVCC
AVCC
CLK
CS
DOUT
DIN
REF+
REF−
AGND
V−
22µF TANTALUM
TO/FROM 68HC11 PROCESSOR
LTC1293 TA03

* TRW-IRC MAR-6 RESISTOR – 0.1%
** 1% FILM RESISTOR
Rplat. = 1kΩ AT 0°C – ROSEMOUNT #118MF

TYPICAL APPLICATIONS

Micropower, 5000V Opto-Isolated, Multichannel,12-Bit Data Acquisition System is Accessed Once Every Two Seconds


LT1027
9V
10k
2N3906
10k
10µF*
4N28s
51k
51k
51k
51k
5V
10k
2N3906
150Ω
C1
SCK
C0
MOSI
TO 68HC11
5.1k (3)
8 ANALOG INPUTS 0–5V RANGE
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
LTC1294
DV_{CC}
AV_{CC}
CLK
$\overline{CS}$
D_{OUT}
D_{IN}
REF^+
REF^-
AGND
V^-
TO ADDITIONAL LTC1294s
*SOLID TANTALUM
300Ω
4N28
51k
5.1k
MISO
10k
2N3904
ISOLATION BARRIER
5V
4N28
NC
LT1292 TA02

SECTION 7—VOLTAGE REFERENCES

SECTION 7—VOLTAGE REFERENCES

INDEX 7-2
SELECTION GUIDES 7-3

PROPRIETARY PRODUCTS

LT1027, Precision 5V Reference 7-6
LT1431, Programmable Reference 7-13

VOLTAGE REFERENCES

Listed by Temperature Drift (T.C.) and Initial Accuracy

1.25V Output

T.C.	ACCURACY
*LT1034B-1.2	*LT1004-1.2
*LT1034-1.2	*LT1034B-1.2
*LT1004-1.2	*LT1034-1.2
*LM385B-1.2	*LM385B-1.2
*LM385-1.2	*LM385-1.2

2.5V Output

T.C.	ACCURACY
LT1019C-2.5	LT580M
LT1009C-2.5	LT1019C-2.5
LT580M	LT1009-2.5
LT1034B-2.5	LT580L
LT580L	LT1034-2.5
*LT1004C-2.5	LT580K
LT1034-2.5	*LT1004C-2.5
LT580K	*LM385B-2.5
*LM385B-2.5	*LM385-2.5
LM336B-2.5	LT580J
*LM385-2.5	LM336B-2.5
LM336-2.5	LM336-2.5

4.5V Output

T.C.	ACCURACY
LT1019C-4.5	LT1019C-4.5

5.0V Output

T.C.	ACCURACY
LT1027C-5	LT1027C-5
LT1027D-5	LT1021B-5
LT1027E-5	LT1027D-5
LT1021C-5	LT1027E-5
LT1019-5	REF-02E
LT1029A	LT1019-5
REF-02E	LT1021C-5
REF-02H	LT1021D-5
LT1021B-5	LT1029A
LT1021D-5	REF-02H
LT1029	LT1029
REF-02C	REF-02C
REF-02D	REF-02D

6.9V to 6.95V Output

T.C.	ACCURACY
LTZ1000	LM329A
LM399A	LTZ1000
LM399	LM329B
LM329A	LM329C
LM329B	LM329D
LM329C	LM399A

7V Output

T.C.	ACCURACY
LT1021B-7	LT1021B-7
LT1021D-7	LT1021D-7
LT1034	LT1034

10V Output

T.C.	ACCURACY
LT1021C-10	LT1021B-10
LT1031C	LT1031B-10
LT581K	REF-01E
LT1019-10	LT1031C
LT1031D	LT581K
LT581J	LT1019-10
REF-01E	LT1021C-10
LT1021B-10	LT1021D-10
LT1021D-10	LT1031D
LT1031B	REF-01H
REF-01H	LT581J
REF-01C	REF-01C

* Micropower

VOLTAGE REFERENCE SELECTION GUIDE

MILITARY

VOLTAGE V_Z (V)	VOLTAGE TOLERANCE MAXIMUM $T_A = 25°C$	PART NUMBER	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	PACKAGE TYPE	IMPORTANT FEATURES
1.235	±0.32%	LT1004M-1.2	20ppm (typ)	10µA to 20mA	H	Micropower
	±1%	LM185-1.2	20ppm (typ)	10µA to 20mA	H	Micropower
	±1%	LT1034BM-1.2	20ppm (max)	20µA to 20mA	H	Low TC Micropower with 7V Aux Reference
	±1%	LT1034M-1.2	40ppm (max)	20µA to 20mA	H	Low TC Micropower with 7V Aux Reference
2.5	±0.5%	LT1004M-2.5	20ppm (typ)	20µA to 20mA	H	Micropower
	±0.2%	LT1009M	18mV (max)	400µA to 10mA	H	Precision
	±0.05%	LT1019AM-2.5	10ppm (max)	1.0mA	H	Precision Bandgap
	±0.2%	LT1019M-2.5	25ppm (max)	1.2mA	H	Precision Bandgap
	±1%	LT1034BM-2.5	20ppm (max)	20µA to 20mA	H	Low TC Micropower with 7V Aux Reference
	±1%	LT1034M-2.5	40ppm (max)	20µA to 20mA	H	Low TC Micropower with 7V Aux Reference
	±2%	LM136-2.5	18mV (max)	400µA to 10mA	H	General Purpose
	±1%	LM136A-2.5	18mV (max)	400µA to 10mA	H	General Purpose
	±1.5%	LM185-2.5	20ppm (typ)	20µA to 20mA	H	Micropower
	±1%	LT580S	55ppm (max)	1.5mA	H	3 Terminal Low Drift
	±0.4%	LT580T	25ppm (max)	1.5mA	H	3 Terminal Low Drift
	±0.4%	LT580U	10ppm (max)	1.5mA	H	3 Terminal Low Drift
4.5	±0.05%	LT1019AM-4.5	10ppm (max)	1.0mA	H	Precision Bandgap
	±0.2%	LT1019M-4.5	25ppm (max)	1.2mA	H	Precision Bandgap
5.0	±0.05%	LT1019AM-5	10ppm (max)	1.0mA	H	Precision Bandgap
	±0.2%	LT1019M-5	25ppm (max)	1.2mA	H	Precision Bandgap
	±1%	LT1021BM-5	5ppm (max)	1.2mA	H	Very Low Drift
	±0.05%	LT1021CM-5	20ppm (max)	1.2mA	H	Very Tight Initial Tolerance
	±1%	LT1021DM-5	20ppm (max)	1.2mA	H	Low Cost, High Performance
	±0.2%	LT1029AM	20ppm (max)	700µA to 10mA	H	Precision Bandgap
	±1%	LT1029M	40ppm (max)	700µA to 10mA	H	Precision Bandgap
	±0.3%	REF02A	8.5ppm (max)	1.4mA	H, J	Precision Bandgap
	±0.5%	REF02	25ppm (max)	1.4mA	H, J	Precision Bandgap
6.9	±3%	LM129A	10ppm (max)	600µA to 15mA	H	Low Drift
	±3%	LM129B	20ppm (max)	600µA to 15mA	H	Low Drift
	±3%	LM129C	50ppm (max)	600µA to 15mA	H	Low Cost
6.95	±2%	LM199A	0.5ppm (max) –55°C to +85°C 10ppm (max) –85°C to +125°C	500µA to 10mA	H	Ultra Low Drift
	±2%	LM199	1ppm (max) –55°C to +85°C 15ppm (max) +85°C to +125°C	500µA to 10mA	H	Ultra Low Drift
7.0	±0.7%	LT1021BM-7	5ppm (max)	1.0mA	H	Low Drift/Noise, Exc Stability
	±0.7%	LT1021DM-7	20ppm (max)	1.0mA	H	Low Cost, High Performance
10.0	±0.05%	LT1019AM-10	10ppm (max)	1.0mA	H	Precision Bandgap
	±0.2%	LT1019M-10	25ppm (max)	1.2mA	H	Precision Bandgap
	±0.5%	LT1021BM-10	5ppm (max)	1.7mA	H	Very Low Drift
	±0.05%	LT1021CM-10	20ppm (max)	1.7mA	H	Very Tight Initial Tolerance
	±0.5%	LT1021DM-10	20ppm (max)	1.7mA	H	Low Cost, High Performance
	±0.05%	LT1031BM	5ppm (max)	1.7mA	H	Very Low Drift
	±0.1%	LT1031CM	15ppm (max)	1.7mA	H	Very Tight Initial Tolerance
	±0.2%	LT1031DM	25ppm (max)	1.7mA	H	Low Cost, High Performance
	±0.3%	LT581J	30ppm (max)	1.0mA	H	3 Terminal Low Drift
	±0.1%	LT581T	15ppm (max)	1.0mA	H	3 Terminal Low Drift
	±0.05%	LH0070-2	6.7ppm (max)	5.0mA	H	Low Drift
	±0.1%	LH0070-1	17ppm (max)	5.0mA	H	Good Initial Tolerance
	±0.1%	LH0070-0	33ppm (max)	5.0mA	H	Low Cost, High Performance
	±0.3%	REF01A	8.5ppm (max)	1.4mA	H, J	Precision Bandgap
	±0.5%	REF01	25ppm (max)	1.4mA	H, J	Precision Bandgap

VOLTAGE REFERENCE SELECTION GUIDE

COMMERCIAL

0°C to +70°C

VOLTAGE V_Z (V)	VOLTAGE TOLERANCE MAXIMUM $T_A = 25°C$	PART NUMBER	TEMPERATURE DRIFT, ppm/°C OR mV CHANGE	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	PACKAGE TYPE	IMPORTANT FEATURES
1.235	±0.32%	LT1004C-1.2	20ppm (typ)	10μA to 20mA	H, S, Z	Micropower
	±1%	LT1034BC-1.2	20ppm (max)	20μA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±1%	LT1034C-1.2	40ppm (max)	20μA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±2%	LM385-1.2	20ppm (typ)	15μA to 20mA	H, Z	Micropower
	±1%	LM385B-1.2	20ppm (typ)	15μA to 20mA	H, Z	Micropower
2.5	±0.8%	LT1004C-2.5	20ppm (typ)	20μA to 20mA	H, S, Z	Micropower
	±0.2%	LT1009C	6mV (max)	400μA to 10mA	H, Z	Precision
	±0.4%	LT1009S8	25ppm (max)	400μA to 20mA	S	Precision
	±0.05%	LT1019AC-2.5	5ppm (max)	1.0mA	H, N	Precision Bandgap
	±0.2%	LT1019C-2.5	20ppm (max)	1.2mA	H, N, S	Precision Bandgap
	±1%	LT1034BC-2.5	20ppm (max)	20μA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±1%	LT1034C-2.5	40ppm (max)	20μA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±4%	LM336-2.5	6mV (max)	400μA to 10mA	H, Z	General Purpose
	±2%	LM336B-2.5	6mV (max)	400μA to 10mA	H, Z	General Purpose
	±3%	LM385-2.5	20ppm (typ)	20μA to 20mA	H, Z	Micropower
	±1.5%	LM385B-2.5	20ppm (typ)	20μA to 20mA	H, Z	Micropower
	±3%	LT580J	85ppm (max)	1.5mA	H	3 Terminal Low Drift
	±1%	LT580K	40ppm (max)	1.5mA	H	3 Terminal Low Drift
	±0.4%	LT580L	25ppm (max)	1.5mA	H	3 Terminal Low Drift
	±0.4%	LT580M	10ppm (max)	1.5mA	H	3 Terminal Low Drift
4.5	±0.05%	LT1019AC-4.5	5ppm (max)	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019C-4.5	20ppm (max)	1.2mA	H, N, S	Precision Bandgap
5.0	±0.05%	LT1019AC-5	5ppm (max)	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019C-5	20ppm (max)	1.2mA	H, N, S	Precision Bandgap
	±1%	LT1021BC-5	5ppm (max)	1.2mA	H, N	Very Low Drift
	±0.05%	LT1021CC-5	20ppm (max)	1.2mA	H, N	Very Tight Initial Tolerance
	±1%	LT1021DC-5	20ppm (max)	1.2mA	H, J, N, S	Low Cost, High Performance
	± 0.05%	LT1027C	3ppm (max)	2mA	N, H	Precision, Dynamics
	± 0.05%	LT1027D	5ppm (max)	2mA	N, H	Precision, Dynamics
	± 0.1%	LT1027E	7.5ppm (max)	2mA	N, H	Precision, Dynamics
	±0.2%	LT1029AC	20ppm (max)	700μA to 10mA	H, Z	Precision Bandgap
	±1%	LT1029C	34ppm (max)	700μA to 10mA	H, Z	Precision Bandgap
	±1%	REF02C	65ppm (max)	1.6mA	H, J, N	Precision Bandgap
	±2%	REF02D	250ppm (max)	2.0mA	H, J, N	Bandgap
	±0.3%	REF02E	8.5ppm (max)	1.4mA	H, J, N	Precision Bandgap
	±0.5%	REF02H	25ppm (max)	1.4mA	H, J, N	Precision Bandgap
6.9	±3%	LM329A	10ppm (max)	600μA to 15mA	H, Z	Low Drift
	±5%	LM329B	20ppm (max)	600μA to 15mA	H, Z	Low Drift
	±5%	LM329C	50ppm (max)	600μA to 15mA	H, Z	General Purpose
	±5%	LM329D	100ppm (max)	600μA to 15mA	H, Z	General Purpose
	±4%	LTZ1000	0.1ppm	4mA	H	Ultra Low Drift, 2ppm Long Term Stability*
6.95	±5%	LM399	2ppm (max)	500μA to 10mA	H	Ultra Low Drift
	±5%	LM399A	1ppm (max)	500μA to 10mA	H	Ultra Low Drift
7.0	±0.7%	LT1021BC-7	5ppm (max)	1.0mA	H, N	Low Drift/Noise, Exc Stability
	±0.7%	LT1021DC-7	20ppm (max)	1.0mA	H, N, S	Low Cost, High Performance
10.0	±0.05%	LT1019AC-10	5ppm (max)	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019C-10	20ppm (max)	1.2mA	H, N, S	Precision Bandgap
	±0.5%	LT1021BC-10	5ppm (max)	1.7mA	H, N	Very Low Drift
	±0.05%	LT1021CC-10	20ppm (max)	1.7mA	H, N	Very Tight Initial Tolerance
	±0.5%	LT1021DC-10	20ppm (max)	1.7mA	H, N, S	Low Cost, High Performance
	±0.05%	LT1031BC	5ppm (max)	1.7mA	H	Very Low Drift
	±0.1%	LT1031CC	15ppm (max)	1.7mA	H	Very Tight Initial Tolerance
	±0.2%	LT1031DC	25ppm (max)	1.7mA	H	Low Cost, High Performance
	±0.3%	LT581J	30ppm (max)	1.0mA	H	3 Terminal Low Drift
	±0.1%	LT581K	15ppm (max)	1.0mA	H	3 Terminal Low Drift
	±1%	REF01C	65ppm (max)	1.6mA	H, J, N	Precision Bandgap
	±0.3%	REF01E	8.5ppm (max)	1.4mA	H, J, N	Precision Bandgap
	±0.5%	REF01H	25ppm (max)	1.4mA	H, J, N	Precision Bandgap

*LTZ1000 requires external control and biasing circuits.

LT1027

Precision 5V Reference

FEATURES

- Very Low Drift – 2ppm/°C Max TC
- Pin Compatible with LT1021-5, REF-02
- Output Sources 15mA, Sinks 10mA
- Excellent Transient Response Suitable for A-to-D Reference Inputs
- Noise Reduction Pin
- Excellent Long-Term Stability
- Less Than 1ppm p-p Noise (0.1Hz to 10Hz)

APPLICATIONS

- A-to-D and D-to-A Converters
- Digital Voltmeters
- Reference Standard
- Precision Current Source

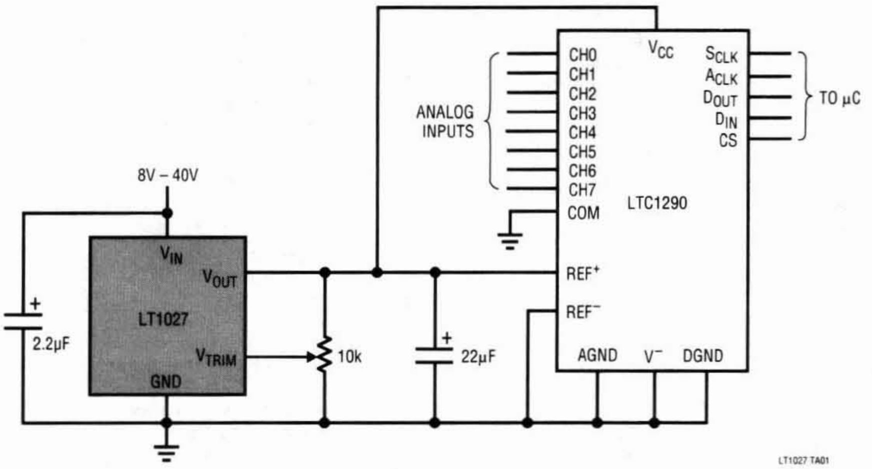
DESCRIPTION

The LT1027 is a precision reference with extra-low drift, superior accuracy, excellent line and load regulation and low output impedance at high frequency. This device is intended for use in 12- to 16-bit A-to-D and D-to-A systems where demanding accuracy requirements must be met without the use of power-hungry heated-substrate references. The fast-settling output recovers quickly from load transients such as those presented by A-to-D converter reference inputs. The LT1027 brings together both outstanding accuracy and temperature coefficient specifications.

The LT1027 reference is based on LTC's proprietary advanced sub-surface zener bipolar process which eliminates noise and stability problems associated with surface-breakdown devices.

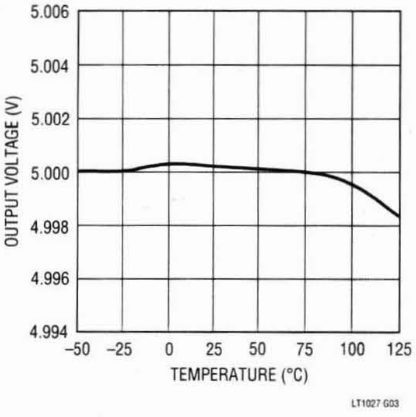
TYPICAL APPLICATION

Supplying V_{REF} and V_{CC} to the LTC1290 12-bit ADC



8V – 40V
V_{IN}
V_{OUT}
LT1027
V_{TRIM}
GND
2.2µF
10k
22µF
ANALOG INPUTS
CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
V_{CC}
S_{CLK}
A_{CLK}
D_{OUT}
D_{IN}
CS
TO µC
LTC1290
REF⁺
REF⁻
AGND
V⁻
DGND
LT1027 TA01

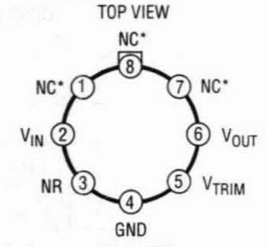
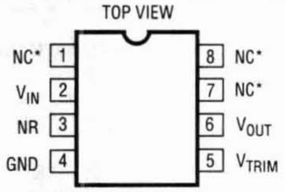
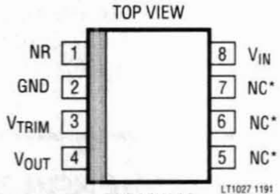
Output Voltage



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 40V
Input-Output Voltage Differential 35V
Output to Ground Voltage 7V
V_{TRIM} to Ground Voltage
    Positive 5V
    Negative .... –0.3V
Output Short Circuit Duration
    V_{IN} > 20V .... 10 sec.
    V_{IN} ≤ 20V .... Indefinite
Operating Temperature Range
    LT1027M .... –55°C to 125°C
    LT1027C .... 0°C to 70°C
Storage Temperature Range
    All Devices .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW NC* 8 NC* 1 7 NC* V_{IN} 2 6 V_{OUT} NR 3 5 V_{TRIM} 4 GND H PACKAGE 8-LEAD TO-5 METAL CAN	LT1027ACH LT1027BCH LT1027CCH LT1027DCH LT1027ECH LT1027DMH LT1027EMH
 TOP VIEW NC* 1 V_{IN} 2 NR 3 GND 4 8 NC* 7 NC* 6 V_{OUT} 5 V_{TRIM} N8 PACKAGE 8-LEAD PLASTIC DIP	LT1027BCN8 LT1027CCN8 LT1027DCN8 LT1027ECN8
 TOP VIEW NR 1 GND 2 V_{TRIM} 3 V_{OUT} 4 8 V_{IN} 7 NC* 6 NC* 5 NC* LT1027 1191 S8 PACKAGE 8-LEAD PLASTIC SOIC	LT1027ECS8

* CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, I_{LOAD} = 0, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage (Note 1)	LT1027A		4.9990	5.000	5.0010	V
		LT1027B, C, D		4.9975	5.000	5.0025	V
		LT1027E		4.9950	5.000	5.0050	V
TCV_{OUT}	Output Voltage Temperature Coefficient (Note 2)	LT1027A, B	●		1	2	ppm/°C
		LT1027C	●		2	3	ppm/°C
		LT1027D	●		2	5	ppm/°C
		LT1027E	●		3	7.5	ppm/°C
	Line Regulation (Note 3)	8V ≤ V_{IN} ≤ 10V			6	12	ppm/V
			●			25	ppm/V
		10V ≤ V_{IN} ≤ 40V			3	6	ppm/V
			●			8	ppm/V
	Load Regulation (Note 3)	Sourcing Current			3	6	ppm/mA
		0 ≤ I_{OUT} ≤ 15mA	●			8	ppm/mA
		Sinking Current			30	50	ppm/mA
		0 ≥ I_{OUT} ≥ –10mA	●			100	ppm/mA

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 10V$, $I_{LOAD} = 0$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Supply Current				1.8	2.4	mA
			●			2.8	mA
	V_{TRIM} Adjust Range		●	±30	±50		mV
e_n	Output Noise (Note 4)	0.1Hz ≤ f ≤ 10Hz			3		μVp-p
		10Hz ≤ f ≤ 1kHz			2.0	4.0	μV_{RMS}
	Temperature Hysteresis	H package; ΔT = 25°C			10		ppm
	Long Term Stability	H package			20		ppm/month

The ● denotes specifications which apply over the operating temperature range.

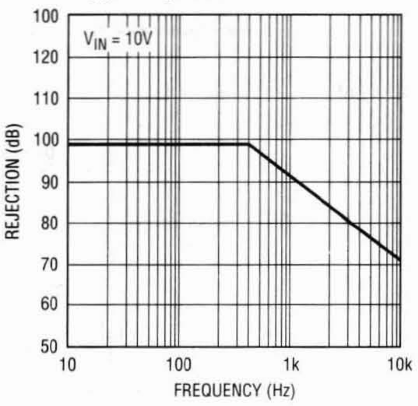
Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is determined by the "box" method in which the maximum ΔV_{OUT} over the temperature range is divided by ΔT.

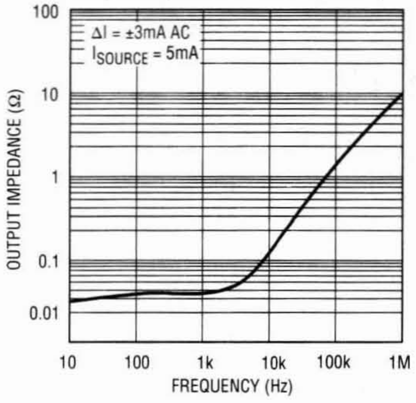
Note 3: Line and load regulation measurements are done on a pulse basis. Output voltage changes due to die temperature change must be taken into account separately. Package thermal resistance is 150°C/W for TO-5 (H), 130°C/W for plastic DIP (N8), and 180°C/W for plastic SOIC (S8).

Note 4: RMS noise is measured with an 8-pole bandpass filter with a center frequency of 30Hz and a Q of 1.5. The filter output is then rectified and integrated for a fixed time period, resulting in an average, as opposed to RMS voltage. A correction factor is used to convert average to RMS. This value is then used to obtain RMS noise voltage in the 10Hz to 1000Hz frequency band. This test also screens for low-frequency "popcorn" noise within the bandwidth of the filter. Consult factory for 100% 0.1Hz to 10Hz noise testing.

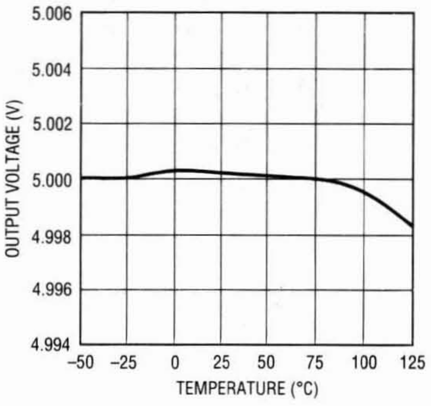
TYPICAL PERFORMANCE CHARACTERISTICS


Ripple Rejection

LT1027 G01


Output Impedance vs Frequency

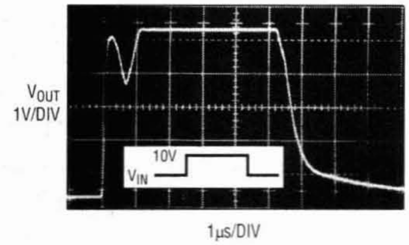
LT1027G02


Output Voltage

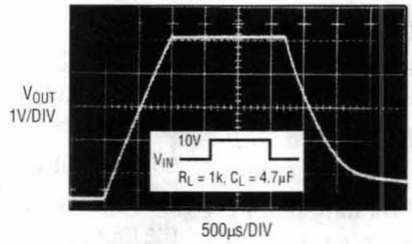
LT1027 G03

TYPICAL PERFORMANCE CHARACTERISTICS

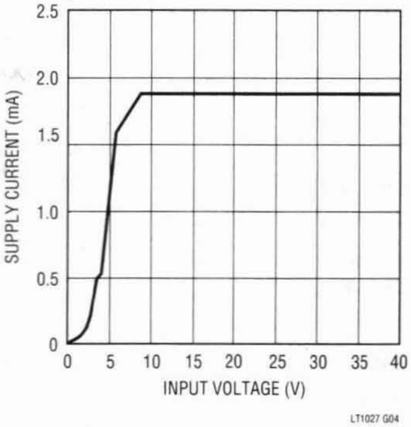
Start-Up and Turn-Off (No Load)



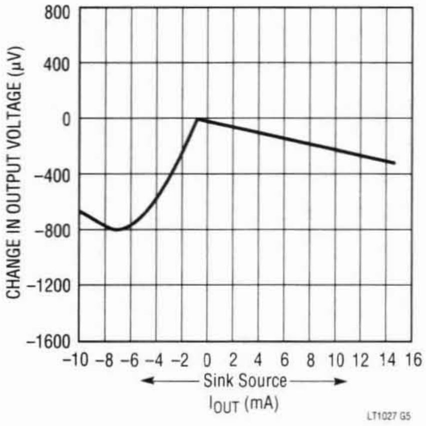
Start-Up and Turn-Off



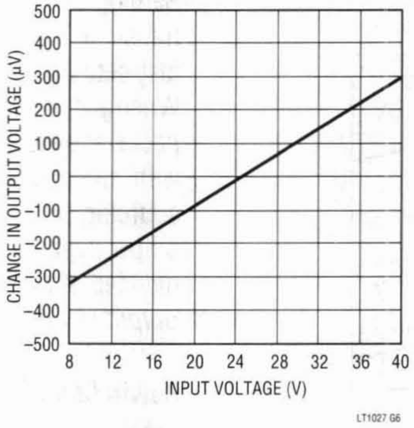
Quiescent Current



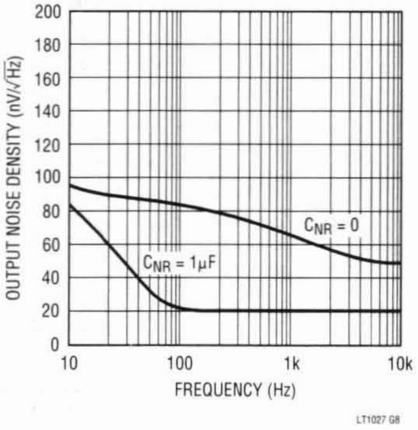
Load Regulation



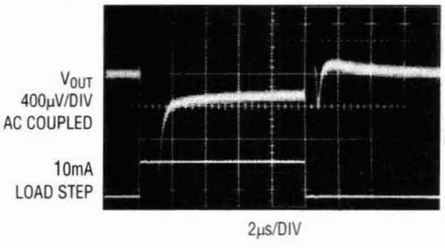
Line Regulation



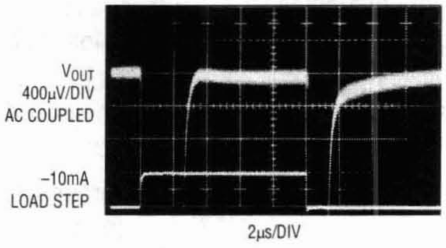
Output Noise Voltage Density



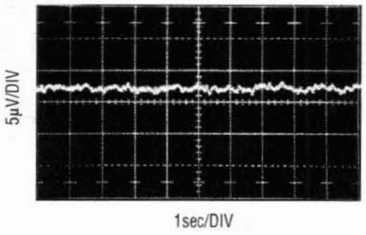
Output Settling Time (Sourcing)



Output Settling Time (Sinking)



0.1Hz to 10Hz Output Noise
Filtering = 1 zero at 0.1Hz
2 poles at 10Hz

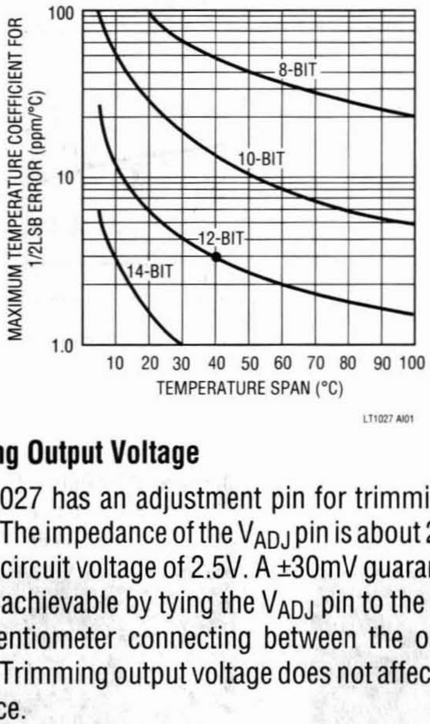


APPLICATIONS INFORMATION

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. This graph indicates the maximum temperature coefficient allowable if the reference is to contribute no more than 1/2LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 3ppm/°C if it is to contribute less than 1/2LSB error. For this reason, the LT1027 has been optimized for low drift.

Maximum Allowable Reference Drift



Trimming Output Voltage

The LT1027 has an adjustment pin for trimming output voltage. The impedance of the V_{ADJ} pin is about 20kΩ with an open circuit voltage of 2.5V. A ±30mV guaranteed trim range is achievable by tying the V_{ADJ} pin to the wiper of a 10k potentiometer connecting between the output and ground. Trimming output voltage does not affect the TC of the device.

Noise Reduction

The positive input of the internal scaling amplifier is brought out as the Noise Reduction (NR) pin. Connecting a 1µF Mylar capacitor between this pin and ground will reduce the wideband noise of the LT1027 from 2.0µV_{RMS} to approximately 1.2µV_{RMS} in a 10Hz to 1kHz bandwidth. Transient response is not affected by this capacitor. Start-up settling time will increase to several milliseconds due to the 7kΩ impedance looking into the NR pin. The capacitor *must* be a low-leakage type. Electrolytics are *not* suitable for this application. Just 100nA leakage current will result in a 150ppm error in output voltage. This pin is the most sensitive pin on the device. For maximum protection a guard ring is recommended. The ring should be driven from a resistive divider from V_{OUT} set to 4.4V (the open circuit voltage on the NR pin).

Transient Response

The LT1027 has been optimized for transient response. Settling Time is under 2µs when an AC-coupled 10mA load transient is applied to the output. The LT1027 achieves fast settling by using a class B NPN/PNP output stage. When sinking current, the device may oscillate with capacitive loads greater than 100pF. The LT1027 is stable with all capacitive loads when at no DC load or when sourcing current, although for best settling time either no output bypass capacitor or a 4.7µF tantalum unit is recommended. An 0.1µF ceramic output capacitor will *maximize output ringing* and is *not* recommended.

Kelvin Connections

Although the LT1027 does not have true force-sense capability, proper hook-up can improve line loss and ground loop problems significantly. Since the ground pin of the LT1027 carries only 2mA, it can be used as a low-side sense line, greatly reducing ground loop problems on the low side of the reference. The V_{OUT} pin should be close to the load or connected via a heavy trace as the resistance of this trace directly affects load regulation. It is important to remember that a 1.22mV drop due to trace resistance is equivalent to a 1LSB error in a 5VFS, 12-bit system.

The circuits in Figures 1 and 2 illustrate proper hook-up to minimize errors due to ground loops and line losses. Losses in the output lead can be further reduced by adding a PNP boost transistor if load current is 5mA or higher. R2 can be added to further reduce current in the output sense load.

APPLICATIONS INFORMATION

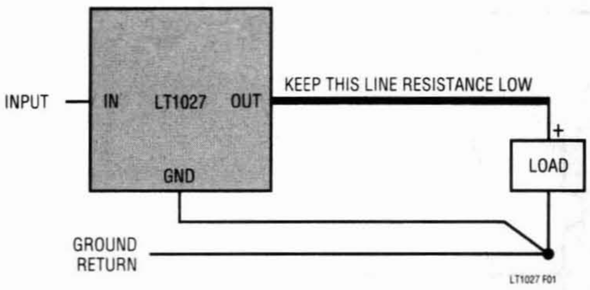
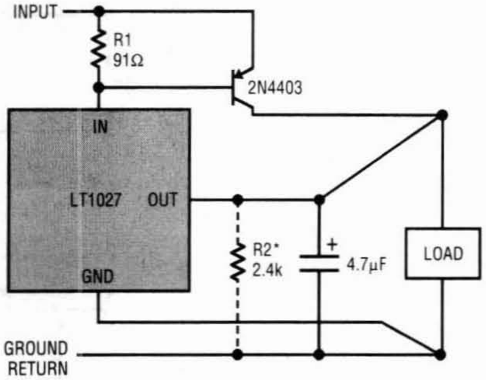

INPUT
IN
LT1027
OUT
GND
KEEP THIS LINE RESISTANCE LOW
+
LOAD
GROUND
RETURN
LT1027 F01

Figure 1. Standard Hook-Up


INPUT
R1
91Ω
2N4403
IN
LT1027
OUT
GND
R2*
2.4k
+
4.7μF
LOAD
GROUND
RETURN

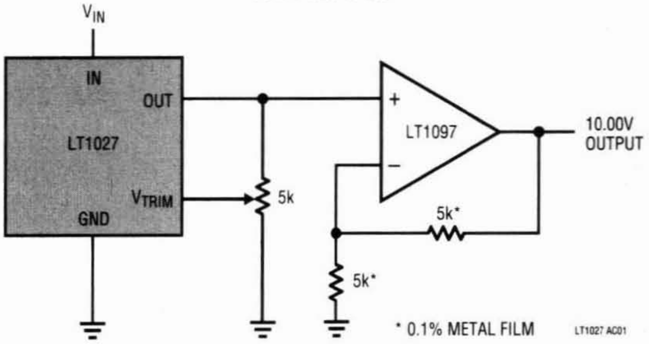
*OPTIONAL–REDUCES CURRENT IN OUTPUT SENSE LEAD

LT1027 F02

Figure 2. Driving Higher Load Currents

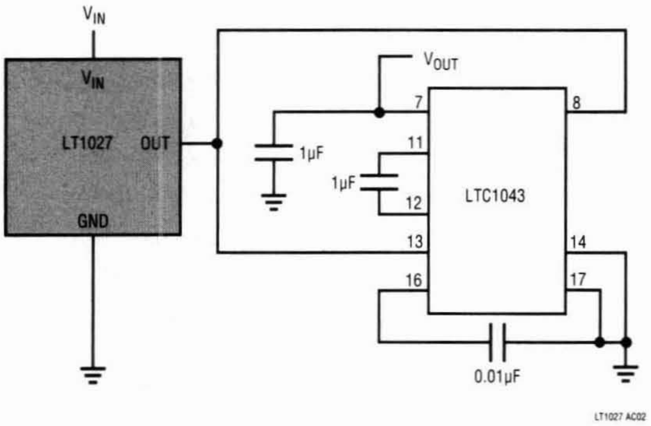
APPLICATION CIRCUITS

10V Reference

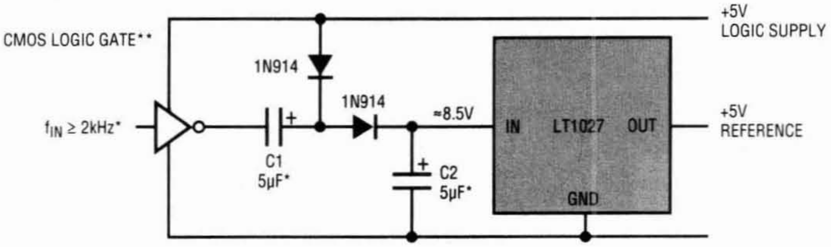

V_IN
IN
OUT
LT1027
V_TRIM
GND
5k
+
–
LT1097
5k*
5k*
10.00V
OUTPUT
LT1027 AC01

* 0.1% METAL FILM

10V Reference

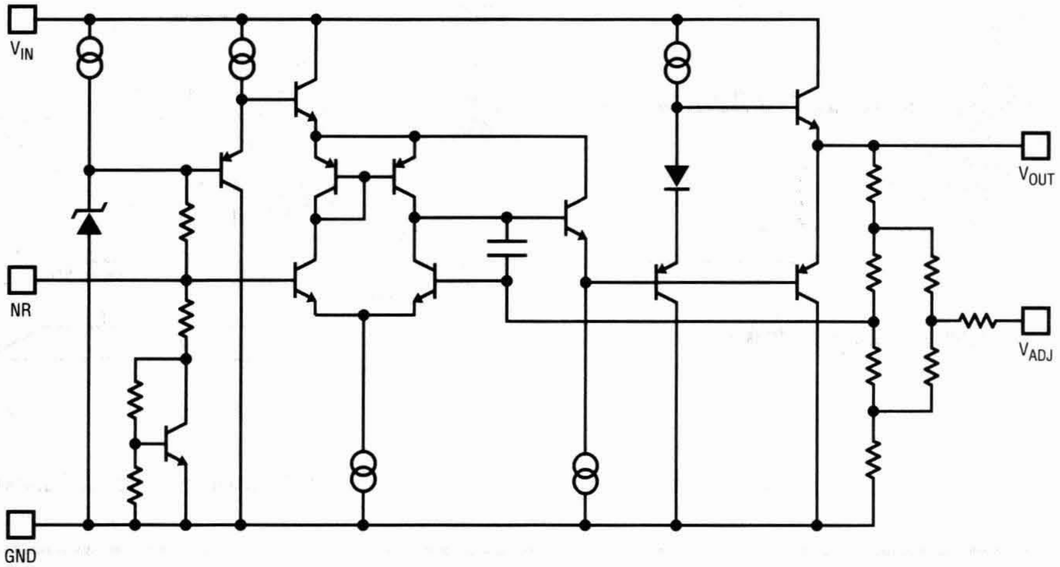

V_IN
V_IN
LT1027
OUT
GND
V_OUT
7
8
1μF
11
1μF
12
LTC1043
13
14
16
17
0.01μF
LT1027 AC02

Operating 5V Reference from 5V Supply


CMOS LOGIC GATE**
1N914
1N914
f_IN ≥ 2kHz*
+
C1
5μF*
≈8.5V
+
C2
5μF*
IN
LT1027
OUT
GND
+5V
LOGIC SUPPLY
+5V
REFERENCE
LT1027 AC03

*FOR HIGHER FREQUENCIES C1 AND C2 MAY BE DECREASED.
**PARALLEL GATES FOR HIGHER REFERENCE CURRENT LOADING.

EQUIVALENT SCHEMATIC


V_{IN}
NR
GND
V_{OUT}
V_{ADJ}

OUTPUT CURRENT LIMIT AND
BIAS CIRCUITS NOT SHOWN.

LT1027 ES01

Programmable Reference

FEATURES

- *Guaranteed* 0.4% Initial Voltage Tolerance
- 0.1Ω Typical Dynamic Output Impedance
- Fast Turn-On
- Sink Current Capability, 1mA to 100mA
- Low Ref Pin Current

APPLICATIONS

- Linear Regulators
- Adjustable Power Supplies
- Switching Power Supplies

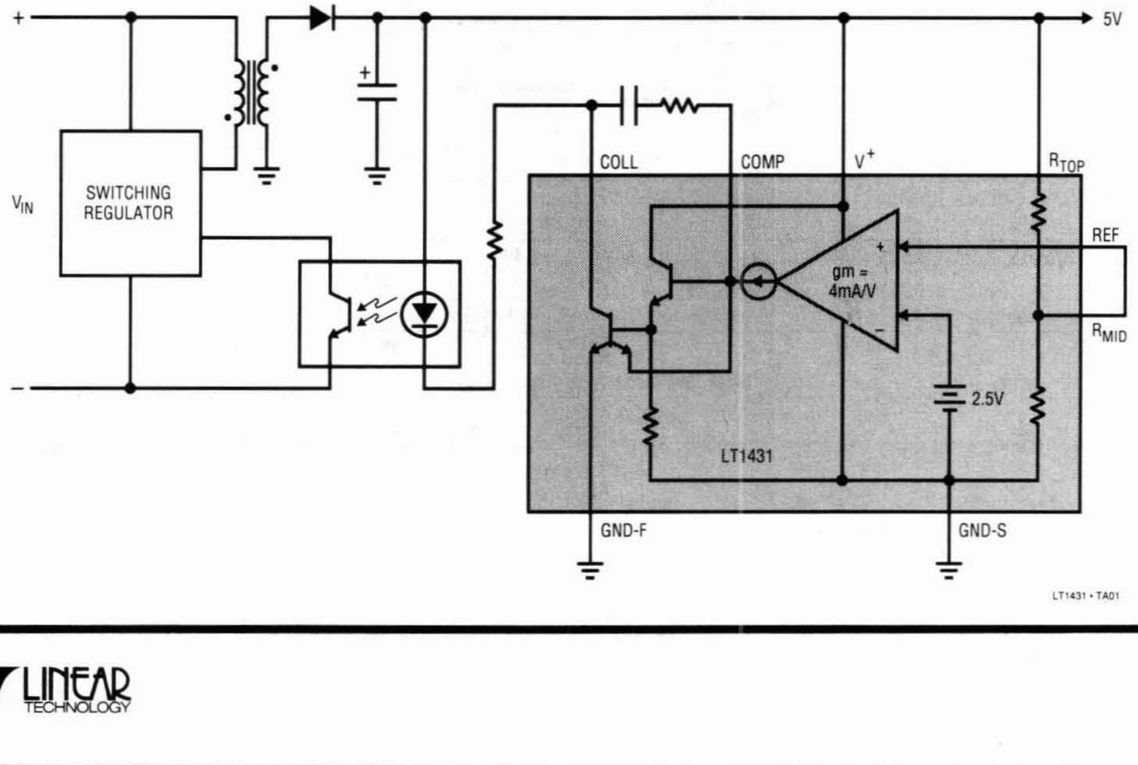
DESCRIPTION

The LT1431 is an adjustable shunt voltage regulator with 100mA sink capability, 0.4% initial reference voltage tolerance, and 0.3% typical temperature stability. On-chip divider resistors allow the LT1431 to be configured as a 5V shunt regulator, with 1% initial voltage tolerance and requiring no additional external components. By adding two external resistors, the output voltage may be set to any value between 2.5V and 36V. The nominal internal current limit of 100mA may be decreased by including one external resistor.

A simplified three pin version, the LT1431CZ/IZ, is available for applications as an adjustable reference and is pin compatible with the TL431.

TYPICAL APPLICATION

Isolated 5V Regulator

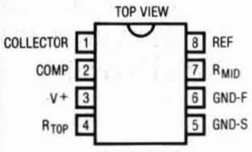
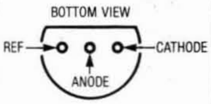
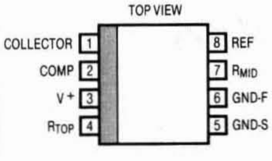


ABSOLUTE MAXIMUM RATINGS

V^+, $V_{COLLECTOR}$ 36V
V_{COMP}, R_{TOP}, R_{MID}, V_{REF} 6V
GND-F to GND-S 0.7V
Ambient Temperature Range
  LT1431M .... −55°C to 125°C
  LT1431I .... −40°C to 85°C
  LT1431C .... 0°C to 70°C

Junction Temperature Range
  LT1431M .... −55°C to 150°C
  LT1431I .... − 40°C to 100°C
  LT1431C .... 0°C to 100°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER		ORDER PART NUMBER
 TOP VIEW COLLECTOR 1 COMP 2 V+ 3 R_{TOP} 4 8 REF 7 R_{MID} 6 GND-F 5 GND-S J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP	LT1431MJ8 LT1431CN8 LT1431IN8	 Z PACKAGE 3-LEAD TO-92 PLASTIC	LT1431CZ LT1431IZ	 TOP VIEW COLLECTOR 1 COMP 2 V+ 3 R_{TOP} 4 8 REF 7 R_{MID} 6 GND-F 5 GND-S S8 PACKAGE 8-LEAD PLASTIC SOIC	LT1431CS8 LT1431IS8

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $I_K = 10mA$, unless otherwise specified (Note 1).

				LT1431M/I			LT1431C			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{REF}	Reference Voltage	$V_{KA} = 5V$, $I_K = 2mA$, (Note 2)		2490	2500	2510	2490	2500	2510	mV
			●	2465		2535	2480		2520	mV
$\Delta V_{REF}/\Delta T$	Reference Drift	$V_{KA} = 5V$, $I_K = 2mA$	●		50			30		ppm/°C
$\frac{\Delta V_{REF}}{\Delta V_{KA}}$	Voltage Ratio, Reference to Cathode (Open Loop Gain)	$I_K = 2mA$, $V_{KA} = 3V$ to 36V	●		0.2	0.5		0.2	0.5	mV/V
$\lvert I_{REF} \rvert$	Reference Input Current	$V_{KA} = 5V$, $T_A = 25°C$			0.2	1		0.2	1	μA
			●			1.5			1.2	μA
I_{MIN}	Minimum Operating Current	$V_{KA} = V_{REF}$ to 36V			0.6	1		0.6	1	mA
$\lvert I_{OFF} \rvert$	Off-State Cathode Current	$V_{KA} = 36V$, $V_{REF} = 0V$				1			1	μA
			●			15			2	μA
$\lvert I_{LEAK} \rvert$	Off-State Collector Leakage Current	$V_{COLL} = 36V$, $V^+ = 5V$, $V_{REF} = 2.4V$				1			1	μA
			●			5			2	μA
$\lvert Z_{KA} \rvert$	Dynamic Impedance	$V_{KA} = V_{REF}$, $I_K = 1mA$ to 100mA, $f \leq 1kHz$				0.2			0.2	Ω
I_{LIM}	Collector Current Limit	$V_{KA} = V_{REF} + 50mV$	●	80		360	100		260	mA
	5V Reference Output	Internal Divider Used, $I_K = 2mA$		4950	5000	5050	4950	5000	5050	mV

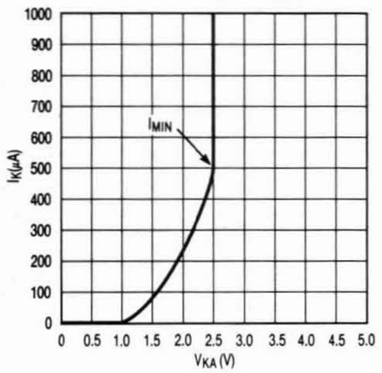
The ● denotes specifications which apply over the full operating temperature range.

Note 1: V_{KA} is the cathode voltage of the LT1431CZ/IZ and corresponds to V^+ of the LT1431CN8/IN8/MJ8. I_K is the cathode current of the LT1431CZ/IZ and corresponds to $I(V^+) + I_{COLLECTOR}$ of the LT1431CN8/MJ8/IN8.

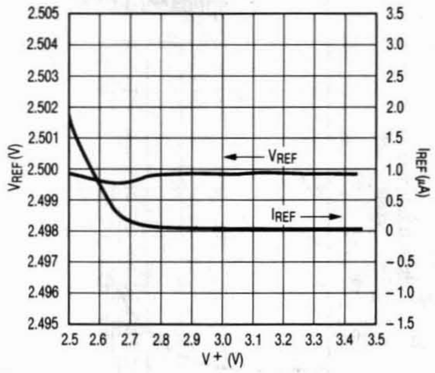
Note 2: The LT1431 has bias current cancellation which is effective only for $V_{KA} \geq 3V$. A slight (≈2mV) shift in reference voltage occurs when V_{KA} drops below 3V. For this reason, these tests are not performed at $V_{KA} = V_{REF}$.

TYPICAL PERFORMANCE CHARACTERISTICS

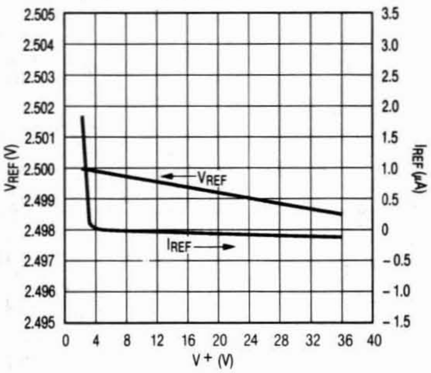
2.5V Reference I_K vs V_{KA}



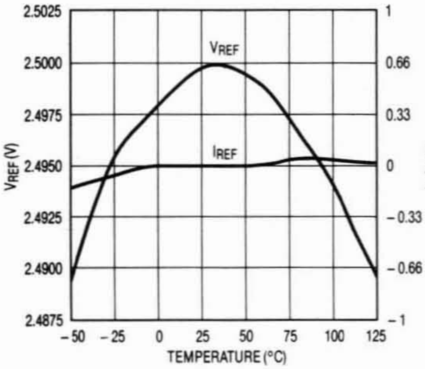
V_{REF} and I_{REF} vs V^+



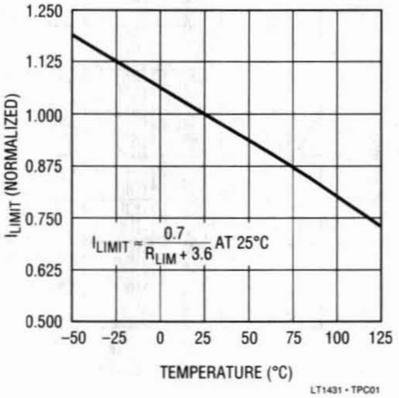
V_{REF} and I_{REF} vs V^+



V_{REF} and I_{REF} vs Temperature

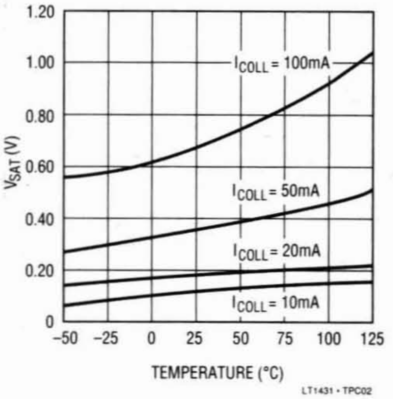


I_{LIMIT} vs Temperature with External Resistor



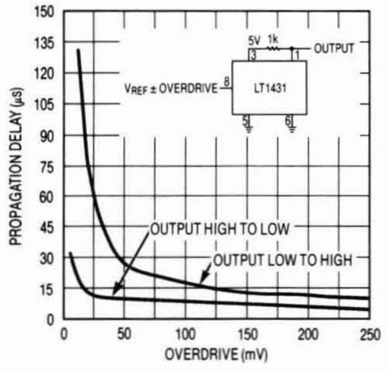
LT1431 • TPC01

COLLECTOR V_{SAT} vs Temperature vs Current

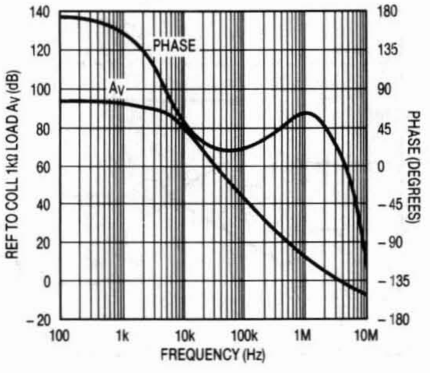


LT1431 • TPC02

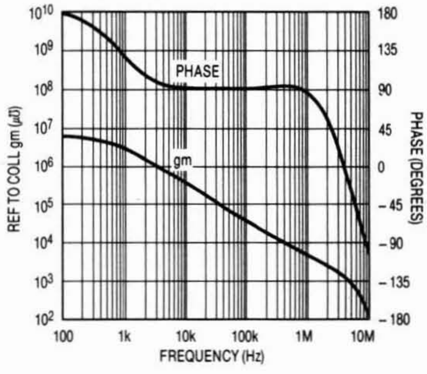
Propagation Delay vs Overdrive



Voltage Gain and Phase vs Frequency

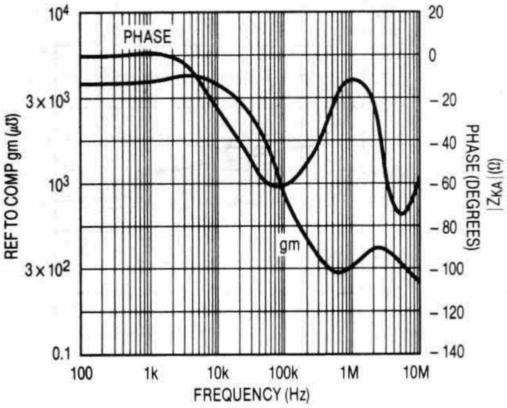


Transconductance and Phase vs Frequency (Ref to Coll)

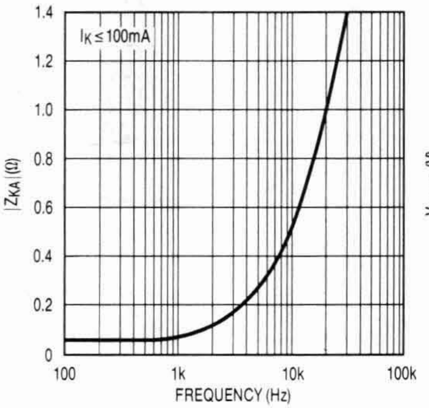


TYPICAL PERFORMANCE CHARACTERISTICS

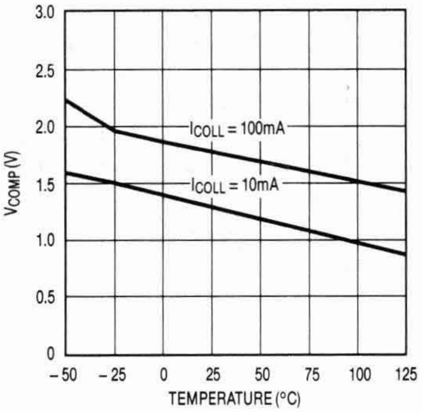
Transconductance and Phase vs Frequency (Ref to Comp)



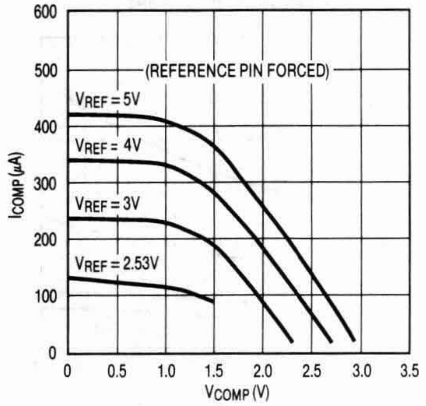
Dynamic Impedance vs Frequency



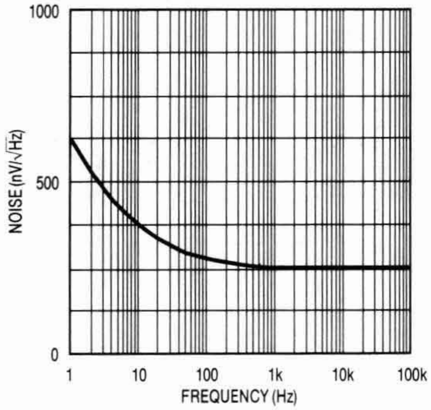
V_{COMP} vs Temperature vs I_{COLL}



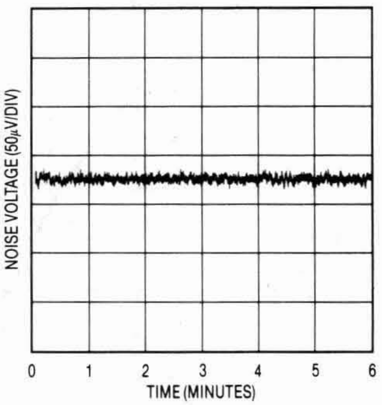
I_{COMP} vs V_{COMP} vs V_{REF}



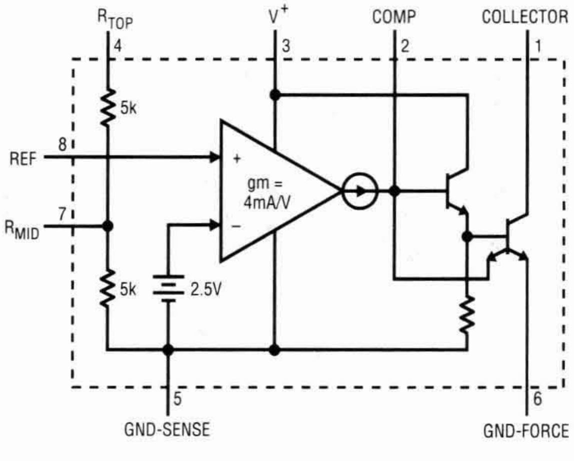
Noise vs Frequency



0.1Hz to 10Hz Noise



BLOCK DIAGRAM


RTOP
4
V⁺
3
COMP
2
COLLECTOR
1
5k
REF
8
+
gm =
4mA/V
–
RMID
7
5k
2.5V
5
GND-SENSE
6
GND-FORCE

LT1431 • TA02

APPLICATIONS INFORMATION

Pin Functions

Pin 1 COLL: Open collector of the output transistor. The maximum pin voltage is 36V. The saturation voltage at 100mA is approximately 1V.

Pin 2 COMP: Base of the driver for the output transistor. This pin allows additional compensation for complex feedback systems and shutdown of the regulator. It must be left open if unused.

Pin 3 V^+: Bias voltage for the entire shunt regulator. The maximum input voltage is 36V and the minimum to operate is equal to V_{REF} (2.5V). The quiescent current is typically 0.6mA.

Pin 4 R_{TOP}: Top of the on-chip 5k-5k resistive divider that guarantees 1% accuracy of operation as a 5V shunt regulator with no external trim. The pin is tied to COLL for self-contained 5V operation. It may be left open if unused. See note on parasitic diodes below.

Pin 5 GND-S: Ground reference for the on-chip resistive divider and shunt regulator circuitry except for the output transistor. This pin allows external current limit of the output transistor with one resistor between GND-F (force) and GND-S (sense).

Pin 6 GND-F: Emitter of the output transistor and substrate connection for the die.

Pin 7 R_{MID}: Middle of the on-chip resistive divider string between R_{TOP} and GND-S. The pin is tied to REF for self-contained 5V operation. It may be left open if unused.

Pin 8 REF: Control pin of the shunt regulator with a 2.5V threshold. If $V^+ > 3V$, input bias current cancellation reduces Ib to 0.2μA typical.

COMP, R_{TOP}, R_{MID}, and REF have static discharge protection circuits that must not be activated on a continuous basis. Therefore, the absolute maximum DC voltage on these pins is 6V, well beyond the normal operating conditions.

As with all bipolar ICs, the LT1431 contains parasitic diodes which must not be forward biased or else anomalous behavior will result. Pin conditions to be avoided are R_{TOP} below R_{MID} in voltage and any pin below GND-F in voltage (except for GND-S).

The following pin definitions apply to the Z package.

Pin 1 CATHODE: Corresponds to COLL and V^+ tied together.

Pin 2 ANODE: Corresponds to GND-S and GND-F tied together.

Pin 3 REF: Corresponds to REF.

Frequency Compensation

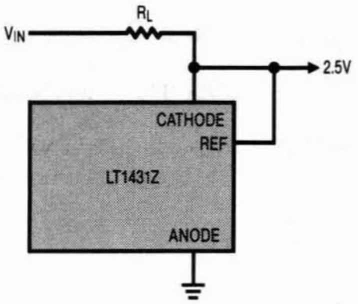
As a shunt regulator, the LT1431 is stable for all capacitive loads on the COLL pin. Capacitive loading between 0.01μF and 18μF causes reduced phase margin with some ringing under transient conditions. Output capacitors should not be used arbitrarily because output noise is not necessarily reduced.

Excess capacitance on the REF pin can introduce enough phase shift to induce oscillation when configured as a reference >2.5V. This can be compensated with capacitance between COLL and REF (phase lead). More complicated feedback loops may require shaping of the frequency response of the LT1431 with dominant pole or pole-zero compensation. This can be accomplished with a capacitor or series resistor and capacitor between COLL and COMP.

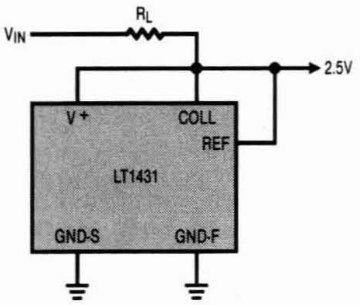
The compensation schemes mentioned above use voltage feedback to stabilize the circuits. There must be voltage gain at the COLL pin for them to be effective, so the COLL pin must see a reasonable AC impedance. Capacitive loading of the COLL pin reduces the AC impedance, voltage gain, and frequency response, thereby decreasing the effectiveness of the compensation schemes, but also decreasing their necessity.

TYPICAL APPLICATIONS

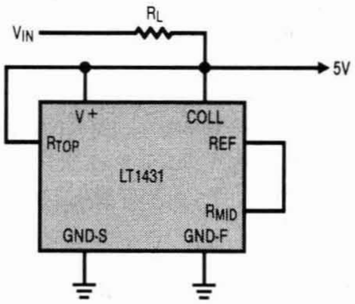
2.5V Reference
3-Pin Package


V_IN
R_L
2.5V
CATHODE
REF
LT1431Z
ANODE

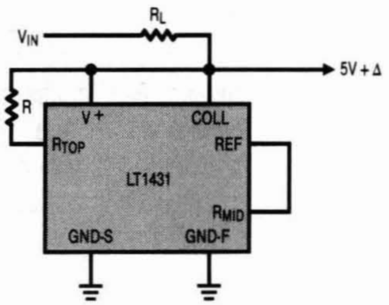
2.5V Reference
8-Pin Package


V_IN
R_L
2.5V
V+
COLL
REF
LT1431
GND-S
GND-F

5V Reference

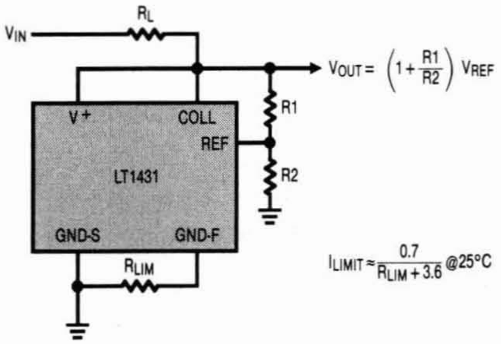

V_IN
R_L
5V
V+
COLL
R_TOP
REF
LT1431
R_MID
GND-S
GND-F

Increasing 5V Reference


V_IN
R_L
5V + Δ
R
V+
COLL
R_TOP
REF
LT1431
R_MID
GND-S
GND-F

Δ = R × (0.5mA) ± 25% PROCESS TOLERANCE
Δ ≤ 500mV

Programmable Reference with Adjustable Current Limit

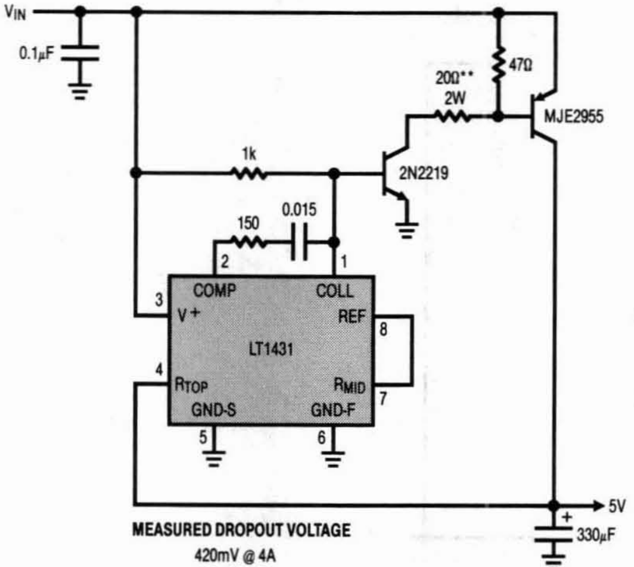

V_IN
R_L
V+
COLL
REF
LT1431
GND-S
GND-F
R1
R2
R_LIM

$V_{OUT} = \left(1 + \frac{R1}{R2}\right) V_{REF}$

$I_{LIMIT} \approx \frac{0.7}{R_{LIM} + 3.6}$ @25°C

TYPICAL APPLICATIONS

PNP Low Dropout 5V Regulator*

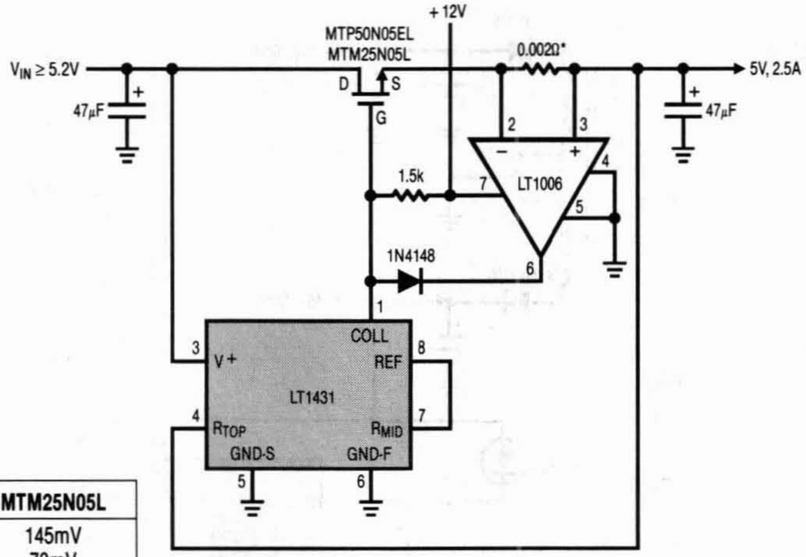

VIN
0.1µF
47Ω
20Ω**
2W
MJE2955
1k
2N2219
150
0.015
2
1
3
COMP
COLL
V+
REF
8
LT1431
4
RTOP
RMID
7
GND-S
GND-F
5
6
5V
330µF

MEASURED DROPOUT VOLTAGE

420mV @ 4A
190mV @2A
95mV @ 1A
60mV @ 0.5A

*NO SHORT CIRCUIT PROTECTION
**MAY BE INCREASED AT LOWER WATTAGE
FOR LOWER OUTPUT CURRENTS

FET Low Dropout 5V Regulator with Current Limit


+12V
MTP50N05EL
MTM25N05L
0.002Ω*
VIN ≥ 5.2V
D
S
G
5V, 2.5A
47µF
47µF
2
3
1.5k
7
LT1006
4
5
1N4148
6
1
COLL
3
V+
REF
8
LT1431
4
RTOP
RMID
7
GND-S
GND-F
5
6

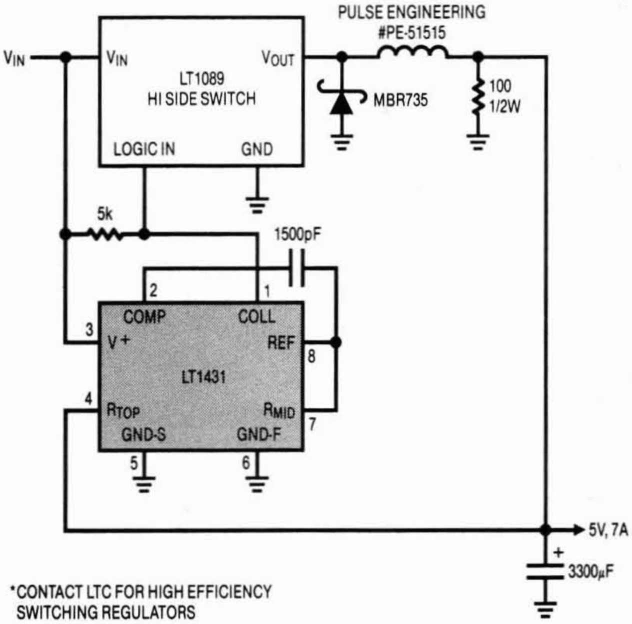
*1.5" #23 SOLID COPPER WIRE
~0.002Ω → 3A LIMIT

Measured Dropout Voltages

I_{LOAD}	MTP50N05EL	MTM25N05L
2A	47mV	145mV
1A	22mV	73mV
0.5A	11.5mV	37mV

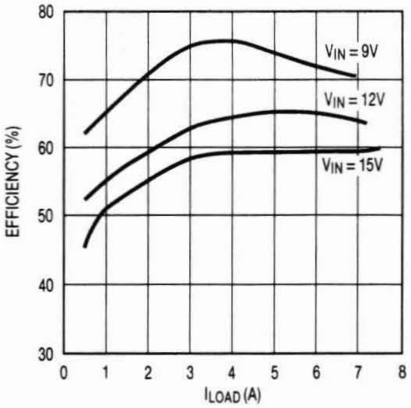
TYPICAL APPLICATIONS

12V to 5V Buck Converter with Foldback Current Limit*

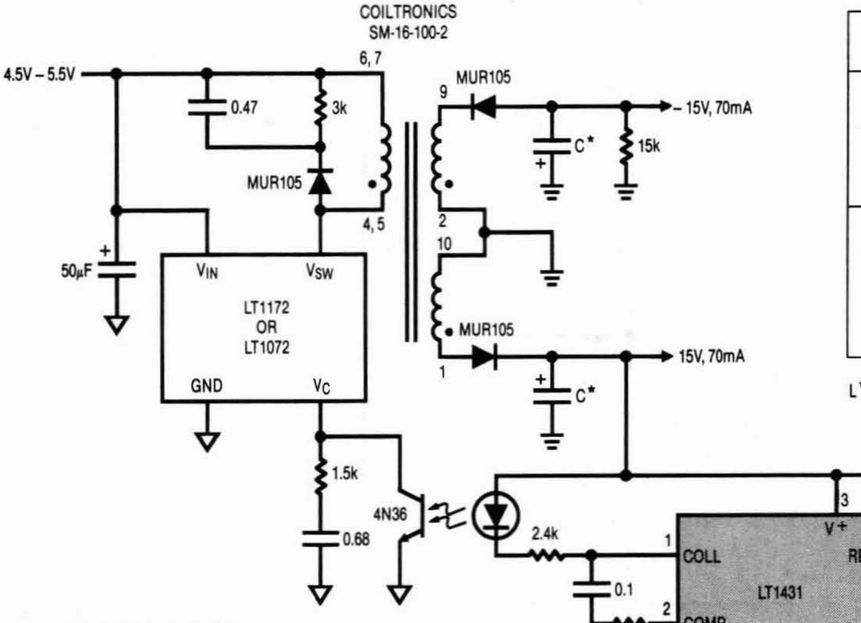

PULSE ENGINEERING
#PE-51515
VIN
VIN
VOUT
LT1089
HI SIDE SWITCH
LOGIC IN
GND
MBR735
100
1/2W
5k
1500pF
2
1
3
COMP
COLL
V+
REF
8
LT1431
4
RTOP
RMID
7
GND-S
GND-F
5
6
5V, 7A
+
3300μF

*CONTACT LTC FOR HIGH EFFICIENCY SWITCHING REGULATORS

Buck Converter Efficiency



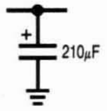
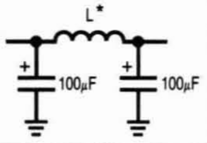
Isolated 5V to ± 15V Flyback Converter


COILTRONICS
SM-16-100-2
6, 7
4.5V – 5.5V
0.47
3k
MUR105
4, 5
+
50μF
VIN
VSW
LT1172
OR
LT1072
GND
VC
9
MUR105
– 15V, 70mA
C*
+
15k
2
10
MUR105
1
15V, 70mA
+
C*
1.5k
0.68
4N36
2.4k
0.1
20k
1
2
COLL
COMP
LT1431
V+
REF
3
8
13.3k
2.7k
GND-S
GND-F
5
6

MEASURED EFFICIENCY

LT1172	67.8%@2.2W_{OUT}
LT1072	68.6%@2.2W_{OUT}
LT1071	61.1%@4.4W_{OUT}

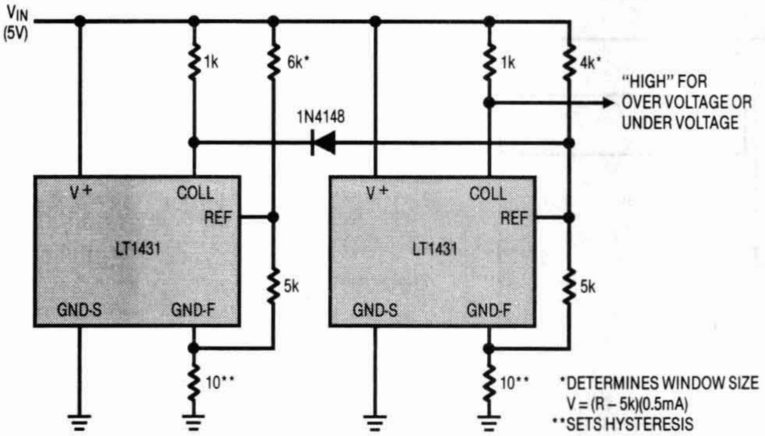
Fully Loaded Output Ripple vs Filtering

C*	LT1172	LT1072
	30mVp-p	40mVp-p
 L* + 100μF + 100μF	6mVp-p	8mVp-p

L* BELL INDUSTRIES J.W. MILLER DIVISION 9310-36 10μH, 450mA

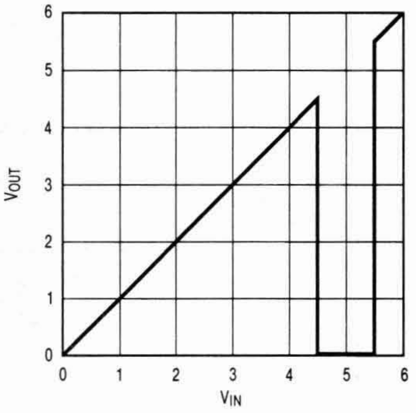
TYPICAL APPLICATIONS

5V Power Supply Monitor with ± 500mV Window and 50mV Hysteresis

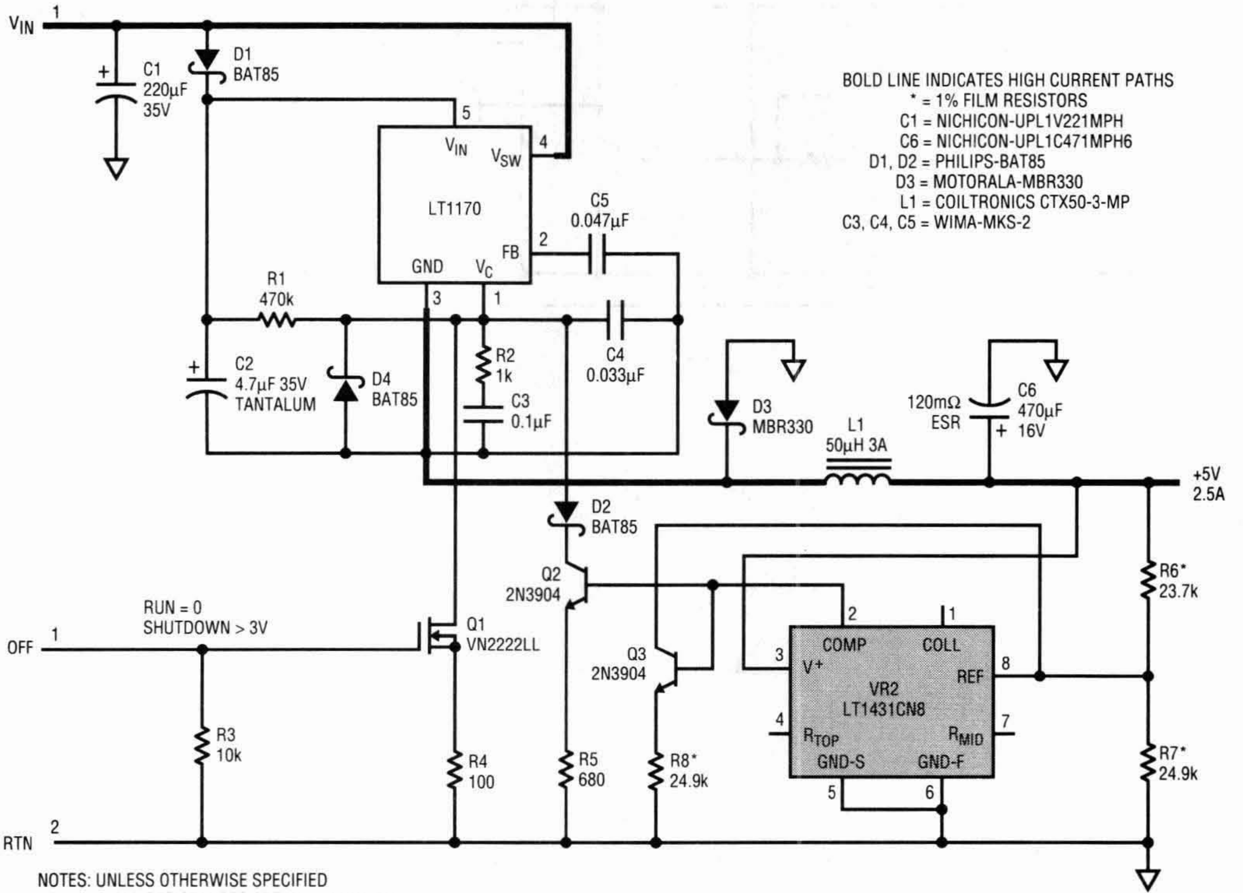

VIN (5V)
1k
6k*
1k
4k*
"HIGH" FOR OVER VOLTAGE OR UNDER VOLTAGE
1N4148
V+
COLL
REF
LT1431
GND-S
GND-F
V+
COLL
REF
LT1431
GND-S
GND-F
5k
5k
10**
10**

*DETERMINES WINDOW SIZE
V = (R – 5k)(0.5mA)
**SETS HYSTERESIS

Transfer Function



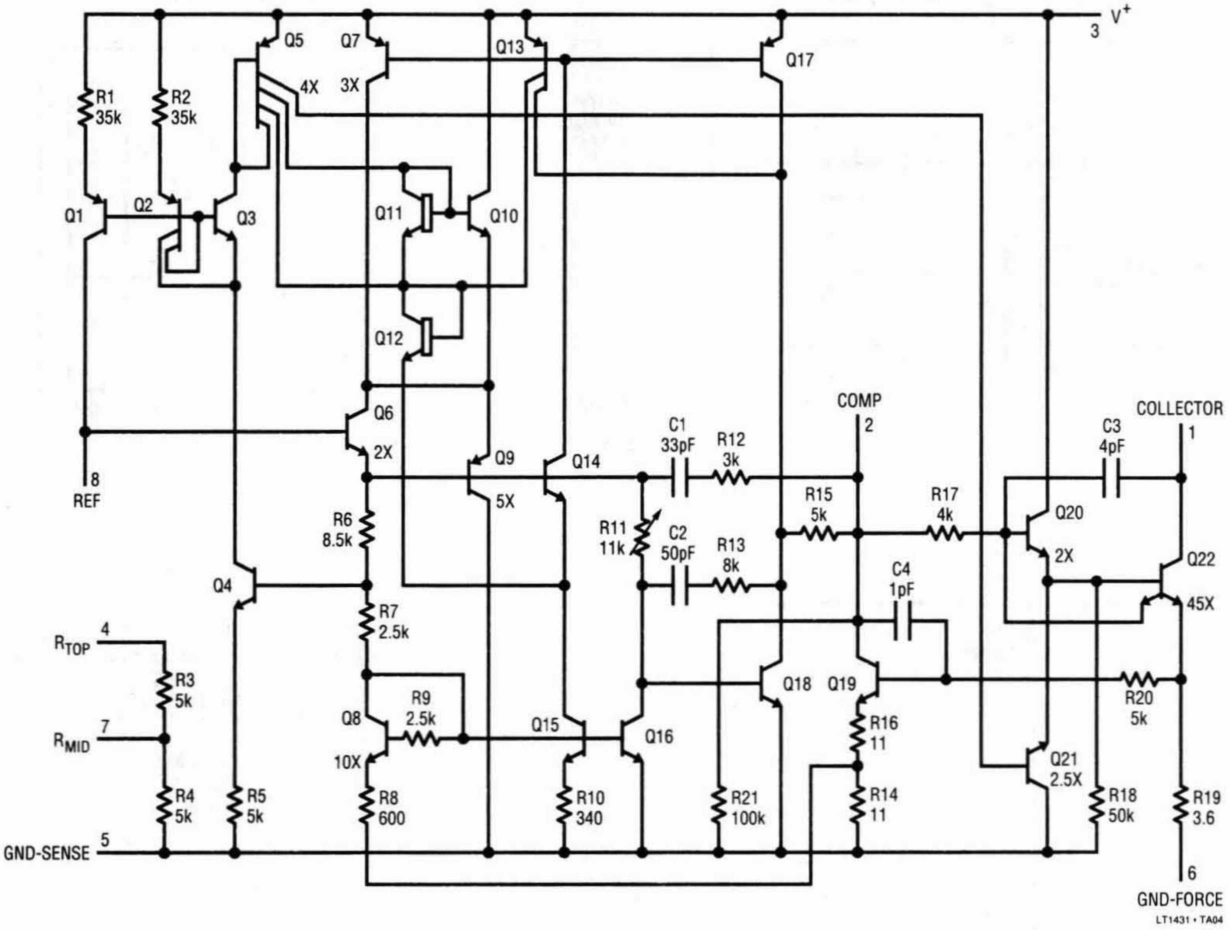
High Efficiency Buck Converter E = 85 – 89%


VIN
1
C1 220µF 35V
D1 BAT85
5
VIN
VSW
4
LT1170
C5 0.047µF
FB
2
GND
VC
3
1
R1 470k
C2 4.7µF 35V TANTALUM
D4 BAT85
R2 1k
C3 0.1µF
C4 0.033µF
D3 MBR330
L1 50µH 3A
120mΩ ESR
C6 470µF 16V
+5V 2.5A
D2 BAT85
Q2 2N3904
Q3 2N3904
2
1
COMP
COLL
3
V+
VR2 LT1431CN8
REF
8
4
RTOP
RMID
7
GND-S
GND-F
5
6
R6* 23.7k
R7* 24.9k
RUN = 0
SHUTDOWN > 3V
OFF
1
Q1 VN2222LL
R3 10k
R4 100
R5 680
R8* 24.9k
RTN
2
LT1431 • TA03

BOLD LINE INDICATES HIGH CURRENT PATHS
* = 1% FILM RESISTORS
C1 = NICHICON-UPL1V221MPH
C6 = NICHICON-UPL1C471MPH6
D1, D2 = PHILIPS-BAT85
D3 = MOTOROLA-MBR330
L1 = COILTRONICS CTX50-3-MP
C3, C4, C5 = WIMA-MKS-2

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCES ARE IN Ω, 1/4W, 5%
2. ALL CAPACITANCES ARE IN µF, 50V, 10%
3. SHUTDOWN LOGIC STATE MUST BE DEFINED BY A LOGIC GATE OR BY TYING TO GND

SCHEMATIC


V+
3
Q5
Q7
Q13
Q17
4X
3X
R1
35k
R2
35k
Q1
Q2
Q3
Q11
Q10
Q12
Q6
2X
Q9
5X
Q14
8
REF
C1
33pF
R12
3k
COMP
2
C3
4pF
COLLECTOR
1
R15
5k
R17
4k
Q20
2X
Q22
45X
R6
8.5k
R11
11k
C2
50pF
R13
8k
C4
1pF
Q4
R7
2.5k
4
RTOP
R3
5k
7
RMID
R4
5k
R5
5k
Q8
10X
R9
2.5k
R8
600
Q15
R10
340
Q16
Q18
Q19
R16
11
R14
11
R21
100k
Q21
2.5X
R18
50k
R20
5k
R19
3.6
GND-SENSE
5
6
GND-FORCE
LT1431 • TA04

SECTION 8—MONOLITHIC FILTERS

SECTION 8—MONOLITHIC FILTERS

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LTC1264-7, Linear Phase, Group Delay Equalized, 8th Order Lowpass Filter 13-84

SWITCHED CAPACITOR FILTERS

User Configured Universal Filters

- Very High Speed
  - LTC1264 (200kHz, 4 Section)
- High Speed/Low Noise
  - LTC1064 (140kHz, 4 Section)
- Medium Speed
  - LTC1059 (40kHz, 1 Section)
  - LTC1060 (20kHz, 2 Section)
  - LTC1061 (35kHz, 3 Section)
- Low Power/Low Noise
  - LTC1164 (20kHz, 4 Section)
- Semi–Custom/Low Noise
  - LTC1064-XX (4 Section)
  - LTC1064-XX (4 Section)

Lowpass Filters

- DC Accurate
  - LTC1062 (20kHz, 5th Order)
  - LTC1063 (20kHz, 5th Order)
- 8th Order Cauer/Low Noise
  - LTC1064-1 (50kHz)
  - LTC1064-4 (100kHz)
  - LTC1164-6 (20kHz; Low Power)
- 8th Order Butterworth/Low Noise
  - LTC1064-2 (Up to 140kHz)
- 8th Order Linear Phase Bessel/Low Noise
  - LTC1064-3 (Up to 100kHz)
- 8th Order Selectable Btrwth/Linear Phase
  - LTC1164-5 (Up to 20kHz, Low Noise)
- 8th Order Linear Phase and Fast Rolloff
  - LTC1264-7 (Up to 250kHz, High Speed)
  - LTC1164-7 (Up to 20kHz, Low Power)
  - LTC1064-7 (Up to 100kHz, Low Noise)

FILTER SELECTION GUIDE

INTRODUCTION

The LTC family of switched capacitor filters offers the system designer cost effective and space saving alternatives to filter designs implemented with op amps. A single IC filter can be used to replace multiple amplifiers and external capacitors.

Since their center frequencies are set by a stable external clock, switched capacitor filters virtually eliminate the temperature drift problems associated with active RC filter designs. This clock tuning also allows the adjustment of corner frequency over a wide range (greater than 10^6:1 for the LTC1064 family), permitting one filter to do the job of multiple active RC filters.

LTC's filter offerings include single, dual, triple, and quad block products and range in performance from improved replacements for the industry standard MF5 and MF10, to state-of-the-art products such as the LTC1064/1164/1264 families. The LTC1064/1164/1264 "Dash Series" products are one chip solutions requiring no external components. Our semi-custom programs offer an ASIC solution to high performance or higher volume system needs.

FEATURES

- Clock Tunable Center Frequencies
- Stable, Selectable Clock to Center Frequency Ratios
- Center Frequencies to 300kHz
- Noise Performance As Low As 80μV, Wideband
- Available with Zero DC Offset
- Filter CAD Program Available for Low-Effort Design
- Available as Universal Filter Blocks, Dedicated Filters, or Semi-Custom Fixed Filters
- Improved Replacements for Industry Standard MF5 and MF10
- Available in Surface Mount Packages

APPLICATIONS

- Antialiasing Filters
- Telecom Filters
- Spectral Analysis
- DSP
- Loop Filters
- Audio

PART NUMBER	# SECTIONS	f_0 MAX	f_0/f_{CLK}	TCf_0	SO PKG	PIN COUNT	FEATURES
LTC1059	1	40kHz	100, 50:1	5ppm/°C	Y	14	Low Noise, Low Crosstalk, Universal Filter Block
LTC1060	2	20kHz	100, 50:1	10ppm/°C	Y	20	Improved MF5 Replacement
LTC1061	3	35kHz	100, 50:1	1ppm/°C	Y	20	Improved MF10 Replacement
LTC1062	2	20kHz	100:1	10ppm/°C	Y	8	Fifth Order Low Pass Filter, No DC Offset
LTC1064	4	140kHz	100, 50:1	1ppm/°C	Y	24	Universal, Low Noise, Fast Quad Filter
LTC1064-1	4	50kHz	100:1	1ppm/°C	Y	14	Low Noise, Cauer Lowpass Filter
LTC1064-2	4	140kHz	100, 50:1	1ppm/°C	Y	14	Low Noise, High Frequency Butterworth Lowpass Filter
LTC1064-3	4	100kHz	150, 75:1	1ppm/°C	Y	14	Low Noise, Linear Phase Bessel Lowpass Filter
LTC1064-4	4	100kHz	100, 50:1	1ppm/°C	Y	14	Low Noise, High Speed Cauer Lowpass Filter
LTC1064-7	4	100kHz	100, 50:1	1ppm/°C	Y	14	Constant Group Delay, Lowpass Filter
LTC1064-XX	4	to 140kHz	100, 50:1	1ppm/°C	Y	14	Semi-Custom Low Noise, High Speed Filter
LTC1164	4	20kHz	100, 50:1	1ppm/°C	Y	24	Universal, Low Noise, Low Power, Wide Dynamic Range Filter
LTC1164-5	4	20kHz	100, 50:1	1ppm/°C	Y	14	Low Power, Butterworth/Bessel Lowpass Filter
LTC1164-7	4	20kHz	100, 50:1	1ppm/°C	Y	14	Constant Group Delay, Low Power, Lowpass Filter
LTC1164-XX	4	to 20kHz	100, 50:1	1ppm/°C	Y	14	Semi-Custom Low Noise, Low Power Filter
LTC1264	4	300kHz	20:1	1ppm/°C	Y	24	Very High Speed Universal Quad Filter
LTC1264-7	4	250kHz	50, 25:1	1ppm/°C	Y	14	Constant Group Delay, High Speed, Lowpass Filter

LINEAR TECHNOLOGY

LTC1064-2

Low Noise, High Frequency, 8th Order Butterworth Lowpass Filter

FEATURES

- 8th Order Filter in a 14-Pin Package
- 140kHz Maximum Corner Frequency
- No External Components
- 50:1 and 100:1 Clock to Cutoff Frequency Ratio
- 80μV_{RMS} Total Wideband Noise
- 0.03% THD or Better
- Operates from ±2.37V to ±8V Power Supplies

APPLICATIONS

- Antialiasing Filters
- Smoothing Filters
- Tracking High Frequency Lowpass Filters

DESCRIPTION

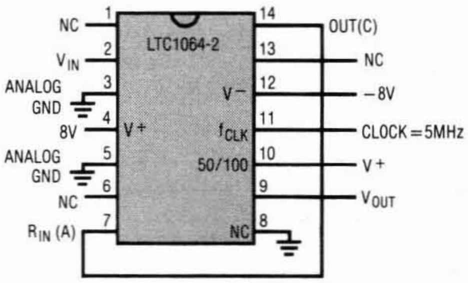
The LTC1064-2 is a monolithic 8th order lowpass Butterworth filter, which provides a maximally flat passband. The attenuation slope is −48dB/octave and the maximum attenuation is in excess of 80dB. An external TTL or CMOS clock programs the filter's cutoff frequency. The clock to cutoff frequency ratio is 100:1 (pin 10 at negative supply) or 50:1 (pin 10 at V^+). The maximum cutoff frequency is 140kHz. No external components are needed.

The LTC1064-2 features low wideband noise and low harmonic distortion even for input voltages up to $3V_{RMS}$. In fact the LTC1064-2 overall performance competes with equivalent multi-op amp RC active realizations. The LTC1064-2 is available in a 14-pin DIP or 16-pin surface mounted SOL package. The LTC1064-2 is fabricated using LTC's enhanced analog CMOS Si-gate process.

The LTC1064-2 is pin compatible with the LTC1064-1.

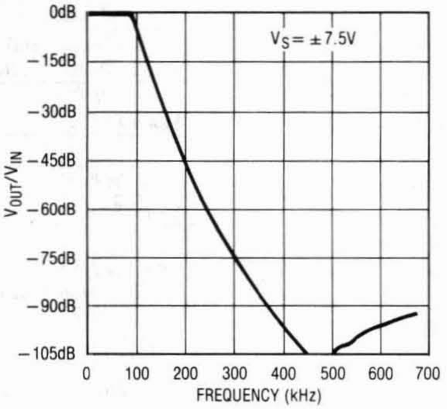
TYPICAL APPLICATION

8th Order Clock Sweepable Lowpass Butterworth Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1μF CAPACITOR CLOSE TO THE PACKAGE. THE NC PINS 1, 6, 8, AND 13 SHOULD BE PREFERABLY GROUNDED.

Measured Frequency Response

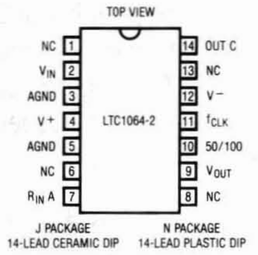


ABSOLUTE MAXIMUM RATINGS

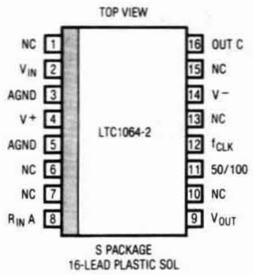
Total Supply Voltage (V+ to V−) 16.5V
Power Dissipation 400mW
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

Operating Temperature Range
LTC1064-2M.......................... −55°C to 125°C
LTC1064-2C........................... −40°C to 85°C

PACKAGE/ORDER INFORMATION


TOP VIEW
NC 1
V_{IN} 2
AGND 3
V+ 4
AGND 5
NC 6
R_{IN} A 7
14 OUT C
13 NC
12 V−
11 f_{CLK}
10 50/100
9 V_{OUT}
8 NC
LTC1064-2
J PACKAGE
14-LEAD CERAMIC DIP
N PACKAGE
14-LEAD PLASTIC DIP

ORDER PART NUMBER
LTC1064-2MJ LTC1064-2CJ LTC1064-2CN


TOP VIEW
NC 1
V_{IN} 2
AGND 3
V+ 4
AGND 5
NC 6
NC 7
R_{IN} A 8
16 OUT C
15 NC
14 V−
13 NC
12 f_{CLK}
11 50/100
10 NC
9 V_{OUT}
LTC1064-2
S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER
LTC1064-2CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, 100:1, $f_{CLK} = 2MHz$, R1 = 10kΩ, $T_A = 25°$, TTLclock input level, unless otherwise specified.

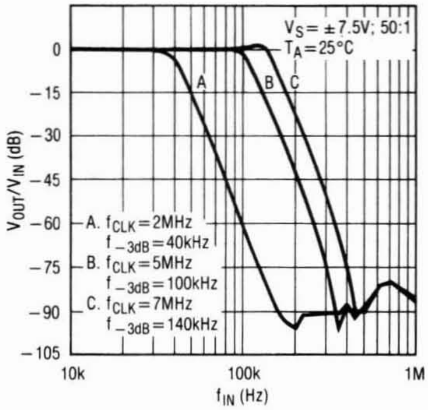
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain (Note 1)	Referenced to 0dB, 1Hz to 1kHz	●	−0.5		0.15	dB
Gain TempCo				0.0002		dB/°C
−3dB Frequency	100:1			20		kHz
	50:1			40		kHz
Gain at −3dB Frequency	Referenced to 0dB, $f_{IN} = 20kHz$	●		−3	−2.75	dB
Stopband Attenuation	At $1.5f_{-3dB}$, 50:1, $f_{IN} = 60kHz$	●	−24	−27		dB
Stopband Attenuation	At $2f_{-3dB}$, 100:1, $f_{IN} = 40kHz$	●	−44	−47		dB
Stopband Attenuation	At $3f_{-3dB}$, 100:1, $f_{IN} = 60kHz$			−74		dB
Stopband Attenuation	At $4f_{-3dB}$, 100:1, $f_{IN} = 80kHz$			−90		dB
Input Frequency Range	100:1		0		$<f_{CLK}/2$	kHz
	50:1		0		$<f_{CLK}$	kHz
Output Voltage Swing and Operating Input Voltage Range	$V_S = \pm 2.37V$	●	±1.1			V
	$V_S = \pm 5V$	●	±3.1			V
	$V_S = \pm 7.5V$	●	±5.0			V
Total Harmonic Distortion	$V_S = \pm 5V$, Input = $1V_{RMS}$ at 1kHz			0.015		%
	$V_S = \pm 7.5V$, Input = $3V_{RMS}$ at 1kHz			0.03		%
Wideband Noise	$V_S = \pm 5V$, Input = GND 1Hz-1.99MHz			80		μV_{RMS}
	$V_S = \pm 7.5V$, Input = GND 1Hz-1.99MHz			90		μV_{RMS}
Output DC Offset (Note 1)	$V_S = \pm 7.5V$			±30	±125	mV
Output DC Offset TempCo	$V_S = \pm 5V$			±90		µV/°C
Input Impedance			10	20		kΩ
Output Impedance	$f_{OUT} = 10kHz$			2		Ω
Output Short Circuit Current	Source/Sink			3/1		mA
Clock Feedthrough				200		μV_{RMS}
Maximum Clock Frequency	50% Duty Cycle, $V_S = \pm 5V$				5	MHz
	50% Duty Cycle, $T_A = 25°C$, $V_S = \pm 7.5V$				7	MHz
Power Supply Current	$V_S = \pm 2.37V$, $f_{CLK} = 1MHz$	●		11	22	mA
	$V_S = \pm 5V$, $f_{CLK} = 1MHz$			14	23	mA
		●			26	mA
	$V_S = \pm 7.5V$, $f_{CLK} = 1MHz$			17	28	mA
		●			32	mA
Power Supply Voltage Range		●	±2.37		±8	V

The ● denotes the specifications which apply over the full operating temperature range.

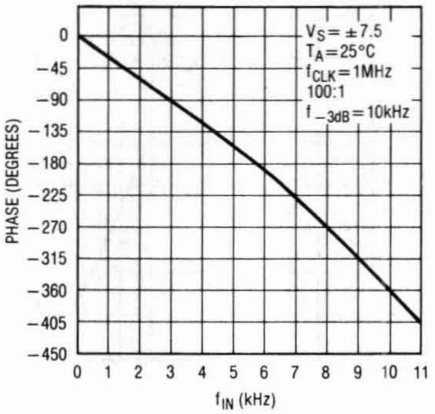
Note 1: For tighter specifications contact LTC Marketing.

TYPICAL PERFORMANCE CHARACTERISTICS

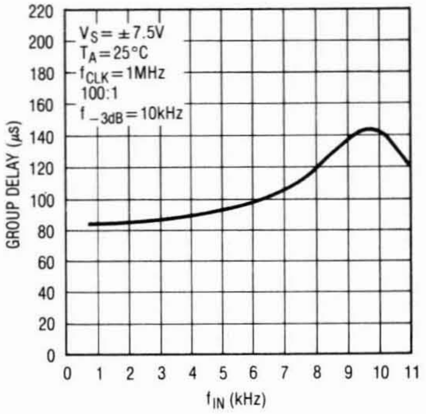
Graph 1. Amplitude Response



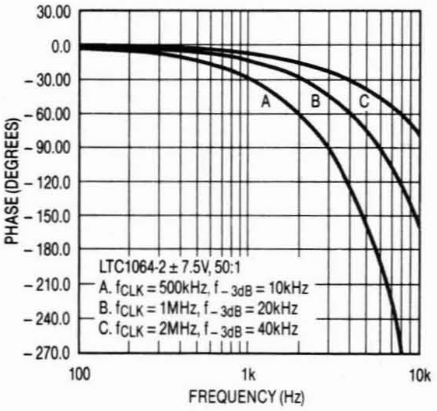
Graph 2. Phase Response



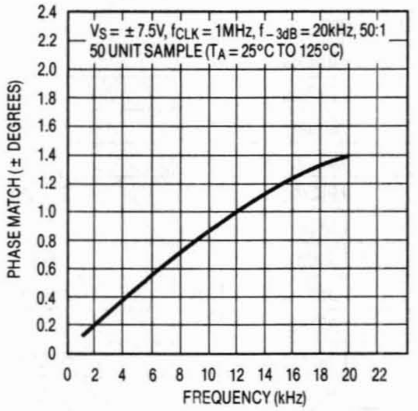
Graph 3. Group Delay vs Frequency



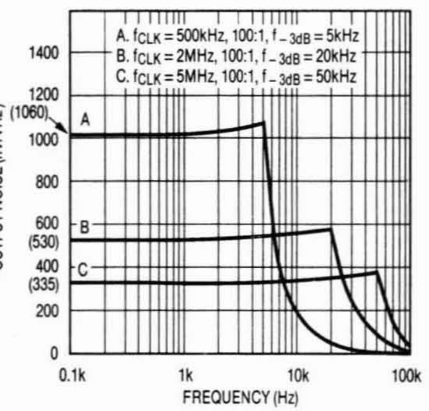
Graph 4. Phase vs f−3dB Frequency



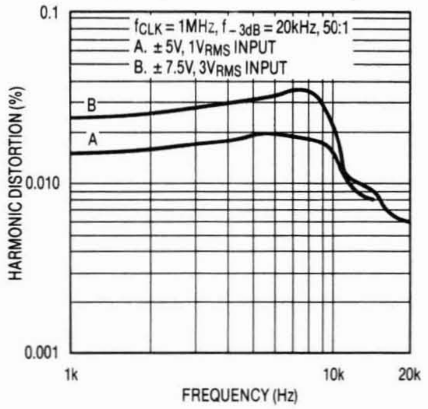
Graph 5. Phase Matching



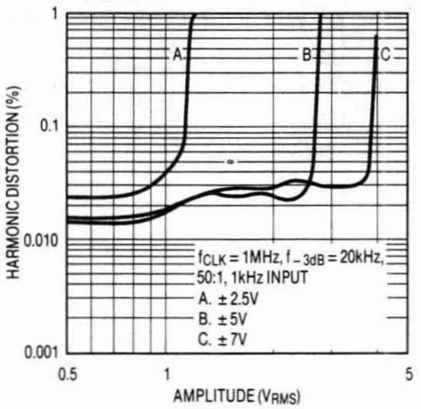
Graph 6. Noise Spectral Density



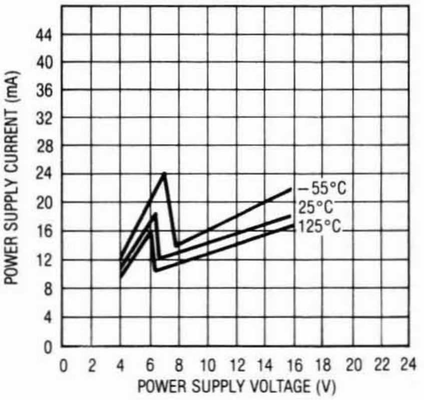
Graph 7. Harmonic Distortion vs Frequency



Graph 8. Harmonic Distortion vs Amplitude



Graph 9. Power Supply vs Current



8

TYPICAL PERFORMANCE CHARACTERISTICS

Graph 10. Amplitude Response with Pin 10 at Ground

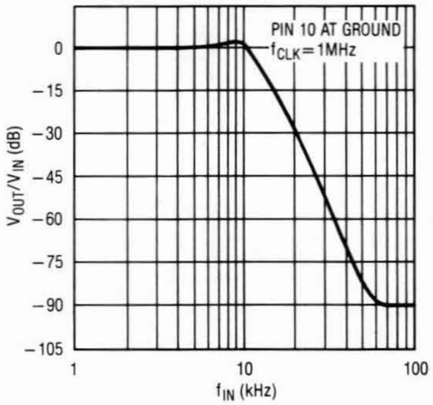


Table 1. Gain/Delay, f_{-3dB} = 1kHz, LTC1064-2 Typical Response V_S = ± 5V, T_A = 25°C f_{CLK} = 50kHz, Ratio = Pin 10 at V^+ (fltr 50:1)

FREQUENCY	GAIN	DELAY
0.200kHz	− 0.247dB	0.857ms
0.300kHz	− 0.270dB	0.872ms
0.400kHz	− 0.290dB	0.893ms
0.500kHz	− 0.300dB	0.929ms
0.600kHz	− 0.320dB	0.983ms
0.700kHz	− 0.370dB	1.071ms
0.800kHz	− 0.520dB	1.210ms
0.900kHz	− 1.200dB	1.364ms
1.000kHz	− 3.380dB	1.381ms
1.100kHz	− 7.530dB	1.192ms
1.200kHz	− 12.670dB	0.935ms

Table 3. Gain/Delay, f_{-3dB} = 1kHz, LTC1064-2 Typical Response V_S = ± 5V, T_A = 25°C f_{CLK} = 100kHz, Ratio = Pin 10 at V^- (fltr 100:1)

FREQUENCY	GAIN	DELAY
0.200kHz	− 0.213dB	0.821ms
0.300kHz	− 0.240dB	0.837ms
0.400kHz	− 0.260dB	0.858ms
0.500kHz	− 0.280dB	0.893ms
0.600kHz	− 0.310dB	0.947ms
0.700kHz	− 0.370dB	1.034ms
0.800kHz	− 0.530dB	1.172ms
0.900kHz	− 1.200dB	1.325ms
1.000kHz	− 3.370dB	1.346ms
1.100kHz	− 7.500dB	1.158ms
1.200kHz	− 12.640dB	0.899ms

Table 2. Gain, f_{-3dB} = 1kHz, LTC1064-2 Typical Response V_S = ± 5V, T_A = 25°C f_{CLK} = 50kHz, Ratio = Pin 10 at V^+ (fltr 50:1)

FREQUENCY	GAIN
0.500kHz	− 0.298dB
1.000kHz	− 3.380dB
1.500kHz	− 27.500dB
2.000kHz	− 47.200dB
2.500kHz	− 63.300dB
3.000kHz	− 75.190dB
3.500kHz	− 86.100dB
4.000kHz	− 95.310dB
4.500kHz	− 104.240dB
5.000kHz	− 109.650dB
5.500kHz	− 121.930dB
6.000kHz	− 123.920dB
6.500kHz	− 114.150dB
7.000kHz	− 116.990dB
7.500kHz	− 120.070dB
8.000kHz	− 113.470dB
8.500kHz	− 130.090dB
9.000kHz	− 114.770dB
9.500kHz	− 117.760dB

TYPICAL PERFORMANCE CHARACTERISTICS

Table 4. Gain, $f_{-3dB} = 1kHz$,
LTC1064-2 Typical Response $V_S = \pm 5V$, $T_A = 25°C$
$f_{CLK} = 100kHz$, Ratio = Pin 10 at V^- (fltr 100:1)

FREQUENCY	GAIN
0.500kHz	−0.279dB
1.000kHz	−3.370dB
1.500kHz	−27.500dB
2.000kHz	−47.200dB
2.500kHz	−62.300dB
3.000kHz	−75.130dB
3.500kHz	−86.090dB
4.000kHz	−95.210dB
4.500kHz	−103.030dB
5.000kHz	−108.690dB
5.500kHz	−114.830dB
6.000kHz	−120.540dB
6.500kHz	−114.750dB
7.000kHz	−116.430dB
7.500kHz	−120.790dB
8.000kHz	−121.290dB
8.500kHz	−119.970dB
9.000kHz	−120.020dB
9.500kHz	−125.170dB

Table 5. Gain, $f_{-3dB} = 20kHz$,
LTC1064-2 Typical Response $V_S = \pm 7.5V$, $T_A = 25°C$
$f_{CLK} = 1MHz$, Ratio = Pin 10 at V^+ (fltr 50:1)

FREQUENCY	GAIN
10.000kHz	−0.308dB
20.000kHz	−3.350dB
30.000kHz	−27.400dB
40.000kHz	−47.100dB
50.000kHz	−62.300dB
60.000kHz	−74.890dB
70.000kHz	−85.430dB
80.000kHz	−95.070dB
90.000kHz	−103.150dB
100.000kHz	−108.700dB
110.000kHz	−107.520dB
120.000kHz	−108.030dB
130.000kHz	−104.990dB
140.000kHz	−106.090dB
150.000kHz	−105.320dB

Table 6. Gain, $f_{-3dB} = 140kHz$,
LTC1064-2 Typical Response $V_S = \pm 7.5V$, $T_A = 25°C$
$f_{CLK} = 7MHz$, Ratio = Pin 10 at V^+ (fltr 50:1)

FREQUENCY	GAIN
50.000kHz	−0.238dB
60.000kHz	−0.140dB
70.000kHz	0.050dB
80.000kHz	0.350dB
90.000kHz	0.810dB
100.000kHz	1.450dB
110.000kHz	2.110dB
120.000kHz	1.830dB
130.000kHz	−0.700dB
140.000kHz	−4.840dB
150.000kHz	−9.350dB
160.000kHz	−13.690dB
170.000kHz	−17.760dB
180.000kHz	−21.600dB
190.000kHz	−25.200dB
200.000kHz	−28.500dB
210.000kHz	−31.800dB
220.000kHz	−34.800dB
230.000kHz	−37.700dB
240.000kHz	−40.500dB
250.000kHz	−43.200dB
260.000kHz	−45.700dB
270.000kHz	−48.200dB
280.000kHz	−50.500dB
290.000kHz	−52.700dB
300.000kHz	−54.900dB

TYPICAL PERFORMANCE CHARACTERISTICS

Table 7. Gain for Non-Butterworth Response (Pin 10 to GND)
LTC1064-2 Typical Response $V_S = \pm 5V$, $T_A = 25°C$
$f_{CLK} = 100kHz$

FREQUENCY	GAIN
0.500kHz	– 0.012dB
1.000kHz	1.240dB
1.500kHz	– 14.690dB
2.000kHz	– 28.600dB
2.500kHz	– 41.100dB
3.000kHz	– 52.500dB
3.500kHz	– 62.800dB
4.000kHz	– 71.500dB
4.500kHz	– 79.370dB
5.000kHz	– 86.730dB
5.500kHz	– 93.340dB
6.000kHz	– 99.350dB
6.500kHz	– 105.270dB
7.000kHz	– 113.270dB
7.500kHz	– 114.600dB
8.000kHz	– 114.010dB
8.500kHz	– 122.810dB
9.000kHz	– 122.980dB
9.500kHz	– 119.450dB

PIN DESCRIPTION

Power Supply Pins (4, 12)

The V^+ (pin 4) and V^- (pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. Low noise, non-switching power supplies are recommended. **To avoid latch up when the power supplies exhibit high turn-on transients, a 1N5817 schottky diode should be added from the V^+ and V^- pins to ground, Figures 1, 2 and 3.**

Clock Pin (11)

For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are 2.2V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 7MHz. Do not allow the clock levels to exceed the power supplies. For single supply operation ≥6V use level shifting at pin 11 with T^2L levels, see Figure 4.

Analog Ground Pins (3, 5)

For dual supply operation these pins should be connected to a ground plane. For single supply operation both pins should be tied to one half supply, Figure 3.

PIN DESCRIPTION

Connection Pins (7, 14)

A very short connection between pins 14 and 7 is recommended. This connection should be preferably done under the IC package. In a breadboard, use a one inch, or less, shielded coaxial cable; the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

Input, Output Pins (2, 9)

The input pin 2 is connected to an 18kΩ resistor tied to the inverting input of an op amp. Pin 2 is protected against static discharge. The device's output, pin 9, is the output of an op amp which can typically source/sink 3/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, pin 9, should be buffered, Figure 1. **The op amp power supply wire (or trace) should be connected directly to the power source. To eliminate switching transients from filter output, buffer filter output with a third order lowpass, see Figure 5.**

NC Pins (1, 6, 8, 13)

The "no connection" pins should be preferably grounded. These pins are not internally connected.

Ratio Pin (10)

The DC level at this pin determines the ratio of clock frequency to the −3dB frequency of the filter. The ratio is 50:1 when pin 10 is at V^+ and 100:1 when pin 10 is at V^-. This pin should be bypassed with a 0.1μF capacitor to analog ground when it's connected to V^- or V^+, Figure 1. See Tables 1 through 7 for typical gain and delay responses for the two ratios.

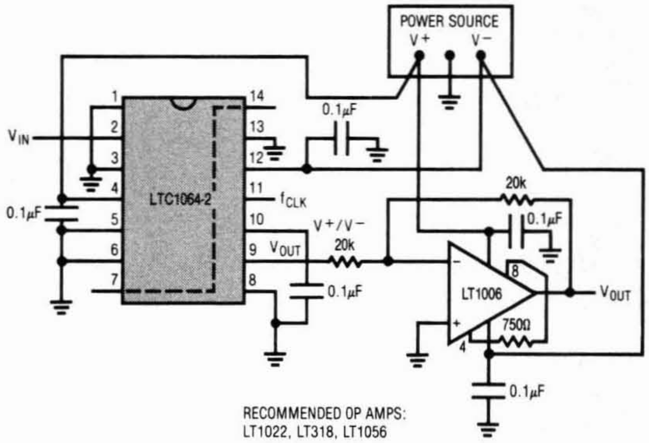

POWER SOURCE
V+
V−
VIN
0.1μF
LTC1064-2
1
2
3
4
5
6
7
14
13
12
11
10
9
8
fCLK
V+/V−
VOUT
20k
20k
0.1μF
0.1μF
LT1006
−
+
8
4
750Ω
0.1μF
VOUT
RECOMMENDED OP AMPS:
LT1022, LT318, LT1056

Figure 1. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-2 Power Lines.

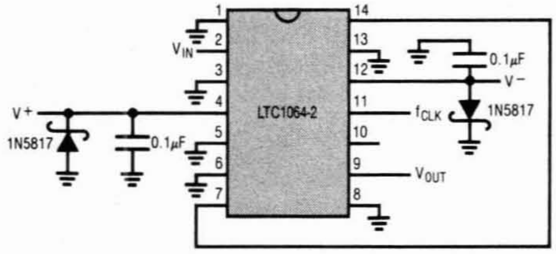

V+
1N5817
0.1μF
VIN
LTC1064-2
1
2
3
4
5
6
7
14
13
12
11
10
9
8
0.1μF
V−
fCLK
1N5817
VOUT

Figure 2. Using Schottky Diodes to Protect the IC from Transient Supply Reversal.

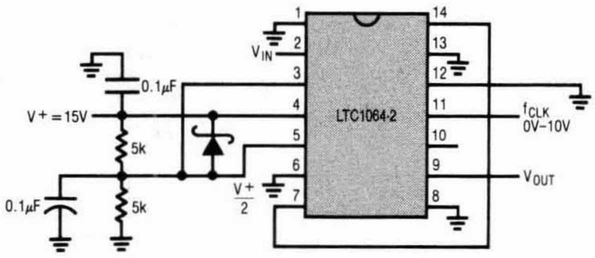

0.1μF
V+ = 15V
5k
5k
0.1μF
V+/2
VIN
LTC1064-2
1
2
3
4
5
6
7
14
13
12
11
10
9
8
fCLK
0V–10V
VOUT

Figure 3. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pins 4 and 5. For $V^+ = 5V$, Derive the Mid-Supply Voltage with a 7.5k Resistor and an LT1004 2.5V Reference.

PIN DESCRIPTION

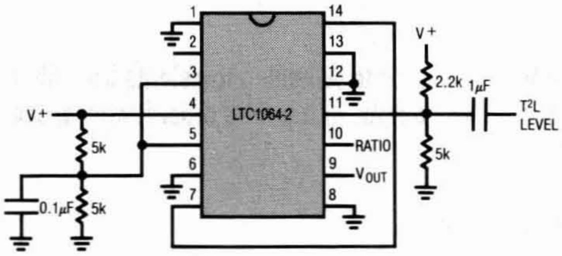

1
2
3
4
5
6
7
14
13
12
11
10
9
8
LTC1064-2
V+
5k
0.1µF
5k
RATIO
V_{OUT}
V+
2.2k
1µF
5k
T²L
LEVEL

Figure 4. Level Shifting the Input T²L Clock for Single Supply Operation ≥ 6V.

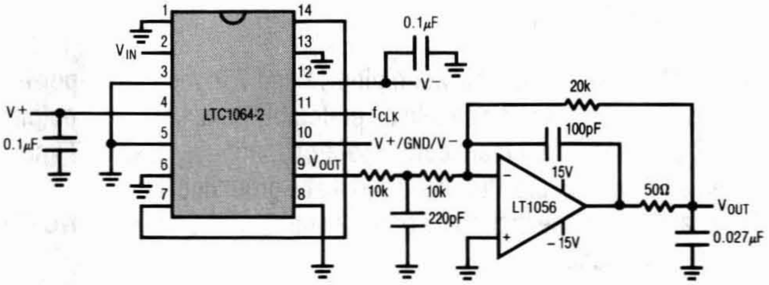

V_{IN}
1
2
3
4
5
6
7
14
13
12
11
10
9
8
LTC1064-2
V+
0.1µF
0.1µF
V−
f_{CLK}
V+/GND/V−
V_{OUT}
10k
10k
220pF
20k
100pF
15V
LT1056
−15V
50Ω
V_{OUT}
0.027µF

Figure 5. Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough. Passband ±0.1dB to 50kHz, −3dB at 94kHz.

LINEAR TECHNOLOGY

LTC1064-3

Low Noise, High Frequency, 8th Order Linear Phase Lowpass Filter

FEATURES

- 8th Order Filter in a 14-Pin Package
- 95kHz Maximum Corner Frequency
- No External Components
- 75:1, 150:1, and 120:1 Clock to Cutoff Frequency Ratio
- $60\mu V_{RMS}$ Total Wideband Noise
- 0.03% THD or Better
- Operates from ±2.37V to ±8V Power Supplies
- Low Total Output DC Offset

APPLICATIONS

- Antialiasing Filters
- Smoothing Filters
- Tracking High Frequency Lowpass Filters

DESCRIPTION

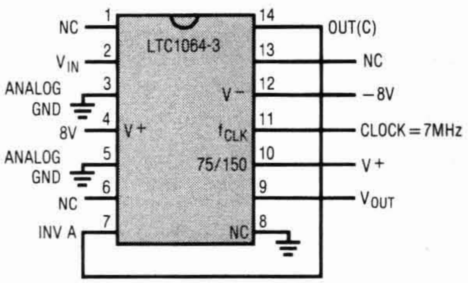
The LTC1064-3 is a monolithic 8th order lowpass Bessel filter, which provides a linear phase response over its entire passband. An external TTL or CMOS clock programs the filter's cutoff frequency. The clock to cutoff frequency ratio is 75:1 (pin 10 at V^+) or 150:1 (pin 10 at V^-) or 120:1 (pin 10 at GND). The maximum cutoff frequency is 95kHz. No external components are needed.

The LTC1064-3 features low wideband noise and low harmonic distortion even for input voltages up to $3V_{RMS}$. In fact the LTC1064-3 overall performance competes with equivalent multiple op amp RC active realizations. The LTC1064-3 is available in a 14-pin DIP or 16-pin surface mounted SOL package. The LTC1064-3 is fabricated using LTC's enhanced analog CMOS Si-gate process.

The LTC1064-3 is pin compatible with the LTC1064-1, -2, and -4.

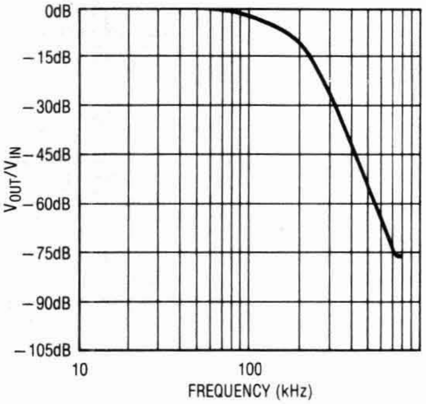
TYPICAL APPLICATION

8th Order Clock Sweepable Lowpass Bessel Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF OR LARGER CAPACITOR CLOSE TO THE PACKAGE. THE CONNECTION BETWEEN PINS 7 AND 14 SHOULD BE MADE UNDER THE I.C. PACKAGE.

Measured Frequency Response



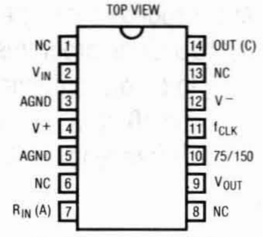
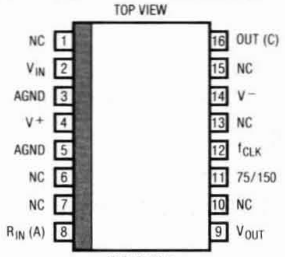
$V_S = \pm 7.5V$, $f_{CLK} = 7MHz$, PIN 10 TO V+, $f_{-3dB} = 95kHz$, GROUP DELAY = 6µs

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V$^+$ to V$^-$) 16.5V
Power Dissipation 400mW
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

Operating Temperature Range
LTC1064-3M .... – 55°C to 125°C
LTC1064-3C .... – 40°C to 85°C
Input Voltage .... (V$^+$ + 0.3V) to (V$^-$ – 0.3V)
Burn-In Voltage 15V

PACKAGE/ORDER INFORMATION

 TOP VIEW NC 1 V_{IN} 2 AGND 3 V+ 4 AGND 5 NC 6 R_{IN} (A) 7 14 OUT (C) 13 NC 12 V– 11 f_{CLK} 10 75/150 9 V_{OUT} 8 NC J PACKAGE 14-LEAD CERAMIC DIP N PACKAGE 14-LEAD PLASTIC DIP	ORDER PART NUMBER	 TOP VIEW NC 1 V_{IN} 2 AGND 3 V+ 4 AGND 5 NC 6 NC 7 R_{IN} (A) 8 16 OUT (C) 15 NC 14 V– 13 NC 12 f_{CLK} 11 75/150 10 NC 9 V_{OUT} S PACKAGE 16-LEAD PLASTIC SOL	ORDER PART NUMBER
	LTC1064-3MJ LTC1064-3CJ LTC1064-3CN		LTC1064-3CS

ELECTRICAL CHARACTERISTICS

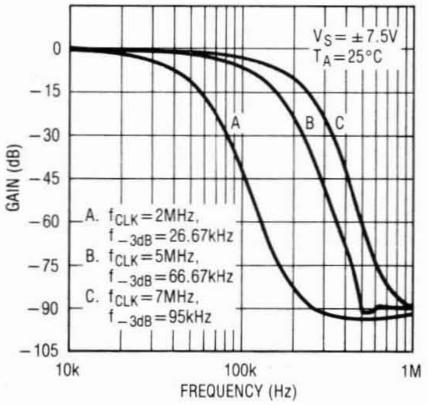
$V_S = \pm 7.5V$, 75:1, $f_{CLK} = 2MHz$, $R_I = 10k\Omega$, $T_A = 25°$, TTL or CMOS clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	Referenced to 0dB, 1Hz to 1kHz	●	– 0.5		0.15	dB
Gain TempCo				0.0002		dB/°C
– 3dB Frequency	50:1 ($f_{CLK}/f_{-3dB} = 75$)			26.67		kHz
	100:1 ($f_{CLK}/f_{-3dB} = 150$)			13.34		kHz
Gain at – 3dB Frequency	Ref. to 0dB, $f_{IN} = 26.67/13.34kHz$	●	– 3.8		– 2.75	dB
Stopband Attenuation	At $3f_{-3dB}$	●	– 25	– 29		dB
Stopband Attenuation	At $5f_{-3dB}$	●	– 56	– 60		dB
Stopband Attenuation	At $7f_{-3dB}$			– 84		dB
Input Frequency Range	100:1		0		$< f_{CLK}/2$	kHz
	50:1		0		$< f_{CLK}$	kHz
Output Voltage Swing and Operating Input Voltage Range	$V_S = \pm 2.37V$	●	± 1.1			V
	$V_S = \pm 5V$	●	± 3.1			V
	$V_S = \pm 7.5V$	●	± 5.1			V
Total Harmonic Distortion	$V_S = \pm 5V$, Input = $1V_{RMS}$ at 1kHz			0.015		%
	$V_S = \pm 7.5V$, Input = $3V_{RMS}$ at 1kHz			0.03		%
Wideband Noise	$V_S = \pm 5V$, Input = GND 1Hz-1.99MHz			55		μV_{RMS}
	$V_S = \pm 7.5V$, Input = GND 1Hz-1.99MHz			60		μV_{RMS}
Output DC Offset	$V_S = \pm 7.5V$			± 30	± 150	mV
Output DC Offset TempCo	$V_S = \pm 5V$			± 20		μV/°C
	$V_S = \pm 7.5V$			± 50		μV/°C
Input Impedance			14	22		kΩ
Output Impedance	$f_{OUT} = 10kHz$			2		Ω
Output Short Circuit Current	Source/Sink			3/1		mA
Clock Feedthrough				200		μV_{RMS}
Maximum Clock Frequency	$V_S > \pm 7V$ 50% Duty Cycle				5	MHz
	$V_S > \pm 7V$ 50% Duty Cycle, $T_A < 55°C$				7	MHz
Power Supply Current	$V_S = \pm 2.37V$, $f_{CLK} = 1MHz$	●		10	18	mA
	$V_S = \pm 5V$, $f_{CLK} = 1MHz$			12	20	mA
		●			24	mA
	$V_S = \pm 7.5V$, $f_{CLK} = 1MHz$			16	24	mA
		●			32	mA
Power Supply Voltage Range		●	± 2.37		± 8	V

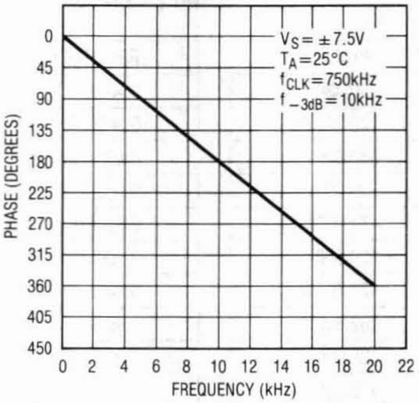
The ● denotes the specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

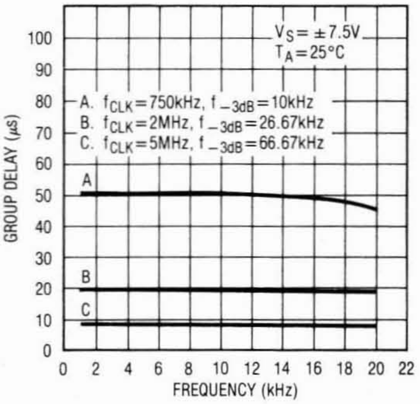
Graph 1. Gain vs Frequency



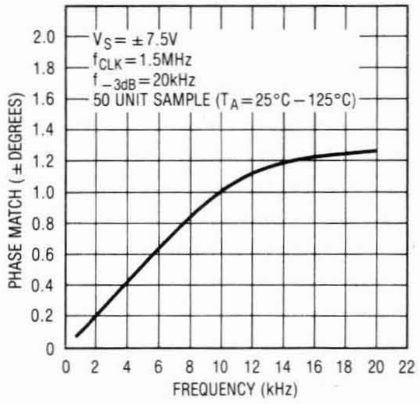
Graph 2. Phase vs Frequency



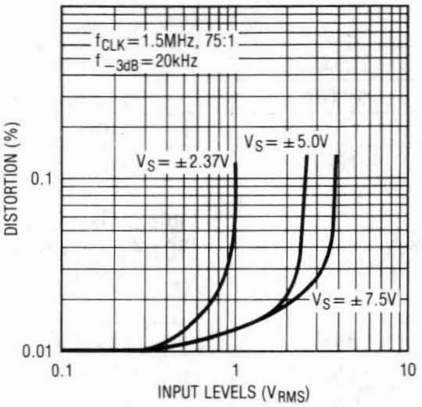
Graph 3. Group Delay



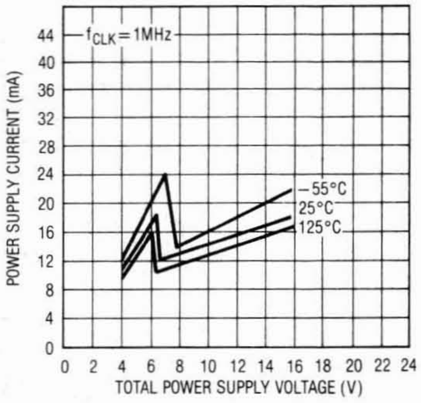
Graph 4. Phase Matching



Graph 5. Total Harmonic Distortion



Graph 6. Power Supply Current vs Power Supply Voltage



Graph 7. Transient Response Input 10Vp-p Square Wave $V_S = \pm 7.5V$, Pin 10 to V^+, $f_{CLK} = 1.5MHz$

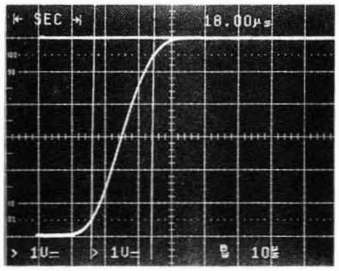


Table 1. Wideband Noise (μV_{RMS})

		$V_S = \pm 2.37V$	$V_S = \pm 5V$	$V_S = \pm 7.5V$
PIN 10 TO	**f_{CLK}/f_{-3dB}**	**NOISE μV_{RMS}**	**NOISE μV_{RMS}**	**NOISE μV_{RMS}**
V^+	75/1	50	55	60
V^-	150/1	52	58	62
GND	120/1	45	50	54

TYPICAL PERFORMANCE CHARACTERISTICS

**Table 2. Gain/Phase, $f_{-3dB} = 1kHz$,
LTC1064-3 Typical Response $V_S = \pm 5V$, $T_A = 25°C$
$f_{CLK} = 75kHz$, Pin 10 at V^+ (fltr 75:1)**

FREQUENCY	GAIN	PHASE
0.500kHz	−0.858dB	−90.430 deg
1.000kHz	−2.990dB	179.200 deg
1.500kHz	−6.840dB	89.600 deg
2.000kHz	−12.780dB	3.800 deg
2.500kHz	−20.800dB	−71.000 deg
3.000kHz	−29.900dB	−129.600 deg
3.500kHz	−38.800dB	−173.700 deg
4.000kHz	−47.100dB	152.600 deg
4.500kHz	−54.700dB	126.000 deg
5.000kHz	−61.600dB	103.300 deg
5.500kHz	−68.000dB	85.190 deg
6.000kHz	−73.840dB	69.060 deg
6.500kHz	−79.250dB	54.780 deg
7.000kHz	−84.230dB	42.440 deg
7.500kHz	−88.940dB	30.060 deg
8.000kHz	−93.360dB	21.300 deg
8.500kHz	−97.510dB	10.000 deg
9.000kHz	−100.880dB	1.520 deg
9.500kHz	−105.780dB	−7.820 deg

**Table 3. Gain/Delay, $f_{-3dB} = 1kHz$,
LTC1064-3 Typical Response $V_S = \pm 5V$, $T_A = 25°C$
$f_{CLK} = 75kHz$, Pin 10 at V^+ (fltr 75:1)**

FREQUENCY	GAIN	DELAY
0.200kHz	−0.281dB	0.502ms
0.300kHz	−0.420dB	0.503ms
0.400kHz	−0.610dB	0.503ms
0.500kHz	−0.860dB	0.502ms
0.600kHz	−1.160dB	0.502ms
0.700kHz	−1.530dB	0.502ms
0.800kHz	−1.950dB	0.503ms
0.900kHz	−2.430dB	0.503ms
1.000kHz	−2.990dB	0.500ms
1.100kHz	−3.610dB	0.500ms
1.200kHz	−4.300dB	0.500ms
1.300kHz	−5.060dB	0.498ms
1.400kHz	−5.920dB	0.495ms
1.500kHz	−6.830dB	0.491ms
1.600kHz	−7.840dB	0.489ms
1.700kHz	−8.930dB	0.481ms
1.800kHz	−10.130dB	0.473ms
1.900kHz	−11.410dB	0.465ms
2.000kHz	−12.780dB	0.454ms

**Table 4. Gain/Phase, $f_{-3dB} = 1kHz$,
LTC1064-3 Typical Response $V_S = \pm 5V$, $T_A = 25°C$
$f_{CLK} = 150kHz$, Pin 10 at V^- (fltr 150:1)**

FREQUENCY	GAIN	PHASE
0.500kHz	−0.955dB	−88.100 deg
1.000kHz	−3.380dB	−175.300 deg
1.500kHz	−7.570dB	99.700 deg
2.000kHz	−13.770dB	20.100 deg
2.500kHz	−21.800dB	−48.000 deg
3.000kHz	−30.700dB	−100.700 deg
3.500kHz	−39.400dB	−139.900 deg
4.000kHz	−47.600dB	−169.200 deg
4.500kHz	−55.100dB	168.300 deg
5.000kHz	−61.900dB	150.300 deg
5.500kHz	−68.260dB	135.830 deg
6.000kHz	−74.050dB	123.660 deg
6.500kHz	−79.450dB	113.440 deg
7.000kHz	−84.330dB	104.440 deg
7.500kHz	−89.010dB	97.670 deg
8.000kHz	−93.250dB	91.580 deg
8.500kHz	−97.340dB	84.670 deg
9.000kHz	−101.390dB	74.600 deg
9.500kHz	−104.980dB	75.990 deg

**Table 5. Gain/Delay, $f_{-3dB} = 1kHz$,
LTC1064-3 Typical Response $V_S = \pm 5V$, $T_A = 25°C$
$f_{CLK} = 150kHz$, Pin 10 at V^- (fltr 150:1)**

FREQUENCY	GAIN	DELAY
0.200kHz	−0.284dB	0.490ms
0.300kHz	−0.450dB	0.489ms
0.400kHz	−0.670dB	0.489ms
0.500kHz	−0.960dB	0.487ms
0.600kHz	−1.310dB	0.487ms
0.700kHz	−1.730dB	0.485ms
0.800kHz	−2.210dB	0.484ms
0.900kHz	−2.750dB	0.482ms
1.000kHz	−3.380dB	0.478ms
1.100kHz	−4.070dB	0.478ms
1.200kHz	−4.820dB	0.475ms
1.300kHz	−5.660dB	0.470ms
1.400kHz	−6.580dB	0.467ms
1.500kHz	−7.570dB	0.463ms
1.600kHz	−8.640dB	0.456ms
1.700kHz	−9.790dB	0.448ms
1.800kHz	−11.050dB	0.438ms
1.900kHz	−12.360dB	0.428ms
2.000kHz	−13.770dB	0.417ms

TYPICAL PERFORMANCE CHARACTERISTICS

Table 6. Gain/Phase, f_{-3dB} = 1kHz,
LTC1064-3 Typical Response V_S = ± 5V, T_A = 25°C
f_{CLK} = 120kHz, Pin 10 at GND (fltr 120:1)

FREQUENCY	GAIN	PHASE
0.500kHz	– 0.994dB	– 82.210 deg
1.000kHz	– 3.050dB	– 162.800 deg
1.500kHz	– 6.520dB	116.700 deg
2.000kHz	– 12.180dB	40.200 deg
2.500kHz	– 19.460dB	– 23.600 deg
3.000kHz	– 27.200dB	– 74.000 deg
3.500kHz	– 34.700dB	– 114.200 deg
4.000kHz	– 41.900dB	– 146.800 deg
4.500kHz	– 48.700dB	– 173.300 deg
5.000kHz	– 55.100dB	164.700 deg
5.500kHz	– 60.900dB	145.800 deg
6.000kHz	– 66.500dB	130.610 deg
6.500kHz	– 71.660dB	117.130 deg
7.000kHz	– 76.390dB	105.880 deg
7.500kHz	– 80.910dB	96.140 deg
8.000kHz	– 84.900dB	87.510 deg
8.500kHz	– 88.750dB	81.380 deg
9.000kHz	– 92.410dB	78.190 deg
9.500kHz	– 98.290dB	52.860 deg

Table 7. Gain/Delay, f_{-3dB} = 1kHz,
LTC1064-3 Typical Response V_S = ± 5V, T_A = 25°C
f_{CLK} = 120kHz, Pin 10 at GND (fltr 120:1)

FREQUENCY	GAIN	DELAY
0.200kHz	– 0.354dB	0.458ms
0.300kHz	– 0.520dB	0.456ms
0.400kHz	– 0.730dB	0.454ms
0.500kHz	– 1.000dB	0.452ms
0.600kHz	– 1.320dB	0.449ms
0.700kHz	– 1.670dB	0.448ms
0.800kHz	– 2.090dB	0.446ms
0.900kHz	– 2.540dB	0.446ms
1.000kHz	– 3.050dB	0.445ms
1.100kHz	– 3.600dB	0.446ms
1.200kHz	– 4.220dB	0.449ms
1.300kHz	– 4.900dB	0.448ms
1.400kHz	– 5.670dB	0.447ms
1.500kHz	– 6.520dB	0.446ms
1.600kHz	– 7.470dB	0.441ms
1.700kHz	– 8.500dB	0.432ms
1.800kHz	– 9.650dB	0.422ms
1.900kHz	– 10.870dB	0.409ms
2.000kHz	– 12.180dB	0.395ms

Table 8. Gain/Phase, f_{-3dB} = 20kHz,
LTC1064-3 Typical Response V_S = ± 7.5V,
f_{CLK} = 1.5MHz, Pin 10 at V^+ (fltr 75:1)

T_A = 25°C

FREQUENCY	GAIN	PHASE
10.000kHz	– 0.912dB	– 92.270 deg
20.000kHz	– 3.090dB	176.000 deg
30.000kHz	– 6.910dB	85.500 deg
40.000kHz	– 12.710dB	– 1.200 deg
50.000kHz	– 20.500dB	– 77.800 deg
60.000kHz	– 29.400dB	– 138.700 deg
70.000kHz	– 38.300dB	174.600 deg
80.000kHz	– 46.500dB	138.300 deg
90.000kHz	– 54.000dB	109.100 deg
100.000kHz	– 61.000dB	84.800 deg
110.000kHz	– 67.310dB	64.040 deg
120.000kHz	– 73.170dB	46.260 deg
130.000kHz	– 78.600dB	31.120 deg
140.000kHz	– 83.760dB	18.050 deg
150.000kHz	– 88.630dB	7.770 deg

T_A = 125°C

FREQUENCY	GAIN	PHASE
10.000kHz	– 0.944dB	– 92.880 deg
20.000kHz	– 3.170dB	175.500 deg
30.000kHz	– 6.910dB	85.700 deg
40.000kHz	– 12.450dB	– 0.600 deg
50.000kHz	– 19.920dB	– 78.000 deg
60.000kHz	– 28.500dB	– 140.700 deg
70.000kHz	– 37.200dB	170.500 deg
80.000kHz	– 45.300dB	132.200 deg
90.000kHz	– 52.700dB	100.900 deg
100.000kHz	– 59.600dB	74.900 deg
110.000kHz	– 65.900dB	52.600 deg
120.000kHz	– 71.750dB	32.850 deg
130.000kHz	– 77.170dB	15.840 deg
140.000kHz	– 82.370dB	1.130 deg
150.000kHz	– 87.400dB	– 11.380 deg

PIN DESCRIPTION

Power Supply Pins (4, 12)

The V$^+$ (pin 4) and V$^-$ (pin 12) should be bypassed with a 0.1μF capacitor to an adequate analog ground. Low noise, non-switching power supplies are recommended. **To avoid latch up when the power supplies exhibit high turn-on transients, a 1N5817 schottky diode should be added from the V$^+$ and V$^-$ pins to ground, Figures 1, 2 and 3.**

Clock Pin (11)

For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are 2.2V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 7MHz. Do not allow the clock levels to exceed the power supplies. For single supply operation ≥6V use level shifting at pin 11 with T^{2}L levels, see Figure 4.

Analog Ground Pins (3, 5)

For dual supply operation these pins should be connected to a ground plane. For single supply operation both pins should be tied to one half supply, Figure 3.

Connection Pins (7, 14)

A very short connection between pins 14 and 7 is recommended. This connection should be preferably done under the IC package. In a breadboard, use a one inch, or less, shielded coaxial cable; the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

Input, Output Pins (2, 9)

The input pin 2 is connected to an 18kΩ resistor tied to the inverting input of an op amp. Pin 2 is protected against static discharge. The device's output, pin 9, is the output of an op amp which can typically source/sink 3/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, pin 9, should be buffered, Figure 1. **The op amp power supply wire (or trace) should be connected directly to the power source. To eliminate switching transients from filter output, buffer filter output with a third order lowpass, see Figure 5.**

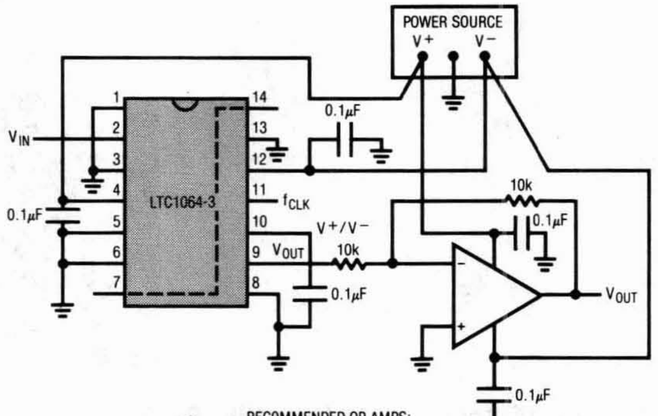
NC Pins (1, 6, 8, 13)

The "no connection" pins should be preferably grounded. These pins are not internally connected.

Ratio Pin (10)

The DC level at this pin determines the ratio of clock frequency to the −3dB frequency of the filter. The ratio is 75:1 when pin 10 is at V$^+$, 120:1 when pin 10 is at GND and 150:1 when pin 10 is at V$^-$. This pin should be bypassed with a 0.1μF capacitor to analog ground when it's connected to V$^-$ or V$^+$, Figure 1. See Tables 2 through 8 for typical gain, phase and delay responses for the three ratios.

PIN DESCRIPTION


POWER SOURCE
V+
V−
LTC1064-3
VIN
0.1μF
0.1μF
0.1μF
0.1μF
0.1μF
10k
10k
fCLK
V+/V−
VOUT
VOUT
1
2
3
4
5
6
7
8
9
10
11
12
13
14

RECOMMENDED OP AMPS:
LT1022, LT318, LT1056

Figure 1. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-3 Power Lines.

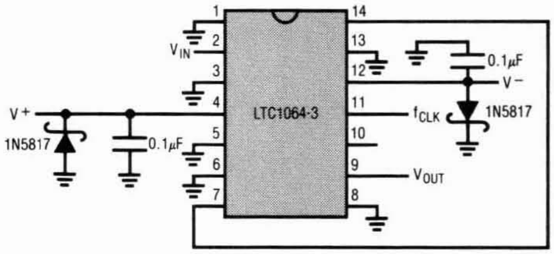

LTC1064-3
VIN
V+
V−
1N5817
1N5817
0.1μF
0.1μF
fCLK
VOUT
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 2. Using Schottky Diodes to Protect the IC from Transient Supply Reversal.

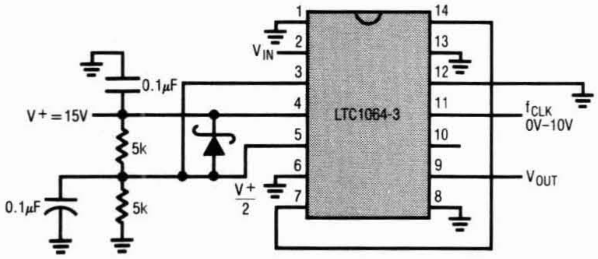

LTC1064-3
VIN
V+ = 15V
0.1μF
0.1μF
5k
5k
V+/2
fCLK 0V–10V
VOUT
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 3. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pins 4 and 5.

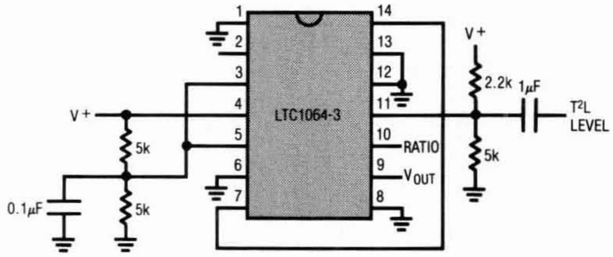

LTC1064-3
V+
V+
5k
5k
5k
2.2k
1μF
0.1μF
T²L LEVEL
RATIO
VOUT
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 4. Level Shifting the Input T²L Clock for Single Supply Operation ≥ 6V.

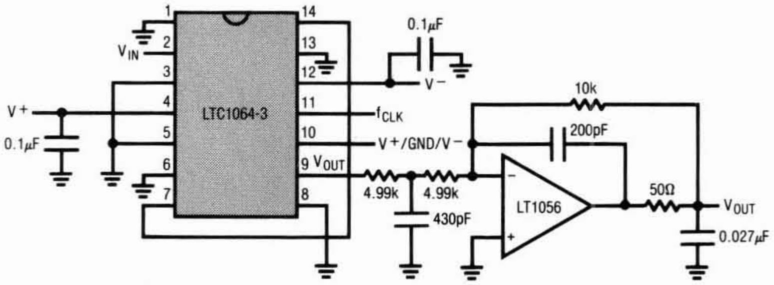

LTC1064-3
VIN
V+
V−
0.1μF
0.1μF
fCLK
V+/GND/V−
VOUT
10k
200pF
4.99k
4.99k
430pF
LT1056
50Ω
VOUT
0.027μF
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 5. Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough. Passband ±0.1dB to 50kHz, −3dB at 94kHz.

TYPICAL APPLICATION

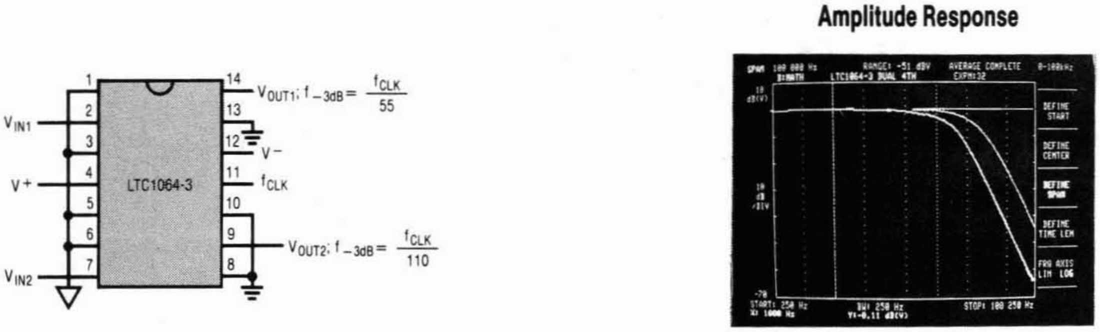

1
2
3
4
5
6
7
14
13
12
11
10
9
8
V_{IN1}
V^+
V_{IN2}
LTC1064-3
V_{OUT1}; $f_{-3dB} = \frac{f_{CLK}}{55}$
V^-
f_{CLK}
V_{OUT2}; $f_{-3dB} = \frac{f_{CLK}}{110}$
Amplitude Response
SPAN 100 000 Hz
B:MATH
RANGE: -51 dBV
LTC1064-3 DUAL 4TH
AVERAGE COMPLETE
EXPN:32
0-100kHz
10 dB(V)
10 dB /DIV
-70
START: 250 Hz
X: 1000 Hz
BW: 250 Hz
Y:-0.11 dB(V)
STOP: 100 250 Hz
DEFINE START
DEFINE CENTER
DEFINE SPAN
DEFINE TIME LEN
FRQ AXIS LIN LOG

Figure 6. Dual 4th Order Bessel Filters. V_S = ± 7.5V, f_{CLK} = 1MHz, Pin 10 to GND. f_{-3dB} = 9kHz and 18kHz.

LTC1064-4

Low Noise, 8th Order, Clock Sweepable Cauer Lowpass Filter

FEATURES

- 8th Order Filter in a 14-Pin Package
- 80dB or More Stopband Attenuation at 2 × f_{CUTOFF}
- 50:1 f_{CLOCK} to f_{CUTOFF} Ratio (Cauer)
  100:1 f_{CLOCK} to f_{-3dB} Ratio (Transitional)
- 135μV_{RMS} Total Wideband Noise
- 0.03% THD or Better
- 100kHz Maximum f_{CUTOFF} Frequency
- Operates up to ± 8V Power Supplies
- Input Frequency Range up to 50 Times the Filter Cutoff Frequency

APPLICATIONS

- Antialiasing Filters
- Telecom Filters
- Sinewave Generators

DESCRIPTION

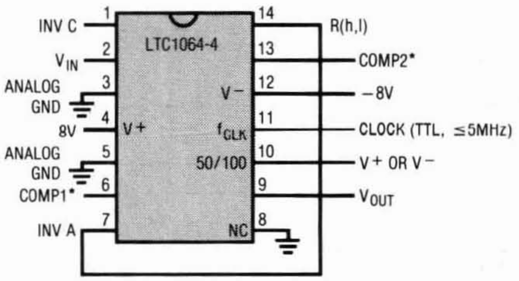
The LTC1064-4 is an 8th order, clock sweepable Cauer lowpass switched capacitor filter. An external TTL or CMOS clock programs the value of the filter's cutoff frequency. With pin 10 at V^+, the f_{CLOCK} to f_{CUTOFF} ratio is 50:1; the filter has a Cauer response and with compensation the passband ripple is ±0.1dB. The stopband attenuation is 80dB at 2 × f_{CUTOFF}. Cutoff frequencies up to 100kHz can be achieved. With pin 10 at V^-, the f_{CLOCK} to f_{-3dB} ratio is 100:1, the filter has a transitional Butterworth-Cauer response with lower noise and lower delay nonlinearity than the Cauer response. The stopband attenuation at 2.5 × f_{-3dB} is 92dB. Cutoff frequencies up to 50kHz can be achieved.

The LTC1064-4 features low noise and low harmonic distortion even when input voltages up to 3V_{RMS} are applied. The LTC1064-4 overall performance competes with equivalent multi-op amp active realizations. The LTC1064-4 is pin compatible with the LTC1064-1, LTC1064-2, and LTC1064-3.

The LTC1064-4 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

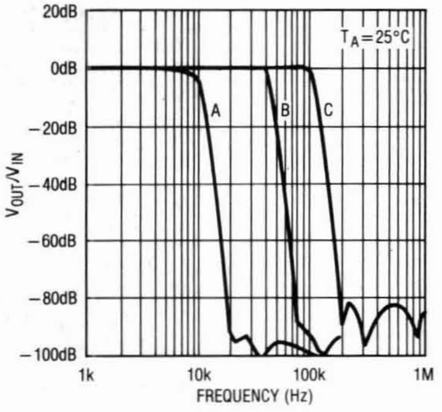
TYPICAL APPLICATION

8th Order Clock Sweepable Lowpass Elliptic Filter



*FOR FREQUENCIES ABOVE 20kHz AND MINIMUM PASSBAND RIPPLE REFER TO THE PIN DESCRIPTION SECTION FOR COMPENSATION GUIDELINES.
NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR CLOSE TO THE PACKAGE.
BYPASSING PIN 10 WITH 0.1µF CAPACITOR REDUCES CLOCK FEEDTHROUGH.
THE CONNECTION BETWEEN PINS 7 AND 14 SHOULD BE PHYSICALLY DONE UNDER THE PACKAGE.

Frequency Response

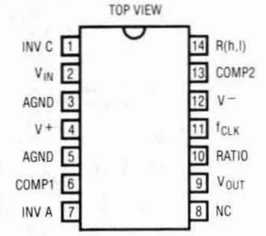
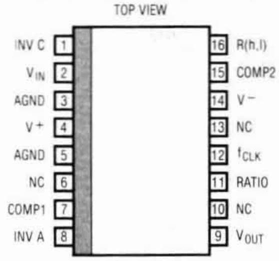


CURVE A: f_{CLK} = 1MHz, 100:1
CURVE B: f_{CLK} = 2MHz, 50:1
CURVE C: f_{CLK} = 5MHz, 50:1
C_{COMP1} = 30pF
C_{COMP2} = 18pF

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Input Voltage at Any Pin ......$V^- - 0.3V \leq V_{IN} \leq V^+ + 0.3V$
Power Dissipation 400mW
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C
Operating Temperature Range
LTC1064-4M .... – 55°C to 125°C
LTC1064-4C .... – 40°C to 85°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
 J PACKAGE 14-LEAD CERAMIC DIP N PACKAGE 14-LEAD PLASTIC DIP	LTC1064-4MJ LTC1064-4CJ LTC1064-4CN	 S PACKAGE 16-LEAD PLASTIC SOL	LTC1064-4CS

ELECTRICAL CHARACTERISTICS

$V_S = \pm 7.5V$, 50:1, $f_{CLK} = 1MHz$, $f_C = 20kHz$, $R_l = 10k\Omega$, $T_A = 25°$, TTL clock input level unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	Referenced to 0dB, 1Hz – $0.05f_{CUTOFF}$	●	– 0.5		0.1	dB
Gain TempCo				0.0002		dB/°C
Passband Edge Frequency, f_C				20 ± 1%		kHz
Gain at f_C	Referenced to Passband Gain, $f_C = 20kHz$	●	– 0.4		0.7	dB
– 3dB Frequency	50:1 (Cauer Response)			21.5		kHz
	100:1 (Transitional Response)			10		kHz
Passband Ripple (Note 1)	$0.1f_C$ to $0.95f_C$ Referenced to Passband Gain	●	0		0.75	dB
Stopband Attenuation	At $1.7f_{CUTOFF}$	●	– 56	– 60		dB
Stopband Attenuation	At $2f_{CUTOFF}$			– 80		dB
Input Frequency Range	50:1, Pin 10 at V^+		0		f_{CLK}	kHz
	100:1, Pin 10 at V^-		0		$f_{CLK}/2$	kHz
Output Voltage Swing and	$V_S = \pm 2.37V$	●	± 1.1			V
Operating Input Voltage Range	$V_S = \pm 5V$	●	± 3.1			V
	$V_S = \pm 7.5V$	●	± 5.0			V
Total Harmonic Distortion	$V_S = \pm 5V$, Input = $1V_{RMS}$ at 1kHz			0.015		%
	$V_S = \pm 7.5V$, Input = $3V_{RMS}$ at 1kHz			0.03		%
Wideband Noise	$V_S = \pm 5V$, Input = GND 1Hz-999kHz			120		μV_{RMS}
	$V_S = \pm 7.5V$, Input = GND 1Hz-999kHZ			135		μV_{RMS}
Output DC Offset	$V_S = \pm 7.5V$			± 50	± 160	mV
Output DC Offset TempCo	$V_S = \pm 5V$			– 100		$\mu V/°C$
	$V_S = \pm 7.5V$			– 200		$\mu V/°C$
Input Impedance			9	13		kΩ
Output Impedance	$f_{OUT} = 10kHz$			2		Ω
Output Short Circuit Current	Source/Sink			3/1		mA
Clock Feedthrough	Input = GND			200		μV_{RMS}
Maximum Clock Frequency	50% Duty Cycle, $V_S = \pm 7.5V$ (Note 2)				5	MHz
Power Supply Current	$V_S = \pm 2.37V$, $f_{CLK} = 1MHz$	●		11	18	mA
	$V_S = \pm 5V$, $f_{CLK} = 1MHz$			14	20	mA
		●			24	mA
	$V_S = \pm 7.5V$, $f_{CLK} = 1MHz$			17	24	mA
		●			32	mA
Power Supply Voltage Range		●	± 2.37		± 8	V

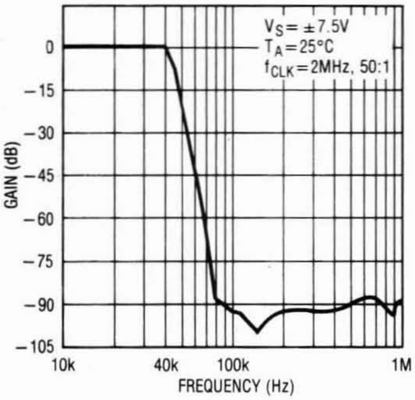
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: For tighter passband ripple specifications please consult with LTC's marketing.

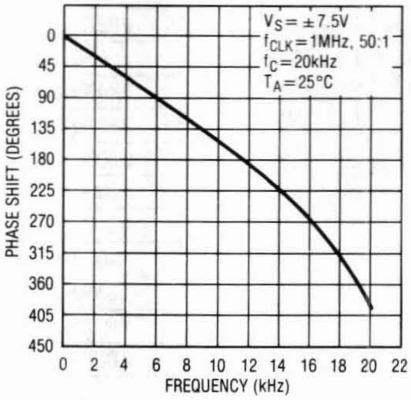
Note 2: Not tested, guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

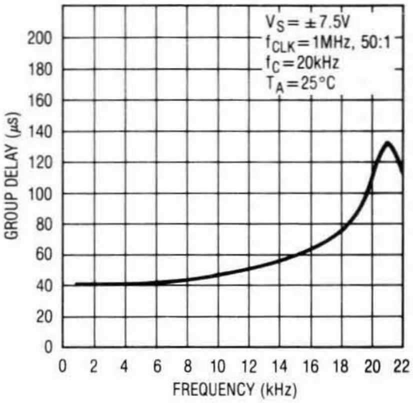
Graph 1. Gain vs Frequency



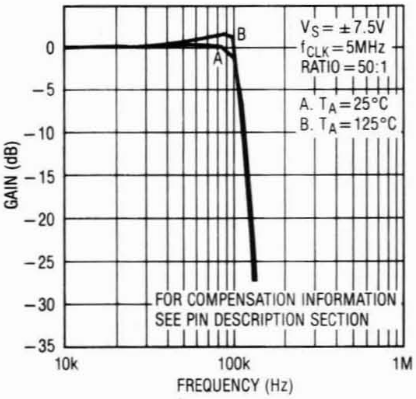
Graph 2. Passband Phase Shift vs Frequency



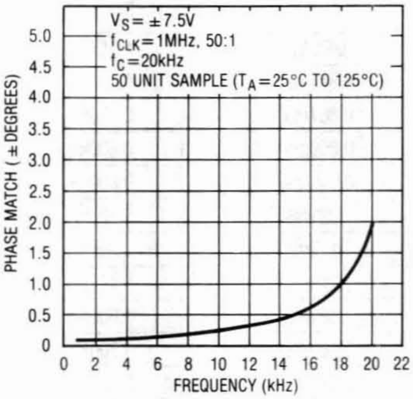
Graph 3. Passband Group Delay



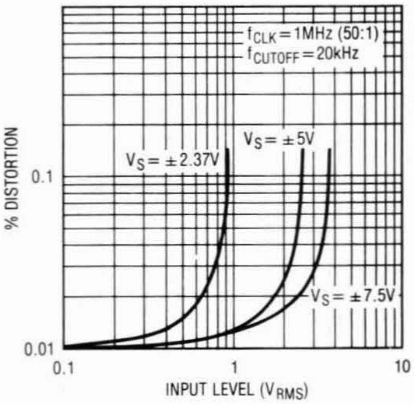
Graph 4. Gain vs Frequency with Compensation



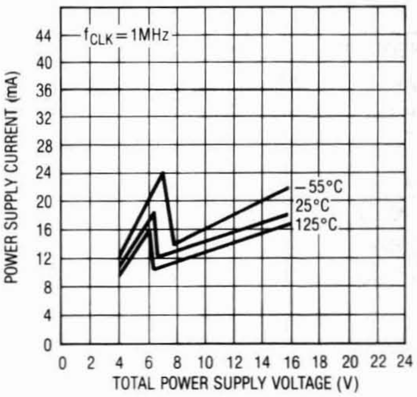
Graph 5. Device to Device Phase Matching



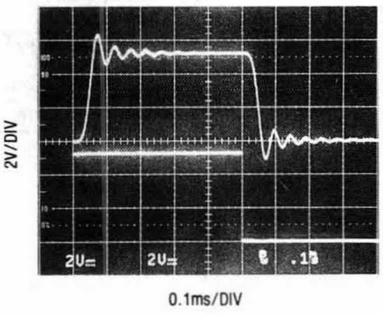
Graph 6. Total Harmonic Distortion



Graph 7. Power Supply Current vs Power Supply Voltage



Graph 8. Transient Response $f_{CLK} = 1MHz$, Ratio = 50:1, $f_C = 20kHz$, $V_S = \pm 7.5V$, 1kHz, Square Wave Input



TYPICAL PERFORMANCE CHARACTERISTICS

Table 1. Wideband Noise (μV_{RMS}). Input Grounded, f_{CLK} = 1MHz.

		V_S = ± 2.37V	V_S = ± 5V	V_S = ± 7.5V
PIN 10 TO	f_{CLK}/f_{CUTOFF}	NOISE (μV_{RMS})	NOISE (μV_{RMS})	NOISE (μV_{RMS})
V^+	50:1	120	135	145
V^-	100:1	100	120	130

Table 2. Gain/Phase, Pin 10 at V^+. Typical Response.
f_{CUTOFF} = 1kHz, V_S = ± 5V, T_A = 25°C f_{CLK} = 50kHz Ratio = 50:1

FREQUENCY	GAIN	PHASE
0.200kHz	– 0.075dB	– 59.990 deg
0.400kHz	– 0.050dB	– 122.400 deg
0.600kHz	0.020dB	169.300 deg
0.800kHz	0.060dB	88.500 deg
1.000kHz	0.090dB	– 26.100 deg
1.200kHz	– 15.640dB	– 175.100 deg
1.400kHz	– 34.700dB	126.500 deg
1.600kHz	– 51.700dB	87.600 deg
1.800kHz	– 68.600dB	38.400 deg
2.000kHz	– 84.110dB	– 47.860 deg

Table 3. Gain/Delay, Pin 10 at V^+. Typical Response.
f_{CUTOFF} = 1kHz, V_S = ± 5V, T_A = 25°C f_{CLK} = 50kHz Ratio = 50:1

FREQUENCY	GAIN	DELAY
0.200kHz	– 0.074dB	0.844ms
0.300kHz	– 0.070dB	0.867ms
0.400kHz	– 0.050dB	0.899ms
0.500kHz	– 0.020dB	0.949ms
0.600kHz	0.020dB	1.021ms
0.700kHz	0.050dB	1.122ms
0.800kHz	0.060dB	1.275ms
0.900kHz	0.120dB	1.592ms
1.000kHz	0.090dB	2.160ms
1.100kHz	– 5.020dB	2.070ms
1.200kHz	– 15.650dB	1.288ms

Table 4. Gain/Phase, Pin 10 at V^-. Typical Response.
f_{-3dB} = 1kHz, V_S = ± 5V, T_A = 25°C f_{CLK} = 100kHz Ratio = 100:1

FREQUENCY	GAIN	PHASE
0.200kHz	– 0.179dB	– 60.090 deg
0.400kHz	– 0.440dB	– 122.000 deg
0.600kHz	– 0.810dB	170.800 deg
0.800kHz	– 1.480dB	91.900 deg
1.000kHz	– 3.500dB	– 16.300 deg
1.200kHz	– 17.720dB	– 140.500 deg
1.400kHz	– 35.700dB	164.800 deg
1.600kHz	– 52.700dB	135.000 deg
1.800kHz	– 71.900dB	114.000 deg
2.000kHz	– 96.160dB	– 49.670 deg

Table 5. Gain/Delay, Pin 10 at V^-. Typical Response.
f_{-3dB} = 1kHz, V_S = ± 5V, T_A = 25°C f_{CLK} = 100kHz Ratio = 100:1

FREQUENCY	GAIN	DELAY
0.200kHz	– 0.174dB	0.842ms
0.300kHz	– 0.300dB	0.861ms
0.400kHz	– 0.440dB	0.888ms
0.500kHz	– 0.610dB	0.933ms
0.600kHz	– 0.810dB	0.999ms
0.700kHz	– 1.090dB	1.095ms
0.800kHz	– 1.480dB	1.242ms
0.900kHz	– 2.080dB	1.503ms
1.000kHz	– 3.500dB	1.832ms
1.100kHz	– 8.720dB	1.724ms
1.200kHz	– 17.720dB	1.183ms

Table 6. Gain/Phase, Pin 10 at GND.
V_S = ± 5V, T_A = 25°C

FREQUENCY	GAIN	PHASE
0.200kHz	– 0.383dB	– 47.140 deg
0.400kHz	– 1.000dB	– 92.000 deg
0.600kHz	– 1.300dB	– 134.300 deg
0.800kHz	– 0.280dB	– 178.800 deg
1.000kHz	2.670dB	109.200 deg
1.200kHz	– 3.500dB	6.000 deg
1.400kHz	– 12.510dB	– 47.400 deg
1.600kHz	– 20.000dB	– 88.800 deg
1.800kHz	– 27.300dB	– 127.800 deg
2.000kHz	– 35.000dB	– 164.200 deg

TYPICAL PERFORMANCE CHARACTERISTICS

Table 7. Gain/Phase for Figure 6.
Typical Response, Pin 10 at V$^+$, f_{CUTOFF} = 40kHz
V_S = ± 7.5V, f_{CLK} = 2MHz, Ratio = 50:1

FREQUENCY	GAIN	PHASE
10.000kHz	– 0.094dB	– 75.900 deg
12.000kHz	– 0.100dB	– 91.400 deg
14.000kHz	– 0.090dB	– 107.200 deg
16.000kHz	– 0.080dB	– 123.300 deg
18.000kHz	– 0.060dB	– 139.600 deg
20.000kHz	– 0.040dB	– 156.500 deg
22.000kHz	– 0.020dB	– 173.800 deg
24.000kHz	0.000dB	168.200 deg
26.000kHz	0.020dB	149.400 deg
28.000kHz	0.030dB	130.000 deg
30.000kHz	0.020dB	109.400 deg
32.000kHz	0.010dB	87.700 deg
34.000kHz	– 0.020dB	64.600 deg
36.000kHz	– 0.030dB	39.500 deg
38.000kHz	– 0.010dB	11.400 deg
40.000kHz	– 0.070dB	– 22.000 deg
42.000kHz	– 0.920dB	– 64.100 deg
44.000kHz	– 4.000dB	– 110.100 deg
46.000kHz	– 8.970dB	– 147.000 deg
48.000kHz	– 14.320dB	– 173.500 deg
50.000kHz	– 19.460dB	166.800 deg

Table 8. Gain/Phase for Figure 7.
Typical Response, Pin 10 at V$^+$, f_{CUTOFF} = 100kHz
V_S = ± 7.5V, T_A = 25°C f_{CLK} = 5MHz Ratio = 50:1

FREQUENCY	GAIN	PHASE
10.000kHz	– 0.096dB	– 32.390 deg
20.000kHz	– 0.100dB	– 64.900 deg
30.000kHz	– 0.080dB	– 98.100 deg
40.000kHz	– 0.040dB	– 132.300 deg
50.000kHz	0.020dB	– 168.200 deg
60.000kHz	0.070dB	153.600 deg
70.000kHz	0.040dB	112.100 deg
80.000kHz	– 0.120dB	66.400 deg
90.000kHz	– 0.460dB	14.600 deg
100.000kHz	– 1.310dB	– 49.300 deg
110.000kHz	– 5.640dB	– 129.000 deg
120.000kHz	– 14.530dB	167.800 deg
130.000kHz	– 23.800dB	126.700 deg
140.000kHz	– 32.600dB	96.200 deg
150.000kHz	– 41.000dB	71.300 deg
160.000kHz	– 49.200dB	49.200 deg
170.000kHz	– 57.500dB	29.000 deg
180.000kHz	– 66.500dB	9.800 deg
190.000kHz	– 77.770dB	– 2.320 deg
200.000kHz	– 92.050dB	76.740 deg

Table 9. Gain/Phase for Figure 7.
Typical Response, Pin 10 at V$^+$, f_{CUTOFF} = 100kHz
V_S = ± 7.5V, T_A = 125°C f_{CLK} = 5MHz Ratio = 50:1

FREQUENCY	GAIN	PHASE
10.000kHz	– 0.071dB	– 33.800 deg
20.000kHz	– 0.040dB	– 67.800 deg
30.000kHz	0.050dB	– 102.500 deg
40.000kHz	0.190dB	– 138.300 deg
50.000kHz	0.410dB	– 176.100 deg
60.000kHz	0.670dB	143.100 deg
70.000kHz	0.920dB	98.400 deg
80.000kHz	1.150dB	48.200 deg
90.000kHz	1.530dB	– 10.900 deg
100.000kHz	1.110dB	– 96.500 deg
110.000kHz	– 7.420dB	172.100 deg
120.000kHz	– 18.240dB	119.400 deg
130.000kHz	– 28.000dB	83.300 deg
140.000kHz	– 37.000dB	54.000 deg
150.000kHz	– 45.700dB	– 27.600 deg
160.000kHz	– 54.300dB	2.100 deg
170.000kHz	– 63.300dB	– 24.900 deg
180.000kHz	– 73.610dB	– 60.210 deg
190.000kHz	– 85.300dB	– 138.990 deg
200.000kHz	– 83.390dB	129.580 deg

PIN DESCRIPTION

Power Supply Pins (4, 12)

The V^+ (pin 4) and V^- (pin 12) should be bypassed with a 0.1μF capacitor to an adequate analog ground. Low noise, non-switching power supplies are recommended. **To avoid latch up when the power supplies exhibit high turn-on transients, a 1N5817 Schottky diode should be added from the V^+ and V^- pins to ground, Figures 1 and 2.**

Clock Pin (11)

For ±5V supplies the logic threshold level is 1.4V. For ±8V and 0V to 5V supplies the logic threshold levels are 2.4V and 3V respectively. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50% although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for ±5V supplies is 4MHz. For ±7V supplies and above, the maximum clock frequency is 5MHz. Do not allow the clock levels to exceed the power supplies. For single supply operation and for $V_S \geq 6V$, T^2L clock signals can be accommodated through level shifting, Figure 3.

Analog Ground Pins (3, 5)

For dual supply operation these pins should be connected to a ground plane. For single supply operation both pins should be tied to one half supply, Figure 2.

Connection Pins (7, 14)

A very short connection between pins 14 and 7 is recommended. This connection should be preferably done under the IC package. In a breadboard, use a one inch, or less, shielded coaxial cable; the shield should be grounded. In a PC board, use a one inch trace or less; surround the trace by a ground plane.

NC Pin (8)

Pin 8 is not internally connected, it should be preferably grounded.

Input, Output Pins (2, 9)

The input pin 2 is connected to a 12kΩ resistor tied to the inverting input of an op amp. Pin 2 is protected against static discharge. The device's output, pin 9, is the output of an op amp which can typically source/sink 3/1mA. Although the internal op amps are unity gain stable, driving long coax cables is not recommended.

When testing the device for noise and distortion, the output, pin 9, should be buffered, Figure 4. **The op amp power supply wire (or trace) should be connected directly to the power source.** To eliminate any output clock feedthrough, pin 9 should be buffered with a simple R, C lowpass filter, Figure 5. The cutoff frequency of the output filter should be $f_{CLK}/3$.

50/100 Ratio Pin (10)

For an f_{CLK}/f_C ratio of 50:1, pin 10 should be tied to V^+. For an f_{CLK}/f_{-3dB} ratio of 100:1, pin 10 should be tied to V^-. When pin 10 is at mid-supplies (i.e. ground), the filter response is neither Cauer nor transitional. Table 6 illustrates this response. Bypassing pin 10 with a 0.1μF capacitor reduces the, already small, clock feedthrough.

Compensation Pins (6, 7 and 1, 13)

To obtain a Cauer response with minimum passband ripple and cutoff frequencies above 20kHz, compensating components are required. Figure 6 uses ±7.5V power supplies and compensation components to achieve up to 40kHz **sweepable** cutoff frequencies and ±0.1dB passband ripple. Table 7 lists the typical amplitude response of Figure 6. Figure 7 illustrates the compensation scheme required to obtain a 100kHz cutoff frequency; Graph 4 and Tables 8 and 9 list the typical response of Figure 7 for 25°C and 125°C ambient temperature. As shown the ripple increases at high temperatures but still a ±0.25dB figure can be obtained for ambient temperatures below 70°C.

PIN DESCRIPTION

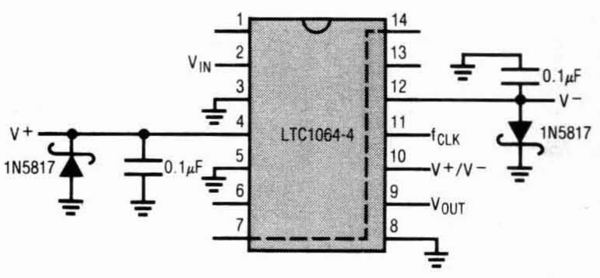

LTC1064-4
V+
1N5817
0.1μF
VIN
fCLK
V+/V−
VOUT
V−
1N5817
0.1μF

Figure 1. Using Schottky Diodes to Protect the IC from Power Supply Spikes.

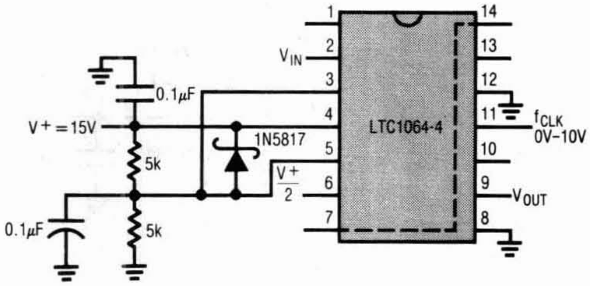

LTC1064-4
V+ = 15V
0.1μF
5k
5k
0.1μF
1N5817
V+/2
VIN
fCLK
0V–10V
VOUT

Figure 2. Single Supply Operation. If Fast Power Up or Down Transients are Expected, Use a 1N5817 Schottky Diode Between Pins 4 and 5.

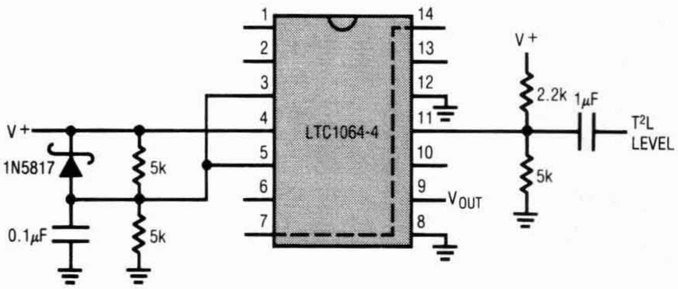

LTC1064-4
V+
1N5817
5k
5k
0.1μF
V+
2.2k
1μF
5k
T²L LEVEL
VOUT

Figure 3. Level Shifting the Input T²L Clock for Single Supply Operation ≥ 6V.

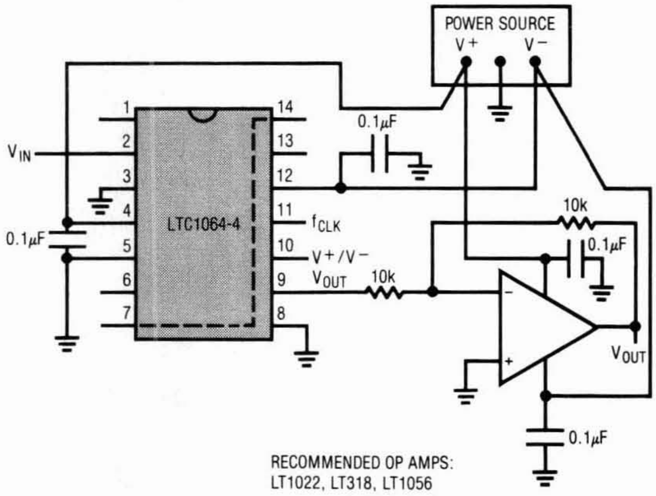

POWER SOURCE
V+
V−
VIN
0.1μF
LTC1064-4
0.1μF
fCLK
V+/V−
VOUT
10k
10k
0.1μF
VOUT
0.1μF
RECOMMENDED OP AMPS:
LT1022, LT318, LT1056

Figure 4. Buffering the Filter Output. The Buffer Op Amp Should Not Share the LTC1064-4 Power Lines.

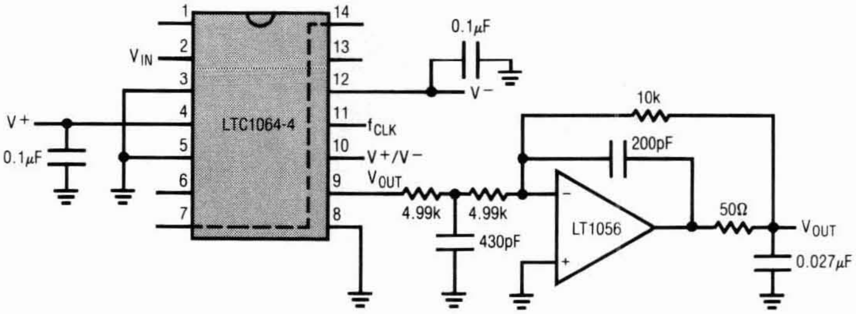

LTC1064-4
VIN
V+
0.1μF
0.1μF
V−
fCLK
V+/V−
VOUT
10k
200pF
4.99k
4.99k
430pF
LT1056
50Ω
VOUT
0.027μF

Figure 5. Adding an Output Buffer-Filter to Eliminate Any Clock Feedthrough. Passband Error of Output Buffer is ±0.1dB to 50kHz, −3dB at 94kHz.

PIN DESCRIPTION

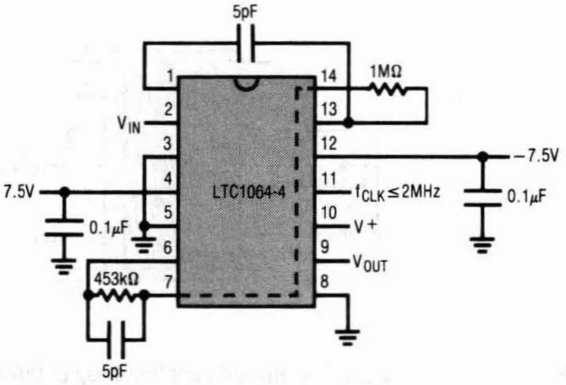

5pF
1MΩ
V_{IN}
7.5V
0.1µF
453kΩ
5pF
LTC1064-4
−7.5V
$f_{CLK} \le 2MHz$
0.1µF
V+
V_{OUT}
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 6. Compensating LTC1064-4 for Passband Ripple of ±0.1dB and f_{CUTOFF} Sweeps to 40kHz.

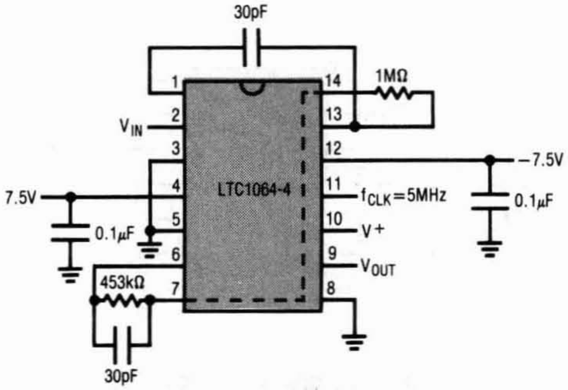

30pF
1MΩ
V_{IN}
7.5V
0.1µF
453kΩ
30pF
LTC1064-4
−7.5V
$f_{CLK} = 5MHz$
0.1µF
V+
V_{OUT}
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 7. Compensating LTC1064-4 for $f_{CUTOFF} = 100kHz$, Gain at $f_{CUTOFF} \approx -1.3dB$, Table 8.

LTC1164

Low Power, Low Noise, Quad Universal Filter Building Block

FEATURES

- Low Power
- 4 Filters in a 0.3″ Wide Package
- 1/2 the Noise of the LTC1059, 60, 61 Devices
- Wide Output Swing
- Clock to Center Frequency Ratios of 50:1 and 100:1
- Operates from ± 2.37V to ± 8V Power Supplies
- Customized Version with Internal Resistors Available
- Ratio of 50:1 and 100:1 Simultaneously Available

APPLICATIONS

- Antialiasing Filters
- Telecom Filters
- Spectral Analysis
- Loop Filters
- For Fixed Lowpass Filter Requirements use the LTC1164-XX Series

DESCRIPTION

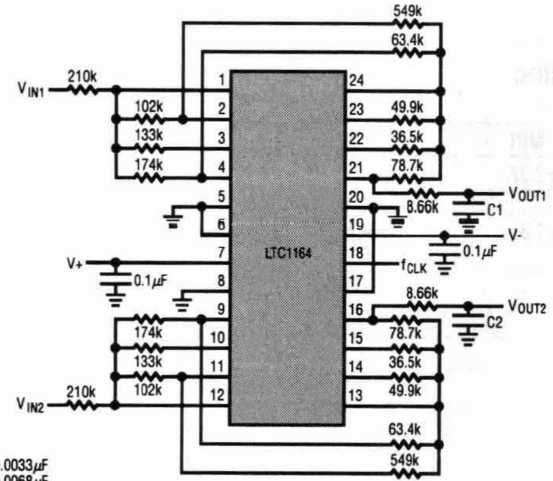
The LTC1164 consists of four low power, low noise 2nd order switched capacitor filter building blocks. Each building block typically consumes 850μA supply current. Low power is achieved without sacrificing noise and distortion. Each building block, together with 3 to 5 resistors, can provide 2nd order functions like lowpass, highpass, bandpass, and notch. The center frequency of each 2nd order section can be tuned with an external clock, or a clock and resistor ratio. For Q < 5, the center frequency range is from 0.1Hz to 20kHz. Up to 8th order filters can be realized by cascading all four 2nd order sections. Any classical filter realization (such as Butterworth, Cauer, Bessel, and Chebyshev) can be formed.

A customized monolithic version of the LTC1164 including internal thin film resistors can be obtained. Consult LTC Marketing for details.

The LTC1164 is manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process.

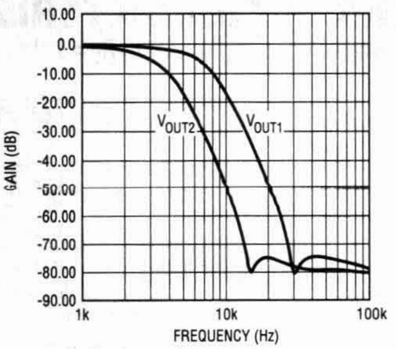
TYPICAL APPLICATION

Dual 5th Order Linear Phase Filter with Stopband Notch



C1 = 0.0033μF
C2 = 0.0068μF
f_{CLK} = 500kHz
WIDEBAND NOISE = 50μV_{RMS}
TOTAL SUPPLY CURRENT = 3mA
ALL RESISTORS ARE 1% METAL FILM

Dual 5th Order Linear Phase Filter with Stopband Notch, f_{CLK} = 500kHz

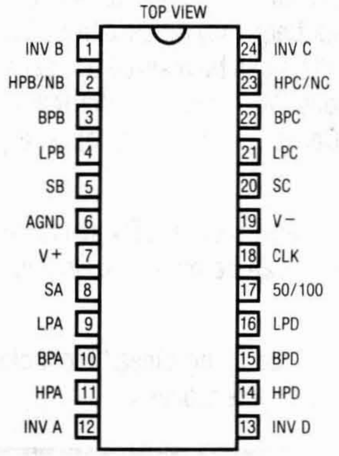
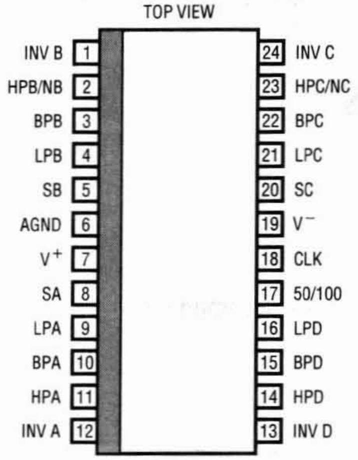


SUPPLY VOLTAGE	V_{IN}	TOTAL HARMONIC DISTORTION	SIGNAL/NOISE
± 2.5V	1V_{RMS}	0.015% (−76dB)	86dB
± 5.0V	2V_{RMS}	0.025% (−72dB)	92dB
± 7.5V	4V_{RMS}	0.04% (−68dB)	98dB

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 500mW
Operating Temperature Range
  LTC1164AM, LTC1164M .... – 55°C to 125°C
  LTC1164AC, LTC1164C .... – 40°C to 85°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
 J PACKAGE 24-LEAD CERAMIC DIP N PACKAGE 24-LEAD PLASTIC DIP	LTC1164AMJ LTC1164MJ LTC1164ACJ LTC1164CJ LTC1164ACN LTC1164CN	 SO PACKAGE 24-LEAD PLASTIC SOIC	LTC1164CS LTC1164ACS

TOP VIEW
INV B 1
HPB/NB 2
BPB 3
LPB 4
SB 5
AGND 6
V+ 7
SA 8
LPA 9
BPA 10
HPA 11
INV A 12
24 INV C
23 HPC/NC
22 BPC
21 LPC
20 SC
19 V–
18 CLK
17 50/100
16 LPD
15 BPD
14 HPD
13 INV D

ELECTRICAL CHARACTERISTICS

(Internal Op Amps) $V_S = \pm 5V$, $T_A = 25°C$, $R_L = 5k\Omega$ unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range			± 2.37		± 8	V
Voltage Swings	$V_S = \pm 2.5V$			± 1.6		V
	$V_S = \pm 5.0V$	●	± 3.8	± 4.2		V
	$V_S = \pm 7.5V$			± 6.1		V
Output Short Circuit Current (Source/Sink)	$V_S = \pm 5.0V$			1		mA
DC Open Loop Gain	$V_S = \pm 5.0V$			80		dB
GBW Product	$V_S = \pm 5.0V$			2		MHz
Slew Rate	$V_S = \pm 5.0V$			1.6		V/µs

ELECTRICAL CHARACTERISTICS

(Complete Filter) $V_S = \pm 5V$, $T_A = 25°C$, TTL Clock Input Level, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range				0.1-20k		Hz
Input Frequency Range (Note 1)	50:1 100:1				$<f_{CLK}$ $<f_{CLK}/2$	Hz Hz
Clock to Center Frequency Ratio, f_{CLK}/f_o	Sides A, B, C: Mode 1, R1 = R3 = 50kΩ, R2 = 5kΩ, Side D: Mode 3, R1 = R3 = 50kΩ, R2 = R4 = 5kΩ $f_o = 5kHz$, Q = 10					
LTC1164A	50:1, $f_{CLK} = 250kHz$	●			50 ± 0.5	%
LTC1164	50:1, $f_{CLK} = 250kHz$	●			50 ± 0.9	%
LTC1164A	100:1, $f_{CLK} = 500kHz$	●			100 ± 0.5	%
LTC1164	100:1, $f_{CLK} = 500kHz$	●			100 ± 0.9	%
Clock to Center Frequency Ratio, Side to Side Matching	Sides A, B, C, Mode 1, $f_o = 5kHz$, Q = 10 Side D Mode 3, $f_o = 5kHz$, Q = 10					
LTC1164A	50:1, $f_{CLK} = 250kHz$	●			0.5	%
LTC1164	50:1, $f_{CLK} = 250kHz$	●			1.0	%
Q Accuracy	Sides A, B, C, Mode 1, $f_o = 5kHz$, Q = 10 50:1, $f_{CLK} = 250kHz$	●		± 2	± 5	%
	100:1, $f_{CLK} = 500kHz$	●		± 2	± 5	%
	Side D Mode 3, $f_o = 5kHz$, Q = 10 50:1, $f_{CLK} = 250kHz$	●		± 3	± 6	%
	100:1, $f_{CLK} = 500kHz$	●		± 6	± 12	%
f_o Temperature Coefficient	$f_{CLK} \leq 500kHz$			± 1		ppm/°C
Q Temperature Coefficient	$f_{CLK} \leq 250kHz$			± 5		ppm/°C
Maximum Clock Frequency	Mode 1, Q < 2.5 $V_S \geq \pm 7.0V$, 50:1 or 100:1			1.5		MHz
	Mode 3, Q < 5.0 $V_S \geq \pm 5.0V$, 50:1 or 100:1			1.0		MHz
	Mode 3, Q < 5.0 $V_S = \pm 2.5V$, 50:1 or 100:1			500		kHz
f_{CLK} Feedthrough	$f_{CLK} \leq 500kHz$, $V_S = \pm 5V$			200		μV_{RMS}
DC Offset Voltages (See Figure 1 and Table 1)	V_{OS1} V_{OS2} V_{OS3}	● ● ●		2 3 3	20 45 45	mV mV mV
Power Supply Current	$V_S = \pm 2.5V$			4.0		mA
	$V_S = \pm 5.0V$, Temp ≥ + 25°C $V_S = \pm 5.0V$	 ●		3.6 5.6	5.0 8	mA mA
	$V_S = \pm 7.5V$, Temp ≥ + 25°C $V_S = \pm 7.5V$	 ●		6.0 9.0	8 11.0	mA mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Guaranteed by design. Not tested.

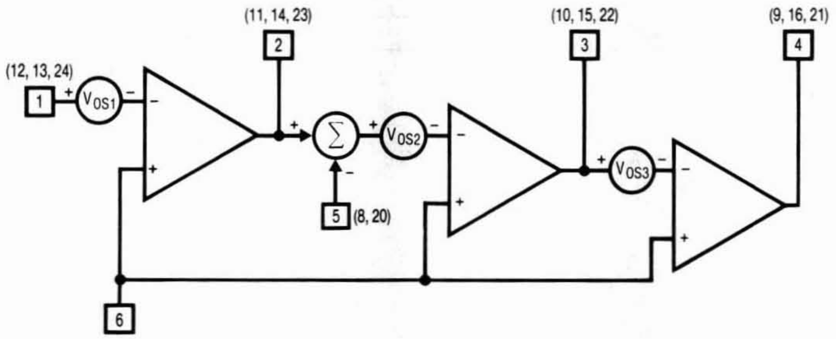
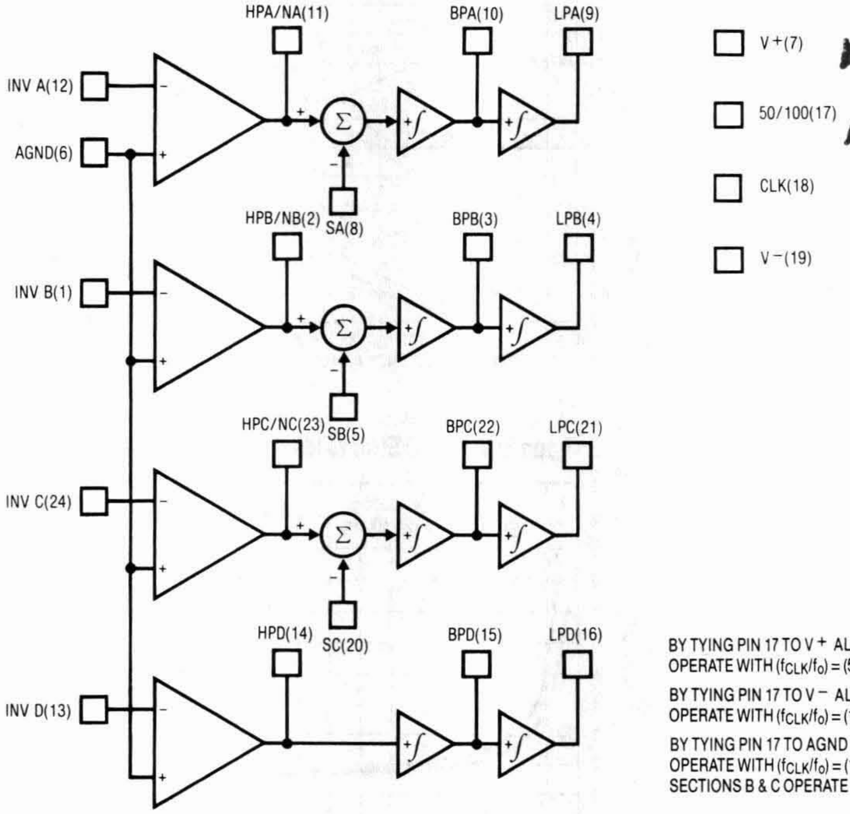

(11, 14, 23)
2
(10, 15, 22)
3
(9, 16, 21)
4
(12, 13, 24)
1
+
V_OS1
–
–
+
+
Σ
–
+
V_OS2
–
–
+
5
(8, 20)
+
V_OS3
–
–
+
6

Figure 1. Equivalent Input Offsets of $^1/_4$ LTC1164 Filter Building Block

Table 1. Output DC Offsets One 2nd Order Section

MODE	V_{OSN} PIN 2, 11, 14, 23	V_{OSBP} PIN 3, 10, 15, 22	V_{OSLP} PIN 4, 9, 16, 21
1	$V_{OS1}[(1/Q) + 1 + \lVert H_{OLP} \rVert] - V_{OS3}/Q$	V_{OS3}	$V_{OSN} - V_{OS2}$
1b	$V_{OS1}[(1/Q) + 1 + R2/R1] - V_{OS3}/Q$	V_{OS3}	$\sim(V_{OSN} - V_{OS2})(1 + R5/R6)$
2	$[V_{OS1}(1 + R2/R1 + R2/R3 + R2/R4) - V_{OS3}(R2/R3)] \times [R4/(R2 + R4)] + V_{OS2}[R2/(R2 + R4)]$	V_{OS3}	$V_{OSN} - V_{OS2}$
3	V_{OS2}	V_{OS3}	$V_{OS1}\left[1+\frac{R4}{R1}+\frac{R4}{R2}+\frac{R4}{R3}\right] - V_{OS2}\left(\frac{R4}{R2}\right) - V_{OS3}\left(\frac{R4}{R3}\right)$

BLOCK DIAGRAM


HPA/NA(11)
BPA(10)
LPA(9)
INV A(12)
AGND(6)
SA(8)
HPB/NB(2)
BPB(3)
LPB(4)
INV B(1)
SB(5)
HPC/NC(23)
BPC(22)
LPC(21)
INV C(24)
SC(20)
HPD(14)
BPD(15)
LPD(16)
INV D(13)
Σ
+
−
∫
V +(7)
50/100(17)
CLK(18)
V −(19)

+V = /50
−V = /100
OR

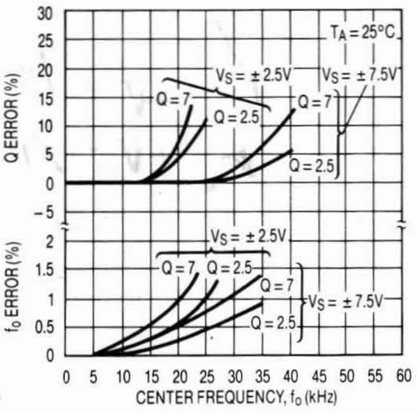
BY TYING PIN 17 TO V + ALL SECTIONS OPERATE WITH (f_{CLK}/f_o) = (50:1)

BY TYING PIN 17 TO V − ALL SECTIONS OPERATE WITH (f_{CLK}/f_o) = (100:1)

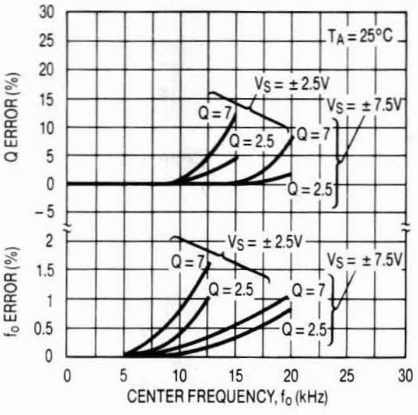
BY TYING PIN 17 TO AGND SECTIONS A & D OPERATE WITH (f_{CLK}/f_o) = (100:1) AND SECTIONS B & C OPERATE AT (50:1)

TYPICAL PERFORMANCE CHARACTERISTICS

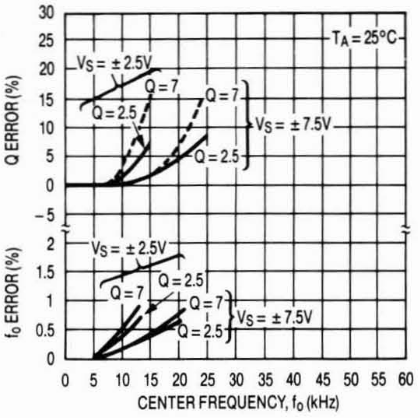
Graph 1. Mode 1, $(f_{CLK}/f_o) = 50{:}1$



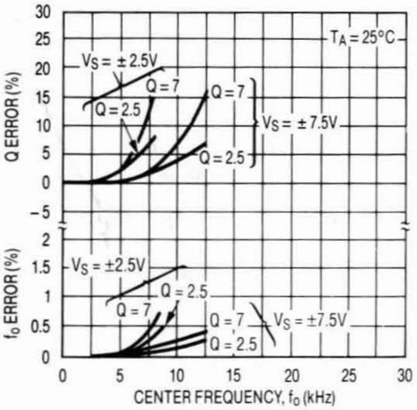
Graph 2. Mode 1, $(f_{CLK}/f_o) = 100{:}1$



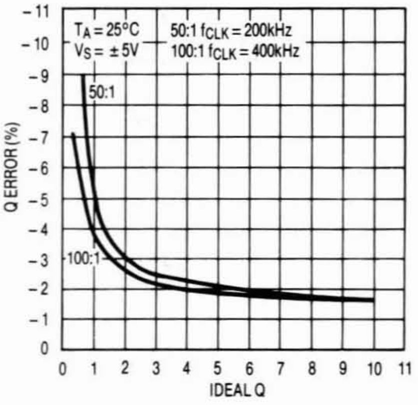
Graph 3. Mode 3, $(f_{CLK}/f_o) = 50{:}1$



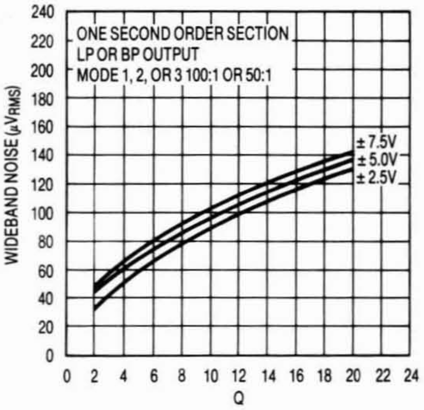
Graph 4. Mode 3, $(f_{CLK}/f_o) = 100{:}1$



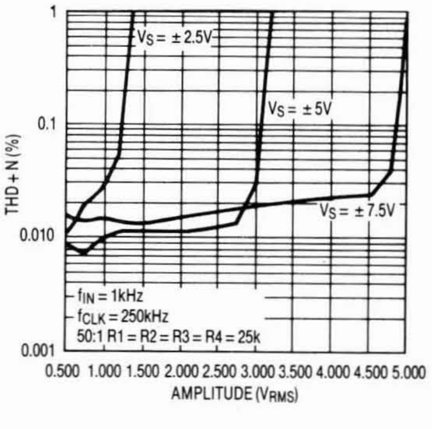
Graph 5. Mode 3 Q Error vs Ideal Q



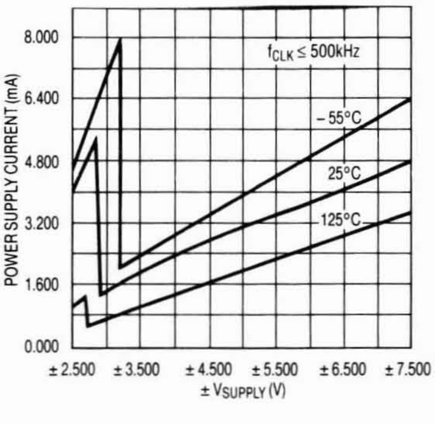
Graph 6. Wideband Noise vs Q



Graph 7. Total Harmonic Distortion vs Output Amplitude



Graph 8. Power Supply Current vs Voltage



PIN DESCRIPTION

Power Supplies (Pins 7, 19)

They should be bypassed with 0.1μF ceramic disc. Low noise, non-switching, power supplies are recommended. The device operates with a single 5V supply and with dual supplies. The absolute maximum operating power supply voltage is ±8.25V. Supply reversal is not allowed and can cause latch up. When using dual supplies, loads between the positive and negative supply (even light loads) can cause momentary supply reversal during power-up. A clamp diode from each supply to ground will prevent reversal and latch problems.

Clock (Pin 18)

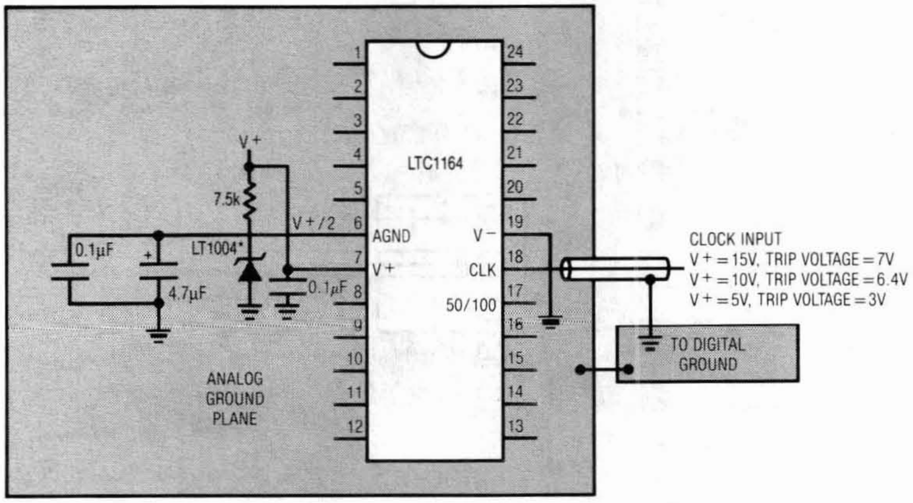
For ±5V supplies the logic threshold level is 1.8V. For ±8V and 0 to 5V supplies the logic threshold level is 2.8V. The logic threshold levels vary ±100mV over the full military temperature range. The recommended duty cycle of the input clock is 50%, although for clock frequencies below 500kHz the clock "on" time can be as low as 200ns. The maximum clock frequency for single 5V supply and Q values <5 is 500kHz and for ±5V supplies and above is 1MHz. The clock input can be applied before power is turned on as long as there is no chance the clock signal will go below the V^- supply.

AGND (Pin 6)

When the LTC1164 operates with dual supplies, Pin 6 should be tied to system ground. When the LTC1164 operates with a single positive supply, the analog ground pin should be tied to 1/2 supply and it should be bypassed with a 4.7μF solid tantalum in parallel with a 0.1μF ceramic disc, Figure 2. The positive input of all the internal op amps, as well as the common reference of all the internal switches, are internally tied to the analog ground pin. Because of this, a very "clean" ground is recommended.

50/100 (Pin 17)

By tying Pin 17 to V^+, all filter sections operate with a clock to center frequency ratio internally set at 50:1. When Pin 17 is at mid-supplies, sections B and C operate with $(f_{CLK}/f_o) = 50:1$ and sections A and D operate at (100:1). When Pin 17 is shorted to the negative supply pin, all filter sections operate with $(f_{CLK}/f_o) = 100:1$.



NOTE: PIN 5, 8, 20, IF NOT USED, SHOULD BE CONNECTED TO PIN 6.
*LT1004 CAN BE REPLACED WITH A 7.5k RESISTOR FOR V+ >6.5V.

Figure 2. Single Supply Operation

APPLICATIONS INFORMATION

ANALOG CONSIDERATIONS

1. Grounding and Bypassing

The LTC1164 should be used with separated analog and digital ground planes and single point grounding techniques.

Pin 6 (AGND) should be tied directly to the analog ground plane.

Pin 7 (V^+) should be bypassed to the ground plane with a 0.1μF ceramic disk with leads as short as possible. Pin 19 (V^-) should be bypassed with a 0.1μF ceramic disk. For single supply applications, V^- can be tied to the analog ground plane.

For good noise performance, V^+ and V^- must be free of noise and ripple.

All analog inputs should be referenced directly to the single point ground. The clock inputs should be shielded from and/or routed away from the analog circuitry and a separate digital ground plane used.

Figure 3 shows an example of an ideal ground plane design for a two sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this as possible. Proto boards are not recommended.

2. Buffering the Filter Output

When driving coaxial cables and 1× scope probes, the filter output should be buffered. This is important especially when high Qs are used to design a specific filter. *Inadequate buffering may cause errors in noise, distortion, Q, and gain measurements.* When 10× probes are used, buffering is usually not required. A buffer is recommended especially when THD tests are performed. As shown in Figure 4, the buffer should be adequately bypassed to minimize clock feedthrough.

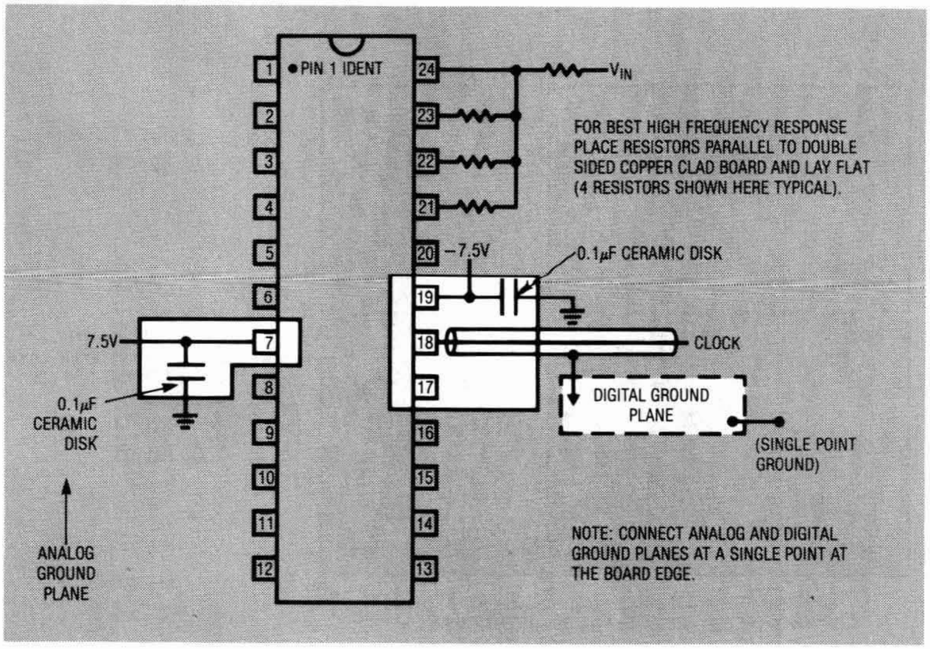

● PIN 1 IDENT
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
V_{IN}
FOR BEST HIGH FREQUENCY RESPONSE PLACE RESISTORS PARALLEL TO DOUBLE SIDED COPPER CLAD BOARD AND LAY FLAT (4 RESISTORS SHOWN HERE TYPICAL).
–7.5V
0.1μF CERAMIC DISK
CLOCK
DIGITAL GROUND PLANE
(SINGLE POINT GROUND)
NOTE: CONNECT ANALOG AND DIGITAL GROUND PLANES AT A SINGLE POINT AT THE BOARD EDGE.
7.5V
0.1μF CERAMIC DISK
ANALOG GROUND PLANE

Figure 3. Example Ground Plane Breadboard Technique for LTC1164

APPLICATIONS INFORMATION

3. Offset Nulling

Lowpass filters may have too much DC offset for some users. A servo circuit may be used to actively null the offsets of the LTC1164 or any LTC switched capacitor filter. The circuit shown in Figure 5 will null offsets to better than 300µV. This circuit takes seconds to settle because of the integrator pole frequency.

4. Noise

All the noise performance mentioned excludes the clock feedthrough. Noise measurements will degrade if, the already described grounding, bypassing, and buffering techniques are not practiced. Graph 6 is a very good representation of the noise performance of this device.

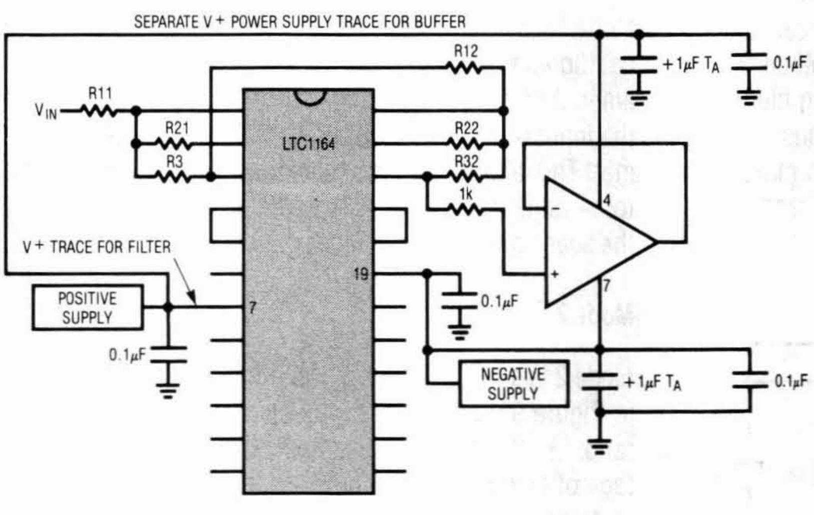

SEPARATE V + POWER SUPPLY TRACE FOR BUFFER
R12
+1µF TA
0.1µF
VIN
R11
R21
R3
LTC1164
R22
R32
1k
4
V + TRACE FOR FILTER
19
0.1µF
POSITIVE SUPPLY
7
7
0.1µF
NEGATIVE SUPPLY
+1µF TA
0.1µF

Figure 4. Buffering the Output of a 4th Order Bandpass Realization

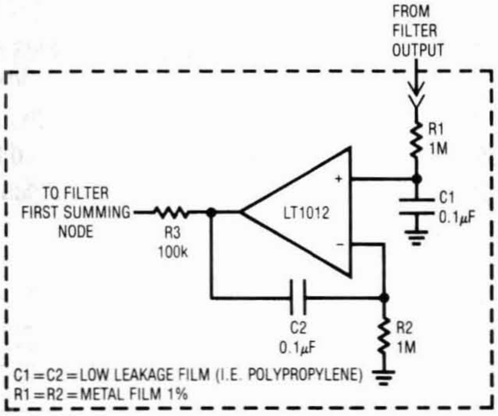

FROM FILTER OUTPUT
R1
1M
C1
0.1µF
TO FILTER FIRST SUMMING NODE
R3
100k
LT1012
C2
0.1µF
R2
1M
C1 = C2 = LOW LEAKAGE FILM (I.E. POLYPROPYLENE)
R1 = R2 = METAL FILM 1%

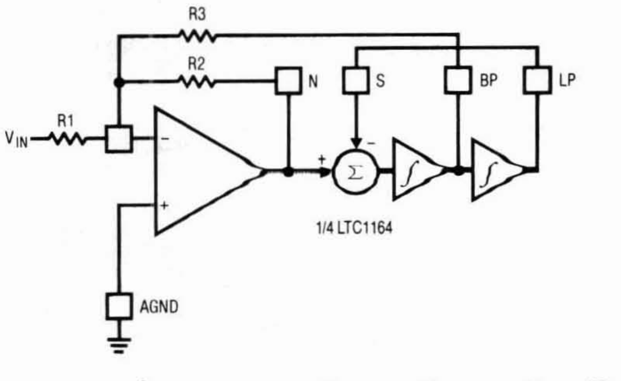
Figure 5. Servo Amplifier

MODES OF OPERATION

PRIMARY MODES

Mode 1

In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at 50:1 or 100:1. Figure 6 illustrates Mode 1 providing 2nd order notch, lowpass, and bandpass outputs. Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency with unity gain. Mode 1 is faster than Mode 3. Note that Mode 1 can only be implemented with 3 of the 4 LTC1164 sections because section D has no


R3
R2
N
S
BP
LP
R1
VIN
–
+
+
–
Σ
∫
∫
1/4 LTC1164
AGND

$f_0 = \frac{f_{CLK}}{100(50)}$; $f_n = f_0$; $H_{OLP} = -\frac{R2}{R1}$; $H_{OBP} = -\frac{R3}{R1}$; $H_{ON1} = -\frac{R2}{R1}$ $Q = \frac{R3}{R2}$

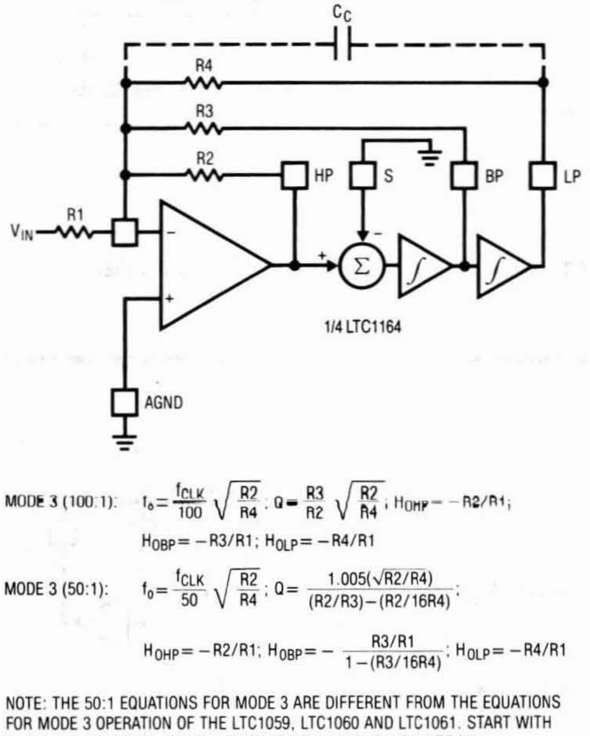
Figure 6. Mode 1: 2nd Order Filter Providing Notch, Bandpass, Lowpass

MODES OF OPERATION

externally available summing node. Section D, however, can be internally connected in Mode 1 upon special request.

Mode 3

Mode 3 is the second of the primary modes. In Mode 3, the ratio of the external clock frequency to the center frequency of each 2nd order section can be adjusted above or below 50:1 or 100:1. Side D of the LTC1164 can only be connected in Mode 3. Figure 7 illustrates Mode 3, the classical state variable configuration, providing highpass, bandpass, and lowpass 2nd order filter functions. Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass, highpass and notch filters.



MODE 3 (100:1): $f_0 = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}}$; $Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}}$; $H_{OHP} = -R2/R1$;

$H_{OBP} = -R3/R1$; $H_{OLP} = -R4/R1$

MODE 3 (50:1): $f_0 = \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}}$; $Q = \frac{1.005(\sqrt{R2/R4})}{(R2/R3)-(R2/16R4)}$;

$H_{OHP} = -R2/R1$; $H_{OBP} = -\frac{R3/R1}{1-(R3/16R4)}$; $H_{OLP} = -R4/R1$

NOTE: THE 50:1 EQUATIONS FOR MODE 3 ARE DIFFERENT FROM THE EQUATIONS FOR MODE 3 OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_0, CALCULATE R2/R4, SET R4; FROM THE Q VALUE, CALCULATE R3:

$R3 = \frac{R2}{\frac{1.005}{Q}\sqrt{\frac{R2}{R4}} + \frac{R2}{16R4}}$; THEN CALCULATE R1 TO SET THE DESIRED GAIN.

Figure 7. Mode 3: 2nd Order Filter Providing Highpass, Bandpass, Lowpass

When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case. This was done to provide speed without penalizing the noise performance.

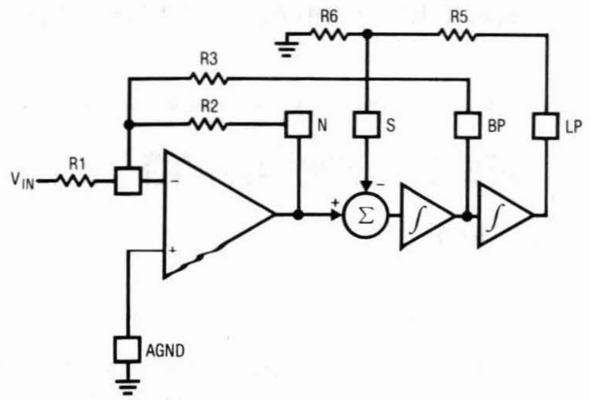
SECONDARY MODES

Mode 1b

Mode 1b is derived from Mode 1. In Mode 1b, Figure 8, two additional resistors R5 and R6, are added to alternate the amount of voltage fed back from the low pass output into the input of the SA (or SB or SC) switched capacitor summer. This allows the filter clock to center frequency ratio to be adjusted beyond 50:1 or 100:1. Mode 1b maintains the speed advantages of Mode 1.

Mode 2

Mode 2 is a combination of Mode 1 and Mode 3, as shown in Figure 9. With Mode 2, the clock to center frequency ratio, f_{CLK}/f_O, is always less than 50:1 or 100:1. The advantage of Mode 2 is that it provides less sensitivity to resistor tolerances than does Mode 3. As in Mode 1, Mode 2 has



$f_0 = \frac{f_{CLK}}{100(50)}\sqrt{\frac{R6}{R5+R6}}$; $f_n = f_0$; $Q = \frac{R3}{R2}\sqrt{\frac{R6}{R5+R6}}$;

$H_{ON1}(f \to 0) = H_{ON2}\left(f \to \frac{f_{CLK}}{2}\right) = -\frac{R2}{R1}$; $H_{OLP} = \frac{-R2/R1}{R6/(R5+R6)}$;

$H_{OBP} = -\frac{R3}{R1}$; $(R5//R6) < 5k\Omega$

Figure 8. Mode 1b: 2nd Order Filter Providing Notch, Bandpass, Lowpass

MODES OF OPERATION

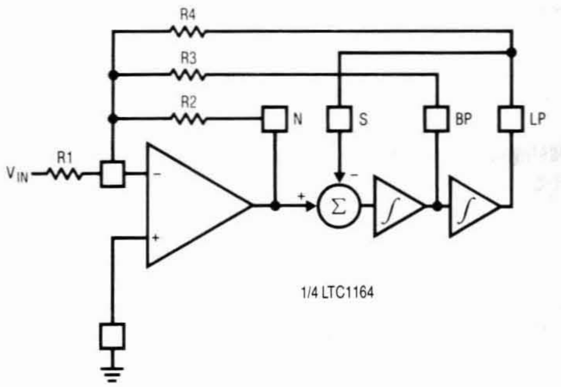
a notch output which depends on the clock frequency, and the notch frequency is therefore less than the center frequency, f_0.

When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case.

Mode 3A

This is an extension of Mode 3 where the highpass and lowpass output are summed through two external resistors R_h and R_l to create a notch. This is shown in Figure 10. Mode 3A is more versatile than Mode 2 because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 10 is not always required. When cascading the sections of the LTC1164, the highpass and lowpass outputs can be summed directly into the inverting input of the next section. The topology of Mode 3A is useful for elliptic highpass and notch filters with clock to cutoff frequency ratios higher than 100:1. This is often required to extend the allowed input signal frequency range and to avoid premature aliasing.

When the internal clock to center frequency ratio is set at 50:1, the design equations for Q and bandpass gain are different from the 100:1 case.



MODE 2 (100:1): $f_0 = \frac{f_{CLK}}{100}\sqrt{1+\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{50}$; $Q = \frac{R3}{R2}\sqrt{1+\frac{R2}{R4}}$; $H_{OLP} = \frac{-R2/R1}{1+(R2/R4)}$

$H_{OBP} = -R3/R1$; $H_{ON1}(f\to 0) = \frac{-R2/R1}{1+(R2/R4)}$; $H_{ON2}\left(f\to \frac{f_{CLK}}{2}\right) = -R2/R1$

MODE 2 (50:1): $f_0 = \frac{f_{CLK}}{50}\sqrt{1+\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{50}$; $Q = \frac{1.005(\sqrt{1+R2/R4})}{(R2/R3)-(R2/16R4)}$; $H_{OLP} = \frac{-R2/R1}{1+(R2/R4)}$

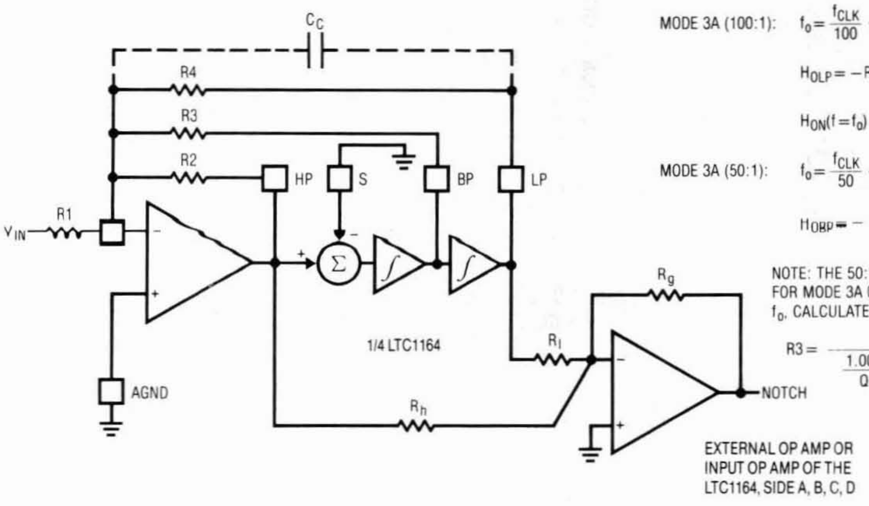
$H_{OBP} = -\frac{R3/R1}{1-(R3/16R4)}$; $H_{ON1}(f\to 0) = \frac{-R2/R1}{1+(R2/R4)}$

$H_{ON2}\left(f\to \frac{f_{CLK}}{2}\right) = -R2/R1$

NOTE: THE 50:1 EQUATIONS FOR MODE 2 ARE DIFFERENT FROM THE EQUATIONS FOR MODE 2 OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_0, CALCULATE R2/R4, SET R4; FROM THE Q VALUE, CALCULATE R3:

$R3 = \frac{R2}{\frac{1.005}{Q}\sqrt{1+\frac{R2}{R4}}+\frac{R2}{16R4}}$; THEN CALCULATE R1 TO SET THE DESIRED GAIN.

Figure 9. Mode 2: 2nd Order Filter Providing Notch, Bandpass, Lowpass


C_C
R4
R3
R2
HP
S
BP
LP
R1
V_{IN}
R_g
1/4 LTC1164
R_l
R_h
AGND
NOTCH
EXTERNAL OP AMP OR INPUT OP AMP OF THE LTC1164, SIDE A, B, C, D

MODE 3A (100:1): $f_0 = \frac{f_{CLK}}{100}\sqrt{\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{100}\sqrt{\frac{R_h}{R_l}}$; $H_{OHP} = -R2/R1$; $H_{OBP} = -R3/R1$

$H_{OLP} = -R4/R1$; $H_{ON1}(f\to 0) = \frac{R_g}{R_l}\times\frac{R4}{R1}$; $H_{ON2}\left(f\to \frac{f_{CLK}}{2}\right) = \frac{R_g}{R_h}\times\frac{R2}{R1}$

$H_{ON}(f=f_0) = Q\left(\frac{R_g}{R_l}H_{OLP}-\frac{R_g}{R_h}H_{OHP}\right)$; $Q = \frac{R3}{R2}\sqrt{\frac{R2}{R4}}$

MODE 3A (50:1): $f_0 = \frac{f_{CLK}}{50}\sqrt{\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{50}\sqrt{\frac{R_h}{R_l}}$; $H_{OHP}\left(f\to \frac{f_{CLK}}{2}\right) = -R2/R1$

$H_{OBP} = -\frac{R3/R1}{1-(R3/16R4)}$; $H_{OLP}(f=0) = -R4/R1$; $Q = \frac{1.005(\sqrt{R2/R4})}{(R2/R3)-(R2/16R4)}$

NOTE: THE 50:1 EQUATIONS FOR MODE 3A ARE DIFFERENT FROM THE EQUATIONS FOR MODE 3A OPERATION OF THE LTC1059, LTC1060 AND LTC1061. START WITH f_0, CALCULATE R2/R4, SET R4; FROM THE Q VALUE, CALCULATE R3:

$R3 = \frac{R2}{\frac{1.005}{Q}\sqrt{\frac{R2}{R4}}+\frac{R2}{16R4}}$; THEN CALCULATE R1 TO SET THE DESIRED GAIN.

Figure 10. Mode 3A: 2nd Order Filter Providing Highpass, Bandpass, Lowpass, Notch

APPLICATION CIRCUITS

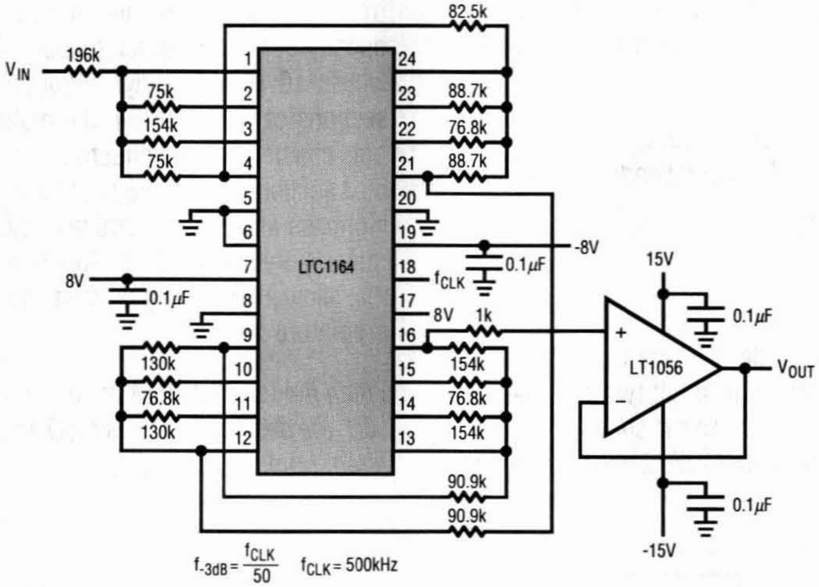
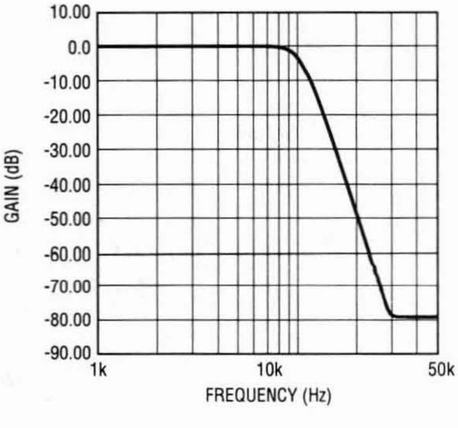
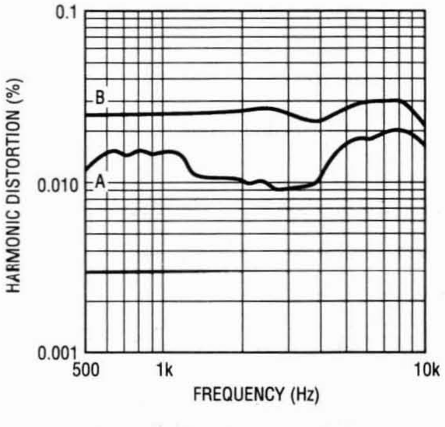

82.5k
VIN
196k
75k
154k
75k
88.7k
76.8k
88.7k
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
LTC1164
8V
0.1μF
-8V
0.1μF
fCLK
8V
1k
15V
0.1μF
LT1056
+
–
VOUT
130k
76.8k
130k
154k
76.8k
154k
90.9k
90.9k
0.1μF
-15V
$f_{-3dB} = \frac{f_{CLK}}{50}$
f_{CLK} = 500kHz

Figure 11. 8th Order Lowpass Butterworth, Passband Noise 90μV_{RMS} (Also Refer to the LTC1164-5)

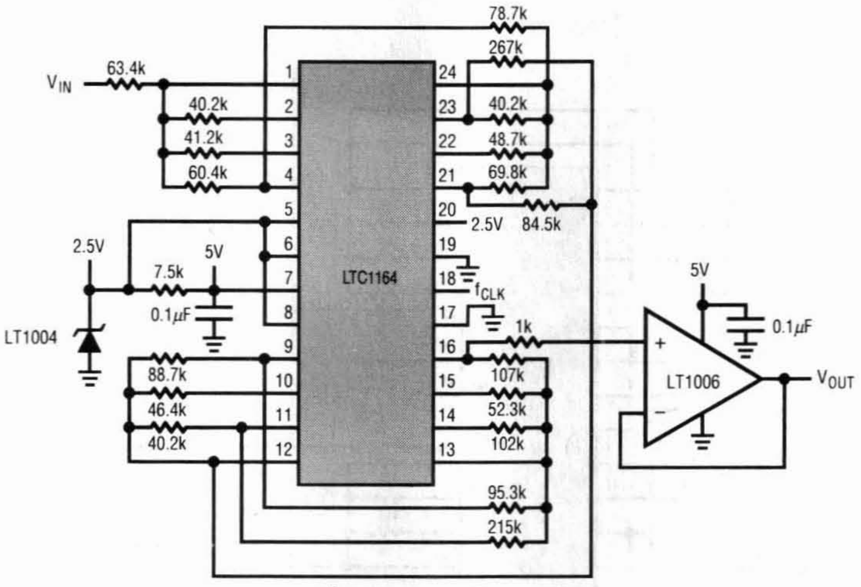


Graph 9. LTC1164 8th Order Butterworth, f_{CLK} = 500kHz, f_{-3dB} = 10kHz



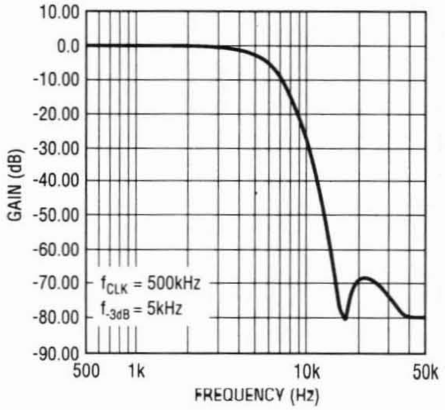
Graph 10. LTC1164 8th Order Butterworth, f_{CLK} = 500kHz, f_{-3dB} = 10kHz ±8V, A. 2V_{RMS}, B. 4V_{RMS}

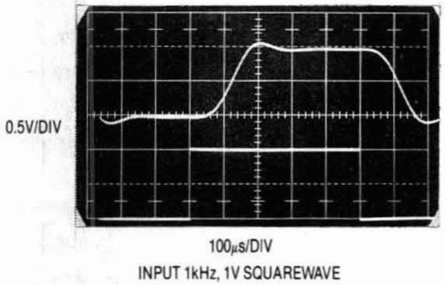
APPLICATION CIRCUITS


VIN
63.4k
40.2k
41.2k
60.4k
2.5V
5V
7.5k
0.1μF
LT1004
88.7k
46.4k
40.2k
1
2
3
4
5
6
7
8
9
10
11
12
LTC1164
24
23
22
21
20
19
18
17
16
15
14
13
78.7k
267k
40.2k
48.7k
69.8k
2.5V
84.5k
fCLK
1k
107k
52.3k
102k
95.3k
215k
5V
0.1μF
LT1006
+
−
VOUT

$f_{-3dB} = \frac{f_{CLK}}{100}$ $f_{CLK} = 500kHz$

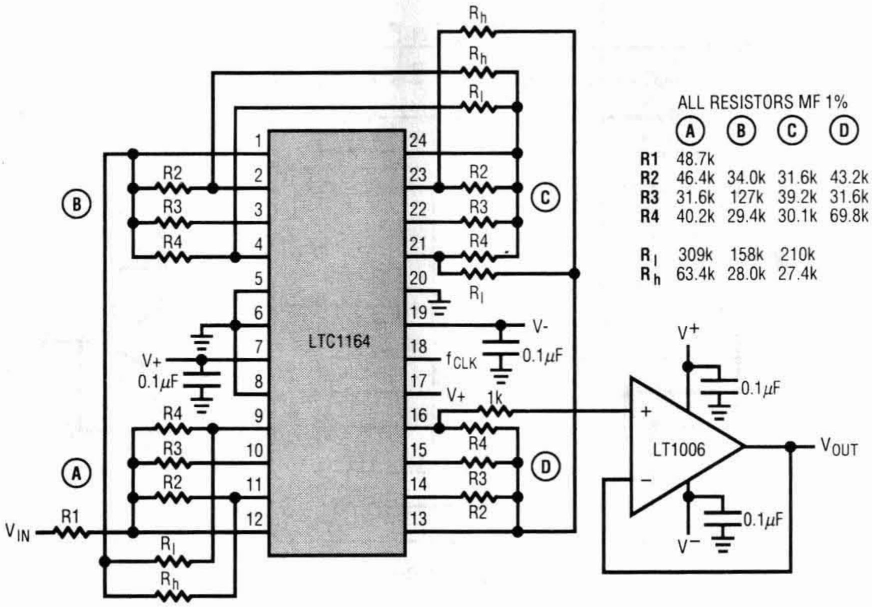
Figure 12. 8th Order Lowpass Single Supply Elliptic-Bessel Transitional Filter Total Supply Current = 4mA, Passband Noise $50\mu V_{RMS}$





Graph 11. LTC1164 8th Order Lowpass, Elliptic-Bessel Transitional Filter Single 5V Supply

APPLICATION CIRCUITS


Rh
Rh
Rl
R2
R3
R4
R2
R3
R4
Rl
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
LTC1164
Ⓑ
Ⓒ
Ⓐ
Ⓓ
V+
0.1μF
V-
f_{CLK}
0.1μF
V+
1k
R4
R3
R2
R4
R3
R2
R1
V_{IN}
Rl
Rh
V+
0.1μF
LT1006
+
−
V_{OUT}
0.1μF
V−

ALL RESISTORS MF 1%

	Ⓐ	Ⓑ	Ⓒ	Ⓓ
R1	48.7k			
R2	46.4k	34.0k	31.6k	43.2k
R3	31.6k	127k	39.2k	31.6k
R4	40.2k	29.4k	30.1k	69.8k
R_l	309k	158k	210k	
R_h	63.4k	28.0k	27.4k	

Figure 13. LTC1164 8th Order Lowpass Elliptic, f_{CUTOFF} = 5kHz, f_{CLK} = 250kHz, −78dB at 10kHz, Passband Noise = 110μV_{RMS} ±5V (Also Refer to the LTC1164-6)

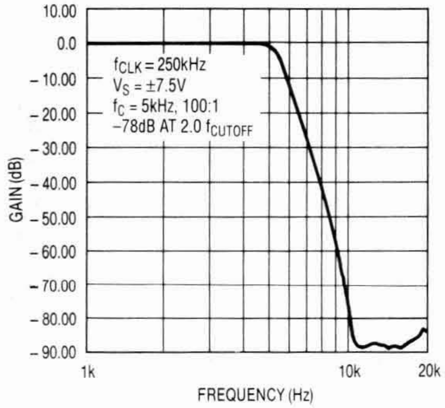
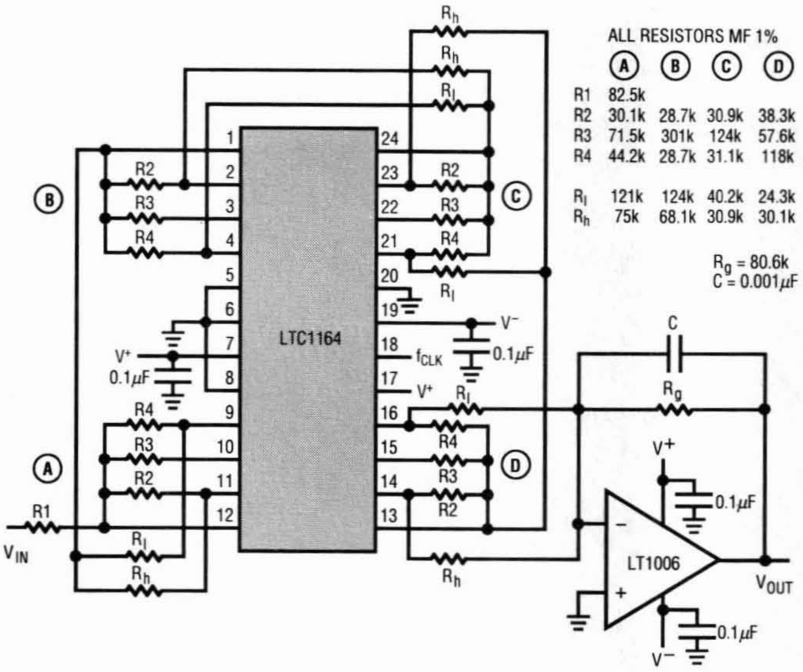


Figure 14. LTC1164 8th Order Lowpass Elliptic, f_{CUTOFF} = 5kHz

APPLICATION CIRCUITS



Rh
Rh
Rl
R2
R3
R4
Ⓑ
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
R2
R3
R4
Rl
Ⓒ
LTC1164
V⁺
0.1μF
V⁻
fCLK
0.1μF
V⁺
Rl
C
Rg
R4
R3
R2
Ⓐ
R1
VIN
Rl
Rh
R4
R3
R2
Ⓓ
Rh
V⁺
0.1μF
LT1006
VOUT
V⁻
0.1μF

ALL RESISTORS MF 1%

	Ⓐ	Ⓑ	Ⓒ	Ⓓ
R1	82.5k			
R2	30.1k	28.7k	30.9k	38.3k
R3	71.5k	301k	124k	57.6k
R4	44.2k	28.7k	31.1k	118k
R_l	121k	124k	40.2k	24.3k
R_h	75k	68.1k	30.9k	30.1k

$R_g = 80.6k$
$C = 0.001\mu F$

Figure 15. LTC1164 9th Order Lowpass Elliptic, Fixed $f_{CUTOFF} = 4kHz$, $f_{CLK} = 400kHz$, – 74dB at 5kHz, Passband Noise = $210\mu V_{RMS}$ ± 5V

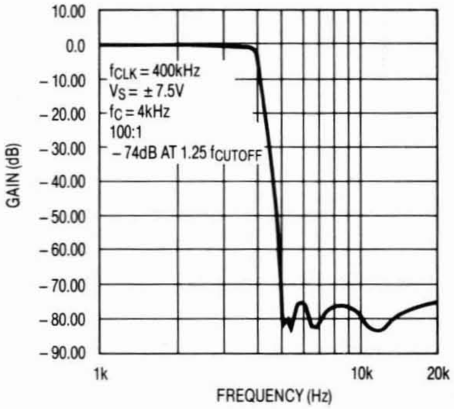


Figure 16. LTC1164 9th Order Lowpass Elliptic, $f_{CUTOFF} = 4kHz$

8

NOTES

SECTION 9—MICROPROCESSOR SUPERVISORY CIRCUITS

SECTION 9—MICROPROCESSOR SUPERVISORY CIRCUITS

INDEX **9-2**

SELECTION GUIDE **9-3**

PROPRIETARY PRODUCTS

LTC690/LTC691/LTC694/LTC695, Microprocessor Supervisory Circuits **9-4**

LTC699, Microprocessor Supervisory Circuit **9-18**

LTC1232, Microprocessor Supervisory Circuit **9-22**

LTC1235, Microprocessor Supervisory Circuit with Conditional Battery Backup **9-29**

LTC FAMILY OF SUPERVISORY CIRCUIT PRODUCTS

FUNCTION		LTC1235	LTC690	LTC691	LTC694	LTC695	LTC699	LTC1232
Pushbutton Reset		X						X
Battery Backup Switching		X	X	X	X	X		
Conditional Battery Backup		X						
RAM Write Protect		X		X		X		
Watchdog Timer		X	X	X	X	X	X	X
Power Fail Warning		X	X	X	X	X		
Power Up/Down Reset		X	X	X	X	X	X	X
Reset Threshold (V)		4.65	4.65	4.65	4.65	4.65	4.65	4.62/4.37
Reset Pulse Width (ms)		200	50	50	200	200	200	610
Guaranteed Reset Level (V_{CC})		1.0	1.0	1.0	1.0	1.0	1.0	1.0
Power Supply Current (μA)		600	600	600	600	600	600	500
Packages:	Plastic	16	8	16	8	16	8	8
	Ceramic DIP		8	16	8	16		
	SOIC	16*	8	16*	8	16*	8	8
Temperature Ranges		C	C, I, M	C, I, M	C, I, M	C, I, M	C	C, I

Notes: C = 0°C to +70°C I = –40°C to +85°C M = –55°C to +125°C *0.3 Inch Wide SOL Package

DEFINITIONS OF FUNCTIONS

Pushbutton Reset: Provides a manual reset input, usually triggered by a pushbutton switch, which is debounced and will initiate the usual reset sequence.

Battery Backup Switching: When V_{CC} drops below the battery voltage, V_{OUT} is connected to V_{BATT} and the device is placed in standby mode to conserve power. This provides backup power to the CMOS RAM while consuming less than 1μA of supply current.

Conditional Battery Backup: Electrically disconnects the battery during shipment and storage to prevent unnecessary discharge. Disconnection is done by detecting the power down sequencing of the supply and battery inputs.

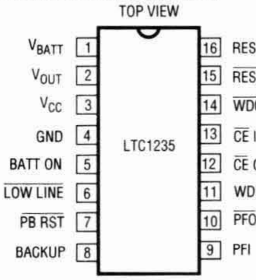
RAM Write Protect: The system RAM enable line is gated by the supervisory circuit. When the supply voltage drops below the reset voltage threshold, the enable line is inhibited, preventing erroneous data from being written into the RAM when V_{CC} is at an invalid level. The maximum enable delay for LTC's supervisors is 45ns.

Watchdog Timer: Monitors the activity of the μP. The processor must toggle this input line before the given timeout period expires, or a reset will be initiated. This function is intended to prevent μP's from becoming accidentally stalled in microcode loops indefinitely.

Power Fail Warning: Provides early warning to the μP of an impending power failure by monitoring the unregulated power supply. This gives the processor time to perform shutdown activities before all regulated power is lost.

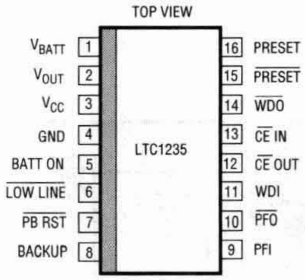
Power Up/Down Reset: Resets the μP when the power supply line drops below the preset threshold. LTC's supervisors will hold the reset line low down to supply voltages of 1.0V, providing a reliable reset through V_{CC} voltages which may allow the processor to begin operation.

PIN CONFIGURATIONS


TOP VIEW
VBATT 1
VOUT 2
VCC 3
GND 4
BATT ON 5
LOW LINE 6
PB RST 7
BACKUP 8
LTC1235
16 RESET
15 RESET
14 WDO
13 CE IN
12 CE OUT
11 WDI
10 PFO
9 PFI

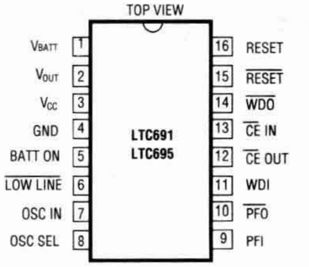
N PACKAGE
16-LEAD PLASTIC DIP

LTC1235 • 01


TOP VIEW
VBATT 1
VOUT 2
VCC 3
GND 4
BATT ON 5
LOW LINE 6
PB RST 7
BACKUP 8
LTC1235
16 PRESET
15 PRESET
14 WDO
13 CE IN
12 CE OUT
11 WDI
10 PFO
9 PFI

S PACKAGE
16-LEAD PLASTIC SOL

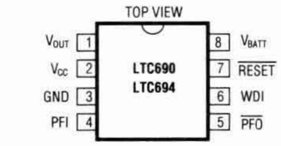
LTC1235 • 02


TOP VIEW
VBATT 1
VOUT 2
VCC 3
GND 4
BATT ON 5
LOW LINE 6
OSC IN 7
OSC SEL 8
LTC691
LTC695
16 RESET
15 RESET
14 WDO
13 CE IN
12 CE OUT
11 WDI
10 PFO
9 PFI

J PACKAGE
16-LEAD CERAMIC DIP

N PACKAGE
16-LEAD PLASTIC DIP

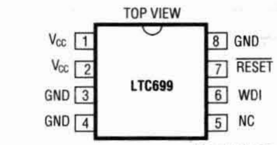
S PACKAGE
16-LEAD PLASTIC SOL


TOP VIEW
VOUT 1
VCC 2
GND 3
PFI 4
LTC690
LTC694
8 VBATT
7 RESET
6 WDI
5 PFO

J8 PACKAGE
8-LEAD CERAMIC DIP

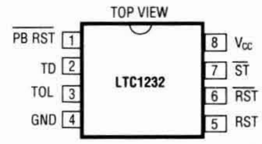
N8 PACKAGE
8-LEAD PLASTIC DIP

S8 PACKAGE
8-LEAD PLASTIC SOIC


TOP VIEW
VCC 1
VCC 2
GND 3
GND 4
LTC699
8 GND
7 RESET
6 WDI
5 NC

J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP


TOP VIEW
PB RST 1
TD 2
TOL 3
GND 4
LTC1232
8 VCC
7 ST
6 RST
5 RST

J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP

LINEAR TECHNOLOGY

LTC690/LTC691
LTC694/LTC695
Microprocessor Supervisory Circuits

FEATURES

- *Guaranteed* Reset Assertion at V_{CC} = 1V
- 1.5mA Maximum Supply Current
- Fast (35ns Max.) Onboard Gating of RAM Chip Enable Signals
- SO-8 and SO-16 Packaging
- 4.65V Precision Voltage Monitor
- Power OK/Reset Time Delay: 50ms, 200ms, or Adjustable
- Minimum External Component Count
- 1μA Maximum Standby Current
- Voltage Monitor for Power Fail or Low Battery Warning
- Thermal Limiting
- Performance Specified Over Temperature
- Superior Upgrade for MAX690 Family

APPLICATIONS

- Critical μP Power Monitoring
- Intelligent Instruments
- Battery-Powered Computers and Controllers
- Automotive Systems

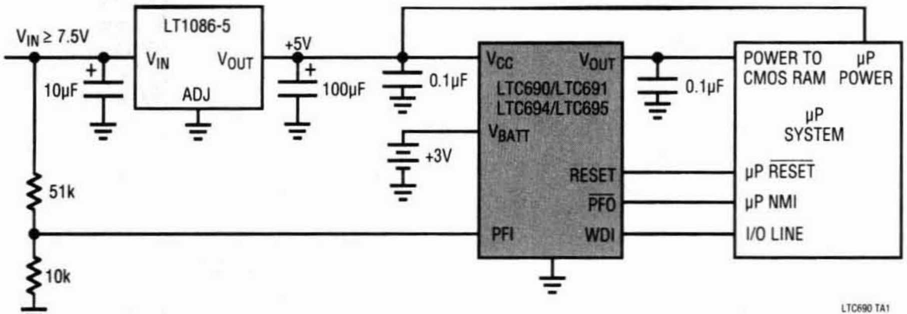
DESCRIPTION

The LTC690 family provides complete power supply monitoring and battery control functions for microprocessor reset, battery backup, CMOS RAM write protection, power failure warning and watchdog timing. A precise internal voltage reference and comparator circuit monitor the power supply line. When an out-of-tolerance condition occurs, the reset outputs are forced to active states and the Chip Enable output unconditionally write-protects external memory. In addition, the $\overline{\text{RESET}}$ output is guaranteed to remain logic low even with V_{CC} as low as 1V.

The LTC690 family powers the active CMOS RAMs with a charge pumped NMOS power switch to achieve low dropout and low supply current. When primary power is lost, auxiliary power, connected to the battery input pin, powers the RAMs in standby through an efficient PMOS switch.

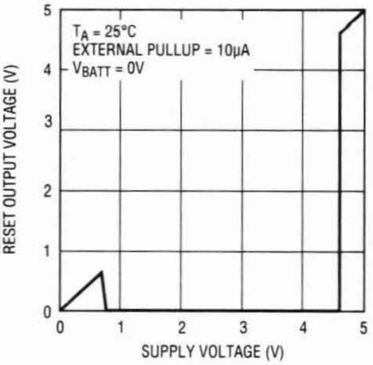
For an early warning of impending power failure, the LTC690 family provides an internal comparator with a user-defined threshold. An internal watchdog timer is also available, which forces the reset pins to active states when the watchdog input is not toggled prior to a preset time-out period.

TYPICAL APPLICATION



MICROPROCESSOR RESET, BATTERY BACKUP, POWER FAILURE WARNING AND WATCHDOG TIMING ARE ALL IN A SINGLE CHIP FOR MICROPROCESSOR SYSTEMS.

$\overline{\text{RESET}}$ Output Voltage vs Supply Voltage



LTC690 TA2

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Terminal Voltage
- V_{CC} .... –0.3V to 6.0V
- V_{BATT} .... –0.3V to 6.0V
- All Other Inputs .... –0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

V_{OUT} Output Current .... Short Circuit Protected

Power Dissipation 500mW

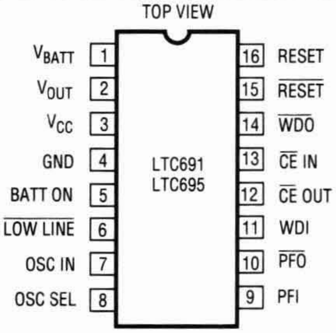
Operating Temperature Range
- LTC690/91/94/95C .... 0°C to 70°C
- LTC690/91/94/95I .... –40°C to 85°C

Storage Temperature Range .... –65°C to 150°C

Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

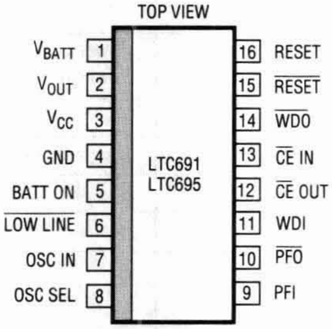
(Note 3)


TOP VIEW
V_{BATT} 1
V_{OUT} 2
V_{CC} 3
GND 4
BATT ON 5
$\overline{\text{LOW LINE}}$ 6
OSC IN 7
OSC SEL 8
16 RESET
15 $\overline{\text{RESET}}$
14 $\overline{\text{WDO}}$
13 $\overline{\text{CE}}$ IN
12 $\overline{\text{CE}}$ OUT
11 WDI
10 $\overline{\text{PFO}}$
9 PFI
LTC691
LTC695

N PACKAGE
16-LEAD PLASTIC DIP

ORDER PART NUMBER

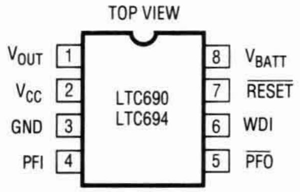
LTC691CN
LTC691IN
LTC695CN
LTC695IN


TOP VIEW
V_{BATT} 1
V_{OUT} 2
V_{CC} 3
GND 4
BATT ON 5
$\overline{\text{LOW LINE}}$ 6
OSC IN 7
OSC SEL 8
16 RESET
15 $\overline{\text{RESET}}$
14 $\overline{\text{WDO}}$
13 $\overline{\text{CE}}$ IN
12 $\overline{\text{CE}}$ OUT
11 WDI
10 $\overline{\text{PFO}}$
9 PFI
LTC691
LTC695

S PACKAGE
16-LEAD PLASTIC SOL

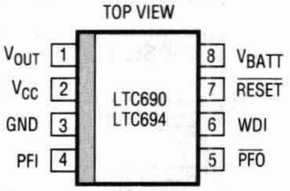
ORDER PART NUMBER

LTC691CS
LTC691IS
LTC695CS
LTC695IS


TOP VIEW
V_{OUT} 1
V_{CC} 2
GND 3
PFI 4
8 V_{BATT}
7 $\overline{\text{RESET}}$
6 WDI
5 $\overline{\text{PFO}}$
LTC690
LTC694

N8 PACKAGE
8-LEAD PLASTIC DIP

LTC690CN8
LTC690IN8
LTC694CN8
LTC694IN8


TOP VIEW
V_{OUT} 1
V_{CC} 2
GND 3
PFI 4
8 V_{BATT}
7 $\overline{\text{RESET}}$
6 WDI
5 $\overline{\text{PFO}}$
LTC690
LTC694

S8 PACKAGE
8-LEAD PLASTIC SOIC

S8 PART MARKING

690
690I
694
694I

LTC690CS8
LTC690IS8
LTC694CS8
LTC694IS8

PRODUCT SELECTION GUIDE

PART NUMBER	CHIP ENABLE SIGNALS	RESET ACTIVE TTIME	WATCHDOG TIME-OUT PERIOD	BASE DRIVE FOR EXT. PNP TRANSISTOR	ADDITIONAL OUTPUTS $\overline{\text{WDO}}$, RESET, $\overline{\text{LOW LINE}}$
LTC690	No	50ms	1.6 sec	No	No
LTC691	Yes	50ms or Adjustable	1.6 sec or Adjustable	Yes	Yes
LTC694	No	200ms	1.6 sec	No	No
LTC695	Yes	200ms or Adjustable	1.6 sec or Adjustable	Yes	Yes

ELECTRICAL CHARACTERISTICS

V_{CC} = Full Operating Range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
Battery Backup Switching						
Operating Voltage Range V_{CC} V_{BATT}			 4.75 2.0		 5.5 4.25	V
V_{OUT} Output Voltage	I_{OUT} = 1mA	 ●	V_{CC} − 0.05 V_{CC} − 0.1	V_{CC} − 0.005 V_{CC} − 0.005		V
	I_{OUT} = 50mA		V_{CC} − 0.5	V_{CC} − 0.25		
V_{OUT} in Battery Backup Mode	I_{OUT} = 250µA, $V_{CC} < V_{BATT}$		V_{BATT} − 0.1	V_{BATT} − 0.02		V
Supply Current (exclude I_{OUT})	$I_{OUT} \leq$ 50mA	 ●		0.6 0.6	1.5 2.5	mA
Supply Current in Battery Backup Mode	V_{CC} = 0V, V_{BATT} = 2.8V	 ●		0.04 0.04	1 5	µA
Battery Standby Current (+ = Discharge, − = Charge)	5.5 > V_{CC} > V_{BATT} + 0.2V	 ●	−0.1 −1.0		+0.02 +0.1	µA
Battery Switchover Threshold $V_{CC} - V_{BATT}$	Power Up Power Down			70 50		mV
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage (Note 4)	I_{SINK} = 3.2mA				0.4	V
BATT ON Output Short Circuit Current (Note 4)	BATT ON = V_{OUT} Sink Current			35		m
	BATT ON = 0V Source Current		0.5	1	25	µA
Reset and Watchdog Timer						
Reset Voltage Threshold		●	4.5	4.65	4.75	V
Reset Threshold Hysteresis				40		mV
Reset Active Time (LTC690/91) (Note 5)	OSC SEL HIGH, V_{CC} = 5V	 ●	40 35	50 50	60 70	ms
Reset Active Time (LTC694/95) (Note 5)	OSC SEL HIGH, V_{CC} = 5V	 ●	160 140	200 200	240 280	ms
Watchdog Timeout Period, Internal Oscillator	Long Period, V_{CC} = 5V	 ●	1.2 1.0	1.6 1.6	2.0 2.25	sec
	Short Period, V_{CC} = 5V	 ●	80 70	100 100	120 140	ms
Watchdog Time-out Period, External Clock (Note 6)	Long Period Short Period		4032 960		4097 1025	Clock Cycles
Reset Active Time PSRR				1		ms/V
Watchdog Time-out Period PSRR, Internal OSC				1		ms/V
Minimum WDI Input Pulse Width	V_{IL} = 0.4V, V_{IH} = 3.5V	●	200			ns
$\overline{\text{RESET}}$ Output Voltage At V_{CC} = 1V	I_{SINK} = 10µA, V_{CC} = 1V			4	200	mV
$\overline{\text{RESET}}$ and $\overline{\text{LOW LINE}}$ Output Voltage (Note 4)	I_{SINK} = 1.6mA, V_{CC} = 4.25V I_{SOURCE} = 1µA, V_{CC} = 5V		 3.5		0.4	V
RESET and $\overline{\text{WDO}}$ Output Voltage (Note 4)	I_{SINK} = 1.6mA, V_{CC} = 5V SOURCE = 1µA, V_{CC} = 4.25V		 3.5		0.4	V

ELECTRICAL CHARACTERISTICS

V_{CC} = Full Operating Range, V_{BATT} = 2.8V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
RESET, $\overline{\text{RESET}}$, $\overline{\text{WDO}}$, $\overline{\text{LOW LINE}}$	Output Source Current		1	3	25	µA
Output Short Circuit Current (Note 4)	Output Sink Current			25		mA
WDI Input Threshold	Logic Low Logic High		 2.0		0.8	V
WDI Input Current	WDI = V_{OUT} WDI = 0V	● ●	 −50	4 −8	50	µA
Power Fail Detector						
PFI Input Threshold	V_{CC} = 5V	●	1.25	1.3	1.35	V
PFI Input Threshold PSRR				0.3		mV/V
PFI Input Current				±0.01	±25	nA
$\overline{\text{PFO}}$ Output Voltage (Note 4)	I_{SINK} = 3.2mA I_{SOURCE} = 1µA		 3.5		0.4	V
$\overline{\text{PFO}}$ Short Circuit Source Current	PFI = HIGH, $\overline{\text{PFO}}$ = 0V		1	3	25	µA
(Note 4)	PFI = LOW, $\overline{\text{PFO}}$ = V_{OUT}			25		mA
PFI Comparator Response Time (falling)	ΔV_{IN} = −20mV, V_{OD} = 15mV			2		µs
PFI Comparator Response Time (rising) (Note 4)	ΔV_{IN} = 20mV, V_{OD} = 15mV with 10kΩ Pullup			40 8		µs
Chip Enable Gating						
$\overline{\text{CE}}$ IN Threshold	V_{IL} V_{IH}		 2.0		0.8	V
$\overline{\text{CE}}$ IN Pullup Current (Note 7)				3		µA
$\overline{\text{CE}}$ OUT Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 3.0mA I_{SOURCE} = 1µA, V_{CC} = 0V		 V_{OUT} − 1.5 V_{OUT} − 0.05		0.4	V
$\overline{\text{CE}}$ Propagation Delay	V_{CC} = 5V, C_L = 20pF	 ●		20 20	35 45	ns
$\overline{\text{CE}}$ OUT Output Short Circuit Current	Output Source Current Output Sink Current			30 35		mA
Oscillator						
OSC IN Input Current (Note 7)				±2		µA
OSC SEL Input Pullup Current (Note 7)				5		µA
OSC IN Frequency Range	OSC SEL = 0V	●	0		250	kHz
OSC IN Frequency with External Capacitor	OSC SEL = 0V, C_{OSC} = 47pF			4		kHz

The ● denotes specifications which apply over the operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: For military temperature range parts or for the LTC692 and LTC693, consult the factory.

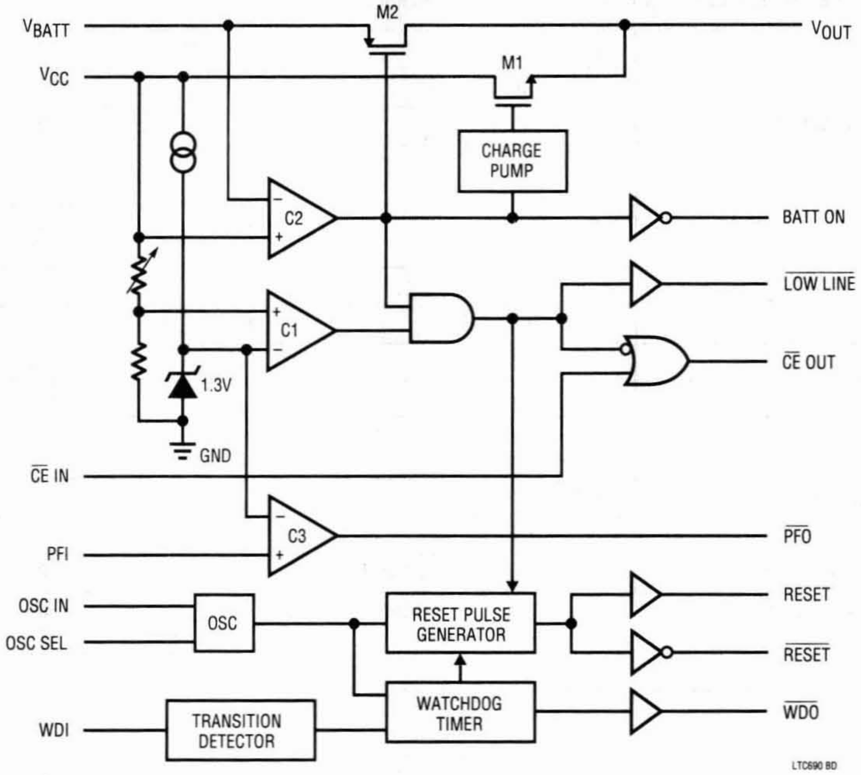
Note 4: The output pins of BATT ON, $\overline{\text{LOW LINE}}$, $\overline{\text{PFO}}$, $\overline{\text{WDO}}$, $\overline{\text{RESET}}$ and RESET have weak internal pullups of typically 3µA. However, external pullup resistors may be used when higher speed is required.

Note 5: The LTC690 and LTC691 have minimum reset active time of 35ms (50ms typically) while the LTC694 and LTC695 have longer minimum reset active time of 140ms (200ms typically). The reset active time of the LTC691 and LTC695 can be adjusted (see Table 2 in Applications Information Section).

Note 6: The external clock feeding into the circuit passes through the oscillator before clocking the watchdog timer (See BLOCK DIAGRAM). Variation in the time-out period is caused by phase errors which occur when the oscillator divides the external clock by 64. The resulting variation in the time-out period is 64 clocks plus one clock of jitter.

Note 7: The input pins of $\overline{\text{CE}}$ IN, OSC IN and OSC SEL have weak internal pullups which pull to the supply when the input pins are floating.

BLOCK DIAGRAM


VBATT
VCC
M2
M1
VOUT
CHARGE PUMP
C2
C1
C3
1.3V
GND
CE IN
PFI
OSC IN
OSC SEL
OSC
WDI
TRANSITION DETECTOR
RESET PULSE GENERATOR
WATCHDOG TIMER
BATT ON
LOW LINE
CE OUT
PFO
RESET
RESET
WDO
LTC690 BD

PIN FUNCTIONS

V_{CC}: +5V supply input. The V_{CC} pin should be bypassed with a 0.1µF capacitor.

V_{OUT}: Voltage output for backed up memory. Bypass with a capacitor of 0.1µF or greater. During normal operation, V_{OUT} obtains power from V_{CC} through an NMOS power switch, M1, which can deliver up to 50mA and has a typical on resistance of 5Ω. When V_{CC} is lower than V_{BATT}, V_{OUT} is internally switched to V_{BATT}. If V_{OUT} and V_{BATT} are not used, connect V_{OUT} to V_{CC}.

V_{BATT}: Backup battery input. When V_{CC} falls below V_{BATT}, auxiliary power, connected to V_{BATT}, is delivered to V_{OUT} through PMOS witch, M2. If backup battery or auxiliary power is not used, V_{BATT} should be connected to GND.

GND: Ground pin.

BATT ON: Battery on logic output from comparator C2. BATT ON goes low when V_{OUT} is internally connected to V_{CC}. The output typically sinks 35mA and can provide base drive for an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}. BATT ON goes high when V_{OUT} is internally switched to V_{BATT}.

PFI: Power Failure Input. PFI is the noninverting input to the Power Fail Comparator, C3. The inverting input is internally connected to a 1.3V reference. The Power Failure Output remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. Connect PFI to GND or V_{OUT} when C3 is not used.

PIN FUNCTIONS

$\overline{\text{PFO}}$: Power Failure Output from C3. $\overline{\text{PFO}}$ remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. When V_{CC} is lower than V_{BATT}, C3 is shut down and $\overline{\text{PFO}}$ is forced low.

$\overline{\text{RESET}}$: Logic output for µP reset control. Whenever V_{CC} falls below either the reset voltage threshold (4.65V, typically) or V_{BATT}, $\overline{\text{RESET}}$ goes active low. After V_{CC} returns to 5V, reset pulse generator forces $\overline{\text{RESET}}$ to remain active low for a minimum of 35ms for the LTC690/1 (140ms for the LTC694/5). When the watchdog timer is enabled but not serviced prior to a preset time-out period, reset pulse generator also forces $\overline{\text{RESET}}$ to active low for a minimum of 35ms for the LTC690/1 (140ms for the LTC694/5) for every preset time-out period (see Figure 10). The reset active time is adjustable on the LTC691/5.

RESET: RESET is an active high logic ouput. It is the inverse of $\overline{\text{RESET}}$.

$\overline{\text{LOW LINE}}$: Logic output from comparator C1. $\overline{\text{LOW LINE}}$ indicates a low line condition at the V_{CC} input. When V_{CC} falls below the reset voltage threshold (4.65V typically), $\overline{\text{LOW LINE}}$ goes low. As soon as V_{CC} rises above the reset voltage threshold, $\overline{\text{LOW LINE}}$ returns high (see Figure 1). $\overline{\text{LOW LINE}}$ goes low when V_{CC} drops below V_{BATT} (see Table 1).

WDI: Watchdog Input, WDI, is a three level input. Driving WDI either high or low for longer than the watchdog time-out period, forces both $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ low. Floating WDI disables the Watchdog Timer. The timer resets itself with each transition of the Watchdog Input (see Figure 10).

$\overline{\text{WDO}}$: Watchdog logic output. When the watchdog input remains either high or low for longer than the watchdog time-out period, $\overline{\text{WDO}}$ goes low. $\overline{\text{WDO}}$ is set high whenever there is a transition on the WDI pin, or $\overline{\text{LOW LINE}}$ goes low. The watchdog timer can be disabled by floating WDI (see Figure 10).

$\overline{\text{CE}}$ IN: Logic input to the $\overline{\text{Chip Enable}}$ gating circuit. $\overline{\text{CE}}$ IN can be derived from microprocessor's address line and/or decoder output. See Applications Information Section and Figure 4 for additional information.

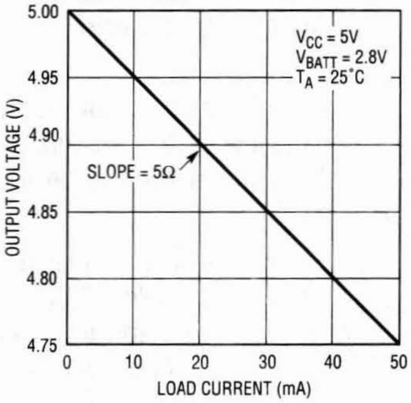
$\overline{\text{CE}}$ OUT: Logic output on the $\overline{\text{Chip Enable}}$ gating circuit. When V_{CC} is above the reset voltage threshold, $\overline{\text{CE}}$ OUT is a buffered replica of $\overline{\text{CE}}$ IN. When V_{CC} is below the reset voltage threshold $\overline{\text{CE}}$ OUT is forced high (see Figure 4).

OSC SEL: Oscillator Selection input. When OSC SEL is high or floating, the internal oscillator sets the reset active time and watchdog time-out period. Forcing OSC SEL low, allows OSC IN be driven from an external clock signal or external capacitor be connected between OSC IN and GND.

OSC IN: Oscillator Input. OSC IN can be driven by an external clock signal or external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In this configuration the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula (see Applications Information Section). When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 50ms typical for the LTC691 and 200ms typical for the LTC695. OSC IN selects between the 1.6 seconds and 100ms typical watchdog time-out periods. In both cases, the time-out period immediately after a reset is 1.6 seconds typical.

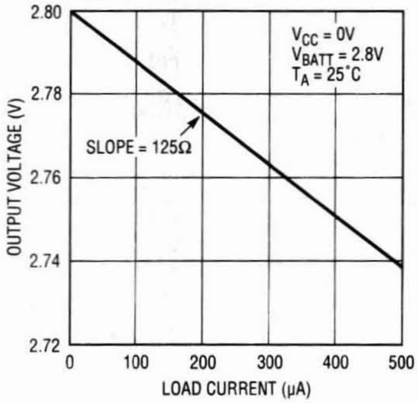
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUT} vs I_{OUT}



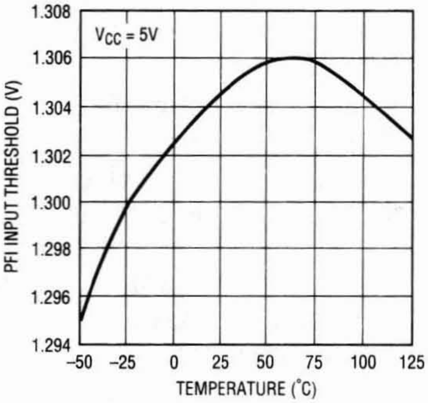
LTC690 G1

V_{OUT} vs I_{OUT}



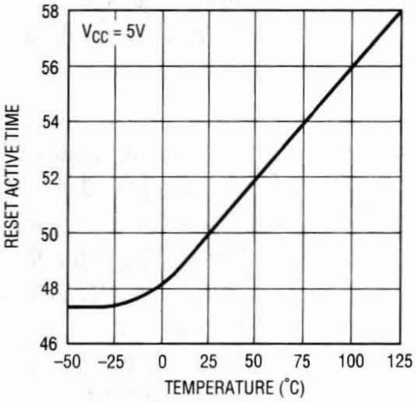
LTC690 G2

Power Failure Input Threshold vs Temperature



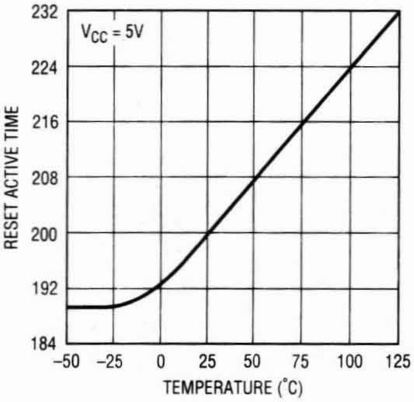
LTC690 G3

Reset Active Time vs Temperature LTC690-1



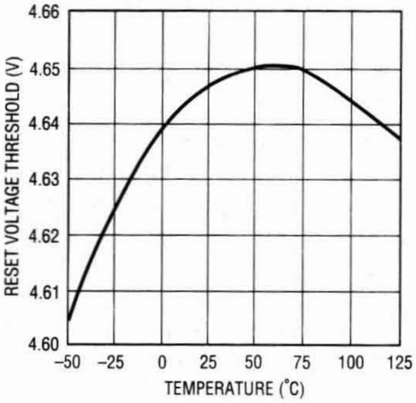
LTC690 G4

Reset Active Time vs Temperature LTC694-5



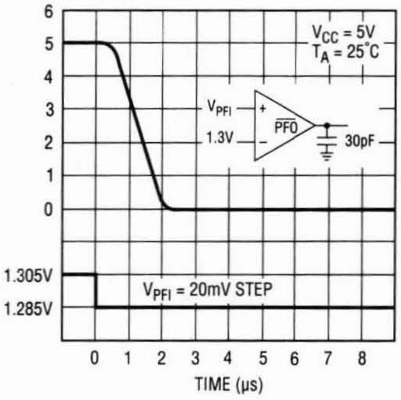
LTC690 G5

Reset Voltage Threshold vs Temperature



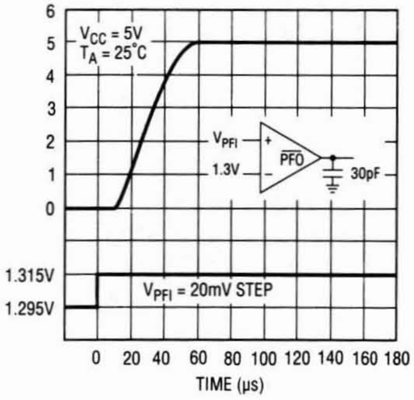
LTC690 G6

Power Fail Comparator Response Time



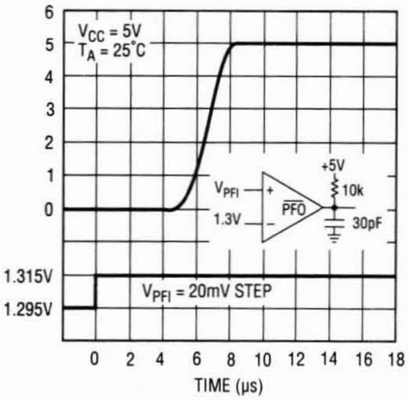
LTC690 G7

Power Fail Comparator Response Time



LTC690 G8

Power Fail Comparator Response Time with Pullup Resistor



LTC690 G9

APPLICATIONS INFORMATION

Microprocessor Reset

The LTC690 family uses a bandgap voltage reference and a precision voltage comparator C1 to monitor the 5V supply input on V_{CC} (see BLOCK DIAGRAM). When V_{CC} falls below the reset voltage threshold, the $\overline{RESET}$ output is forced to active low state. The reset voltage threshold accounts for a 5% variation on V_{CC}, so the $\overline{RESET}$ output becomes active low when V_{CC} falls below 4.75V (4.65V typical). On power-up, the $\overline{RESET}$ signal is held active low for a minimum of 35ms for the LTC690/1 (140ms for the LTC694/5) after reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. The reset active time is adjustable on the LTC691/5. On power-down, the $\overline{RESET}$ signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the $\overline{RESET}$ signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at V_{CC} pin do not activate the $\overline{RESET}$ output. Response time is typically 10µs. To help prevent mistriggering due to transient loads, V_{CC} pin should be bypassed with a 0.1µF capacitor with the leads trimmed as short as possible.

The LTC691 and LTC695 have two additional outputs: RESET and $\overline{LOW\ LINE}$. RESET is an active high output and is the inverse of $\overline{RESET}$. $\overline{LOW\ LINE}$ is the output of the precision voltage comparator C1. When V_{CC} falls below the reset voltage threshold, $\overline{LOW\ LINE}$ goes low. $\overline{LOW\ LINE}$ returns high as soon as V_{CC} rises above the reset voltage threshold.

Battery Switchover

The battery switchover circuit compares V_{CC} to the V_{BATT} input, and connects V_{OUT} to whichever is higher. When V_{CC} is rising and is 70mV higher than V_{BATT}, the battery switchover comparator, C2, connects V_{OUT} to V_{CC} through a charge pumped NMOS power switch, M1. When V_{CC} falls to 50mV greater than V_{BATT}, C2 connects V_{OUT} to V_{BATT} through a PMOS switch, M2. C2 has typically 20mV of hysteresis to prevent spurious switching when V_{CC} remains nearly equal to V_{BATT}. The response time of C2 is approximately 20µs.

During normal operation, the LTC690 family uses a charge pumped NMOS power switch to achieve low dropout and low supply current. This power switch can deliver up to 50mA to V_{OUT} from V_{CC} and has a typical on resistance of 5Ω. The V_{OUT} pin should be bypassed with a capacitor of 0.1µF or greater to ensure stability. Use of a larger bypass capacitor is advantageous for supplying current to heavy transient loads.

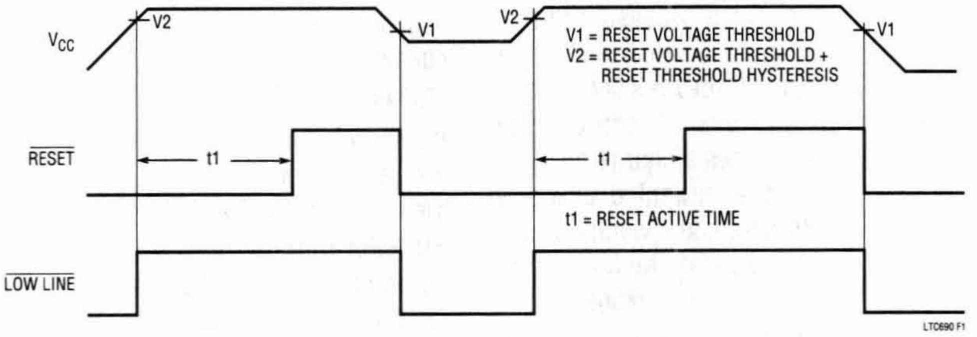

V_{CC}
V2
V1
V2
V1
V1 = RESET VOLTAGE THRESHOLD
V2 = RESET VOLTAGE THRESHOLD + RESET THRESHOLD HYSTERESIS
RESET
t1
t1
t1 = RESET ACTIVE TIME
LOW LINE
LTC690 F1

Figure 1. Reset Active Time

APPLICATIONS INFORMATION

When operating currents larger than 50mA are required from V_{OUT}, or a lower dropout (V_{CC} - V_{OUT} voltage differential) is desired, the LTC691 and LTC695 should be used. These products provide BATT ON output to drive the base of external PNP transistor (Figure 2). If higher currents are needed with the LTC690 and LTC694, a high current Schottky diode can be connected from the V_{CC} pin to the V_{OUT} pin to supply the extra current.

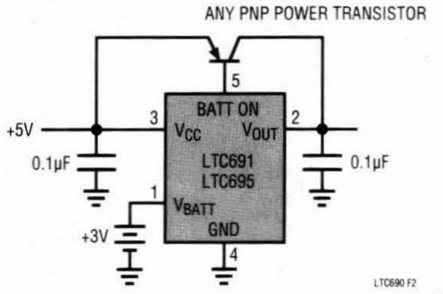


Figure 2. Using BATT ON to Drive External PNP Transistor

The LTC690 family is protected for safe area operation with short circuit limit. Output current is limited to approximately 200mA. If the device is overloaded for long period of time, thermal shutdown turns the power switch off until the device cools down. The threshhold temperature for thermal shutdown is approximately 155°C with about 10°C of hysteresis which prevents the device from oscillating in and out of shutdown.

The PNP switch used in competitive devices was not chosen for the internal power switch because it injects unwanted current into the substrate. This current is collected by the V_{BATT} pin in competitive devices and adds to the charging current of the battery which can damage lithium batteries. LTC690 family uses a charge pumped NMOS power switch to eliminate unwanted charging current while achieving low dropout and low supply current. Since no current goes to the substrate, the current collected by V_{BATT} pin is strictly junction leakage.

A 125Ω PMOS switch connects the V_{BATT} input to V_{OUT} in battery backup mode. The switch is designed for very low dropout voltage (input-to-output differential). This feature is advantageous for low current applications such as battery backup in CMOS RAM and other low power CMOS circuitry. The supply current in battery backup mode is 1µA maximum.

The operating voltage at the V_{BATT} pin ranges from 2.0V to 4.25V. High value capacitors, such as electrolytic or farad-size double layer capacitors, can be used for short term memory backup instead of a battery. The charging resistor for both capacitors and rechargeable batteries should be connected to V_{OUT} since this eliminates the discharge path that exists when the resistor is connected to V_{CC} (Figure 3).

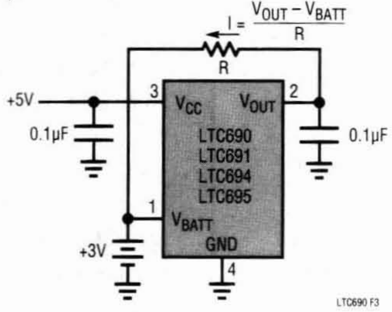


Figure 3. Charging External Battery Through V_{OUT}

Replacing the Backup Battery

When changing the backup battery with system power on, spurious resets can occur while battery is removed due to battery standby current. Although battery standby current is only a tiny leakage current, it can still charge up the stray capacitance on the V_{BATT} pin. The oscillation cycle is as follows: When V_{BATT} reaches within 50mV of V_{CC}, the LTC690 switches to battery backup. V_{OUT} pulls V_{BATT} low and the device goes back to normal operation. The leakage current then charges up the V_{BATT} pin again and the cycle repeats.

If spurious resets during battery replacement pose no problems, then no action is required. Otherwise, two methods can be used to eliminate this problem. First, a capacitor from V_{BATT} to GND will allow time for battery replacement by slowing the charge rate. For example, the battery standby current is 1µA maximum over temperature and the external capacitor required to slow the charge rate is:

$$C_{EXT} \geq T_{REQ'D}\left(\frac{1\mu A}{V_{CC} - V_{BATT}}\right)$$

where $T_{REQ'D}$ is the maximum time required to replace the

APPLICATIONS INFORMATION

backup battery. With V_{CC} = 4.5V, V_{BATT} = 3V and $T_{REQ'D}$ = 3 sec, the value for external capacitor is 2μF. Second, a resistor from V_{BATT} to GND will hold the pin low while changing the battery. For example, the battery standby current is 1μA maximum over temperature and the external resistor required to hold V_{BATT} below V_{CC} is:

$$R \le \frac{V_{CC} - 50\text{mV}}{1\mu\text{A}}$$

With V_{CC} = 4.5V, a 4.3MΩ resistor will work. With a 3V battery, this resistor will draw only 0.7μA from the battery, which is negligible in most cases.

Table 1. Input and Output Status in Battery Backup Mode

SIGNAL	STATUS
V_{CC}	C2 monitors V_{CC} for active switchover.
V_{OUT}	V_{OUT} is connected to V_{BATT} through an internal PMOS switch.
V_{BATT}	The supply current is 1μA maximum.
BATT ON	Logic high. The open circuit output voltage is equal to V_{OUT}.
PFI	Power Failure Input is ignored.
$\overline{\text{PFO}}$	Logic low
RESET	Logic low
$\overline{\text{RESET}}$	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{\text{LOW LINE}}$	Logic low
WDI	Watchdog Input is ignored.
WDO	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{\text{CE}}$ IN	Chip Enable Input is ignored.
$\overline{\text{CE}}$ OUT	Logic high. The open circuit output voltage is equal to V_{OUT}.
OSC IN	OSC IN is ignored.
OSC SEL	OSC SEL is ignored.

Table 1 shows the state of each pin during battery backup. When the battery switchover section is not used, connect V_{BATT} to GND and V_{OUT} to V_{CC}.

Memory Protection

The LTC691 and LTC695 include memory protection circuitry which ensures the integrity of the data in memory by preventing write operations when V_{CC} is at invalid level. Two additional pins, $\overline{\text{CE}}$ IN and $\overline{\text{CE}}$ OUT, control the $\overline{\text{Chip Enable}}$ or $\overline{\text{Write}}$ inputs of CMOS RAM. When V_{CC} is +5V, $\overline{\text{CE}}$ OUT follows $\overline{\text{CE}}$ IN with a typical propagation delay of 20ns. When V_{CC} falls below the reset voltage threshold or V_{BATT}, $\overline{\text{CE}}$ OUT is forced high, independent of $\overline{\text{CE}}$ IN. $\overline{\text{CE}}$ OUT is an alternative signal to drive the $\overline{\text{CE}}$, $\overline{\text{CS}}$, or $\overline{\text{Write}}$ input of battery-backed up CMOS RAM. $\overline{\text{CE}}$ OUT can also be used to drive the $\overline{\text{Store}}$ or $\overline{\text{Write}}$ input of an EEPROM, EAROM or NOVRAM to achieve similar protection. Figure 4 shows the timing diagram of $\overline{\text{CE}}$ IN and $\overline{\text{CE}}$ OUT.

$\overline{\text{CE}}$ IN can be derived from the microprocessor's address decoder output. Figure 5 shows a typical nonvolatile CMOS RAM application.

Memory protection can also be achieved with the LTC690 and LTC694 by using $\overline{\text{RESET}}$ as shown in Figure 6.

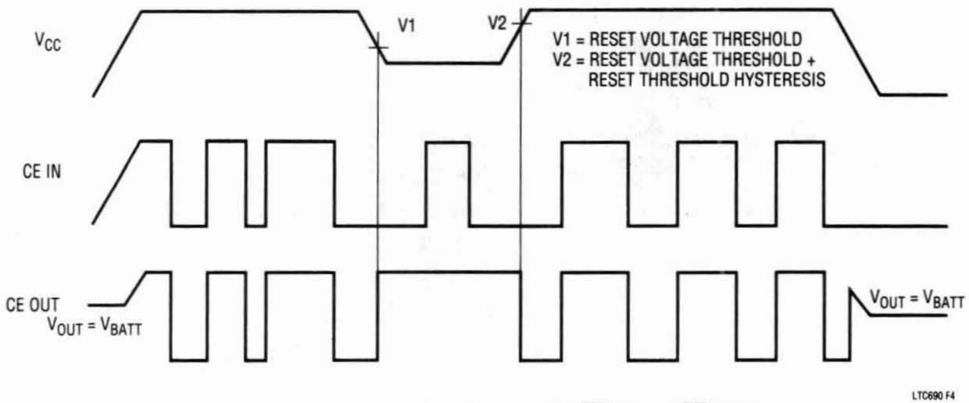


Figure 4. Timing Diagram for $\overline{\text{CE}}$ IN and $\overline{\text{CE}}$ OUT

APPLICATIONS INFORMATION

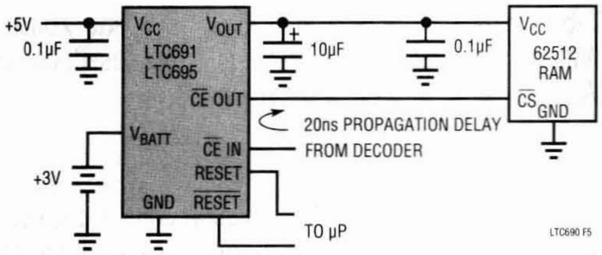

+5V
0.1µF
VCC
VOUT
LTC691
LTC695
CE OUT
VBATT
CE IN
RESET
GND
RESET
+3V
10µF
0.1µF
VCC
62512
RAM
CS
GND
20ns PROPAGATION DELAY
FROM DECODER
TO µP
LTC690 F5

Figure 5. A Typical Nonvolatile CMOS RAM Application

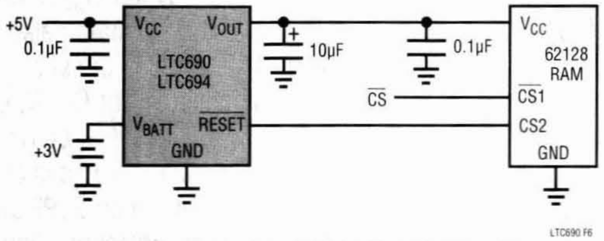

+5V
0.1µF
VCC
VOUT
LTC690
LTC694
VBATT
RESET
GND
+3V
10µF
0.1µF
CS
VCC
62128
RAM
CS1
CS2
GND
LTC690 F6

Figure 6. Write Protect for RAM with LTC690 or LTC694

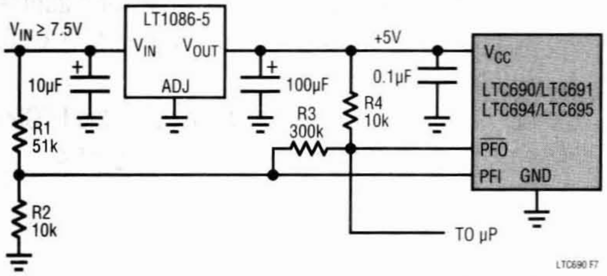

VIN ≥ 7.5V
LT1086-5
VIN
VOUT
ADJ
10µF
R1
51k
R2
10k
100µF
R3
300k
+5V
0.1µF
R4
10k
VCC
LTC690/LTC691
LTC694/LTC695
PFO
PFI
GND
TO µP
LTC690 F7

Figure 7. Monitoring *Unregulated* DC Supply with the LTC690's Power Fail Comparator

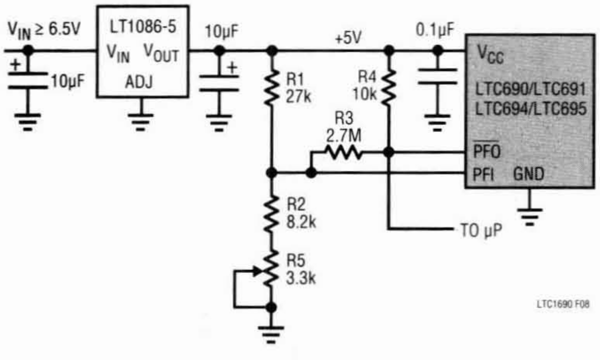

VIN ≥ 6.5V
10µF
LT1086-5
VIN
VOUT
ADJ
10µF
+5V
R1
27k
R4
10k
R3
2.7M
0.1µF
VCC
LTC690/LTC691
LTC694/LTC695
PFO
PFI
GND
R2
8.2k
R5
3.3k
TO µP
LTC1690 F08

Figure 8. Monitoring *Regulated* DC Supply with the LTC690's Power Fail Comparator

Power Fail Warning

The LTC690 family generates a Power Failure Output ($\overline{\text{PFO}}$) for early warning of failure in the microprocessor's power supply. This is accomplished by comparing the Power Failure Input (PFI) with an internal 1.3V reference. $\overline{\text{PFO}}$ goes low when the voltage at PFI pin is less than 1.3V. Typically PFI is driven by an external voltage divider (R1 and R2 in Figures 7 and 8) which senses either an unregulated DC input or a regulated 5V output. The voltage divider ratio can be chosen such that the voltage PFI pin falls below 1.3V several milliseconds before the +5V supply falls below the maximum reset voltage threshold 4.75V. $\overline{\text{PFO}}$ is normally used to interrupt the microprocessor to execute shut-down procedure between $\overline{\text{PFO}}$ and $\overline{\text{RESET}}$ or RESET.

The power fail comparator, C3, does not have hysteresis. Hysteresis can be added however, by connecting a resistor between the $\overline{\text{PFO}}$ output and the noninverting PFI input pin as shown in Figures 7 and 8. The upper and lower trip points in the comparator are established as follows:

When $\overline{\text{PFO}}$ output is low, R3 sinks current from the summing junction at the PFI pin.

$$V_H = 1.3V\left(1 + \frac{R1}{R2} + \frac{R1}{R3}\right)$$

When $\overline{\text{PFO}}$ output is high, the series combination of R3 and R4 source current into the PFI summing junction.

$$V_L = 1.3V\left(1 + \frac{R1}{R2} - \frac{(5V - 1.3V)R1}{1.3V(R3 + R4)}\right)$$

$$\text{Assuming } R4 \ll R3,\ V_{HYSTERESIS} = 5V\frac{R1}{R3}$$

Example 1: The circuit in Figure 7 demonstrates the use of the power fail comparator to monitor the unregulated power supply input. Assuming the the rate of decay of the supply input V_{IN} is 100mV/ms and the total time to execute a shut-down procedure is 8ms. Also the noise of V_{IN} is 200mV. With these assumptions in mind, we can reasonably set V_L = 7.5V which 1.25V greater than the sum of maximum reset voltage threshold and the dropout voltage

APPLICATIONS INFORMATION

of LT1086-5 (4.75V + 1.5V) and $V_{HYSTERESIS}$ = 850mV.

$$V_{HYSTERESIS} = 5V\frac{R1}{R3} = 850V$$

$$R3 \approx 5.88\ R1$$

Choose R3 = 300kΩ and R1 = 51kΩ. Also select R4 = 10kΩ which is much smaller than R3.

$$7.5V = 1.3V\left(1 + \frac{51k\Omega}{R2} - \frac{(5V - 1.3V)51k\Omega}{1.3V(310k\Omega)}\right)$$

R2 = 9.7kΩ, Choose nearest 5% resistor 10k and recalculate V_L,

$$V_L = 1.3V\left(1 + \frac{51k\Omega}{10k\Omega} - \frac{(5V - 1.3V)51k\Omega}{1.3V(310k\Omega)}\right) = 7.32V$$

$$V_H = 1.3V\left(1 + \frac{51k\Omega}{10k\Omega} + \frac{51k\Omega}{300k\Omega}\right) = 8.151V$$

$$\frac{(7.32V - 6.25V)}{100mV/ms} = 10.7ms$$

$$V_{HYSTERESIS} = 8.151V - 7.32V = 831mV$$

The 10.7ms allows enough time to execute shut-down procedure for microprocessor and 831mV of hysteresis would prevent $\overline{\text{PFO}}$ from going low due to the noise of V_{IN}.

Example 2: The circuit in Figure 8 can be used to measure the regulated 5V supply to provide early warning of power failure. Because of variations in the PFI threshold, this circuit requires adjustment to ensure the PFI comparator trips before the reset threshold is reached. Adjust R5 such that the $\overline{\text{PFO}}$ output goes low when the V_{CC} supply reaches the desired level (e.g., 4.85V).

Monitoring the Status of the Battery

C3 can also monitor the status of the memory backup battery (Figure 9). If desired, the $\overline{\text{CE}}$ OUT can be used to apply a test load to the battery. Since $\overline{\text{CE}}$ OUT is forced high in battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

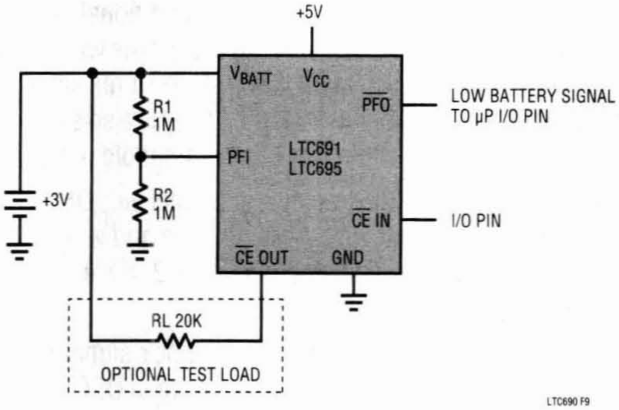


Figure 9. Backup Battery Monitor with Optional Test Load

Watchdog Timer

The LTC690 family provides a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within a seleced time-out period, $\overline{\text{RESET}}$ is forced to active low for a minimum of 35ms for the LTC690/1 (140ms for the LTC694/5). The reset active time is adjustable on the LTC691/5. Since many systems can not service the watchdog timer immediately after a reset, the LTC691 and LTC695 have longer time-out period (1.0 second minimum) right after a reset is issued. The normal time-out period (70ms minimum) becomes effective following the first transition of WDI after $\overline{\text{RESET}}$ is inactive. The watchdog time-out period is fixed at 1.0 second minimum on the LTC690 and LTC694. Figure 10 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as $\overline{\text{RESET}}$ is inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog time is reset and begins to time out again. To ensure the watchdog time does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog time can be deactivated by floating the WDI pin. The timer is also disabled when V_{CC} falls below the reset voltage threshold or V_{BATT}.

APPLICATIONS INFORMATION

The LTC691 and LTC695 provide an additional output (Watchdog Output, $\overline{\text{WDO}}$) which goes low if the watchdog timer is allowed to time out and remains low until set high by the next transition on the WDI pin. $\overline{\text{WDO}}$ is also set high when V_{CC} falls below the reset voltage threshold or V_{BATT}.

The LTC691 and LTC695 have two additonal pins OSC SEL and OSC IN, which allow reset active time and watchdog time-out period to be adjusted per Table 2. Several configurations are shown in Figure 11.

OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND when OSC SEL is forced low. In these configurations, the nominal reset active time and watchdog time-out period are determined by the number of clocks or set by the formula in Table 2. When OSC SEL is high or floating, the internal oscillator is enabled and the reset active time is fixed at 35ms minimum for the LTC691 and 140ms minimum for the LTC695. OSC IN selectes between the 1 second and 70ms minimum normal watchdog time-out periods. In both cases, the time-out period immediately after a reset is at least 1 second.

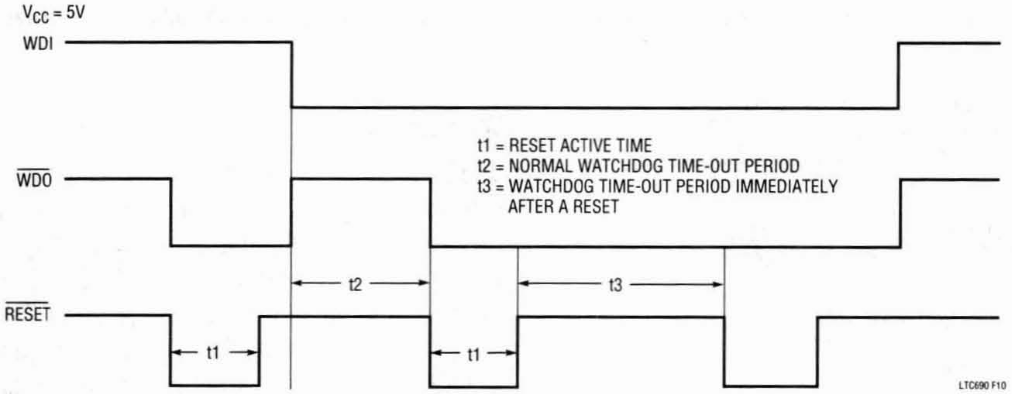


Figure 10. Watchdog Time-out Period and Reset Active Time

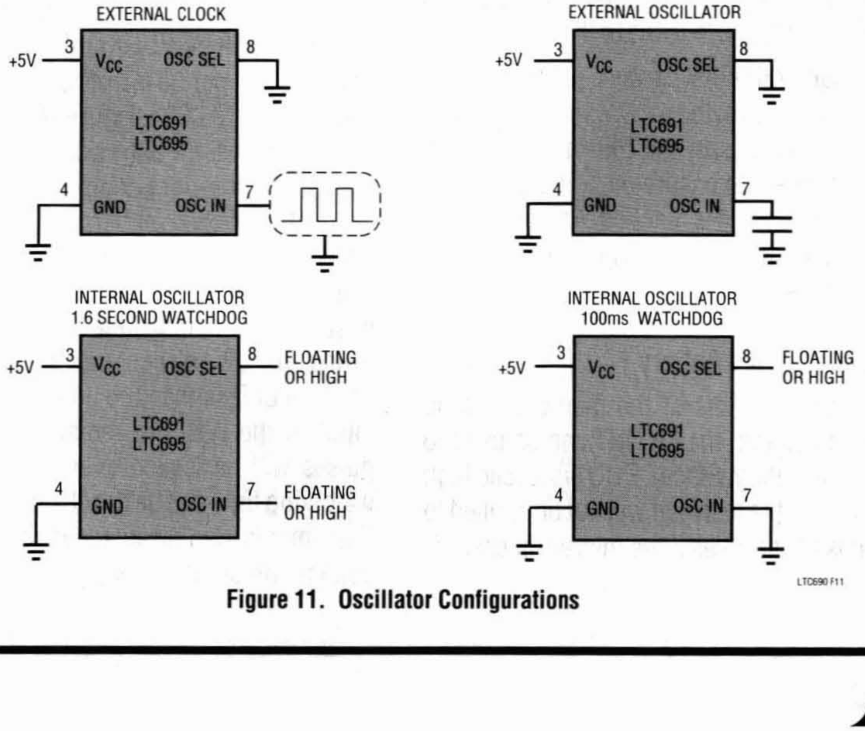

EXTERNAL CLOCK
EXTERNAL OSCILLATOR
INTERNAL OSCILLATOR 1.6 SECOND WATCHDOG
INTERNAL OSCILLATOR 100ms WATCHDOG
+5V
3
V_{CC}
OSC SEL
8
LTC691
LTC695
4
GND
OSC IN
7
FLOATING OR HIGH
LTC690 F11

Figure 11. Oscillator Configurations

APPLICATIONS INFORMATION

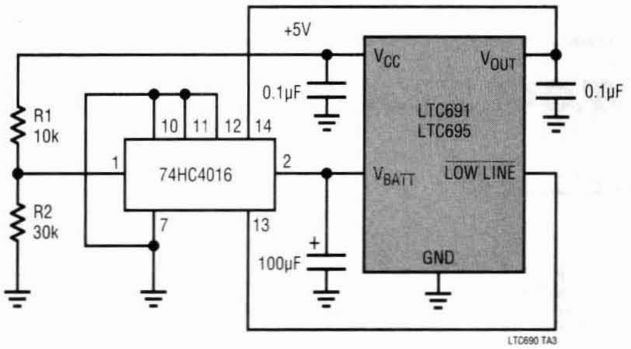
Table 2. LTC691 and LTC695 Reset Active Time and Watchdog Time-out Selections

OSC SEL	OSC IN	WATCHDOG TIME-OUT PERIOD		RESET ACTIVE TIME	
		NORMAL (Short Period)	IMMEDIATELY AFTER RESET (Long Period)	LTC691	LTC695
Low	External Clock Input	1024 clks	4096 clks	512 clks	2048 clks
Low	External Capacitor*	$\frac{400ms}{47pF} \times C$	$\frac{1.6\ sec}{47pF} \times C$	$\frac{200ms}{47pF} \times C$	$\frac{800ms}{47pF} \times C$
Floating or High	Low	100ms	1.6 sec	50ms	200ms
Floating or High	Floating or High	1.6 sec	1.6 sec	50ms	200ms

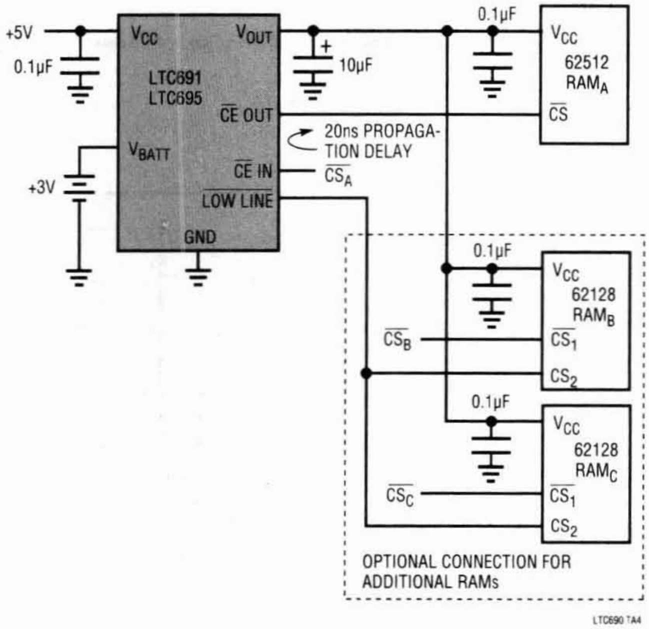
*The nominal internal frequency is 10.24kHz. The nominal oscillator frequency with external capacitor is F_{OSC} (Hz) = $\frac{184,000}{C(pF)}$

TYPICAL APPLICATIONS

Capacitor Backup with 74HC4016 Switch


+5V
R1
10k
R2
30k
74HC4016
1
2
7
10
11
12
13
14
0.1µF
100µF
V_{CC}
V_{OUT}
LTC691
LTC695
V_{BATT}
$\overline{LOW\ LINE}$
GND
0.1µF
LTC690 TA3

Write Protect for Additional RAMs


+5V
0.1µF
+3V
V_{CC}
V_{OUT}
LTC691
LTC695
V_{BATT}
$\overline{CE}$ OUT
$\overline{CE}$ IN
$\overline{LOW\ LINE}$
GND
10µF
0.1µF
V_{CC}
62512
RAM_A
$\overline{CS}$
20ns PROPAGATION DELAY
$\overline{CS_A}$
0.1µF
V_{CC}
62128
RAM_B
$\overline{CS_B}$
$\overline{CS_1}$
CS_2
0.1µF
V_{CC}
62128
RAM_C
$\overline{CS_C}$
$\overline{CS_1}$
CS_2
OPTIONAL CONNECTION FOR ADDITIONAL RAMs
LTC690 TA4

LINEAR TECHNOLOGY

LTC699

Microprocessor Supervisory Circuit

FEATURES

- *Guaranteed* Reset Assertion at V_{CC} = 1V
- 1.5mA Maximum Supply Current
- SO-8 Packaging
- 4.65V Precision Voltage Monitor
- Power OK/Reset Time Delay: 200ms
- Minimum External Component Count
- Performance Specified Over Temperature
- Superior Upgrade for MAX699

APPLICATIONS

- Critical µP Power Monitoring
- Intelligent Instruments
- Computers and Controllers
- Automotive Systems

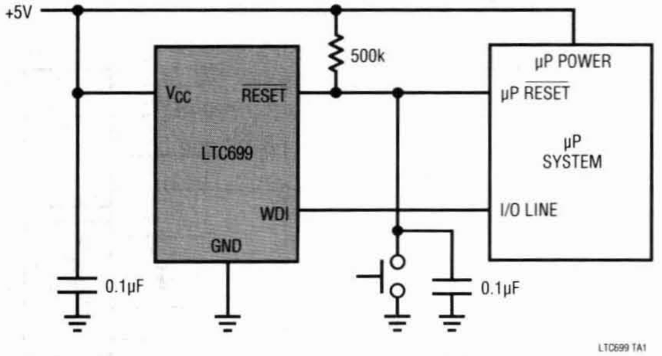
DESCRIPTION

The LTC699 provides power supply monitoring for microprocessor-based systems. The features include microprocessor reset and watchdog timing. Precise internal voltage reference and comparator circuit monitor the power supply line. When an out-of-tolerance condition occurs, the $\overline{\text{RESET}}$ output is forced to active low. In addition, the $\overline{\text{RESET}}$ output is guaranteed to remain logic low even with V_{CC} as low as 1V.

An internal watchdog timer is also available, which forces the $\overline{\text{RESET}}$ output to active low when the watchdog input is not toggled prior to the time-out period of 1.6 seconds.

The LTC699 is offered in DIP and surface mount packages.

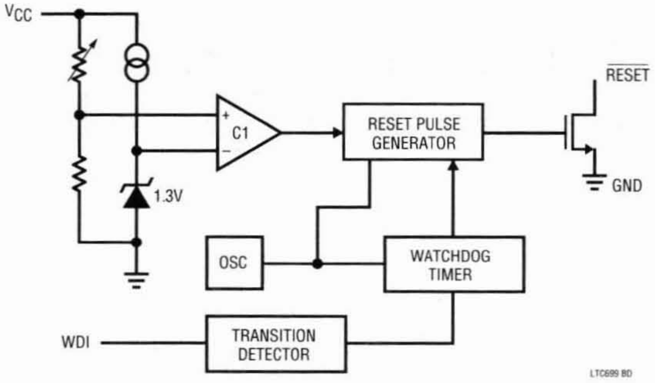
TYPICAL APPLICATION



+5V
500k
V_CC
RESET
LTC699
WDI
GND
0.1µF
µP POWER
µP RESET
µP SYSTEM
I/O LINE
0.1µF
LTC699 TA1

MICROPROCESSOR RESET AND WATCHDOG TIMING IN A SINGLE CHIP FOR MICROPROCESSOR SYSTEMS.

BLOCK DIAGRAM



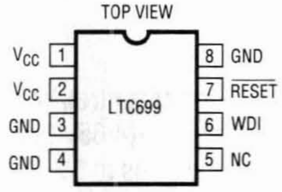
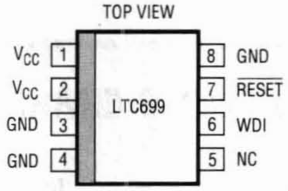
V_CC
+
C1
−
1.3V
RESET PULSE GENERATOR
RESET
GND
OSC
WATCHDOG TIMER
WDI
TRANSITION DETECTOR
LTC699 BD

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Terminal Voltage	
V_{CC}	−0.3V to 6.0V
WDI Input	−0.3V to V_{CC} + 0.3V
$\overline{\text{RESET}}$ Output	−0.3V to 6V
Power Dissipation	500mW
Operating Temperature Range	
LTC699C	0°C to 70°C
LTC699I	−40°C to 85°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW VCC 1 VCC 2 GND 3 GND 4 8 GND 7 RESET 6 WDI 5 NC LTC699 N8 PACKAGE 8-LEAD PLASTIC DIP	LTC699CN8 LTC699IN8
 TOP VIEW VCC 1 VCC 2 GND 3 GND 4 8 GND 7 RESET 6 WDI 5 NC LTC699 S8 PACKAGE 8-LEAD PLASTIC SOIC	LTC699CS8 LTC699IS8 **S8 PART MARKING** 699 699I

ELECTRICAL CHARACTERISTICS

V_{CC} = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
Operating Voltage Range		●	3.0		5.5	V
Supply Current				0.6	1.5	mA
		●		0.6	2.5	
Power Down Reset Assertion		●	4.5	4.65	4.75	V
Power Up Reset De-Assertion		●			4.75	V
Reset Threshold Hysteresis				40		mV
Reset Active Time			160	200	240	ms
		●	140	200	280	
Watchdog Time-out Period			1.2	1.6	2.0	sec
		●	1.0	1.6	2.25	
Reset Active Time PSRR				1		ms/V
Watchdog Time-out Period PSRR				8		ms/V
Minimum WDI Input Pulse Width	V_{IL} = 0.4, V V_{IH} = 3.5V	●	200			ns
$\overline{\text{RESET}}$ output Voltage at V_{CC} = 1V (Note 3)	I_{SINK} = 10μA, V_{CC} = 1V			4	200	mV
$\overline{\text{RESET}}$ output Voltage	I_{SINK} = 1.6mA, V_{CC} = 4.25V				0.4	V
$\overline{\text{RESET}}$ Output Short Circuit Current	Output Sink Current			25		mA
WDI Input Threshold	Logic Low				0.8	V
	Logic High		2.0			
WDI Input Current	WDI = V_{OUT}	●		4	50	μA
	WDI = 0V	●	−50	−8		

The ● denotes specifications which apply over the operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: $\overline{\text{RESET}}$ is active low, open drain output.

PIN FUNCTIONS

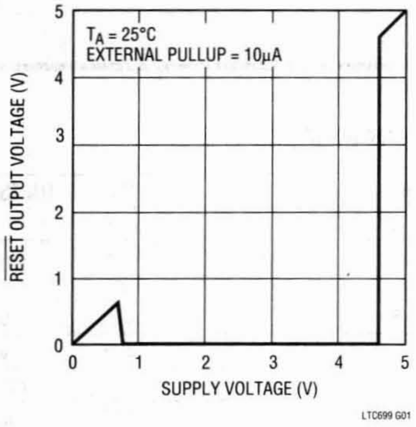
V_{CC}: +5V supply input. The V_{CC} pin should be bypassed with a 0.1µF capacitor.

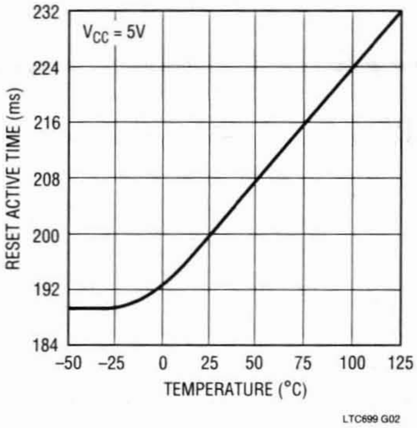
GND: Ground pin.

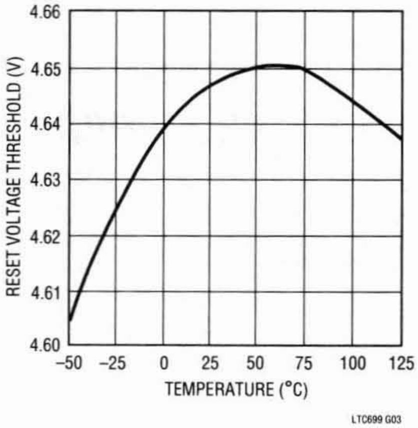
$\overline{\text{RESET}}$: Open drain output for µP reset control. When V_{CC} falls below the reset voltage threshold (4.65V typically), $\overline{\text{RESET}}$ goes active low. After V_{CC} returns to 5V, the reset pulse generator forces $\overline{\text{RESET}}$ to remain active low for a minimum of 140ms . When the watchdog timer is enabled but not serviced prior to the time-out period, the reset pulse generator also forces $\overline{\text{RESET}}$ to active low for a minimum of 140ms for every time-out period (see Figure 2).

WDI: Watchdog Input, WDI, is a three level input. Driving WDI either high or low for longer than the watchdog time-out period forces $\overline{\text{RESET}}$ low. Floating WDI disables the Watchdog Timer. The timer resets itself with each transition of the Watchdog Input (see Figure 2).

TYPICAL PERFORMANCE CHARACTERISTICS


$\overline{\text{RESET}}$ Output Voltage vs Supply Voltage


Reset Active Time vs Temperature


Reset Voltage Threshold vs Temperature

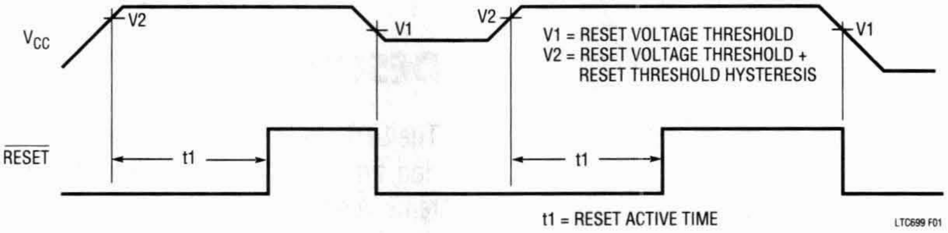
APPLICATIONS INFORMATION

Microprocessor Reset

The LTC699 uses a bandgap voltage reference and a precision voltage comparator C1 to monitor the 5V supply input V_{CC} (see BLOCK DIAGRAM). When V_{CC} falls below the reset voltage threshold, the $\overline{\text{RESET}}$ output is forced to active low state. The reset voltage threshold accounts for a 5% variation on V_{CC}, so the $\overline{\text{RESET}}$ output becomes active low when V_{CC} falls below 4.65V typical. On power-up, the $\overline{\text{RESET}}$ signal is held active low for a minimum of 140ms after reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RESET}}$ signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the $\overline{\text{RESET}}$ signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at V_{CC} pin do not activate the $\overline{\text{RESET}}$ output. Response time is typically 10µs. To help prevent mistriggering due to transient loads, V_{CC} pin should be bypassed with a 0.1µF capacitor with the leads trimmed as short as possible.

APPLICATIONS INFORMATION



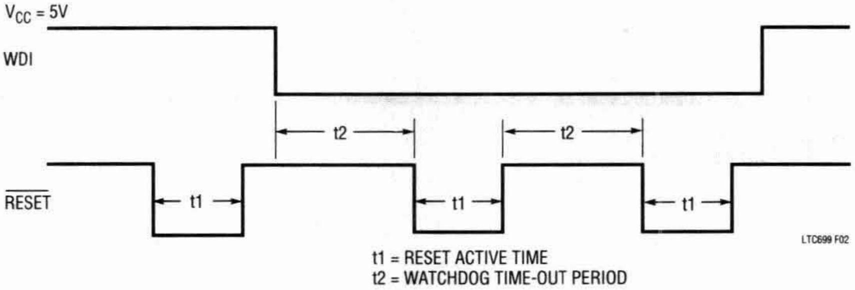
V1 = RESET VOLTAGE THRESHOLD
V2 = RESET VOLTAGE THRESHOLD + RESET THRESHOLD HYSTERESIS

t1 = RESET ACTIVE TIME

Figure 1. Reset Active Time

Watchdog Timer

The LTC699 provides a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the time-out period, $\overline{\text{RESET}}$ is forced to active low for a minimum of 140ms. The watchdog time-out period is fixed at a 1.0 second minimum on the LTC699, which is adequate time for most systems to service the watchdog timer immediately after a reset. Figure 2 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as $\overline{\text{RESET}}$ is inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog time is reset and begins to time out again. To ensure the watchdog time does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog time can be deactivated by floating the WDI pin. The timer is also disabled when V_{CC} falls below the reset voltage threshold.



t1 = RESET ACTIVE TIME
t2 = WATCHDOG TIME-OUT PERIOD

Figure 2. Watchdog Time-Out Period and Reset Active Time

LTC1232

Microprocessor Supervisory Circuit

FEATURES

- *Guaranteed* Reset Assertion at V_{CC} = 1V
- 8-Pin SOIC Plastic Package
- 2.0mA Maximum Supply Current
- 4.62V/4.37V Precision Voltage Monitor
- Power OK/Reset Time Delay: 600ms
- Minimum External Component Count
- Superior Upgrade for DS1232

APPLICATIONS

- Critical µP Power Monitoring
- Intelligent Instruments
- Computers and Controllers
- Automotive Systems

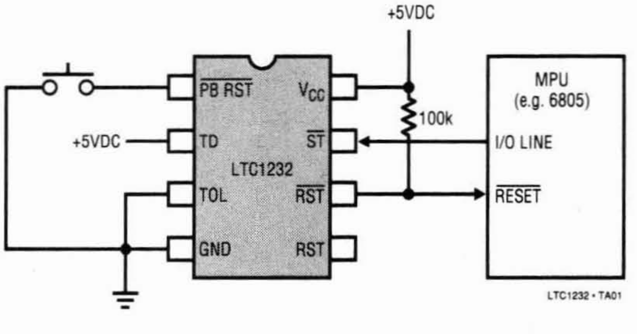
DESCRIPTION

The LTC1232 provides power supply monitoring, watchdog timing and external reset for microprocessor systems. A precise internal voltage reference and comparator circuit monitor the power supply line. When an out-of-tolerance condition occurs, the reset outputs are forced to active states. The $\overline{\text{RST}}$ output is guaranteed to remain logic low even with V_{CC} as low as 1V.

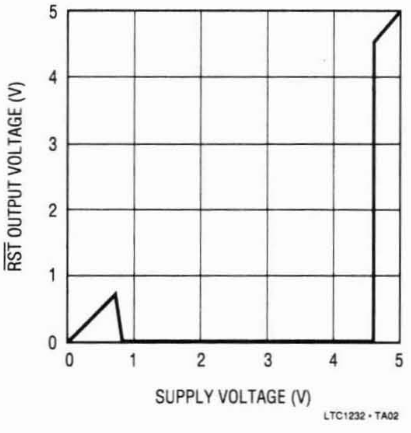
The LTC1232 has an internal watchdog timer which forces the reset outputs to active states when the $\overline{\text{Strobe}}$ input is not forced low prior to a preset time-out period. The watchdog timing can be set to operate on time-out periods of typically 150ms, 600ms or 1.2 seconds.

The LTC1232 performs push-button reset control. The LTC1232 debounces the push-button input and guarantees an active reset pulse width of 250ms minimum.

TYPICAL APPLICATION


+5VDC
$\overline{\text{PB RST}}$
V_{CC}
+5VDC
TD
$\overline{\text{ST}}$
LTC1232
TOL
$\overline{\text{RST}}$
GND
RST
100k
MPU
(e.g. 6805)
I/O LINE
$\overline{\text{RESET}}$
LTC1232 • TA01

$\overline{\text{RST}}$ Ouput Voltage vs Supply Voltage



ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Terminal Voltage
- V_{CC} .... −0.3V to 7.0V
- $\overline{ST}$ and $\overline{RST}$ .... −0.3V to 7.0V
- All Other Inputs and Outputs ..... −0.3V to V_{CC} + 0.3V

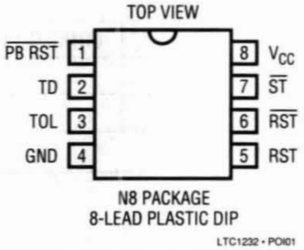
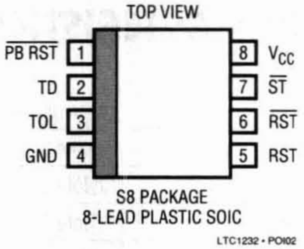
Power Dissipation 500mW

Operating Temperature Range
- LTC1232C .... 0°C to 70°C
- LTC1232I .... −40°C to 85°C

Storage Temperature Range .... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW $\overline{PB\ RST}$ 1 TD 2 TOL 3 GND 4 8 V_{CC} 7 $\overline{ST}$ 6 $\overline{RST}$ 5 RST N8 PACKAGE 8-LEAD PLASTIC DIP LTC1232 • POI01	LTC1232CN8 LTC1232IN8
 TOP VIEW $\overline{PB\ RST}$ 1 TD 2 TOL 3 GND 4 8 V_{CC} 7 $\overline{ST}$ 6 $\overline{RST}$ 5 RST S8 PACKAGE 8-LEAD PLASTIC SOIC LTC1232 • POI02	LTC1232CS8 LTC1232IS8 S8 PART MARKING 1232 1232I

PRODUCT SELECTION GUIDE

	Pins	Reset	Watchdog Timer	Battery Backup	Power Fail Warning	RAM Write Protect	Push-Button Reset	Conditional Battery Backup
LTC1232	**8**	**X**	**X**				**X**	
LTC690	8	X	X	X	X			
LTC691	16	X	X	X	X	X		
LTC694	8	X	X	X	X			
LTC695	16	X	X	X	X	X		
LTC699	8	X	X					
LTC1235	16	X	X	X	X	X	X	X

RECOMMENDED OPERATING CONDITIONS V_{CC} = Full Operating Range

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	4.5	5.0	5.5	V
V_{IH}	$\overline{\text{ST}}$ and $\overline{\text{PB RST}}$ Input High Level		●	2.0		V_{CC}+0.3	V
V_{IL}	$\overline{\text{ST}}$ and $\overline{\text{PB RST}}$ Input Low Level		●	−0.3		0.8	V

DC ELECTRICAL CHARACTERISTICS V_{CC} = Full Operating Range

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Input Leakage	(Note 3)	●	−1.0		1.0	µA
I_{OH}	Output Current at 2.4V	(Note 5)	●	−1.0	−13.0		mA
I_{OL}	Output Current at 0.4V	(Note 5)	●	2.0	6.0		mA
I_{CC}	Supply Current	(Note 4)	●		0.5	2.0	mA
V_{CCTP}	V_{CC} Trip Point	TOL = GND	●	4.50	4.62	4.74	V
V_{CCTP}	V_{CC} Trip Point	TOL = V_{CC}	●	4.25	4.37	4.49	V
V_{HYS}	V_{CC} Trip Point Hysteresis				40		mV
$V_{\overline{RST}}$	$\overline{\text{RST}}$ Output Voltage at V_{CC} = 1V	I_{SINK} = 10µA			4	200	mV

AC CHARACTERISTICS V_{CC} = Full Operating Range

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PB}	$\overline{\text{PB RST}}$ = V_{IL}		●	40			ms
t_{RST}	RESET Active Time		●	250	610	1000	ms
t_{ST}	$\overline{\text{ST}}$ Pulse Width		●	20			ns
t_{RPD}	V_{CC} Detect to RST and $\overline{\text{RST}}$		●			100	ns
t_F	V_{CC} Slew Rate 4.75V-4.25V		●	300			µs
t_{RPU}	V_{CC} Detect to RST and $\overline{\text{RST}}$ (Reset Active Time)	t_R = 5µs	●	250	610	1000	ms
t_R	V_{CC} Slew Rate 4.25V-4.75V		●	0			ns
t_{TD}	$\overline{\text{ST}}$ Pin Detect to RST and $\overline{\text{RST}}$ (Watchdog Time-Out Period)	TD = GND TD = Floating TD = V_{CC}	● ● ●	60 250 500	150 610 1200	250 1000 2000	ms ms ms
C_{IN}	Input Capacitance				5		pF
C_{OUT}	Output Capacitance				5		pF

The ● indicates specifications which apply over the full operating temperature.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

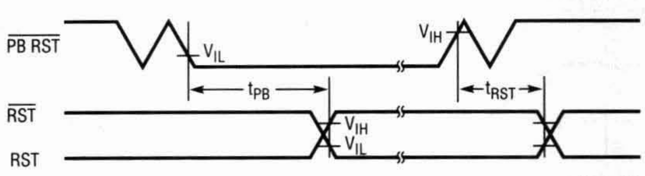
Note 3: The $\overline{\text{PB RST}}$ pin is internally pulled up to V_{CC} with an internal impedance of 10k typical. The TD pin has internal bias current.

Note 4: Measured with outputs open.

Note 5: The $\overline{\text{RST}}$ pin is an open drain output.

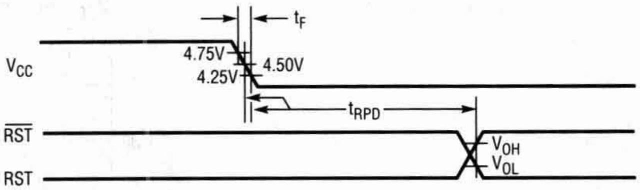
TIMING DIAGRAMS

Push-Button Reset


$\overline{PB\ RST}$
V_{IL}
V_{IH}
t_{PB}
t_{RST}
$\overline{RST}$
V_{IH}
V_{IL}
RST

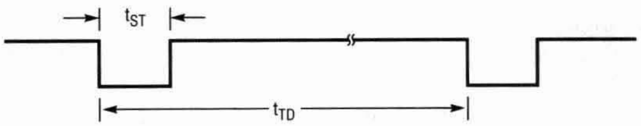
LTC1232 • TD01

Power Down


t_F
V_{CC}
4.75V
4.50V
4.25V
t_{RPD}
$\overline{RST}$
V_{OH}
V_{OL}
RST

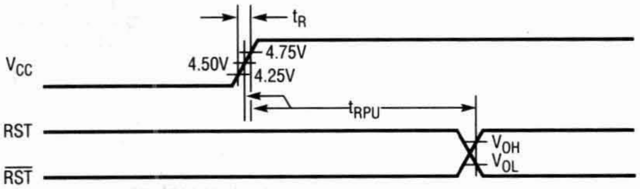
LTC1232 • TD03

Strobe Input



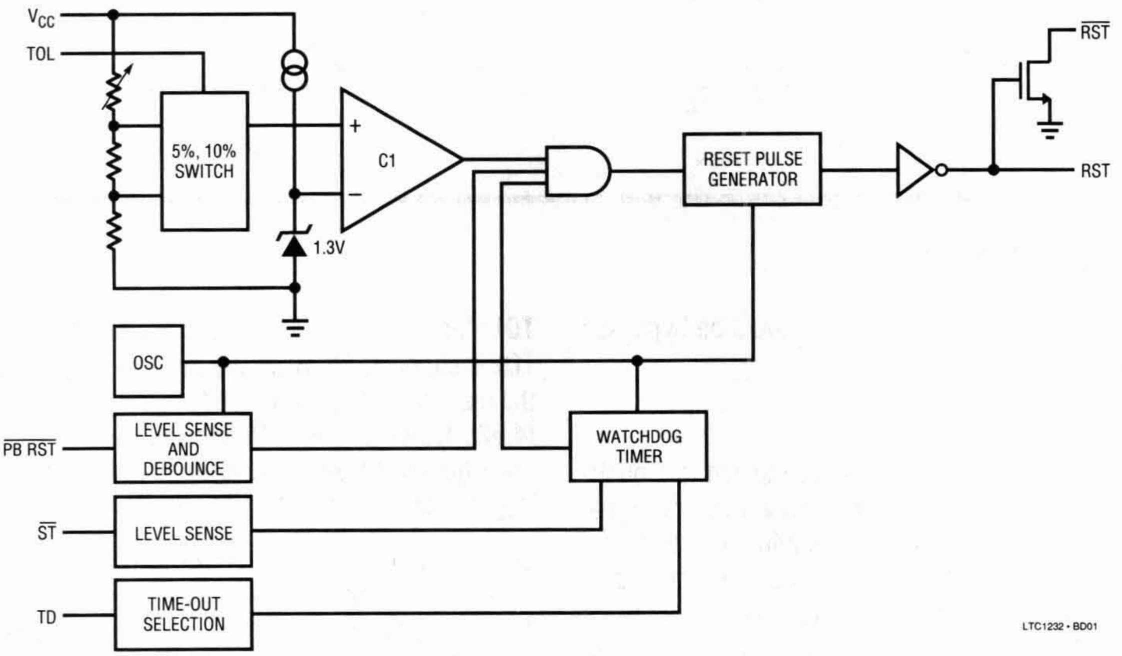
LTC1232 • TD02

Power Up


t_R
V_{CC}
4.50V
4.75V
4.25V
t_{RPU}
RST
V_{OH}
V_{OL}
$\overline{RST}$

LTC1232 • TD04

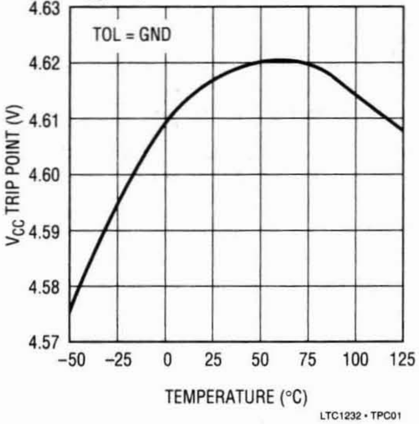
BLOCK DIAGRAM


V_{CC}
TOL
5%, 10% SWITCH
+
C1
–
1.3V
RESET PULSE GENERATOR
$\overline{RST}$
RST
OSC
$\overline{PB\ RST}$
LEVEL SENSE AND DEBOUNCE
WATCHDOG TIMER
$\overline{ST}$
LEVEL SENSE
TD
TIME-OUT SELECTION

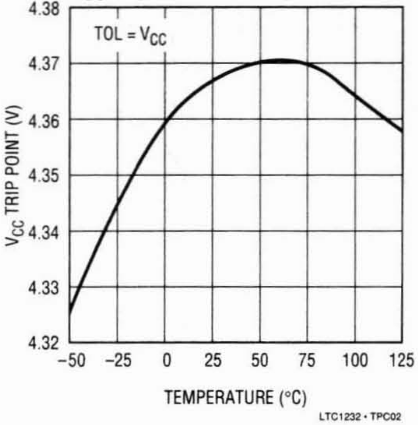
LTC1232 • BD01

TYPICAL PERFORMANCE CHARACTERISTICS

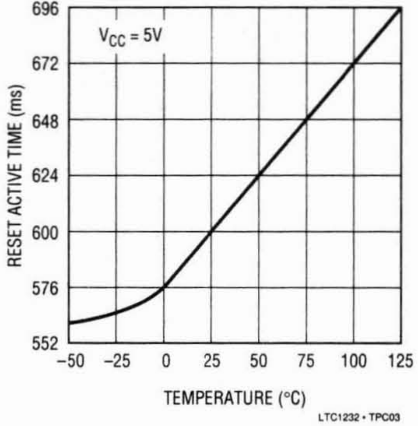
V_{CC} Trip Point vs Temperature



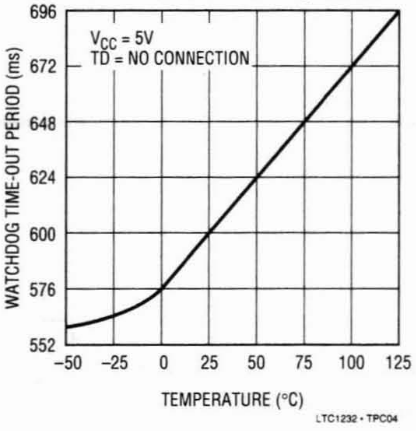
V_{CC} Trip Point vs Temperature



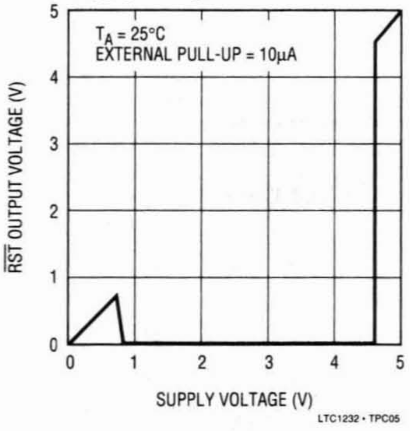
Reset Active Time vs Temperature



Time-Out Period vs Temperature



$\overline{\text{RST}}$ Output Voltage vs Supply Voltage



PIN FUNCTIONS

V_{CC}: +5V supply input. The V_{CC} pin should be bypassed with a 0.1µF capacitor.

GND: Ground pin.

$\overline{\text{PB RST}}$: Logic input to be directly connected to a push-button. The $\overline{\text{PB RST}}$ input requires an active low signal which is debounced and timed for a minimum of 40ms. When this condition is satisfied, the reset pulse generator forces the reset outputs to active states. The reset outputs remain in active states for a minimum of 250ms after $\overline{\text{PB RST}}$ is released from logic low level.

TOL: Input to select 5% or 10% variation on V_{CC}. When TOL is connected to GND, the reset pulse generator forces the reset outputs to active states as V_{CC} falls below 4.75V (4.62V typical). When TOL is connected to V_{CC}, the reset pulse generator forces the reset outputs to active states as V_{CC} falls below 4.5V (4.37V typical).

TD: Time-out Delay, TD is a three level input to select three different time-out periods. The time-out period is set by the TD input to be 150ms with TD connected to GND, 600ms with TD left floating, and 1.2 seconds with TD connected to V_{CC}.

PIN FUNCTIONS

$\overline{\text{RST}}$: Open drain logic output for µP reset control. The LTC1232 provides three ways to generate µP reset. First, when V_{CC} falls below V_{CC} trip point (4.75V with TOL = GND and 4.5V with TOL = V_{CC}), $\overline{\text{RST}}$ goes active low. After V_{CC} returns to 5V, the reset pulse generator forces $\overline{\text{RST}}$ to remain active low for a minimum of 250ms. Second, when the watchdog timer is not serviced prior to a selected time-out period, the reset pulse generator also forces $\overline{\text{RST}}$ to active low for a minimum of 250ms and repeats for every time-out period. Third and the last, when the $\overline{\text{PB RST}}$ pin stays active low for a minimum of 40ms, $\overline{\text{RST}}$ becomes active low. The $\overline{\text{RST}}$ output will remain active low for a minimum of 250ms from the moment the push-button reset input is released from logic low level.

RST: RST is an active high logic output. It is the inverse of $\overline{\text{RST}}$.

$\overline{\text{ST}}$: Logic input to reset the watchdog timer. Driving $\overline{\text{ST}}$ either high or low longer than the time-out period set by the TD input, forces the reset outputs to active states for a minimum of 250ms. The timer resets itself and begins to time-out again with each high to low transition on the $\overline{\text{ST}}$ input (see Figure 2).

APPLICATIONS INFORMATION

Power Monitoring

The LTC1232 uses a bandgap voltage reference and a precision voltage comparator, C1, to monitor the 5V supply input on V_{CC} (see BLOCK DIAGRAM). When V_{CC} falls below the V_{CC} trip point (4.62V typical with TOL = GND and 4.37V typical with TOL = V_{CC}), the reset outputs are forced to active states. The V_{CC} trip point accounts for a 5% or 10% variation on V_{CC}, so the reset outputs become active when V_{CC} falls below the V_{CC} trip point. On power-up, the reset signals are held in active states for a minimum of 250ms after the V_{CC} trip point is reached to allow the power supply and microprocessor to stabilize. On power-down, the $\overline{\text{RST}}$ signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the $\overline{\text{RST}}$ signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at V_{CC} pin do not activate the reset outputs. Response time is typically 10µs. To help prevent mitriggering due to transient loads, V_{CC} pin should be bypassed with a 0.1µF capacitor with the leads trimmed as short as possible.

Push-Button Reset

The LTC1232 provides a logic input pin, $\overline{\text{PB RST}}$, for direct connection to a push-button. This push-button reset input requires an active low signal. Internally, this input signal is debounced and timed for a minimum of 40ms. When

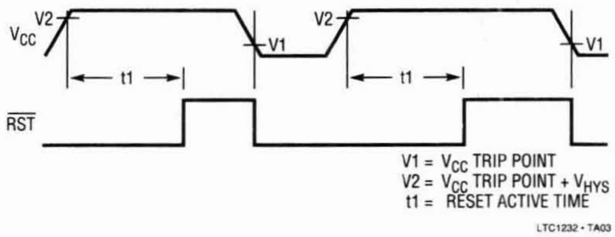


Figure 1. Reset Active Time

APPLICATIONS INFORMATION

this condition is satisfied, the reset pulse generator forces the reset outputs to active states. The reset signals will remain active for a minimum of 250ms from the moment the push-button reset input is released from logic low level (see TIMING DIAGRAM).

Watchdog Timer

The LTC1232 provides a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not stimulate the strobe input, $\overline{ST}$, within a selected time-out period, the reset outputs are forced to active states for a minimum of 250ms. The time-out period is selected by the Time-out Delay input, TD, to be 150ms with TD connected to GND, 600ms with TD left floating, and 1.2 seconds with TD connected to V_{CC}. The 1.2 second time-out period is adequate for many systems to serve the watchdog timer immediately after a reset. Figure 2 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as the reset outputs are inactive. When a high-to-low transition occurs at the $\overline{ST}$ pin prior to time-out, the watchdog time is reset and begins to time-out again. To ensure the watchdog time does not time-out, a high-to-low transition on the $\overline{ST}$ pin must occur at or less than the minimum time-out period. If the input to the $\overline{ST}$ pin remains either high or low, reset pulses will be issued for every time-out period selected by the TD pin. The watchdog timer is disabled when V_{CC} falls below the V_{CC} trip point.

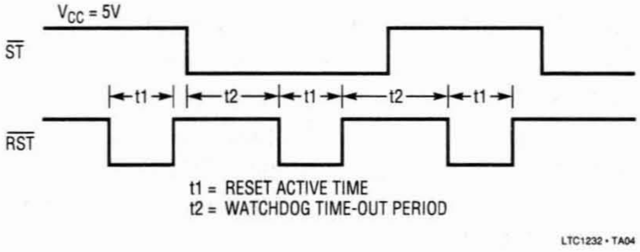


Figure 2. Watchdog Time-Out Period and Reset Active Time

LTC1235

Microprocessor Supervisory Circuit

FEATURES

- *Guaranteed* Reset Assertion at V_{CC} = 1V
- 1.5mA Maximum Supply Current
- Fast (35ns Max.) Onboard Gating of RAM Chip Enable Signals
- Conditional Battery Backup Extends Battery Life
- 4.65V Precision Voltage Monitor
- Power OK/Reset Time Delay: 200ms
- External Reset Control
- Minimum External Component Count
- 1μA Maximum Standby Current
- Voltage Monitor for Power Fail or Low Battery Warning
- Thermal Limiting
- Performance Specified Over Temperature
- All the LTC695 Features Plus Conditional Battery Backup and External Reset Control

APPLICATIONS

- Critical μP Power Monitoring
- Intelligent Instruments
- Battery-Powered Computers and Controllers
- Automotive Systems

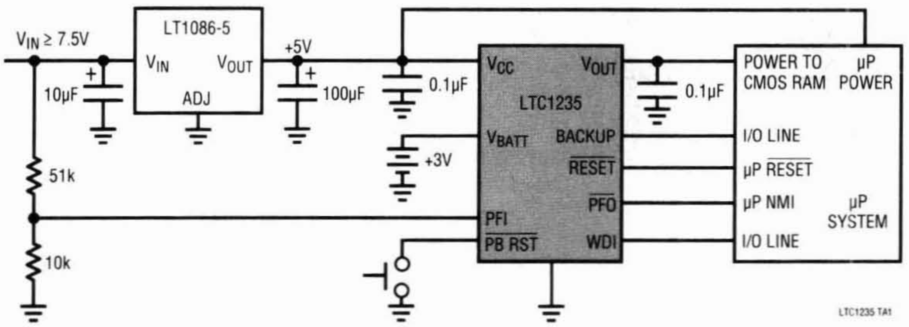
DESCRIPTION

The LTC1235 provides complete power supply monitoring and battery control functions for microprocessor reset, battery backup, RAM write protection, power failure warning and watchdog timing. The LTC1235 has all the LTC695 features plus conditional battery backup and external reset control. When an out-of-tolerance power supply condition occurs, the reset outputs are forced to active states and the Chip Enable output write-protects external memory. The $\overline{\text{RESET}}$ output is guaranteed to remain logic low with V_{CC} as low as 1V. External reset control is provided by a debounced push-button reset input.

The LTC1235 powers the active CMOS RAMs with a charge pumped NMOS power switch to achieve low dropout and low supply current. When primary power is lost, auxiliary power, connected to the battery input pin, provides backup power to the RAMs. The LTC1235 can be programmed by a μP signal to either back up the RAMs or not. This extends the battery life in situations where RAM data need not always be saved when power goes down.

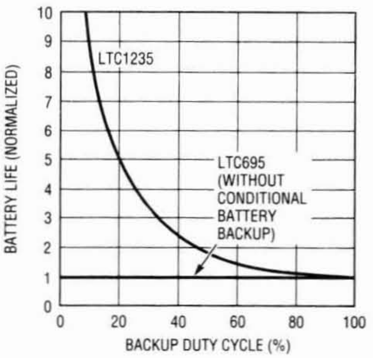
For an early warning of impending power failure, the LTC1235 provides an internal comparator with a user-defined threshold. An internal watchdog timer is also available, which forces the reset pins to active states when the watchdog input is not toggled prior to the time-out period.

TYPICAL APPLICATION



THE LTC1235 EXTENDS BATTERY LIFE BY PROVIDING BATTERY POWER ONLY WHEN REQUIRED TO BACK UP RAM DATA.
IT SAVES THE BATTERY WHEN NO DATA BACKUP IS NEEDED. THE μP REQUESTS BACKUP WITH THE BACKUP PIN.

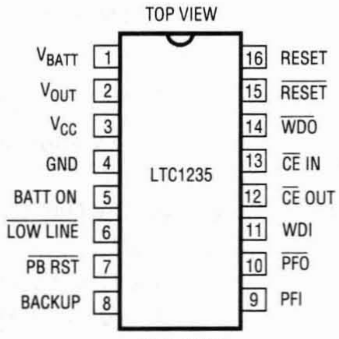
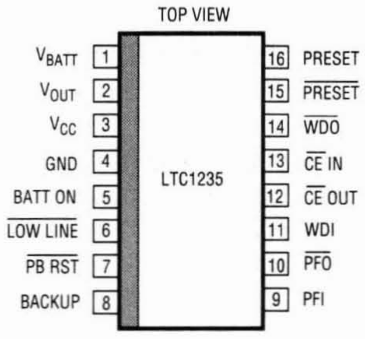
Battery Life vs Backup Duty Cycle



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Terminal Voltage	
V_{CC}	−0.3V to 6.0V
V_{BATT}	−0.3V to 6.0V
All Other Inputs	−0.3V to (V_{CC} + 0.3V)
Input Current	
V_{CC}	200mA
V_{BATT}	50mA
V_{OUT} Output Current	Short Circuit Protected
Power Dissipation	500mW
Operating Temperature Range	
LTC1235C	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION (Note 3)

	ORDER PART NUMBER		ORDER PART NUMBER
 TOP VIEW V_{BATT} 1 V_{OUT} 2 V_{CC} 3 GND 4 BATT ON 5 $\overline{LOW\ LINE}$ 6 $\overline{PB\ RST}$ 7 BACKUP 8 LTC1235 16 RESET 15 $\overline{RESET}$ 14 $\overline{WDO}$ 13 $\overline{CE}$ IN 12 $\overline{CE}$ OUT 11 WDI 10 $\overline{PFO}$ 9 PFI N PACKAGE 16-LEAD PLASTIC DIP	LTC1235CN	 TOP VIEW V_{BATT} 1 V_{OUT} 2 V_{CC} 3 GND 4 BATT ON 5 $\overline{LOW\ LINE}$ 6 $\overline{PB\ RST}$ 7 BACKUP 8 LTC1235 16 PRESET 15 $\overline{PRESET}$ 14 $\overline{WDO}$ 13 $\overline{CE}$ IN 12 $\overline{CE}$ OUT 11 WDI 10 $\overline{PFO}$ 9 PFI S PACKAGE 16-LEAD PLASTIC SOL	LTC1235CS

PRODUCT SELECTION GUIDE

	PINS	RESET	WATCHDOG TIMER	BATTERY BACKUP	POWER FAIL WARNING	RAM WRITE PROTECT	PUSH-BUTTON RESET	CONDITIONAL BATTERY BACKUP
LTC1235	**16**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
LTC690	8	X	X	X	X			
LTC691	16	X	X	X	X	X		
LTC694	8	X	X	X	X			
LTC695	16	X	X	X	X	X		
LTC699	8	X	X					
LTC1232	8	X	X				X	

ELECTRICAL CHARACTERISTICS

V_{CC} = Full Operating Range, V_{BATT} = 2.8V, Backup = No Connection, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
Battery Backup Switching						
Operating Voltage Range						
V_{CC}			4.75		5.50	V
V_{BATT}			2.00		4.25	
V_{OUT} Output Voltage	I_{OUT} = 1mA		V_{CC} − 0.05	V_{CC} − 0.005		V
		●	V_{CC} − 0.1	V_{CC} − 0.005		
	I_{OUT} = 50mA		V_{CC} − 0.5	V_{CC} − 0.25		
BACKUP Input Threshold	V_{CC} > Reset Voltage Threshold					
	Logic Low				0.8	V
	Logic High		2.0			
BACKUP Pullup Current (Note 4)				3		µA
V_{OUT} in Battery Backup Mode (Note 5)	I_{OUT} = 250µA, V_{CC} < V_{BATT}		V_{BATT} − 0.1	V_{BATT} − 0.02		V
V_{OUT} in Battery Saving Mode (Note 5)	V_{CC} < V_{BATT} 1MΩ Pulldown on V_{OUT}			0		V
V_{CC} Supply Current (excluding I_{OUT})	I_{OUT} ≤ 50mA			0.6	1.5	mA
		●		0.6	2.5	
Battery Supply Current in Battery Backup Mode and Battery Saving Mode (Note 5)	V_{CC} = 0V, V_{BATT} = 2.8V			0.04	1	µA
		●		0.04	5	
Battery Standby Current (+ = Discharge, − = Charge)	5.5 > V_{CC} > V_{BATT} + 0.2V		−0.1		+0.02	µA
		●	−1.0		+0.10	
Battery Switchover Threshold	Power Up			70		mV
V_{CC} − V_{BATT}	Power Down			50		
Battery Switchover Hysteresis				20		mV
BATT ON Output Voltage (Note 6)	I_{SINK} = 3.2mA				0.4	V
BATT ON Output Short Circuit Current (Note 6)	BATT ON = V_{OUT} Sink Current			35		mA
	BATT ON = 0V Source Current		0.5	1	25	µA
Push-Button Reset						
$\overline{\text{PB RST}}$ Input Threshold	Logic Low				0.8	V
	Logic High		2.0			
$\overline{\text{PB RST}}$ Input Low Time (Notes 4, 7)		●	40			ms
Reset and Watchdog Timer						
Reset Voltage Threshold		●	4.5	4.65	4.75	V
Reset Threshold Hysteresis				40		mV
Reset Active Time	V_{CC} = 5V		160	200	240	ms
		●	140	200	280	
Watchdog Time-out Period	V_{CC} = 5V		1.2	1.6	2.00	sec
		●	1.0	1.6	2.25	
Reset Active Time PSRR				1		ms/V
Watchdog Time-out Period PSRR				8		ms/V
Minimum WDI Input Pulse Width	V_{IL} = 0.4V, V_{IH} = 3.5V	●	200			ns
$\overline{\text{RESET}}$ Output Voltage At V_{CC} = 1V	I_{SINK} = 10µA, V_{CC} = 1V			4	200	mV
$\overline{\text{RESET}}$ and $\overline{\text{LOW LINE}}$ Output Voltage (Note 6)	I_{SINK} = 1.6mA, V_{CC} = 4.25V				0.4	V
	I_{SOURCE} = 1µA, V_{CC} = 5V		3.5			

ELECTRICAL CHARACTERISTICS

V_{CC} = Full Operating Range, V_{BATT} = 2.8V, Backup = No Connection, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITONS		MIN	TYP	MAX	UNITS
RESET and $\overline{\text{WDO}}$ Output Voltage (Note 6)	I_{SINK} = 1.6mA, V_{CC} = 5V I_{SOURCE} = 1μA, V_{CC} = 4.25V		 3.5		0.4	V
RESET, $\overline{\text{RESET}}$, $\overline{\text{WDO}}$, $\overline{\text{LOW LINE}}$ Output Short Circuit Current (Note 6)	Output Source Current Output Sink Current		1	3 25	25	μA mA
WDI Input Threshold	Logic Low Logic High		 2.0		0.8	V
WDI Input Current	WDI = V_{OUT} WDI = 0V	● ●	 –50	4 –8	50	μA
Power Fail Detector						
PFI Input Threshold	V_{CC} = 5V	●	1.25	1.3	1.35	V
PFI Input Threshold PSRR				0.3		mV/V
PFI Input Current				±0.01	±25	nA
$\overline{\text{PFO}}$ Output Voltage (Note 6)	I_{SINK} = 3.2mA I_{SOURCE} = 1μA		 3.5		0.4	V
$\overline{\text{PFO}}$ Short Circuit Source Current (Note 6)	PFI = HIGH, $\overline{\text{PFO}}$ = 0V PFI = LOW, $\overline{\text{PFO}}$ = V_{OUT}		1	3 30	25	μA mA
PFI Comparator Response Time (falling)	ΔV_{IN} = –20mV, V_{OD} = 15mV			2		μs
PFI Comparator Response Time (rising) (Note 6)	ΔV_{IN} = 20mV, V_{OD} = 15mV with 10kΩ Pullup			40 8		μs
Chip Enable Gating						
$\overline{\text{CE}}$ IN Threshold	V_{IL} V_{IH}		 2.0		0.8	V
$\overline{\text{CE}}$ IN Pullup Current (Note 4)				3		μA
$\overline{\text{CE}}$ OUT Output Voltage	I_{SINK} = 3.2mA I_{SOURCE} = 3.0mA I_{SOURCE} = 1μA, V_{CC} = 0V		 V_{OUT} – 1.50 V_{OUT} – 0.05		0.4	V
$\overline{\text{CE}}$ Propagation Delay	V_{CC} = 5V, C_L = 20pF	 ●		20 20	35 45	ns
$\overline{\text{CE}}$ OUT Output Short Circuit Current	Output Source Current Output Sink Current			30 35		mA

The ● denotes specifications which apply over the operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: For military temperature range parts, consult the factory.

Note 4: The input pins of $\overline{\text{PB RST}}$, BACKUP and $\overline{\text{CE}}$ IN, have weak internal pullups which pull to the supply when the input pins are floating.

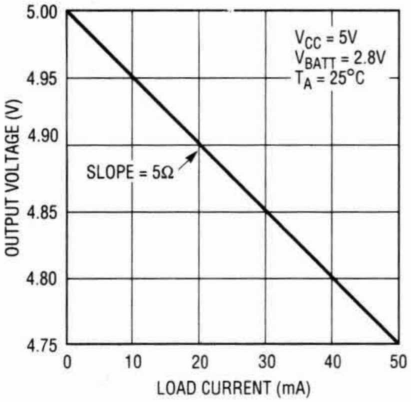
Note 5: The LTC1235 can be programmed either to provide or not to provide battery backup power to the V_{OUT} pin during power failure. The power down condition of V_{OUT} is selected by the logic level of the BACKUP pin which is latched internally when V_{CC} falls through the reset voltage threshold. If the latched logic level of the BACKUP pin is high, V_{OUT} will be in Battery Backup Mode and will be switched to V_{BATT} when V_{CC} falls below V_{BATT}. If the latched logic level of the BACKUP pin is low, V_{OUT} will be in Battery Saving Mode when V_{CC} falls below V_{BATT}.

Note 6: The output pins of BATT ON, $\overline{\text{LOW LINE}}$, $\overline{\text{PFO}}$, $\overline{\text{WDO}}$, $\overline{\text{RESET}}$ and RESET have weak internal pullups of typically 3μA. However, external pullup resistors may be used when higher speed is required.

Note 7: The push-button reset input requires an active low signal. Internally, this input signal is debounced and timed for a minimum of 40ms. When this condition is satisfied, the reset outputs go to the active states. The reset outputs will remain in active states for a minimum of 140ms from the moment the push-button reset input is released from logic low level.

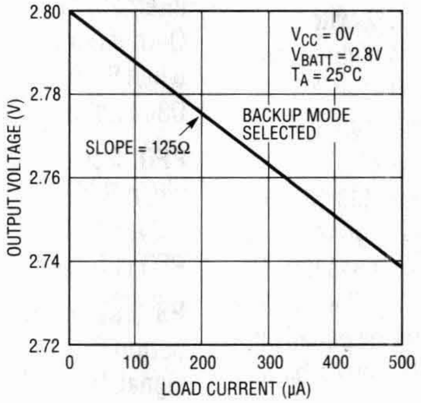
TYPICAL PERFORMANCE CHARACTERISTICS

V_{OUT} vs I_{OUT}



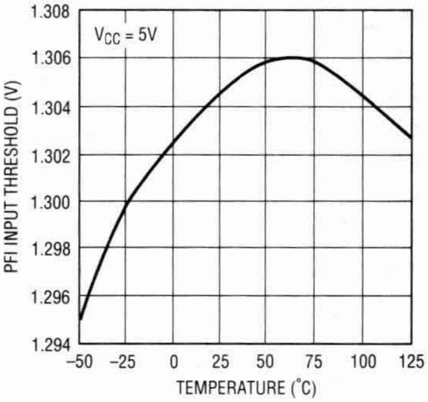
LTC1235 G01

V_{OUT} vs I_{OUT}



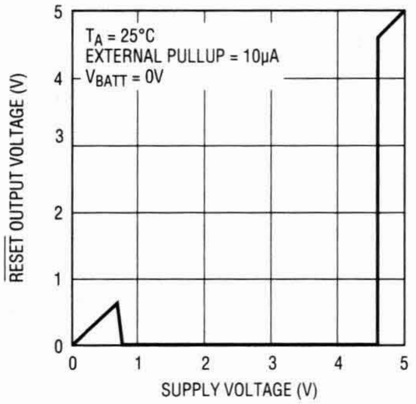
LTC1235 G02

Power Failure Input Threshold vs Temperature



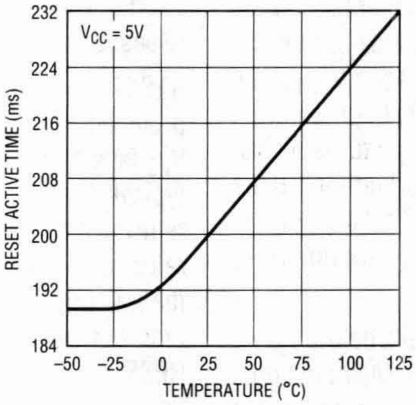
LTC1235 G03

RESET Output Voltage vs Supply Voltage



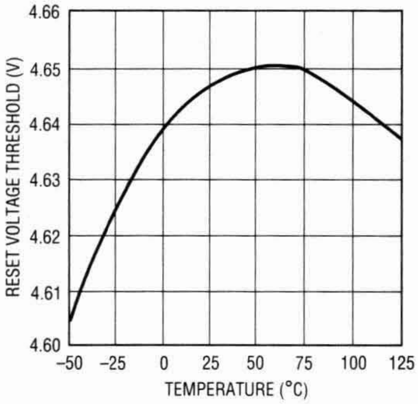
LTC1235 G04

Reset Active Time vs Temperature



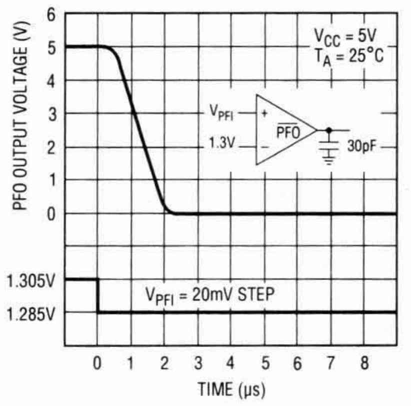
LTC1235 G05

Reset Voltage Threshold vs Temperature



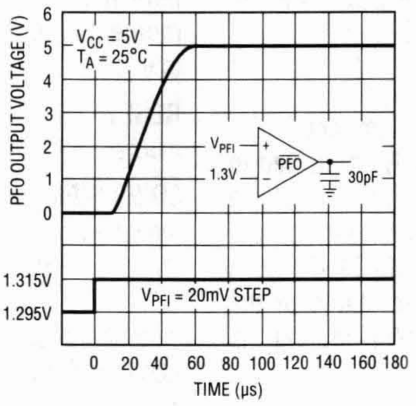
LTC1235 G06

Power Fail Comparator Response Time



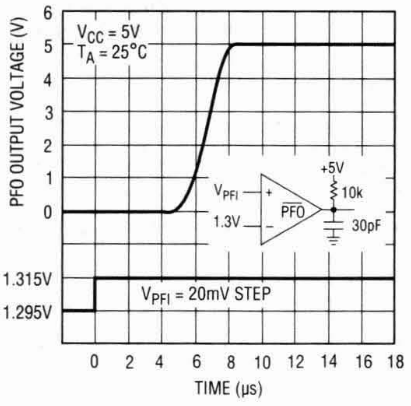
LTC1235 G07

Power Fail Comparator Response Time



LTC1235 G08

Power Fail Comparator Response Time with Pullup Resistor



LTC1235 G09

PIN FUNCTIONS

V_{CC}: +5V supply input. The V_{CC} pin should be bypassed with a 0.1μF capacitor.

Backup: Logic input to control the PMOS switch, M2, when V_{CC} is lower than V_{BATT}. While V_{CC} is falling through the reset voltage threshold, the status of the BACKUP pin (logic low or logic high) is latched in Memory Logic and used to turn on or off M2 when V_{CC} is below V_{BATT}. If the latched status of the BACKUP pin is high, the Memory Logic turns on M2 when V_{CC} falls to 50mV greater than V_{BATT}. If the latched status of the BACKUP pin is low, the Memory Logic keeps M2 off even after V_{CC} falls below V_{BATT}. If the BACKUP pin is left floating it will be pulled high by an internal pullup and the LTC1235 will provide battery backup when V_{CC} falls.

V_{OUT}: Voltage output for backed up memory. Bypass with a capacitor of 0.1μF or greater. During normal operation, V_{OUT} obtains power from V_{CC} through an NMOS power switch, M1, which can deliver up to 50mA and has a typical on resistance of 5Ω. When V_{CC} is lower than V_{BATT}, the status of the BACKUP pin stored in Memory Logic controls M2. If the status is high, the Memory Logic turns on M2 and V_{OUT} is internally switched to V_{BATT} through M2. If the status is low, the Memory Logic keeps M2 off and V_{OUT} is in Battery Saving Mode. If V_{OUT} and V_{BATT} are not used, connect V_{OUT} to V_{CC}.

V_{BATT}: Backup battery input. When V_{CC} falls below V_{BATT}, the status of the BACKUP pin stored in the Memory Logic controls M2. If the status is high, auxiliary power, connected to V_{BATT} is delivered to V_{OUT} through M2. If the status is low, the Memory Logic keeps M2 off and V_{OUT} is in Battery Saving Mode. If backup battery or auxiliary power is not used, V_{BATT} should be connected to GND.

GND: Ground pin.

BATT ON: Battery on logic output from comparator C2. BATT ON goes low when V_{OUT} is internally connected to V_{CC}. The output typically sinks 35mA and can provide base drive for an external PNP transistor to increase the output current above the 50mA rating of V_{OUT}. BATT ON goes high when V_{CC} falls below V_{BATT}, if the status of the BACKUP pin stored in Memory Logic is high and V_{OUT} is switched to V_{BATT}.

PFI: Power Failure Input. PFI is the noninverting input to the Power Fail Comparator, C3. The inverting input is internally connected to a 1.3V reference. The Power Failure Output remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. Connect PFI to GND or V_{OUT} when C3 is not used.

$\overline{\text{PFO}}$: Power Failure Output from C3. $\overline{\text{PFO}}$ remains high when PFI is above 1.3V and goes low when PFI is below 1.3V. When V_{CC} is lower than V_{BATT}, C3 is shut down and $\overline{\text{PFO}}$ is forced low.

$\overline{\text{PB RST}}$: Logic input for direct connection to a push-button. The push-button reset input requires an active low signal. Internally, this input signal is debounced and timed for a minimum of 40ms. When this condition is satisfied, the reset pulse generator forces $\overline{\text{RESET}}$ to active low. The $\overline{\text{RESET}}$ signal will remain active low for a minimum of 140ms from the moment the push-button reset input is released from logic low level.

$\overline{\text{RESET}}$: Logic output for μP reset control. The LTC1235 provides three ways to generate μP reset. First, whenever V_{CC} falls below either the reset voltage threshold (4.65V, typically) or V_{BATT}, $\overline{\text{RESET}}$ goes active low. After V_{CC} returns to 5V, the reset pulse generator forces $\overline{\text{RESET}}$ to remain active low for a minimum of 140ms. Second, when the watchdog timer is enabled but not serviced prior to the time-out period, the reset pulse generator also forces $\overline{\text{RESET}}$ to active low for a minimum of 140ms for every time-out period (see Figure 11). Third, when the $\overline{\text{PB RST}}$ pin stays active low for a minimum of 40ms, $\overline{\text{RESET}}$ is forced low by reset pulse generator. The $\overline{\text{RESET}}$ signal will remain active low for a minimum of 140ms from the moment the push-button reset input is released from logic low level.

RESET: RESET is an active high logic output. It is the inverse of $\overline{\text{RESET}}$.

$\overline{\text{LOW LINE}}$: Logic output from comparator C1. $\overline{\text{LOW LINE}}$ indicates a low line condition at the V_{CC} input. When V_{CC} falls below the reset voltage threshold (4.65V typically), $\overline{\text{LOW LINE}}$ goes low. As soon as V_{CC} rises above the reset voltage threshold, $\overline{\text{LOW LINE}}$ returns high (see Figure 1). $\overline{\text{LOW LINE}}$ goes low when V_{CC} drops below V_{BATT} (see Table 1).

PIN FUNCTIONS

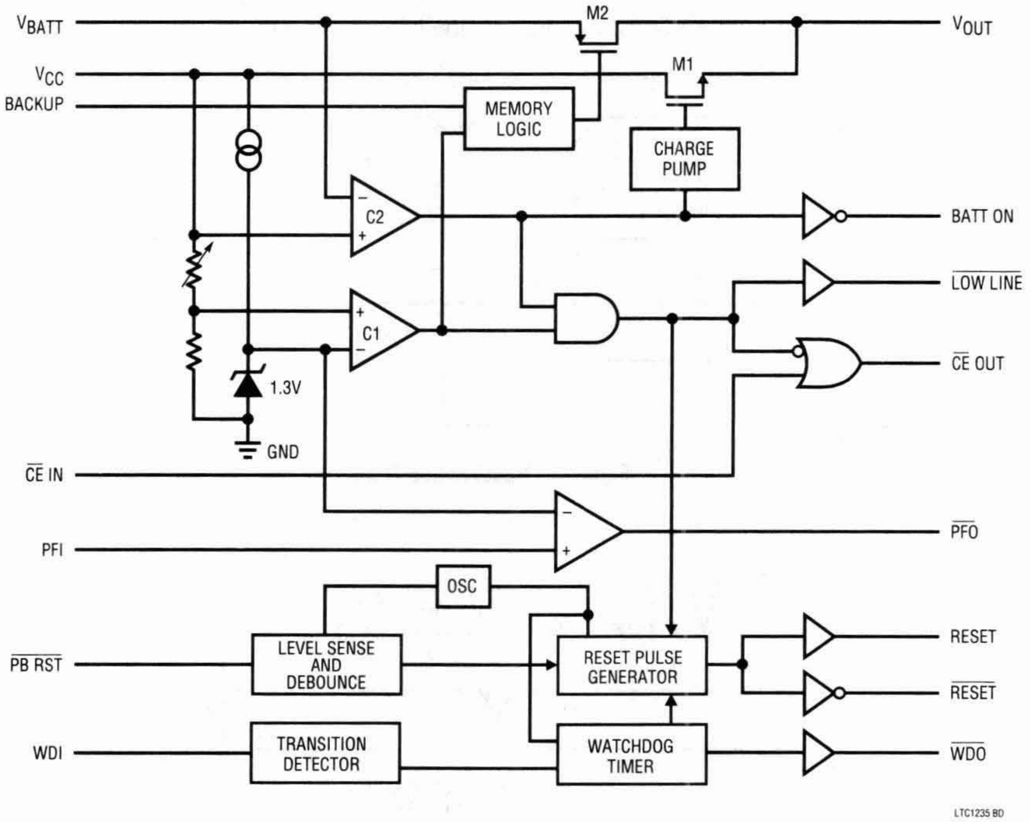
WDI: Watchdog Input, WDI, is a three level input. Driving WDI either high or low for longer than the watchdog time-out period, forces both $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ low. Floating WDI disables the Watchdog Timer. The timer resets itself with each transition of the Watchdog Input (see Figure 11).

$\overline{\text{WDO}}$: Watchdog logic output. When the watchdog input remains either high or low for longer than the watchdog time-out period, $\overline{\text{WDO}}$ goes low. $\overline{\text{WDO}}$ is set high whenever there is a transition on the WDI pin, or $\overline{\text{LOW LINE}}$ goes low. The watchdog timer can be disabled by floating WDI (see Figure 11).

$\overline{\text{CE}}$ IN: Logic input to the $\overline{\text{Chip Enable}}$ gating circuit. $\overline{\text{CE}}$ IN can be derived from microprocessor's address line and/or decoder output. See Applications Information Section and Figure 6 for additional information.

$\overline{\text{CE}}$ OUT: Logic output from the $\overline{\text{Chip Enable}}$ gating circuit. When V_{CC} is above the reset voltage threshold, $\overline{\text{CE}}$ OUT is a buffered replica of $\overline{\text{CE}}$ IN. When V_{CC} is below the reset voltage threshold $\overline{\text{CE}}$ OUT is forced high (see Figure 6).

BLOCK DIAGRAM



V_BATT
V_CC
BACKUP
M2
M1
MEMORY LOGIC
CHARGE PUMP
V_OUT
C2
C1
1.3V
GND
BATT ON
LOW LINE
CE OUT
CE IN
PFI
PFO
OSC
PB RST
LEVEL SENSE AND DEBOUNCE
RESET PULSE GENERATOR
RESET
RESET
WDI
TRANSITION DETECTOR
WATCHDOG TIMER
WDO
LTC1235 BD

APPLICATIONS INFORMATION

Power Monitoring

The LTC1235 uses a bandgap voltage reference and a precision voltage comparator C1 to monitor the 5V supply input on V_{CC} (see BLOCK DIAGRAM). When V_{CC} falls below the reset voltage threshold, the reset outputs are forced to active states. The reset voltage threshold accounts for a 5% variation on V_{CC}, so the reset outputs become active when V_{CC} falls below 4.75V (4.65V typical). On power-up, the reset signals are held active states for a minimum of 140ms after the reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. On power-down, the RESET signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the RESET signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at V_{CC} pin do not activate the reset outputs. Response time is typically 10µs. To help prevent mistriggering due to transient loads, V_{CC} pin should be bypassed with a 0.1µF capacitor with the leads trimmed as short as possible.

LOW LINE is the output of the precision voltage comparator C1. When V_{CC} falls below the reset voltage threshold, LOW LINE goes low. LOW LINE returns high as soon as V_{CC} rises above the reset voltage threshold.

Push-Button Reset

The LTC1235 provides an logic input pin for direct connection to a push-button. The push-button reset input, PB RST, requires an active low signal. Internally, this input signal is debounced and timed for a minimum of 40ms. When this condition is satisfied, the reset pulse generator forces the reset outputs to active states. The reset signals will remain in active states for a minimum of 140ms from the moment the push-button reset input is released from logic low level (Figure 2).

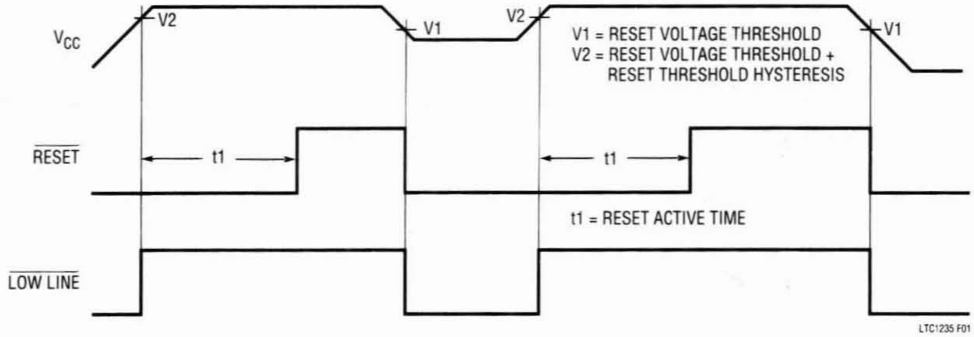

V_{CC}
V2
V1
V2
V1
V1 = RESET VOLTAGE THRESHOLD
V2 = RESET VOLTAGE THRESHOLD + RESET THRESHOLD HYSTERESIS
RESET
t1
t1
t1 = RESET ACTIVE TIME
LOW LINE
LTC1235 F01

Figure 1. Reset Active Time

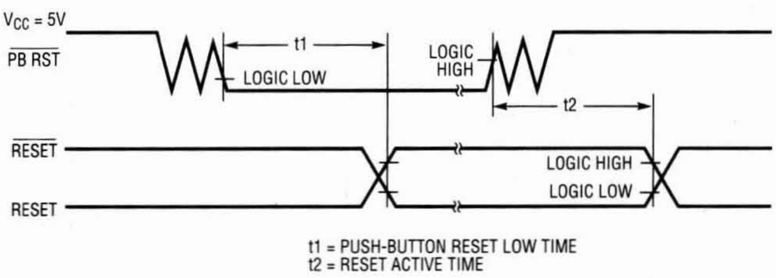

V_{CC} = 5V
PB RST
t1
LOGIC LOW
LOGIC HIGH
t2
RESET
LOGIC HIGH
LOGIC LOW
RESET
t1 = PUSH-BUTTON RESET LOW TIME
t2 = RESET ACTIVE TIME

Figure 2. Push-Button Reset

APPLICATIONS INFORMATION

Voltage Output

During normal operation, the LTC1235 uses a charge pumped NMOS power switch to achieve low dropout and low supply current. This power switch can deliver up to 50mA to V_{OUT} from V_{CC} and has a typical on resistance of 5Ω. The V_{OUT} pin should be bypassed with a capacitor of 0.1μF or greater to ensure stability. Use of a larger bypass capacitor is advantageous for supplying current to heavy transient loads.

When operating currents larger than 50mA are required from V_{OUT}, or a lower dropout (V_{CC} - V_{OUT} voltage differential) is desired, the LTC1235 provides BATT ON output to drive the base of external PNP transistor (Figure 3). Another alternative to provide higher current is to connect a high current Schottky diode from the V_{CC} pin to the V_{OUT} pin to supply the extra current.

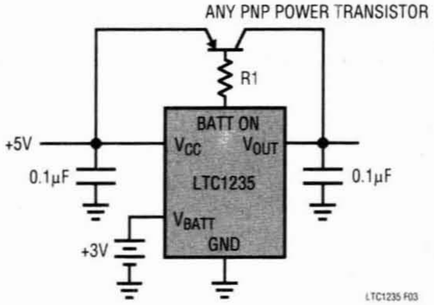


Figure 3. Using BATT ON to Drive External PNP Transistor

The LTC1235 is protected for safe area operation with short circuit limit. Output current is limited to approximately 200mA. If the device is overloaded for a long period of time, thermal shutdown turns the power switch off until the device cools down. The threshold temperature for thermal shutdown is approximately 155°C with about 10°C of hysteresis which prevents the device from oscillating in and out of shutdown.

The PNP switch was not chosen for the internal power switch because it injects unwanted current into the substrate. This current is collected by the V_{BATT} pin in competitive devices and adds to the charging current of the battery which can damage lithium batteries. LTC1235 uses a charge pumped NMOS power switch to eliminate unwanted charging current while achieving low dropout and low supply current. Since no current goes to the substrate, the current collected by V_{BATT} pin is strictly junction leakage.

Conditional Battery Backup

LTC1235 provides an unique feature to either allow V_{OUT} to be switched to V_{BATT} or to disable the CMOS RAM battery backup function when primary power is lost. Disabling the battery backup function is useful in conserving the backup battery's life when the SRAM doesn't need battery backup during long term storage of a computer system, or delivery of the computer system to the end user.

The BACKUP pin (Pin 8) is used to serve this feature on power-down. When V_{CC} is falling through the reset voltage threshold, the status of the BACKUP pin (logic low or logic high) is stored in the Memory Logic (see BLOCK DIAGRAM). If the stored status is logic high and V_{CC} fall to 50mV greater than V_{BATT}, a 125Ω PMOS switch, M2, connects the V_{BATT} input to V_{OUT} and the battery switchover comparator, C2, shuts off the NMOS power switch, M1. M2 is designed for very low dropout voltage (input-to-output differential). This feature is advantageous for low current applications such as battery backup in CMOS RAM and other low power CMOS circuitry. If the stored status is logic low and V_{CC} falls to 50mV greater than V_{BATT}, the Memory Logic keeps M2 off and C2 shuts off M1. V_{OUT} is in Battery Saving Mode (see Figure 4). The supply current in both mode is 1μA maximum.

On power-ups, C2 keeps M1 off before V_{CC} reaches 70mV higher than V_{BATT}. On the first power-up after the battery is replaced (with power off), the status stored in the Memory Logic is undetermined. V_{OUT} could be either in Battery Backup Mode or in Battery Saving Mode. When V_{CC} is 70mV greater than V_{BATT}, M1 connects V_{OUT} to V_{CC}. C2 has typically 20mV of hysteresis to prevent spurious switching when V_{CC} remains nearly equal to V_{BATT} and the status stored in the Memory Logic is high. The response time of C2 is approximately 20μs.

APPLICATIONS INFORMATION

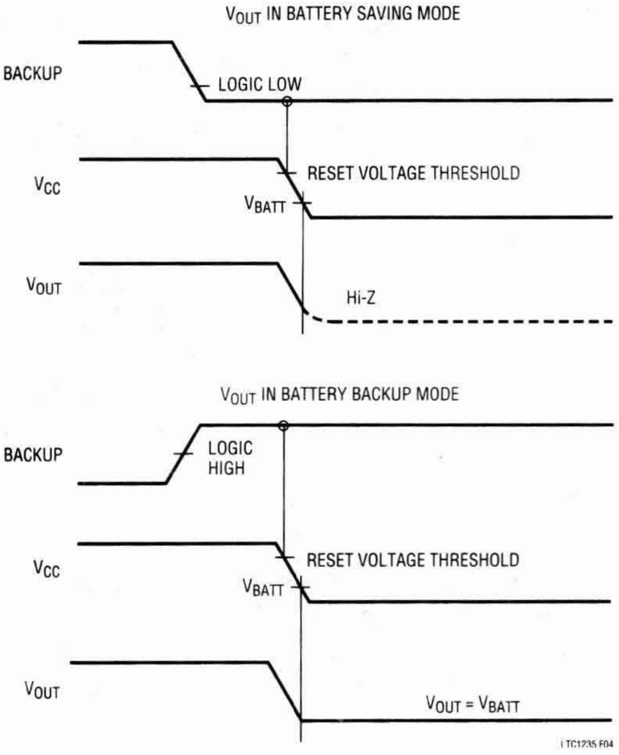

V_{OUT} IN BATTERY SAVING MODE
BACKUP
LOGIC LOW
V_{CC}
RESET VOLTAGE THRESHOLD
V_{BATT}
V_{OUT}
Hi-Z
V_{OUT} IN BATTERY BACKUP MODE
BACKUP
LOGIC HIGH
V_{CC}
RESET VOLTAGE THRESHOLD
V_{BATT}
V_{OUT}
$V_{OUT} = V_{BATT}$
LTC1235 F04

Figure 4. Conditional Battery Backup Operation

The operating voltage at the V_{BATT} pin ranges from 2.0V to 4.25V. High value capacitors, such as electrolytic or farad-size double layer capacitors, can be used for short term memory backup instead of a battery. For capacitor backup, see Typical Applications. The charging resistor for recharging rechargeable batteries should be connected to V_{OUT} through a diode since this eliminates the discharge path that exists when V_{CC} collapses and RAM is not backed up (Figure 5).

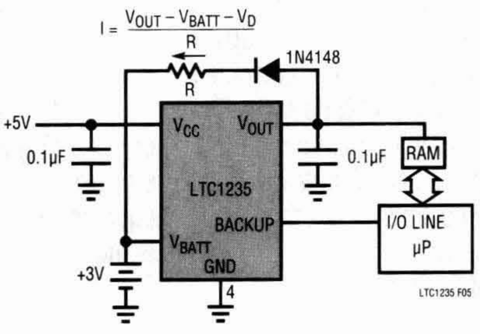

$I = \frac{V_{OUT} - V_{BATT} - V_D}{R}$
1N4148
R
+5V
0.1µF
V_{CC}
V_{OUT}
0.1µF
RAM
LTC1235
BACKUP
I/O LINE
µP
V_{BATT}
GND
+3V
4
LTC1235 F05

Figure 5. Charging External Battery Through V_{OUT}

Replacing the Backup Battery with Power On

When changing the backup battery with system power on, spurious resets can occur while battery is removed due to battery standby current. Although battery standby current is only a tiny leakage current, it can still charge up the stray capacitance on the V_{BATT} pin. The oscillation cycle is as follows: When V_{BATT} reaches within 50mV of V_{CC}, the LTC1235 switches to battery backup or battery saving mode. In either case, the battery supply current pulls V_{BATT} low and the device goes back to normal operation. The leakage current then charges up the V_{BATT} pin again and the cycle repeats.

If spurious resets during battery replacement pose no problems, then no action is required. Otherwise, two methods can be used to eliminate this problem. First, a capacitor from V_{BATT} to GND will allow time for battery replacement by slowing the charge rate. For example, the battery standby current is 1µA maximum over temperature and the external capacitor required to slow the charge rate is:

$$C_{EXT} \geq T_{REQ'D}\left(\frac{1\mu A}{V_{CC} - V_{BATT}}\right)$$

where $T_{REQ'D}$ is the maximum time required to replace the backup battery. With $V_{CC} = 4.5V$, $V_{BATT} = 3V$ and $T_{REQ'D} = 3$ sec, the value for external capacitor is 2µF. Second, a resistor from V_{BATT} to GND will hold the pin low while changing the battery. For example, the battery standby current is 1µA maximum over temperature and the external resistor required to hold V_{BATT} below V_{CC} is:

$$R \leq \frac{V_{CC} - 50mV}{1\mu A}$$

With $V_{CC} = 4.5V$, a 4.3MΩ resistor will work. With a 3V battery, this resistor will draw only 0.7µA from the battery, which is negligible in most cases.

If the battery connections are made with long wires or PC traces, inductive spikes can be generated during battery replacement. Even if a resistor is used to prevent spurious resets as described above, these spikes can take the V_{BATT} pin below GND violating the LTC1235 absolute maximum ratings. A 0.1µF capacitor from V_{BATT} to GND is recommended to eliminate these potential spikes when battery replacement is made through long wires.

APPLICATIONS INFORMATION

Table 1 shows the state of each pin during battery backup. If the backup battery is not used, connect V_{BATT} to GND and V_{OUT} to V_{CC}.

Table 1. Input and Output Status in Battery Backup Mode

SIGNAL	STATUS
V_{CC}	C2 monitors V_{CC} for active switchover.
BACKUP	BACKUP is ignored.
V_{OUT}	V_{OUT} is connected to V_{BATT} through an internal PMOS switch.
V_{BATT}	The supply current is 1µA maximum.
BATT ON	Logic high. The open circuit output voltage is equal to V_{OUT}.
PFI	Power Failure Input is ignored.
$\overline{\text{PFO}}$	Logic low
$\overline{\text{PB RST}}$	$\overline{\text{PB RST}}$ is ignored.
$\overline{\text{RESET}}$	Logic low
RESET	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{\text{LOW LINE}}$	Logic low
WDI	Watchdog Input is ignored.
$\overline{\text{WDO}}$	Logic high. The open circuit output voltage is equal to V_{OUT}.
$\overline{\text{CE}}$ IN	$\overline{\text{Chip Enable}}$ Input is ignored.
$\overline{\text{CE}}$ OUT	Logic high. The open circuit output voltage is equal to V_{OUT}.

Memory Protection

The LTC1235 includes memory protection circuitry which ensures the integrity of the data in memory by preventing write operations when V_{CC} is at invalid level. Two pins, $\overline{\text{CE}}$ IN and $\overline{\text{CE}}$ OUT, control the $\overline{\text{Chip Enable}}$ or $\overline{\text{Write}}$ inputs of CMOS RAM. When V_{CC} is +5V, $\overline{\text{CE}}$ OUT follows $\overline{\text{CE}}$ IN with a typical propagation delay of 20ns. When V_{CC} falls below the reset voltage threshold or V_{BATT}, $\overline{\text{CE}}$ OUT is forced high, independent of $\overline{\text{CE}}$ IN. $\overline{\text{CE}}$ OUT is an alternative signal to drive the $\overline{\text{CE}}$, $\overline{\text{CS}}$, or $\overline{\text{Write}}$ input of battery-backed up CMOS RAM. $\overline{\text{CE}}$ OUT can also be used to drive the $\overline{\text{Store}}$ or $\overline{\text{Write}}$ input of an EEPROM, EAROM or NOVRAM to achieve similar protection. Figure 6 shows the timing diagram of $\overline{\text{CE}}$ IN and $\overline{\text{CE}}$ OUT.

$\overline{\text{CE}}$ IN can be derived from the microprocessor's address decoder output. Figure 7 shows a typical nonvolatile CMOS RAM application.

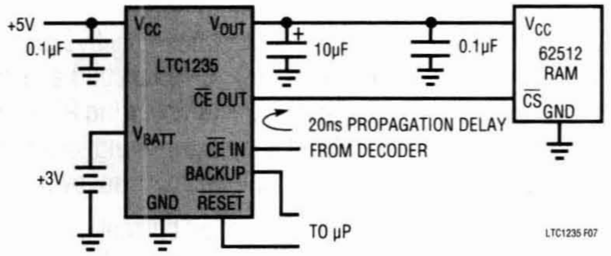

+5V
0.1µF
V_CC
V_OUT
LTC1235
CE OUT
V_BATT
CE IN
BACKUP
GND
RESET
+3V
10µF
0.1µF
V_CC
62512
RAM
CS
GND
20ns PROPAGATION DELAY
FROM DECODER
TO µP
LTC1235 F07

Figure 7. A Typical Nonvolatile CMOS RAM Application

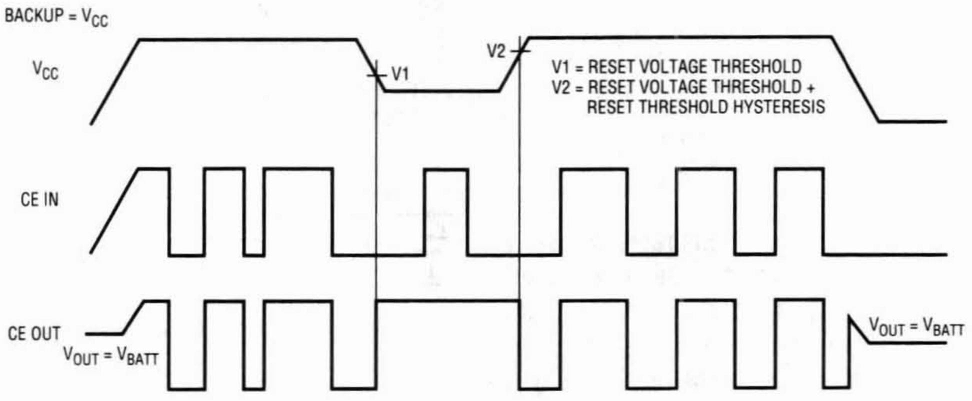

BACKUP = V_CC
V_CC
V1
V2
V1 = RESET VOLTAGE THRESHOLD
V2 = RESET VOLTAGE THRESHOLD + RESET THRESHOLD HYSTERESIS
CE IN
CE OUT
V_OUT = V_BATT
V_OUT = V_BATT
LTC1235 F06

Figure 6. Timing Diagram for $\overline{\text{CE}}$ IN and $\overline{\text{CE}}$ OUT

APPLICATIONS INFORMATION

Power Fail Warning

The LTC1235 generates a Power Failure Output ($\overline{PFO}$) for early warning of failure in the microprocessor's power supply. This is accomplished by comparing the Power Failure Input (PFI) with an internal 1.3V reference. $\overline{PFO}$ goes low when the voltage at PFI pin is less than 1.3V. Typically PFI is driven by an external voltage divider (R1 and R2 in Figures 8 and 9) which senses either an unregulated DC input or a regulated 5V output. The voltage divider ratio can be chosen such that the voltage at PFI pin falls below 1.3V several milliseconds before the +5V supply falls below the maximum reset voltage threshold 4.75V. $\overline{PFO}$ is normally used to interrupt the microprocessor to execute shut-down procedure between $\overline{PFO}$ and $\overline{RESET}$ or RESET.

The power fail comparator, C3, does not have hysteresis. Hysteresis can be added however, by connecting a resistor between the $\overline{PFO}$ output and the noninverting PFI input pin as shown in Figures 8 and 9. The upper and lower trip points in the comparator are established as follows:

When $\overline{PFO}$ output is low, R3 sinks current from the summing junction at the PFI pin.

$$V_H = 1.3V\left(1 + \frac{R1}{R2} + \frac{R1}{R3}\right)$$

When $\overline{PFO}$ output is high, the series combination of R3 and R4 source current into the PFI summing junction.

$$V_L = 1.3V\left(1 + \frac{R1}{R2} - \frac{(5V - 1.3V)R1}{1.3V(R3 + R4)}\right)$$

$$\text{Assuming } R4 \ll R3,\ V_{HYSTERESIS} = 5V\frac{R1}{R3}$$

Example 1: The circuit in Figure 8 demonstrates the use of the power fail comparator to monitor the unregulated power supply input. Assuming the the rate of decay of the supply input V_{IN} is 100mV/ms and the total time to execute a shut-down procedure is 8ms. Also the noise of V_{IN} is 200mV. With these assumptions in mind, we can reasonably set V_L = 7.5V which 1.25V greater than the sum of maximum reset voltage threshold and the dropout voltage of LT1086-5 (4.75V + 1.5V) and $V_{HYSTERESIS}$ = 850mV.

$$V_{HYSTERESIS} = 5V\frac{R1}{R3} = 850mV$$

$$R3 \approx 5.88\ R1$$

Choose R3 = 300kΩ and R1 = 51kΩ. Also select R4 = 10kΩ which is much smaller than R3.

$$7.5V = 1.3V\left(1 + \frac{51k\Omega}{R2} - \frac{(5V - 1.3V)51k\Omega}{1.3V(310k\Omega)}\right)$$

R2 = 9.7kΩ, Choose nearest 5% resistor 10k and recalculate V_L,

$$V_L = 1.3V\left(1 + \frac{51k\Omega}{10k\Omega} - \frac{(5V - 1.3V)51k\Omega}{1.3V(310k\Omega)}\right) = 7.32V$$

$$V_H = 1.3V\left(1 + \frac{51k\Omega}{10k\Omega} + \frac{51k\Omega}{300k\Omega}\right) = 8.151V$$

$$\frac{(7.32V - 6.25V)}{100mV/ms} = 10.7ms$$

$$V_{HYSTERESIS} = 8.151V - 7.32V = 831mV$$

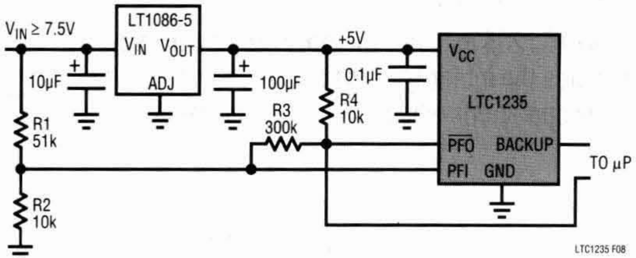


Figure 8. Monitoring *Unregulated* DC Supply with the LTC1235 Power Fail Comparator

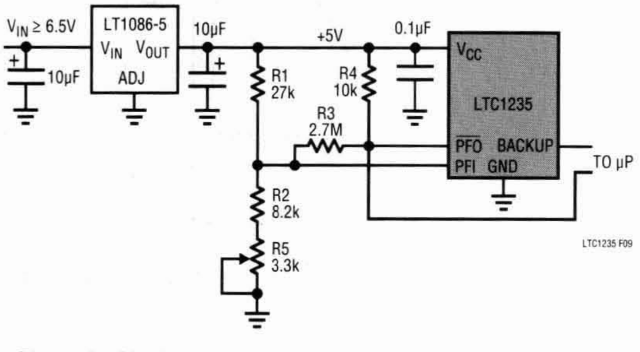


Figure 9. Monitoring *Regulated* DC Supply with the LTC1235 Power Fail Comparator

APPLICATIONS INFORMATION

The 10.7ms allows enough time to execute shut-down procedure for microprocessor and 831mV of hysteresis would prevent $\overline{PFO}$ from going low due to the noise of V_{IN}.

Example 2: The circuit in Figure 9 can be used to measure the regulated 5V supply to provide early warning of power failure. Because of variations in the PFI threshold, this circuit requires adjustment to ensure that the PFI comparator trips before the reset threshold is reached. Adjust R5 such that the $\overline{PFO}$ output goes low when the V_{CC} supply reaches the desired level (e.g., 4.85V).

Monitoring the Status of the Battery

C3 can also monitor the status of the memory backup battery (Figure 10). If desired, the $\overline{CE}$ OUT can be used to apply a test load to the battery. Since $\overline{CE}$ OUT is forced high in battery backup mode, the test load will not be applied to the battery while it is in use, even if the microprocessor is not powered.

Watchdog Timer

The LTC1235 provides a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the time-out period, the reset outputs are forced to active states for a minimum of 140ms. The watchdog time-out period is fixed at 1.0 second minimum on the LTC1235. This time-out period provides adequate time for many systems to service the watchdog timer immediately after a reset. Figure 11 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon as the reset outputs are inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog time is reset and begins to time out again. To ensure the watchdog time does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog timer can be deactivated by floating the WDI pin. The timer is also disabled when V_{CC} falls below the reset voltage threshold or V_{BATT}.

The Watchdog Output, $\overline{WDO}$, goes low if the watchdog timer is allowed to time out and remains low until set high by the next transition on the WDI pin. $\overline{WDO}$ is also set high when V_{CC} falls below the reset voltage threshold or V_{BATT}.

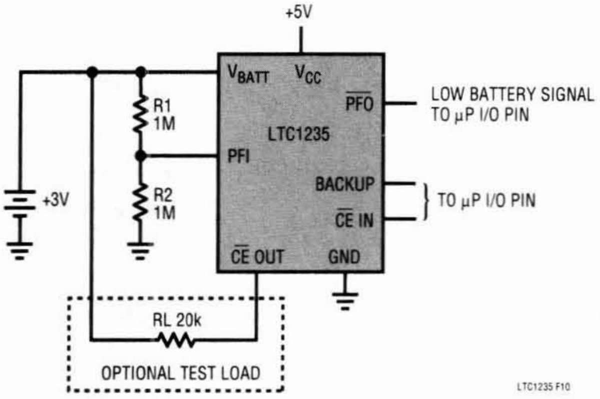


Figure 10. Backup Battery Monitor with Optional Test Load

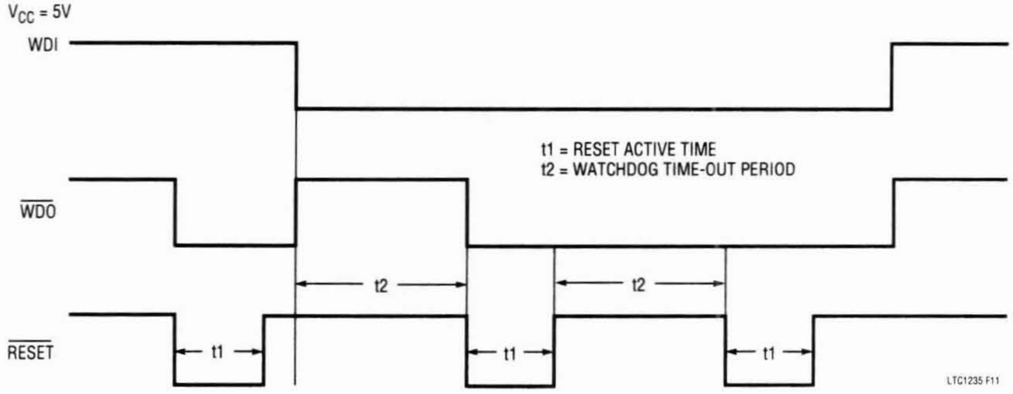
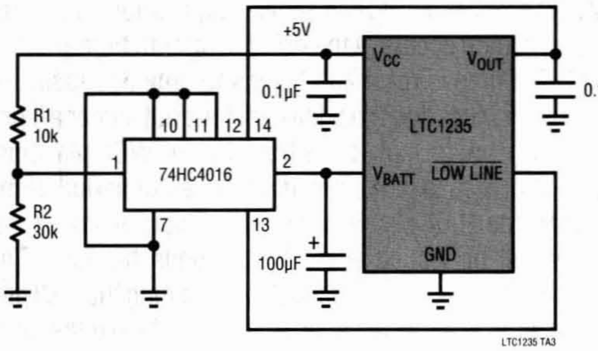


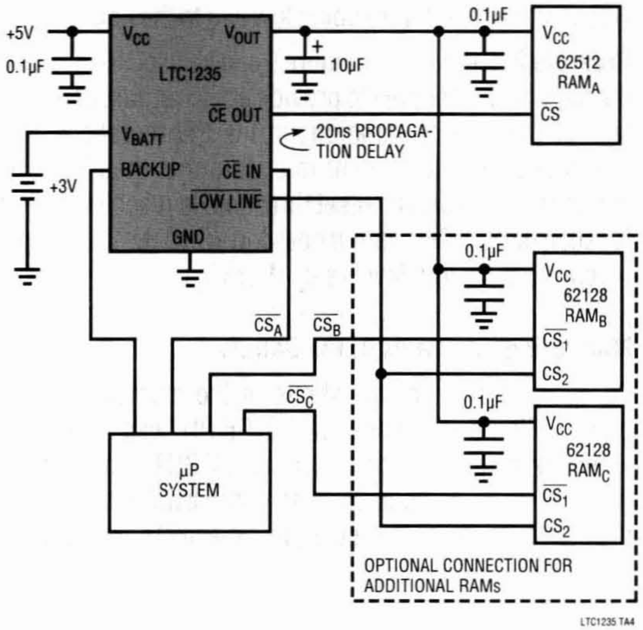
Figure 11. Watchdog Time-out Period and Reset Active Time

TYPICAL APPLICATIONS

Capacitor Backup with 74HC4016 Switch


+5V
V_{CC}
V_{OUT}
0.1µF
0.1µF
LTC1235
R1
10k
10
11
12
14
1
74HC4016
2
V_{BATT}
$\overline{LOW\ LINE}$
R2
30k
7
13
100µF
GND
LTC1235 TA3

Write Protect for Additional RAMs


+5V
0.1µF
V_{CC}
V_{OUT}
LTC1235
10µF
0.1µF
V_{CC}
62512
RAM_A
$\overline{CS}$
V_{BATT}
$\overline{CE}$ OUT
20ns PROPAGATION DELAY
+3V
BACKUP
$\overline{CE}$ IN
$\overline{LOW\ LINE}$
GND
0.1µF
V_{CC}
62128
RAM_B
$\overline{CS_A}$
$\overline{CS_B}$
$\overline{CS_1}$
CS_2
$\overline{CS_C}$
0.1µF
V_{CC}
62128
RAM_C
µP SYSTEM
$\overline{CS_1}$
CS_2
OPTIONAL CONNECTION FOR ADDITIONAL RAMs
LTC1235 TA4

SECTION 10—COMPARATORS

SECTION 10—COMPARATORS

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PROPRIETARY PRODUCTS
LT1015, High Speed Dual Line Receiver **10-4**
LT1017CS8/LT1018CS8, Micropower Dual Comparator **10-6**
LT1116, 12ns, Single Supply Ground-Sensing Comparator **10-7**

COMPARATOR SELECTION GUIDE

MILITARY

PART NUMBER	RESPONSE TIME MAX (ns)	V_{OS} MAX (mV)	I_B MAX (nA)	DRIVE CAPABILITY (mA)	GAIN MIN (V/mV)	I_{SUPPLY} POSITIVE (mA)	I_{SUPPLY} NEGATIVE (mA)	PACKAGES AVAILABLE	IMPORTANT FEATURES
LT1011AM	250	0.5	25	50	200	4.0	2.5	H, J8	Low V_{OS}, Low I_B, High Output Drive, 12-Bit Acc.
LT1011M	250	1.5	50	50	200	4.0	2.5	H, J8	
LT1015M	16	20	30000	4	1	70	—	J8, N8	Dual, Ultra High Speed, Latched TTL Outputs, Stable in Active Region
LT1016M	12	±2.5	10000	10	2	35	5	H, J8	Ultra High Speed, TTL Outputs, True Output Latch, Stable in Active Region, Pin/Pin Replacement for AM686
LT1017M	—	1	15	30	1000	0.060	—	H, J8	LT1017 has Lowest Supply Current, LT1018 is Faster. Both are Dual Comparators with Same Pinout as 193 Types.
LT1018M	—	1	75	35	1000	0.250	—	H, J8	
LT111A	250	1.0	100	50	200	4.0	2.5	H, J8	Low V_{OS}, High Gain
LM111	—	3.0	100	50	40	6.0	5.0	H, J8	General Purpose
LT119A	80 (typ)	1.0	500	25	20	11.5	4.5	H, J	Dual, Low V_{OS}, High CMRR
LM119	80 (typ)	4.0	500	25	10	11.5	4.5	H, J	Dual, General Purpose
LTC1040M	100µs	0.5	3	*	†	300nA**	1nA	J	CMOS Sampling Comparator
LTC1041M	100µs	0.5	0.3	10	—	3	—	J8, N8	CMOS Bang-Bang Controller
LTC1042M	100µs	1.0	3	*	†	300nA**	1nA	J8	CMOS Window Comparator
LT685M	6.5	±2.0	10000	††	1.6 (typ)	22	26	H, J	Ultra High Speed, ECL Outputs, Output Latch, External Hysteresis Control

COMMERCIAL

PART NUMBER	RESPONSE TIME MAX (ns)	V_{OS} MAX (mV)	I_B MAX (nA)	DRIVE CAPABILITY (mA)	GAIN MIN (V/mV)	I_{SUPPLY} POSITIVE (mA)	I_{SUPPLY} NEGATIVE (mA)	PACKAGES AVAILABLE	IMPORTANT FEATURES
LT1011AC	250	0.5	25	50	200	4.0	2.5	H, J8, N8	Low V_{OS}, Low I_B, High Output Drive, 12-Bit Acc.
LT1011C	250	0.5	50	50	200	4.0	2.5	H, J8, N8	
LT1015C	14	20	30000	4	1	70	—	J8, N8	Dual, Ultra High Speed, Latched TTL Outputs, Stable in Active Region
LT1016C	12	±2.5	10000	10	1.4	35	5	H, J8, S8	Ultra High Speed, TTL Outputs, True Output Latch, Stable in Active Region, Pin/Pin Replacement for AM686, Single Supply Operation
LT1017C	—	1	15	30	1000	0.060	—	H, S	LT1017 has Lowest Supply Current, LT1018 is Faster. Both are Dual Comparators with Same Pinout as 193 Types.
LT1018C	—	1	75	35	1000	0.250	—	H, S	
LT311A	250	1.0	100	50	200	4.0	2.5	H, J8	Low V_{OS}, High Gain
LM311	—	7.5	250	50	40	7.5	5.0	H, J8	General Purpose
LT319A	80 (typ)	1.0	500	25	20	12.5	5.0	H, J, N	Dual, Low V_{OS}, High CMRR
LM319	80 (typ)	8.0	1000	25	8	12.5	5.0	H, J, N	Dual, General Purpose
LTC1040C	100µs	0.5	3	*	†	300nA**	1nA	J, N, S	CMOS Sampling Comparator
LTC1041C	100µs	0.5	0.3	10	—	3	—	J8, N8	CMOS Bang-Bang Controller
LTC1042C	100µs	1.0	3	*	†	300nA**	1nA	J, N8	CMOS Window Comparator
LT685C	6.5	±2.0	10000	††	1.6 (typ)	22	26	H, J, N	Ultra High Speed, ECL Outputs, Output Latch, External Hysteresis Control
LT1116	14	±3.0	20000	10	2.4	38	7	N8, S8	Ground Sense Capability, Ultra High Speed, TTL Outputs, True Output Latch, Stable in Active Region, Single Supply Operation, Pin/Pin Replacement for AM686

* 1 Std. TTL Load.

** Supply Current Depends on Clock Rate.

† Gain Errors are Included in V_{OS} Spec.

†† Can Drive Terminated 50Ω Transmission Lines.

LINEAR TECHNOLOGY

LT1015

High Speed Dual Line Receiver

FEATURES

- 10ns Response Time
- 2ns Setup Time for Latch
- Operates on Single 5V Supply
- Dual Function in 8-Pin Package
- No Input Slew Rate Requirement
- Latch Function Included On Chip
- True Differential Inputs

APPLICATIONS

- High Speed Differential Line Receiver
- Pulse Height/Width Discriminator
- Timing and Delay Generators
- Analog to Digital Interface

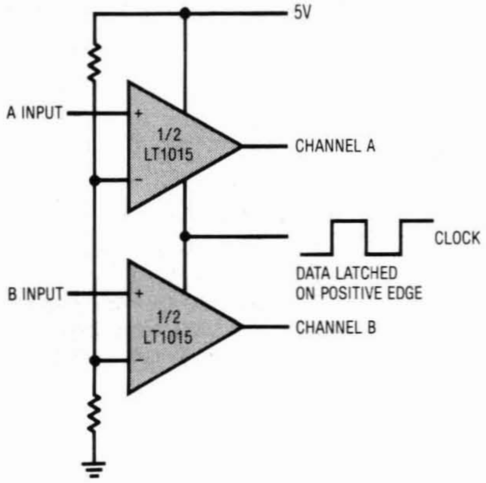
DESCRIPTION

The LT1015 is a dual high speed comparator intended for line receiver and other general purpose fast comparator functions. It has 10ns response time, true differential inputs, TTL outputs, and operates from a single 5V supply. A unique output stage design virtually eliminates power supply glitching during transitions. This greatly reduces instability and crosstalk problems in multiple line applications. No minimum input slew rate is required as in previous TTL output comparators.

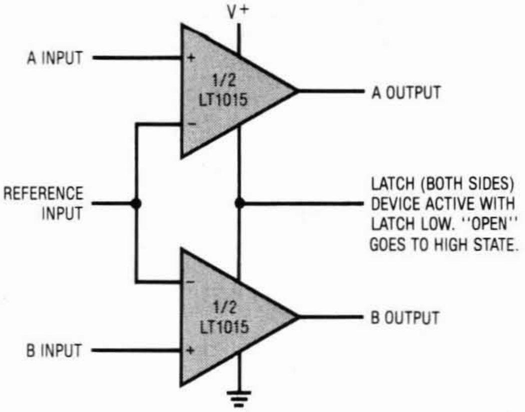
The LT1015 has a true latch pin for retaining output data. Setup time is 2ns, allowing the comparators to capture data much faster than the actual flowthrough response time. 8-pin miniDIP and ceramic packages allow high packing density.

TYPICAL APPLICATION

2 Channel 20MHz Clocked Line Receiver


5V
A INPUT
1/2
LT1015
CHANNEL A
CLOCK
DATA LATCHED
ON POSITIVE EDGE
B INPUT
1/2
LT1015
CHANNEL B

BLOCK DIAGRAM

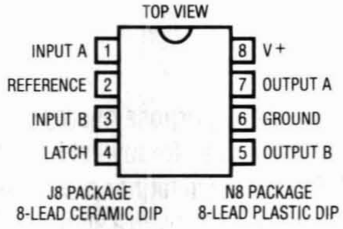

V+
A INPUT
1/2
LT1015
A OUTPUT
REFERENCE
INPUT
LATCH (BOTH SIDES)
DEVICE ACTIVE WITH
LATCH LOW. "OPEN"
GOES TO HIGH STATE.
1/2
LT1015
B OUTPUT
B INPUT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7V
Differential Input Voltage	5V
Input Voltage Positive	Supply + 0.5V
Negative	– 1V
Input Current (Forced) Positive	20mA
Latch Pin Voltage	Supply + 1V
Output Current (Continuous)	± 20mA
Operating Temperature Range	
LT1015M	– 55°C to 125°C*
LT1015C	0°C to 70°C
Storage Temperature Range	– 65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

*Air flow must be provided for $T_A > 100°C$.

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1015MJ8
LT1015CJ8
LT1015CN8

ELECTRICAL CHARACTERISTICS

$V^+ = 4.6V$ to $5.4V$, $V_{LATCH} = 0V$, Common Mode Input Voltage = 2.5V, $T_j = 25°C$, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 1)	$V_{CM} = 1.25V$ to $(V^+ - 1.5V)$	●		1	20	mV
Input Bias Current	$\Delta V_{IN} = 0V$ (Note 2)	●		15	30	μA
Reference Input Current	$\Delta V_{IN} = 0V$ (Note 2)	●		30	60	μA
Voltage Gain (Note 3)	$V_{OUT} = 0.5V$ to $2.5V$ Load = 1 TTL Gate	●	1000	2500		V/V
Common Mode Input Range (Note 5)	Minimum Input Maximum Input	● ●	 $V^+ - 1.5$	1.0 $V^+ - 1.0$	1.25	V V
Output High Voltage Output Low Voltage	$I_{OUT} = 4mA$ $I_{SINK} = 4mA$	● ●	2.5	 0.3	 0.5	V V
Supply Current	$V^+ = 5V$	●		55	70	mA
Latch Pin High Input Voltage	Device Latched	●			2	V
Latch Pin Low Input Voltage	Device Active	●	0.8			V
Latch Pin Current		●			1	mA
Propagation Delay	$\Delta V_{IN} \geq 20mV$ (Note 4) $0°C \leq T_j \leq 100°C$ $-55°C \leq T_j \leq 150°C$	 ● ●	 7 7	 10 10	 14 16	 ns ns
Latch Setup Time				2		ns

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input offset voltage is the maximum required to drive the output to a low state of 0.5V and a high state of 2.5V.

Note 2: Input currents are measured by applying a large positive differential input voltage. The resulting input current is divided by two to obtain input current at $\Delta V_{IN} = 0V$.

Note 3: Voltage gain is guaranteed by design, but not tested.

Note 4: Propagation delay is sample tested in production with a large overdrive. The limit is guard banded to account for the slight increase (≈ 500ps) at 20mV overdrive.

Note 5: Common mode input range is the voltage range over which the differential input offset voltage is less than 20mV. If both inputs remain inside this common mode range, propagation delay will be unaffected. It will also be normal if the signal input is below the 1.25V lower limit when the input transition begins. An increase in propagation delay of up to 10ns may occur if the signal input is above the upper common mode limit when the transition begins. Sine wave inputs may not be affected when the peak exceeds the common mode range if the signal is inside the common mode range for 10ns before threshold is reached.

Note 6: For typical curves see the LT1016 data sheet.

LT1017CS8/LT1018CS8

Dual Micropower Comparator

DESCRIPTION

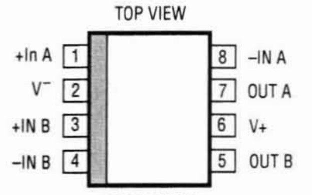
The LT1017 and LT1018 are general purpose micropower comparators. The LT1017 is optimized for lowest operating power while the LT1018 operates at higher power and higher speed. Both devices can operate from a single 1.1V cell up to 40V. The output stage includes a class "B" pull-up current source, eliminating the need for an external resistive pull-up and saving power. The output stage is also designed to allow driving loads connected to a supply more positive than the device, as can comparators with open collector output stages.

Input specifications are also excellent. On-chip trimming minimizes offset voltage, while high gain and common-mode rejection ratio keep other input-referred errors low. Common-mode voltage range includes ground. Special circuitry prevents false output states even if the input is overdriven.

APPLICATIONS

- Power Supply Monitors
- Relay Driving
- Oscillators

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO
(0.15" BODY WIDTH)

ORDER PART NUMBER
LT1017CS8 LT1018CS8
PART MARKING
1017 1018

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range
LT1017CS8 .... $0°C \le T_A \le 70°C$
LT1018CS8 .... $0°C \le T_A \le 70°C$

ELECTRICAL CHARACTERISTICS

Electrical characteristics of the LT1017CS8 and LT1018CS8 are idential to those of the standard datasheet electricals for the LT1071CS/LT1018CS and LT1017CN8/LT1018CN8. Please refer to the standard datasheet for $0°C \le T_A \le 70°C$ electricals.

Note: The pin assignment of the LT1017CS8/LT1018CS8 does not match the pin assignment for the LT1017CN8/LT1018CN8 plastic dual-in-line package.

12ns, Single Supply Ground-Sensing Comparator

FEATURES

- Ultra Fast (12ns Typ)
- Operates off **Single** +5V Supply or ±5V
- Input Common Mode Extends to Negative Supply
- No Minimum Input Slew Rate Requirement
- Complementary TTL Output
- Inputs Can Exceed the Positive Supply Up to +15V without Damaging the Comparator
- Low Offset Voltage
- Pin-Compatible with LT1016
- Output Latch Capability

APPLICATIONS

- High Speed A/D Converters
- Zero Crossing Detectors
- Current Sense for Switching Regulators
- Extended Range V to F Converters
- Fast Pulse Height/Width Discriminators
- High Speed Triggers
- Line Receivers
- High Speed Sampling Circuits

DESCRIPTION

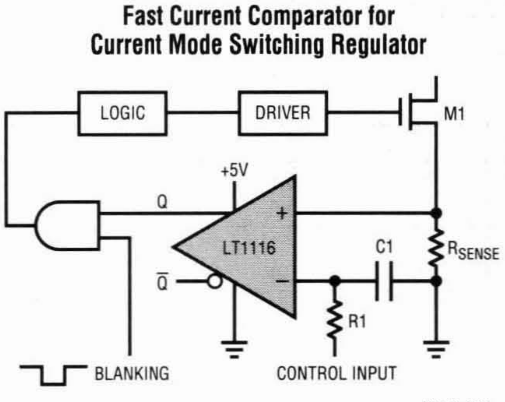
The LT1116 is an ultra fast (12ns) comparator designed for sensing signals near the negative supply. The input common mode range extends from 2.5V below the positive supply down to the negative supply rail. Like the LT1016, this comparator is specifically designed to interface directly to TTL logic with complementary outputs. The comparator may operate from either a single +5V supply or dual ±5V supplies. Tight offset voltage specifications and high gain allow the LT1116 to be used in precision applications.

The LT1116 is designed for improved speed and stability for a wide range of operating conditions. The output stage provides active drive in both directions for maximum speed into TTL logic or passive loads, yet it has minimal cross-conduction current. Unlike other fast comparators, the LT1116 remains stable even for slow transitions through the active region, which eliminates the need to specify a minimum input slew rate.

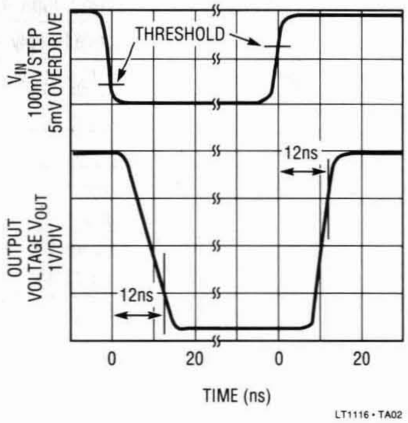
The LT1116 has an internal, TTL compatible latch for retaining data at the outputs. The latch holds data as long as the latch pin is held high. Device parameters such as gain, offset, and negative power supply current are not significantly affected by variations in negative supply voltage.

TYPICAL APPLICATION

Fast Current Comparator for Current Mode Switching Regulator



Comparator Response Time

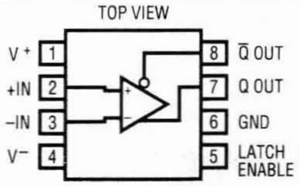
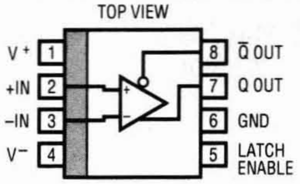


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) to GND 7V
Negative Supply Voltage (V^-) .... –7V to GND
Voltage
  Differential Input Voltage .... ±15V
  Inputs Voltage (Either Input) .... (V^-) –0.3V to 15V
  Latch Pin Voltage .... Equal to Supplies
Output Current (Continuous) .... ±20mA
Operating Temperature Range
  LT1116C .... 0°C to 70°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

 TOP VIEW V+ 1 +IN 2 –IN 3 V– 4 8 Q̄ OUT 7 Q OUT 6 GND 5 LATCH ENABLE + – N8 PACKAGE 8-LEAD PLASTIC DIP LT1116 • POI01	ORDER PART NUMBER LT1116CN8
 TOP VIEW V+ 1 +IN 2 –IN 3 V– 4 8 Q̄ OUT 7 Q OUT 6 GND 5 LATCH ENABLE + – S8 PACKAGE 8-LEAD PLASTIC SOIC LT1116 • POI02	LT1116CS8 S8 PART MARKINGS 1116

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $V^- = -5V$, V_{OUT} (Q) = 1.4V, LATCH = 0V, $T_A = 25°C$.
Specifications for V_{OS}, I_B, CMRR, and Voltage Gain are valid for single supply operation, $V^+ = 5V$, $V^- = 0V$, unless otherwise noted.

				LT1116			
SYMBOL	**PARAMETERS**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$ (Note 2)			1.0	±3.0	mV
			●			3.5	mV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage Drift		●		5		$\frac{\mu V}{°C}$
I_{OS}	Input Offset Current	(Note 2)	●		0.5	2	μA
I_B	Input Bias Current, Sourcing	(Note 3)	●		10	20	μA
	Input Voltage Range	Arbitrary Supply Range	●	V^-		(V^+) –2.5	V
		Single +5V Supply	●	0		2.5	V
CMRR	Common Mode Rejection Ratio	$-5V \le V_{CM} \le 2.5V$, $V_S = \pm5V$	●	75	90		dB
		$0V \le V_{CM} \le 2.5V$	●	65	90		dB
PSRR	Power Supply Rejection Ratio	Positive Supply $4.6V \le V^+ \le 5.4V$	●	60	75		dB
		Negative Supply $-7V \le V^- \le -2V$	●	80	100		dB
A_V	Small Signal Voltage Gain	$1V \le V_{OUT} \le 2V$		1400	3000		V/V
I+	+Supply Current		●		27	38	mA
I–	–Supply Current		●		5	7	mA
V_{OH}	Output High Voltage	$I_{SOURCE} = 1mA$	●	2.7	3.4		V
		$I_{SOURCE} = 10mA$	●	2.4	3.0		V
V_{OL}	Output Low Voltage	$I_{SINK} = 4mA$	●		0.3	0.5	V
		$I_{SINK} = 10mA$			0.4		V

ELECTRICAL CHARACTERISTICS $V^+ = 5V$, $V^- = -5V$, V_{OUT} (Q) = 1.4V, LATCH = 0V, $T_A = 25°C$, unless otherwise noted.

SYMBOL	PARAMETERS	CONDITIONS		LT1116 MIN	LT1116 TYP	LT1116 MAX	UNITS
V_{IH}	+Latch Threshold		●	2.0			V
V_{IL}	–Latch Threshold		●			0.8	V
I_{IL}	Latch Input Current	$V_{LATCH} = 0V$	●		–20	–500	μA
t_{PD}	Propagation Delay	$\Delta V_{IN} = 100mV$, OD = 5mV (Note 4)	 ●		12	16 18	ns ns
t_{PD}	Propagation Delay	$\Delta V_{IN} = 100mV$, OD = 20mV (Note 4)	 ●		10	14 16	ns ns
Δt_{PD}	Differential Propagation Delay	$\Delta V_{IN} = 100mV$, OD = 5mV (Note 4)				3	ns
t_{SU}	Latch Set-Up Time	(Note 5)			2		ns
t_H	Latch Hold Time	(Note 5)			2		ns

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impared.

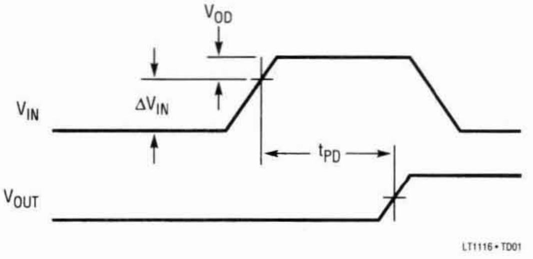
Note 2: Input offset voltage is defined as the average of two offset voltages measured by forcing first the Q output to 1.4V then forcing the $\overline{Q}$ output to 1.4V.

Note 3: Input bias current is defined as the average of the two input currents.

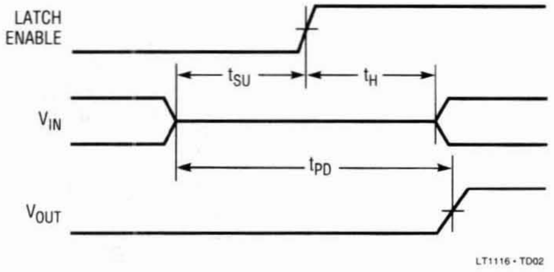
Note 4: t_{PD} and Δt_{PD} cannot be measured in automatic handling equipment with low values of overdrive. The LT1116 is sample tested with a 1V step and 500mV overdrive. Correlation tests have shown that t_{PD} and Δt_{PD} can be guaranteed with this test if additional DC tests are performed to verify internal bias conditions are correct. For low overdrive conditions V_{OS} is added to the measured overdrive.

Note 5: Input latch set-up time, t_{SU}, is the interval in which the input signal must be stable prior to asserting the latch signal. The hold time, t_H, is the interval after the latch is asserted in which the input signal must be stable.

TIMING DIAGRAMS



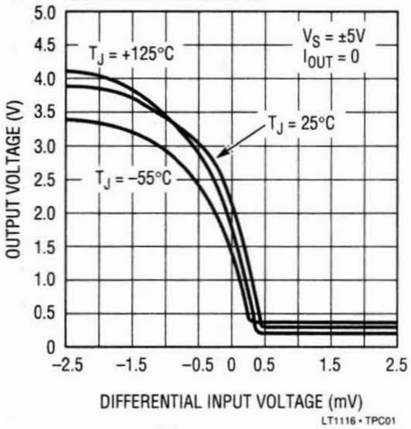
LT1116 • TD01



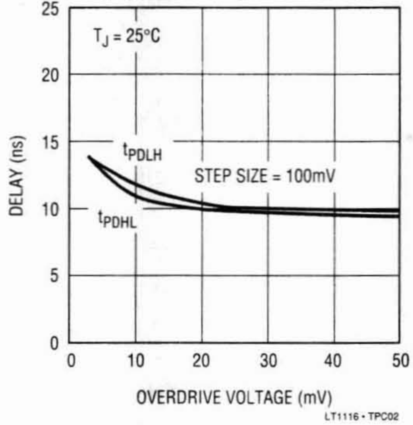
LT1116 • TD02

TYPICAL PERFORMANCE CHARACTERISTICS

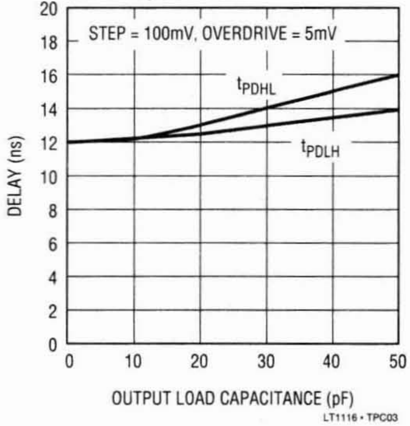
Gain Characteristics



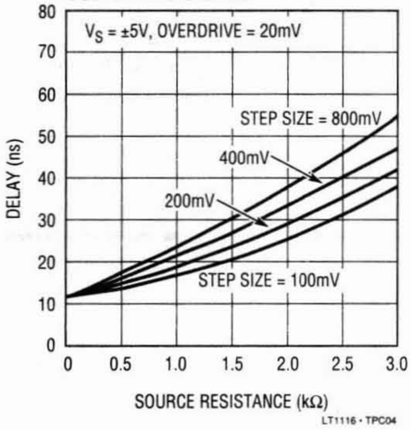
Propagation Delay vs Overdrive



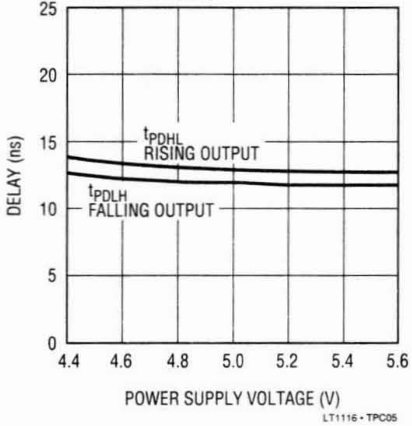
Propagation Delay vs Load Capacitance



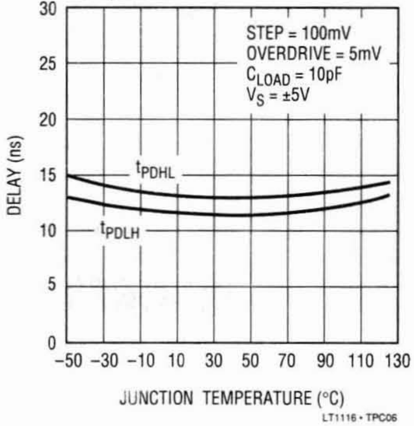
Propagation Delay vs Source Resistance



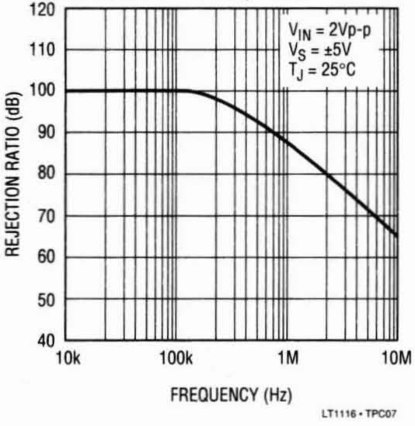
Propagation Delay vs Positive Supply



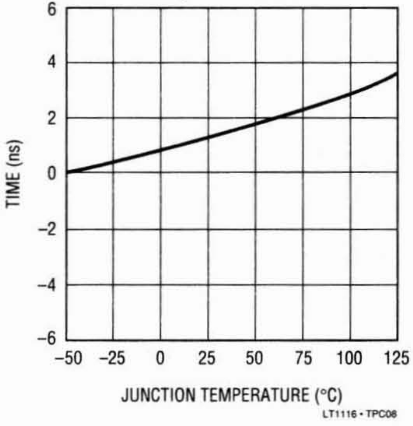
Propagation Delay vs Temperature



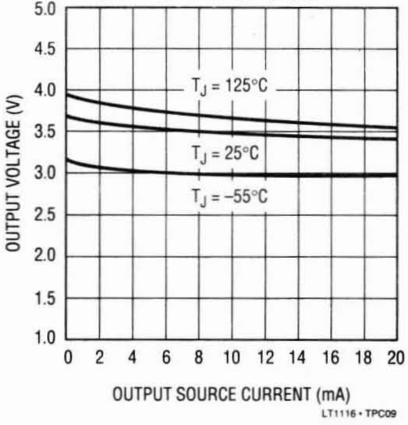
Common Mode Rejection



Latch Set-Up Time

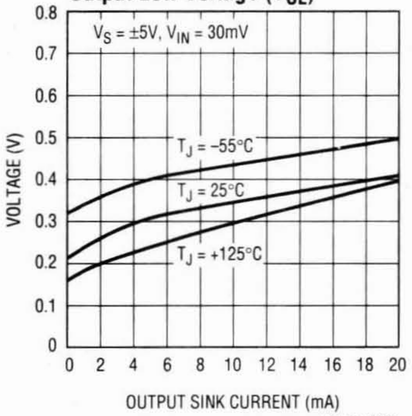


Output High Voltage (V_{OH})



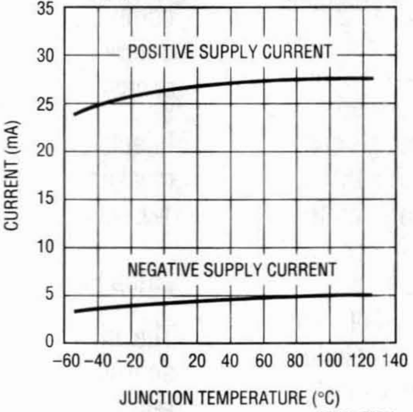
TYPICAL PERFORMANCE CHARACTERISTICS

Output Low Voltage (V_{OL})



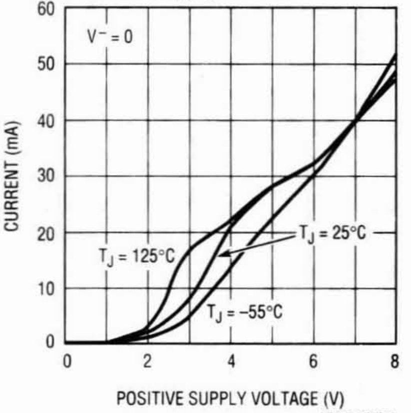
LT1116 • TPC10

Supply Current vs Temperature



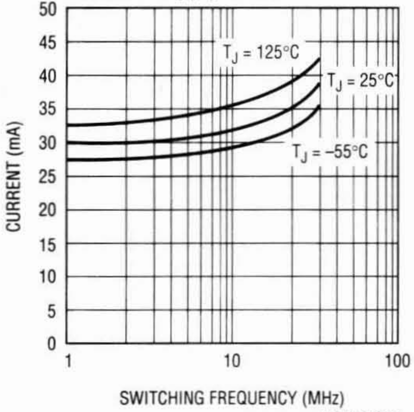
LT1116 • TPC11

Positive Supply Current



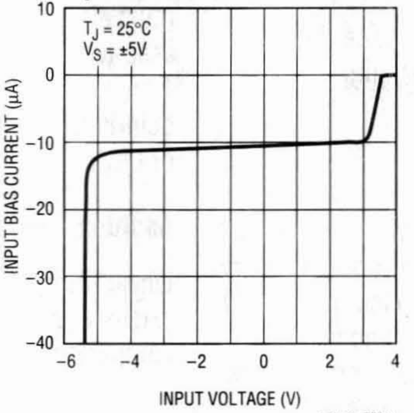
LT1116 • TPC12

Positive Supply Current



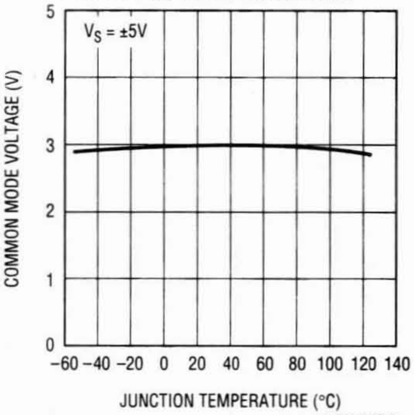
LT1116 • TPC13

Input Bias Current



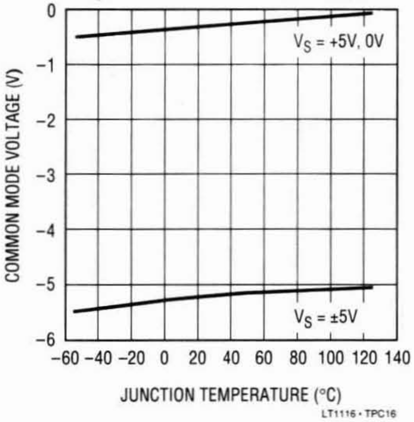
LT1116 • TPC14

Positive Common Mode Limit



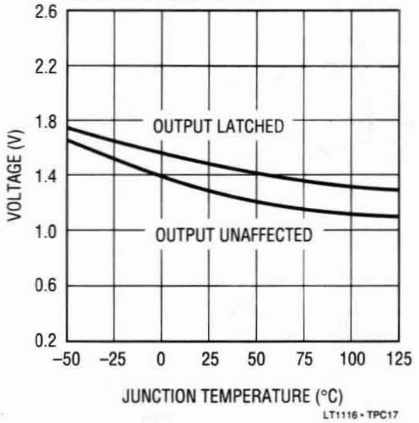
LT1116 • TPC15

Negative Common Mode Limit



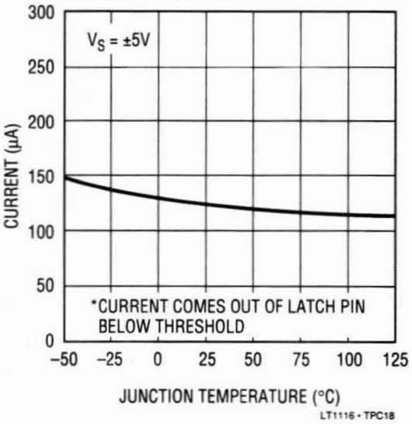
LT1116 • TPC16

Latch Pin Threshold



LT1116 • TPC17

Latch Pin Current*



LT1116 • TPC18

APPLICATIONS INFORMATION

Common Mode Considerations

The LT1116 is specified for a common mode range of 0V to 2.5V with a single +5V supply, and –5V to 2.5V with ±5V supplies. The common mode range is defined as the DC input for which the output responds correctly to small changes in the input differential. Input signals can exceed the positive common mode limit up to the 15V absolute maximum rating without damaging the comparator. There will, however, be an increase in propagation delay of up to 10ns when the input signal switches back into the common mode range. When input signals fall below the negative common mode limit, the internal PN diode formed with the substrate can turn on resulting in significant charge flow throughout the die. A Schottky clamp diode between the input and the negative rail speeds up recovery from negative overdrive by preventing the substrate diode from turning on. The zero crossing detector in Figure 1 demonstrates the use of a fast clamp diode. Recovery from 500mV overdrive below V^- for this circuit is approximately 18ns.

Input Characteristics

Each input to the LT1116 is buffered with a fast PNP follower — input bias current therefore does not vary significantly throughout the common mode range. When either input exceeds the positive common mode limit, the bias current drops to zero. Inputs that fall more than one diode drop below V^- will forward bias the substrate or clamp diode, and will cause large input current to flow.

Fast Zero Crossing Detector

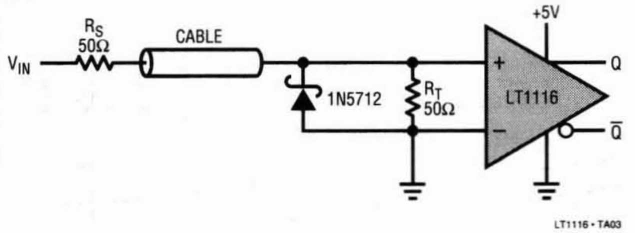


Figure 1. The zero crossing detector terminates the transmission line at its 50Ω characteristic impedance. Negative inputs should not fall below –2V to keep the signal current within the clamp diode's maximum forward rating. Positive inputs should not exceed the devices absolute maximum ratings nor the power rating on the terminating resistor.

Single ended input resistance is about 5MΩ, and remains roughly constant over the input common mode range. The common mode resistance is about 2.5MΩ with zero differential input voltage, and does not change significantly with the absolute value of differential input.

Effective input capacitance, typically 5pF, is determined by measuring the resulting change in propagation delay for a 1kΩ change in source resistance.

Latch Pin Dynamics

The internal latch uses local regenerative feedback to shorten set-up and hold times. Driving the latch pin high retains the output state. The latch pin floats to a high state when disconnected, so it must be driven low for flow-through operation. The set-up time required to guarantee detecting a given transition of the inputs is 2ns. The inputs must also remain stable for a 2ns hold time after latch is asserted. New data will appear at the output approximately 10ns to 12ns after the latch goes low. The latch pin has no built-in hysteresis, and is designed to be driven from TTL or CMOS logic gates.

Additional Information

Linear Technology's Application Note 13 provides an extensive discussion of design techniques for high speed comparators.

Single Supply Crystal Oscillator 10MHz-15MHz

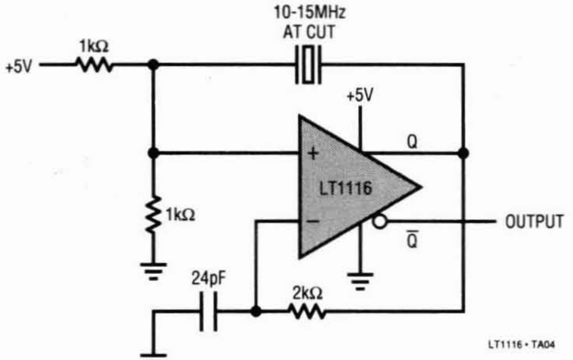


Figure 2. This single supply crystal oscillator utilizes crystals from 10MHz to 15MHz without component changes.

APPLICATIONS INFORMATION

High Speed Adaptive Trigger Circuit

Line receivers often require an adaptive trigger to compensate for variations in signal amplitude and DC offsets. The circuit in Figure 3 triggers on 2mV to 200mV signals from 100Hz to 10MHz from a single 5V rail. The trigger level is the average of the input signal's positive and negative peaks stored on 0.005µF capacitors. Pairs of NPN and PNP transistors are used instead of diodes to temperature compensate the peak detector.

To achieve single supply operation, the input signal must be shifted into the pre-amplifier's common mode range. The input amplifier A1, adds a 1V level shift, while A2 provides a gain of 20 for high frequency signals. Capacitors C1 and C2 insure that low frequency signals see unity gain. Bandwidth limiting in A1 and A2 does not affect triggering because the adaptive trigger threshold varies ratiometrically to maintain circuit output.

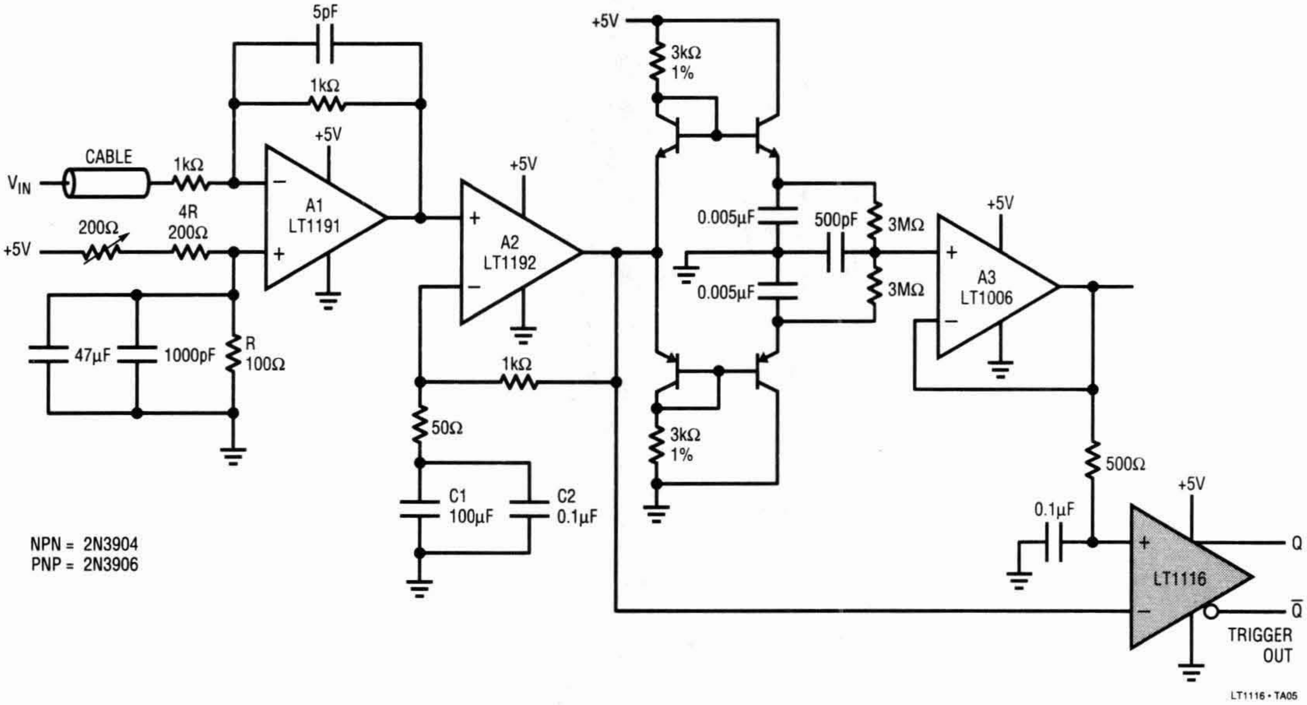

5pF
1kΩ
+5V
CABLE
1kΩ
V_IN
4R
200Ω
200Ω
+5V
A1
LT1191
47µF
1000pF
R
100Ω
+5V
A2
LT1192
1kΩ
50Ω
C1
100µF
C2
0.1µF
+5V
3kΩ
1%
0.005µF
500pF
3MΩ
0.005µF
3MΩ
3kΩ
1%
+5V
A3
LT1006
500Ω
+5V
0.1µF
LT1116
Q
Q̄
TRIGGER
OUT
NPN = 2N3904
PNP = 2N3906
LT1116 • TA05

Figure 3. Fast Single Supply Adaptive Trigger

NOTES

SECTION 11— SPECIAL FUNCTION

11

SECTION 11—SPECIAL FUNCTION

INDEX **11-2**
SELECTION GUIDE **11-3**
PROPRIETARY PRODUCTS
LTC201A/LTC202/LTC203, Micropower, Low Charge Injection, Quad CMOS Analog Switches **11-4**
LTC221/LTC222, Micropower, Low Charge Injection, Quad CMOS Analog Switches with Data Latches **11-15**

ANALOG SWITCHES

FAMILY FEATURES

- Micropower: 40µA Max Supply Current
- Single 5V or ±15V Operation
- 8pC Charge Injection
- Low ON Resistance
- Low Leakage
- Guaranteed Break Before Make

PART NUMBER	NUMBER OF CHANNELS	LATCHED INPUTS	MAX ON RESISTANCE	MAX INPUT AND OUTPUT OFF LEAKAGE	MAX SUPPLY CURRENT	MAX T_{ON}/T_{OFF}	FEATURES
LTC201A	4		125Ω	5nA	40µA	400ns/300ns	Lower ON Resistance, Charge Injection, Supply Current Than DG201A. Single 5V to ±15V Supply Operation
LTC202	4		125Ω	5nA	40µA	400ns/300ns	Lower ON Resistance, Charge Injection, Supply Current Than DG202. Single 5V to ±15V Supply Operation
LTC203	4		125Ω	5nA	40µA	400ns/300ns	Low ON Resistance, Charge Injection, Supply Current
LTC221	4	X	90Ω	5nA	40µA	400ns/300ns	Lower Charge Injection, Supply Current Than DG221
LTC222	4	X	90Ω	5nA	40µA	400ns/300ns	Lower Charge Injection, Supply Current Than DG222

OTHER PRODUCTS

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LF198(A)/LF398(A)	Sample and Hold Amplifier	H, J8, N8, S	12-Bit Accurate (LF198A), 6µs Acquisition Time, 0.005% Max Gain Error.
LM134/LM334	Adjustable Current Source	H, Z, S8	1µA to 10mA Adjustment Range, Floating Current Source, 0.02%/Volt Regulation, Can Be Used as Temperature Sensor.
LT1025	Thermocouple Cold Junction Compensator	J8, N8	Provides 0°C Cold Junction Compensation of Types E, J, K, R, S, T Thermocouples. Low Supply Current (80µA) and Operates with Single +4V to +36V DC Supply.
LT1088	RMS to DC Converter	D, N	Thermal RMS to DC Conversion Permits 1% Accuracy to 50MHz, 2% to 100MHz and Handles Crest Factors up to 50:1.
LTC1043	Precision Switched-Capacitor Building Block	D, N, S	120dB CMRR, when Used as Instrumentation Front End, Allows Switched-Capacitor Design Techniques at Board Level.
LTK001	Thermocouple Cold Junction Compensator with Matched Amplifier	J, N	LT1025 with Matched Amplifier (LTKA00 or LTKA01) Provides Lower Error Specs than using Worst-Case Errors of LT1025 and Standard Precision Op Amp.

LINEAR TECHNOLOGY

LTC201A/LTC202/LTC203

Micropower, Low Charge Injection, Quad CMOS Analog Switches

FEATURES

- Micropower Operation
- Single 5V or ± 15V Supply Operation
- Low Charge Injection
- Low R_{ON}
- Low Leakage
- Guaranteed Break Before Make
- Latch Resistant Design
- TTL/CMOS Compatible
- Improved Second Source for DG201A/DG202

KEY SPECIFICATIONS

■ Supply Current		$I^+ = 40\mu A$, $I^- = 5\mu A$ Max.
■ Charge Injection	(± 15V Supplies)	± 25pC Max.
	(Single 5V Supply)	2pC Typ.
■ R_{ON}		65Ω Typ.
■ Signal Range		± 15V

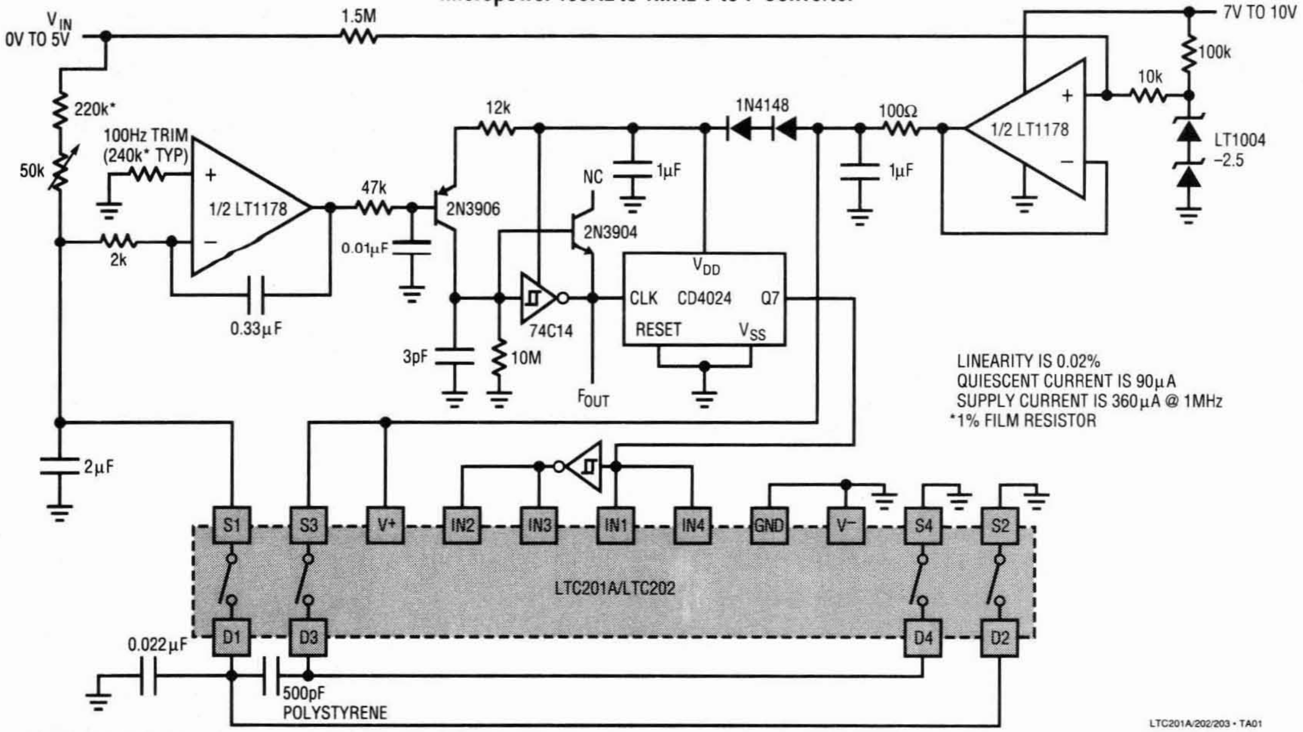
DESCRIPTION

The LTC201A, LTC202, and LTC203 are micropower, quad CMOS analog switches which typically dissipate only 250µW from ±15V supplies and 40µW from a single 5V supply. The switches have 65Ω typical on resistance and a very high off resistance. A break before make characteristic, inherent in these switches, prevents the shorting of two channels. With a supply voltage of ±15V, the signal range is ±15V. These switches have special charge compensation circuitry which greatly reduces charge injection to a maximum of ± 25pC (±15V supplies).

The LTC201A, LTC202, and LTC203 are designed for applications such as programmable gain amplifiers, analog multiplexers, sample and hold circuits, precision charge switching and remote switching. These three devices are differentiated by the type of switch action, as shown in the logic table.

TYPICAL APPLICATION

Micropower 100Hz to 1MHz V-to-F Converter



V_{IN}
0V TO 5V
1.5M
7V TO 10V
100k
10k
+
1/2 LT1178
−
LT1004
−2.5
100Ω
1µF
1N4148
12k
1µF
NC
220k*
100Hz TRIM
(240k* TYP)
50k
+
1/2 LT1178
−
47k
2N3906
2N3904
0.01µF
2k
0.33µF
V_{DD}
CLK
CD4024
Q7
RESET
V_{SS}
74C14
3pF
10M
F_{OUT}
2µF
S1
S3
V+
IN2
IN3
IN1
IN4
GND
V−
S4
S2
LTC201A/LTC202
D1
D3
D4
D2
0.022µF
500pF
POLYSTYRENE

LINEARITY IS 0.02%
QUIESCENT CURRENT IS 90µA
SUPPLY CURRENT IS 360µA @ 1MHz
*1% FILM RESISTOR

LTC201A/202/203 • TA01

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Voltages Referenced to V^-

V^+ 44V

GND 25V

Digital Inputs, S,D (Note 2) .... −2V to (V^++2V) or 20mA, Whichever Occurs First

Current

Any Input Except S or D 30mA

Continuous S or D 20mA

Peaks S or D (Pulsed at 1ms, 10% Duty Cycle Max). 70mA

ESD Susceptibility (Note 3) 4kV

Power Dissipation (Plastic) 500mW

Power Dissipation (Ceramic) 900mW

Operating Temperature Range

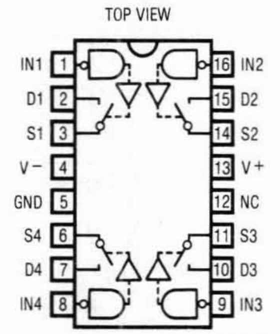
LTC201AC/LTC202C/LTC203C .... 0°C to 70°C

LTC201AM/LTC202M/LTC203M ..... −55°C to 125°C

Storage Temperature Range .... −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
16-LEAD CERAMIC DIP

N PACKAGE
16-LEAD PLASTIC DIP

SO PACKAGE
16-LEAD PLASTIC SOIC

ORDER PART NUMBER
LTC201AMJ
LTC201ACJ
LTC201ACN
LTC201ACS
LTC202MJ
LTC202CJ
LTC202CN
LTC202CS
LTC203MJ
LTC203CJ
LTC203CN
LTC203CS

LOGIC TABLE

	LTC201A	LTC202	LTC203	
IN_X	IN1-IN4	IN1-IN4	IN1,IN4	IN2,IN3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V^- = -15V$, GND = 0V unless otherwise noted.

				LTC201AM/LTC202M/LTC203M			LTC201AC/LTC202C/LTC203C			
PARAMETER	CONDITIONS			MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Analog Signal Range			●			±15			±15	V
R_{ON}	$V_S = \pm10V$	T_{MIN}				110			125	Ω
	$I_D = 1mA$	25°C			65	110		65	125	
		T_{MAX}				160			160	
ΔR_{ON} vs V_S					20			20		%
ΔR_{ON} vs Temperature					0.5			0.5		%/°C
R_{ON} Match	$V_S = 0V$, $I_{DS} = 1mA$				5			5		%
Off Input Leakage I_S(OFF)	$V_D = \pm14V$, $V_S = \mp14V$				0.01	±1		0.01	±5	nA
	Switch Off		●			±100			±100	
Off Output Leakage I_D(OFF)	$V_D = \pm14V$, $V_S = \mp14V$				0.01	±1		0.01	±5	nA
	Switch Off		●			±100			±100	
On Channel Leakage I_D(ON)	$V_D = V_S = \pm14V$				0.02	±1		0.02	±5	nA
	Switch On		●			±200			±200	
Input High Voltage V_{INH}			●	2.4			2.4			V
Input Low Voltage V_{INL}			●			0.8			0.8	V
Input High or Low Current I_{INH} and I_{INL}	$V_{IN} = 15V, 0V$		●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V^- = -15V$, GND = 0V unless otherwise noted.

			LTC201AM/LTC202M/LTC203M			LTC201AC/LTC202C/LTC203C			
PARAMETER	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
C_S(OFF)				5			5		pF
C_D(OFF)				12			12		pF
C_D, C_S(ON)				30			30		pF
I^+	All Logic Inputs Tied Together V_{IN} = 0V or 4.0V		16		40		16	40	µA
		●			60			60	
I^-				0.1	5		0.1	5	
		●			10			10	

AC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V^- = -15V$, GND = 0V unless otherwise noted.

		LTC201AM/LTC202M/LTC203M			LTC201AC/LTC202C/LTC203C			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
T_{ON}	V_S = 2V, R_L = 1kΩ, C_L = 35pF		290	400		290	400	ns
T_{OFF}			210	300		210	300	
T_{OPEN}		20	85		20	85		ns
Off Isolation	V_S = 2Vp-p, R_L = 1kΩ, f = 100kHz		75			75		dB
Crosstalk			90			90		
Charge Injection Q_{INJ}	R_S = 0Ω, C_L = 1000pF, V_S = 0V		5	±25		8	±25	pC
Total Harmonic Distortion THD	V_S = 2Vp-p, R_L = 10kΩ		0.01			0.01		%

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

$V^+ = +5V$, $V^- =$ GND = 0V unless otherwise noted.

				LTC201AM/LTC202M/LTC203M			LTC201AC/LTC202C/LTC203C			
PARAMETER	**CONDITIONS**			**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Analog Signal Range			●	0		5	0		5	V
R_{ON}	V_S = +1.5V, +3V	T_{MIN}				450			520	Ω
	I_D = 0.25mA	25°C			280	450		280	525	
		T_{MAX}				650			650	
ΔR_{ON} vs V_S					20			20		%
ΔR_{ON} vs Temperature					0.5			0.5		%/°C
R_{ON} Match	V_S = 2.5V, I_{DS} = 0.25mA				5			5		%
Off Input Leakage I_S(OFF)	V_D = 4V, 1V; V_S = 1V, 4V (Note 4)				0.01	±1		0.01	±5	nA
	Switch Off		●			±100			±100	
Off Output Leakage I_D(OFF)	V_D = 4V, 1V; V_S = 1V, 4V (Note 4)				0.01	±1		0.01	±5	nA
	Switch Off		●			±100			±100	
On Channel Leakage I_D(ON)	V_D = V_S = 1V, 4V (Note 4)				0.01	±1		0.01	±5	nA
	Switch On		●			±200			±200	
Input High Voltage V_{INH}			●	2.4			2.4			V
Input Low Voltage V_{INL}			●			0.8			0.8	V
Input High or Low Current I_{INH} and I_{INL}	V_{IN} = 5V, 0V		●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

$V^+ = +5V$, $V^- = GND = 0V$ unless otherwise noted.

PARAMETER	CONDITIONS		LTC201AM/LTC202M/LTC203M MIN	TYP	MAX	LTC201AC/LTC202C/LTC203C MIN	TYP	MAX	UNITS
C_S(OFF)				5			5		pF
C_D(OFF)				12			12		pF
C_D, C_S(ON)				30			30		pF
I^+	All Logic Inputs Tied Together			8	20		8	20	μA
	V_{IN} = 0V or 4.0V	●			30			30	

AC ELECTRICAL CHARACTERISTICS

$V^+ = +5V$, $V^- = GND = 0V$ unless otherwise noted.

PARAMETER	CONDITIONS	LTC201AM/LTC202M/LTC203M MIN	TYP	MAX	LTC201AC/LTC202C/LTC203C MIN	TYP	MAX	UNITS
T_{ON}	$V_S = 2V$, $R_L = 1k\Omega$, $C_L = 35pF$		450	600		450	600	ns
T_{OFF}			190	300		190	300	
T_{OPEN}		100	250		100	250		ns
Off Isolation	$V_S = 2Vp\text{-}p$, $R_L = 1k\Omega$, f = 100kHz		75			75		dB
Crosstalk			90			90		
Charge Injection Q_{INJ}	$R_S = 0\Omega$, $C_L = 1000pF$, $V_S = 2.5V$		2			2		pC
Total Harmonic Distortion THD	$V_S = 2Vp\text{-}p$, $R_L = 10k\Omega$		0.01			0.01		%

The ● denotes the specifications which apply over full operating temperature range. All other limits and typicals $T_A = 25°C$.

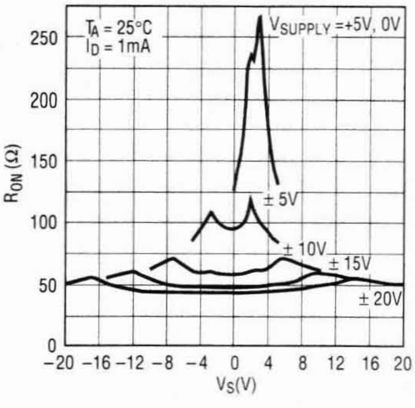
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Signals on S, D, or IN exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current rating.

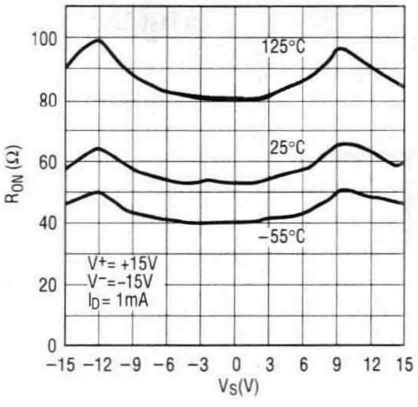
Note 3: In-circuit ESD on the switch pins (S or D) exceeds 4kV (see test circuit).

Note 4: Leakage current with a single 5V supply is guaranteed by correlation with the ±15V leakage current.

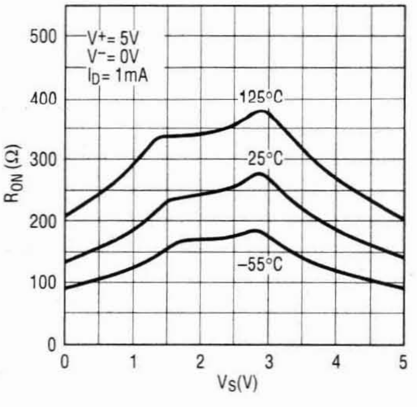
TYPICAL PERFORMANCE CHARACTERISTICS



R_{ON} vs V_S Over Supply Voltage



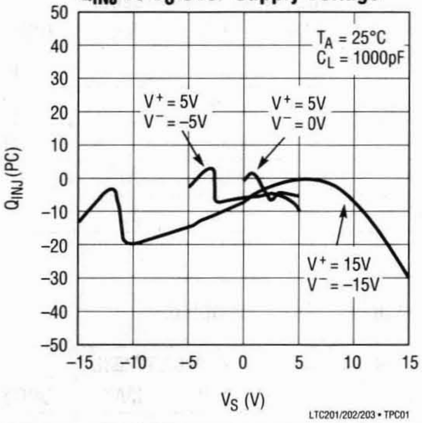
R_{ON} vs V_S Over Temperature



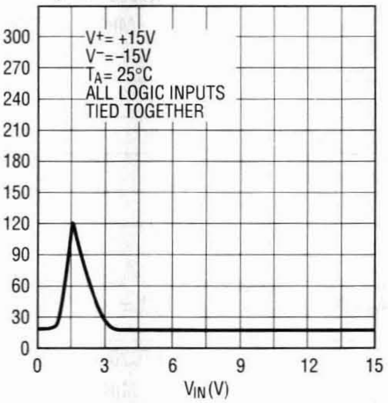
R_{ON} vs V_S Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

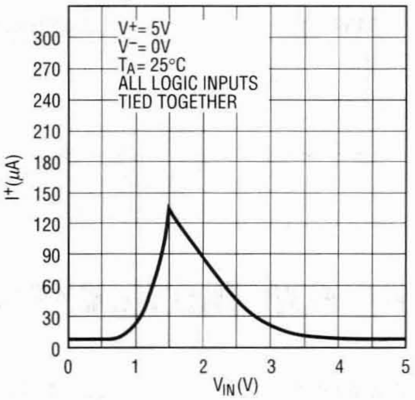
Q_{INJ} vs V_S Over Supply Voltage



Positive Supply Current vs Logic Input Voltage



Supply Current vs Logic Input Voltage

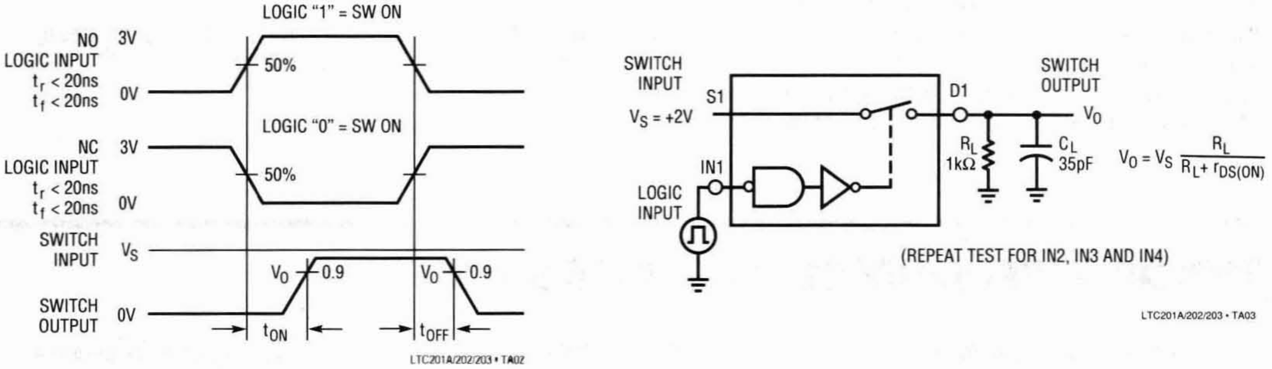


APPLICATIONS INFORMATION

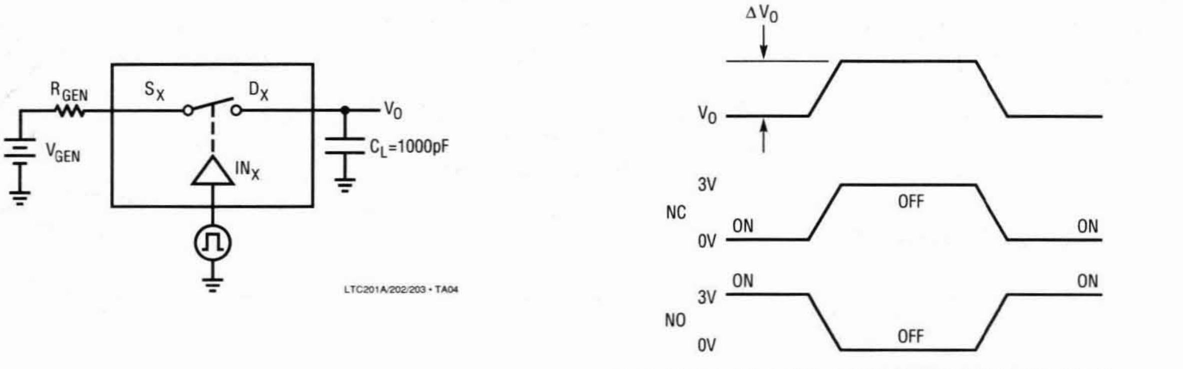
Switching Time Test Circuit

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

Switching Time Test Circuit


LOGIC "1" = SW ON
NO
LOGIC INPUT
t_r < 20ns
t_f < 20ns
3V
0V
50%
LOGIC "0" = SW ON
NC
LOGIC INPUT
t_r < 20ns
t_f < 20ns
3V
0V
50%
SWITCH
INPUT
V_S
SWITCH
OUTPUT
0V
V_O
0.9
V_O
0.9
t_{ON}
t_{OFF}
LTC201A/202/203 • TA02
SWITCH
INPUT
V_S = +2V
S1
D1
SWITCH
OUTPUT
V_O
IN1
R_L
1kΩ
C_L
35pF
LOGIC
INPUT
$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$
(REPEAT TEST FOR IN2, IN3 AND IN4)
LTC201A/202/203 • TA03

Charge Injection Test Circuit

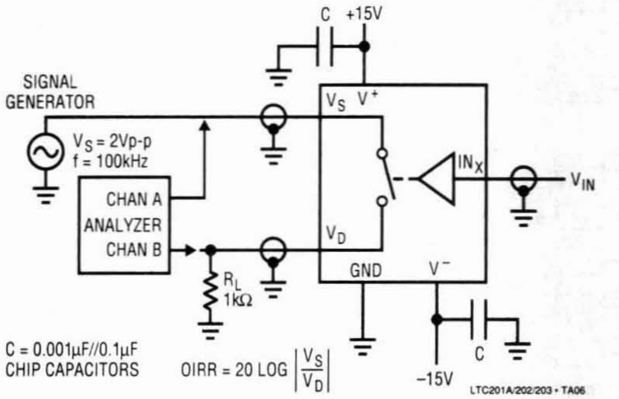

R_{GEN}
S_X
D_X
V_O
V_{GEN}
IN_X
C_L=1000pF
LTC201A/202/203 • TA04
ΔV_O
V_O
3V
NC
0V
ON
OFF
ON
3V
NO
0V
ON
ON
OFF

ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION.
THE ERROR VOLTAGE IN COULOMBS IS $\Delta Q = C_L \times \Delta V_O$.

LTC201A/202/203 • TA05

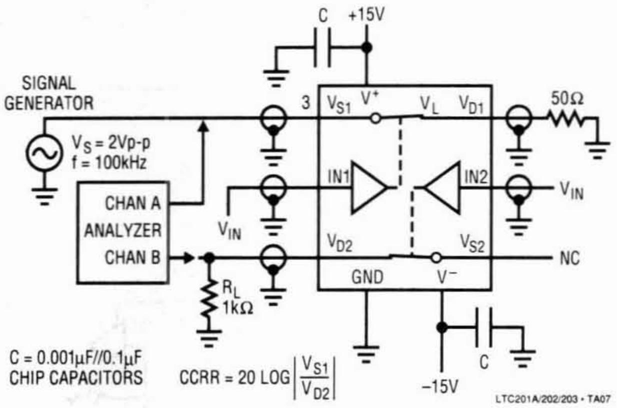
APPLICATIONS INFORMATION

OIRR-Off Isolation Test Circuit


C
+15V
SIGNAL GENERATOR
V_S = 2Vp-p
f = 100kHz
CHAN A
ANALYZER
CHAN B
V_S
V^+
IN_X
V_{IN}
V_D
GND
V^-
R_L 1kΩ
C = 0.001µF//0.1µF
CHIP CAPACITORS
OIRR = 20 LOG $\left|\frac{V_S}{V_D}\right|$
C
–15V
LTC201A/202/203 • TA06

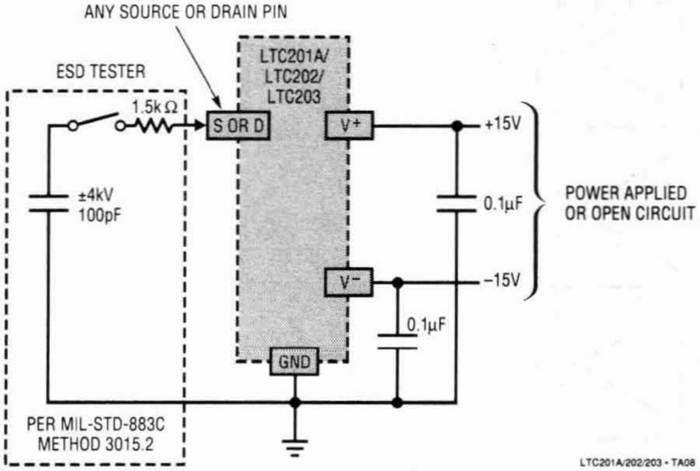
V_{IN}	
3V	NC
0V	NO

CCRR-Channel to Channel Crosstalk Test Circuit

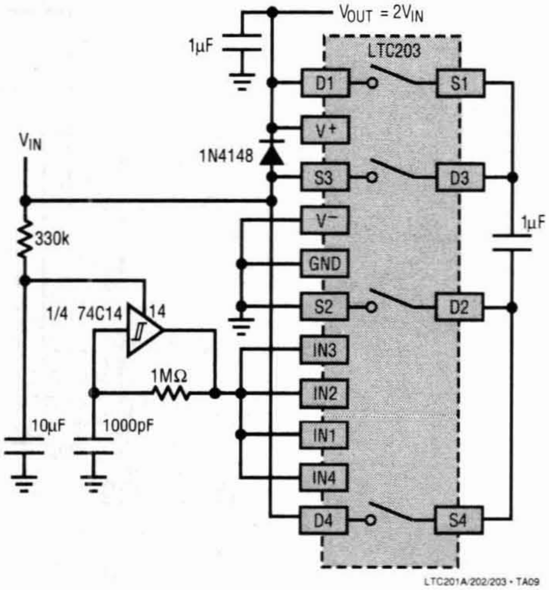

C
+15V
SIGNAL GENERATOR
V_S = 2Vp-p
f = 100kHz
CHAN A
ANALYZER
CHAN B
3
V_{S1}
V^+
V_L
V_{D1}
50Ω
IN1
IN2
V_{IN}
V_{IN}
V_{D2}
V_{S2}
NC
GND
V^-
R_L 1kΩ
C = 0.001µF//0.1µF
CHIP CAPACITORS
CCRR = 20 LOG $\left|\frac{V_{S1}}{V_{D2}}\right|$
C
–15V
LTC201A/202/203 • TA07

V_{IN}	
3V	NC
0V	NO

In-Circuit ESD Test Circuit


ANY SOURCE OR DRAIN PIN
ESD TESTER
1.5kΩ
S OR D
LTC201A/
LTC202/
LTC203
V+
+15V
±4kV
100pF
0.1µF
POWER APPLIED
OR OPEN CIRCUIT
V–
–15V
0.1µF
GND
PER MIL-STD-883C
METHOD 3015.2
LTC201A/202/203 • TA08

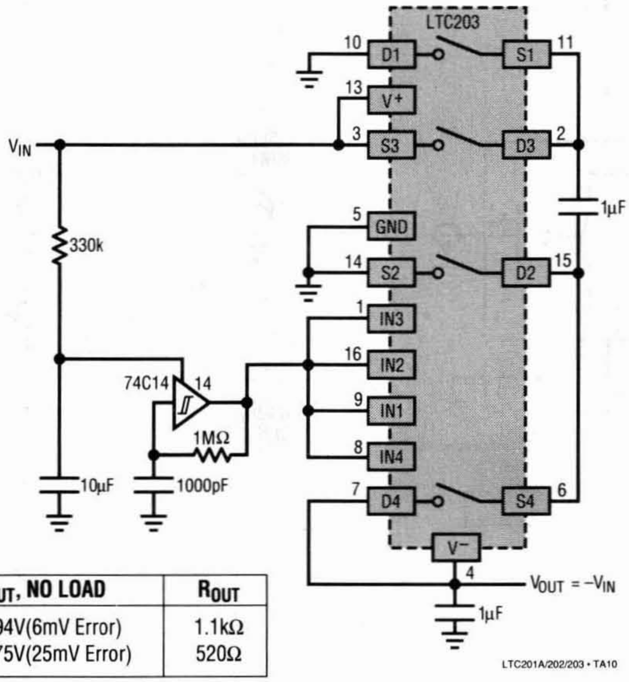
Micropower, 4.5V–15V Input, Voltage Doubler Using the LTC203


V_{OUT} = $2V_{IN}$
1µF
LTC203
D1
S1
V+
1N4148
V_{IN}
S3
D3
V–
1µF
330k
GND
1/4 74C14
14
S2
D2
IN3
1MΩ
IN2
10µF
1000pF
IN1
IN4
D4
S4
LTC201A/202/203 • TA09

V_{IN}	I_Q	V_{OUT}, NO LOAD	R_{OUT}
4.5V	20µA	8.988V(12mV Error)	1.2k
15V	130µA	29.96V(40mV Error)	600Ω

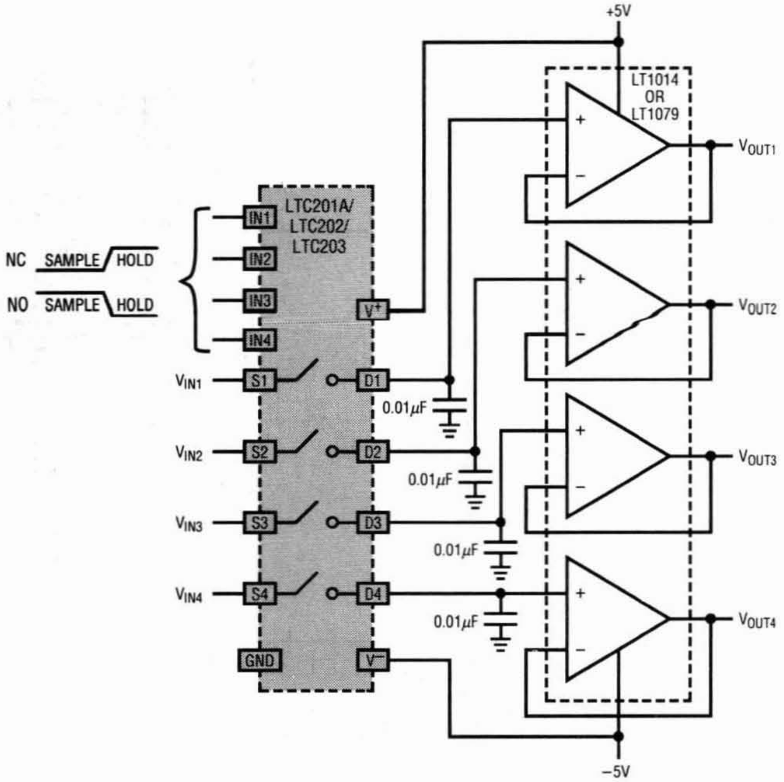
APPLICATIONS INFORMATION

Micropower, ±4.5V – ±15V, Voltage Inverter Using the LTC203


LTC203
10
D1
S1
11
13
V+
3
S3
D3
2
V_{IN}
1µF
5
GND
330k
14
S2
D2
15
1
IN3
16
IN2
74C14
14
9
IN1
1MΩ
8
IN4
10µF
1000pF
7
D4
S4
6
V−
4
$V_{OUT} = -V_{IN}$
1µF
LTC201A/202/203 • TA10

V_{IN}	I_Q	V_{OUT}, NO LOAD	R_{OUT}
4.5V	15µA	−4.494V(6mV Error)	1.1kΩ
15V	125µA	−14.975V(25mV Error)	520Ω

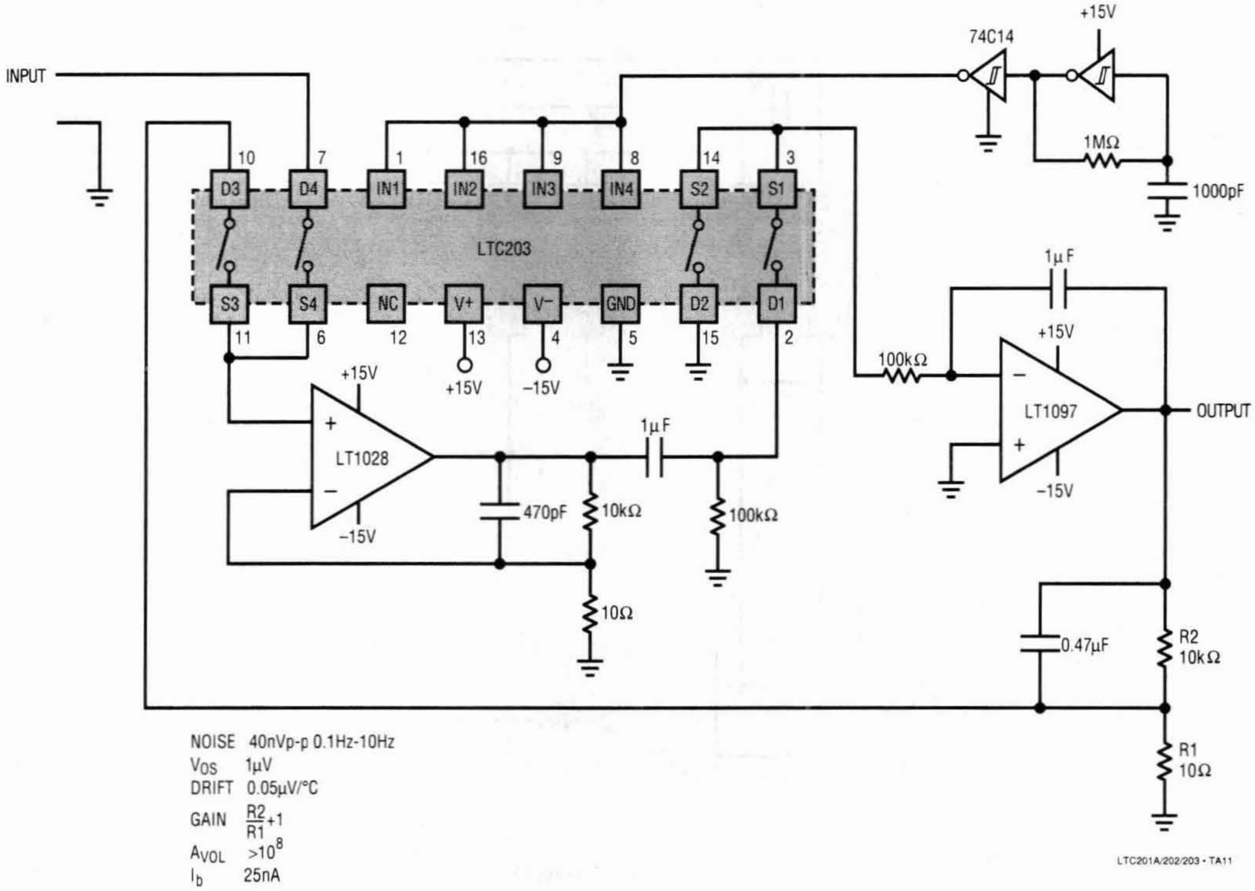
Quad 12-Bit Sample and Hold


+5V
LT1014
OR
LT1079
+
−
V_{OUT1}
V_{OUT2}
V_{OUT3}
V_{OUT4}
LTC201A/
LTC202/
LTC203
IN1
IN2
IN3
IN4
NC SAMPLE HOLD
NO SAMPLE HOLD
V+
V_{IN1}
V_{IN2}
V_{IN3}
V_{IN4}
S1
S2
S3
S4
D1
D2
D3
D4
0.01µF
0.01µF
0.01µF
0.01µF
GND
V−
−5V

	LT1014	LT1079
Sample-to-Hold Offset	0.6mV	0.6mV
Aperture Time	300ns	300ns
Acquisition Time to 0.01% (0 to 2V step)	14µs	27µs
Slew Rate (0 to 5V step)	0.4V/µs	0.07V/µs
Droop Rate	0.8mV/ms	0.6mV/ms
Supply Current	1.6mA	180µA

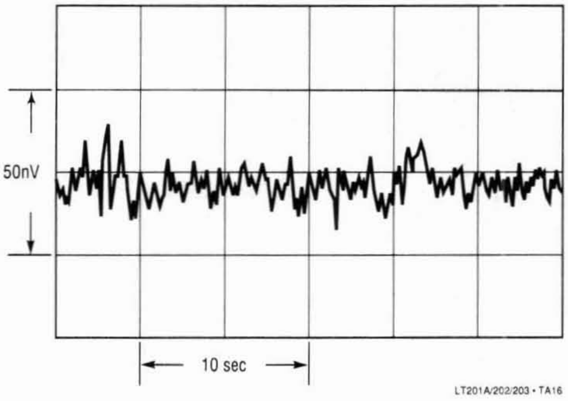
APPLICATIONS INFORMATION

Ultra Low Noise, Low Drift Chopper Amplifier


INPUT
74C14
+15V
1MΩ
1000pF
10
7
1
16
9
8
14
3
D3
D4
IN1
IN2
IN3
IN4
S2
S1
LTC203
S3
S4
NC
V+
V−
GND
D2
D1
11
6
12
13
4
5
15
2
+15V
−15V
1μF
+15V
100kΩ
LT1097
OUTPUT
−15V
+15V
LT1028
−15V
1μF
470pF
10kΩ
100kΩ
10Ω
0.47μF
R2
10kΩ
R1
10Ω
LTC201A/202/203 • TA11

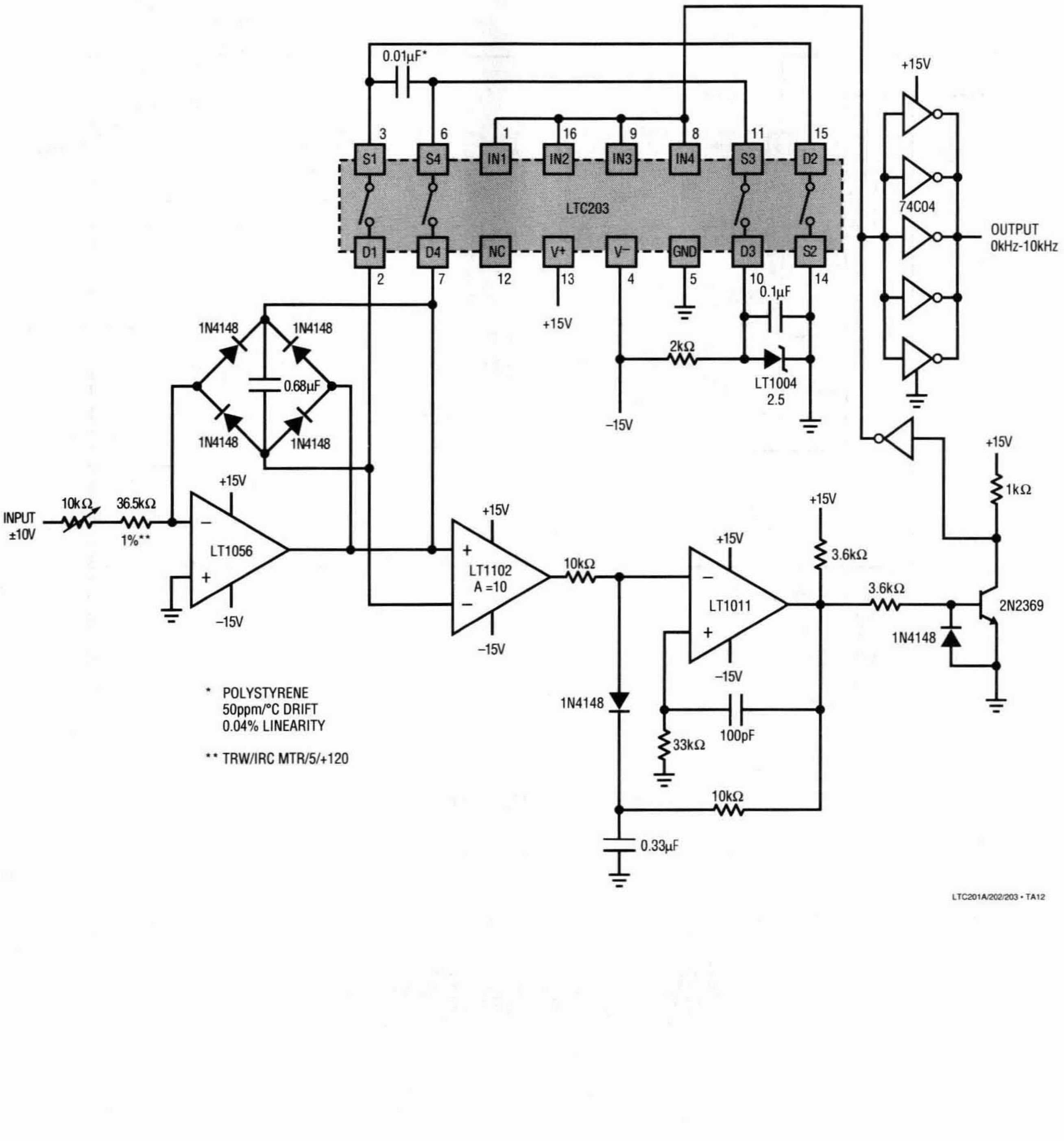
NOISE	40nVp-p 0.1Hz-10Hz
V_{OS}	1μV
DRIFT	0.05μV/°C
GAIN	$\frac{R2}{R1}+1$
A_{VOL}	$>10^8$
I_b	25nA

Noise in a 0.1-10Hz Bandwidth



APPLICATIONS INFORMATION

Bipolar (AC) Input V → F Converter

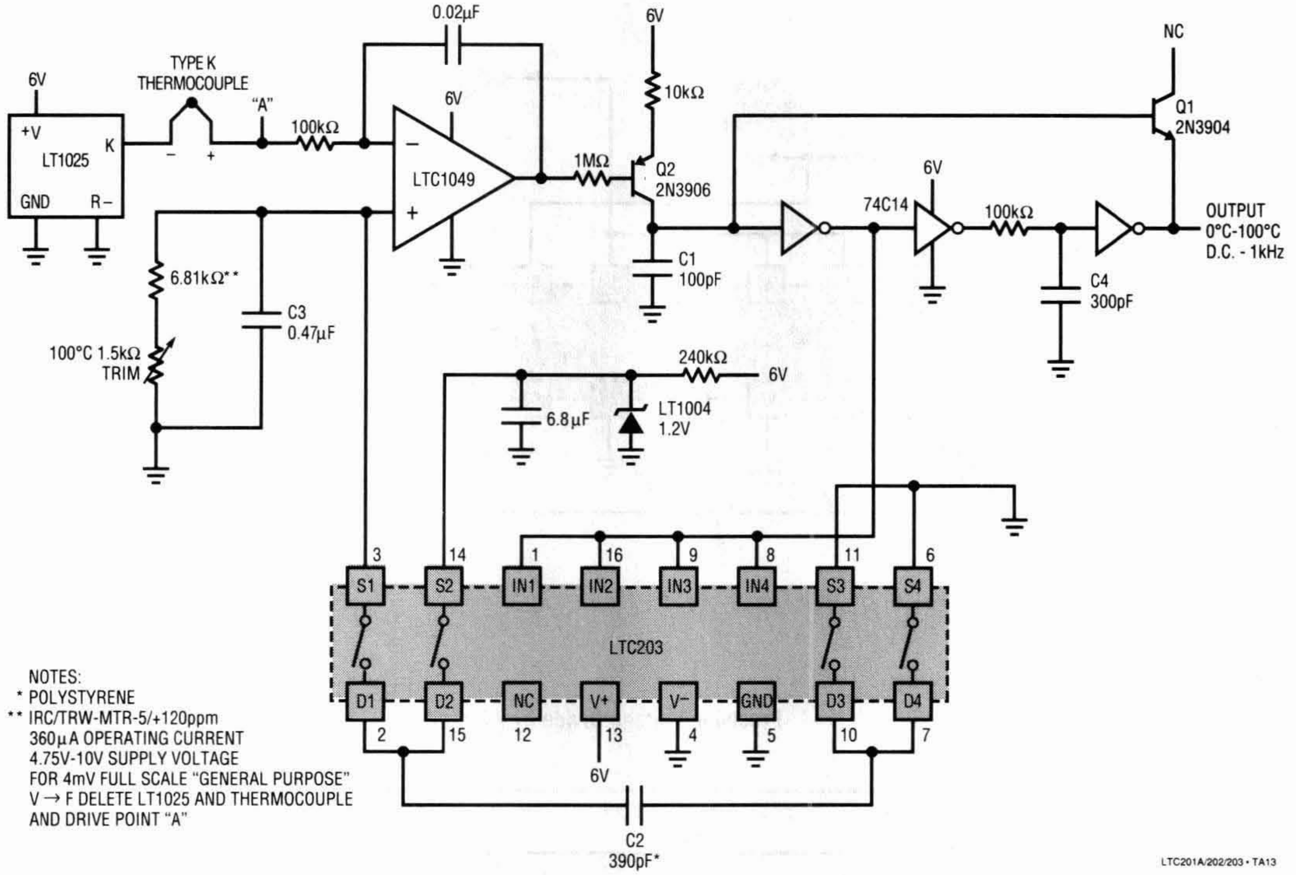

0.01µF*
+15V
3
6
1
16
9
8
11
15
S1
S4
IN1
IN2
IN3
IN4
S3
D2
LTC203
D1
D4
NC
V+
V–
GND
D3
S2
2
7
12
13
4
5
10
14
+15V
0.1µF
2kΩ
LT1004
2.5
–15V
74C04
OUTPUT
0kHz-10kHz
1N4148
1N4148
0.68µF
1N4148
1N4148
INPUT
±10V
10kΩ
36.5kΩ
1%**
+15V
LT1056
–15V
+15V
LT1102
A =10
–15V
10kΩ
+15V
LT1011
–15V
+15V
3.6kΩ
3.6kΩ
2N2369
1N4148
+15V
1kΩ
1N4148
33kΩ
100pF
10kΩ
0.33µF
LTC201A/202/203 • TA12

* POLYSTYRENE
50ppm/°C DRIFT
0.04% LINEARITY

** TRW/IRC MTR/5/+120

APPLICATIONS INFORMATION

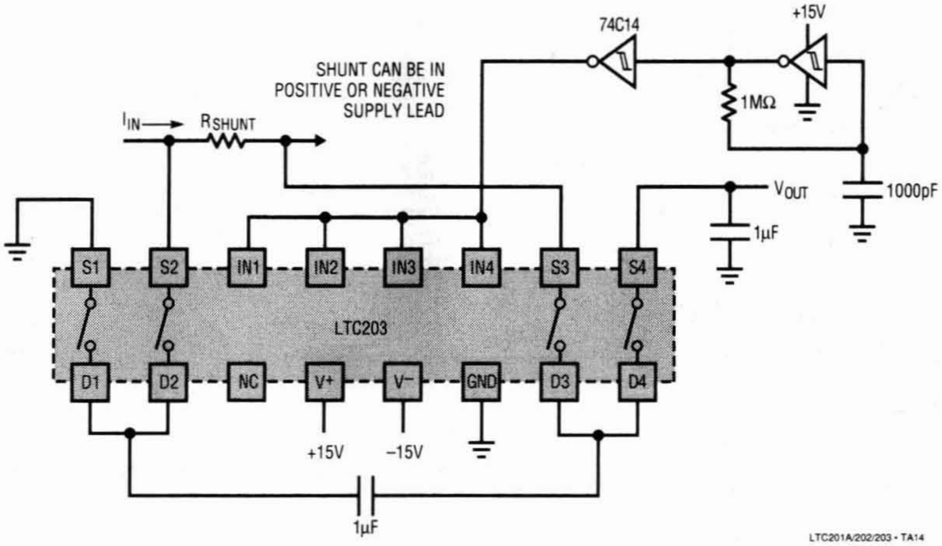
Micropower Thermocouple Temperature to Frequency Converter


0.02µF
6V
NC
TYPE K
THERMOCOUPLE
10kΩ
Q1
2N3904
+V
LT1025
K
GND
R–
"A"
100kΩ
LTC1049
1MΩ
Q2
2N3906
6V
74C14
100kΩ
OUTPUT
0°C-100°C
D.C. - 1kHz
C1
100pF
C4
300pF
6.81kΩ**
C3
0.47µF
100°C 1.5kΩ
TRIM
240kΩ
6.8µF
LT1004
1.2V
3
14
1
16
9
8
11
6
S1
S2
IN1
IN2
IN3
IN4
S3
S4
LTC203
D1
D2
NC
V+
V–
GND
D3
D4
2
15
12
13
4
5
10
7
C2
390pF*
LTC201A/202/203 • TA13

NOTES:
* POLYSTYRENE
** IRC/TRW-MTR-5/+120ppm
360µA OPERATING CURRENT
4.75V-10V SUPPLY VOLTAGE
FOR 4mV FULL SCALE "GENERAL PURPOSE"
V → F DELETE LT1025 AND THERMOCOUPLE
AND DRIVE POINT "A"

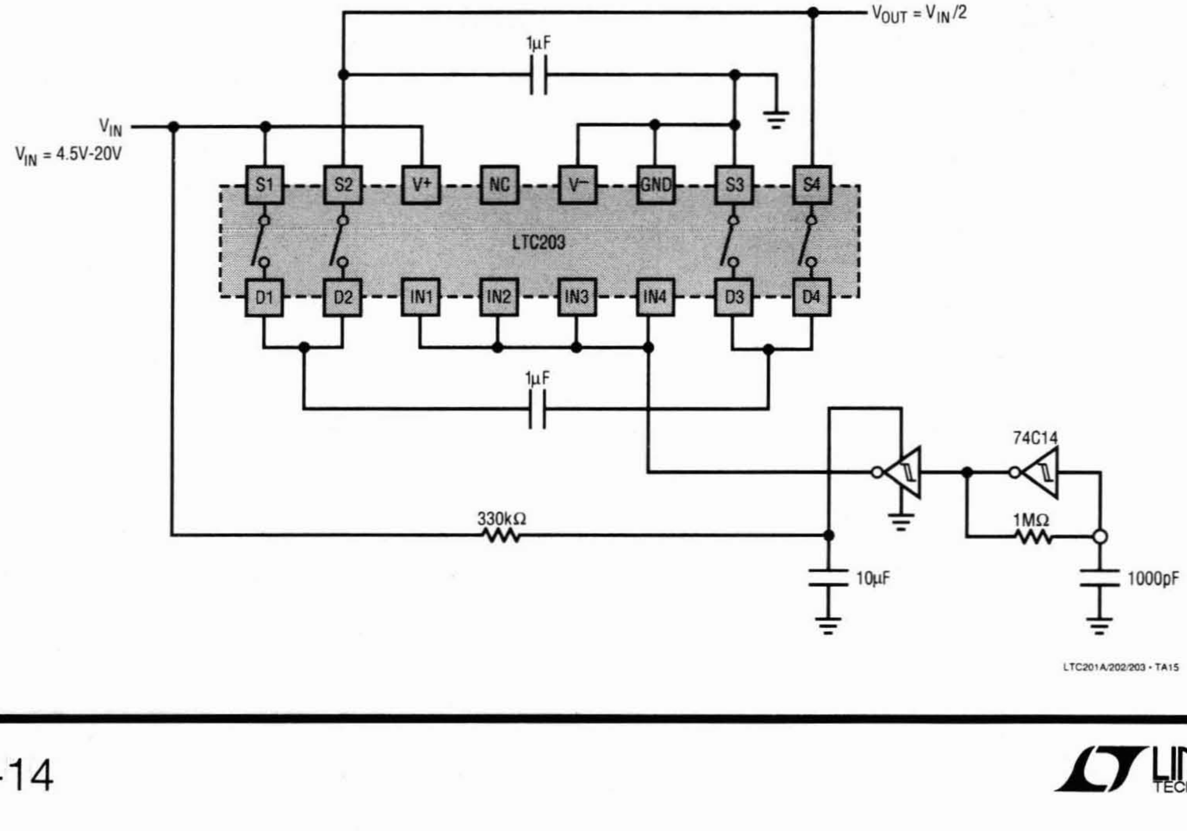
APPLICATIONS INFORMATION

Precision Current Sensing in Supply Rails


74C14
+15V
SHUNT CAN BE IN
POSITIVE OR NEGATIVE
SUPPLY LEAD
I_{IN}
R_{SHUNT}
1MΩ
V_{OUT}
1000pF
1μF
S1
S2
IN1
IN2
IN3
IN4
S3
S4
LTC203
D1
D2
NC
V+
V−
GND
D3
D4
+15V
−15V
1μF

LTC201A/202/203 • TA14

Precision Voltage Divide by 2 Circuit


$V_{OUT} = V_{IN}/2$
1μF
V_{IN}
V_{IN} = 4.5V-20V
S1
S2
V+
NC
V−
GND
S3
S4
LTC203
D1
D2
IN1
IN2
IN3
IN4
D3
D4
1μF
74C14
330kΩ
1MΩ
10μF
1000pF

LTC201A/202/203 • TA15

LTC221/LTC222

Micropower, Low Charge Injection, Quad CMOS Analog Switches with Data Latches

FEATURES

- Micropower Operation
- Single 5V or ±15V Supply Operation
- Low Charge Injection
- Low R_{ON}
- Low Leakage
- Guaranteed Break Before Make
- Latch Resistant Design
- TTL/CMOS Compatible
- Improved Second Source for DG221/DG222
- Microprocessor Bus Compatible

KEY SPECIFICATIONS

■ Supply Current	I^+ = 40µA, I^- = 5µA Max
■ Charge Injection (±15V Supplies)	±25pC Max
(Single 5V Supply)	2pC Typ
■ R_{ON}	65Ω Typ
■ Signal Range	±15V

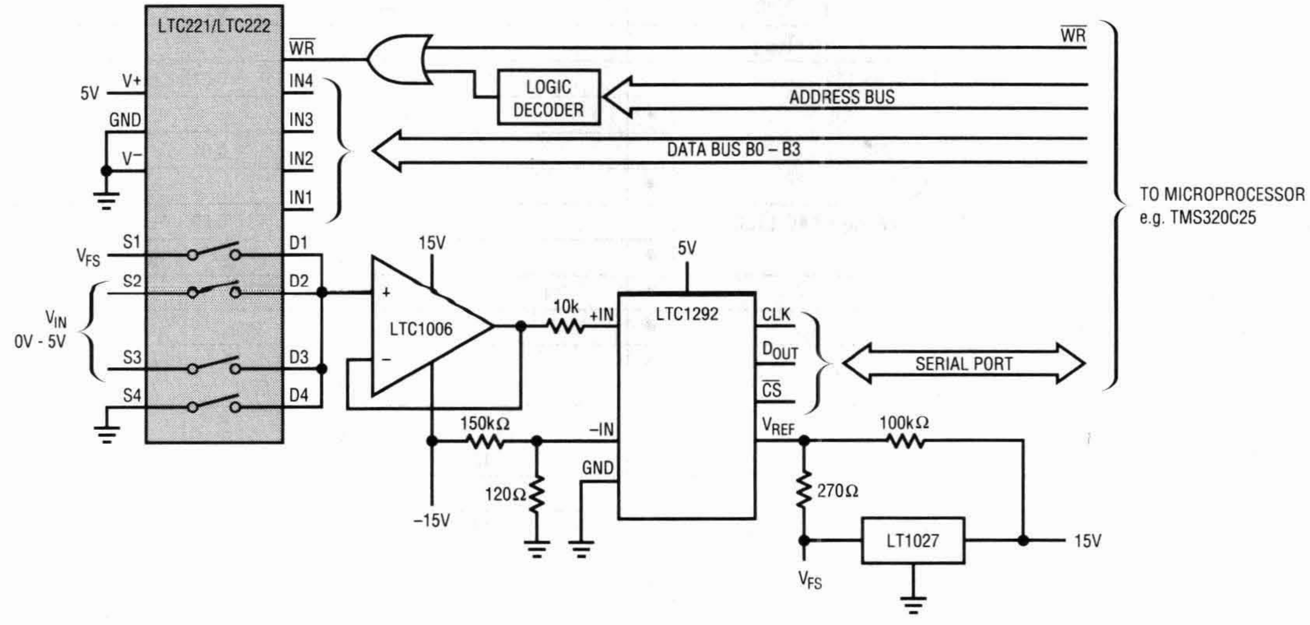
DESCRIPTION

The LTC221 and LTC222 are micropower, quad CMOS analog switches which typically dissipate only 250µW from ±15V supplies and 40µW from a single 5V supply. Onboard latches allow the LTC221 and LTC222 to interface directly to most microprocessor buses. The switches have 65Ω typical on resistance and a very high off resistance. A break before make characteristic is inherent in these switches to prevent the shorting of two channels. The signal range is ±15V with a supply voltage of ±15V and 0V-5V with a single 5V supply. The switches have special charge compensation circuitry which greatly reduces charge injection to a maximum of ±25pC (±15V supplies).

The LTC221 and LTC222 are designed for applications such as microprocessor controlled programmable gain amplifiers, automatic test equipment, communication systems, and data acquisition systems. The LTC221 is normally closed and the LTC222 is normally open as shown in the Logic Table.

TYPICAL APPLICATION

Two-Channel, 12-Bit, Self Calibrating Data Acquisition System


LTC221/LTC222
5V
V+
GND
V−
WR
IN4
IN3
IN2
IN1
LOGIC DECODER
ADDRESS BUS
DATA BUS B0 – B3
WR
TO MICROPROCESSOR e.g. TMS320C25
V_{FS}
S1
S2
S3
S4
D1
D2
D3
D4
V_{IN} 0V - 5V
15V
LTC1006
−15V
10k
150kΩ
120Ω
5V
LTC1292
+IN
−IN
GND
CLK
D_{OUT}
$\overline{CS}$
V_{REF}
SERIAL PORT
100kΩ
270Ω
LT1027
15V
V_{FS}
LTC221/222 • TA01

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Voltages Referenced to V^-

V^+ 44V

GND 25V

Digital Inputs, S, D (Note 2) .... – 2V to (V^+ + 2V) or 20mA, Whichever Occurs First

Current

- Any Input Except S or D 30mA
- Continuous S or D 20mA
- Peak S or D
  - (Pulsed at 1ms, 10% Duty Cycle Max) 70mA

ESD Susceptibility (Note 3) 4kV

Power Dissipation (Plastic) 500mW

Power Dissipation (Ceramic) 900mW

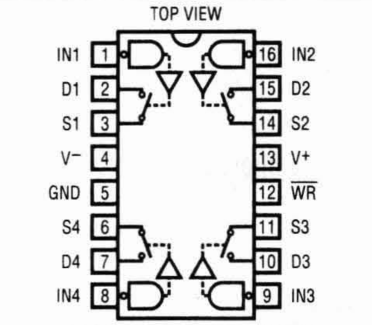
Operating Temperature Range

- LTC221C/LTC222C .... 0°C to 70°C
- LTC221M/LTC222M .... – 55°C to 125°C

Storage Temperature Range .... – 65°C to 150°C

Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
16-LEAD CERAMIC DIP

N PACKAGE
16-LEAD PLASTIC DIP

SO PACKAGE
16-LEAD PLASTIC SOIC

ORDER PART NUMBER

LTC221MJ
LTC221CJ
LTC221CN
LTC221CS
LTC222MJ
LTC222CJ
LTC222CN
LTC222CS

LOGIC TABLE

IN_X	$\overline{WR}$	LTC221	LTC222
0	0	On	Off
1	0	Off	On
X	1	Maintain Previous State	Maintain Previous State

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V^- = -15V$, GND = 0V unless otherwise noted.

PARAMETER	CONDITIONS			LTC221M/LTC222M MIN	TYP	MAX	LTC221C/LTC222C MIN	TYP	MAX	UNITS
Analog Signal Range			●			±15			±15	V
R_{ON}	$V_S = \pm 10V$ $I_D = 1mA$	T_{MIN}				90			90	Ω
		25°C			65	90		65	90	
		T_{MAX}				135			135	
Off Input Leakage I_S (OFF)	$V_D = \pm 14V$, $V_S = \mp 14V$				0.01	±1		0.01	±5	nA
			●			±100			±100	
Off Output Leakage I_D (OFF)	$V_{IN} = 2.4V$, LTC221				0.01	±1		0.01	±5	
	$V_{IN} = 0.8V$, LTC222		●			±100			±100	
On Channel Leakage I_D (ON)	$V_D = V_S = \pm 14V$, $V_{IN} = 2.4V$, LTC222				0.02	±1		0.02	±5	nA
	$V_{IN} = 0.8V$, LTC221		●			±200			±200	
Input High Voltage V_{INH}, $V_{\overline{WR}H}$			●	2.4			2.4			V
Input Low Voltage V_{INL}, $V_{\overline{WR}L}$			●			0.8			0.8	V
Input High or Low Current I_{INH}, I_{INL}, $I_{\overline{WR}H}$, $I_{\overline{WR}L}$	$V_{IN} = 15V, 0V$ $V_{\overline{WR}} = 15V, 0V$		●			±1			±1	μA
C_S (OFF)					5			5		pF
C_D (OFF)					12			12		pF
C_D, C_S (ON)					30			30		pF
I^+	All Channels On or Off $V_{IN} = V_{\overline{WR}} = 0V$ or 4.0V				16	40		16	40	μA
			●			60			60	
I^-					0.1	5		0.1	5	
			●			10			10	

AC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V^- = -15V$, GND = 0V unless otherwise noted.

PARAMETER	CONDITIONS	LTC221M/LTC222M MIN	TYP	MAX	LTC221C/LTC222C MIN	TYP	MAX	UNITS
T_{ON}	$V_S = 2V$, $R_L = 1k\Omega$, $C_L = 35pF$		290	400		290	400	ns
T_{OFF}			210	300		210	300	
T_{OPEN}		20	85		20	85		ns
Off Isolation	$V_S = 2Vp\text{-}p$, $R_L = 1k\Omega$		75			75		dB
Crosstalk	f = 100kHz		90			90		
Charge Injection Q_{INJ}	$R_{GEN} = 0\Omega$, $C_L = 1000pF$, $V_{GEN} = 0$		5	±25		8	±25	pC
Total Harmonic Distortion THD	$V_S = 2Vp\text{-}p$, $R_L = 10k\Omega$		0.01			0.01		%
T_{ON}, $\overline{WR}$	$V_S = 2V$, $R_L = 1k\Omega$, $C_L = 35pF$		270	400		270	400	ns
T_{OFF}, $\overline{WR}$			160	300		160	300	

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

$V^+ = +5V$, $V^- = GND = 0V$ unless otherwise noted.

PARAMETER	CONDITIONS			LTC221M/LTC222M MIN	TYP	MAX	LTC221C/LTC222C MIN	TYP	MAX	UNITS
Analog Signal Range			●	0		5	0		5	V
R_{ON}	$V_S = +1.5V, +3V$ $I_D = 0.25mA$	T_{MIN}				450			520	Ω
		25°C			280	450		280	520	
		T_{MAX}				650			650	
Off Input Leakage I_S (OFF)	$V_D = 4V, 1V$; $V_S = 1V, 4V$ (Note 4)				0.01	±1		0.01	±5	nA
			●			±100			±100	
Off Output Leakage I_D (OFF)					0.01	±1		0.01	±5	
			●			±100			±100	
On Channel Leakage I_D (ON)	$V_D = V_S = 1V, 4V$ (Note 4)				0.01	±1		0.01	±5	nA
			●			±200			±200	
Input High Voltage V_{INH}, $V_{\overline{WR}H}$			●	2.4			2.4			V
Input Low Voltage V_{INL}, $V_{\overline{WR}L}$			●			0.8			0.8	V
Input High or Low Current I_{INH}, I_{INL}, $I_{\overline{WR}H}$, $I_{\overline{WR}L}$	$V_{IN} = 5V, 0V$ $V_{\overline{WR}} = 5V, 0V$		●			±1			±1	μA
C_S (OFF)					5			5		pF
C_D (OFF)					12			12		pF
C_D, C_S (ON)					30			30		pF
I^+	All Channels On or Off				8	20		8	20	μA
	$V_{IN} = V_{\overline{WR}} = 0V$ or 4.0V		●			30			30	

AC ELECTRICAL CHARACTERISTICS

$V^+ = +5V$, $V^- = GND = 0V$ unless otherwise noted.

PARAMETER	CONDITIONS	LTC221M/LTC222M MIN	TYP	MAX	LTC221C/LTC222C MIN	TYP	MAX	UNITS
T_{ON}	$V_S = 2V$, $R_L = 1k\Omega$, $C_L = 35pF$		450	600		450	600	ns
T_{OFF}			190	300		190	300	
T_{OPEN}		100	250		100	250		ns
Off Isolation	$V_S = 2Vp\text{-}p$, $R_L = 1k\Omega$		75			75		dB
Crosstalk	f = 100kHz		90			90		
Charge Injection Q_{INJ}	$R_{GEN} = 0\Omega$, $C_L = 1000pF$, $V_{GEN} = 2.5V$		2			2		pC
Total Harmonic Distortion THD	$V_S = 2Vp\text{-}p$, $R_L = 10k\Omega$		0.01			0.01		%
T_{ON}, $\overline{WR}$	$V_S = 2V$, $R_L = 1k\Omega$, $C_L = 35pF$		430	600		430	600	ns
T_{OFF}, $\overline{WR}$			160	300		160	300	

The ● denotes the specifications which apply over full operating temperature range. All other limits and typicals $T_A = 25°C$.

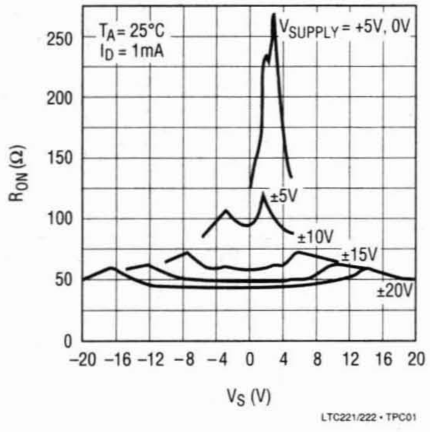
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Signals on S, D, or IN exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 3: In-circuit ESD on the switch pins (S or D) exceeds 4kV (see test circuit).

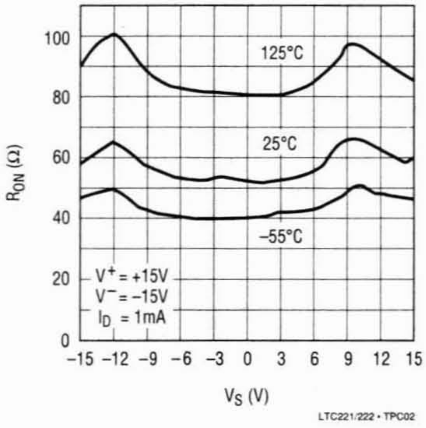
Note 4: Leakage current with a 5V supply is guaranteed by correlation with the ±15V leakage current.

TYPICAL PERFORMANCE CHARACTERISTICS



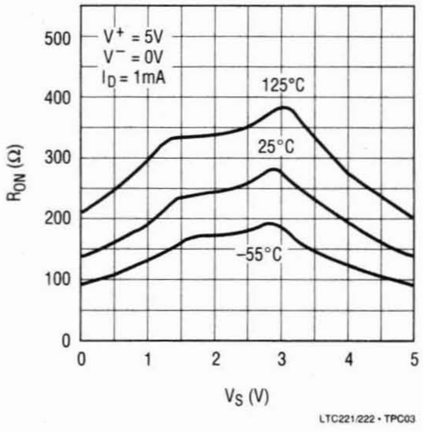
R_{ON} vs V_S Over Supply Voltage

LTC221/222 • TPC01



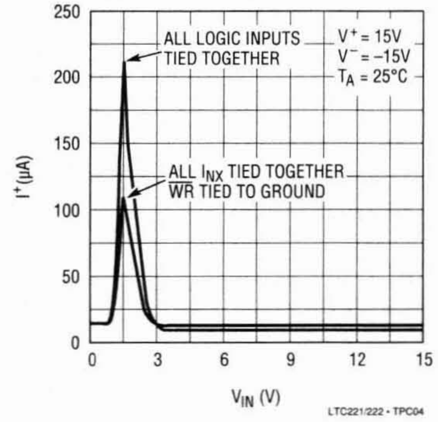
R_{ON} vs V_S Over Temperature

LTC221/222 • TPC02



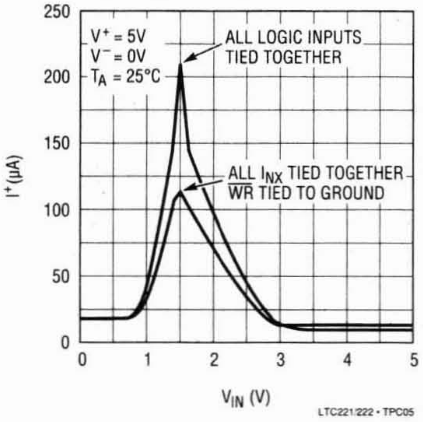
R_{ON} vs V_S Over Temperature

LTC221/222 • TPC03



Positive Supply Current vs Logic Input Voltage

LTC221/222 • TPC04



Positive Supply Current vs Logic Input Voltage

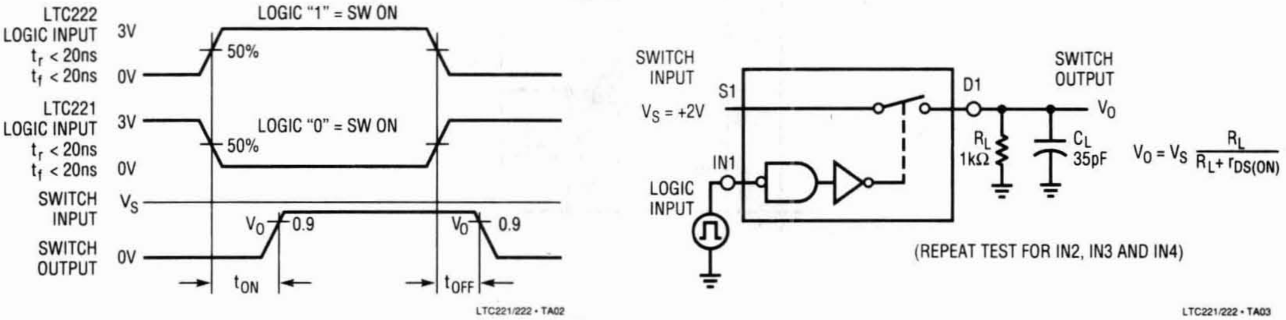
LTC221/222 • TPC05

APPLICATIONS INFORMATION

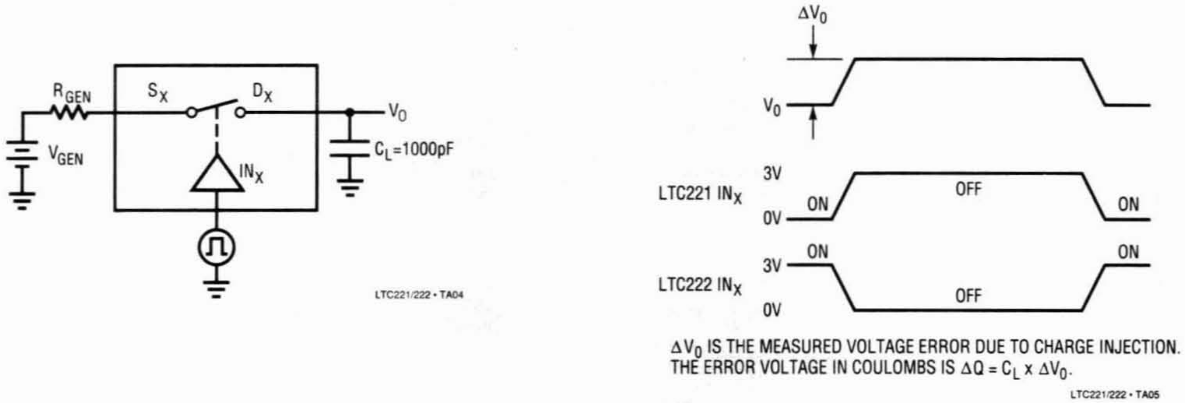
Switching Time Test Circuit

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be (+) or (–) as per switching time test circuit. V_O is the steady state output switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

Switching Time Test Circuit


LTC222 LOGIC INPUT
t_r < 20ns
t_f < 20ns
3V
0V
LOGIC "1" = SW ON
50%
LTC221 LOGIC INPUT
t_r < 20ns
t_f < 20ns
3V
0V
LOGIC "0" = SW ON
50%
SWITCH INPUT
V_S
SWITCH OUTPUT
0V
V_O
0.9
V_O
0.9
t_{ON}
t_{OFF}
LTC221/222 • TA02
SWITCH INPUT
V_S = +2V
S1
D1
SWITCH OUTPUT
V_O
R_L 1kΩ
C_L 35pF
$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$
IN1
LOGIC INPUT
(REPEAT TEST FOR IN2, IN3 AND IN4)
LTC221/222 • TA03

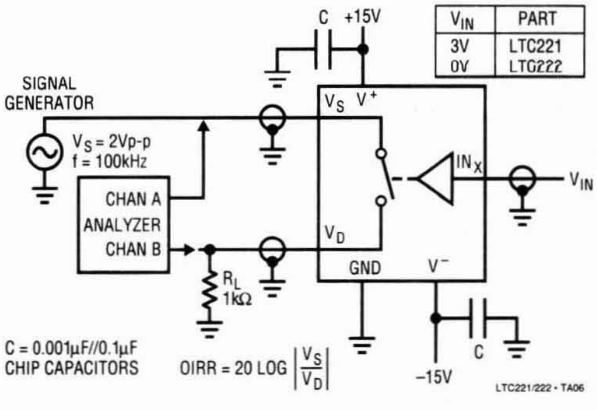
Charge Injection Test Circuit


R_{GEN}
V_{GEN}
S_X
D_X
IN_X
V_O
C_L=1000pF
LTC221/222 • TA04
ΔV_O
V_O
LTC221 IN_X
3V
0V
ON
OFF
ON
LTC222 IN_X
3V
0V
ON
OFF
ON

ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $\Delta Q = C_L \times \Delta V_O$.

LTC221/222 • TA05

OIRR-Off Isolation Test Circuit

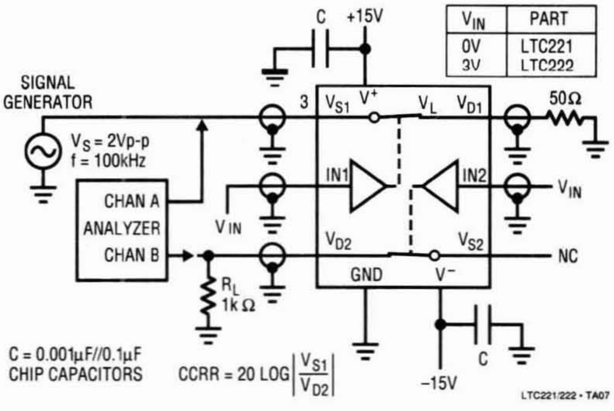

C
+15V
V_{IN} | PART
3V | LTC221
0V | LTC222
SIGNAL GENERATOR
V_S = 2Vp-p
f = 100kHz
CHAN A
ANALYZER
CHAN B
R_L 1kΩ
V_S
V^+
IN_X
V_{IN}
V_D
GND
V^-
C
–15V

C = 0.001µF//0.1µF CHIP CAPACITORS

$\text{OIRR} = 20\ \text{LOG} \left| \frac{V_S}{V_D} \right|$

LTC221/222 • TA06

CCRR-Channel to Channel Crosstalk Test Circuit


C
+15V
V_{IN} | PART
0V | LTC221
3V | LTC222
SIGNAL GENERATOR
V_S = 2Vp-p
f = 100kHz
CHAN A
ANALYZER
CHAN B
R_L 1kΩ
3
V_{S1}
V^+
V_L
V_{D1}
50Ω
IN1
IN2
V_{IN}
V_{IN}
V_{D2}
V_{S2}
NC
GND
V^-
C
–15V

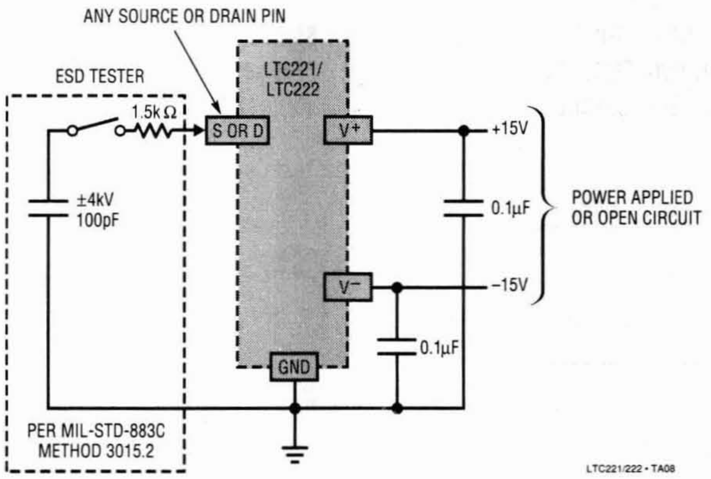
C = 0.001µF//0.1µF CHIP CAPACITORS

$\text{CCRR} = 20\ \text{LOG} \left| \frac{V_{S1}}{V_{D2}} \right|$

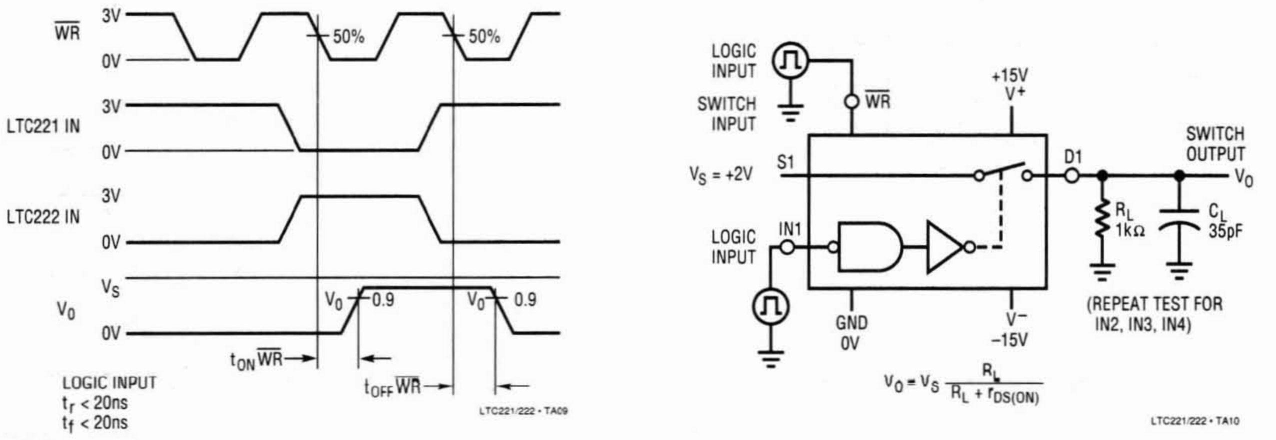
LTC221/222 • TA07

APPLICATIONS INFORMATION

In-Circuit ESD Test Circuit

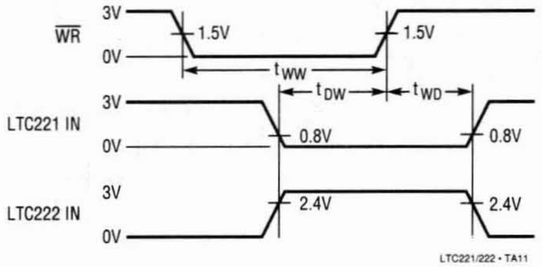

ANY SOURCE OR DRAIN PIN
ESD TESTER
1.5kΩ
S OR D
LTC221/
LTC222
V+
+15V
±4kV
100pF
0.1μF
POWER APPLIED
OR OPEN CIRCUIT
V−
−15V
0.1μF
GND
PER MIL-STD-883C
METHOD 3015.2
LTC221/222 • TA08

$\overline{WR}$ Switching Time Test Circuit


WR
3V
0V
50%
50%
LTC221 IN
3V
0V
LTC222 IN
3V
0V
VO
VS
0V
VO 0.9
VO 0.9
tON WR
tOFF WR
LOGIC INPUT
tr < 20ns
tf < 20ns
LTC221/222 • TA09
LOGIC INPUT
SWITCH INPUT
WR
+15V
V+
VS = +2V
S1
D1
SWITCH OUTPUT
VO
RL 1kΩ
CL 35pF
LOGIC INPUT
IN1
GND
0V
V−
−15V
(REPEAT TEST FOR IN2, IN3, IN4)
LTC221/222 • TA10

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

$\overline{WR}$ Setup Conditions

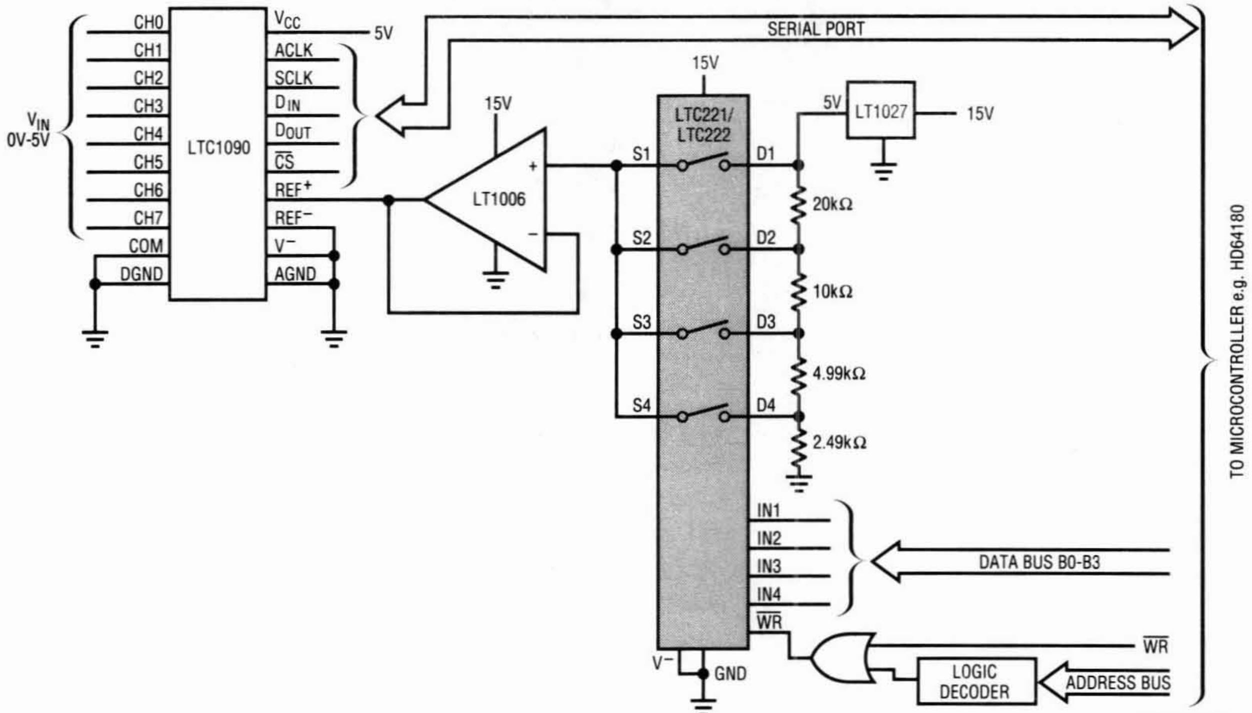

WR
3V
0V
1.5V
1.5V
tWW
tDW
tWD
LTC221 IN
3V
0V
0.8V
0.8V
LTC222 IN
3V
0V
2.4V
2.4V
LTC221/222 • TA11

$\overline{WR}$/Input Minimum Timing Requirements

	PARAMETER	MIN LIMIT	UNITS
t_{WW}	Write Pulse Width	230	ns
t_{DW}	Data Valid to Write	180	
t_{WD}	Data Valid After Write	30	

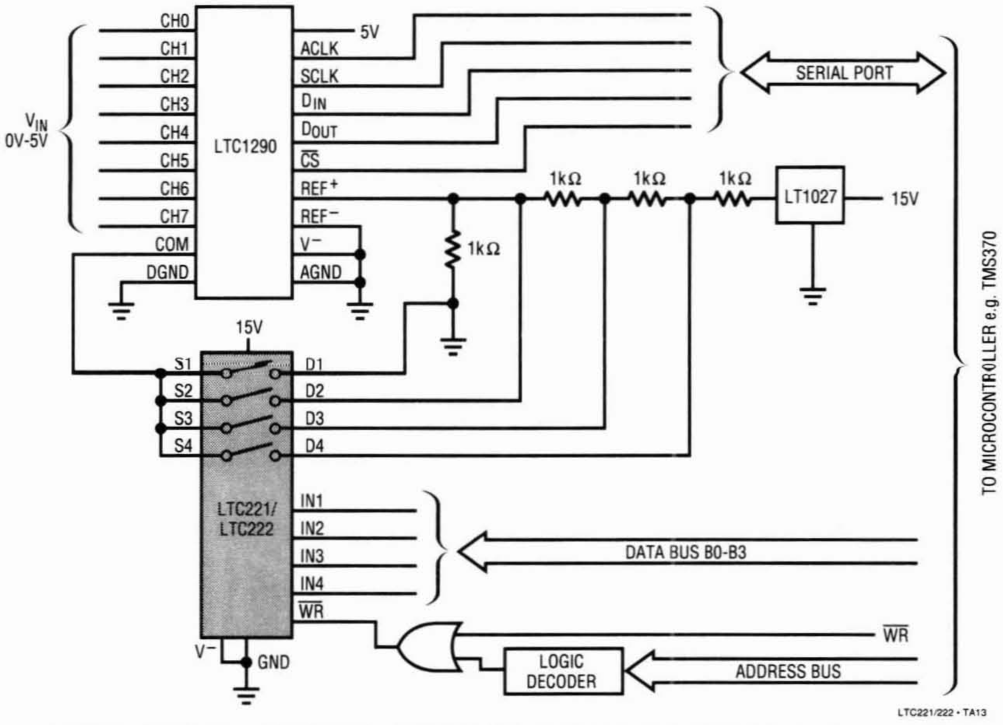
APPLICATIONS INFORMATION

Auto Ranging an 8-Channel, 10-Bit A/D Converter


CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
V_{IN}
0V-5V
LTC1090
V_{CC}
ACLK
SCLK
D_{IN}
D_{OUT}
$\overline{CS}$
REF+
REF−
V−
AGND
5V
SERIAL PORT
15V
LT1006
15V
LTC221/
LTC222
S1
S2
S3
S4
D1
D2
D3
D4
5V
LT1027
15V
20kΩ
10kΩ
4.99kΩ
2.49kΩ
IN1
IN2
IN3
IN4
$\overline{WR}$
DATA BUS B0-B3
$\overline{WR}$
V−
GND
LOGIC
DECODER
ADDRESS BUS
TO MICROCONTROLLER e.g. HD64180

LTC221/222 • TA12

8-Channel, 14-Bit A/D Converter


CH0
CH1
CH2
CH3
CH4
CH5
CH6
CH7
COM
DGND
V_{IN}
0V-5V
LTC1290
5V
ACLK
SCLK
D_{IN}
D_{OUT}
$\overline{CS}$
REF+
REF−
V−
AGND
SERIAL PORT
1kΩ
1kΩ
1kΩ
1kΩ
LT1027
15V
15V
S1
S2
S3
S4
D1
D2
D3
D4
LTC221/
LTC222
IN1
IN2
IN3
IN4
$\overline{WR}$
DATA BUS B0-B3
$\overline{WR}$
V−
GND
LOGIC
DECODER
ADDRESS BUS
TO MICROCONTROLLER e.g. TMS370

LTC221/222 • TA13

NOTES

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SECTION 12—MILITARY PRODUCTS

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NOTE

Military product data sheets are available from your local LTC Sales Representative, or by calling LTC Communications at (800) 637-5545.

LINEAR TECHNOLOGY MILITARY PRODUCTS/ PROGRAMS

Linear Technology Corporation (LTC) offers a comprehensive range of high performance analog/linear integrated circuits including; Data Converters, Interface devices, High Speed Amplifiers, Precision Operational Amplifiers, Comparators, Voltage References, DC-DC Converters, Switches, Voltage Regulators, Switching Regulators, PWMs, and other special function products serving the rigorous demands of the military marketplace.

The Company's specification system, quality procedures and policies were set up from the beginning to meet the exacting demands of MIL-Q-9858 (Quality Program Requirements), MIL-I-45208 (Inspection System Requirements), MIL-M-38510 (General Specification for Microcircuits), MIL-STD-976 (Certification Requirements for Microcircuits), MIL-STD-883 (Test Methods and Procedures for Microelectronics) and more recently the ISO 9000 (Internal Standards for Quality Management).

In addition, the Company has introduced a line of radiation tolerant devices which are offered with three different in-house levels of enhanced reliability processing to serve ground, air and/or space applications, including customer generated Source Controlled Drawings (SCDs) for a variety of missions.

LTC's military programs include:

- JAN Class S
- JAN Class B
- Standard Military Drawings (SMDs)
- 883
- Hi-Rel (SCDs)
- LTC "RH", Radiation hardened devices

LTC JAN

At the end of 1969, the Solid State Applications Branch of the Rome Air Development Center (RADC) issued the first copy of MIL-M-38510. This general specification for microcircuits established the procedures that a manufacturer must follow to have products listed on the Qualified Parts List (QPL).

One major problem faced by defense contractors using semiconductor devices was the inability to interchange devices caused by a proliferation of non-standard electrical specifications. The 38510 (JAN) program addressed this problem by publishing detailed electrical specifications (slash sheets) for each component to be listed on the QPL.

JAN devices are completely processed in the United States or its territories and all wafer fabrication, wafer sort, assembly, testing, and conformance testing are performed onshore.

In August 1984, LTC was visited by a team of Defense Electronics Supply Center (DESC) personnel. This team spent almost four days auditing LTC and at the end of the visit they awarded the Company "Class B Line Certification." *This was a first for any company to receive this distinction on their first audit!*

In early 1985, LTC joined the ranks of the eighteen existing QPL suppliers. Of these eighteen, only a handful of suppliers participate in the linear military JAN market. LTC believes its analog design experience and manufacturing strength has and will continue to make significant contributions to this market.

LTC's first QPL listing was achieved in February 1985, one year after the Company made JAN Class B a corporate goal. Other companies have typically taken 2 to 3 years to achieve this status. The line certification and QPL approvals were awarded to MIL-M-38510 and MIL-STD-883 Rev.C specifications. Since that time the Company has been re-audited to the latest revisions of these specifications and has maintained an uninterrupted certification record for the manufacture of JAN QPL products.

In November 1987, LTC was audited by a team from DESC, Naval Weapons Support Center and Aerospace Corporation and was awarded "Class S Line Certification."

LTC's policy of providing JAN linear components supports the United States Government's position of standardization to decrease the number of active part types maintained by DESC. This number is currently in excess of 85,000 for all types of components (contrasted to approximately 8,000 industry standard components). Standardization will clearly decrease costs and assist in the maintenance of military weapons systems and equipment now in the field.

LTC maintains an aggressive program to expand its JAN product offerings such that LTC now offers 45 products listed on the Class B Qualified Parts List (Part 1) and 40 products on the Class S Qualified Parts List (Parts 1 and 2). To receive an updated copy of LTC's current JAN QPL product offering, contact your local LTC sales office or LTC Military Marketing.

For JAN Flows see Figure 1 and Figure 2.

LTC Standard Military Drawings

DESC drawings were initiated in 1976 to standardize the electrical requirements for full temperature-tested military components. These DESC drawings (or minispecs) were initially issued for low power Schottky devices (54LS) used by defense subcontractors on the Air Force's F16. The program accomplished standardization of testing, without the delays associated with the qualification process for JAN components.

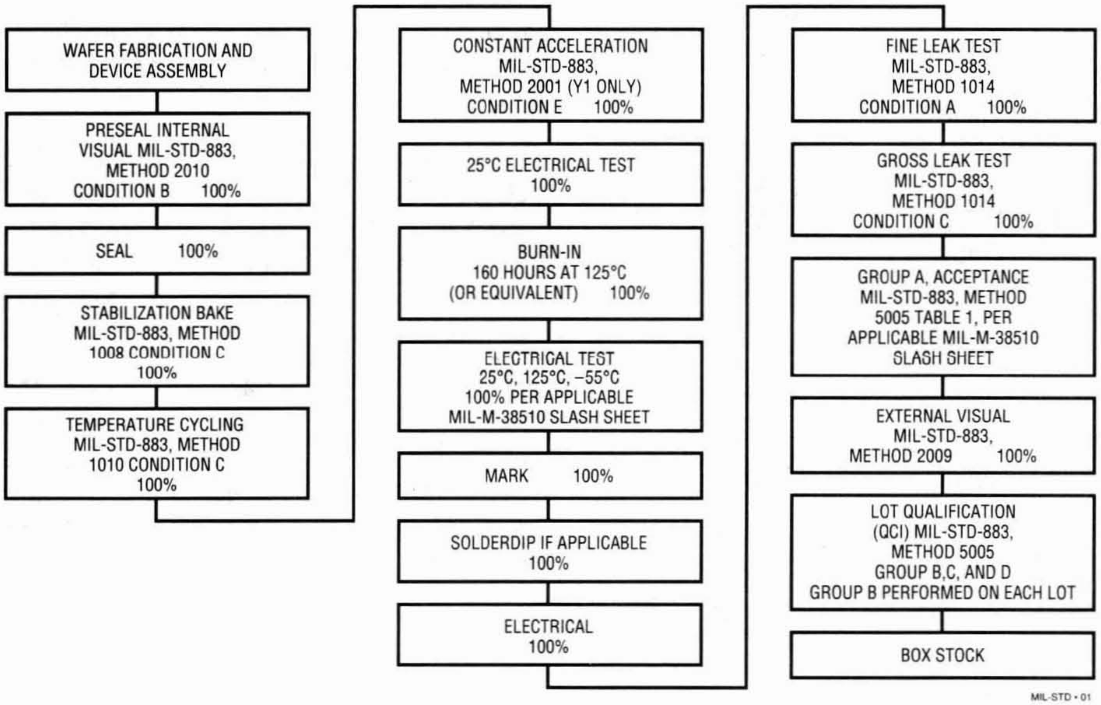

WAFER FABRICATION AND DEVICE ASSEMBLY
PRESEAL INTERNAL VISUAL MIL-STD-883, METHOD 2010 CONDITION B 100%
SEAL 100%
STABILIZATION BAKE MIL-STD-883, METHOD 1008 CONDITION C 100%
TEMPERATURE CYCLING MIL-STD-883, METHOD 1010 CONDITION C 100%
CONSTANT ACCELERATION MIL-STD-883, METHOD 2001 (Y1 ONLY) CONDITION E 100%
25°C ELECTRICAL TEST 100%
BURN-IN 160 HOURS AT 125°C (OR EQUIVALENT) 100%
ELECTRICAL TEST 25°C, 125°C, –55°C 100% PER APPLICABLE MIL-M-38510 SLASH SHEET
MARK 100%
SOLDERDIP IF APPLICABLE 100%
ELECTRICAL 100%
FINE LEAK TEST MIL-STD-883, METHOD 1014 CONDITION A 100%
GROSS LEAK TEST MIL-STD-883, METHOD 1014 CONDITION C 100%
GROUP A, ACCEPTANCE MIL-STD-883, METHOD 5005 TABLE 1, PER APPLICABLE MIL-M-38510 SLASH SHEET
EXTERNAL VISUAL MIL-STD-883, METHOD 2009 100%
LOT QUALIFICATION (QCI) MIL-STD-883, METHOD 5005 GROUP B,C, AND D GROUP B PERFORMED ON EACH LOT
BOX STOCK
MIL-STD • 01

Figure 1. MIL-M-38510 Class B Flow

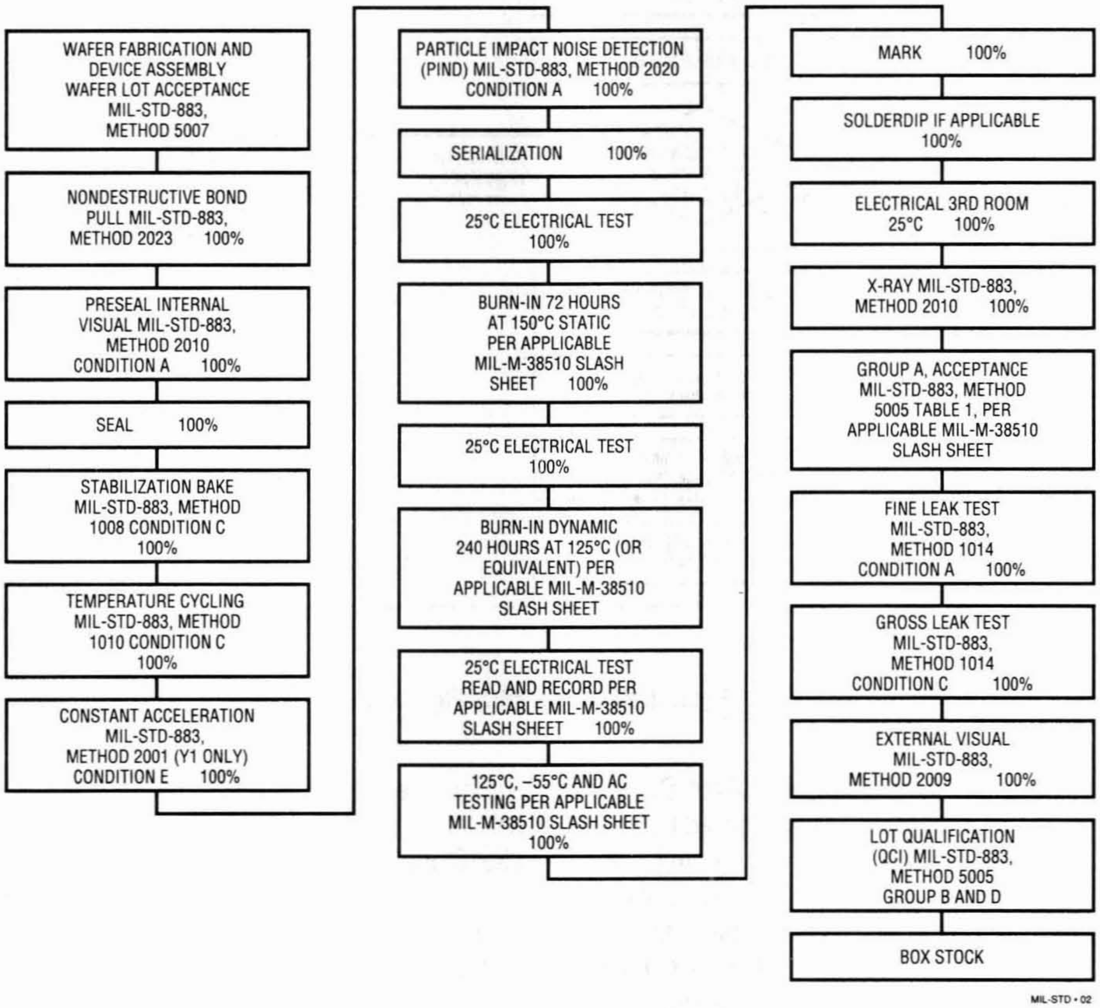
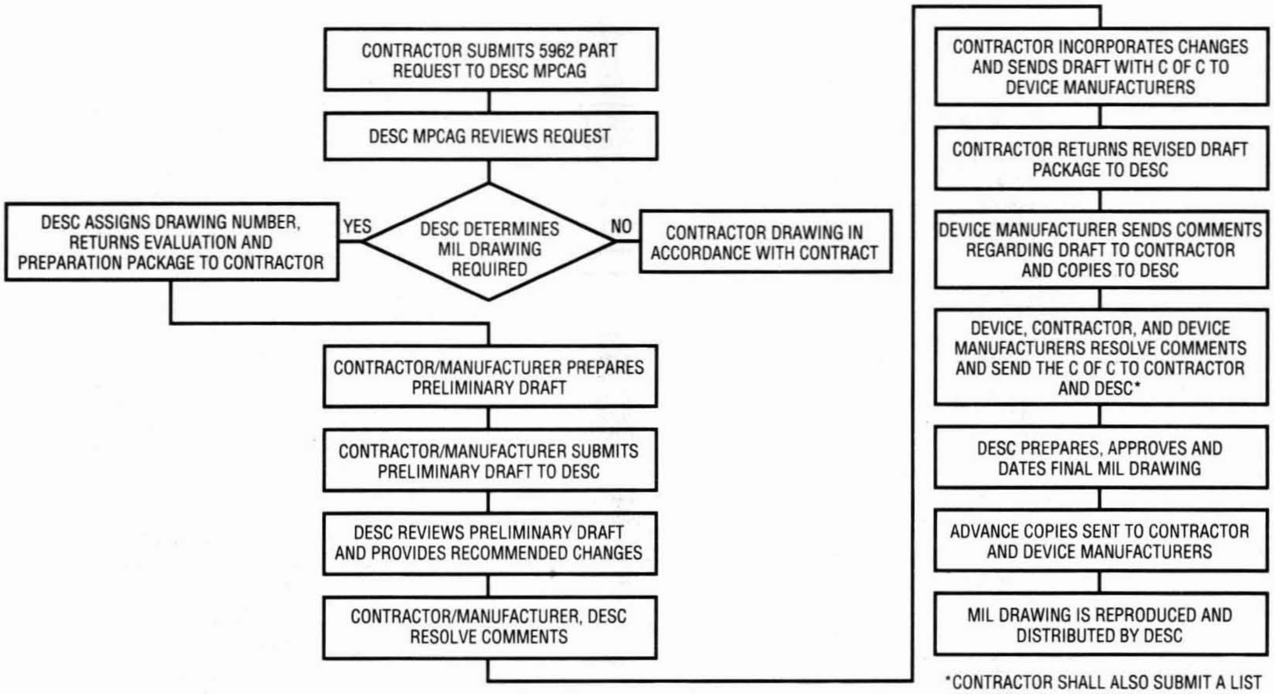

WAFER FABRICATION AND DEVICE ASSEMBLY WAFER LOT ACCEPTANCE MIL-STD-883, METHOD 5007
NONDESTRUCTIVE BOND PULL MIL-STD-883, METHOD 2023 100%
PRESEAL INTERNAL VISUAL MIL-STD-883, METHOD 2010 CONDITION A 100%
SEAL 100%
STABILIZATION BAKE MIL-STD-883, METHOD 1008 CONDITION C 100%
TEMPERATURE CYCLING MIL-STD-883, METHOD 1010 CONDITION C 100%
CONSTANT ACCELERATION MIL-STD-883, METHOD 2001 (Y1 ONLY) CONDITION E 100%
PARTICLE IMPACT NOISE DETECTION (PIND) MIL-STD-883, METHOD 2020 CONDITION A 100%
SERIALIZATION 100%
25°C ELECTRICAL TEST 100%
BURN-IN 72 HOURS AT 150°C STATIC PER APPLICABLE MIL-M-38510 SLASH SHEET 100%
25°C ELECTRICAL TEST 100%
BURN-IN DYNAMIC 240 HOURS AT 125°C (OR EQUIVALENT) PER APPLICABLE MIL-M-38510 SLASH SHEET
25°C ELECTRICAL TEST READ AND RECORD PER APPLICABLE MIL-M-38510 SLASH SHEET 100%
125°C, –55°C AND AC TESTING PER APPLICABLE MIL-M-38510 SLASH SHEET 100%
MARK 100%
SOLDERDIP IF APPLICABLE 100%
ELECTRICAL 3RD ROOM 25°C 100%
X-RAY MIL-STD-883, METHOD 2010 100%
GROUP A, ACCEPTANCE MIL-STD-883, METHOD 5005 TABLE 1, PER APPLICABLE MIL-M-38510 SLASH SHEET
FINE LEAK TEST MIL-STD-883, METHOD 1014 CONDITION A 100%
GROSS LEAK TEST MIL-STD-883, METHOD 1014 CONDITION C 100%
EXTERNAL VISUAL MIL-STD-883, METHOD 2009 100%
LOT QUALIFICATION (QCI) MIL-STD-883, METHOD 5005 GROUP B AND D
BOX STOCK
MIL-STD • 02

Figure 2. MIL-M-38510 Class S Flow

The DESC drawing was viewed as a preliminary specification prior to JAN approval, and it ranks second in the order of purchasing hierarchy to JAN. This order is defined in Requirement 64 of MIL-STD-454. If a JAN part is available, it is still preferred, however, there are many types of devices where the volume is such that the cost of a full JAN qualification may not be justified, but where a need exists for electrical standardization.

CMOS and analog circuits were added to the DESC Drawing Program in 1977, 1978 and 1979, but widespread acceptance of these parts was not achieved. Today with more emphasis being placed on standardization, the interest level in DESC drawings has accelerated. This category of product can be built offshore with 883-level processing and the electrical parameters are tested specifically to the DESC drawing.

To provide parts to a DESC drawing, a manufacturer has to have at least one part on the 38510 QPL. He must also provide DESC with a certificate of compliance agreeing to the tests and conditions listed on the drawing.


CONTRACTOR SUBMITS 5962 PART REQUEST TO DESC MPCAG
DESC MPCAG REVIEWS REQUEST
DESC ASSIGNS DRAWING NUMBER, RETURNS EVALUATION AND PREPARATION PACKAGE TO CONTRACTOR
YES
DESC DETERMINES MIL DRAWING REQUIRED
NO
CONTRACTOR DRAWING IN ACCORDANCE WITH CONTRACT
CONTRACTOR/MANUFACTURER PREPARES PRELIMINARY DRAFT
CONTRACTOR/MANUFACTURER SUBMITS PRELIMINARY DRAFT TO DESC
DESC REVIEWS PRELIMINARY DRAFT AND PROVIDES RECOMMENDED CHANGES
CONTRACTOR/MANUFACTURER, DESC RESOLVE COMMENTS
CONTRACTOR INCORPORATES CHANGES AND SENDS DRAFT WITH C OF C TO DEVICE MANUFACTURERS
CONTRACTOR RETURNS REVISED DRAFT PACKAGE TO DESC
DEVICE MANUFACTURER SENDS COMMENTS REGARDING DRAFT TO CONTRACTOR AND COPIES TO DESC
DEVICE, CONTRACTOR, AND DEVICE MANUFACTURERS RESOLVE COMMENTS AND SEND THE C OF C TO CONTRACTOR AND DESC*
DESC PREPARES, APPROVES AND DATES FINAL MIL DRAWING
ADVANCE COPIES SENT TO CONTRACTOR AND DEVICE MANUFACTURERS
MIL DRAWING IS REPRODUCED AND DISTRIBUTED BY DESC

*CONTRACTOR SHALL ALSO SUBMIT A LIST OF ALTERNATE SOURCES TO DESC–ECS AT TIME OF SUBMISSION OF C OF C

MIL-STD • 03

Figure 3. SMD Preparation Flowchart

In 1986 a new program named Standard Military Drawings (SMDs) was launched by DESC. This replaced the previous DESC Drawing Program. This new program is aimed directly at standardizing electrical requirements with the objective to decrease the time required to issue a military drawing. To achieve this, we have set up a computer link-up with the DESC Standardized Mil Drawing Group. LTC is actively supporting this Standard Military Drawing program and we are working closely with DESC and OEMs to participate in this government plan toward a greater level of standardization in military specifications.

LTC has over 134 devices listed on DESC and Mil drawings, and we are actively supporting these standardization programs by having parts available off the shelf from LTC and from distribution outlets.

For SMD Flow see Figure 3.

SMDs Get A New Part Numbering System

A new numbering system has been introduced to standardize the part numbering system for JAN 38510 and SMD (Standard Military Drawing) products.

Under the new system, the SMD number 5962-XXXXXZZ(_)YY will be used, with a minor change for the 38510 qual'd devices. This will make one part have one part number with just the grade identification being different (M = SMD, B = JAN B and S = JAN S). An example of this follows:

Old System

LTC PART NUMBER	"OLD" SMD NO.	JAN PART NUMBER
LT1021CMH-5/883	5962-8876202GA	JM38510/12407BGA

New System

LTC PART NUMBER	"NEW" SMD ONE PART NUMBER SYSTEM
LT1021CMH-5/883	5962-8876202(M, B or S)GA

This was implemented on January 1, 1990, for all SMDs and slash sheets created after this date. Devices listed or approved in the past will retain their respective existing part numbers.

LTC MIL-STD-883 Product

The semicondutcor industry 883 designation on military semiconductor components established a defacto standard in response to a significant demand from the military defense contractors. The Government recognized the existence of 883 components in the recent revisions of MIL-STD-883 and MIL-M-38510, and the requirements for compliant 883 components are now defined very specifically in these documents.

MIL-STD-883 is a test procedures and methods document which is revised periodically and defines the conditions for two categories of product, Class B and Class S. Class B is intended for applications where maintenance is difficult or expensive and where reliability is vital. Class S is intended for space and critical applications where replacement is extremely difficult or impossible and where reliability is imperative.

On December 31, 1984, a key clause was added to MIL-STD-883 Rev. C, "paragraph 1.2.1." This states that if a manufacturer advertises, certifies, or marks parts as compliant with MIL-STD-883 those parts must meet all of the provisions of MIL-STD-883, a practice consistent with "Truth in Advertising."

According to the Defense Electronics Supply Center (a branch of the Defense Department's Logistics Agency), the intent of paragraph 1.2.1 was to link MIL-STD-883 with the controls and details contained in MIL-M-38510.

LTC can state that all of its 883 products are in full compliance with the latest revision of MIL-STD-883. We have over 333 versions of our 883 products listed in our current catalog, including operational amplifiers, voltage regulators, voltage references, comparators, and our advanced line of proprietary CMOS circuits.

Table 1. LTC 883 Group A Sampling Plan

		883C	
TEST	**CONDITION**	**SAMPLE SIZE**	**LTPD**
DC Parametric	$T_A = 25°C$	116	2.0%
DC Parametric	$T_A = -55°C$ $+125°C$	116 116	2.0% 2.0%
AC Parametric	$T_A = 25°C$	116	2.0%

LTC Hi-Rel (SCDs)

LTC recognizes the need for Source Controlled Drawings (SCDs) and the Company's DESC-certified line is well equipped to handle these requirements for space and hi-rel applications. The Company has a comprehensive specification review procedure and emphasis is placed on compliance to test methods and procedures. Over 8,000 specifications have been reviewed to date with fast feedback to our customers.

LTC has serviced SCD orders including "S" level specifications with an emphasis on compliance with customer purchase order requirements and on-time delivery performance. A dedicated SL traveller is initiated to baseline the manufacturing and test flow requirements to service each order.

LTC's Product Marketing Group can provide you with more details on a case-by-case basis.

LTC's Radiation Hardness Program

LTC has developed a proprietary design/wafer fabrication process for RAD HARD (RH prefix) products, complemented by a separate set of RH data sheets. Each RH data sheet specifies the end point electrical test requirements for Total Dose irradiation testing performed on a sample basis in accordance with MIL-STD-883 Method 1019. We offer in certain cases, the option of using the slash sheet electricals for the pre-radiation test limits instead of the LTC RH data sheet electricals. But in all cases the post-radiation electricals are per LTC's RH data sheets.

Due to the unique wafer processing required to make RH products, the RH products are not totally compliant with all the Class S requirements of MIL-STD-883. Since MIL-STD-883 specifically prohibits the marking of non-compliant products with the 883C compliance indicator, LTC's RH products are marked with the LTC RH prefix part number or with a special mark specified by the customer.

Military Market Commitment

LTC is a focused, dedicated company servicing the needs of the linear military marketplace. We are shipping to the top U.S. defense electronics contractors who have qualified and approved our products. LTC is committed to being the best and most proficient high quality supplier of analog military components.

883 CERTIFICATE OF CONFORMANCE — LEVEL B

LTC Part Number ________________________

Lot Traceability No. ________________________

Purchase Order No. ________________________

QUALITY ASSURANCE INSPECTOR	
DATE	SIGNATURE

Customer Name ________________ P/N ________________ Qty ________________

Date Code ________________ Shipper # ________________ Traveller Lot # ________________

Group A = __________ Group B = __________ Group C = __________ Group D = __________

Group B/3 Re-Inspection Date, If Applicable ________________________________

LINEAR TECHNOLOGY CORPORATION HEREBY DECLARES THAT THE COMPONENTS SPECIFIED ON THE ABOVE PURCHASE ORDER COMPLY WITH YOUR SPECIFICATIONS AND REQUIREMENTS OF MIL-STD-883 REV C. ALL SUPPORTING DOCUMENTATION AND RECORDS ARE RETAINED ON FILE BY LTC AND ARE AVAILABLE FOR INSPECTION. THE MAJOR ELEMENTS OF THE 883C PROGRAM ARE SHOWN BELOW.

Operation	**Screening Procedure MIL-STD-883C, Method 5004**
Internal Visual	Method 2010, Condition B
Stabilization Bake	Method 1008, Condition C
Temperature Cycling	Method 1010, Condition C, 10 cycles −65°C to 150°C
Constant Acceleration	Method 2001, Condition E, 30k g Y1 axis (TO-3 PKG at 20k g)
Fine Leak	Method 1014, Condition A
Gross Leak	Method 1014, Condition C
Burn-in	Method 1015, 160 hrs at 125°C (or equivalent)
Final Electrical	+25°C DC (per LTC Data Sheet) PDA = 5%
	+125°C or 150°C DC
	−55°C DC
	+25°C AC
QA Acceptance	Method 5005 Group A (sample/lot)
Quality Conformance	Group B (sample/lot)
	Group C (sample every 3 months/Generic Group)
	Group D (sample every 6 months/Package Type)
External Visual	Method 2009

EXAMPLE

NOTE: Each operation is performed on a 100% basis unless otherwise stated.

FORM No. 00-03-6072

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP A DATA
Mil-Std-883, METHOD 5005

LTC P/N: ______________________ LOT #: ____________________
GENERIC TYPE: __________________ PKG: ____________________ DATE CODE: ________________
ASSEMBLY LOC: __________________

	ACC #	S/S	# FAILED	DATE TESTED	OPER NUMBER
SUBGROUP 1 Static tests at 25°C	0	116			
SUBGROUP 2 Static tests at maximum rated operating temperature	0	116			
SUBGROUP 3 Static tests at minimum rated operating temperature	0	116			
SUBGROUP 4 Dynamic tests at 25°C	0	116			
SUBGROUP 5 Dynamic tests at maximum rated operating temperature	0	116			
SUBGROUP 6 Dynamic tests at minimum rated operating temperature	0	116			
SUBGROUP 7 Functional tests at 25°C	0	116			
SUBGROUP 8 Functional tests at maximum and minimum operating temperature	0	116			
SUBGROUP 9 Switching tests at 25°C	0	116			
SUBGROUP 10 Switching tests at maximum rated operating temperature	0	116			
SUBGROUP 11 Switching tests at minimum rated operating temperature	0	116			

EXAMPLE

QA APPROVAL: ____________ DATE: ____________

FORM No. 00-03-6037

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP B DATA (Class B)
Mil-Std-883, METHOD 5005

LTC P/N: ____________ LOT #: ____________
GENERIC TYPE: ____________ PKG: ____________ DATE CODE: ____________
ASSEMBLY LOC: ____________

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 2 Resistance to Solvents	2015			0	4			
SUBGROUP 3 Solderability	2003	Soldering Temp. of 245°C ± 5°C	10	0				
SUBGROUP 5 Bond Strength	2011	C or D	15	0				

EXAMPLE

QA APPROVAL: ____________ DATE: ____________

FORM No. 00-03-6006

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP C DATA (Class B)
Mil-Std-883, METHOD 5005

LTC P/N: ____________ LOT #: ____________
GENERIC TYPE: ____________ PKG: ____________ DATE CODE: ____________
CT. GROUP: ____________

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Steady State Life Test	1005	$T_A = 125°C$ (1000 Hours or Equiv.)	5	0	45			
Electrical Endpoints		Test #						

EXAMPLE

QA APPROVAL: ____________ DATE: ____________

FORM No. 00-03-6007

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP B DATA (Class S)
Mil-Std-883, METHOD 5005

LTC P/N: ______________________ LOT #: ____________________
GENERIC TYPE: __________________ PKG: ____________________ DATE CODE: ________________
ASSEMBLY LOC: __________________

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1				0	3			
Physical Dimensions	2016							
Internal Water-Vapor Content	1018	5000 ppm Max						
SUBGROUP 2								
Resistance to Solvents	2015			0	4			
Internal Visual and Mechanical	2013, 2014	Design and Construction Requirements		0	2			
Bond Strength	2011	C or D	10	0	22 Wires			
Die Shear Test	2019			0	3			
SUBGROUP 3								
Solderability	2003 or 2022	Soldering Temp. of 245°C ±5°C	10	0	22 Leads			
SUBGROUP 4								
Lead Integrity	2004	B_2 (Lead Fatigue)	5	0	45 Leads			
Seal	1014							
Fine								
Gross								
Lid Torque	2024	Glass Frit Seal Only						
SUBGROUP 5								
Electrical End-Points		Test #	5	0	45			
Steady State Life	1005	C, D, or E						
Electrical End-Points		Test #						
SUBGROUP 6								
Electrical End-Points		Test #	15	0	15			
Temperature Cycling	1010	C 100 Cycles						
Constant Acceleration	2001	E Y_1 Only						
Seal	1014							
Fine								
Gross								
Electrical End-Points		Test #						
SUBGROUP 7								
ESD Classification	3015	Qual or Re-Design Only	15	N/A	—			

EXAMPLE

QA APPROVAL: ______________ DATE: ____________

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP D DATA (Class B or S)

Mil-Std-883, METHOD 5005

LTC P/N: ______________________ LOT #: ____________________
GENERIC TYPE: __________________ PKG: ____________________ DATE CODE: ________________
ASSEMBLY LOC: __________________

TEST	METHOD	CONDITION	LTPD	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1			15	0	15			
Physical Dimensions	2016							
SUBGROUP 2			5	0	45 Leads			
Lead Integrity	2004	B_2 (Lead Fatigue)						
Fine Leak	1014							
Gross Leak	1014							
SUBGROUP 3			15	0	15			
Thermal Shock	1011	B 15 Cycles						
Temperature Cycle	1010	C 100 Cycles						
Moisture Resistance	1004							
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1004/ 1010							
Electrical End-Points		Test #						
SUBGROUP 4			15	0	15			
Mechanical Shock	2002	B						
Vibration Variables-Frequency	2007	A						
Constant Acceleration	2001	E Y1 Only						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1010/ 1011							
Electrical End-Points		Test #						
SUBGROUP 5			15	0	15			
Salt Atmosphere	1009	A						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1009	Visual Criteria						
SUBGROUP 6				0	3			
Internal Water-Vapor	1018	5000 ppm Max						
SUBGROUP 7			15	0	15			
Adhesion of Lead Finish	2025							
SUBGROUP 8				0	5			
Lid Torque	2024	Glass Frit Seal Only						

EXAMPLE

QA APPROVAL: ____________ DATE: ____________

FORM No. 00-03-6008

MILITARY PARTS LIST

JAN S QPL

JM38510/10103SGA (LM101AH)
JM38510/10103SHA (LM101AW)
JM38510/10103SPA (LM101AJ8)
JM38510/10104SCA (LM108AJ)
JM38510/10104SGA (LM108AH)
JM38510/10104SHA (LM108AW)
JM38510/10104SPA (LM108AJ8)
JM38510/10304SGA (LM111H)
JM38510/10306SCA (LM119J)
JM38510/10306SIA (LM119H)
JM38510/10306SHA (LM119W)
JM38510/10307SCA (LM119AJ)
JM38510/10307SIA (LM119AH)
JM38510/10307SHA (LM119AW)
JM38510/11402SGA (LF156H)
JM38510/11404SGA (LF155AH)
JM38510/11405SGA (LF156AH)
JM38510/11703SXA (LM117H)
JM38510/11704SYA (LM117K)
JM38510/11803SXA (LM137H)
JM38510/11804SYA (LM137K)
JM38510/12407SGA (LT1021-5H)
JM38510/12409SGA (LT1021-10H)
JM38510/12501SGA (LF198H)
JM38510/12601SEA (LT1524J)
JM38510/13501SGA (OP07AH)
JM38510/13501SPA (OP07AJ8)
JM38510/13502SGA (OP07H)
JM38510/13502SPA (OP07J8)
JM38510/13503SGA (OP27AH)
JM38510/13503SPA (OP27AJ8)
JM38510/14802SXA (LT1009H3)

JAN B QPL

JM38510/10103BCA (LM101AJ)
JM38510/10103BGA (LM101AH)
JM38510/10103BHA (LM101AW)
JM38510/10103BPA (LM101AJ8)
JM38510/10104BCA (LM108AJ)
JM38510/10104BGA (LM108AH)
JM38510/10104BPA (LM108AJ8)
JM38510/10106BEA (LH2108AD)
JM38510/10107BCA (LM118J)
JM38510/10107BGA (LM118H)
JM38510/10107BHA (LM118W)
JM38510/10107BPA (LM118J8)
JM38510/10304BGA (LM111H)
JM38510/10306BIA (LM119H)
JM38510/10306BCA (LM119J)
JM38510/10306BHA (LM119W)
JM38510/10307BCA (LM119AJ)
JM38510/10307BIA (LM119AH)
JM38510/10307BHA (LM119AW)
JM38510/11401BGA (LF155H)
JM38510/11401BPA (LF156J8)
JM38510/11402BGA (LF156H)
JM38510/11402BHA (LF156W)
JM38510/11402BPA (LF156J8)
JM38510/11404BGA (LF155AH)
JM38510/11404BPA (LF155AJ8)
JM38510/11405BGA (LF156AH)
JM38510/11405BHA (LF156W)
JM38510/11405BPA (LF156AJ8)
JM38510/11703BXA (LM117H)
JM38510/11704BYA (LM117K)
JM38510/11706BYA (LM138K
JM38510/11803BXA (LM137H)
JM38510/11804BYA (LM137K)
JM38510/12407BGA (LT1021-5H)
JM38510/12409BGA (LT1021-10H)
JM38510/12501BGA (LF198H)
JM38510/12601BEA (SG1524J)
JM38510/13501BGA (OP07AH)
JM38510/13501BPA (OP07AJ8)
JM38510/13502BGA (OP07H)
JM38510/13502BPA (OP07J8)
JM38510/13503BGA (OP27AH)
JM38510/13503BPA (OP27AJ8)
JM38510/14802BXA (LT1009H)

DESC Drawings

7703401XA (LM117H)
7703401YA (LM117K)
7703402XA (LM117HVH)
7703402YA (LM117HVK)
7703403XA (LM137H)
7703403YA (LM137K)
7703404XA (LM137HVH)
7703404YA (LM137HVK)
7703405XA (LT117AH)
7703405YA (LT117AK)
7703406XA (LT137AH)
7703406YA (LT137AK)
7703407XA (LT117AHVH)
7703407YA (LT117AHVK)
7703408XA (LT137AHVH)
7703408YA (LT137AHVK)
7802801EA (SG1524J)
8203601GA (OP07AH)
8203601PA (OP07AJ8)
8203602GA (OP07H)
8203602PA (OP07J8)
8418001XA (LM136AH-2.5)
8551401GA (REF02AH)
8551401PA (REF02AJ8)
8551501VA (LT1526J)
8601401CA (LM119J)
8601401HA (LM119W)
8601401IA (LM119H)
8601402CA (LT119AJ)
8601402HA (LT119AW)
8601402IA (LT119AH)

Standard Military Drawings (SMD)

5962-8680601EA (LT1846J)
5962-8680602EA (LT1847J)
5962-8684501IA (LT1016MH)
5962-8684501PA (LT1016MJ8)
5962-8686101XA (LT580SH)
5962-8686102XA (LT580TH)
5962-8686103XA (LT580UH)
5962-8688201XA (LH0070-0H)
5962-8688202XA (LH0070-1H)
5962-8688203XA (LH0070-2H)
5962-8688701CA (OP227AJ)
5962-8757801GA (LT1007AMH)
5962-8757801PA (LT1007AMJ8)
5962-8759401XA (LM185H-1.2)
5962-8759402XA (LM185H-2.5)
5962-8760401GA (LM10H)
5962-8760401PA (LM10J8)
5962-8766601VA (LT1080MJ)
5962-8766602EA (LT1081MJ)
5962-8767501XA (LM150K)
5962-8767502XA (LT150AK)
5962-8771501CA (LT1002AMJ)
5962-8773801GA (LT1001MH)
5962-8773801PA (LT1001MJ8)
5962-8774101XA (LT1033MK)
5962-8777501YA (LM123K)
5962-8853701GA (OP37AH)
5962-8853701PA (OP37AJ8)
5962-8853702GA (OP37BH)
5962-8853702PA (OP37BJ8)
5962-8853703GA (OP37CH)
5962-8853703PA (OP37CJ8)
5962-8853801GA (OP215AH)
5962-8853801PA (OP215AJ8)
5962-8853802GA (OP215BH)
5962-8853802PA (OP215BJ8)
5962-8856101XA (LM199AH)
5962-8856102XA (LM199H)
5962-8856201XA (LT1010MH)
5962-8856201YA (LT1010MK)
5962-8856701GA (LT1037AMH)
5962-8856701PA (LT1037AMJ8)
5962-8859701XA (LT1004MH-1.2)
5962-8859702XA (LT1004MH-2.5)
5962-8860001GA (LT1021BMH-10)
5962-8860002GA (LT1021CMH-10)
5962-8860003GA (LT1021DMH-10)
5962-8862201GA (LT1028MH)
5962-8862201PA (LT1028MJ8)
5962-8862202GA (LT1028AMH)
5962-8862202PA (LT1028AMJ8)
5962-8864101RA (LTC1060AMJ)
5962-8864102RA (LTC1060MJ)
5962-8864601XA (LT1085MK)
5962-8864701GA (LT1021BMH-7)
5962-8864702GA (LT1021DMH-7)
5962-8875101VA (LT1039MJ)
5962-8875102EA (LT1039MJ16)
5962-8876001GA (LT1013AMH)
5962-8876001PA (LT1013AMJ8)
5962-8876002GA (LT1013MH)
5962-8876002PA (LT1013MJ8)
5962-8876201GA (LT1021BMH-5)
5962-8876202GA (LT1021CMH-5)
5962-8876203GA (LT1021DMH-5)
5962-8950401GA (LT1017MH)
5962-8950401PA (LT1017MJ8)
5962-8950402GA (LT1018MH)
5962-8950402PA (LT1018MJ8)
5962-8951101EA (LT1525AJ)
5962-8951102EA (LT1527AJ)
5962-8952101XA (LT1084MK)
5962-8956201GA (LT1054MH)
5962-8956201PA (LT1054MJ8)
5962-8958101GA (REF01AH)
5962-8958101PA (REF01AJ8)
5962-8961001XA (LT1009MH)
5962-8962201GA (LT1022AMH)
5962-8962202GA (LT1022MH)
5962-8967701CA (LT1014AMJ)
5962-8967702CA (LT1014MJ)
5962-8978201CA (LTC1052MJ)
5962-8978201GA (LTC1052MH)
5962-8078201PA (LTC1052MJ8)
5962-8980201XA (LT1031BH)
5962-8980202XA (LT1031CH)
5962-8980203XA (LT1031DH)
5962-8983001RA (LTC1090MJ)
5962-8992101XA (LM129AH)
5962-8992102XA (LM129BH)
5962-8992103XA (LM129CH)
5962-8997601GA (LT1055AMH)
5962-8997602GA (LT1056AMH)
5962-8997603GA (LT1055MH)
5962-8997604GA (LT1056MH)
5962-8998101YA (LT1086MK)
5962-9059501GA (LT1019AMH-10)
5962-9059502GA (LT1019AMH-5)
5962-9059503GA (LT1019AMH-4.5)
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5962-9059505GA (LT1019MH-10)
5962-9059506GA (LT1019MH-5)
5962-9059507GA (LT1019MH-4.5)
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5962-9062701GA (LT1011AMH)
5962-9062701PA (LT1011AMJ8)
5962-9062702GA (LT1011MH)
5962-9062702PA (LT1011MJ8)
5962-9064901CA (LT1064-4MJ)
5962-9064901XA (LT1064-4ML)
5962-9082501MYA (LT1070MK)
5962-9082502MYA (LT1071MK)
5962-9082503MYA (LT1072MK)
5962-9082503MPA (LT1072MJ8)
5962-9082504MYA (LT1070HVMK)
5962-9082505MYA (LT1071HVMK)
5962-9082506MYA (LT1072HVMK)
5962-9084101MCA (LT1020MJ)

Radiation Hardened

RH07
RH27C
RH37C
RH101A
RH108A
RH111
RH117
RH118
RH119
RH129
RH137
RH1009
RH1011
RH1013
RH1014
RH1021-5
RH1021-7
RH1021-10
RH1056

MILITARY PARTS LIST

883 Operational Amplifiers

LF155AH/883
LF155H/883
LF156AH/883
LF156H/883
LF156J8/883
LF156W/883
LF412AMH/883
LF412MH/883
LF412AMJ8/883
LF412MJ8/883
LH0070-0H/883
LH0070-1H/883
LH0070-2H/883
LH2108AD/883
LH2108D/883
LM10H/883
LM10J8/883
LM101AH/883
LM101AJ8/883
LM107H/883
LM107J8/883
LM108AH/883
LM108H/883
LM108AJ8/883
LM118H/883
LM118J8/883
LM118W/883
LT118AH/883
LT118AJ8/883
LT1001AMH/883
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LT1008MH/883
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LT1012MH/883
LT1013AMH/883
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LT1013MH/883
LT1013MJ8/883
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LT1014MJ/883
LT1022AMH/883
LT1022MH/883
LT1024AMD/883
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LT1028AMH/883
LT1028AMJ8/883
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LT1028MJ8/883
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LT1037AMJ8/883
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LT1037MJ8/883
LT1055AMH/883
LT1055MH/883
LT1056AMH/883
LT1056MH/883
LT1057AMH/883
LT1057AMJ8/883
LT1057MH/883
LT1057MJ8/883
LT1058AMJ/883
LT1058AML/883
LT1058MJ/883
LT1073AW/883
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LT1127AMJ8/883
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OP-16BH/883
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OP-27CJ8/883
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OP-37CH/883
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OP-215AH/883
OP-215AJ8/883
OP-215CH/883
OP-215CJ8/883
OP-227AJ/883
OP-227CJ/883
OP-237AJ/883
OP-237CJ/883

883 Regulators

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LM117HVH/883
LM117HVK/883
LM117K/883
LM123K/883
LM137H/883
LM137HVH/883
LM137HVK/883
LM137K/883
LM138K/883
LM150K/883
LT117AH/883
LT117AHVH/883
LT117AHVK/883
LT117AK/883
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LT150AK/883
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LT1083MK-5/883
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LT1084MK/883
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LT1086MK-5/883
LT1086MK-12/883
LT1120MJ8/883

883 References

LM129AH/883
LM129BH/883
LM129CH/883
LM134H/883
LM134H-3/883
LM134H-6/883
LM136AH-2.5/883
LM136H-2.5/883
LM185H-1.2/883
LM185H-2.5/883
LM199AH/883
LM199AH-20/883
LM199H/883
LT580SH/883
LT580TH/883
LT580UH/883
LT581SH/883
LT581TH/883
LT581UH/883
LT1004MH-1.2/883
LT1004MH-2.5/883
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LT1031CMH/883
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LT1034MH-2.5/883
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REF-01AJ8/883
REF-01H/883
REF-01J8/883
REF-02AH/883
REF-02AJ8/883
REF-02H/883
REF-02J8/883

883 Comparators

LM111H/883
LM111J8/883
LM119H/883
LM119J/883
LM119W/883
LT111AH/883
LT111AJ8/883
LT119AH/883
LT119AJ/883
LT685MH/883
LT685MJ/883
LT1011AMH/883
LT1011AMJ8/883
LT1011MH/883
LT1011MJ8/883
LT1016MH/883
LT1016MJ/883
LT1016MJ8/883
LT1017MH/883
LT1017MJ8/883
LT1018MH/883
LT1018MJ8/883
LTC1040MJ/883
LTC1042MJ8/883

883 Switched-Mode Control Circuits

LT1070MK/883
LT1070HVMK/883
LT1071MK/883
LT1071HVMK/883
LT1072MK/883
LT1072HVMK/883
LT1072MJ8/883
LT1241MJ8/883
LT1242MJ8/883
LT1243MJ8/883
LT1244MJ8/883
LT1245MJ8/883
LT1524J/883
LT1525AJ/883
LT1526J/883
LT1527AJ/883
LT1846J/883
LT1847J/883
SG1524J/883
SG1525AJ/883
SG1527AJ/883

883 Interface

LT1032MJ/883
LT1039MJ/883
LT1039MJ16/883
LT1080MJ/883
LT1081MJ/883
LTC1045MJ/883
LT1280MJ/883
LT1281MJ/883

883 Filters

LTC1059AMJ/883
LTC1059MJ/883
LTC1060AMJ/883
LTC1060MJ/883
LTC1061AMJ/883
LTC1061MJ/883
LTC1062MJ8/883
LTC1064MJ/883
LTC1064-1MJ/883
LTC1064-2MJ/883
LTC1064-2ML/883
LTC1064-4ML/883
LTC1164MJ/883

883 Data Converters

LTC1090MJ/883
LTC1091MJ8/883
LTC1092MJ8/883
LTC1093MJ/883
LTC1094MJ/883
LTC1290BMJ/883
LTC1290CMJ/883
LTC1290DMJ/883

Other 883

LF198AH/883
LF198H/883
LT1010MH/883
LT1010MK/883
LTC201AMJ/883
LTC1041MJ8/883
LTC1043MD/883
LTC1044MH/883
LTC1044MJ8/883

SECTION 13—NEW PRODUCTS

SECTION 13—NEW PRODUCTS

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PRELIMINARY

LTC488

Quad RS485 Line Receiver

September 1991

FEATURES

- Low Power : Icc=8 mA typ.
- Designed for RS485 or RS422 applications.
- Single +5V supply.
- -7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- 70 mV typical input hysteresis.
- Receiver maintains high impedance in Three-state or with the power off.
- 25 nS typical receiver propagation delay.
- Pin compatiable with the SN75173.

APPLICATIONS

- Low Power RS485/RS422 Receivers
- Level translator

DESCRIPTION

The LTC488 is a low power differential bus/line receiver designed for multipoint data transmission standard RS485 applications with extended common mode range (+12V to -7V). It also meets the requirements of RS422.

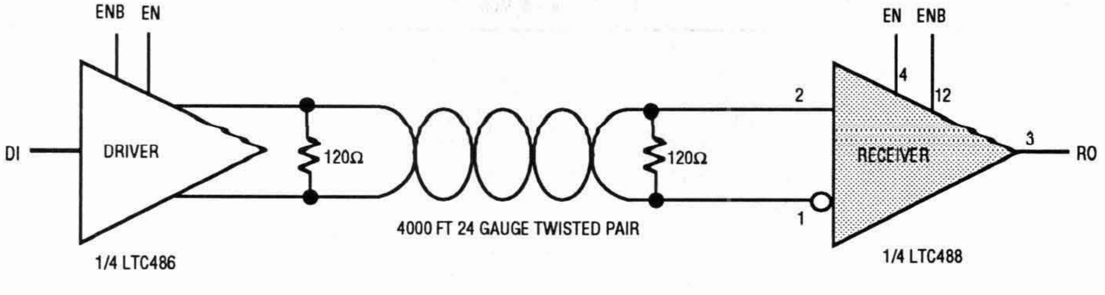
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

The receiver features three-state outputs, with the receiver output maintaining high impedance over the entire common mode range.

The receiver has a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed from 0°C to 70°C and 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Note1)

Supply Voltage (Vcc)..12V

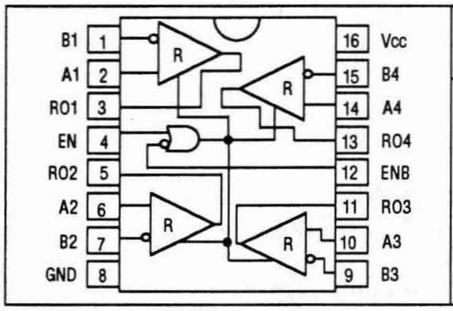
Control Input Currents...........................-25mA to 25mA

Control Input Voltages.......................-0.5V to Vcc+0.5V

Receiver Input Voltages ....±14V

Receiver Output Voltages.................-0.5V to Vcc+0.5V

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC488CN
LTC488CS
LTC488IN
LTC488IS

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ± 5% , 0 °C ≤ Temp. ≤ 70 °C (Note 2 &3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Vih	Input High Voltage	EN, ENB		2.0			V
Vil	Input Low Voltage					0.8	V
Iin1	Inout Current					±2	μA
Iin2	Input Current (A, B)	Vcc=0V or 5.25V	Vin = 12V			+1.0	mA
			Vin = -7V			-0.8	mA
Vth	Differential Input Threshold Voltage for Receiver	-7V ≤ Vcm ≤ 12V		-0.2		+0.2	V
ΔVth	Receiver Input Hysteresis	Vcm = 0V			70		mV
Voh	Receiver Output High Voltage	Io=-4mA, Vid=+0.2V		3.5			V
Vol	Receiver Output Low Voltage	Io=+4mA, Vid=-0.2V				0.4	V
Iozr	Three-State Output Current at Receiver	Vcc = Max. 0.4V ≤ Vo ≤2.4V				±1	μA
Icc	Supply Current	No Load; D=GND, or Vcc			8		mA
Rin	Receiver Input Resistance	-7 V ≤ Vcm ≤ +12 V		12			KΩ
Iosr	Receiver Short-Circuit Current	0 V ≤ Vo ≤ Vcc		7		85	mA

SWITCHING CHARACTERISTICS

Vcc = 5V ± 5% , 0°C ≤ Temp. ≤ 70°C (Note 2 &3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Receiver Input to Output	$C_L = 15pF$ (Figures 1&3)		25		nS
t_{PHL}	Receiver Input to Output			25		nS
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew			13		nS
t_{ZL}	Receiver Enable to Output Low	$C_L = 15pF$ (Figures 2&4) S1 closed		20		nS
t_{ZH}	Receiver Enable to Output High	$C_L = 15pF$ (Figures 2&4) S2 closed		20		nS
t_{LZ}	Receiver Disable from Low	$C_L = 15pF$ (Figures 2&4) S1 closed		20		nS
t_{HZ}	Receiver Disable from High	$C_L = 15pF$ (Figures 2&4) S2 closed		20		nS

Note 1 : "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2 : All currents into device pins are positive ; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3 : All typicals are given for Vcc = 5 V and Temp. = 25 °C.

FUNCTION TABLE

DIFFERENTIAL	ENABLES		OUTPUT
A - B	EN	ENB	RO
Vid ≥ 0.2 V	H	X	H
	X	L	H
-0.2 V < Vid < 0.2 V	H	X	?
	X	L	?
Vid ≤ 0.2 V	H	X	L
	X	L	L
X	L	H	Z

H : High Level
L : Low Level
X : Irrelevant
? : Indeterminate
Z : High-Impedance (off)

PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1	B1	Receiver1 input.
2	A1	Receiver1 input.
3	RO1	Receiver1 output. If the receiver output is enabled, then if A > B by 200 mV, RO1 will be high. If A < B by 200 mV, then RO1 will be low.
4	EN	Receiver output enabled. See FUNCTION TABLE for details.
5	RO2	Receiver2 output. Refer to RO1.
6	A2	Receiver2 input.
7	B2	Receiver2 input.
8	GND	Ground Connection.
9	B3	Receiver3 input.
10	A3	Receiver3 input.
11	RO3	Receiver3 output. Refer to RO1.
12	ENB	Receiver output disenabled. See FUNCTION TABLE for details.
13	RO4	Receiver4 ouput. Refer to RO1.
14	A4	Receiver4 input.
15	B4	Receiver4 input.
16	Vcc	Positive supply ; $4.75V \leq Vcc \leq 5.25V$

SWITCHING TIME WAVEFORMS

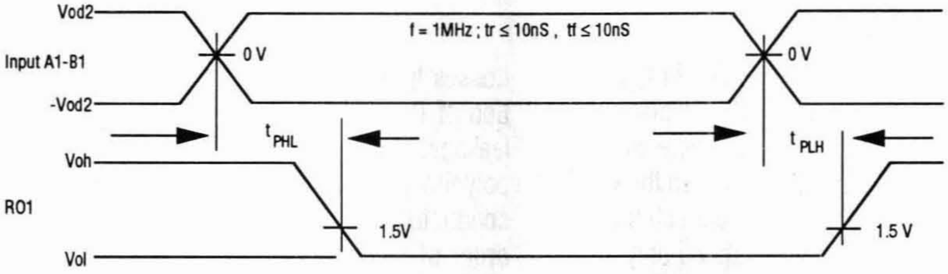


Figure 3. Receiver Propagation Delays

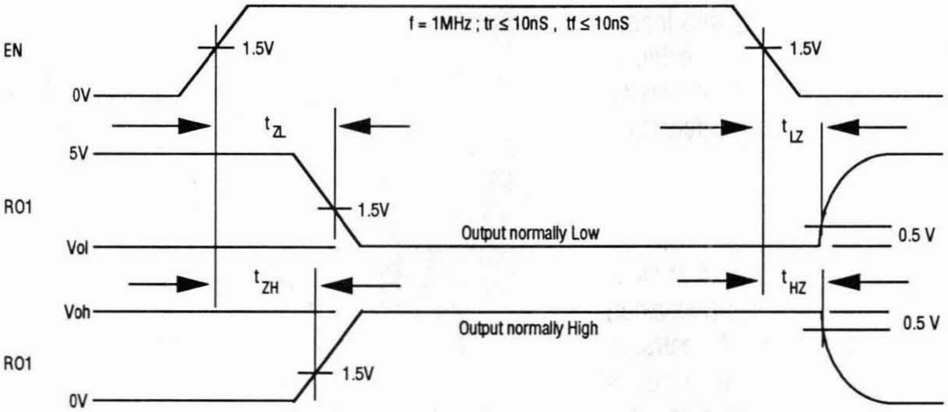


Figure 4. Receiver Enable and Disable Times

TEST CIRCUITS

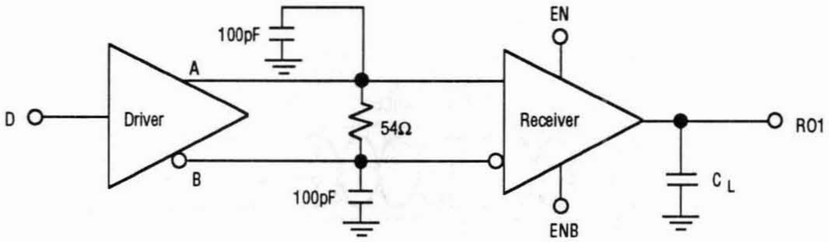

100pF
D
Driver
A
B
54Ω
100pF
EN
Receiver
ENB
RO1
C L

Figure 1. Receiver Timing Test Circuit

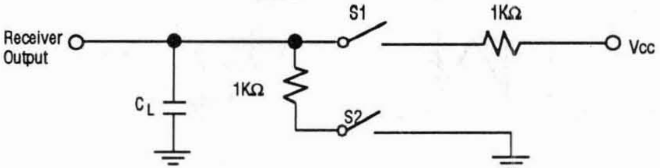

Receiver Output
C L
S1
1KΩ
1KΩ
S2
Vcc

Figure 2. Receiver Enable and Disable Timing Test Circuit

Note : The input pulse is supplied by a generator having the following characteristics:
f=1MHZ , duty cycle=50%, tr≤10nS, tf≤10nS, Zout=50Ω.

APPLICATIONS INFORMATION

TYPICAL APPLICATION

A typical connection of the LTC488 is shown in Figure 1. Two twisted pair wires connect up to 32 driver/receiver pairs for half duplex data transmission. There are no restrictions on where the chips are connected to the wires, and it isn't necessary to have the chips connected at the ends . However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120 Ω. The input impedance of a receiver is typically 20 kΩ to GND, or 0.6 unit RS-485 load, so in practice 50 to 60 transceivers can be connected to the same wires. The optional shields around the twisted pair help reduce unwanted noise, and are connected to GND at one end.

CABLES AND DATA RATE

The transmission line of choice for RS-485 applications is a twisted pair. There are coaxial cables (twinaxial) made for this purpose that contain straight pairs, but these are less flexible, more bulky, and more costly than twisted pairs. Many cable manufacturers offer a broad range of 120 Ω cables designed for RS-485 applications.

Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage, and AC losses in the dielectric. In good polyethylene cables such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low over all loss (Figure 2).

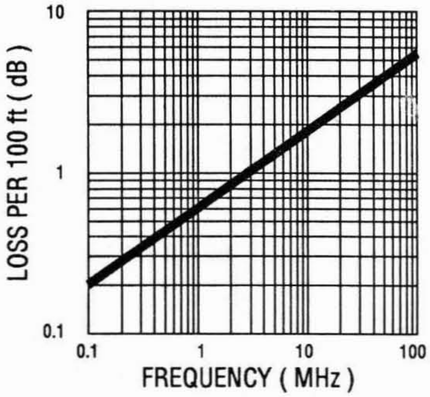


Figure 2. Attenuation - vs - Frequency For Belden 9481

When using low loss cables, Figure 3 can be used as a

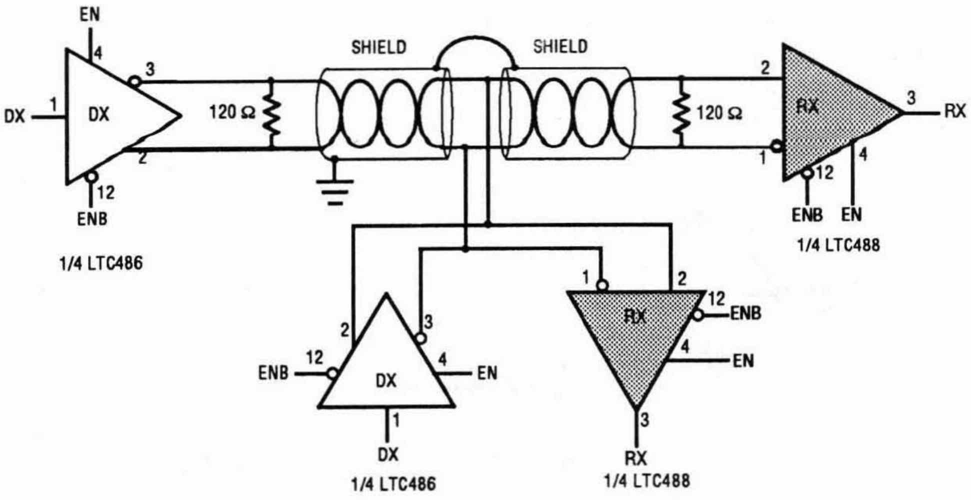


Figure 1. Typical Connection

APPLICATIONS INFORMATION

guideline for choosing the maximum line length for a given data rate. With lower quality PVC cables, the dielectric loss factor can be 1000 times worse. PVC twisted pairs have terrible losses at high data rates (> 100 kbs), and greatly reduce the maximum cable length. At low data rates however, they are acceptable and much more economical.

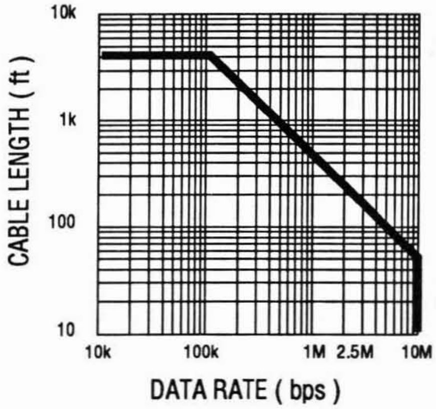


Figure 3. Cable Length - vs - Data Rate

CABLE TERMINATION

The proper termination of the cable is very important. If the cable is not terminated with it's characteristic impedance, distorted waveforms will result. In severe cases, distorted (false) data and nulls will occur. A quick look at the output of the driver will tell how well the cable is terminated. It is best to look at a driver connected to the end of the cable, since this eliminates the possibility of getting reflections from two directions. Simply look at the driver output while transmitting square wave data. If the cable is terminated properly, the waveform will look like a square wave (Figure 4).

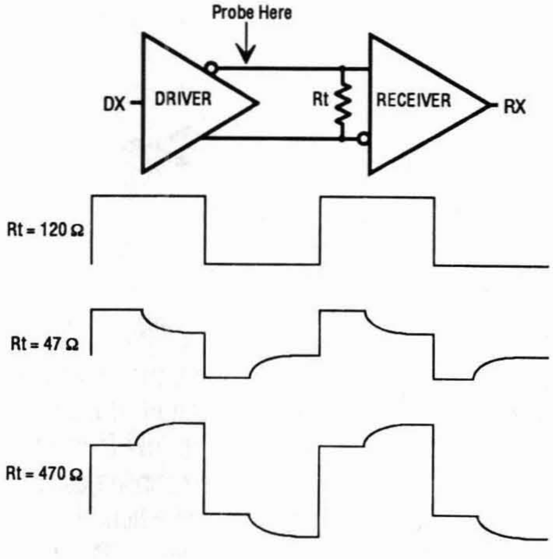


Figure 4. Termination Effects

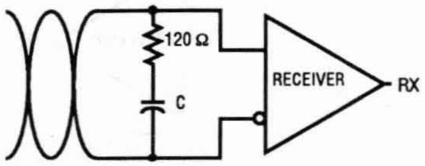
If the cable is loaded excessively (47 Ω), the signal initially sees the surge impedance of the cable and jumps to an initial amplitude. The signal travels down the cable and is reflected back out of phase because of the mistermination. When the reflected signal returns to the driver, the amplitude will be lowered. The width of the pedestal is equal to twice the electrical length of the cable (about 1.5 ns / foot) . If the cable is lightly loaded (470 Ω), the signal reflects in phase and increases the amplitude at the driver output. An input frequency of 30 kHz is adequate for tests out to 4000 ft. of cable.

AC CABLE TERMINATION

Cable termination resistors are necessary to prevent unwanted reflections, but they consume power. The typical differential output voltage of the driver is 2 V when the cable is terminated with two 120 Ω resistors, causing 33 mA of DC current to flow in the cable when no data is being sent. This DC current is about 60 times greater than the supply current of the LTC488. One way to eliminate the

APPLICATIONS INFORMATION

unwanted current is by AC coupling the termination resistors as shown in Figure 5.



C = Line Length (ft) x 16.3 pF

Figure 5. AC Coupled Termination

The coupling capacitor must allow high-frequency energy to flow to the termination, but block DC and low frequencies. The dividing line between high and low frequency depends on the length of the cable. The coupling capacitor must pass frequencies above the point where the line represents an electrical one-tenth wavelength. The value of the coupling capacitor should therefore be set at 16.3 pF per foot of cable length for 120 Ω cables. With the coupling capacitors in place, power is consumed only on the signal edges, and not when the driver output is idling at a 1 or 0 state. A 100 nF capacitor is adequate for lines up to 4000 ' in length. Be aware that the power savings start to decrease once the data rate surpasses 1/(120 Ω x C).

RECEIVER OPEN-CIRCUIT FAIL-SAFE

Some data encoding schemes require that the output of the receiver maintains a known state (usually a logic 1) when the data is finished transmitting and all drivers on the line are forced into tri-state. The receiver of the LTC488 has a fail-safe feature which guarantees the output to be in a logic 1 state when the receiver inputs are left floating (open-circuit). However, when the cable is terminated with 120 Ω, the differential inputs to the receiver are shorted together, not left floating. Because the receiver has about 70 mV of hysteresis, the receiver output will maintain the last data bit received.

If the receiver output must be forced to a known state, the circuits of Figure. 6 can be used.

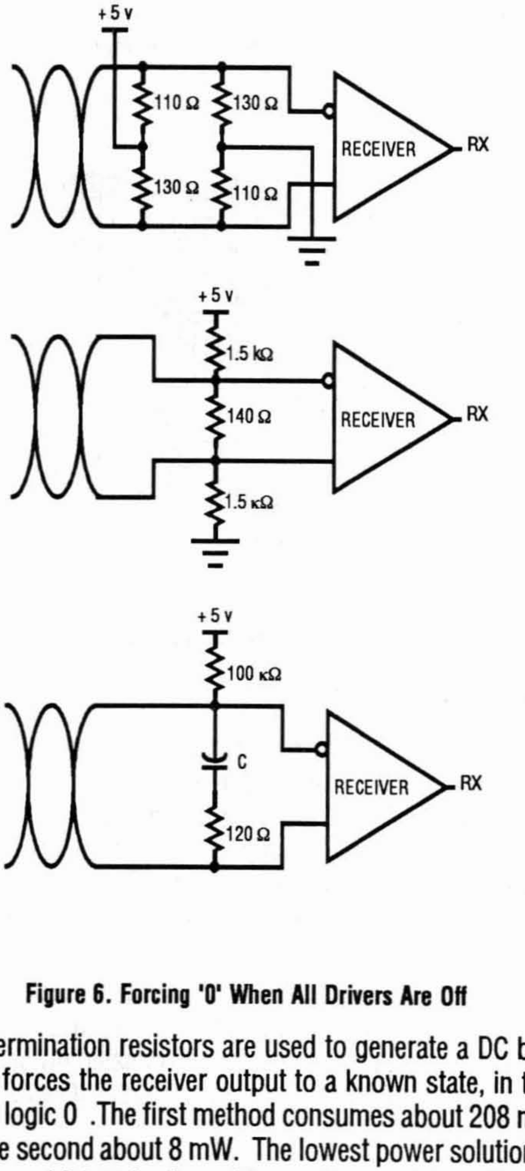


Figure 6. Forcing '0' When All Drivers Are Off

The termination resistors are used to generate a DC bias which forces the receiver output to a known state, in this case a logic 0 .The first method consumes about 208 mW and the second about 8 mW. The lowest power solution is to use an AC termination with a pull-up resistor. Simply swap the receiver inputs for data protocols ending in logic 1.

APPLICATIONS INFORMATION

FAULT PROTECTION

All of LTC's RS-485 products are protected against ESD transients up to 2 kV using the human body model (100 pF,1.5 kΩ). However, some applications need more protection. The best protection method is to connect a bidirectional TransZorb from each line side pin to ground (Figure 7).

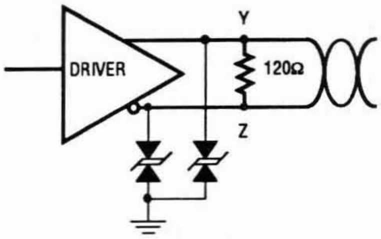
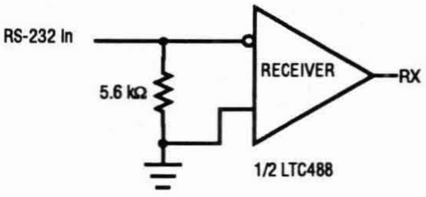


Figure 7. ESD Protection With TransZorbs

A TransZorb is a silicon transient voltage suppressor that has exceptional surge handling capabilities, fast response time, and low series resistance. They are available from General Semiconductor Industries and come in a variety of breakdown voltages and prices. Be sure to pick a breakdown voltage higher than the common mode voltage required for your application (typically 12 V). Also, don't forget to check how much the added parasitic capacitance will load down the bus.

TYPICAL APPLICATIONS

RS-232 Receiver



PRELIMINARY

LTC489

Quad RS485 Line Receiver

September 1991

FEATURES

- Low Power : Icc=8 mA typ.
- Designed for RS485 or RS422 applications.
- Single +5V supply.
- -7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- 70 mV typical input hysteresis.
- Receiver maintains high impedance in Three-state or with the power off.
- 25 nS typical receiver propagation delay.
- Pin compatiable with the SN75175.

APPLICATIONS

- Low Power RS485/RS422 Receivers
- Level translator

DESCRIPTION

The LTC489 is a low power differential bus/line receiver designed for multipoint data transmission standard RS485 applications with extended common mode range (+12V to -7V). It also meets the requirements of RS422.

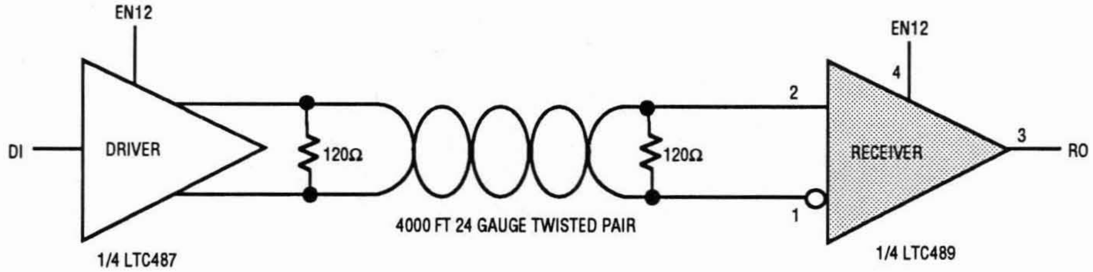
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

The receiver features three-state outputs, with the receiver output maintaining high impedance over the entire common mode range.

The receiver has a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed from 0°C to 70°C and 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION

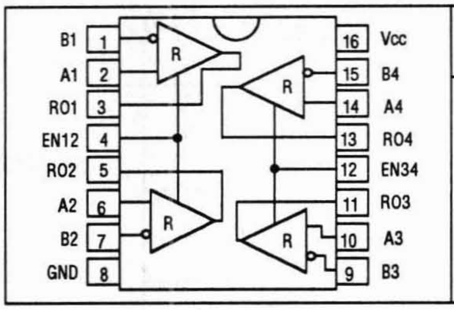


ABSOLUTE MAXIMUM RATINGS

(Note1)

Supply Voltage (Vcc)..12V
Control Input Currents...........................-25mA to 25mA
Control Input Voltages......................-0.5V to Vcc+0.5V
Receiver Input Voltages ....±14V
Receiver Output Voltages................-0.5V to Vcc+0.5V

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC489CN
LTC489CS
LTC489IN
LTC489IS

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ± 5% , 0 °C ≤ Temp. ≤ 70 °C (Note 2 &3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Vih	Input High Voltage	EN12, EN34		2.0			V
Vil	Input Low Voltage					0.8	V
Iin1	Inout Current					±2	μA
Iin2	Input Current (A, B)	Vcc=0V or 5.25V	Vin = 12V			+1.0	mA
			Vin = -7V			-0.8	mA
Vth	Differential Input Threshold Voltage for Receiver	-7V ≤ Vcm ≤ 12V		-0.2		+0.2	V
ΔVth	Receiver Input Hysteresis	Vcm = 0V			70		mV
Voh	Receiver Output High Voltage	Io=-4mA, Vid=+0.2V		3.5			V
Vol	Receiver Output Low Voltage	Io=+4mA, Vid=-0.2V				0.4	V
Iozr	Three-State Output Current at Receiver	Vcc = Max. 0.4V ≤ Vo ≤2.4V				±1	μA
Icc	Supply Current	No Load; D=GND, or Vcc			8		mA
Rin	Receiver Input Resistance	-7 V ≤ Vcm ≤ +12 V		12			KΩ
Iosr	Receiver Short-Circuit Current	0 V ≤ Vo ≤ Vcc		7		85	mA

Switching Characteristics

Vcc = 5V ± 5% , 0°C ≤ Temp. ≤ 70°C (Note 2 &3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Receiver Input to Output	C_L = 15pF (Figures 1&3)		25		nS
t_{PHL}	Receiver Input to Output			25		nS
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew			13		nS
t_{ZL}	Receiver Enable to Output Low	C_L = 15pF (Figures 2&4) S1 closed		20		nS
t_{ZH}	Receiver Enable to Output High	C_L = 15pF (Figures 2&4) S2 closed		20		nS
t_{LZ}	Receiver Disable from Low	C_L = 15pF (Figures 2&4) S1 closed		20		nS
t_{HZ}	Receiver Disable from High	C_L = 15pF (Figures 2&4) S2 closed		20		nS

Note 1 : "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2 : All currents into device pins are positive ; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3 : All typicals are given for Vcc = 5 V and Temp. = 25 °C.

FUNCTION TABLE

DIFFERENTIAL	ENABLES	OUTPUT
A - B	EN12 or EN34	RO
Vid ≥ 0.2 V	H	H
-0.2 V < Vid < 0.2 V	H	?
Vid ≤ 0.2 V	H	L
X	L	Z

H : High Level
L : Low Level
X : Irrelevant
? : Indeterminate
Z : High-Impedance (off)

PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1	B1	Receiver1 input.
2	A1	Receiver1 input.
3	RO1	Receiver1 output. If the receiver output is enabled, then if A > B by 200 mV, RO1 will be high. If A < B by 200 mV, then RO1 will be low.
4	EN12	Receiver 1, 2 output enabled. See FUNCTION TABLE for details.
5	RO2	Receiver2 output. Refer to RO1.
6	A2	Receiver2 input.
7	B2	Receiver2 input.
8	GND	Ground Connection.
9	B3	Receiver3 input.
10	A3	Receiver3 input.
11	RO3	Receiver3 output. Refer to RO1.
12	EN34	Receiver 3, 4 output enabled. See FUNCTION TABLE for details.
13	RO4	Receiver4 ouput. Refer to RO1.
14	A4	Receiver4 input.
15	B4	Receiver4 input.
16	Vcc	Positive supply ; 4.75V ≤ Vcc ≤ 5.25V

SWITCHING TIME WAVEFORMS

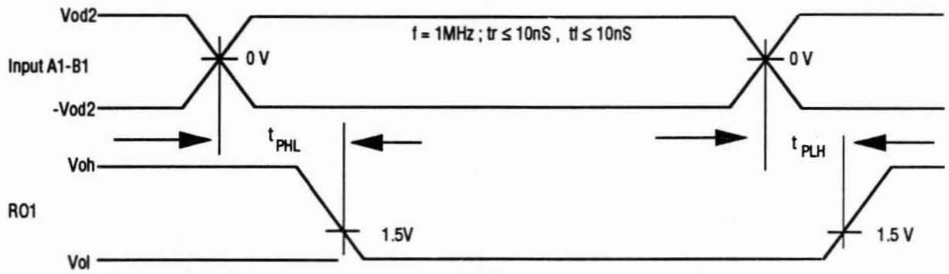

Vod2
Input A1-B1
-Vod2
0 V
f = 1MHz ; tr ≤ 10nS , tf ≤ 10nS
0 V
t PHL
t PLH
Voh
RO1
Vol
1.5V
1.5 V

Figure 3. Receiver Propagation Delays

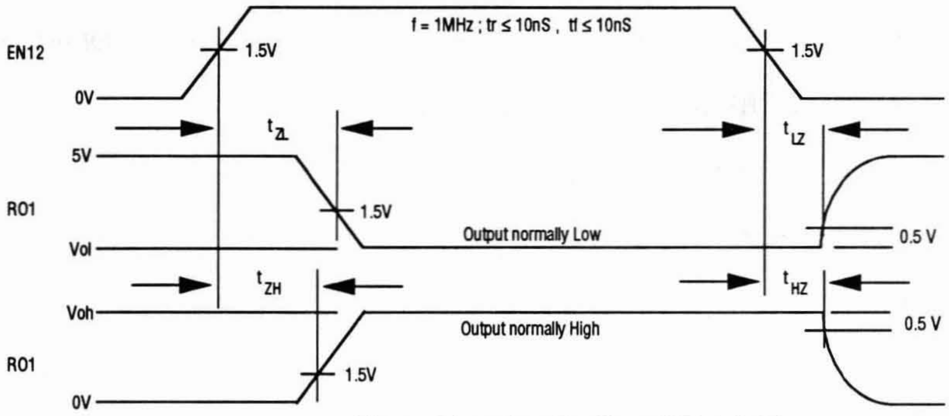

EN12
0V
1.5V
f = 1MHz ; tr ≤ 10nS , tf ≤ 10nS
1.5V
t ZL
t LZ
5V
RO1
Vol
1.5V
Output normally Low
0.5 V
t ZH
t HZ
Voh
RO1
0V
Output normally High
0.5 V
1.5V

Figure 4. Receiver Enable and Disable Times

TEST CIRCUITS

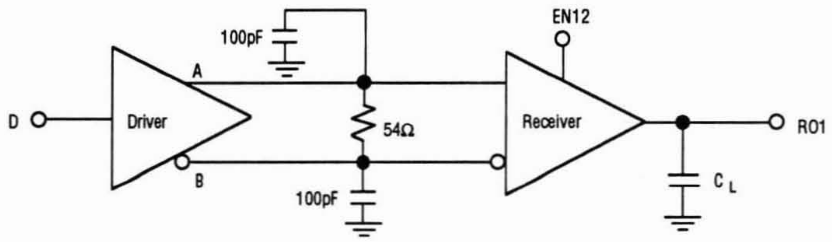

100pF
A
D
Driver
B
54Ω
100pF
EN12
Receiver
RO1
C L

Figure 1. Receiver Timing Test Circuit

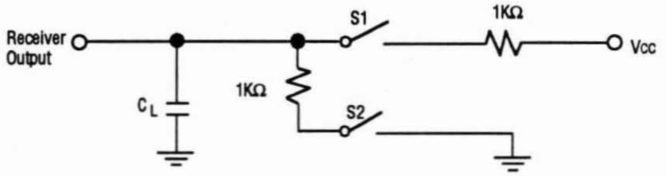

Receiver Output
C L
1KΩ
S1
1KΩ
Vcc
S2

Figure 2. Receiver Enable and Disable Timing Test Circuit

Note : The input pulse is supplied by a generator having the following characteristics:
f=1MHZ , duty cycle=50%, tr≤10nS, tf≤10nS, Zout=50Ω.

APPLICATIONS INFORMATION

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A typical connection of the LTC489 is shown in Figure 1. Two twisted pair wires connect up to 32 driver/receiver pairs for half duplex data transmission. There are no restrictions on where the chips are connected to the wires, and it isn't necessary to have the chips connected at the ends . However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120 Ω. The input impedance of a receiver is typically 20 kΩ to GND, or 0.6 unit RS-485 load, so in practice 50 to 60 transceivers can be connected to the same wires. The optional shields around the twisted pair help reduce unwanted noise, and are connected to GND at one end.

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Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage, and AC losses in the dielectric. In good polyethylene cables such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low over all loss (Figure 2).

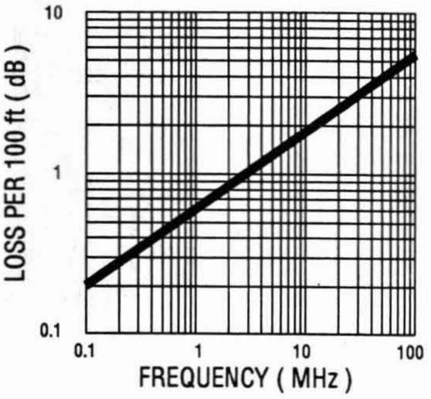

Figure 2. Attenuation - vs - Frequency For Belden 9481

When using low loss cables, Figure 3 can be used as a

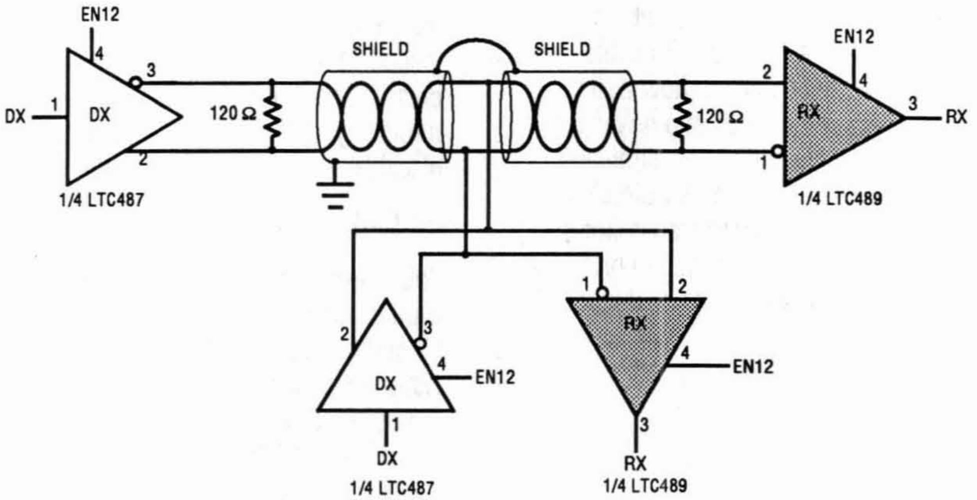

Figure 1. Typical Connection

APPLICATIONS INFORMATION

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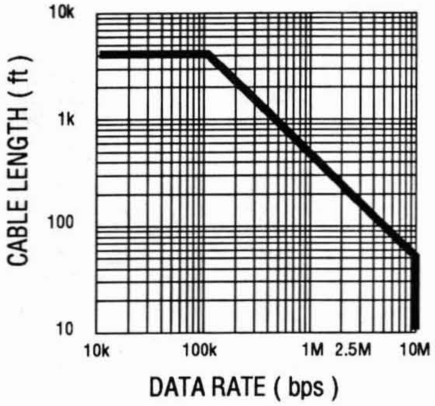

Figure 3. Cable Length - vs - Data Rate

CABLE TERMINATION

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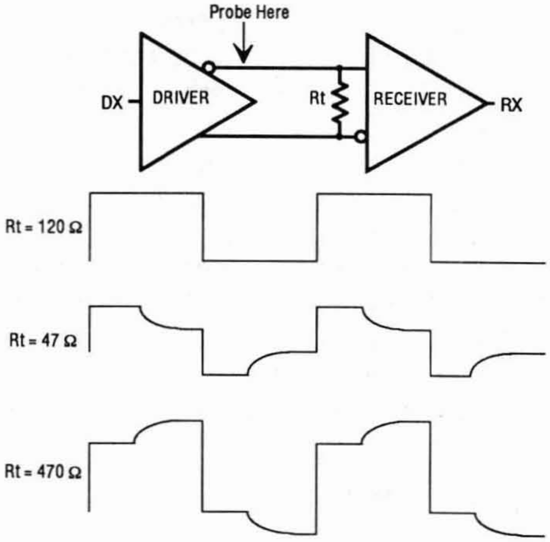

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APPLICATIONS INFORMATION

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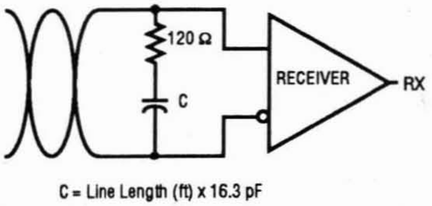

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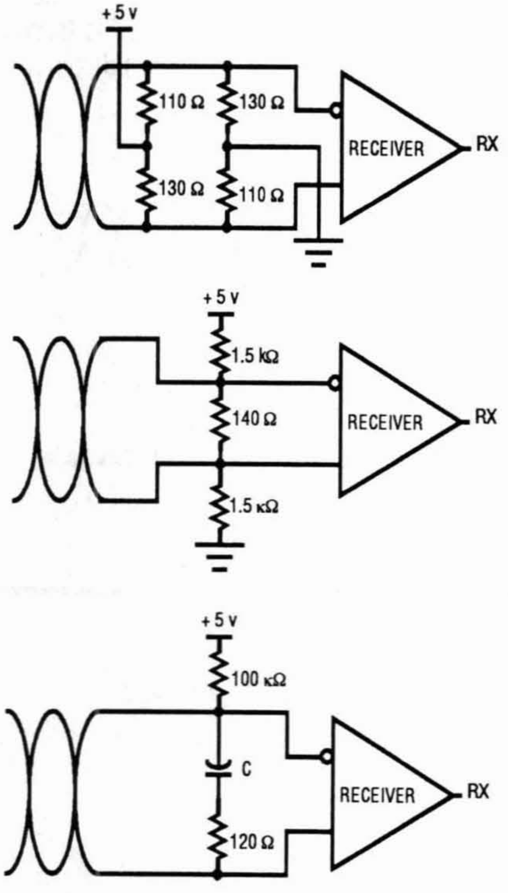

Figure 6. Forcing '0' When All Drivers Are Off

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APPLICATIONS INFORMATION

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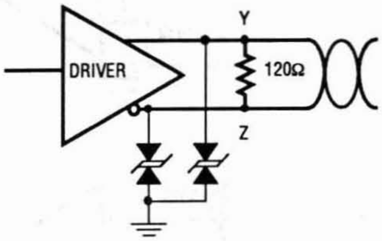

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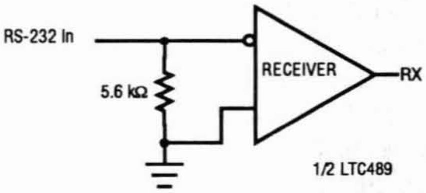
TYPICAL APPLICATIONS

RS-232 Receiver



PRELIMINARY

LTC1063

DC Accurate, Clock Tunable, 5th Order Butterworth Lowpass Filter

May 1992

FEATURES

- Clock Tunable Cutoff Frequency
- 1mV DC Offset (Typical)
- 80 dB CMRR
- Internal or External Clock
- 50µV$_{RMS}$ Clock Feedthrough
- 100:1 Clock to Cutoff Frequency Ratio
- 100µV$_{RMS}$ Total Wideband Noise
- 0.01% THD at 2V$_{RMS}$ Output Level
- 50kHz Maximum Cutoff Frequency
- Cascadable for Faster Rolloff
- Operates from ±2.375V to ±8V Power Supplies
- Self Clocking with 1 RC

APPLICATONS

- Audio
- Strain Gauge Amplifiers
- Anti-aliasing Filters
- Low Level Filtering
- Digital Voltmeters
- 60Hz Lowpass Filters
- Smoothing Filters
- Reconstruction Filters

DESCRIPTION

The LTC1063 is the first monolithic filter providing both clock tunability, low DC output offset and over 12 bit DC accuracy. The frequency response of the LTC1063 closely approximates a 5th order Butterworth polynomial. With appropriate PCB layout techniques the output DC offset is typically 1mV and is constant over a wide range of clock frequencies. With ±5V supplies and ±4V input voltage range, the CMR of the device is 80dB.

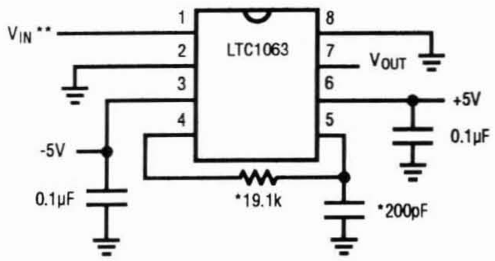
The filter cutoff frequency is controlled either by an internal or external clock. The clock to cutoff frequency ratio is 100:1. The on-board clock is power supply independent, and it is programmed via an external R,C. The 50µV$_{RMS}$ clock feedthrough is considerably reduced over existing monolithic filters.

The LTC1063 wideband noise is 100µV$_{RMS}$, and the device can process large AC input signals with low distortion. With ±7.5V supplies, for instance, the filter handles up to 4V$_{RMS}$ (92 dB S/N ratio) while the standard 1kHz THD is below 0.02%; 80 dB dynamic range (S/N + THD) is obtained with input levels between 1V$_{RMS}$ and 2.3V$_{RMS}$.

The LTC1063 is available in 8 pin minidip and 16 pin SOL.

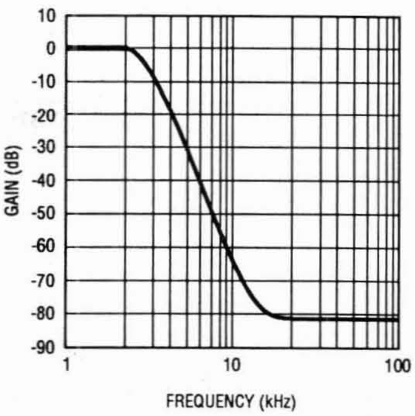
TYPICAL APPLICATIONS

2.5kHz 5th Order Lowpass Filter



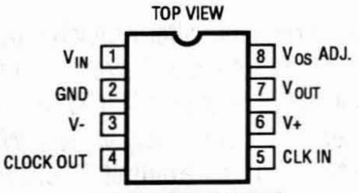
* SELF CLOCKING SCHEME
** IF THE INPUT VOLTAGE CAN EXCEED V+, CONNECT A SIGNAL DIODE BETWEEN PIN 1 AND V+

Frequency Response



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 16V
Power Dissipation 400mW
Storage Temperature Range .... –65°C to 150°C

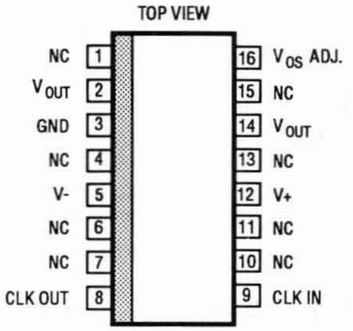

TOP VIEW
V_{IN} 1
GND 2
V- 3
CLOCK OUT 4
8 V_{OS} ADJ.
7 V_{OUT}
6 V+
5 CLK IN

PLASTIC DIP N8 PACKAGE

ORDER PART NUMBER
LTC1063CN8 LTC1063CJ8

PACKAGE/ORDER INFORMATION

Burn-in Voltage 16V
Operating Temperature Range .... -40°C to 85°C
Voltage at Any Input .. [(V-) - 0.3V] -V_{IN} -[(V+) + 0.3V]


TOP VIEW
NC 1
V_{OUT} 2
GND 3
NC 4
V- 5
NC 6
NC 7
CLK OUT 8
16 V_{OS} ADJ.
15 NC
14 V_{OUT}
13 NC
12 V+
11 NC
10 NC
9 CLK IN

S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER
LTC1063CS

ELECTRICAL CHARACTERISTICS

V_S = ±5V, f_{CLK} = 500kHz, f_C = 5kHz, R_{LOAD} = 10k, T_A = 25°C, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Clock to Cutoff Frequency Ratio (f_{CLK}/f_C)	±2.375V ≤ V_S ≤ ±7.5V			100±0.5		
Max Clock Frequency (Note 1)	V_S = ±7.5V			5		MHz
	V_S = ±5.0V			4		MHz
	V_S = ±2.5V			3		MHz
Minimum CLK Frequency (Note 2)	±2.5V ≤ V_S ≤ ±7.5V, T_A < 85°			30		Hz
Input Frequency Fange			0		0.9	f_{CLK}
Filter Gain at f_{IN} = 100	V_S = ± 5V, f_{CLK} = 500kHz, f_C = 5kHz			0		dB
f_{IN} = 1.0kHz = 0.2f_C			- 0.06	- 0.01	0.04	dB
		●	- 0.075	- 0.01	0.055	dB
f_{IN} = 2.5kHz = 0.5f_C			- 0.09	0.16	0.41	dB
		●	- 0.14	0.16	0.46	dB
f_{IN} = 4.0kHz = 0.8f_C			- 0.5	- 0.2	0.1	dB
		●	- 0.6	- 0.2	0.2	dB
f_{IN} = 5.0kHz = f_C			- 3.5	- 3.0	- 2.5	dB
		●	- 3.6	- 3.0	- 2.4	dB
f_{IN} = 20kHz = 4f_C			- 57.5	- 60.0	- 62.0	dB
			- 57.0		- 62.5	dB
Filter Gain at f_{IN} = 1.0kHz	V_S = ± 2.375V, f_{CLK} = 500kHz, f_C = 5kHz		- 0.066	0.004	0.074	dB
		●	- 0.081	0.004	0.089	dB
f_{IN} = 2.5kHz			- 0.24	0.16	0.56	dB
		●	- 0.29	0.16	0.61	dB
f_{IN} = 4.0kHz			- 0.6	- 0.2	0.2	dB
		●	- 0.7	- 0.2	0.3	dB
f_{IN} = 5.0kHz			- 3.5	- 3.0	- 2.5	dB
		●	- 3.6	- 3.0	- 2.4	dB
Filter Gain at f_{IN} = 250Hz	V_S = ±5.0V, f_{CLK} = 25kHz, f_C = 250Hz		- 3.5	- 3.0	- 2.5	dB
		●	- 3.6	- 3.0	- 2.4	dB

ELECTRICAL CHARACTERISTICS

$V_S = \pm 5V$, $f_{CLK} = 500kHz$, $f_C = 5kHz$, $R_{LOAD} = 10k$, $T_A = 25°C$, unless otherwise specified.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Clock Feedthrough	$\pm 2.375V \le V_S \le \pm 7.5V$				50		μV_{RMS}
Wideband Noise (Note 3)	$\pm 2.375V \le V_S \le \pm 7.5V$, $1Hz < f < f_{CLK}$				95		μV_{RMS}
Wideband Noise + THD (Note 4)	$V_S = \pm 7.5V$, $f_C = 20kHz$, $f_{IN} = 1kHz$, $1V_{RMS} \le V_{IN} \le 2.3V_{RMS}$				- 80		dB
Filter Output +/- DC Swing	$V_S = \pm 2.375V$			1.6/-2.0	1.7/-2.2		V
			●	1.4/-1.8			
	$V_S = \pm 5.0V$			4.0/-4.5	4.3/-4.8		V
			●	3.8/-4.3			
	$V_S = \pm 7.5V$			6.5/-7.0	6.8/-7.3		V
			●	6.3/-6.8			
Input Current					10		nA
Dynamic Input Impedance					800		MΩ
Output DC Offset (Note 5)	$V_S = \pm 2.375V$				+ 2	+2±5	mV
	$V_S = \pm 5.0V$				0	±5	mV
	$V_S = \pm 7.5V$				- 4		mV
Output DC Offset Drift	$V_S = \pm 2.375V$				10		µV/°C
	$V_S = \pm 5.0V$				20		µV/°C
	$V_S = \pm 7.5V$				25		µV/°C
Self Clocking Frequency (f_{OSC})	R (pin 4 to 5) = 20k, C (pin 5 to GND) = 470pf						
	$V_S = \pm 2.375V$			99.2	105.2	11.2	kHz
		LTC1063CN,CS,CJ	●	94.9	102.9	111.0	kHz
		LTC1063MJ	●	92.5	100.5	108.5	kHz
	$V_S = \pm 5.0V$			102.0	108.0	114.0	kHz
		LTC1063CN,CS,CJ	●	98.0	106.0	114.0	kHz
		LTC1063MJ	●	97.6	105.6	113.6	kHz
	$V_S = \pm 7.5V$			104.3	110.3	116.3	kHz
		LTC1063CN,CS,CJ	●	101.3	109.3	116.3	kHz
		LTC1063MJ	●	100.4	108.4	116.3	kHz
External CLK Pin Logic Thresholds	$V_S = \pm 2.375V$	Min logical "1"			1.43		V
		Max logical "0"			0.47		V
	$V_S = \pm 5.0V$	Min logical "1"			3		V
		Max logical "0"			1		V
	$V_S = \pm 7.5V$	Min logical "1"			4.5		V
		Max logical "0"			1.5		V
Power Supply Current	$V_S = \pm 2.375V$				2.7	4	mA
		LTC1063CN,CS,CJ	●			5.5	mA
		LTC1063MJ	●			6	mA
	$V_S = \pm 5.0V$				5.5	8	mA
		LTC1063CN,CS,CJ	●			11	mA
		LTC1063MJ	●			12	mA
	$V_S = \pm 7.5V$				7.0		mA
		LTC1063CN,CS,CJ	●			14.5	mA
		LTC1063MJ	●			16	mA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: The maximum clock frequency criterium is arbitrarily defined as: The frequency at which the filter AC response exhibits ≥ 1dB of gain peaking.

Note 2: At limited temperature ranges (i.e. $T_A \le 50°C$) the minimum clock frequency can be as low as 10Hz. The minimum clock frequency is arbitrarily defined to be: The clock frequency at which the output DC offset changes by more than 1 mV.

Note 3: The wideband noise specification does not include the clock feedthrough.

Note 4: To properly evaluate the filter's harmonic distortion an inverting output buffer is recommended, figure 1; output buffering is not necessarily needed when measuring output DC offset or wideband noise.

Note 5: The output DC offset is optimized for ±5V supply. The output DC offset shifts when the power supplies change; however this phenomenon is repeatable and predictable.

TEST CIRCUIT

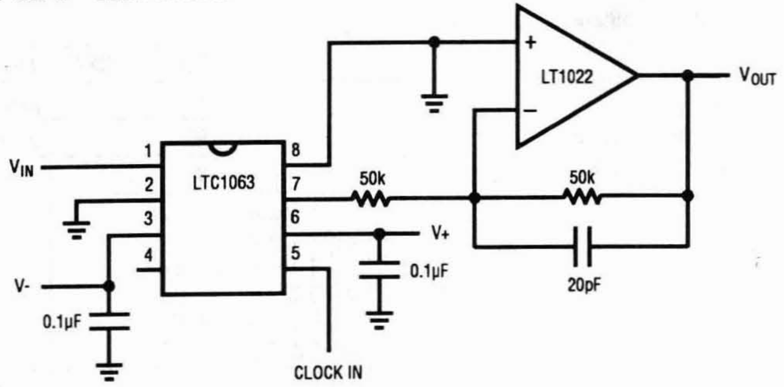
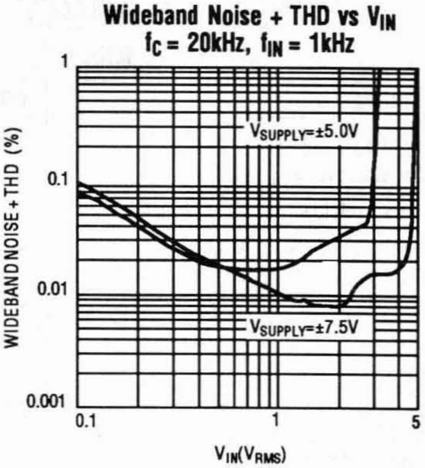
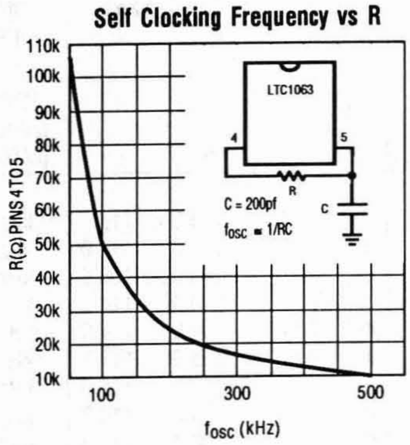
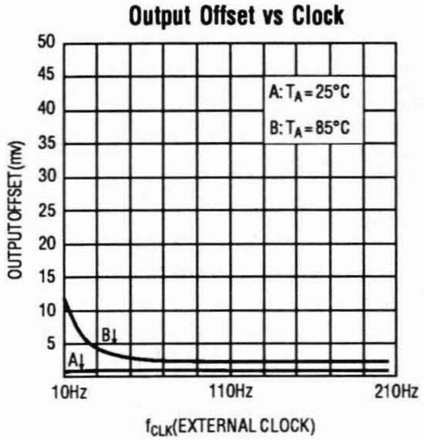
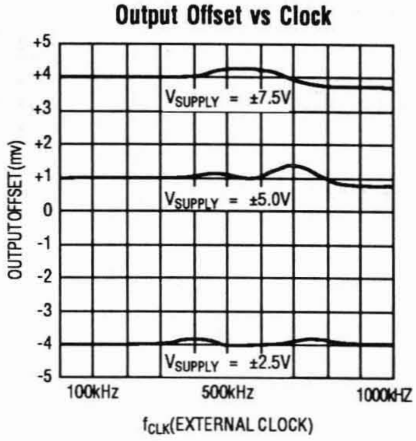

LT1022
+
–
VOUT
VIN
1
2
3
4
8
7
6
5
LTC1063
50k
50k
20pF
V+
0.1µF
V-
0.1µF
CLOCK IN

Figure 1.


Wideband Noise + THD vs V_{IN}
f_C = 20kHz, f_{IN} = 1kHz

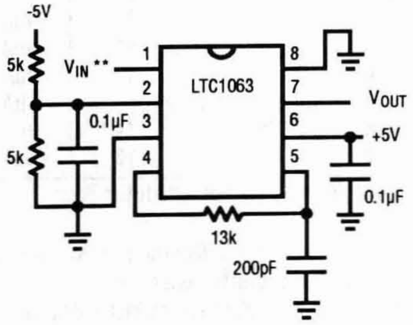

Self Clocking Frequency vs R


Output Offset vs Clock


Output Offset vs Clock

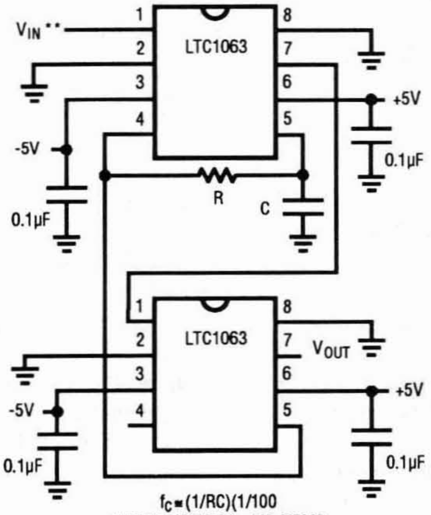
APPLICATIONS

Single 5V Supply Operation
f_C = 3.4kHz


-5V
5k
5k
VIN **
0.1µF
1
2
3
4
8
7
6
5
LTC1063
VOUT
+5V
0.1µF
13k
200pF

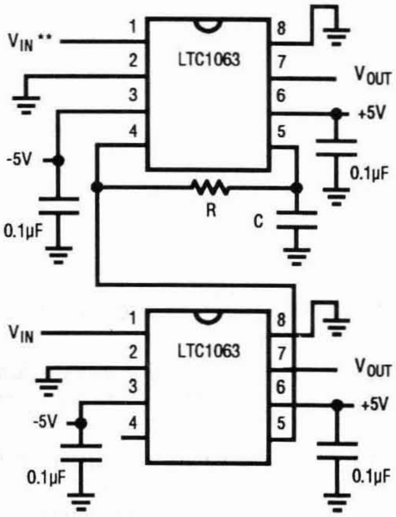
** IF THE INPUT VOLTAGE CAN EXCEED V+, CONNECT A SIGNAL DIODE BETWEEN PIN 1 AND V+

Cascading Two LTC1063s for Steeper Rolloff


VIN **
1
2
3
4
8
7
6
5
LTC1063
+5V
0.1µF
-5V
0.1µF
R
C
1
2
3
4
8
7
6
5
LTC1063
VOUT
+5V
-5V
0.1µF
0.1µF

f_C = (1/RC)(1/100
WIDEBAND NOISE = 140µVRMS
ATTENUATION AT f = $2f_C$ = 60dB

Sharing Clock for Multichannel Applications


VIN **
1
2
3
4
8
7
6
5
LTC1063
VOUT
+5V
0.1µF
-5V
0.1µF
R
C
VIN
1
2
3
4
8
7
6
5
LTC1063
VOUT
+5V
-5V
0.1µF
0.1µF

PRELIMINARY

LTC1064-7/LTC1164-7/LTC1264-7

Linear Phase, Group Delay Equalized, 8th Order Low Pass Filters

September 1991

FEATURES

- Steeper rolloff than Bessel filters
- Low power (LTC1164-7, $fc \leq 20$kHz)
- General purpose (LTC1064-7, $fc \leq 100$kHz)
- High speed (LTC1264-7, $fc \leq 250$kHz)
- Phase and Group Delay response fully tested
- Transient response with 5% overshoot and no ringing
- No external components needed

APPLICATIONS

- Data communication filters
- Time delay networks
- Phase matched filters
- Antialiasing filters
- Smoothing filters for DAC outputs
- Battery operated instrumentation

DESCRIPTION

The LTC1064-7, LTC1164-7, LTC1264-7, are clock tunable monolithic 8th order lowpass filters with linear passband phase and flat group delay. Their amplitude response approximates maximally flat passband and exhibits steeper rolloff than an equivalent 8th order Bessel filter. The cutoff frequency of the filters is tuned with an external TTL or CMOS clock.

The LTC1164-7 features low power, wide dynamic range and a maximum cutoff frequency of 20kHz. With 1V_{RMS} input and an appropriate PCB layout, 76dB (S/N ratio + THD) can be obtained.

The LTC1064-7 features similar dynamic range and a maximum cutoff frequency of 100kHz. The clock to cutoff frequency ratio for both the LTC1064-7 and LTC1164-7 is either 50:1 (pin 10 to V+) or 100:1 (pin 10 to V-).

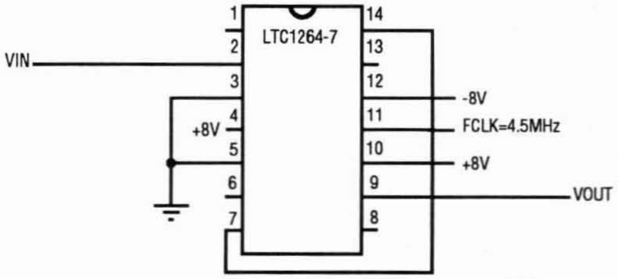
The LTC1264-7 is optimized for speed. Depending on the operating conditions, cutoff frequencies between 200kHz and 250kHz can be obtained. The clock to cutoff frequency ratio of the LTC1264-7 is either 25:1 or 50:1.

All 3 filters are pin compatible with the LTC1064-X series.

See page 13-84 for more complete information on the LTC1264-7.

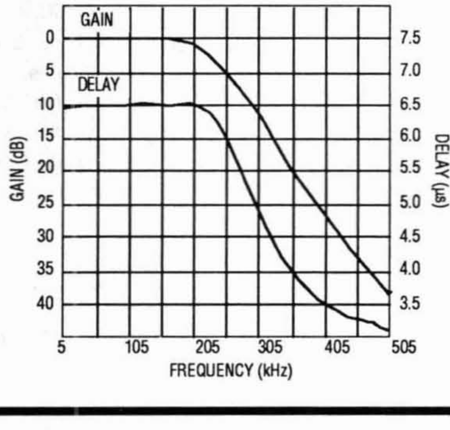
TYPICAL APPLICATION

200kHz Linear Phase Low pass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE FCLK LINE.

Frequency Response



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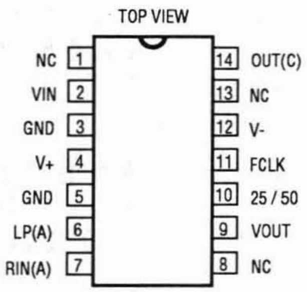
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-)	16V
Power Dissipation	400mW
Storage Temperature Range	–65°C to 150°C
Burn-in Voltage	16V
Operating Temperature Range	-40°C to 85°C
Voltage at Any Input	[(V-) - 0.3V] ≤ V_{IN} ≤ [(V+) + 0.3V]

PACKAGE/ORDER INFORMATION

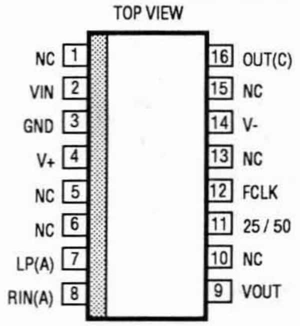

TOP VIEW
NC 1
VIN 2
GND 3
V+ 4
GND 5
LP(A) 6
RIN(A) 7
14 OUT(C)
13 NC
12 V-
11 FCLK
10 25 / 50
9 VOUT
8 NC

N PACKAGE
14 LEAD PLASTIC DIP

ORDER PART NUMBER

LTC1264-7CN

See page 13-84 for more complete information on the LTC1264-7.

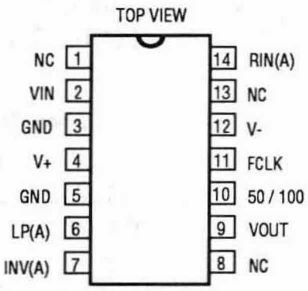

TOP VIEW
NC 1
VIN 2
GND 3
V+ 4
NC 5
NC 6
LP(A) 7
RIN(A) 8
16 OUT(C)
15 NC
14 V-
13 NC
12 FCLK
11 25 / 50
10 NC
9 VOUT

S PACKAGE
16-LEAD PLASTIC SOL

ORDER PART NUMBER

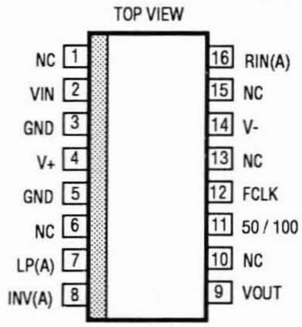
LTC1264-7CS

See page 13-84 for more complete information on the LTC1264-7.


TOP VIEW
NC 1
VIN 2
GND 3
V+ 4
GND 5
LP(A) 6
INV(A) 7
14 RIN(A)
13 NC
12 V-
11 FCLK
10 50 / 100
9 VOUT
8 NC

N PACKAGE
14 LEAD PLASTIC DIP

LTC1164-7CN
LTC1064-7CN


TOP VIEW
NC 1
VIN 2
GND 3
V+ 4
GND 5
NC 6
LP(A) 7
INV(A) 8
16 RIN(A)
15 NC
14 V-
13 NC
12 FCLK
11 50 / 100
10 NC
9 VOUT

S PACKAGE
16-LEAD PLASTIC SOL

LTC1164-7CS
LTC1064-7CS

ELECTRICAL CHARACTERISTICS

V_S=±7.5Volts, R_{LOAD}=10k, T_A=25°C, *f*clk=1MHz(LTC1064-7), 400kHz(LTC1164-7), 2.5MHz(LTC1264-7), TTL or CMOS Level and all Gain measurements are referenced to passband Gain unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Passband Gain (0.1Hz - 0.25*f*cutoff)	LTC1064-7	*f*test=5kHz (50:1)		-0.10		dB
	LTC1164-7	*f*test=2kHz (50:1)		-0.10		dB
	LTC1264-7	*f*test=25kHz (25:1)		-0.10		dB
Gain at 0.5*f*cutoff	LTC1064-7	*f*test=10kHz (50:1)		-0.10		dB
		*f*test=5kHz (100:1)		-0.10		dB
	LTC1164-7	*f*test=4kHz (50:1)		-0.10		dB
		*f*test=2kHz (100:1)		-0.10		dB
	LTC1264-7	*f*test=50kHz(25:1)		-0.30		dB
		*f*test=25kHz (50:1)		-0.15		dB
Gain at 0.75*f*cutoff	LTC1064-7	*f*test=15kHz (50:1)		-0.65		dB
	LTC1164-7	*f*test=6kHz (50:1)		-0.65		dB
	LTC1264-7	*f*test=75kHz (50:1)		-1.00		dB

ELECTRICAL CHARACTERISTICS

V_S=±7.5Volts, R_{LOAD}=10k, T_A=25°C, *f*clk=1MHz(LTC1064-7), 400kHz(LTC1164-7), 2.5MHz(LTC1264-7), TTL or CMOS Level and all Gain measurements are referenced to passband Gain unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Gain at *f*cutoff	LTC1064-7	*f*test=20kHz (50:1)		-3.00		dB
		*f*test=10kHz (100:1)		-3.00		dB
	LTC1164-7	*f*test=8kHz (50:1)		-3.00		dB
		*f*test=4kHz (100:1)		-3.00		dB
	LTC1264-7	*f*test=100kHz(25:1)		-3.00		dB
		*f*test=50kHz (50:1)		-3.00		dB
Gain at 2.0*f*cutoff	LTC1064-7	*f*test=40kHz (50:1)		-34		dB
		*f*test=20kHz (100:1)		-34		dB
	LTC1164-7	*f*test=16kHz (50:1)		-34		dB
		*f*test=8kHz (100:1)		-34		dB
	LTC1264-7	*f*test=200kHz(25:1)		-28		dB
		*f*test=100kHz(50:1)		-30		dB
Gain with fclk=20kHz	LTC1064-7	*f*test=200Hz (100:1)		-3.00		dB
	LTC1164-7	*f*test=200Hz (100:1)		-3.00		dB
	LTC1264-7	*f*test=200Hz (50:1)		-0.30		dB
Gain with V_S=±2.375V, fclk=400kHz	LTC1064-7	*f*test=4kHz (50:1)		-0.10		dB
		*f*test=8kHz (50:1)		-3.00		dB
	LTC1164-7	*f*test=4kHz (50:1)		-0.10		dB
		*f*test=8kHz (50:1)		-3.00		dB
	LTC1264-7	*f*test=8kHz (25:1)		0.15		dB
		*f*test=16kHz (25:1)		-2.70		dB
Gain with fclk=4MHz	LTC1264-7	*f*test=160kHz(25:1) Vin=1V_{RMS}		-1.00		dB
Phase Factor (Φ) (Note 1)		Phase = 180° - Φ (*f* / *f*c) (0.1Hz ≤ *f* ≤ *f*cutoff)				
	LTC1064-7	50:1		432		deg
		100:1		418		deg
	LTC1164-7	50:1		432		deg
		100:1		418		deg
	LTC1264-7	25:1		407		deg
		50:1		390		deg
Phase Deviation from Linear Phase (Note 1)	LTC1064-7	50:1		±0.7		%
		100:1		±1.0		%
	LTC1164-7	50:1		±0.7		%
		100:1		±1.0		%
	LTC1264-7	25:1		±0.7		%
		50:1		±0.5		%
Group Delay (TD) (Note 2)		TD = (1 / 360) (Φ / *f*c)				
	LTC1064-7	*f*c=20kHz (50:1)		60		µs
		*f*c=10kHz (100:1)		116		µs
	LTC1164-7	*f*c=8kHz (50:1)		150		µs
		*f*c=4kHz (100:1)		290.3		µs
	LTC1264-7	*f*c=100kHz (25:1)		11.3		µs
		*f*c=50kHz (50:1)		21.6		µs
Group Delay Deviation (Note 2)	LTC1064-7	50:1		±0.7		%
		100:1		±1.0		%
	LTC1164-7	50:1		±0.7		%
		100:1		±1.0		%
	LTC1264-7	25:1		±0.7		%
		50:1		±0.5		%

ELECTRICAL CHARACTERISTICS

V_S=±7.5Volts, R_{LOAD}=10k, T_A=25°C, *f*clk=1MHz(LTC1064-7), 400kHz(LTC1164-7), 2.5MHz(LTC1264-7), TTL or CMOS Level and all Gain measurements are referenced to passband Gain unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Frequency Range LTC1064-7 / LTC1164-7	50:1	0		<*f*clk	MHz
	100:1	0		<*f*clk/2	MHz
LTC1264-7	25:1	0		<*f*clk	MHz
	50:1	0		<*f*clk/2	MHz
Maximum *f*clk LTC1064-7 / LTC1264-7	V_S=≥7.0V		5		MHz
	V_S=±5.0V		4		MHz
	V_S=±2.5V		2		MHz
LTC1164-7	V_S=≥7.0V		1.5		MHz
	V_S=±5.0V		1.0		MHz
	V_S=±2.5V		0.5		MHz
Clock Feedthrough ($f \geq f$clk)	V_S=±7.5V, Input at GND				
LTC1064-7 / LTC1164-7	50:1		200		μV_{RMS}
LTC1264-7	25:1		200		μV_{RMS}
	50:1		700		μV_{RMS}
Wideband Noise (1Hz ≤ $f \leq f$clk)	V_S=±7.5V, Input at GND				
LTC1064-7 / LTC1164-7	50:1		110		μV_{RMS}
LTC1264-7	25:1		190		μV_{RMS}
Input Impedance LTC1064-7 / LTC1164-7			50		kΩ
LTC1264-7			56		kΩ
Output DC Voltage Swing LTC1064-7	Vs=±5.0V		±3.4		Volts
	Vs=±7.5V		±5.6		Volts
LTC1164-7	Vs=±5.0V		±4.0		Volts
	Vs=±7.5V		±6.1		Volts
LTC1264-7	Vs=±5.0V		±2.4		Volts
	Vs=±7.5V		±4.0		Volts
Power Supply Current					
LTC1064-7 / LTC1264-7	V_S=±2.375V		11		mA
	V_S=±5.0V		14		mA
	V_S=±7.5V		17		mA
LTC1164-7	V_S=±2.375V		3		mA
	V_S=±5.0V		5		mA
	V_S=±7.5V		7		mA
Power Supply Range		4.75		16	V

Note 1: Input frequencies, *f*, are linearly phase shifted through the filter as long as $f \leq fc$; fc = cutoff frequency.

Figure 1 curve (A) shows the typical phase response of an LTC1264-7 operating at *f*clk = 2.5MHz, fc = 100kHz. An endpoint straight line, curve (B), depicts the ideal linear phase response of the filter. It is described by:

$$\text{phase shift} = 180° - \Phi\,(f/fc)\;;\; f \leq fc \qquad (1)$$

Φ is arbitrarily called the "phase factor" expressed in degrees. The phase factor together with the specified deviation from the ideal straight line allows the calculation of the phase at a given frequency . Note, the maximum phase non linearity, figure 1, occurs at the vicinity of $f = 0.25\,fc$, and $= 0.75\,fc$.

Example: The phase shift at 70kHz of the LTC1264-7 shown in figure 1 is:

$$\text{phase shift} = 180° - 407°\,(70\text{kHz}/100\text{kHz}) \pm \text{non linearity}$$
$$= -104.9° \pm 0.7\% \text{ or } -104.9° \pm .73°$$

Note 2: Group Delay and Group Delay Deviation are calculated from the measured Phase Factor and Phase Deviation specifications.

PHASE RESPONSE IN THE PASSBAND
LTC1264-7, FCLK=2.5MHz, RATIO=25:1

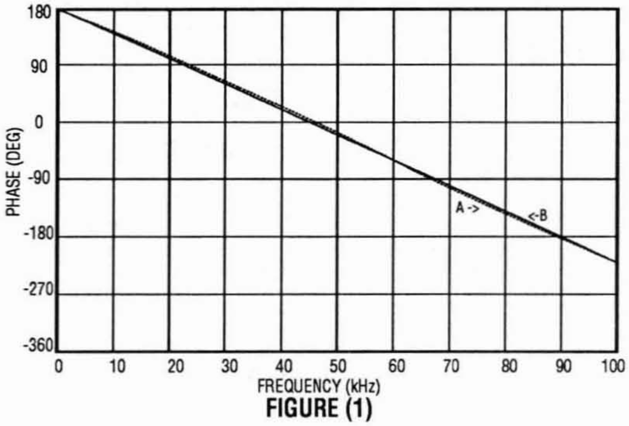


FIGURE (1)

PRELIMINARY

LT1082

1A High Voltage High Efficiency Switching Voltage Regulator

January 1992

FEATURES

- Wide Input Voltage Range 3V - 75V
- High Switch Voltage 100V
- Low Quiescent Current 4.5mA
- Internal 1A Switch
- Shutdown Mode Draws Only 130μA Supply Current
- Isolated Flyback-Regulated Mode for Fully Floating Outputs
- Can Be Externally Synchronized
- Frequency Shifts in Current Limit
- Available in MiniDip, TO-220 and TO-3 Packages
- Same Pinout as LT1072

APPLICATIONS

- Telecom 5V Supply @ 0.8A from -48V (-10V -70V)
- 90V Supply @ 120mA from 15V
- All Applications using LT1072 (See Below for Specification Differences)

LT1082 and LT1072 Major Specification Differences

	LT1082C	**LT1072HV**
V_{IN}	3V - 75V	3V - 60V
V_{SWITCH}	100V	75V
Switch Current Limit	1A	1.25A
Quiescent Current	4.5mA	6mA
Operating Frequency	60kHz	40kHz
Flyback Reference Voltage	$16.2+0.6(35k\Omega/R_{FB})$ (See Figure 2.)	

DESCRIPTION

The LT1082 is a monolithic high power, high voltage switching regulator. It can be operated in all standard switching configurations including buck, boost, flyback, forward and inverting. A high current, high efficiency switch is included on the die along with all oscillator, control and protection circuitry.

The LT1082 operates with supply voltages from 3V to 75V, switch voltage up to 100V and draws only 4.5mA quiescent current. It can deliver load power up to 20 watts with no external power devices. By utilizing current-mode switching techniques, it provides excellent AC and DC load and line regulation.

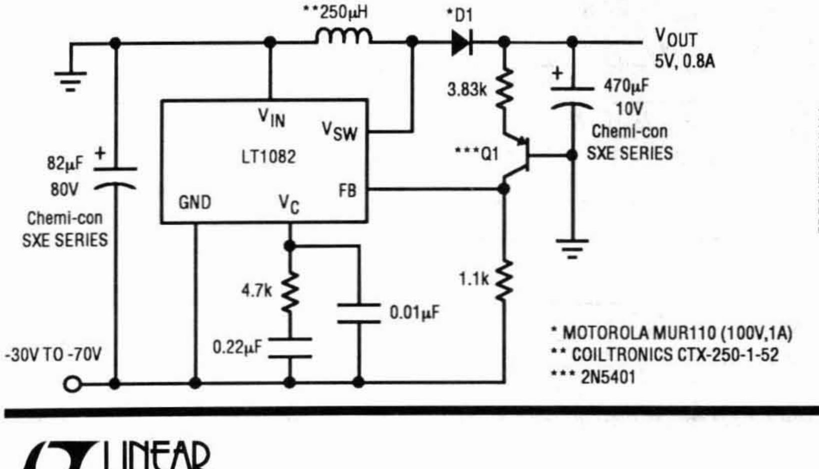
An externally activated shutdown mode reduces total supply current to 130μA typical for standby operation. Totally isolated and regulated outputs can be generated by using the optional "isolated flyback regulation mode" built into the LT1082, without the need for optocouplers or extra transformer windings.

The LT1082 has a unique feature to provide high voltage short circuit protection. When the FB pin is pulled down to 0.6V and the current out of the pin reaches approximately 350μA, the switching frequency will shift down from 60kHz to 14kHz. (See Figure 1.)

The LT1082 is nearly identical to the lower voltage LT1072. For the major differences in specifications, see the table on the left.

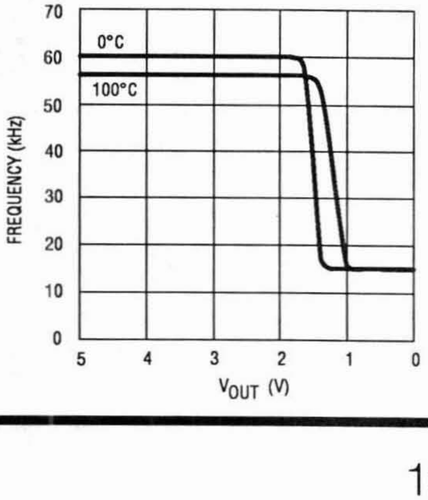
TYPICAL APPLICATION

Telecom 5V Power Supply



* MOTOROLA MUR110 (100V,1A)
** COILTRONICS CTX-250-1-52
*** 2N5401

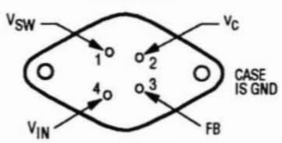
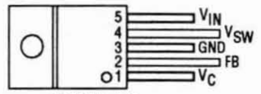
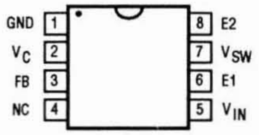
Short-Circuit Frequency Shiftdown



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 75V
Switch Output Voltage 100V
Feedback Pin Voltage (Transient, 1ms) .... ±15V
Operating Junction Temperature Range
LT1082M .... -55°C to 150°C
LT1082I .... -40°C to 125°C
LT1082C .... 0°C to 100°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
BOTTOM VIEW  V_{SW} V_C 1 2 4 3 CASE IS GND V_{IN} FB 4 LEAD TO-3	LT1082MK
FRONT VIEW  5 4 3 2 1 V_{IN} V_{SW} GND FB V_C 5 LEAD TO-220	LT1082CT LT1082IT
TOP VIEW  GND 1 V_C 2 FB 3 NC 4 8 E2 7 V_{SW} 6 E1 5 V_{IN} HERMETIC J8 PACKAGE PLASTIC DIP N8 PACKAGE	LT1082MJ8 LT1082CN8 LT1082IN8

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C= 0.5V, V_{FB} = V_{REF}, output pin is open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
		V_C = 0.8V	●	1.214	1.244	1.274	V
I_B	Feedback Input Current	V_{FB} = V_{REF}			350	750	nA
			●			1100	nA
gm	Error Amplifier Transconductance	$\Delta I_C = \pm 25\mu A$		3000	4400	6000	μmho
			●	2400		7000	μmho
	Error Amplifier Source or Sink Current	V_C = 1.5V		150	200	350	μA
			●	120		400	μA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V		1.8		2.3	V
		Lo Clamp, V_{FB} = 1.5V		0.17	0.22	0.30	V
	Reference Voltage Line Regulation	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.8V	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	$0.9V \le V_C \le 1.4V$		400	700		V/V
	Minimum Input Voltage		●		2.6	3.0	V
I_Q	Supply Current	$3V \le V_{IN} \le V_{MAX}$, V_C = 0.6V			4.5	6.5	mA
	Control Pin Threshold	Duty Cycle = 0		0.8	0.9	1.08	V
			●	0.6		1.25	V
	Normal/Flyback Threshold on Feedback Pin			0.53	0.6	0.72	V
f	Switching Frequency			50	60	70	kHz
			●	45		75	kHz
	Switching Frequency	$800\mu A \ge I_{FB} \ge 450\mu A$			14		kHz
BV	Output Switch Breakdown Voltage	$3V \le V_{IN} \le V_{MAX}$, I_{SW} = 1mA	●	100	115		V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = 15V, V_C= 0.5V, V_{FB} = V_{REF}, output pin is open.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Control Voltage to Switch Current Transconductance				1.5		A/V
V_{FB}	Flyback Reference Voltage	I_{FB} = 60µA		17.5	19	20.5	V
			●	16.5		21.5	V
	Change in Flyback Reference Voltage	60µA ≤ I_{FB} ≤ 200µA		3.5	4.6	6.0	V
	Flyback Reference Voltage Line Regulation	I_{FB} = 60µA, 3V ≤ V_{IN} ≤ V_{MAX}			0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	ΔI_C = ±10µA		150	300	500	µmho
	Flyback Amplifier Source	V_C = 0.6V Source	●	15	32	70	µA
	and Sink Current	I_{FB} = 60µA Sink	●	30	50	90	µA
V_{SAT}	Output Switch "ON" Resistance (Note 1)	I_{SW} = 1A (LT1082C), I_{SW} = 0.8A (LT1082M)	●		0.8	1.2	Ω
I_{LIM}	Switch Current Limit	Duty Cycle ≤ 50% T_j ≥ 25°C	●	1		2.4	A
	(LT1082C)	Duty Cycle ≤ 50% T_j < 25°C	●	1.1		2.6	A
		Duty Cycle = 80% (Note 2)	●	0.8		2.4	A
	Switch Current Limit	Duty Cycle ≤ 50% T_j ≥ 25°C	●	0.9		2.4	A
	(LT1082I)	Duty Cycle ≤ 50% T_j < 25°C	●	1.1		2.8	A
		Duty Cycle = 80% (Note 2)	●	0.7		2.6	A
	Switch Current Limit	Duty Cycle ≤ 50% T_j ≥ 25°C	●	0.8		2.4	A
	(LT1082M)	Duty Cycle ≤ 50% T_j < 25°C	●	1.1		3.0	A
		Duty Cycle = 80% (Note 2)	●	0.65		2.8	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				30	40	mA/A
DC(max)	Maximum Switch Duty Cycle			85	92	97	%
	Flyback Sense Delay Time				1.5		µs
	Shutdown Mode Supply Current	3V ≤ V_{IN} ≤ V_{MAX}, V_C = 0.05V			130	270	µA
	Shutdown Mode	3V ≤ V_{IN} ≤ V_{MAX}		100	150	250	mV
	Threshold Voltage		●	50		300	mV

The ● denotes specifications which apply over the operating temperature range.

Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V.

Note 2: For duty cycles (DC) from 50% and 80%, minimum guaranteed switch current decreases linearly.

TYPICAL PERFORMANCE CHARACTERISTICS

Short-Circuit Frequency Shiftdown

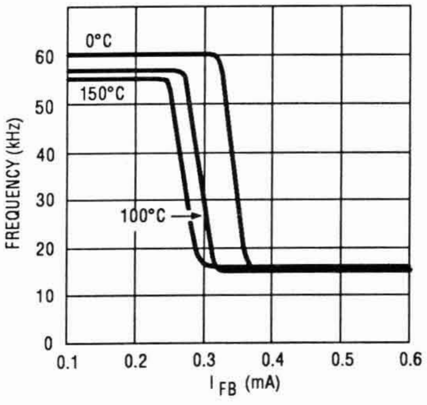


Figure 1.

Isolated Flyback Reference Voltage

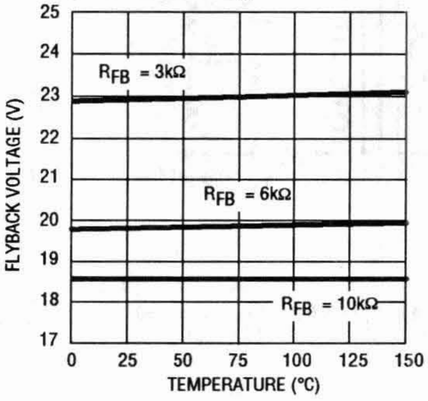


Figure 2.

Normal/Flyback Mode Threshold on Feedback Pin

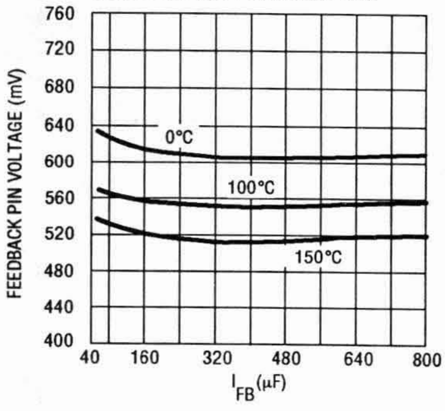
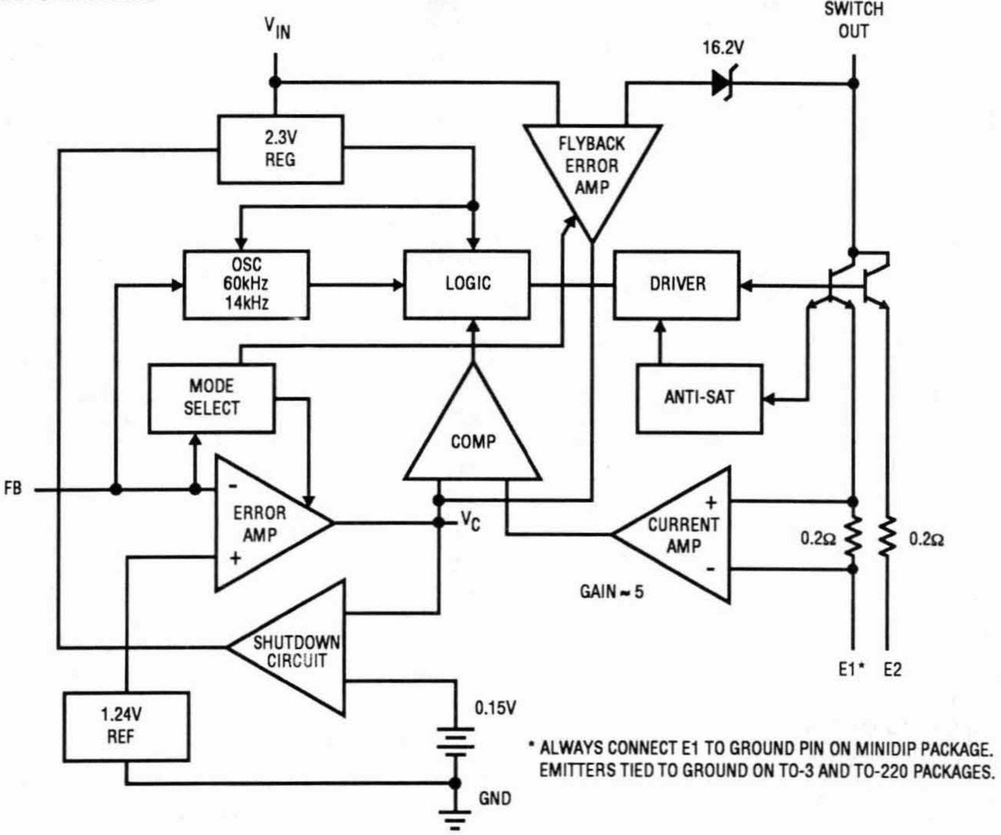


Figure 3.

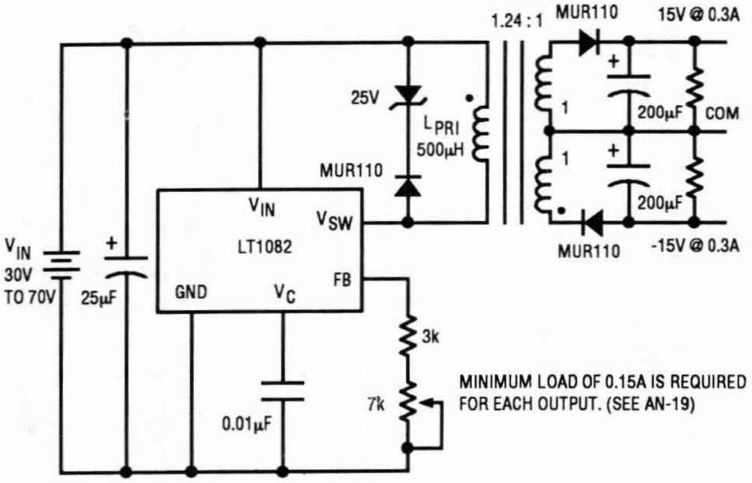
BLOCK DIAGRAM


VIN
SWITCH OUT
16.2V
2.3V REG
FLYBACK ERROR AMP
OSC 60kHz 14kHz
LOGIC
DRIVER
MODE SELECT
ANTI-SAT
COMP
FB
ERROR AMP
VC
CURRENT AMP
GAIN ≈ 5
0.2Ω
0.2Ω
SHUTDOWN CIRCUIT
E1*
E2
1.24V REF
0.15V
GND

* ALWAYS CONNECT E1 TO GROUND PIN ON MINIDIP PACKAGE. EMITTERS TIED TO GROUND ON TO-3 AND TO-220 PACKAGES.

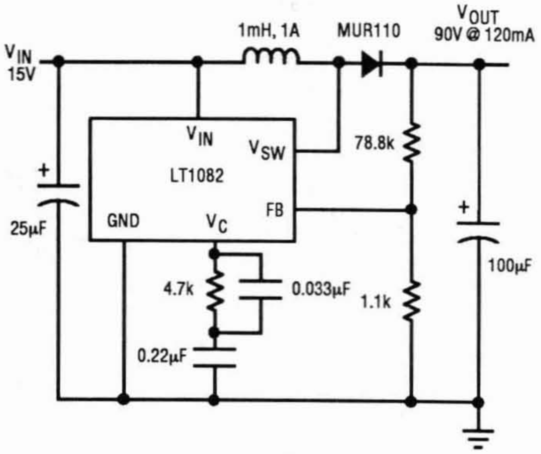
TYPICAL APPLICATIONS

Totally Isolated Converter


1.24 : 1
MUR110
15V @ 0.3A
25V
LPRI 500µH
1
200µF
COM
1
200µF
MUR110
MUR110
-15V @ 0.3A
VIN
VSW
LT1082
GND
VC
FB
VIN 30V TO 70V
25µF
0.01µF
3k
7k

MINIMUM LOAD OF 0.15A IS REQUIRED FOR EACH OUTPUT. (SEE AN-19)

Boost Converter


VOUT 90V @ 120mA
1mH, 1A
MUR110
VIN 15V
VIN
VSW
LT1082
78.8k
25µF
GND
VC
FB
100µF
4.7k
0.033µF
1.1k
0.22µF

LINEAR TECHNOLOGY

PRELIMINARY

LTC1096/LTC1098

Micropower, Sampling 8-bit Serial I/O A/D Converters

September 1991

FEATURES

- 80μA Supply Current
- 3μA Supply Current in Shutdown
- 8 Pin SOIC Plastic Package
- Single Supply 3V to 9V Operation
- Sample and Hold
- 16μS Conversion Time
- 33KHz Sampling Rate
- ±1/2LSB Total Unadjusted Error Over Temp
- Direct 3 Wire Interface to Most MPU Serial Ports and All MPU Parallel I/O Ports
- Analog Inputs Common-Mode to Supply Rails

APPLICATIONS

- Battery Operated Systems
- Remote Data Acquisition
- Battery Monitoring
- Battery Gas Gauges
- Temperature Measurement
- Isolated Data Acquisition

DESCRIPTION

The LTC1096/8 are micropower, 8-bit A/D converters which draw only 80μA of supply current when converting. They automatically power down to 3μA of supply current whenever they are not performing conversions. They are packaged in 8 pin SO packages and operate on 3V to 9V supplies. These 8-bit, switched capacitor, successive approximation ADCs include sample and holds. The 1096 has a single differential analog input. The 1098 offers a software selectable 2 channel mux.

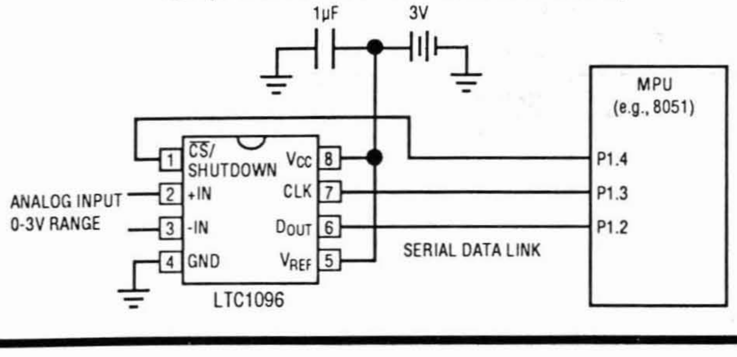
On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over 3 wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (below 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

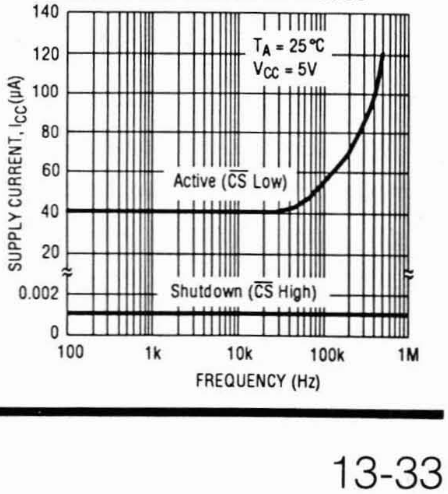
All grades are specified with offset and linearity errors of ±0.5LSB maximum over temperature. The A grade devices are specified with total unadjusted error of ±0.5LSB maximum over temperature.

TYPICAL APPLICATION

10μW, SO-8 Package, 8-Bit ADC Samples at 200Hz and Runs off a 3V Battery



Supply Current vs Clock Rate for Active and Shutdown Modes



ABSOLUTE MAXIMUM RATINGS

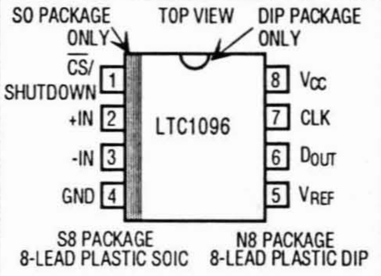
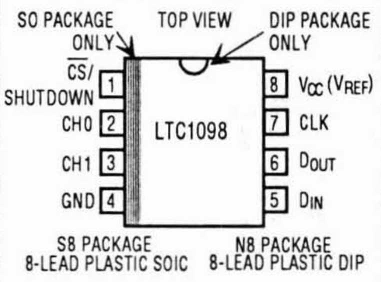
(Notes 1 and 2)

Supply Voltage (V_{CC}) (Transient 10ms) 12V
Supply Voltage (V_{CC}) 10V
Voltage
  Analog Reference .... -0.3V to V_{CC}+0.3V
  Digital Inputs .... -0.3V to 10V
  Digital Output .... -0.3V to V_{CC}+0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1096/8AC, LTC1096/8C .... 0°C to 70°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 SO PACKAGE ONLY TOP VIEW DIP PACKAGE ONLY CS/ SHUTDOWN 1 +IN 2 -IN 3 GND 4 LTC1096 8 VCC 7 CLK 6 DOUT 5 VREF S8 PACKAGE 8-LEAD PLASTIC SOIC N8 PACKAGE 8-LEAD PLASTIC DIP	LTC1096ACN8 LTC1096CN8 LTC1096ACS8 LTC1096CS8
 SO PACKAGE ONLY TOP VIEW DIP PACKAGE ONLY CS/ SHUTDOWN 1 CH0 2 CH1 3 GND 4 LTC1098 8 VCC (VREF) 7 CLK 6 DOUT 5 DIN S8 PACKAGE 8-LEAD PLASTIC SOIC N8 PACKAGE 8-LEAD PLASTIC DIP	LTC1098ACN8 LTC1098CN8 LTC1098ACS8 LTC1098CS8

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{CC}	Supply Voltage		3	10	V
f_{CLK}	Clock Frequency	V_{CC} = 5V	0.025	0.5	MHz
t_{CYC}	Total Cycle Time	LTC1096, f_{CLK} = 500KHz LTC1098, f_{CLK} = 500KHz	29 29		µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 5V	150		ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Figures 1 and 2)	V_{CC} = 5V, LTC1096	1		µs
		V_{CC} = 5V, LTC1098	1		µs
t_{wakeup}	Wakeup Time $\overline{CS}$↓ Before First CLK↓ After First CLK↑ (See Fig. 1)	V_{CC} = 5V, LTC1096	10		µs
	Wakeup Time $\overline{CS}$↓ Before MSBF Bit CLK↓ (See Fig. 2)	V_{CC} = 5V, LTC1098	10		µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 5V	400		ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V	0.8		µs
t_{WLCLK}	CLK Low Time	V_{CC} = 5V	1		µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V	1		µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1096, f_{CLK} = 500KHz LTC1098, f_{CLK} = 500KHz	28 28		µs µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		LTC1096/8A			LTC1096/8			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Offset Error		●			±0.5			±0.5	LSB
Linearity Error	(Note 4)	●			±0.5			±0.5	LSB
Full Scale Error		●			±0.5			±1	LSB
Total Unadjusted Error	V_{REF} = 5.000V (Note 5)	●			±0.5			±1	LSB
Analog and REF Input Range			-0.05V to V_{CC}+0.05V						V
On Channel Leakage Current (Note 6)		●			±1			±1	μA
Off Channel Leakage Current (Note 6)		●			±1			±1	μA

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	μA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			-2.5	μA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10μA I_O = 360μA	● ●	4.5 2.4	4.74 4.72		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ High	●			±3	μA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			-25		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			45		mA
I_{CC}	Supply Current	$\overline{CS}$ = High t_{CYC} ≥ 200μs, f_{CLK} ≤ 50KHz t_{CYC} = 29μs, f_{CLK} = 500KHz	● ● ●		0.001 40 120	3 80 180	μA μA μA
I_{REF}	Reference Current	$\overline{CS}$ = High t_{CYC} ≥ 200μs, f_{CLK} ≤ 50KHz t_{CYC} = 29μs, f_{CLK} = 500KHz	● ● ●		0.001 3.5 35	2.5 7.5 50	μA μA μA
t_{SMPL}	Analog Input Sample Time	See Figures 1 and 2			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Figures 1 and 2			8		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	C_{LOAD} = 100pF	●		50	150	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z		●		170	450	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	C_{LOAD} = 100pF	●		60	150	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			30		ns
t_f	D_{OUT} Fall Time	C_{LOAD} = 100pF	●		70	250	ns
t_r	D_{OUT} Rise Time	C_{LOAD} = 100pF	●		25	100	ns
C_{IN}	Input Capacitance	Analog Inputs On Channel Off Channel Digital Input			30 5 5		pF pF pF

Note 3: V_{CC} = 5V, V_{REF} = 5V and CLK = 0.5MHz unless otherwise specified. The ● denotes specifications which apply over the operating temperature range.

Note 4: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 5: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

Note 6: Channel leakage current is measured after the channel selection.

APPLICATIONS INFORMATION

Figure 1. LTC1096 Operating Sequence

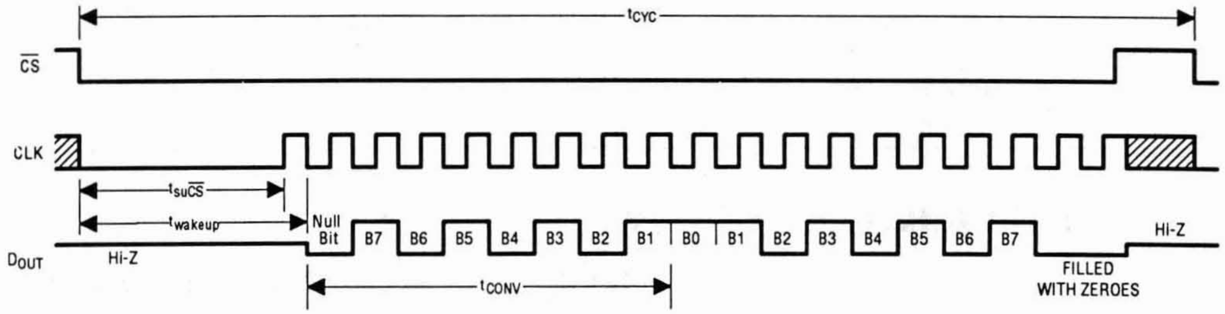
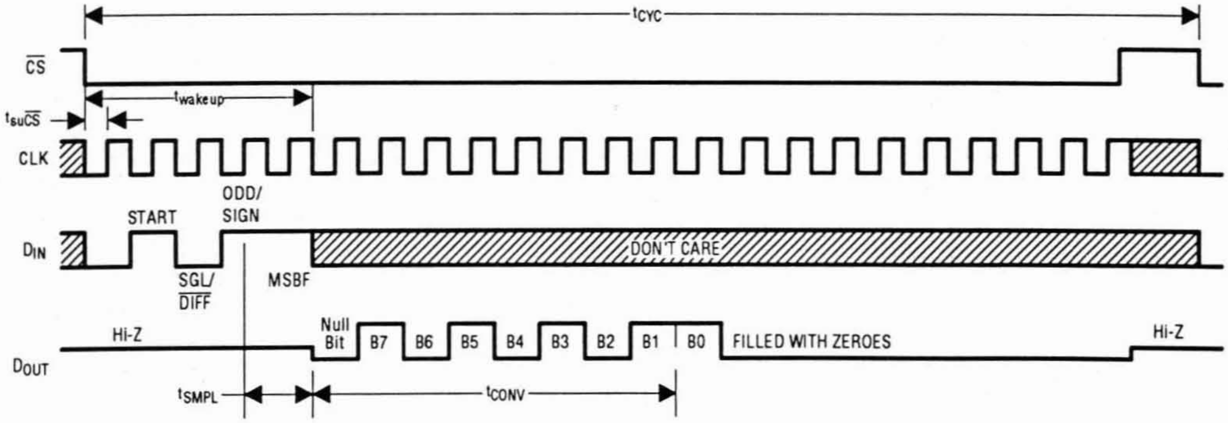
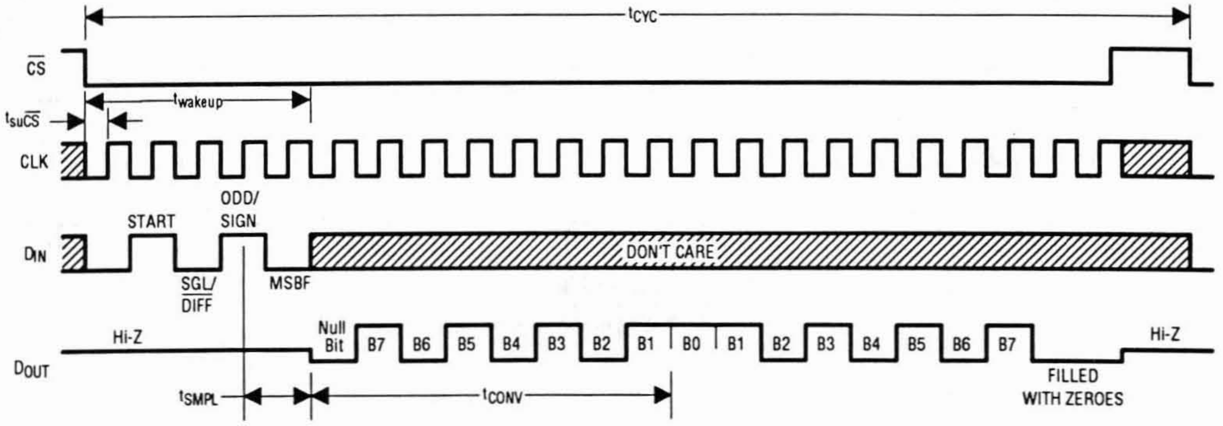

t_{CYC}
$\overline{CS}$
CLK
$t_{su\overline{CS}}$
t_{wakeup}
Null Bit
B7
B6
B5
B4
B3
B2
B1
B0
B1
B2
B3
B4
B5
B6
B7
Hi-Z
D_{OUT}
Hi-Z
t_{CONV}
FILLED WITH ZEROES

Figure 2. LTC1098 Operating Sequence
Example: Differential Inputs (CH+, CH-)

MSB First Data (MSBF=1)


t_{CYC}
$\overline{CS}$
t_{wakeup}
$t_{su\overline{CS}}$
CLK
ODD/ SIGN
START
D_{IN}
DON'T CARE
SGL/ $\overline{DIFF}$
MSBF
Hi-Z
Null Bit
B7
B6
B5
B4
B3
B2
B1
B0
FILLED WITH ZEROES
Hi-Z
D_{OUT}
t_{SMPL}
t_{CONV}

MSB First Data (MSBF=0)


t_{CYC}
$\overline{CS}$
t_{wakeup}
$t_{su\overline{CS}}$
CLK
ODD/ SIGN
START
D_{IN}
DON'T CARE
SGL/ $\overline{DIFF}$
MSBF
Hi-Z
Null Bit
B7
B6
B5
B4
B3
B2
B1
B0
B1
B2
B3
B4
B5
B6
B7
Hi-Z
D_{OUT}
FILLED WITH ZEROES
t_{SMPL}
t_{CONV}

PRELIMINARY

LT1108

Micropower DC-DC Converter Adjustable and Fixed 5V, 12V

FEATURES

- Operates at Supply Voltages From 2.0V to 30V
- Consumes Only 110µA Supply Current
- Works in Step-Up or Step-Down Mode
- Only Three External Components Required
- Low Battery Detector Comparator On-Chip
- User-Adjustable Current Limit
- Internal 1A Power Switch
- Fixed or Adjustable Output Voltage Versions
- Space Saving 8-Pin MiniDIP or SO8 Package

APPLICATIONS

- Palm Top Computers
- 3V to 5V, 5V to 12V Converters
- 9V to 5V, 12V to 5V Converters
- LCD Bias Generators
- Peripherals and Add-On Cards
- Battery Backup Supplies
- Cellular Telephones
- Portable Instruments

DESCRIPTION

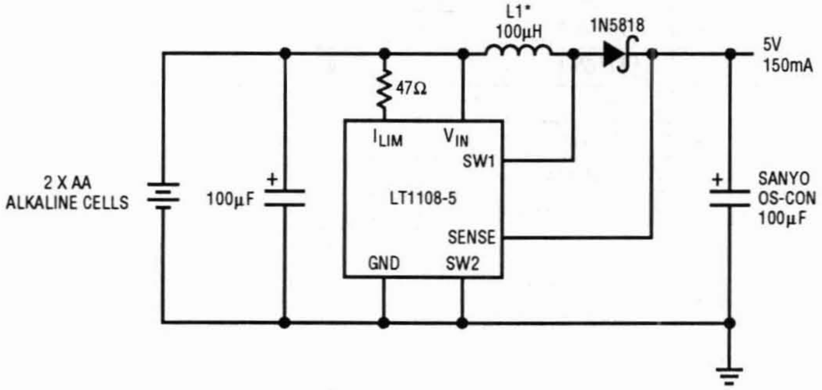
The LT1108 is a versatile micropower DC-DC converter. The device requires only three external components to deliver a fixed output of 5V or 12V. Supply voltage ranges from 2.0V to 12V in step-up mode and to 30V in step-down mode. The LT1108 functions equally well in step-up, step-down or inverting applications.

The LT1108 is pin-for-pin compatible with the LT1173, but has a duty cycle of 70%, resulting in increased output current in many applications. The LT1108 can deliver 150mA at 5V from a 2AA cell input and 5V at 300mA from 9V in stepdown mode. Quiescent current is just 110µA, making the LT1108 ideal for power-conscious battery operated systems.

Switch current limit can be programmed with a single resistor. An auxiliary gain block can be configured as a low battery detector, linear post regulator, under voltage lockout circuit or error amplifier.

TYPICAL APPLICATIONS

Palmtop Computer Logic Supply

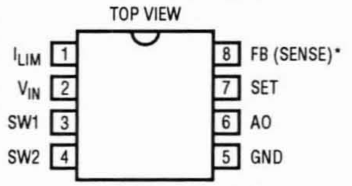
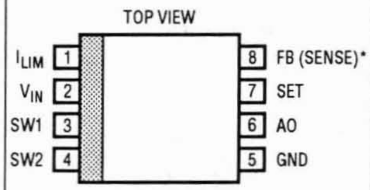


*L1 = GOWANDA GA20-103K
COILTRONICS CTX100-4
SUMIDA CD105-101K

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 36V
SW1 Pin Voltage (V_{SW1}) 50V
SW2 Pin Voltage (V_{SW2}) .... −0.5V to V_{IN}
Feedback Pin Voltage (LT1108) 5V
Sense Pin Voltage (LT1108, -5, -12) 36V
Maximum Power Dissipation 500mW
Maximum Switch Current 1.5A
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature, (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW I_{LIM} 1 V_{IN} 2 SW1 3 SW2 4 8 FB (SENSE)* 7 SET 6 AO 5 GND N8 PACKAGE 8-LEAD PLASTIC DIP *FIXED VERSIONS	LT1108CN8 LT1108CN8-5 LT1108CN8-12
 TOP VIEW I_{LIM} 1 V_{IN} 2 SW1 3 SW2 4 8 FB (SENSE)* 7 SET 6 AO 5 GND S8 PACKAGE 8-LEAD PLASTIC SOIC *FIXED VERSIONS	LT1108CS8 LT1108CS8-5 LT1108CS8-12

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{IN} = 3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off		●		110	150	μA
I_Q	Quiescent Current, Boost Mode Configuration	No Load	LT1108-5			135		μA
			LT1108-12			250		μA
V_{IN}	Input Voltage	Step-Up Mode		●	2.0		12.6	V
		Step-Down Mode		●			30	V
	Comparator Trip Point Voltage	LT1108 (Note 1)		●	1.20	1.245	1.30	V
V_{OUT}	Output Sense Voltage	LT1108-5 (Note 2)		●	4.75	5.00	5.25	V
		LT1108-12 (Note 2)		●	11.4	12.0	12.6	V
	Comparator Hysteresis	LT1108		●		5	10	mV
	Output Hysteresis	LT1108-5		●		20	40	mV
		LT1108-12		●		50	100	mV
f_{OSC}	Oscillator Frequency					19		kHz
	Duty Cycle	Full Load				70		%
t_{ON}	Switch ON Time	I_{LIM} tied to V_{IN}				37		μs
	Feedback Pin Bias Current	LT1108, V_{FB} = 0V		●		10	50	nA
	Set Pin Bias Current	$V_{SET} = V_{REF}$		●		20	100	nA
V_{OL}	Gain Block Output Low	I_{SINK} = 100μA, V_{SET} = 1.00V		●		0.15	0.4	V
	Reference Line Regulation	$2.0V \leq V_{IN} \leq 5V$		●		0.2	0.4	%/V
		$5V \leq V_{IN} \leq 30V$		●		0.02	0.075	%/V
V_{SAT}	SW_{SAT} Voltage, Step-Up Mode	V_{IN} = 3.0V, I_{SW} = 650mA		●		0.5	0.65	V
		V_{IN} = 5.0V, I_{SW} = 1A				0.8	1.0	V

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 3V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SAT}	SW_{SAT} Voltage, Step-Down Mode	$V_{IN} = 12V$, $I_{SW} = 650mA$			1.1	1.5	V
			●			1.7	V
A_V	Gain Block Gain	$R_L = 100k\Omega$ (Note 3)	●	400	1000		V/V
	Current Limit	220Ω from I_{LIM} to V_{IN}			400		mA
	Current Limit Temperature Coeff.		●		−0.3		%/°C
	Switch OFF Leakage Current	Measured at SW1 Pin			1	10	µA
V_{SW2}	Maximum Excursion Below GND	$I_{SW1} \leq 10\mu A$, Switch Off			−400	−350	mV

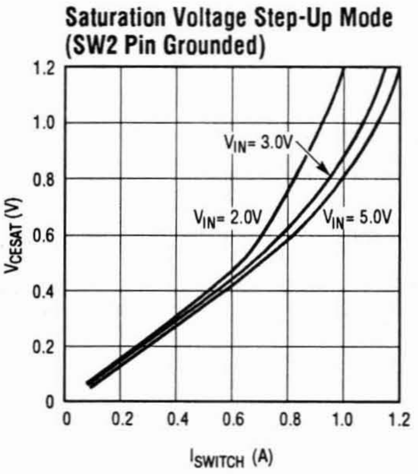
The ● denotes the specifications which apply over the full operating temperature range.

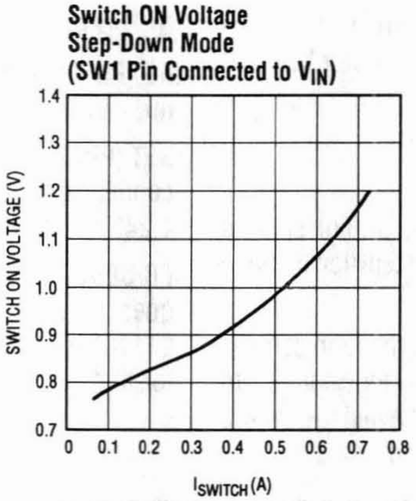
Note 1: This specification guarantees that both the high and low trip points of the comparator fall within the 1.20V to 1.30V range.

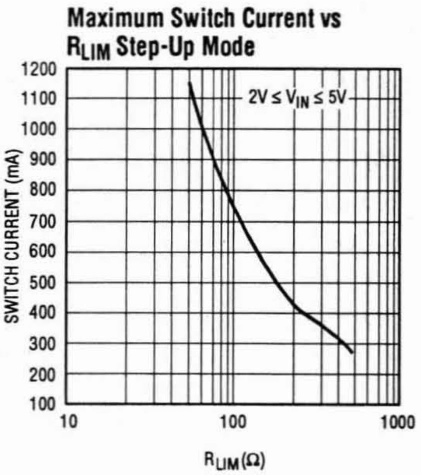
Note 2: The output voltage waveform will exhibit a sawtooth shape due to the comparator hysteresis. The output voltage on the fixed output versions will always be within the specified range.

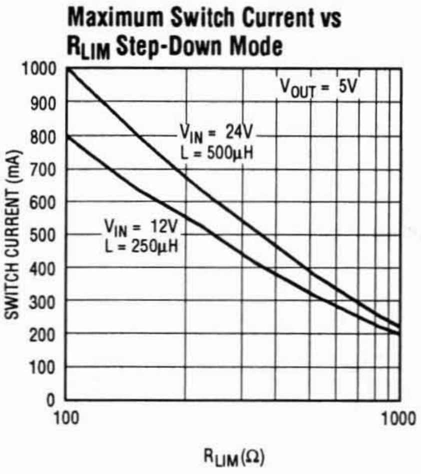
Note 3: 100kΩ resistor connected between a 5V source and the AO pin.

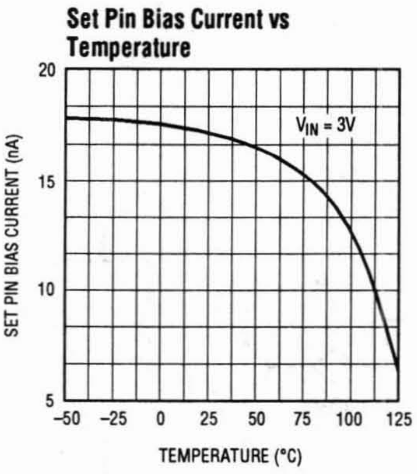
TYPICAL PERFORMANCE CHARACTERISTICS

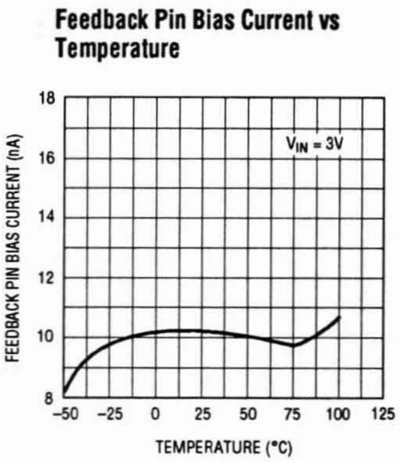

Saturation Voltage Step-Up Mode (SW2 Pin Grounded)


Switch ON Voltage Step-Down Mode (SW1 Pin Connected to V_{IN})

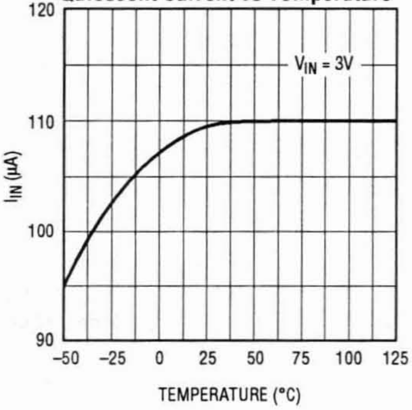

Maximum Switch Current vs R_{LIM} Step-Up Mode


Maximum Switch Current vs R_{LIM} Step-Down Mode

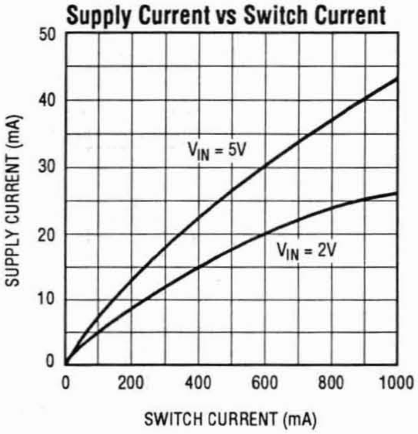

Set Pin Bias Current vs Temperature


Feedback Pin Bias Current vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS



Quiescent Current vs Temperature



Supply Current vs Switch Current

PIN FUNCTIONS

I_{LIM} (Pin 1): Connect this pin to V_{IN} for normal use. Where lower current limit is desired, connect a resistor between I_{LIM} and V_{IN}. A 220Ω resistor will limit the switch current to approximately 400mA.

V_{IN} (Pin 2): Input supply voltage.

SW1 (Pin 3): Collector of power transistor. For step-up mode connect to inductor/diode. For step-down mode connect to V_{IN}.

SW2 (Pin 4): Emitter of power transistor. For step-up mode connect to ground. For step-down mode connect to inductor/diode. This pin must never be allowed to go more than a Schottky diode drop below ground.

GND (Pin 5): Ground.

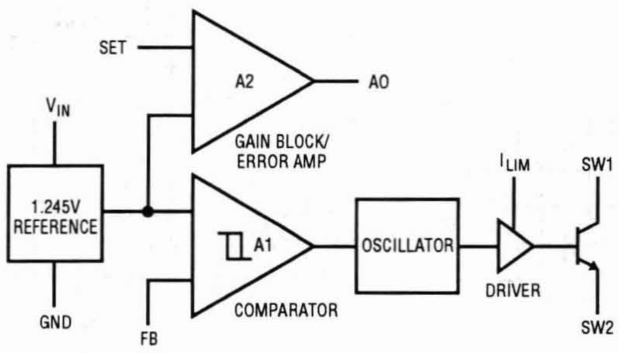
AO (Pin 6): Auxiliary Gain Block (GB) output. Open collector, can sink 100μA.

SET (Pin 7): GB input. GB is an op amp with positive input connected to SET pin and negative input connected to 1.245V reference.

FB/SENSE (Pin 8): On the LT1108 (adjustable) this pin goes to the comparator input. On the LT1108-5 and LT1108-12, this pin goes to the internal application resistor that sets output voltage.

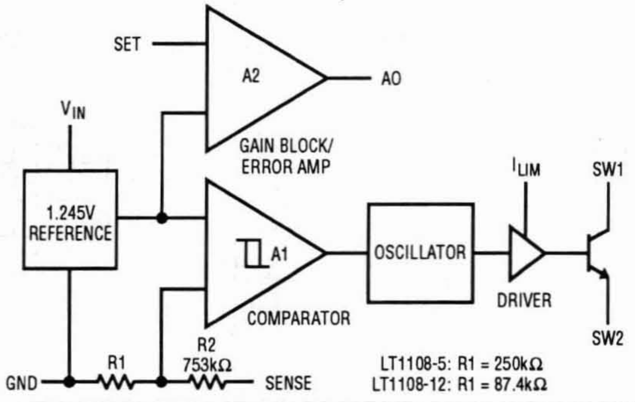
BLOCK DIAGRAMS

LT1108



SET
A2
AO
V_{IN}
GAIN BLOCK/
ERROR AMP
I_{LIM}
SW1
1.245V
REFERENCE
A1
OSCILLATOR
DRIVER
GND
FB
COMPARATOR
SW2

LT1108-5, -12



SET
A2
AO
V_{IN}
GAIN BLOCK/
ERROR AMP
I_{LIM}
SW1
1.245V
REFERENCE
A1
OSCILLATOR
DRIVER
COMPARATOR
SW2
R2
753kΩ
R1
GND
SENSE
LT1108-5: R1 = 250kΩ
LT1108-12: R1 = 87.4kΩ

LINEAR TECHNOLOGY

PRELIMINARY

LT1109A

Micropower Low Cost DC-to-DC Converter Adjustable and Fixed 5V, 12V

February 1992

FEATURES

- Uses Off-the-Shelf Inductors
- Low Cost
- 8-Pin DIP or SO package
- Fixed 5V or 12V Output
- 120kHz Oscillator
- Only Four External Components Required
- 320μA Standby Current
- Logic-Controlled Shutdown

APPLICATIONS

- Flash Memory Vpp Generators
- 3V to 5V Converters
- 5V to 12V Converters
- Disk Drives
- PC Plug-In Cards
- Peripherals
- Battery-Powered Equipment

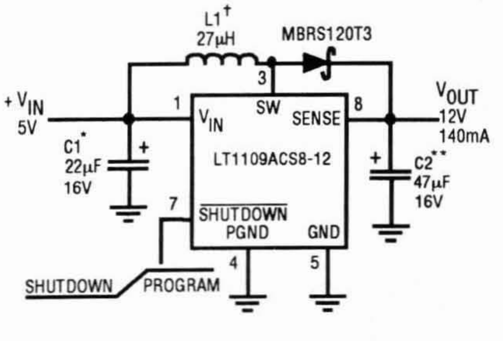
DESCRIPTION

The LT1109A is a simple step-up DC-to-DC converter. The 8-pin DIP or SOIC devices require only four external components to construct a complete DC-to-DC converter. Current drain is just 320μA at no load, making the device ideal for cost-sensitive applications where standby current must be kept to a minimum.

The LT1109A-12 can deliver 12 volts at up to 140mA from a 5 volt supply, enough power to program four Flash Memory chips simultaneously. The LT1109A-5 can deliver 5 volts at up to 150mA from a 2 volt input. The devices feature a SHUTDOWN pin that turns off the oscillator when taken low. The gated-oscillator design requires no frequency compensation components. High frequency 120kHz operation permits the use of small surface mount inductors and capacitors.

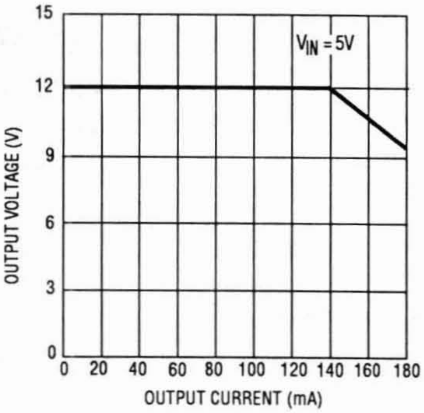
TYPICAL APPLICATION

All Surface Mount
Flash Memory Vpp Generator



† SUMIDA CD54-270K
* MATSUO 267M1602226 OR EQUIVALENT
** MATSUO 267M1602476 OR EQUIVALENT

Output Current

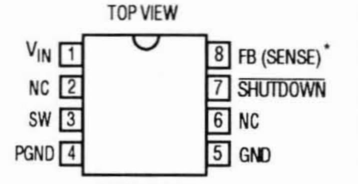


ABSOLUTE MAXIMUM RATINGS

(Voltages Referred to GND Pin)

Supply Voltage (V_{IN})	−0.4V to 20V
SW Pin Voltage	−0.4V to 50V
Feedback Pin Voltage (LT1109A)	5.5V
SHUTDOWN Pin Voltage	5.5V
Maximum Power Dissipation	300mW
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Switch Current	1.6A

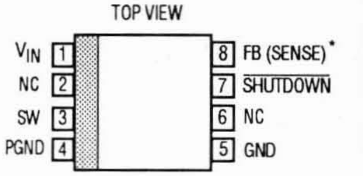
PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
* FIXED VERSIONS

ORDER PART NUMBER

LT1109ACN8
LT1109ACN8-5
LT1109ACN8-12



S8 PACKAGE
8-LEAD PLASTIC SOIC
* FIXED VERSIONS

LT1109ACS8
LT1109ACS8-5
LT1109ACS8-12

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 3V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	Switch Off	●		320	450	μA
V_{IN}	Input Voltage		●	2		9	V
	Comparator Trip Point Voltage	LT1109A	●	1.20	1.25	1.30	V
V_{OUT}	Output Sense Voltage	LT1109A-5; 3V ≤ V_{IN} ≤ 5V	●	4.75	5.00	5.25	V
		LT1109A-12; 3V ≤ V_{IN} ≤ 12V	●	11.52	12.00	12.55	V
	Comparator Hysteresis	LT1109A	●		8	12.5	mV
	Output Voltage Ripple	LT1109A-5	●		25	50	mV
		LT1109A-12	●		60	120	mV
f_{OSC}	Oscillator Frequency				120		kHz
t_{ON}	Switch On Time				5.6		μs
DC	Duty Cycle	Full Load			67		%
V_{CESAT}	Switch Saturation Voltage	Isw = 1A LT1109A-12: V_{IN} = 5V	 ●		0.7 0.8		V V
	Switch Leakage Current				1	10	μA
V_{IH}	SHUTDOWN Pin High		●	2.0			V
V_{IL}	SHUTDOWN Pin Low		●			0.8	V
I_{IH}	SHUTDOWN Pin Input Current	$V_{SHUTDOWN}$ ≥ 2.0V	●			10	μA
I_L	SHUTDOWN Pin Input Current	0V ≤ $V_{SHUTDOWN}$ ≤ 0.8V	●			20	μA

The ● denotes the specifications which apply over the full operating temperature range.

PRELIMINARY

LT1112/LT1114

Dual/Quad Low Power Precision, Picoamp Input Op Amps

FEATURES

■ SO-8 package-standard pin-out	
■ Offset Voltage-prime grade	50μV Max
■ Offset Voltage-low cost grade(incl. SO-8)	75μV Max
■ Offset Voltage Drift	0.2μV/°C
■ Input Bias Current	280pA Max
■ 0.1Hz to 10Hz Noise	0.5μVp-p, 2.2pAp-p
■ Supply Current per amplifier	400μA Max
■ CMRR	120dB Min
■ Voltage Gain	1 Million Min
■ Guaranteed Specs with ±1.0V Supplies	
■ Guaranteed Matching Specifications	

APPLICATIONS

- Picoampere/Microvolt Instrumentation
- Two and Three Op Amp Instrumentation Amplifiers
- Thermocouple and Bridge Amplifiers
- Low Frequency Active Filters
- Photo Current Amplifiers
- Battery Powered Systems

DESCRIPTION

The LT1112 dual and LT1114 quad op amps achieve a new standard in combining low cost and outstanding precision specifications.

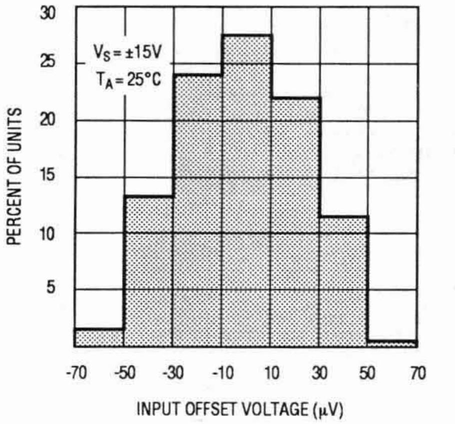
The performance of the selected prime grades matches or exceeds competitive devices. In the design of the LT1112/LT1114, however, particular emphasis has been placed on optimizing performance in the low cost plastic and SO packages. For example, the 75μV maximum offset voltage in these low cost packages is the lowest on any dual or quad, non-chopper op amp.

The LT1112 and LT1114 also provide a full set of matching specifications, facilitating their use in such matching dependent applications as two and three op amp instrumentation amplifiers.

Another set of specifications are furnished at ±1V supplies. This, combined with the low 290μA supply current per amplifier, allow the LT1112/LT1114 to be powered by two nearly discharged AA cells.

Protected by U.S. patents 4,575,685; 4,775,884 and 4,837,496.

DISTRIBUTION OF INPUT OFFSET VOLTAGE (IN ALL PACKAGES)



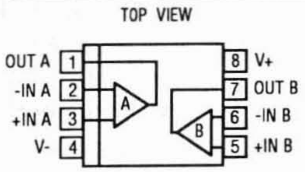
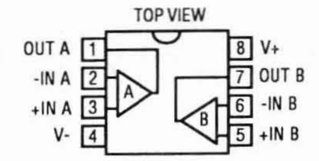
ABSOLUTE MAXIMUM RATINGS

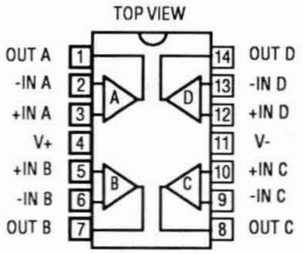
Supply Voltage	±20V
Differential Input Current	±10mA
Input Voltage	±20V
Output Short Circuit Duration	Indefinite
Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range	−65°C to 150°C

Operating Temperature Range

LT1112AM/LT1112M LT1114AM/LT1114M	−55°C to 125°C
LT1112AC/LT1112C/LT1112S8 LT1114AC/LT1114C	−40°C to 85°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW OUT A -IN A +IN A V- 1 2 3 4 A 8 7 6 5 V+ OUT B -IN B +IN B B S8 PACKAGE 8-LEAD PLASTIC SOIC	LT1112S8
 TOP VIEW OUT A -IN A +IN A V- 1 2 3 4 A 8 7 6 5 V+ OUT B -IN B +IN B B J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP	LT1112AMJ8 LT1112MJ8 LT1112ACJ8 LT1112CJ8 LT1112ACN8 LT1112CN8

	ORDER PART NUMBER
 TOP VIEW OUT A -IN A +IN A V+ +IN B -IN B OUT B 1 2 3 4 5 6 7 A B D C 14 13 12 11 10 9 8 OUT D -IN D +IN D V- +IN C -IN C OUT C J PACKAGE 14-LEAD CERAMIC DIP N PACKAGE 14-LEAD PLASTIC DIP	LT1114AMJ LT1114MJ LT1114ACJ LT1114CJ LT1114ACN LT1114CN

ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, $V_{CM} = 0V$, $T_A = 25°C$, unless otherwise noted.

			LT1112AM/AC LT1114AM/AC			LT1112M/C/S8 LT1114M/C			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{OS}	Input Offset Voltage			20	50		25	75	μV
		$V_S = \pm1.0V$		40	95		45	130	μV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			0.3			0.3		μV/Mo
I_{OS}	Input Offset Current			40	150		40	150	pA
I_B	Input Bias Current			±80	±280		±80	±280	pA
e_n	Input Noise Voltage	0.1Hz to 10Hz		0.5			0.5		μVp-p
	Input Noise Voltage Density	$f_O = 10Hz$		16			16		nV/√Hz
		$f_O = 1000Hz$		14			14		nV/√Hz
i_n	Input Noise Current	0.1Hz to 10Hz		2.2			2.2		pAp-p
	Input Noise Current Density	$f_O = 10Hz$		0.030			0.030		pA/√Hz
		$f_O = 1000Hz$		0.008			0.008		pA/√Hz
R_{IN}	Input Resistance Differential Mode		30	80		30	80		MΩ
	Common-Mode			10^{12}			10^{12}		Ω
V_{CM}	Input Voltage Range		±13.5	±14.3		±13.5	±14.3		V

ELECTRICAL CHARACTERISTICS

V_S = ±15V, V_{CM} = 0V, T_A = 25°C, unless otherwise noted.

			LT1112AM/AC LT1114AM/AC			LT1112M/C/S8 LT1114M/C			
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±13.5V	120	136		115	136		dB
PSRR	Power Supply Rejection Ratio	V_S = ±1.0V to ±20V	116	126		114	126		dB
A_{VOL}	Large Signal Voltage Gain	V_O = ±12V, R_L = 10kΩ	1000	3000		800	2500		V/mV
		V_O = ±10V, R_L = 2kΩ	450	2000		600	1800		V/mV
V_{OUT}	Output Voltage Swing	R_L = 10kΩ	±13.0	±13.8		±13.0	±13.8		V
		R_L = 2kΩ	±11.5	±13.0		±11.5	±13.0		V
SR	Slew Rate		0.12	0.18		0.12	0.18		V/μs
GBW	Gain-Bandwidth Product	f_O = 10kHz	450	650		450	650		kHz
I_S	Supply Current Per Amplifier			320	400		320	450	μA
		V_S = ±1.0V		290	370		290	420	μA
ΔV_{OS}	Offset Voltage Match			30	75		35	120	μV
ΔI_{B+}	Non-Inverting Bias Current Match			±80	±450		±80	±450	pA
ΔCMRR	Common-Mode Rejection Match		115	132		110	130		dB
ΔPSRR	Power Supply Rejection Match		112	125		110	125		dB

PRELIMINARY

LT1121-5

Micropower Low Dropout Regulator

April 1992

FEATURES

- 0.4V Dropout Voltage
- 150mA Output Current
- 30μA Quiescent Current
- 5V Trimmed Output Voltage
- Controlled Quiescent Current in Dropout
- Shutdown Available in 8-Pin Pkg.
- 16μA Quiescent Current in Shutdown
- Stable With 0.33μF Output Capacitor
- Reverse Battery Protection
- No Reverse Output Current

APPLICATIONS

- Low Current Regulator
- Regulator for Battery Powered Systems
- Post Regulator for Switching Supplys

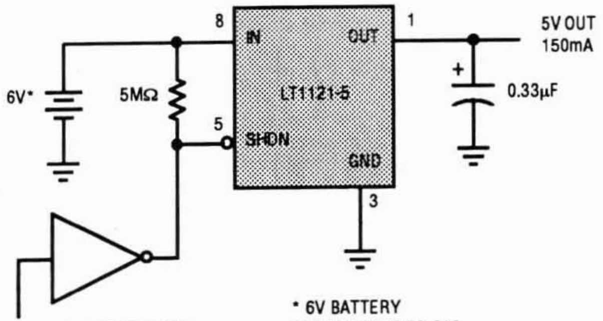
DESCRIPTION

The LT1121-5 is a Micropower Low Dropout Regulator with shutdown. The device is capable of supplying over 150 milliamps of output current with a dropout voltage of 0.4V at maximum output. For use in battery powered systems the low quiescent current, 30 microamps operating and 16 microamps in shutdown, makes it an ideal choice. Also the quiescent current does not rise in dropout as it does with many other low dropout PNP regulators.

Other features of the LT1121-5 include the ability to operate with very small output capacitors. It is stable with only 0.33 μF on the output while most older devices require between 1μF and 100μF for stability. Small ceramic capacitors can be used, enhancing manufacturability. Also the input may be connected to ground or a reverse voltage without reverse current flow from output to input. This makes the LT1121-5 ideal for back-up power situations where the output is held high and the input is at ground or reversed. Only 16μA will flow from the output pin to ground.

TYPICAL APPLICATION

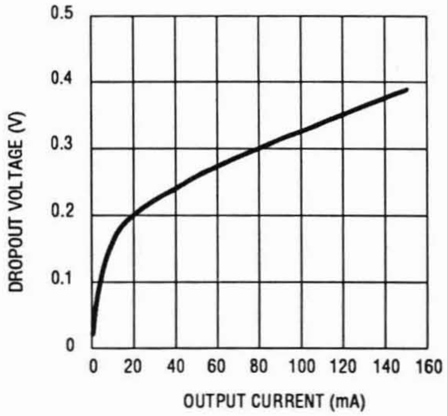
5V BATTERY POWERED SUPPLY WITH SHUTDOWN



OPEN COLLECTOR GATE
SHUTDOWN = INPUT HIGH

* 6V BATTERY
POWER SONIC PS-610
OR EQUIVALENT

Dropout Voltage

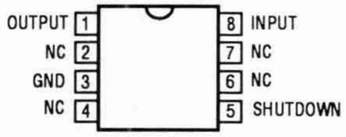
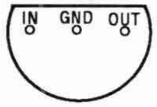


ABSOLUTE MAXIMUM RATINGS

Input Voltage .... ±20V
Shutdown Input Voltage* .... +5.5V, -0.6V
Output Short Circuit Duration .... Indefinite
Operating Junction Temperature Range
  LT1121M .... -55°C to 125°C
  LT1121C .... 0°C to 100°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

* LOW IMPEDANCE SOURCE

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
TOP VIEW  OUTPUT 1 NC 2 GND 3 NC 4 8 INPUT 7 NC 6 NC 5 SHUTDOWN J8 PACKAGE CERAMIC DIP N8 PACKAGE PLASTIC DIP S8 PACKAGE PLASTIC SO	LT1121MJ8-5 LT1121CJ8-5 LT1121CN8-5 LT1121CS8-5 **S8 PART MARKING** 12105
BOTTOM VIEW  Z PACKAGE TO-92 PLASTIC	LT1121CZ-5

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Regulated Output Voltage	V_{IN}= 5.5V, Tj= 25°C		4.925	5.000	5.075	V
	6V< V_{IN}< 20V, 1mA< I_{OUT}< 100mA	●	4.850		5.100	V
	6V< V_{IN}< 20V, 1mA< I_{OUT}< 150mA	●	4.800		5.100	V
Line Regulation	ΔV_{IN} = 5.5V to 20V, I_{OUT} = 1mA	●		1	10	mV
Load Regulation	ΔI_{load} = 1mA to 150mA, Tj = 25C			- 0.005	- 0.007	%/mA
	ΔI_{load} = 1mA to 150mA	●		- 0.008	- 0.012	%/mA
Dropout Voltage	I_{load} = 50mA	●		0.30	0.50	V
	I_{load} =100mA	●		0.37	0.60	V
	I_{load} =150mA	●		0.42	0.70	V
Ground Pin Current	I_{load} =0mA, V_{IN} = 5V	●		30	45	µA
	I_{load} =1mA, V_{IN} = 5V	●		90	130	µA
	I_{load} = 50mA, V_{IN} = 5V	●		2.0	2.5	mA
	I_{load} = 100mA, V_{IN} = 5V	●		5.0	8.0	mA
	I_{load} = 150mA, V_{IN} = 5V	●		10.0	15.0	mA
Input Pin Reverse Leakage Current	V_{IN} = -20V, V_{OUT} = 0V	●			1.0	mA
Reverse Output Current	V_{IN} = 0V, V_{OUT} = 5V			16	25	µA
Shutdown Threshold	V_{OUT} = off to on	●		1.2	3.0	V
	V_{OUT} = on to off	●	0.2	0.75		V
Shutdown Pin Current	V_{SHDN} = 0V	●		6	10	µA
Quiescent Current in Shutdown	V_{IN} = 6V, V_{SHDN} = 0V	●		16	25	µA
Ripple Rejection	V_{IN} = 6V, I_{load} = 0.1A, V_{RIPPLE} = 0.5Vp-p	●	50	58		dB
Current Limit	V_{IN} - V_{OUT} = 7V			220	500	mA

The ● denotes specifications which apply over the operating temperature range.

13

PRELIMINARY

LT1123-2.85

Low Dropout Regulator Driver for SCSI-2 Active Termination

July 1991

FEATURES

- Extremely Low Dropout
- Low Cost
- Fixed 2.85V Output, Trimmed to ±1%
- 600μA Quiescent Current
- 3-Pin TO-92 Package
- 8-Pin SOIC Package
- 1mV Line Regulation
- 2mV Load Regulation
- Thermal Limit

DESCRIPTION

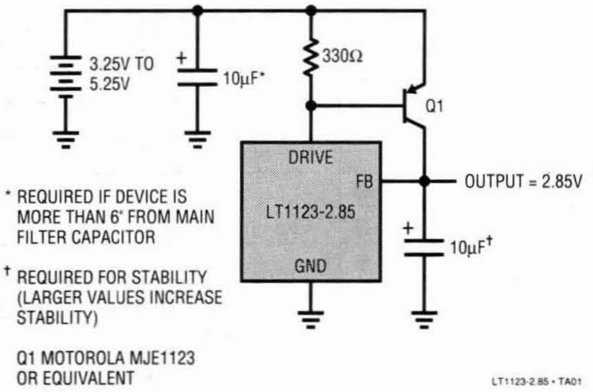
The LT1123-2.85 is a 3-pin bipolar device designed to be used in conjunction with a discrete PNP power device to form an inexpensive low dropout regulator. The LT1123-2.85 consists of a trimmed bandgap reference, error amplifier, and a driver circuit capable of sinking up to 70mA of base current from the external PNP pass device. The LT1123-2.85 is designed to be used in SCSI-2 Active Terminator circuits. It is designed to provide a fixed output voltage of 2.85V, at output currents of up to 1A.

The drive pin of the device can pull down to 2V at 70mA (1.4V at 10mA). This allows a resistor to be used to limit the base drive available to the PNP. This resistor also minimizes the power dissipation in the LT1123-2.85. The drive current of the device is folded back as the feedback pin approaches ground to further limit the available drive current under short circuit conditions.

Total quiescent current for the device is only 600μA. The device is available in a low cost TO-92 package, and an 8-pin SOIC package.

TYPICAL APPLICATION

2.85V Low Dropout Regulator



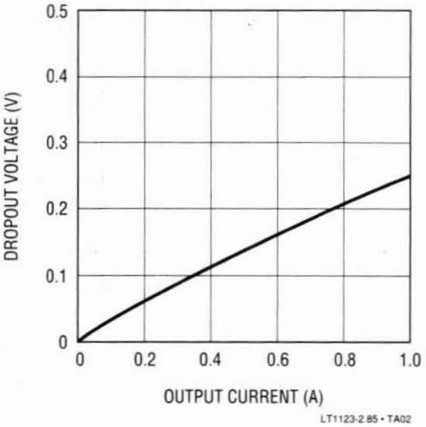
* REQUIRED IF DEVICE IS MORE THAN 6" FROM MAIN FILTER CAPACITOR

† REQUIRED FOR STABILITY (LARGER VALUES INCREASE STABILITY)

Q1 MOTOROLA MJE1123 OR EQUIVALENT

LT1123-2.85 • TA01

Dropout Voltage

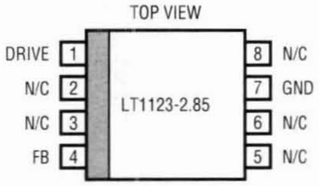
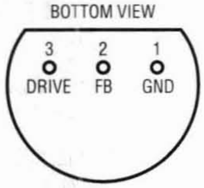


LT1123-2.85 • TA02

ABSOLUTE MAXIMUM RATINGS

Drive Pin Voltage (V_{DRIVE} to Ground) 15V
Feedback Pin Voltage (V_{FB} to Ground) 15V
Operating Temperature Range .... 0°C to 100°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

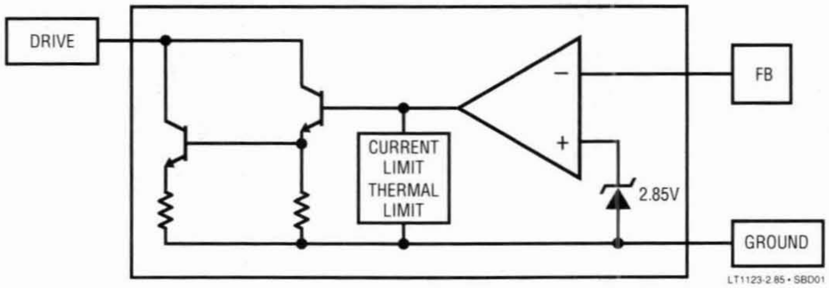
PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW DRIVE 1 N/C 2 N/C 3 FB 4 LT1123-2.85 8 N/C 7 GND 6 N/C 5 N/C S PACKAGE 8-LEAD PLASTIC SOIC LT1123-2.85 • PO02	LT1123CS8-2.85
 BOTTOM VIEW 3 2 1 DRIVE FB GND Z PACKAGE 3-LEAD TO-92 PLASTIC LT1123-2.85 • PO01	LT1123CZ-2.85

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$I_{DRIVE} = 10mA$	2.82	2.85	2.88	V
	$10mA \leq I_{DRIVE} \leq 50mA$ $3V \leq V_{DRIVE} \leq 10V$ $0°C \leq T_J \leq 100°C$	2.79	2.85	2.91	V
Feedback Pin Bias Current	$V_{FB} = 2.85V$		300	500	μA
Drive Current	$V_{FB} = 2.95V$		0.45	1.0	mA
	$V_{FB} = 2.70V$	50	70		mA
	$V_{FB} = 0V$	25	40	100	mA
Drive Pin Saturation Voltage	$I_{DRIVE} = 10mA$		1.4		V
	$I_{DRIVE} = 50mA$		1.7		V
Line Regulation ΔV_{OUT}	$3V < V_{DRIVE} < 10V$		0.3	±10	mV
Load Regulation	$\Delta I_{DRIVE} = 10$ to 50mA		– 2	– 20	mV
Temperature Coeffcient ΔV_{OUT}			0.2		mV/°C

SIMPLIFIED BLOCK DIAGRAM


DRIVE
FB
–
+
CURRENT LIMIT THERMAL LIMIT
2.85V
GROUND

LT1123-2.85 • SBD01

PRELIMINARY

LT1128

Unity Gain Stable Ultra-Low Noise Precision LT1028 Type Op Amp

April 1992

FEATURES

Available in 8-pin SO Package	
Gain-Bandwidth Product	20MHz Typ
Slew Rate	6V/µs Typ 4.5V/µs Min
Voltage and Current Noise 100% Tested	
Voltage Noise	1.1nV/√Hz Max at 1kHz 0.85nV/√Hz Typ at 1kHz 1.0nV/√Hz Typ at 10Hz 35nVp-p Typ, 0.1Hz to 10Hz
Offset Voltage	40µV Max
Voltage Gain	7 Million Min
Drift with Temperature	0.8µV/°C Max

APPLICATIONS

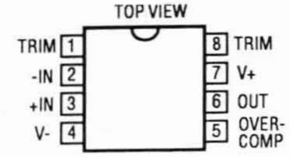
- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

DESCRIPTION

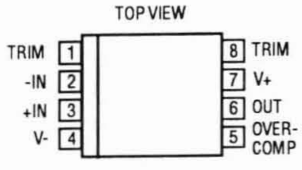
The LT1128 is a unity gain stable version of the LT1028 op amp with a typical slew rate of 6V/µs and a typical gain bandwidth product of 20MHz (measured at 200 kHz). None of the DC specifications of the LT1028 were sacrificed to make the LT1128. 1kHz noise is 0.85nV/√Hz and 1.0nV/√Hz at 10Hz noise. This ultra low noise is combined with true precision parameters, (0.1µV/°C drift, 10µV offset voltage, 30 million voltage gain).

The LT1128's voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1128's contribution to total system noise will be negligible.

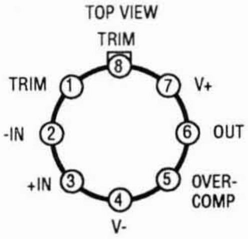
The LT1128 is available in the SO8 package for high density boards.



J PACKAGE 8-LEAD CERAMIC DIP N PACKAGE 8-LEAD PLASTIC DIP

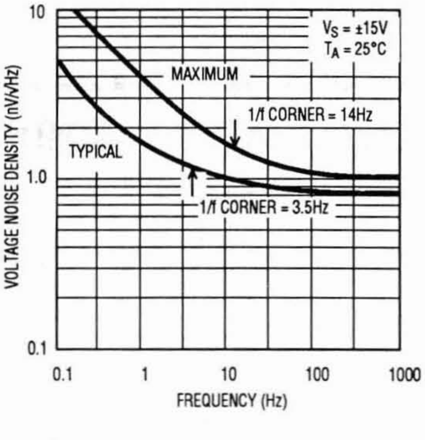


SO PACKAGE 8-LEAD PLASTIC SOIC



H PACKAGE TO-5 METAL CAN

Voltage Noise vs Frequency



PRELIMINARY

LT1129-2.85, LT1129-3.3, LT1129-5

500mA Low Iq Low Dropout Regulator

April 1992

FEATURES

- 0.4V Dropout Voltage
- 500mA Output Current (700mA peak)
- 50µA Quiescent Current
- 2.85V, 3.3V, and 5V Trimmed Output Voltages
- Controlled Quiescent Current in Dropout
- Shutdown Pin
- 30µA Quiescent Current in Shutdown
- Stable With 3.3µF Output Capacitor
- Reverse Battery Protection
- No Reverse Output Current

APPLICATIONS

- Low Current Regulator
- Regulator for Battery Powered Systems
- Post Regulator for Switching Supplys

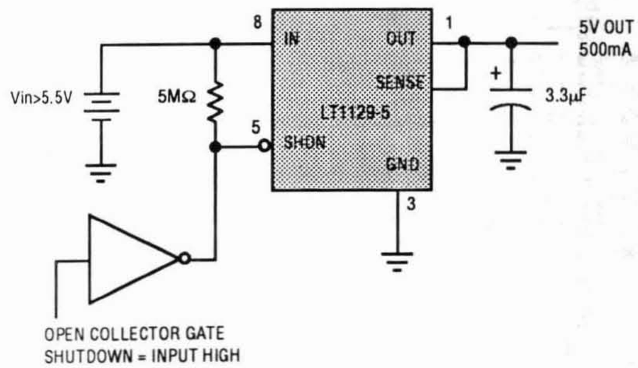
DESCRIPTION

The LT1129 is a Micropower Low Dropout Regulator with shutdown. The device is capable of supplying over 500 milliamps of output current with a dropout voltage of 0.4V at maximum output. For use in battery powered systems the low quiescent current, 50 microamps operating and 30 microamps in shutdown, makes it an ideal choice. Also the quiescent current does not rise in dropout as it does with many other low dropout PNP regulators.

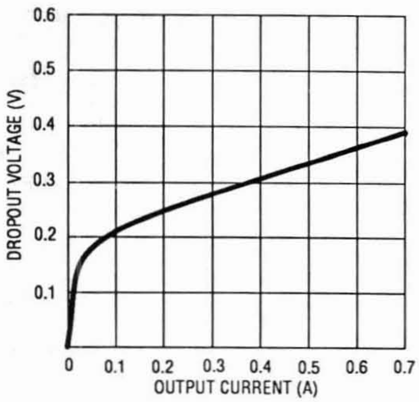
Other features of the LT1129 include the ability to operate with small output capacitors. It is stable with only 3.3µF on the output while most older devices require between 10µF and 100µF for stability. Also the input may be connected to ground or a reverse voltage without reverse current flow from output to input. This makes the LT1129 ideal for back-up power situations where the output is held high and the input is at ground or reversed. Only 16µA will flow from the output pin to ground. The device is available in 5-lead TO-220 and surface mount DD packages.

TYPICAL APPLICATION

5V SUPPLY WITH SHUTDOWN



Dropout Voltage



PRELIMINARY

LT1137A

Advanced Low Power 5V RS232 Transceiver with Small Capacitors

June, 1992

FEATURES

- ESD Protection over ±**10kV**
- Uses Small Capacitors (0.1μF, 0.2μF)
- 1μA Supply Current in SHUTDOWN
- Pin Compatible with LT1137
- Operates to 120kbaud
- CMOS Comparable Low Power-60mW
- Operates from a Single 5V Supply
- Easy PC layout-Flow Through Architecture
- Rugged Bipolar Design
- Outputs assume a High Impedance State When Off or Powered Down
- Improved Protection-RS232 I/O Lines Can be Forced to ±30V Without Damage
- Output Overvoltage Does Not Force Current Back Into Supplies
- Absolutely No Latchup
- Available in SO Package

APPLICATIONS

- Notebook Computers
- Palmtop Computers

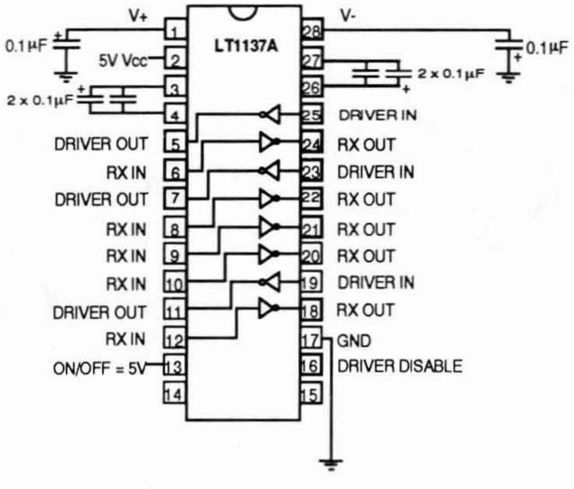
DESCRIPTION

The LT1137A is a 3 driver, 5 receiver RS232 transceiver, pin compatible with the LT1137 - offering performance improvements and two SHUTDOWN modes. The LT1137A's charge pump is designed for extended compliance, and can deliver over 40mA of load current. Supply current is typically 12mA - competitive with similar CMOS devices. An advanced driver output stage operates up to 120kbaud while driving heavy capacitive loads.

The LT1137A is fully compliant with all EIA-RS232 specifications. Special bipolar construction techniques protect the drivers and receivers beyond the fault conditions stipulated for RS232. Driver outputs and receiver inputs can be shorted to ±30V without damaging the device or the power supply generator. In addition, the RS232 I/O pins are resilient to multiple ±10kV ESD strikes.

The transceiver has two shutdown modes. One mode disables the drivers and the charge pump, the other shuts down all circuitry. While shut down, the drivers and receivers assume high impedance output states.

Typical Application


V+
V-
LT1137A
0.1μF
0.1μF
5V Vcc
2 x 0.1μF
2 x 0.1μF
DRIVER OUT
RX IN
DRIVER OUT
RX IN
RX IN
RX IN
DRIVER OUT
RX IN
ON/OFF = 5V
DRIVER IN
RX OUT
DRIVER IN
RX OUT
RX OUT
RX OUT
DRIVER IN
RX OUT
GND
DRIVER DISABLE
1
2
3
4
5
6
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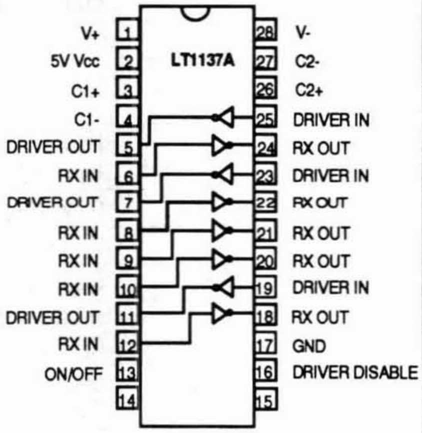
16
15

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Vcc) 6V
V+ .... +13.2V
V- ....-13.2V
Input Voltage
  Driver .... V+ to V-
  Receiver .... +30V to -30V
Output Voltage
  Driver .... -55°C to 125°C
  Receiver .... 0°C to 70°C
Short Circuit Duration
V+ 30s
V- 30s
Driver Output .... Indefinite
Receiver Output .... Indefinite
Operating Temperature Range
  LT1137AM .... -55°C to 125°C
  LT1137AM .... -40°C to 85°C
  LT1137AC .... 0°C to 70°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION


LT1137A
V+ 1
5V Vcc 2
C1+ 3
C1- 4
DRIVER OUT 5
RX IN 6
DRIVER OUT 7
RX IN 8
RX IN 9
RX IN 10
DRIVER OUT 11
RX IN 12
ON/OFF 13
14
28 V-
27 C2-
26 C2+
25 DRIVER IN
24 RX OUT
23 DRIVER IN
22 RX OUT
21 RX OUT
20 RX OUT
19 DRIVER IN
18 RX OUT
17 GND
16 DRIVER DISABLE
15

ORDER PART NUMBER

LT1137AMJ
LT1137ACJ
LT1137ACN
LT1137ACS

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V+ Output				8.6		V
V- Output				-7.8		V
Supply Current (V_{CC})	(Note 3)			12	17	mA
Supply Current when OFF (V_{CC})	SHUTDOWN -55°C ≤ T_A ≤ 125°C (Note 4)	●		0.001	0.10	mA
	SHUTDOWN 0°C ≤ T_A ≤ 70°C	●		0.001	0.010	mA
	DRIVER DISABLE			4		mA
Supply Rise Time	C1,C2,C+,C- = 1.0uF			2		ms
SHUTDOWN to Turn On	C+,C- = 0.1μF, C1, C2 = 0.2μF			0.2		ms
ON/OFF Pin Thresholds	Input Low Level (Device SHUTDOWN)	●		1.4	0.8	V
	Input High Level (Device Enabled)	●	2.0	1.4		V
ON/OFF Pin Current	0V ≤ $V_{ON/OFF}$ ≤ 5V	●	-15		80	μA
Driver Disable Pin Thresholds	Input Low Level (Drivers Enabled)	●		1.4	0.8	V
	Input High Level (Drivers Disabled)	●	2.0	1.4		V
DRIVER DISABLE Pin Current	0V ≤ $V_{DRIVER\ DISABLE}$ ≤ 5V	●	-10		500	μA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Voltage Swing	Load = 3k to GND Positive	●	5.0	7.3		V
	Negative	●	-5.0	-6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT}=High)	●		1.4	0.8	V
	Input High Level (V_{OUT}=Low)	●	2.0	1.4		V
Logic Input Current	$0.8V \le V_{IN} \le 2.0V$	●		5	20	μA
Output Short Circuit Current	$V_{OUT} = 0V$			± 17		mA
Output Leakage Current	SHUTDOWN $V_{OUT} = \pm 30V$ (Note 4)	●		10	100	μA
Slew Rate	R_L=3k, C_L=51pF			15	30	V/μs
	R_L=3k, C_L=2500pF		4	15		V/μs
Propagation Delay	Output Transition t_{HL} High to Low (Note 5)			0.6	1.3	μS
	Output Transition t_{LH} Low to High			0.5	1.3	μS
Any Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)		0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)			1.7	2.4	V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance			3	5	7	kΩ
Output Voltage	Output Low, i_{OUT} = -1.6mA	●		0.2	0.4	V
	Output High, i_{OUT} = 160μA (V_{CC} = 5V)	●	3.5	4.2		V
Ouput Leakage Current	SHUTDOWN (Note) $0 \le V_{OUT} \le V_{CC}$	●		1	10	μA
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$		-10	-20		mA
	Sourcing Current, V_{OUT} = 0V		10	20		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)			250	600	nS
	Output Transition t_{LH} Low to High			350	600	nS

The ● denotes specifications which apply over the operating temperature range. (0 °C ≤ T_A ≤ 70° C for commercial grade, -40°C ≤ T_A ≤ 85°C for industrial grade, and -55°C ≤ T_A ≤ 125°C for military grade.)

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/OFF}$=3V.

Note 3: Supply current is measured with driver and receiver outputs unloaded and the driver inputs tied high.

Note 4: Supply current measurements in SHUTDOWN are performed with $V_{ON/OFF}$ = 0.1V. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE}$ = 3V.

Note 5:For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing. (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V)

Note 6:For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold. (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V)

PIN FUNCTIONS

V_{CC}: +5V Input supply pin. Supply current drops to zero in the SHUTDOWN mode. This pin should be decoupled with a 0.1μF ceramic capacitor.

GND: Ground Pin.

On/Off: Controls the operation mode of the device and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places the all of the drivers and receivers in high impedance state. A logic high fully enables the transceiver.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all drivers in a high impedance state. Supply current drops to 4mA (typ) with Driver Disable active. All receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic low level fully enables the transceiver.

V+: Positive supply output (RS232 drivers). $V+ \approx 2V_{CC}$ - 1.5V. This pin requires an external capacitor C ≥0.1μF for charge storage. The capacitor may be tied to ground or +5V. The V+ output is short circuit proof for 30 seconds. With multiple transceivers, the V+ and V- pins may be paralleled into common capacitors. For large numbers of transceviers, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V-: Negative supply output (RS232 drivers). $V- \approx -(2V_{CC}2.5V)$. This pin requires an external capacitor C ≥ 0.1μF for charge storage. V- is short circuit proof for 30 seconds.

C1+;C1-;C2+;C2-: Commutating capacitor inputs. These pins require two external capacitors C ≥ 0.2μF. One from C1+ to C1-, and another from C2+ to C2-. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2 Ohms. For C≥1μF, low ESR tantalum capacitors work well in this application, although small value ceramic capacitors may be used with a minimal reduction in charge pump compliance. In applications where larger postive voltages are available, such as +12V, C1 may be omitted and the positive voltage may be connected directly to the C1+ pin. In this mode of operation, the V+ pin should be decoupled with a 0.1μF ceramic capacitor.

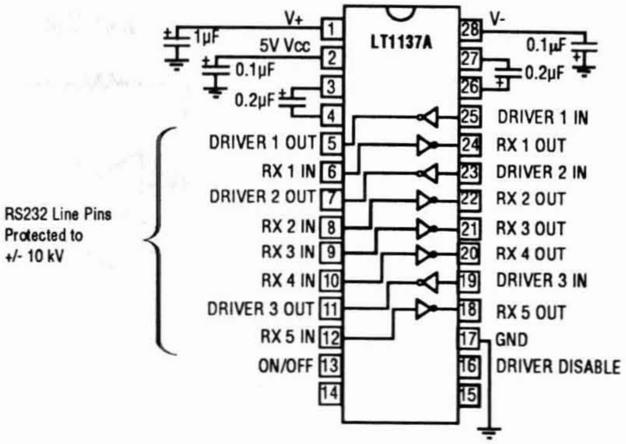
DRIVER IN: RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver outputs at RS232 voltage levels. Outputs are in a high impedance state when in SHUTDOWN mode, V_{CC} = 0V, or when the driver disable pin is active. Outputs are fully short circuit protected from V- + 30V to V+ - 30V with power on, off, SHUTDOWN, or in disabled mode. Typical breakdowns are ±45V. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Although the outputs are protected, short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver inputs. These pins accept RS232 level signals (±30V) into a protected 5kOhm terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance stage when in SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with the power on, off, or in SHUTDOWN mode.

ESD Test Circuit



PRELIMINARY

LTC1151

Dual ±15V Chopper Stabilized Op Amp with Internal Capacitors

September 1991

FEATURES

- High Voltage Operation ±18V Max
- No External Components Required
- Maximum Offset Voltage 5µV
- Maximum Offset Voltage Drift 0.05µV/°C
- Low Noise 1.5µVp-p (0.1Hz to 10Hz)
- Minimum Voltage Gain 140dB
- Minimum CMRR 120dB
- Minimum PSRR 120dB
- Low Supply Current 0.8mA/Amplifier
- Single Supply Operation 4.75V to 36V
- Input Common Mode Range Includes Ground
- Typical Overload Recovery Time 20ms

APPLICATIONS

- Strain Gauge Amplifiers
- Instrumentation Amplifiers
- Electronic Scales
- Medical Instrumentation
- Thermocouple Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

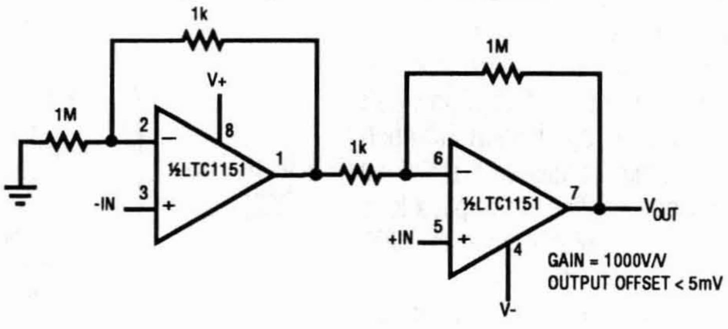
The LTC1151 is a high voltage, high performance dual chopper stabilized operational amplifier. The two sample-and-hold capacitors per amplifier required externally by other chopper amplifiers are integrated on-chip. The LTC1151 also incorporates proprietary high-voltage CMOS structures which allow operation at up to 36V total supply voltage.

The LTC1151 has a typical offset voltage of 0.5µV, drift of 0.01µV/°C, 0.1Hz to 10Hz input noise voltage of 1.5µV p-p, and a typical voltage gain of 180dB. It has a slew rate of 3V/µs and a gain-bandwidth product of 2.5MHz with a supply current of 0.9mA per amplifier. Overload recovery times from positive and negative saturation are 3ms and 20ms, respectively.

The LTC1151 is available in standard plastic 8-pin DIP package, as well as a 16-pin wide-body SO. The LTC1151 is pin compatible with industry standard dual op amps and runs from standard ±15V bipolar supplies, allowing it to plug in to most standard bipolar op amp sockets while offering significant improvement in DC performance.

TYPICAL APPLICATION

High Voltage Instrumentation Amplifier

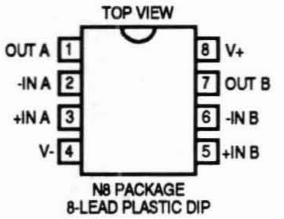
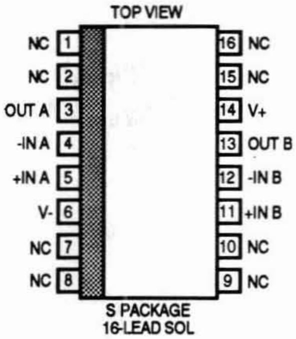


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Input Voltage (Note 2) .... (V^+ + 0.3V) to (V^- - 0.3V)
Output Short Circuit Duration .... Indefinite
Burn-In Voltage 36V
Operating Temperature Range
  LTC1151C .... 0°C to 70°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW OUT A 1 -IN A 2 +IN A 3 V- 4 8 V+ 7 OUT B 6 -IN B 5 +IN B N8 PACKAGE 8-LEAD PLASTIC DIP	LTC1151CN8
 TOP VIEW NC 1 NC 2 OUT A 3 -IN A 4 +IN A 5 V- 6 NC 7 NC 8 16 NC 15 NC 14 V+ 13 OUT B 12 -IN B 11 +IN B 10 NC 9 NC S PACKAGE 16-LEAD SOL	LTC1151CS

ELECTRICAL CHARACTERISTICS

V_S = ±15V, T_A = Operating Temperature Range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1151C MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 3)			±0.5	±5	μV
ΔV_{OS}	Average Offset Voltage Drift	(Note 3)			±0.01	±0.05	μV/°C
I_{OS}	Input Offset Current	T_A = 25°C			±20	±200	pA
			●			±500	pA
I_B	Input Bias Current	T_A = 25°C			±10	±100	pA
			●			±500	pA
E_N	Input Noise Voltage	0.1Hz to 10Hz			1.5		μV p-p
		0.1Hz to 1Hz			0.5		μV p-p
CMRR	Common Mode Rejection Ratio	V_{CM} = V- to 12V		110	130		dB
PSRR	Power Supply Rejection Ratio	V_S = ±2.375V to ±16V		120	145		dB
V_{OUT}	Maximum Output Voltage Swing	R_L = 10KΩ, T_A = 25°C		±13.5	±14.5		V
		R_L = 100KΩ			±14.95		V
I_S	Supply Current per Amplifier	No Load, T_A = 25°C			0.9	1.5	mA
F_S	Internal Sampling Frequency	T_A = 25°C			600		Hz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

Note 2: Connecting any pin to voltages greater than V+ or less than V- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1151.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high-speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

PRELIMINARY

LTC1164-5

Low Power 8th Order Butterworth Lowpass Filter

November 1991

FEATURES

- Butterworth or Bessel Response
- 4mA Supply Current with ±5V Supplies
- f_{CUTOFF} up to 20kHz
- 100μV_{RMS} Wideband Noise
- THD <0.02% (50:1, V_S = ±7.5V, V_{IN} = 2V_{RMS})
- Operates at Single 5V Supply with 1V_{RMS} Input Range
- Operates up to ±8V Supplies
- TTL/CMOS compatible clock input
- 8th Order Filter in a 14-pin Package
- No External Components

APPLICATIONS

- Anti-Aliasing Filters
- Battery Operated Instruments
- Telecommunications Filters
- Smoothing Filters

DESCRIPTION

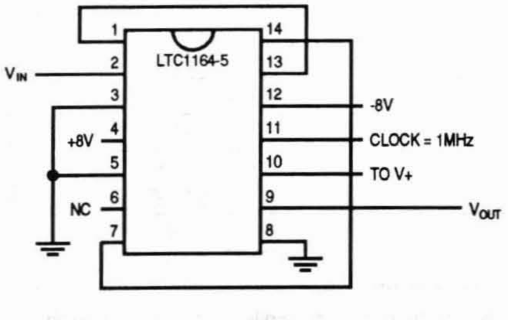
The LTC1164-5 is a monolithic 8th order Butterworth lowpass filter featuring clock-tunable cutoff frequency and low power supply current (4mA with ±5V supplies). Low power operation is achieved without compromising noise or distortion performance. Wideband noise of the LTCC1164-5 is below 100μV_{RMS}. With ±7.5V supplies the filter can handle input signals up to 2.2V_{RMS} with 0.02% THD.

The LTC1164-5 approximates an 8th order Butterworth response with an f_{CLK} to f_{CUTOFF} ratio of 100:1 (pin 10 to V-) or 50:1 (pin 10 to V+ and pin 1 shorted to pin 13). It approximates an 8th order Bessel response with an f_{CLK} to f_{CUTOFF} ratio of 150:1 (pin 10 to gnd). The LTC1164-5 is pin compatible with the LTC1064-2.

The 1164-5 can be clock tuned to a maximum f_{CUTOFF} = 20kHz with ±7.5V supplies, f_{CUTOFF} = 10kHz with ±5V supplies, and f_{CUTOFF} = 6kHz with ±2.5V supplies.

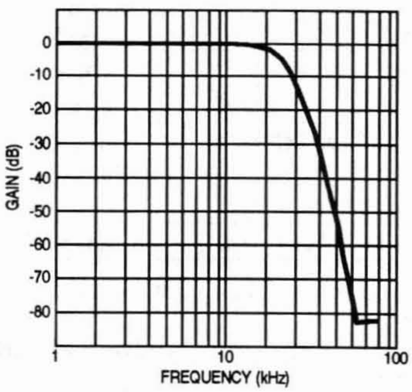
TYPICAL APPLICATION

20kHz Anti-Aliasing Filter



WIDEBAND NOISE = 100μV_{RMS}
THD IN PASSBAND <0.02% AT V_{IN} = 2V_{RMS}
NOTE: THE CONNECTION FROM PIN 7 TO PIN 14 SHOULD BE MADE UNDER THE PACKAGE. FOR 50:1 OPERATION CONNECT PIN 1 TO PIN 13 AS SHOWN. FOR 100:1 OR 150:1 OPERATION PINS 1 AND 13 SHOULD FLOAT. THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1μF CAPACITOR AS CLOSE TO THE PACKAGE AS POSSIBLE.

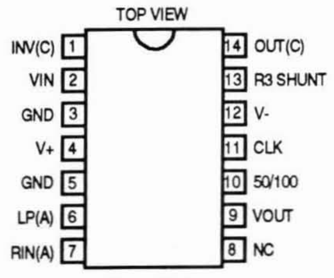
Frequency Response



ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16V
Input Voltage (Note 2) .... (V^+ + 0.3V) to (V^- - 0.3V)
Output Short Circuit Duration .... Indefinite
Power Dissipation 400mW
Burn-In Voltage 16V
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range ....-65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

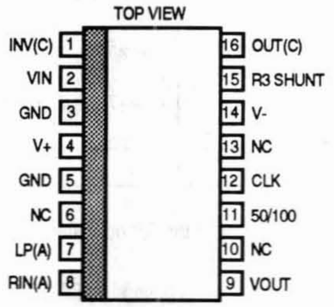
PACKAGE/ORDER INFORMATION


TOP VIEW
INV(C) 1
VIN 2
GND 3
V+ 4
GND 5
LP(A) 6
RIN(A) 7
14 OUT(C)
13 R3 SHUNT
12 V-
11 CLK
10 50/100
9 VOUT
8 NC

N PACKAGE
14-LEAD PLASTIC DIP

ORDER PART NUMBER

LTC1164-5CN
LTC1164-5CJ
LTC1164-5MJ


TOP VIEW
INV(C) 1
VIN 2
GND 3
V+ 4
GND 5
NC 6
LP(A) 7
RIN(A) 8
16 OUT(C)
15 R3 SHUNT
14 V-
13 NC
12 CLK
11 50/100
10 NC
9 VOUT

S PACKAGE
16-LEAD SOL

ORDER PART NUMBER

LTC1164-5CS

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, f_{CLK} = 400kHz, T_A = Operating Temperature Range, unless otherwise specified.

PARAMETER	CONDITIONS		LTC1164-5C MIN	 TYP	 MAX	UNITS
Passband Gain 0.1Hz - 0.25f_{CUTOFF}	f_{IN} = 1kHz, 100:1 f_{IN} = 1kHz, 50:1	● ●	-0.15 -0.20	-0.10 0.10	0.25 0.25	dB dB
Gain at 0.50f_{CUTOFF} (Note 3)	f_{IN} = 2kHz, 100:1 f_{IN} = 4kHz, 50:1	● ●	-0.35 -0.15	-0.20 -0.10	0.17 0.30	dB dB
Gain at 0.90f_{CUTOFF} (Note 3)	f_{IN} = 3.6kHz, 100:1	●	-2.5	-1.90	-1.0	dB
Gain at 0.95f_{CUTOFF} (Note 3)	f_{IN} = 3.8kHz, 100:1	●		-2.60		dB
Gain at f_{CUTOFF} (Note 3)	f_{IN} = 4kHz, 100:1 f_{IN} = 8kHz, 50:1	● ●	-2.75 -2.75	-3.40 -3.80	-4.1 -4.2	dB dB
Gain at 1.44f_{CUTOFF} (Note 3)	f_{IN} = 5.76kHz, 100:1	●	-17.0	-19.0	-20.5	dB
Gain at 2.0f_{CUTOFF} (Note 3)	f_{IN} = 8kHz, 100:1	●	-41.0	-43.0	-45.0	dB
Gain with f_{CLK} = 20kHz	f_{IN} = 200Hz, 100:1	●	-2.75	-3.40	-4.50	dB
Gain with V_S = ±2.375V	f_{CLK} = 400kHz, f_{IN} = 2kHz, 100:1 f_{CLK} = 400kHz, f_{IN} = 4kHz, 100:1		-0.25 -2.0	-0.10 -3.40	0.35 -4.2	dB dB
Input Frequency Range	100:1 50:1			0-<f_{CLK}/2 0-<f_{CLK}		kHz kHz
Maximum f_{CLK}	V_S ≥ ±7.5V V_S = ±5.0V V_S = ±2.375V			1.5 1.0 0.5		MHz MHz MHz
Clock Feedthrough	Input at GND, f ≥ f_{CLK}			200		μV_{RMS}
Wideband Noise	Input at GND, 1Hz ≤ f < f_{CLK}			100±10%		μV_{RMS}

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, F_{CLK} = 400kHz, T_A = Operating Temperature Range, unless otherwise specified.

			LTC1164-5C			
PARAMETER	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
Input Impedance				100		kΩ
Output DC Voltage Swing	V_S = ±2.375V	●	±1.25	±1.5		V
	V_S = ±5.0V	●	±3.70	±4.10		V
	V_S = ±7.5V	●	±5.40	±5.90		V
Output DC Offset				±30	±160	mV
Output DC Offset TempCo				±100		µV/°C
Power Supply Current	V_S = ±2.375V, TA>25°C			2.5	4.0	mA
		●			4.5	mA
	V_S = ±5.0V, TA>25°C			4.5	7.0	mA
		●			8.0	mA
	V_S = ±7.5V, TA>25°C			7.0	11.0	mA
		●			12.5	mA
Power Supply Range			±2.375		±8	V

The ● denotes the specifications which apply over the full operating temprature range.

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impared.

Note 2: Connecting any pin to voltages greater than V+ or less than V- may cause latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1164-5.

Note 3: All gains are measured relative to passband gain.

PIN DESCRIPTION

GENERAL COMMENTS

The following guidelines highlight the information needed to maximize the filter's performance for high precision designs. The filter will function properly when provided with a TTL or CMOS clock source and operated within it's absolute maximum ratings.

Power Supply Pins (4,12)

The V+ (pin 4) and the V- (pin 12) should be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal to noise ratio of the filter. The supply during power up should have a slew rate less than 1V/µS. When V+ is applied before V- and V- is allowed to go above ground, a signal diode should clamp V- to prevent latch up. Figures 1 and 2 show typical connections for dual and single supply operation.

Clock Input Pin (11)

Any TTL or CMOS clock source with a square wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 1 shows the clock's low and high level threshold values for a dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.5µS. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter. The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output in the analog signal path. A 1KΩ resistor between clock source and pin 11 will slow down the rise

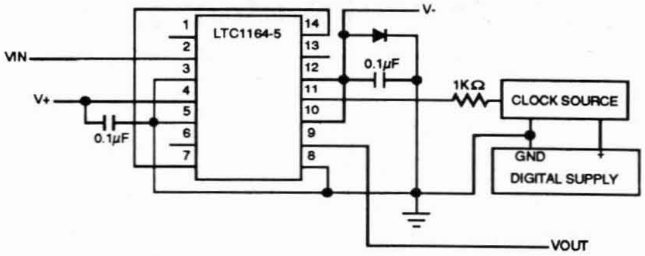


Figure 1. Dual supply operation for a f_{CLK}/f_{CUTOFF} = 100:1.

and fall times of the clock to further reduce charge coupling, figure 1 and 2.

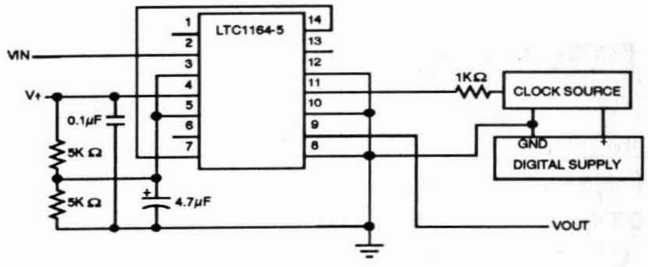


Figure 2. Single supply operation for a f_{CLK}/f_{CUTOFF} = 100:1.

Analog Ground Pins (3,5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pins 3 and 5 should be connected to the analog ground plane. For single supply operation pins 3 and 5 should be biased at 1/2 supply and they should be bypassed to the analog ground plane with at least a 4.7uF capacitor, figure 2.

Ratio Input Pin (10)

The DC level at this pin determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V+ gives a 50:1 ratio and a Butterworth response (pins 1 to 13 should be shorted for 50:1 only.) Pin 10 at V- gives a 100:1 Butterworth response. Pin 10 at ground gives a Bessel response and a ratio of 150:1. For single supply operation the ratio is 50:1 when pin 10 is at V+ (pins 1 to 13 shorted,) 100:1 when pin 10 is at ground and 150:1 when at 1/2 supply. When pin 10 is not tied to ground, it should be bypassed to analog ground with a 0.1μF capacitor. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/μS while the device is operating, a 10kΩ resistor should be connected between pin 10 and the DC source.

Filter Input Pin (2)

The input pin is connected internally through a 100KΩ resistor tied to the inverting input of an op amp.

Filter Output Pins (9,6)

Pin 9 is the specified output of the filter; it can typically source or sink 1 mA. Driving coaxial cables or resistive loads less than 20K will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A non inverting buffer, figure 3, can be used provided that its input common mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

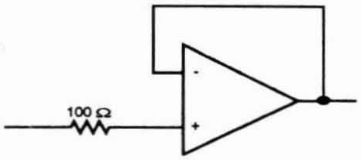


Figure 3. Buffer for filter output.

External Connection Pins (7,14, and 1,13)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane. When the clock to cutoff frequncy ratio is set at 50:1, pin 1 should be shorted to pin 13; if not, the passband will exhibit 1 db of gain peaking and it will deviate from a Butterworth response. Note, for some applications, a small gain peaking may be required to compensate for sinx/x system errors. Pin 1 is the inverting input of an internal op amp and, it should preferably be 0.2 inches away from any other circuit trace.

NC Pin (8)

Pin 8 is not connected to any internal circuit point on the device and should be preferably tied to analog ground.

TABLE 1. Clock Source High and Low threshold levels.

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5Volts	≥ 2.18Volt	≤ 0.5Volt
Dual Supply = ±5.0Volts	≥ 1.45Volt	≤ 0.5Volt
Dual Supply = ±2.5Volts	≥ 0.73Volt	≤ -2.0Volt
Single Supply = 12.0Volt	≥ 7.80Volt	≤ 6.5Volt
Single Supply = 5.0Volt	≥ 1.45Volt	≤ 0.5Volt

PRELIMINARY

LTC1164-6

Low Power 8th Order Elliptic Low Pass Filter

November 1991

FEATURES

- 8th Order Elliptic Filter in a 14-pin Package
- 4mA Supply Current with ±5V Supplies
- 64dB Attenuation at 1.44 f_{CUTOFF}
- f_{CUTOFF} up to 20kHz
- 100:1 f_{CLK} to f_{CUTOFF} Ratio
- $120\mu V_{RMS}$ Wideband Noise
- Operates at Single 5V Supply with $1V_{RMS}$ Input Range
- Operates up to ±8V Supplies
- TTL/CMOS compatible clock input
- No External Components

APPLICATIONS

- Anti-Aliasing Filters
- Battery Operated Instruments
- Telecommunications Filters
- Smoothing Filters

DESCRIPTION

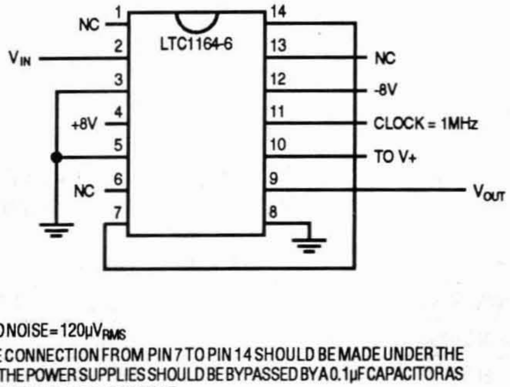
The LTC1164-6 is a monolithic 8th order elliptic lowpass filter featuring clock-tunable cutoff frequency and low power supply current. Low power operation is achieved without compromising noise or distortion performance; the LTC1164-6 uses only 4mA supply current while keeping wideband noise below $120\mu V_{RMS}$.

The LTC1164-6 provides an elliptic low-pass rolloff with stopband attenuation of 64dB at 1.44f_{CUTOFF} and an f_{CLK} to f_{CUTOFF} ratio of 100:1. The LTC1164-6 is pin compatible with the LTC1064-1.

The 1164-6 can be clock tuned to a maximum f_{CUTOFF} = 20kHz with ±7.5V supplies, f_{CUTOFF} = 10kHz with ±5V supplies, and f_{CUTOFF} = 6kHz with ±2.5V supplies.

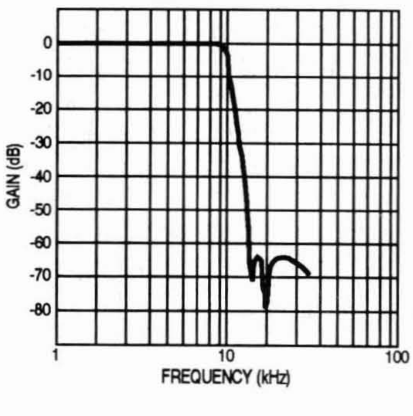
TYPICAL APPLICATION

20kHz Anti-Aliasing Filter



WIDEBAND NOISE = $120\mu V_{RMS}$
NOTE: THE CONNECTION FROM PIN 7 TO PIN 14 SHOULD BE MADE UNDER THE PACKAGE. THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1μF CAPACITOR AS CLOSE TO THE PACKAGE AS POSSIBLE.

Frequency Response

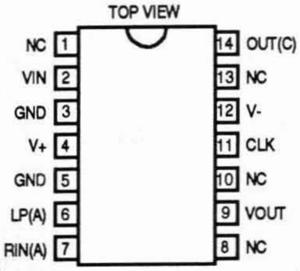
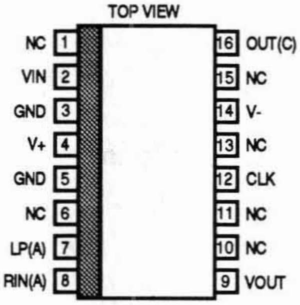


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 16V
Input Voltage (Note 2) .... (V^+ + 0.3V) to (V^- - 0.3V)
Output Short Circuit Duration .... Indefinite
Power Dissipation 400mW

Burn-In Voltage 16V
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range ....-65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER		ORDER PART NUMBER
 TOP VIEW NC 1 VIN 2 GND 3 V+ 4 GND 5 LP(A) 6 RIN(A) 7 14 OUT(C) 13 NC 12 V- 11 CLK 10 NC 9 VOUT 8 NC N PACKAGE 14-LEAD PLASTIC DIP	LTC1164-6CN	 TOP VIEW NC 1 VIN 2 GND 3 V+ 4 GND 5 NC 6 LP(A) 7 RIN(A) 8 16 OUT(C) 15 NC 14 V- 13 NC 12 CLK 11 NC 10 NC 9 VOUT S PACKAGE 16-LEAD SOL	LTC1164-6CS

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, f_{CLK} = 400kHz, T_A = Operating Temperature Range, unless otherwise specified.

PARAMETER	CONDITIONS	LTC1164-6C MIN	TYP	MAX	UNITS
Passband Gain 0.1Hz - 0.25f_{CUTOFF}	f_{TEST} = 1kHz		-0.10		dB
Gain at 0.50f_{CUTOFF} (Note 3)	f_{TEST} = 2kHz		-0.20		dB
Gain at 0.90f_{CUTOFF} (Note 3)	f_{TEST} = 3.6kHz		-0.10		dB
Gain at 0.95f_{CUTOFF} (Note 3)	f_{TEST} = 3.8kHz		-0.40		dB
Gain at f_{CUTOFF} (Note 3)	f_{TEST} = 4kHz		-2.40		dB
Gain at 1.44f_{CUTOFF} (Note 3)	f_{TEST} = 5.75kHz		-65.0		dB
Gain at 2.0f_{CUTOFF} (Note 3)	f_{TEST} = 8kHz		-65.0		dB
Gain with f_{CLK} = 20kHz	f_{TEST} = 200Hz		-2.40		dB
Gain with V_S = ±2.375V	f_{CLK} = 400kHz, f_{TEST} = 2kHz f_{CLK} = 400kHz, f_{TEST} = 4kHz		-0.10 -2.40		dB dB
Input Impedance			30		kΩ
Power Supply Current	V_S = ±5V		4		mA

Note 1: Absolute Maximum Ratings are those values beyond which life of the device may be impared.

Note 2: Connecting any pin to voltages greater than V+ or less than V- may cause latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1164-6.

Note 3: All gains are measured relative to passband gain.

PRELIMINARY

LTC1196/LTC1198

8-Bit, 600ns, 1.3MHz Sampling A/D Converters

November 1991

FEATURES

- 600ns Conversion Time
- 100ns Sample and Hold Acquisition Time
- 1.3MHz Sampling Rate
- SO-8 Plastic Package
- Single Supply 3V to 6V Operation
- Low Power: 10mW @ 3V Supply or
  50mW @ 5V Supply
- 3µA Shutdown (LTC1198)
- ±1/2LSB Total Unadjusted Error Over Temp
- 3 Wire Serial I/O
- 1V to 5V Input Span Range

APPLICATIONS

- High Speed Data Acquisition
- Disk Drives
- Portable or Compact Instrumentation
- Low Power or Battery Operated Systems

DESCRIPTION

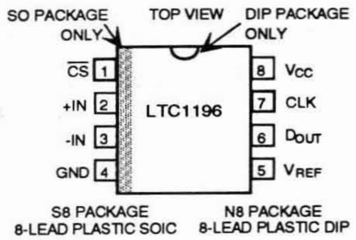
The LTC1196/8 are 600ns, 8-bit A/D converters with a sampling rate of 1.3MHz. They are offered in 8 pin SO packages and operate on 3V to 6V supplies. They draw only 10mW from a 3V supply or 50mW from a 5V supply. The LTC1198 automatically powers down to 3µA of supply current whenever it is not performing conversions. These 8-bit, switched capacitor, successive approximation ADCs include sample and holds. The 1196 has a differential analog input. The 1198 offers a software selectable 2 channel mux.

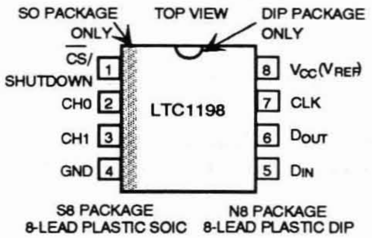
On-chip serial ports allow 8 pin packaging and require only 3 interface lines. The 3 wires transfer data to shift registers, ASICs or microprocessors. SO-8 packages, 3V operation and extremely high sample rate to power ratio (100KHz/mW) provide an ideal choice for compact, high speed systems.

These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans (below 1V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

All grades are specified with offset and linearity errors of ±0.5LSB maximum over temperature. The A grade devices are specified with total unadjusted error of ±0.5LSB maximum over temperature.

PACKAGE INFORMATION


SO PACKAGE ONLY
TOP VIEW
DIP PACKAGE ONLY
$\overline{CS}$ 1
+IN 2
-IN 3
GND 4
LTC1196
8 V_{CC}
7 CLK
6 D_{OUT}
5 V_{REF}
S8 PACKAGE
8-LEAD PLASTIC SOIC
N8 PACKAGE
8-LEAD PLASTIC DIP


SO PACKAGE ONLY
TOP VIEW
DIP PACKAGE ONLY
$\overline{CS}$/SHUTDOWN 1
CH0 2
CH1 3
GND 4
LTC1198
8 V_{CC}(V_{REF})
7 CLK
6 D_{OUT}
5 D_{IN}
S8 PACKAGE
8-LEAD PLASTIC SOIC
N8 PACKAGE
8-LEAD PLASTIC DIP

PRELIMINARY

LT1227

140MHz Video Current Feedback Amplifier

April 1992

FEATURES

- 140MHz Bandwidth, A_V=2, R_L=150Ω
- 1100V/µs Slew Rate
- Low Cost
- 30mA Output Drive Current
- 0.01% Differential Gain
- 0.01° Differential Phase
- High Input Impedance, 14MΩ, 3pF
- Wide Supply Range, ±2V to ±15V
- Shutdown Mode -- I_S<250µA
- Low Supply Current, I_S =10mA
- Inputs Common Mode to Within 1.5V of Supplies
- Outputs Swing Within 0.8V of Supplies

APPLICATIONS

- Video Amplifiers
- Cable Drivers
- RGB Amplifiers
- Test Equipment Amplifiers
- 50Ω Buffers for Driving Mixers

DESCRIPTION

The LT1227 is a current feedback amplifier with wide bandwidth and excellent video characteristics. The low differential gain and phase, wide bandwidth, and the 30mA output current drive makes the LT1227 well suited to drive cables in video systems.

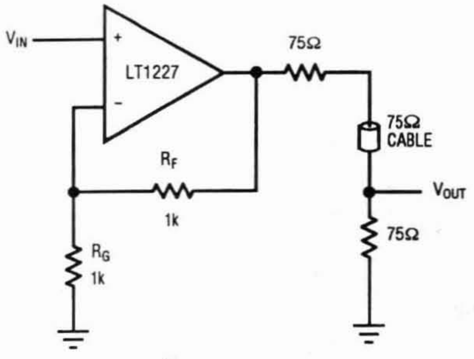
A shutdown feature switches the device into a high impedance, low current mode, allowing multiple devices to be connected in parallel and selected. Input to output isolation in shutdown is 70dB at 10MHz for input amplitudes up to 10Vpp. The shutdown pin interfaces to open collector or open drain logic and takes only 4µs to enable or disable.

The LT1227 comes in the industry standard pinout and can upgrade the performance of many older products. For a dual or quad version, see the LT1229/1230 datasheet.

The LT1227 is manufactured on Linear Technology's proprietary complementary bipolar process.

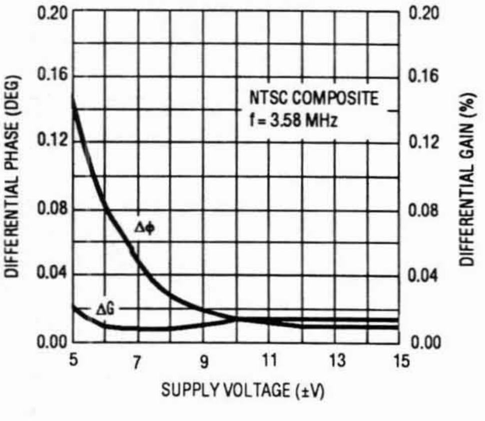
TYPICAL APPLICATION

Video Cable Driver



$$\frac{V_{OUT}}{V_{IN}} = 1$$

Differential Gain and Phase vs Supply Voltage



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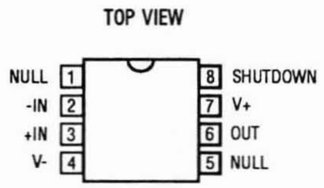
ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... ±18V
Input Current .... ±15mA
Output Short Circuit Duration (Note 1) .... Continuous
Operating Temperature Range
LT1227C .... 0°C to 70°C
LT1227M .... –55°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Junction Temperature
Plastic Package .... 150°C
Ceramic Package .... 175°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1227MJ8 LT1227CN8 LT1227CS8

ELECTRICAL CHARACTERISTICS

V_{CM} = 0, ±5V ≤ V_S ≤ ±15V, pulse tested, unless otherwise noted.

FINAL

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C			±3	±10	mV
			●			±15	mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{IN+}	Non-inverting Input Current	T_A = 25°C			±0.3	±3	µA
			●			±10	µA
I_{IN-}	Inverting Input Current	T_A = 25°C			±10	±60	µA
			●			±100	µA
e_n	Input Noise Voltage Density	f = 1kHz, R_F = 1kΩ, R_G = 10Ω, R_S = 0Ω			3.2		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz, R_F = 1kΩ, R_G = 10Ω, R_S = 10kΩ			1.7		pA/√Hz
R_{IN}	Input Resistance	V_{IN} = ±13V, V_S = ±15V	●	1.5	14		MΩ
		V_{IN} = ±3V, V_S = ±5V	●	1.5	11		MΩ
C_{IN}	Input Capacitance				3		pF
	Input Voltage Range	V_S = ±15V, T_A = 25°C		±13	±13.5		V
			●	±12			V
		V_S = ±5V, T_A = 25°C		±3	±3.5		V
			●	±2			V
CMRR	Common-Mode Rejection Ratio	V_S = ±15V, V_{CM} = ±13V, T_A = 25°C		55	62		dB
		V_S = ±15V, V_{CM} = ±12V	●	55			dB
		V_S = ±5V, V_{CM} = ±3V, T_A = 25°C		55	61		dB
		V_S = ±5V, V_{CM} = ±2V	●	55			dB

ELECTRICAL CHARACTERISTICS

FINAL

V_{CM} = 0, ±5V ≤ V_S ≤ ±15V, pulse tested, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Inverting Input Current Common-Mode Rejection	V_S = ±15V, V_{CM} = ±13V, T_A = 25°C			3.5	10	µA/V
		V_S = ±15V, V_{CM} = ±12V	●			10	µA/V
		V_S = ±5V, V_{CM} = ±3V, T_A = 25°C			4.5	10	µA/V
		V_S = ±5V, V_{CM} = ±2V	●			10	µA/V
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±15V, T_A = 25°C		60	80		dB
		V_S = ±3V to ±15V	●	60			dB
	Non-Inverting Input Current Power Supply Rejection	V_S = ±2V to ±15V, T_A = 25°C			2	50	nA/V
		V_S = ±3V to ±15V	●			50	nA/V
	Inverting Input Current Power Supply Rejection	V_S = ±2V to ±15V, T_A = 25°C			0.25	5	µA/V
		V_S = ±3V to ±15V	●			5	µA/V
A_V	Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_{LOAD} = 1kΩ	●	55	72		dB
		V_S = ±5V, V_{OUT} = ±2V, R_{LOAD} = 150Ω	●	55	72		dB
R_{OL}	Transresistance, $\Delta V_{OUT}/\Delta I_{IN-}$	V_S = ±15V, V_{OUT} = ±10V, R_{LOAD} = 1kΩ	●	100	270		kΩ
		V_S = ±5V, V_{OUT} = ±2V, R_{LOAD} = 150Ω	●	100	240		kΩ
V_{OUT}	Maximum Output Voltage Swing	V_S = ±15V, R_{LOAD} = 400Ω, T_A = 25°C		±12	±13.5		V
			●	±10			V
		V_S = ±5V, R_{LOAD} = 150Ω, T_A = 25°C		±3	±3.7		V
			●	±2.5			V
I_{OUT}	Maximum Output Current	R_{LOAD} = 0Ω, T_A = 25°C		30	60		mA
I_S	Supply Current, Note 2	V_S = ±15V, V_{OUT} = 0V, T_A = 25°C			10	15	mA
			●			17.5	mA
	Positive Supply Current, Shutdown	V_S = ±15V, Pin 8 Voltage = 0V			120	250	µA
			●			500	µA
I_8	Shutdown Pin Current, Note 3	V_S = ±15V	●			200	µA
	Output Leakage Current, Shutdown	V_S = ±15V, Pin 8 Voltage = 0V, T_A = 25°C				10	µA
SR	Slew Rate, Notes 4 and 6	T_A = 25°C		500	1100		V/µs
t_r	Rise Time, Notes 5 and 6	T_A = 25°C			13	25	ns
BW	Small Signal Bandwidth	V_S = ±15V, R_F = 1kΩ, R_G = 1kΩ, R_L = 150Ω			140		MHz
t_r	Small Signal Rise Time	V_S = ±15V, R_F = 1kΩ, R_G = 1kΩ, R_L = 100Ω			3.3		ns
	Propagation Delay	V_S = ±15V, R_F = 1kΩ, R_G = 1kΩ, R_L = 100Ω			3.4		ns
	Small Signal Overshoot	V_S = ±15V, R_F = 1kΩ, R_G = 1kΩ, R_L = 100Ω			5		%
t_s	Settling Time	0.1%, V_{OUT} = 10V, R_F = 1kΩ, R_G = 1kΩ, R_L = 1kΩ			50		ns
	Differential Gain, Note 7	V_S = ±15V, R_F = 1kΩ, R_G = 1kΩ, R_L = 150Ω			0.014		%
	Differential Phase, Note 7	V_S = ±15V, R_F = 1kΩ, R_G = 1kΩ, R_L = 150Ω			0.010		deg

ELECTRICAL CHARACTERISTICS

V_{CM} = 0, ±5V ≤ V_S ≤ ±15V, pulse tested, unless otherwise noted.

FINAL

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Differential Gain, Note 7	V_S = ±15V, R_F = 1kΩ, R_G= 1kΩ, R_L = 1kΩ			0.010		%
	Differential Phase, Note 7	V_S = ±15V, R_F = 1kΩ, R_G= 1kΩ, R_L = 1kΩ			0.013		deg

The ● denotes specifications which apply over the operating temperature range.

Note 1: A heatsink may be required depending on the power supply voltage.

Note 2: The supply current of the LT1227 has a negative temperature coefficient. For more information, see typical performance curves.

Note 3: Ramp pin 8 voltage down from +15V while measuring I_S. When I_S drops to less than .5mA, measure pin8 current.

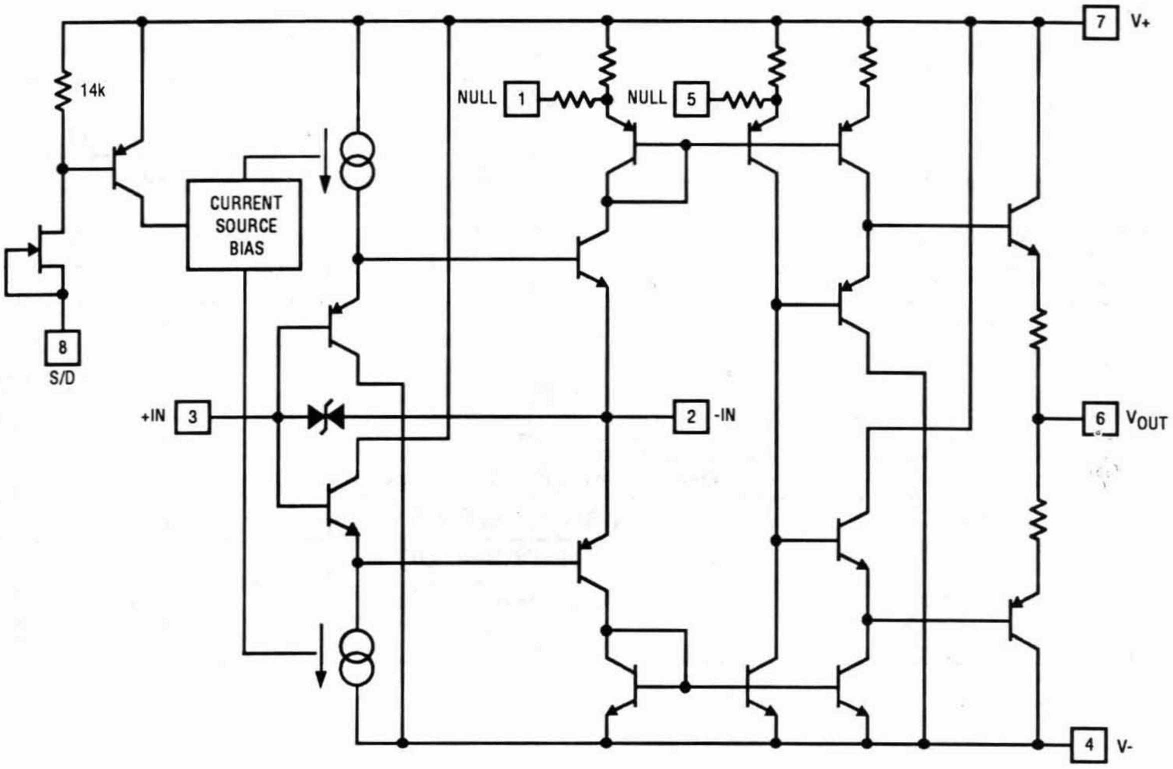
Note 4: Slew rate is measured at ±5 Volts on a ±10 Volt output signal while operating on ±15 Volt supplies with R_F = 2kΩ, R_G = 220Ω and R_{LOAD} = 400Ω.

Note 5: Rise time is measured from 10% to 90% on a ±500 mV output signal while operating on ±15 Volt supplies with R_F = 2kΩ, R_G = 220Ω and R_{LOAD} = 100Ω. This condition is not the fastest possible, however it does guarantee the internal capacitances are correct and it makes automatic testing practical.

Note 6: AC parameters are 100% tested on the ceramic and plastic DIP packaged parts (J and N suffix) and are sample tested on every lot of the SO packaged parts (S suffix).

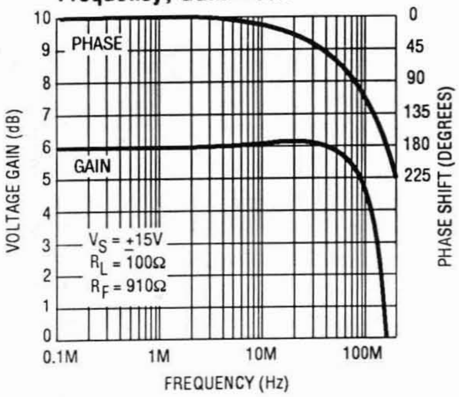
Note 7: NTSC composite video with an output level of 2 Volts.

SIMPLIFIED SCHEMATIC

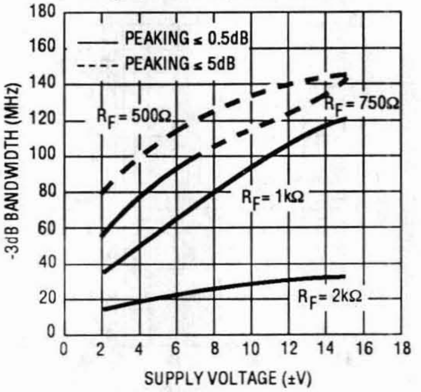


TYPICAL PERFORMANCE CHARACTERISTICS

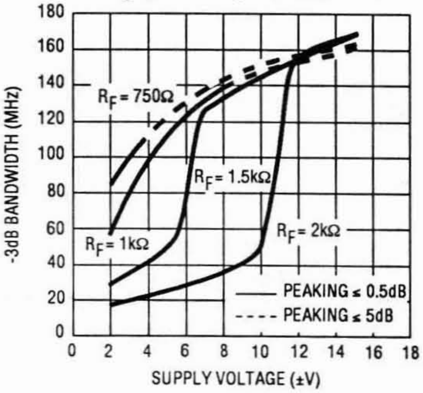
Voltage Gain and Phase vs Frequency, Gain = 6dB



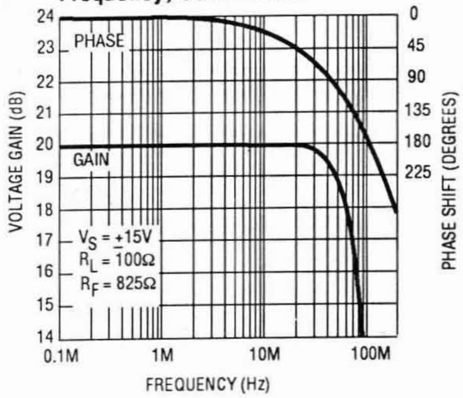
-3dB Bandwidth vs Supply Voltage, Gain=2, RL=100Ω



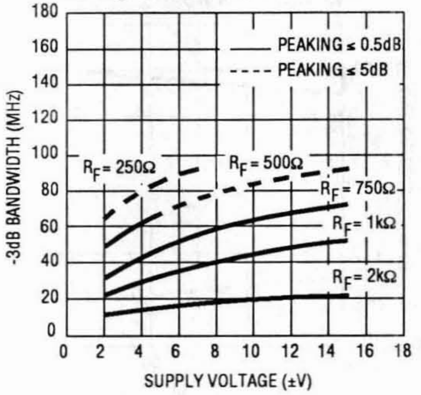
-3dB Bandwidth vs Supply Voltage, Gain=2, RL=1kΩ



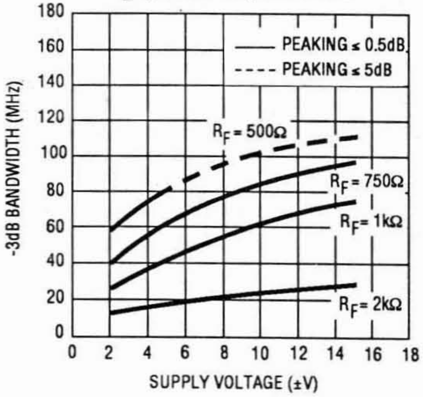
Voltage Gain and Phase vs Frequency, Gain = 20dB



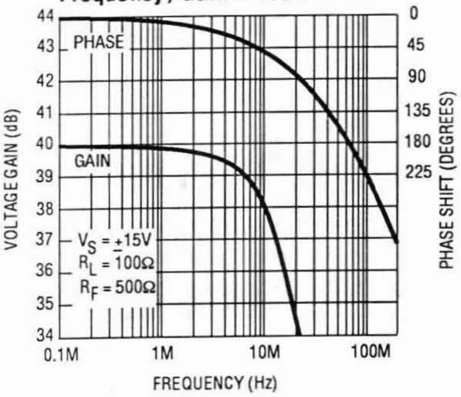
-3dB Bandwidth vs Supply Voltage, Gain=10, RL=100Ω



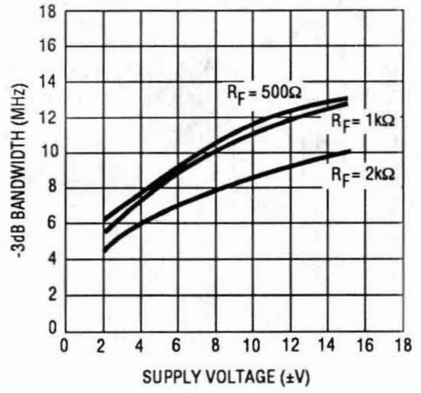
-3dB Bandwidth vs Supply Voltage, Gain=10, RL=1kΩ



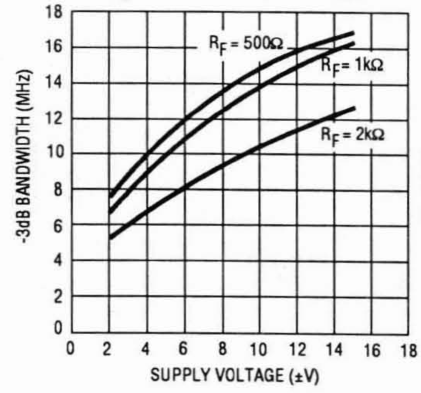
Voltage Gain and Phase vs Frequency, Gain = 40dB



-3dB Bandwidth vs Supply Voltage, Gain=100, RL=100Ω

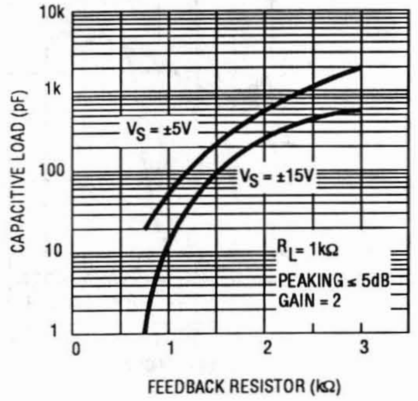


-3dB Bandwidth vs Supply Voltage, Gain=100, RL=1kΩ

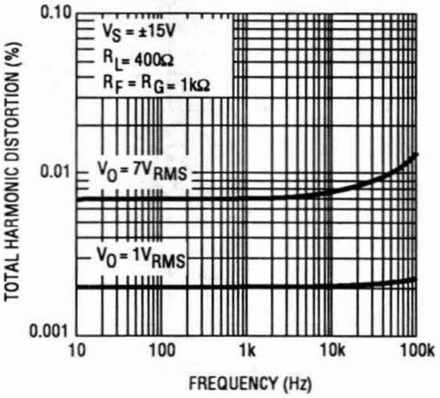


TYPICAL PERFORMANCE CHARACTERISTICS

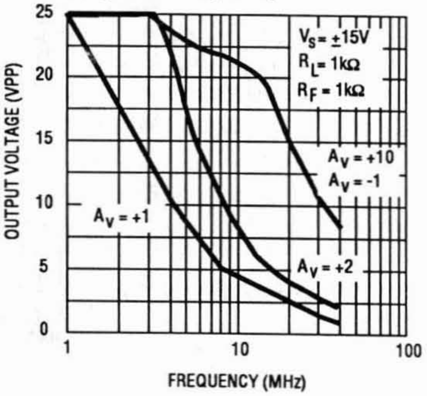
Maximum Capacitive Load vs Feedback Resistor



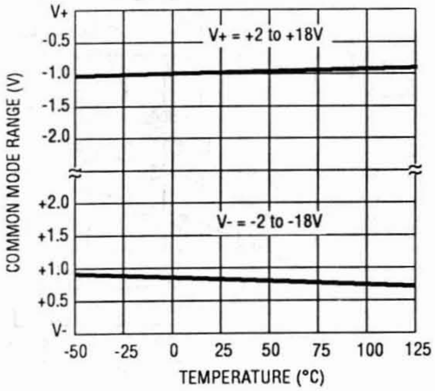
Total Harmonic Distortion vs Frequency



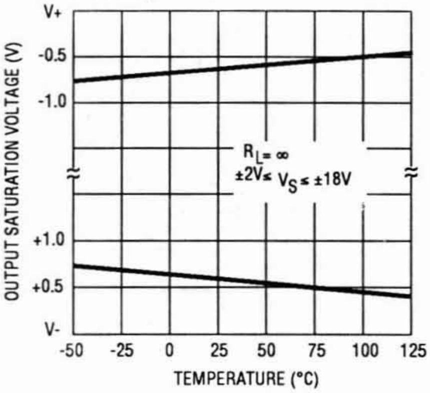
Maximum Undistorted Output vs Frequency



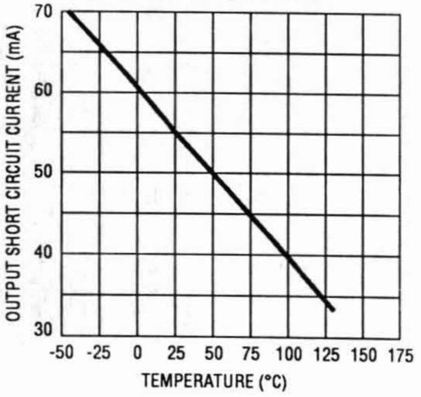
Input Common Mode Limit vs Temperature



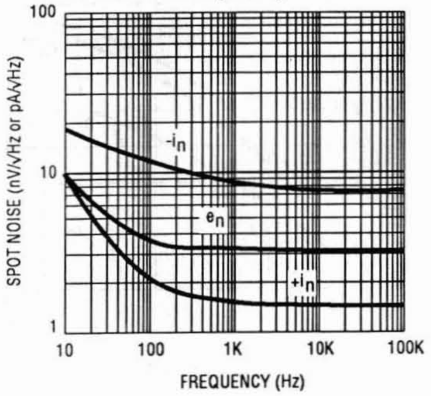
Output Saturation Voltage vs Temperature



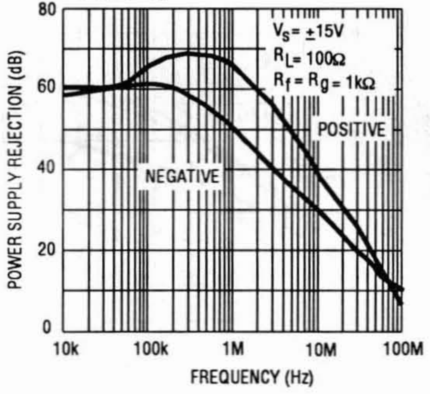
Output Short Circuit Current vs Junction Temperature



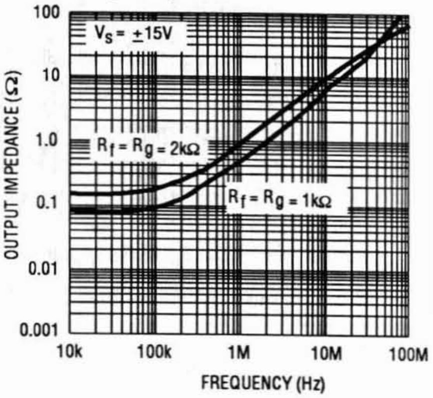
Spot Noise Voltage and Current vs Frequency



Power Supply Rejection vs Frequency

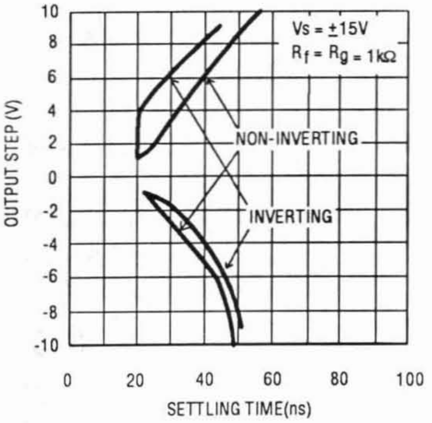


Output Impedance vs Frequency

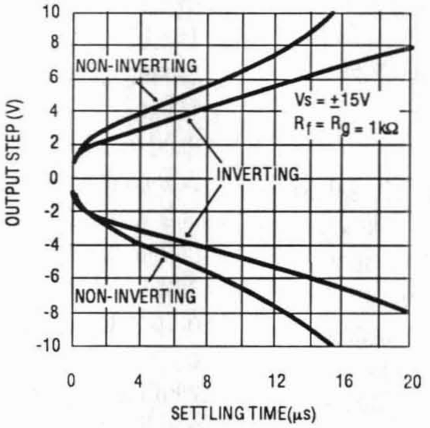


TYPICAL PERFORMANCE CHARACTERISTICS

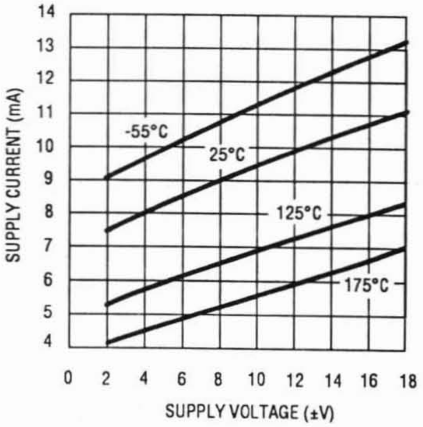
Settling Time to 10 mV vs Output Step



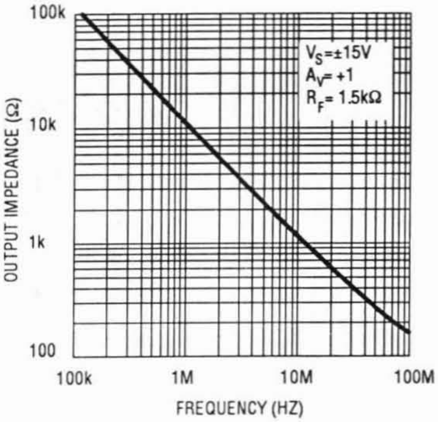
Settling Time to 1 mV vs Output Step



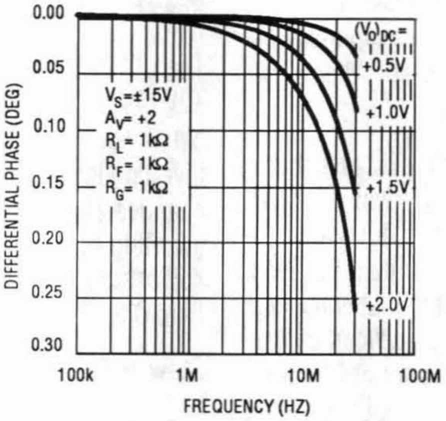
Supply Current vs Supply Voltage



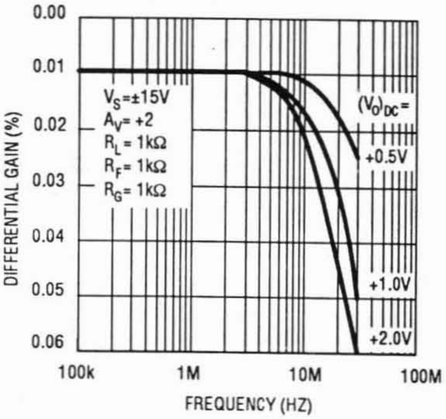
Output Impedance in Shutdown vs Frequency



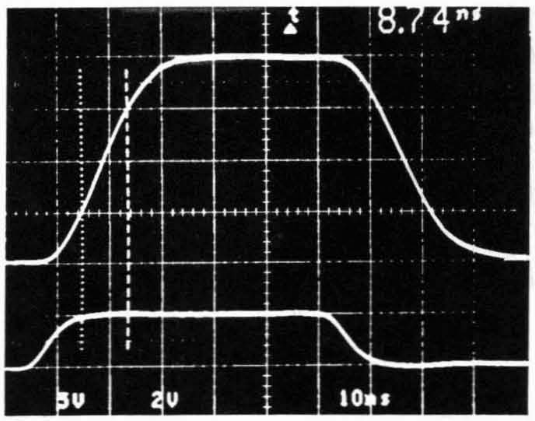
Differential Phase vs Frequency



Differential Gain vs Frequency

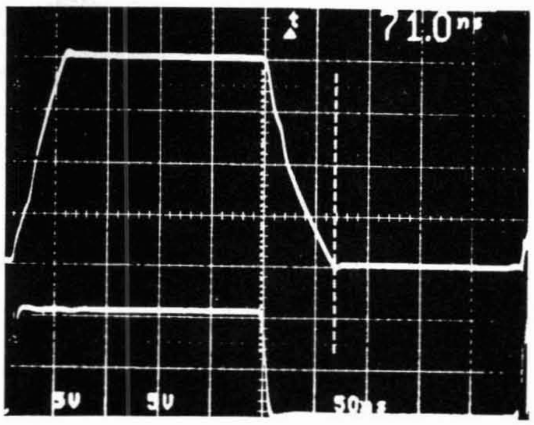


Large Signal Transient Response, A_V = +10



R_F=2kΩ, R_G=220Ω, R_L=400Ω

Large Signal Transient Response, A_V = +2



R_F=1kΩ, R_G=1kΩ, R_L=1kΩ

APPLICATIONS INFORMATION

The LT1227 is a very fast current feedback amplifier. Because it is a current feedback amplifier, the bandwidth is maintained over a wide range of voltage gains. The amplifier is designed to drive low impedance loads such as cables with excellent linearity at high frequencies.

Feedback Resistor Selection

The small signal bandwidth of the LT1227 is set by the external feedback resistors and the internal junction capacitors. As a result, the bandwidth is a function of the supply voltage, the value of the feedback resistor, the closed loop gain and load resistor. The characteristic curves of bandwidth versus supply voltage show the effect of a heavy load (100Ω) and a light load (1kΩ) . These graphs also show the family of curves that result from various values of the feedback resistor. These curves use a solid line when the response has less than 0.5dB of peaking and a dashed line when the response has 0.5 to 5dB of peaking. The curves stop where the response has more than 5dB of peaking.

At a gain of two, on ±15 volt supplies with a 1kΩ feedback resistor, the bandwidth into a light load is over 140MHz without peaking, but into a heavy load the bandwidth reduces to 120MHz. The loading has this effect because there is a mild resonance in the output stage that enhances the bandwidth at light loads but has its Q reduced by the heavy load. This enhancement is only useful at low gain settings; at a gain of ten it does not boost the bandwidth. At unity gain, the enhancement is so effective the value of the feedback resistor has very little effect. At very high closed loop gains, the bandwidth is limited by the gain bandwidth product of about 1GHz. The curves show that the bandwidth at a closed loop gain of 100 is 12MHz, only one tenth what it is at a gain of two.

Capacitance on the Inverting Input

Current feedback amplifiers require resistive feedback from the output to the inverting input for stable operation. Take care to minimize the stray capacitance between the output and the inverting input. Capacitance on the inverting input to ground will cause peaking in the frequency response (and over shoot in the transient response), but it does not degrade the stability of the amplifier.

Capacitive Loads

The LT1227 can drive capacitive loads directly when the proper value of feedback resistor is used. The graph of Maximum Capacitive Load vs Feedback Resistor should be used to select the appropriate value. The value shown is for 5dB peaking when driving a 1kΩ load at a gain of 2. This is a worst case condition, the amplifier is more stable at higher gains and driving heavier loads. Alternatively, a small resistor (10Ω to 20Ω) can be put in series with the output to isolate the capacitive load from the amplifier output. This has the advantage that the amplifier bandwidth is only reduced when the capacitive load is present and the disadvantage that the gain is a function of the load resistance.

Power Supplies

The LT1227 will operate from single or split supplies from ±2V (4V total) to ±15V (30V total). It is not necessary to use equal value split supplies, however the offset voltage and inverting input bias current will change. The offset voltage changes about 500µV per volt of supply mismatch. The inverting bias current can change as much as 5.0µA per volt of supply mismatch, though typically the change is less than 0.5µA per volt.

Slew Rate

The slew rate of a current feedback amplifier is not independent of the amplifier gain configuration the way slew rate is in a traditional op amp. This is because both the input stage and the output stage have slew rate limitations. In the inverting mode, and for higher gains in the noninverting mode, the signal amplitude between the input pins is small and the overall slew rate is that of the output stage. For gains less than ten in the noninverting mode, the overall slew rate is limited by the input stage.

The input stage slew rate of the LT1227 is approximately 125V/µs and is set by internal currents and capacitances. The output slew rate is set by the value of the feedback resistors and the internal capacitances. At a gain of ten with a 1kΩ feedback resistor and ±15V supplies, the output slew

APPLICATIONS INFORMATION

rate is typically 1100V/µs. Larger feedback resistors will reduce the slew rate as will lower supply voltages, similar to the way the bandwidth is reduced.

The graph of Maximum Undistorted Output vs. Frequency relates the slew rate limitations to sinusoidual inputs for various gain configurations.

Settling Time

The characteristic curves show that the LT1227 amplifier settles to within 10mV of final value in 40ns to 55ns for any output step up to 10V. The curve of settling to 1mV of final value shows that there is a slower thermal contribution up to 20µs. The thermal settling component comes from the output and the input stage. The output contributes just under 1mV per volt of output change and the input contributes 300µV per volt of input change. Fortunately the input thermal tends to cancel the output thermal. For this reason the non-inverting gain of two configuration settles faster than the inverting gain of one.

Shutdown

The LT1227 has a high impedance, low supply current mode which is controlled by Pin 8. In the shutdown mode, the output looks like a 12pF capacitor and the supply current drops to approximately the pin 8 current. Pulling a current of greater than 50µA from pin 8 will put the device into the shutdown mode. An easy way to force shutdown is to ground pin 8, using open drain (collector) logic.The logic should have a breakdown voltage of greater than the positive supply. No other circuitry is necessary as an internal JFET limits the pin 8 current to about 100µA. When pin 8 is open, the LT1227 operates normally.

Differential Input Signal Swing

The differential input swing is limited to about ±6V by an ESD protection device connected between the inputs. In normal operation, the differential voltage between the input pins is small,so this clamp has no effect; however, in the shutdown mode, the differential swing can be the same as the input swing. The clamp voltage will then set the maximum allowable input voltage. To allow for some margin, it is recommended that the input signal be less than ±5V when the device is shutdown.

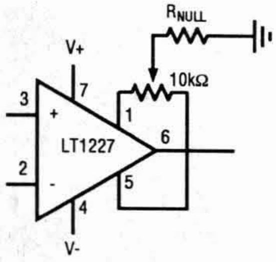
Offset Adjust

The offset adjust pins act on the inverting input bias current. A 10k pot connected to pins 1 and 5 with the wiper connected to V^+ will null out the bias current, but will not affect the offset voltage much. Since the output offset is

$$V_O \cong A_V{*}V_{OS} + (I_{IN-}){*}R_F$$

at higher gains the V_{OS} term will dominate. To null out the V_{OS} term, use a 10k pot between pins 1 and 5 with a 150kΩ resistor from the wiper to ground for 15V split supplies, 47kΩ for 5V split supplies.

Optional Offset Nulling Circuit

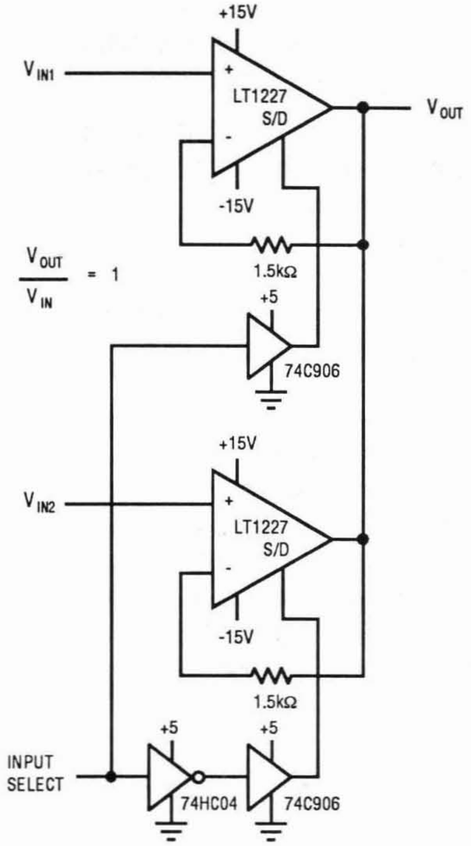


R_{NULL} = 47kΩ for V_S = ±5V
R_{NULL} = 150kΩ for V_S =±15V

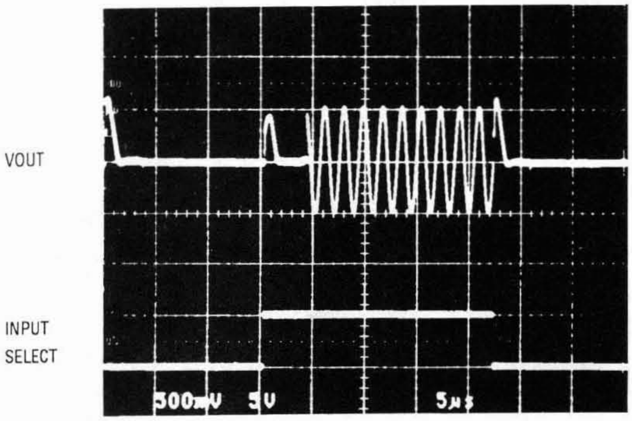
TYPICAL APPLICATIONS

Mux Amplifier

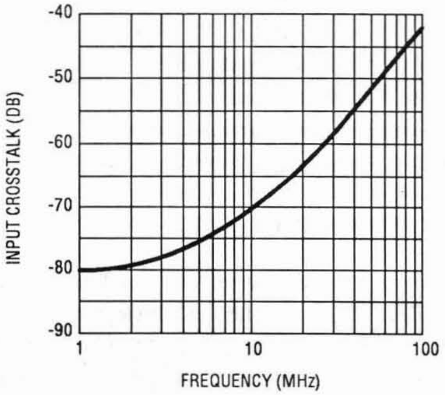
The shutdown function can be effectively used to construct a MUX amplifier. A two channel version is shown, but more inputs could be added with suitable logic. By configuring each amplifier as a unity gain follower, there is no loading by the feedback network when the amplifier is off. The open drains of the 74C906 buffers are used to interface the 5V logic to the shutdown pin. Feedthrough from the unselected input to the output is -70dB at 10MHz. The differential voltage between MUX inputs V_{IN1} and V_{IN2} appears across the inputs of the shutdown device, this voltage should be less than ±5V to avoid turning on the clamp diodes discussed previously. If the inputs are sinusoidal having a zero dc level, this implies that the amplitude of each input should be less than 5Vpp. The output impedance of the off amplifier remains high until the output level exceeds approximately 6Vpp at 10MHz, this sets the maximum usable output level. Switching time between inputs is about 4μs without an external pullup. Adding a 10k pullup resistor from each shutdown pin to V^+ will reduce the switching time to 2μs but will increase the positive supply current in shutdown by 1.5mA.



MUX Output

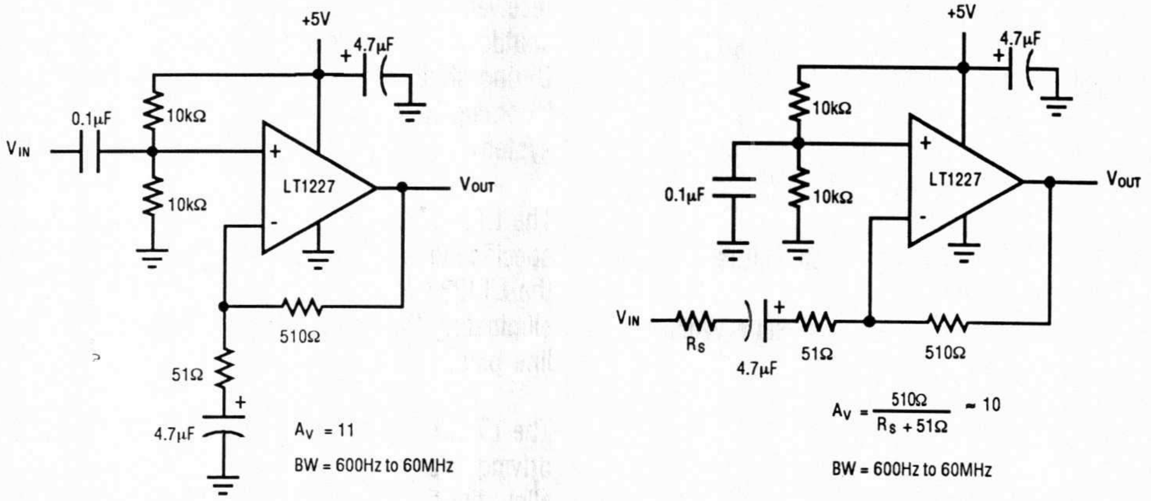


MUX Input Crosstalk vs Frequency



TYPICAL APPLICATIONS

Single Supply AC Coupled Amplifiers

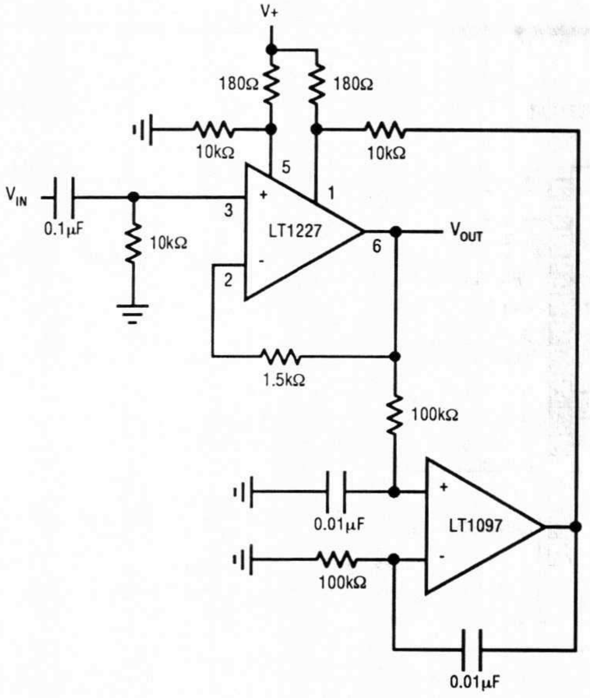


NON-INVERTING

INVERTING

+5V
4.7µF
0.1µF
10kΩ
V_{IN}
10kΩ
LT1227
V_{OUT}
510Ω
51Ω
4.7µF
$A_V = 11$
BW = 600Hz to 60MHz
+5V
4.7µF
10kΩ
LT1227
V_{OUT}
0.1µF
10kΩ
V_{IN}
R_S
4.7µF
51Ω
510Ω
$A_V = \frac{510\Omega}{R_S + 51\Omega} \approx 10$
BW = 600Hz to 60MHz

Buffer with DC Nulling Loop



V+
180Ω
180Ω
10kΩ
10kΩ
5
1
V_{IN}
0.1µF
3
10kΩ
LT1227
6
V_{OUT}
2
1.5kΩ
100kΩ
0.01µF
LT1097
100kΩ
0.01µF

PRELIMINARY

LT1237

5V RS232 Transceiver with Advanced Power Management and One Receiver Active in SHUTDOWN

June, 1992

FEATURES

- One Receiver Remains Active while in SHUTDOWN
- ESD Protection over **±10kV**
- Uses Small Capacitors (0.1μF, 0.2μF,1.0μF)
- 60μA Supply Current in SHUTDOWN
- Pin Compatible with LT1137
- Operates to 120kbaud
- CMOS Comparable Low Power 30mW
- Operates from a Single 5V Supply
- Easy PC Layout-Flow Through Architecture
- Rugged Bipolar Design
- Outputs assume a High Impedance State When Off or Powered Down
- Absolutely No Latchup
- Available in SO Package

APPLICATIONS

- Notebook Computers
- Palmtop Computers

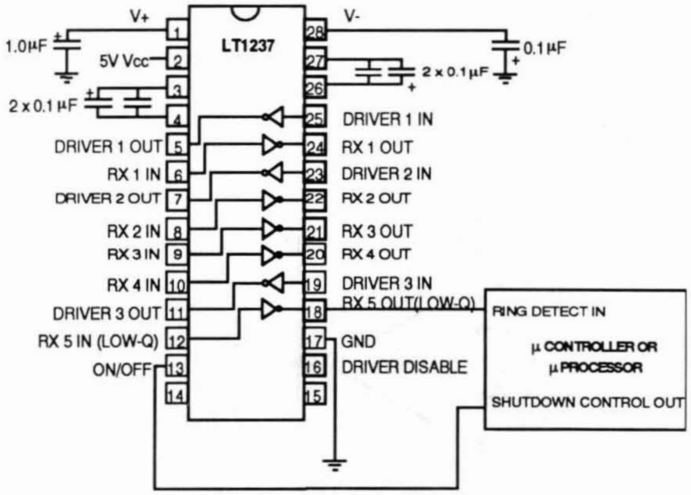
DESCRIPTION

The LT1237 is an advanced low power three driver, five receiver RS232 transceiver. Included on the chip is a shutdown pin for reducing supply current near zero. During shutdown one receiver remains active to detect incoming RS232 signals, for example, to wake up a system.

The LT1237 is fully compliant with all EIA RS232 specifications. New ESD structures on the chip allow the LT1237 to survive multiple +/-10kV strikes, eliminating the need for costly transorbs on the RS232 line pins.

The LT1237 operates in excess of 120 kilobaud even driving heavy capacitive loads. Two shutdown modes allow the driver outputs to be shut down separately from the receivers for more versatile control of the RS232 interface. During shutdown, drivers and receivers assume a high impedance state.

Typical Application

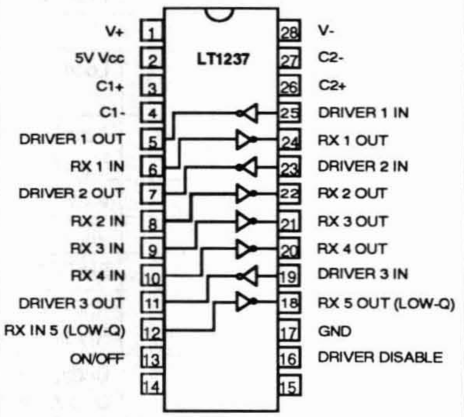

V+
1.0μF
5V Vcc
2 x 0.1 μF
LT1237
V-
0.1 μF
2 x 0.1 μF
DRIVER 1 OUT
RX 1 IN
DRIVER 2 OUT
RX 2 IN
RX 3 IN
RX 4 IN
DRIVER 3 OUT
RX 5 IN (LOW-Q)
ON/OFF
DRIVER 1 IN
RX 1 OUT
DRIVER 2 IN
RX 2 OUT
RX 3 OUT
RX 4 OUT
DRIVER 3 IN
RX 5 OUT(LOW-Q)
GND
DRIVER DISABLE
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
RING DETECT IN
μ CONTROLLER OR
μ PROCESSOR
SHUTDOWN CONTROL OUT

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC})	6V
V+	+13.2V
V-	-13.2V
Input Voltage	
Driver	V+ to V-
Receiver	+30V to -30V
Output Voltage	
Driver	-55°C to 125°C
Receiver	0°C to 70°C
Short Circuit Duration	
V+	30s
V-	30s
Driver Output	Indefinite
Receiver Output	Indefinite
Operating Temperature Range	
LT1237I	-40°C to 85°C
LT1237C	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION


LT1237
V+ 1
5V Vcc 2
C1+ 3
C1- 4
DRIVER 1 OUT 5
RX 1 IN 6
DRIVER 2 OUT 7
RX 2 IN 8
RX 3 IN 9
RX 4 IN 10
DRIVER 3 OUT 11
RX IN 5 (LOW-Q) 12
ON/OFF 13
14
28 V-
27 C2-
26 C2+
25 DRIVER 1 IN
24 RX 1 OUT
23 DRIVER 2 IN
22 RX 2 OUT
21 RX 3 OUT
20 RX 4 OUT
19 DRIVER 3 IN
18 RX 5 OUT (LOW-Q)
17 GND
16 DRIVER DISABLE
15

ORDER PART NUMBER
LT1237IJ LT1237CJ LT1237CN LT1237CS

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V+ Output				8.6		V
V- Output				- 7.0		V
Supply Current (V_{CC})	(Note 3)			6	9	mA
Supply Current when OFF (V_{CC})	SHUTDOWN (Note 4) DRIVER DISABLE	●		0.06 3	0.150	mA mA
Supply Rise Time SHUTDOWN to Turn On	C1=C2=0.2μF, C+=1.0μF, C- = 0.1μF			2		ms
ON/OFF Pin Thresholds	Input Low Level (Device SHUTDOWN)	●		1.4	0.8	V
	Input High Level (Device Enabled)	●	2.0	1.4		V
ON/OFF Pin Current	0V $\le V_{ON/OFF} \le$ 5V	●	- 15		80	μA
Driver Disable Pin Thresholds	Input Low Level (Drivers Enabled)	●		1.4	0.8	V
	Input High Level (Drivers Disabled)	●	2.0	1.4		V
DRIVER DISABLE Pin Current	0V $\le V_{DRIVER\ DISABLE} \le$ 5V	●	- 10		500	μA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	Load = 3k to GND	Positive	●	5.0	7.3		V
		Negative	●	- 5.0	- 6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT}=High)		●		1.4	0.8	V
	Input High Level (V_{OUT}=Low)		●	2.0	1.4		V
Logic Input Current	$0.8V \le V_{IN} \le 2.0V$		●		5	20	μA
Output Short Circuit Current	$V_{OUT} = 0V$				17		mA
Output Leakage Current	SHUTDOWN $V_{OUT} = \pm 30V$ (Note 4)		●		10	100	μA
Slew Rate	R_L=3k, C_L=51pF				15	30	V/μs
	R_L=3k, C_L=2500pF			4	15		V/μs
Propagation Delay	Output Transition t_{HL} High to Low (Note 5)				0.6	1.3	μS
	Output Transition t_{LH} Low to High				0.5	1.3	μS
Any Receiver							
Input Voltage Thresholds	Input Low Threshold (V_{OUT} = High)			0.8	1.3		V
	Input High Threshold (V_{OUT} = Low)				1.7	2.4	V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance				3	5	7	kΩ
Ouput Leakage Current	SHUTDOWN (Note) $0 \le V_{OUT} \le V_{CC}$		●		1	10	μA
Receivers 1 Through 4							
Output Voltage	Output Low, I_{OUT} = -1.6mA		●		0.2	0.4	V
	Output High, I_{OUT} = 160μA (V_{CC}=5V)		●	3.5	4.2		V
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			- 10	- 20		mA
	Sourcing Current, V_{OUT} = 0V			10	20		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)				250	600	nS
	Output Transition t_{LH} Low to High				350	600	nS
Receiver 5 (LOW-I_{SUPPLY} RX)							
Output Voltage	Output Low, I_{OUT} = -500μA		●		0.2	0.4	V
	Output High, I_{OUT} = 160μA (V_{CC} = 5V)		●	3.5	4.2		V
Output Short Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			- 2	- 4		mA
	Sourcing Current, V_{OUT} = 0V			2	4		mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 6)				1.0	3	μS
	Output Transition t_{LH} Low to High				1.0	3	μS

The ● denotes specifications which apply over the operating temperature range. (0°C $\le T_A \le$ 70°C for commercial grade, -40°C $\le T_A \le$ 85°C for industrial grade, and -55°C $\le T_A \le$ 125°C for military grade.)

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/OFF}$=3V.

Note 3: Supply current is measured as the average over several charge pump burst cycles. C+=1.0μF, C-=0.1μF, C1=C2=0.2μF. All outputs are open, with all driver inputs tied high.

Note 4: Supply current measurements in SHUTDOWN are performed with $V_{ON/OFF} \le 0.1V$. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE} \ge 3V$.

Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing. (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V)

Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold. (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V)

PIN FUNCTIONS

V_{CC}: +5V Input supply pin. This pin should be decoupled with a 0.1uF ceramic capacitor.

GND: Ground Pin.

On/Off: TTL/CMOS compatible operating mode control. A logic low puts the device in the low power SHUTDOWN mode. Which places all of the drivers and four receivers in a high impedance state. A logic high fully enables the transceiver.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all drivers in a high impedance state. All receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic low level fully enables the transceiver.

V+: Positive supply output (RS232 drivers). $V+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 1.0\mu F$, tied to ground or +5V. Larger value capacitors may be used to reduce supply ripple. The ratio of the capacitors on V+ and V- should be greater than 5 to 1.

V-: Negative supply output (RS232 drivers). $V- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. To reduce supply ripple, increase the size of the storage capacitor.

C1+;C1-;C2+;C2-: Commutating capacitor inputs, require two external capacitors $C \geq 0.2\mu F$. One from C1+ to C1-, and another from C2+ to C2-. The capacitor's effective series resistance should be less than 2Ω. For $C \geq 1\mu F$, low ESR tantalum capacitors work well in this application, although small value ceramic capacitors may be used with a minimal reduction in charge pump compliance.

DRIVER IN: RS232 driver input pins. These inputs are TTL/ CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to Vcc.

DRIVER OUT: Driver outputs at RS232 voltage levels. Outputs are in a high impedance state when in SHUTDOWN mode, $V_{CC} = 0V$, or when the driver disable pin is active. Outputs are fully short circuit protected from V- + 30V to V+ - 30V. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

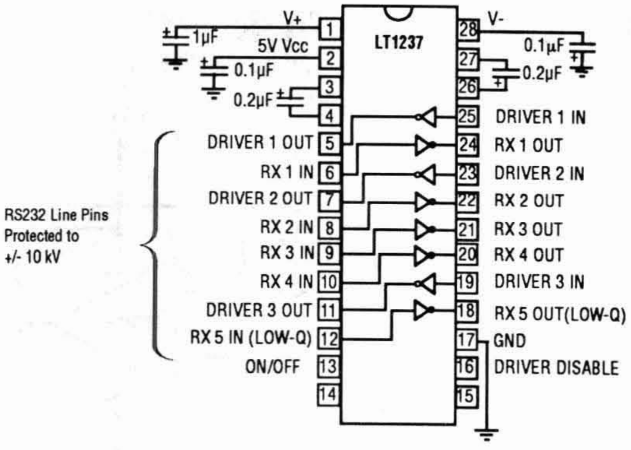
RX IN: Receiver inputs. These pins accept RS232 level signals (±30V) into a protected 5kΩ terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance stage when in SHUTDOWN mode to allow data line sharing. Outputs, including LOW-Q RXOUT, are fully short circuit protected to ground or V_{CC} with the power on, off, or in SHUTDOWN mode.

LOW Q-CURRENT RX IN: Low power receiver input. This special receiver remains active when the part is in SHUTDOWN mode, consuming typically 60μA. This receiver has the same input and protection characteristics as the other receivers.

LOW Q-CURRENT RX OUT: Low power receiver output. This pin produces the same TTL/CMOS output voltage levels with slightly decreased speed and short circuit current.

ESD Test Circuit



PRELIMINARY

LTC1250

Very Low Noise Zero-Drift Bridge Amplifier

March 1992

FEATURES

- Very low noise: 0.75µVp-p typ, 0.1Hz to 10 Hz
- DC to 1Hz noise lower than OP-07
- Full output swing into 1K load
- Maximum offset voltage 10µV
- Maximum offset voltage drift 50nV/°C
- Minimum CMRR, 115dB
- Minimum PSRR, 120dB
- No external components required
- Pin compatible with standard 8-pin op amps

APPLICATIONS

- Electronic scales
- Strain gauge amplifiers
- Thermocouple amplifiers
- High resolution data acquisition
- Low noise transducers
- Instrumentation amplifiers

DESCRIPTION

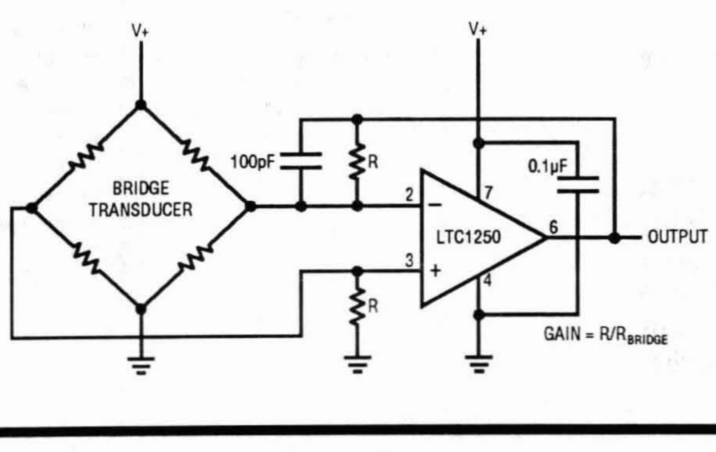
The LTC1250 is a high performance, very low noise zero-drift operational amplifier. The LTC1250's combination of low front end noise and DC precision makes it ideal for use with low-impedance bridge transducers. The LTC1250 features typical input noise of 0.75µVp-p from 0.1Hz to 10Hz, and 0.2µVp-p from 0.1Hz to 1Hz. The LTC1250 has DC to 1Hz noise of 0.35µVp-p, surpassing that of low-noise bipolar parts including the OP-07, OP-77, and LT1012. The LTC1250 uses the industry standard single op amp pinout, and requires no external components or nulling signals, allowing it to be a plug-in replacement for bipolar op amps.

The LTC1250 incorporates an improved output stage capable of driving +4.3V into a 1KΩ load with a single 5V supply; it will swing ±4.9V into 5K with ±5V supplies. The input common mode range includes ground with single power supply voltages above 12V. Supply current is 3mA with a ±5V supply; overload recovery times from positive and negative saturation are 0.5ms and 1.5ms, respectively. The internal nulling clock is set at 5kHz for optimum low-frequency noise and offset drift; no external connections are necessary.

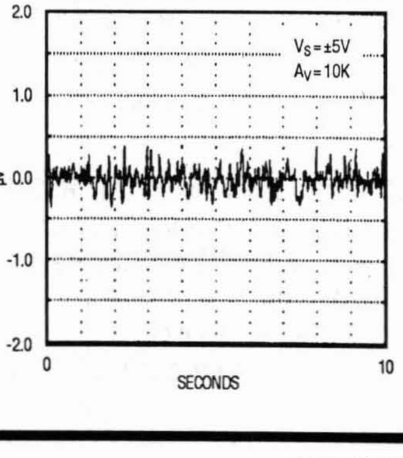
The LTC1250 is available in standard 8-pin ceramic and plastic DIPs, as well as an 8-pin SOIC package.

TYPICAL APPLICATION

Differential Bridge Amplifier



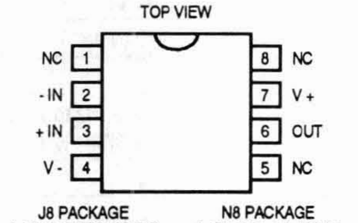
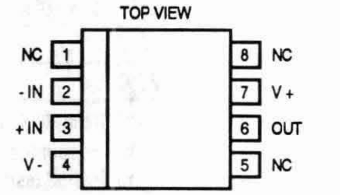
Input Referred Noise 0.1Hz-10Hz



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 18V
Input Voltage .... (V+ + 0.3V) to (V- - 0.3V)
Output Short Circuit Duration .... Indefinite
Operating Temperature Range
  LTC1250M .... -55°C to 125°C
  LTC1250C .... 0°C to 70°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER
 TOP VIEW NC 1 -IN 2 +IN 3 V- 4 8 NC 7 V+ 6 OUT 5 NC J8 PACKAGE 8-LEAD CERAMIC DIP N8 PACKAGE 8-LEAD PLASTIC DIP	LTC1250MJ8 LTC1250CJ8 LTC1250CN8
 TOP VIEW NC 1 -IN 2 +IN 3 V- 4 8 NC 7 V+ 6 OUT 5 NC S8 PACKAGE 8-LEAD PLASTIC SOIC	LTC1250CS8

ELECTRICAL CHARACTERISTICS $V_S = \pm 5V$, T_A = operating temperature range unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS		LTC1250M			LTC1250C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$T_A = 25°C$ (Note 1)			± 5	± 10		± 5	± 10	µV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●		± 0.01	± 0.05		± 0.01	± 0.05	µV/°C
	Long Term Offset Drift				50			50		$nV/\sqrt{Mo}$
e_N	Input Noise Voltage (Note 2)	$T_A = 25°C$, 0.1Hz to 10Hz $T_A = 25°C$, 0.1Hz to 1Hz			0.75 0.22	0.9 0.3		0.75 0.22	0.9 0.3	μV_{p-p} μV_{p-p}
i_N	Input Noise Current	f = 10Hz			4.0			4.0		$fA/\sqrt{Hz}$
I_B	Input Bias Current	$T_A = 25°C$			± 50	± 150		± 50	± 200	pA
			●			± 950			± 450	pA
I_{OS}	Input Offset Current	$T_A = 25°C$			± 100	± 150		± 100	± 200	pA
			●			± 200			± 300	pA
CMRR	Common Mode Rejection Ratio	$V_{CM} = -4V$ to $+3V$, $T_A = 25°C$		115	130		115	130		dB
			●	110			110			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to $\pm 8V$	●	120	130		120	130		dB
A_{VOL}	Large Signal Voltage Gain	$R_L = 10K$, $V_{OUT} = \pm 4V$	●	135	170		140	170		dB
	Maximum Output Voltage Swing	$R_L = 1K$	●	+ 4.0/-4.5	+ 4.3/-4.7		+ 4.0/-4.5	+ 4.3/-4.7		V
		$R_L = 100K$			± 4.95			± 4.95		V
SR	Slew Rate	$R_L = 10K$, $C_L = 50pF$			10			10		V/µs
GBW	Gain-Bandwidth Product				1.5			1.5		MHz
I_S	Supply Current	No Load, $T_A = 25°C$			3.0	4.0		3.0	4.0	mA
			●			5.5			5.0	mA
f_S	Internal Sampling Frequency	$T_A = 25°C$			4.75			4.75		kHz

ELECTRICAL CHARACTERISTICS V_S = +5V, -0V, T_A = operating temperature range unless otherwise specfied.

SYMBOL	PARAMETER	CONDITIONS		LTC1250M MIN	LTC1250M TYP	LTC1250M MAX	LTC1250C MIN	LTC1250C TYP	LTC1250C MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 1)			± 2	± 5		± 2	± 5	µV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●		± 0.01	± 0.05		± 0.01	± 0.05	µV/°C
e_N	Input Noise Voltage (Note 2)	T_A = 25°C, 0.1Hz to 10Hz T_A = 25°C, 0.1Hz to 1Hz			1.0 0.3			1.0 0.3		µVp-p µVp-p
I_B	Input Bias Current	T_A = 25°C			± 20	± 100		± 20	± 100	pA
I_{OS}	Input Offset Current	T_A = 25°C			± 40	± 120		± 40	± 120	pA
	Maximum Output Voltage Swing	T_A = 25°C, R_L = 1k T_A = 25°C, R_L = 100k		4.0	4.3 4.95		4.0	4.3 4.95		V V
I_S	Supply Current	T_A = 25°C			1.8	2.5		1.8	2.5	mA
f_S	Sampling Frequency	T_A = 25°C			3			3		kHz

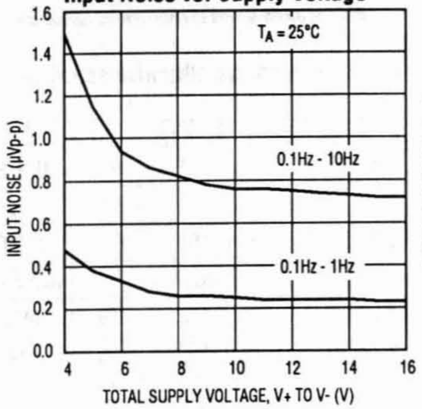
The ● denotes specs which apply over the full operating temperature range.

Note 1: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels during automated testing.

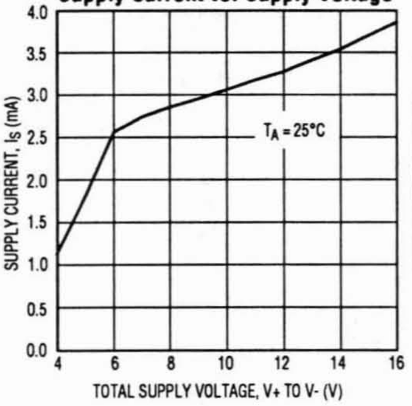
Note 2: 0.1 to 10Hz noise is specified DC coupled in a 10s window; 0.1 to 1Hz noise is specified in a 100s window with a RC highpass at 0.1Hz. The LTC1250 is sample tested for noise; for 100% tested parts contact LTC marketing.

TYPICAL PERFORMANCE CHARACTERISTICS

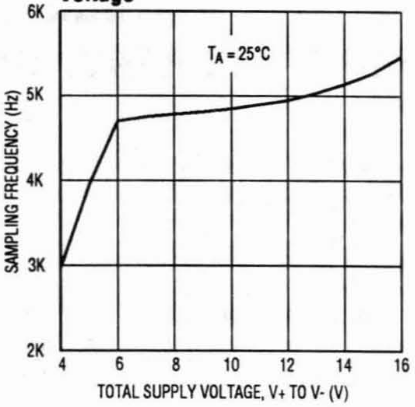
Input Noise vs. Supply Voltage



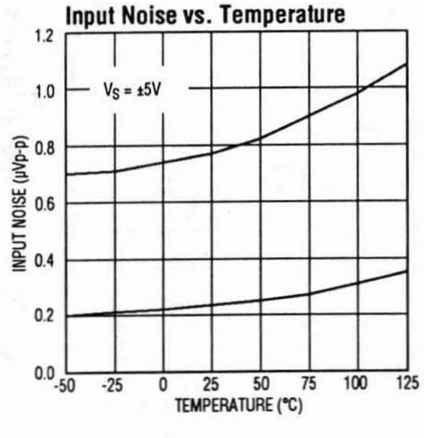
Supply Current vs. Supply Voltage



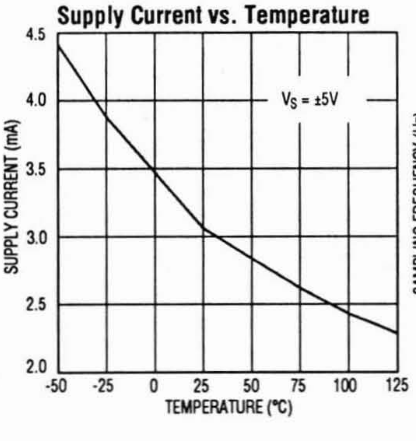
Sampling Frequency vs. Supply Voltage



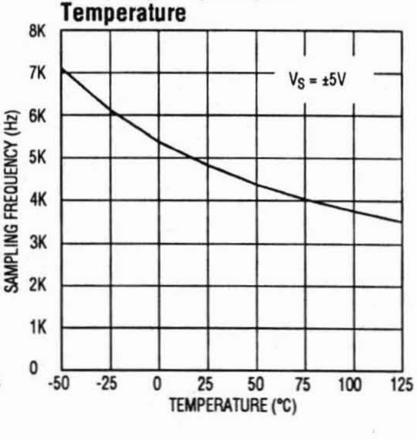
Input Noise vs. Temperature



Supply Current vs. Temperature

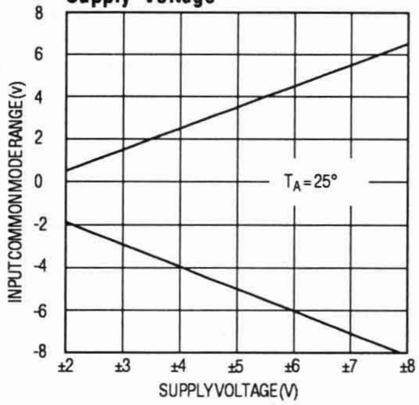


Sampling Frequency vs. Temperature

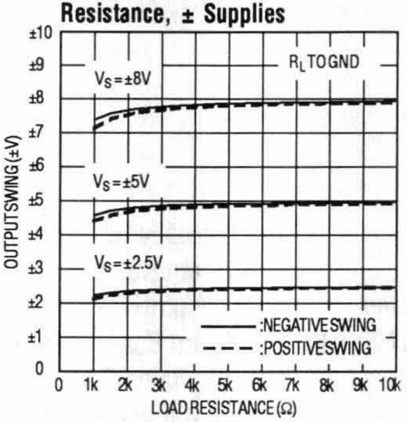


TYPICAL PERFORMANCE CHARACTERISTICS

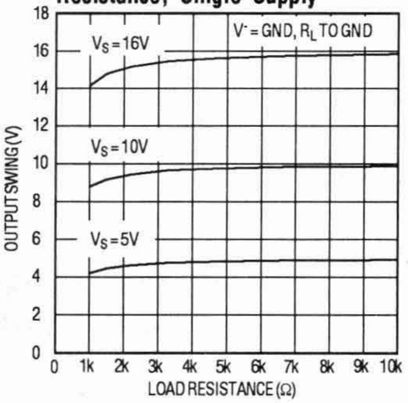
Common Mode Input Range vs. Supply Voltage



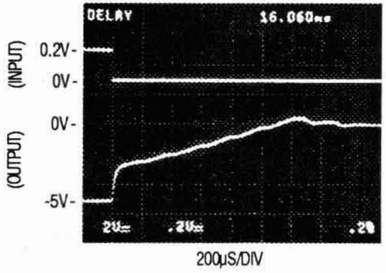
Output Voltage Swing vs. Load Resistance, ± Supplies



Output Voltage Swing vs. Load Resistance, Single Supply

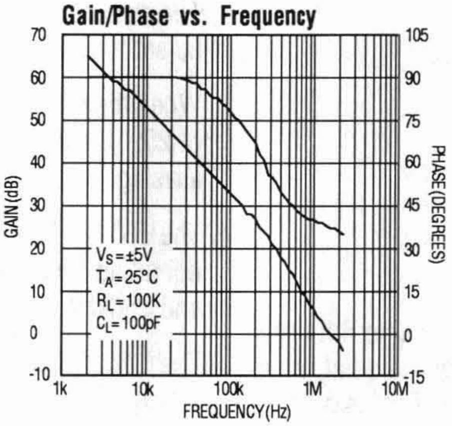


Overload Recovery

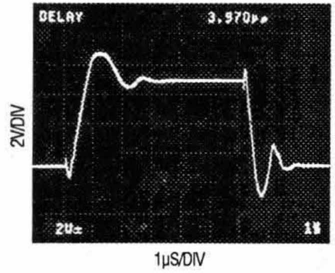


$A_V = -100$ $R_L = 100K$ $C_L = 50pF$ $V_S = ±5V$

Gain/Phase vs. Frequency



Transient Response



$A_V = +1$ $R_L = 100K$ $C_L = 50pF$ $V_S = ±5V$

APPLICATIONS INFORMATION

Input Characteristics

The LTC1250 uses large geometry front end transistors to reduce intrinsic noise and a high-speed zero-drift nulling loop to nearly eliminate 1/f noise. The resultant noise spectrum is low, and is flat below 10Hz, giving the LTC1250 a substantial noise advantage over conventional op amps at very low frequencies.

The large input transistors have an input capacitance of 60pF; this capacitance reacts with the feedback resistor network to form a pole, degrading the amplifier's phase margin. The solution is a 100pF feedback capacitor in parallel with the feedback resistor, providing a corresponding input zero to eliminate the problem. **Nearly all LTC1250 applications will require this capacitor.** For additional information, see the LTC1051 datasheet.

Output Drive

The LTC1250 includes an enhanced output stage which provides nearly symmetrical output source/sink currents. This output is capable of swinging ±4V into a 1K load with ±5V supplies, and can sink or source >20mA into low impedance loads. Into lighter loads, the LTC1250 will swing rail-to-rail, maximizing output dynamic range.

PRELIMINARY

LTC1264-7

Linear Phase, Group Delay Equalized, 8th Order Low Pass Filter

MAY 1992

FEATURES

- Steeper rolloff than Bessel filters
- High speed (fc ≤ 250kHz)
- Phase and Group Delay response fully tested
- Transient response exhibits 5% overshoot and no ringing
- No external components needed

APPLICATIONS

- Data communication filters
- Time delay networks
- Phase matched filters

DESCRIPTION

The LTC1264-7 is a clock tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband and exhibits steeper rolloff than an equivalent 8th order Bessel filter. For instance at twice the cutoff frequency the filter attains 28dB attenuation (12dB for Bessel), while at 3 times the cutoff frequency the filter attains 55dB attenuation (30dB for Bessel). The cutoff frequency of the LTC1264 is tuned via an external TTL or CMOS clock.

The clock to cutoff frequency ratio of the LTC1264-7 can be set to 25:1 (pin 10 to V+) or 50:1 (pin 10 to V-).

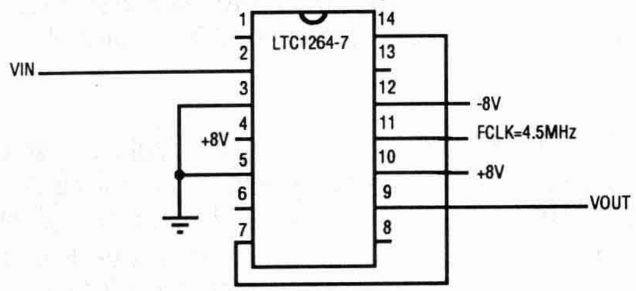
When the filter operates at clock to cutoff frequency ratio of 25:1 the input is double sampled to lower the risk of aliasing.

The LTC1264-7 is optimized for speed. Depending on the operating conditions, cutoff frequencies between 200kHz and 250kHz can be obtained.

The LTC1264-7 is pin compatible with the LTC1064-X series.

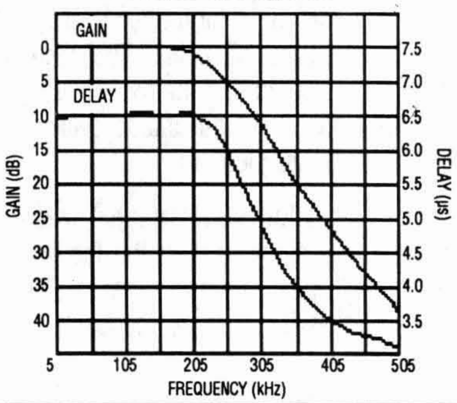
TYPICAL APPLICATION

200kHz Linear Phase Low pass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1μF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE FCLK LINE.

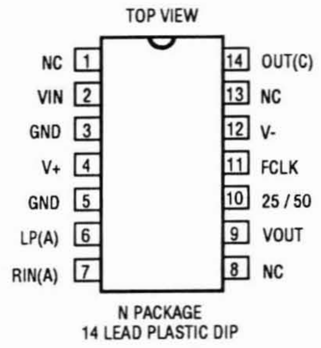
Frequency Response



ABSOLUTE MAXIMUM RATINGS

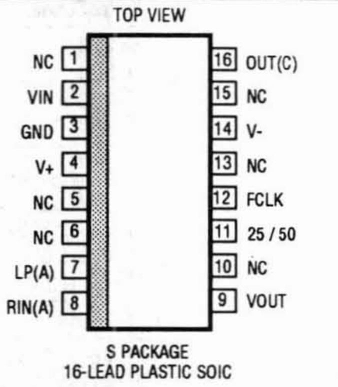
Total Supply Voltage (V+ to V-) 16V
Power Dissipation 400mW
Storage Temperature Range .... −65°C to 150°C
Burn-in Voltage 16V
Operating Temperature Range .... -40°C to 85°C
Voltage at Any Input ...... $[V^- - 0.3V] \le V_{IN} \le [V^+ + 0.3V]$

PACKAGE/ORDER INFORMATION


TOP VIEW
NC 1
VIN 2
GND 3
V+ 4
GND 5
LP(A) 6
RIN(A) 7
14 OUT(C)
13 NC
12 V-
11 FCLK
10 25 / 50
9 VOUT
8 NC

N PACKAGE
14 LEAD PLASTIC DIP

ORDER PART NUMBER
LTC1264-7CN LTC1264-7CJ LTC1264-7MJ


TOP VIEW
NC 1
VIN 2
GND 3
V+ 4
NC 5
NC 6
LP(A) 7
RIN(A) 8
16 OUT(C)
15 NC
14 V-
13 NC
12 FCLK
11 25 / 50
10 NC
9 VOUT

S PACKAGE
16-LEAD PLASTIC SOIC

ORDER PART NUMBER
LTC1264-7CS

ELECTRICAL CHARACTERISTICS

V_S=±7.5Volts, R_{LOAD}=10k, T_A=25°C, fclk=2.5MHz, TTL or CMOS Level and all Gain measurements are referenced to passband Gain unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	0.1Hz ≤ f ≤ 0.25 fcutoff					
	ftest=25kHz (25:1)	●	-0.50	-0.10	0.50	dB
Gain at 0.5 fcutoff	ftest=50kHz (25:1)	●	-0.50		0.20	dB
	ftest=25kHz (50:1)	●	-0.65	-0.15	0.30	dB
Gain at 0.75 fcutoff	ftest=75kHz (25:1)	●	-1.5	-1.00	0.1	dB
Gain at fcutoff	ftest=100kHz(25:1)	●	-3.7	-3.00	-1.9	dB
	ftest=50kHz (50:1)	●	-4.5	-3.00	-2.3	dB
Gain at 2.0 • fcutoff	ftest=200kHz(25:1)	●	-34	-28	-20	dB
	ftest=100kHz(50:1)	●	-34	-30	-27	dB
Gain with fclk=20kHz	ftest=200Hz (50:1)		-0.7	-0.30	0.1	dB
Gain with fclk=400kHz, V_S=±2.375V	ftest=8kHz (25:1)		-0.2	0.15	0.5	dB
	ftest=16kHz (25:1)		-3.5	-2.70	-1.4	dB
Gain with fclk=4MHz	ftest=160kHz, Vin=1V_{RMS}					
	25:1, T_A = 0 - 70°C			0.00±1.0		dB
	25:1	●			3.0	dB
Phase Factor (F) Phase = 180° - F (f / fc) (Note 1)	(0.1Hz ≤ f ≤ fcutoff)					
	25:1			407±2		deg
	50:1			388±2		deg
	25:1	●	392		423	deg
	50:1	●	374		414	deg
Phase Deviation from Linear Phase (Note 1)	25:1			±1.0		%
	50:1			±1.0		%
	25:1	●			±2.0	%
	50:1	●			±2.0	%

ELECTRICAL CHARACTERISTICS

V_S=±7.5Volts, R_{LOAD}=10k, T_A=25°C, fclk=2.5MHz, TTL or CMOS Level and all Gain measurements are referenced to passband Gain unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Group Delay (TD)	fc=100kHz (25:1)			11.3		µs
TD = (1 / 360) (F / fc)	fc=50kHz (50:1)			21.6		µs
(Note 2)	fc=100kHz (25:1)	●	10.9		11.7	µs
	fc=50kHz (50:1)	●	20.8		22.9	µs
Group Delay Deviation	25:1			±1.0		%
(Note 2)	50:1			±1.0		%
	25:1	●			±2.0	%
	50:1	●			±2.0	%
Input Frequency Range	25:1			<fclk		kHz
	50:1			<fclk/2		kHz
Maximum fclk	V_S=±2.375V			1		MHz
	V_S=±5.0V			3		MHz
	V_S=±7.5V			5		MHz
Clock Feedthrough (f ≥ fclk)	25:1			200		μV_{RMS}
Wideband Noise (1Hz ≤ f ≤ fclk)	V_S=±2.375V			155±5%		μV_{RMS}
	V_S=±5.0V			180±5%		μV_{RMS}
	V_S=±7.5V			205±5%		μV_{RMS}
Input Impedance			30	50	75	kΩ
Output DC Voltage Swing	Vs=±2.375V			±1.0		Volts
	Vs=±5.0V	●		±2.3	±2.0	Volts
	Vs=±7.5V	●		±3.8	±3.0	Volts
Output DC Offset	25:1, Vs=±5.0V			±100	±220	mV
	50:1, Vs=±5.0V			±100	±220	mV
Output DC Offset TempCo	25:1, Vs=±5.0V			±200		µV/°C
	50:1, Vs=±5.0V			±200		µV/°C
Power Supply Current	V_S=±2.375V			11		mA
(fclk = 1MHz)		●			22	mA
	V_S=±5.0V			14		mA
		●			26	mA
	V_S=±7.5V			17		mA
		●			32	mA
Power Supply Range			±2.375		±8	V

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Input frequencies, f, are linearly phase shifted through the filter as long as f ≤ fc; fc = cutoff frequency.

Figure 1 curve (A) shows the typical phase response of an LTC1264-7 operating at fclk = 2.5MHz, fc = 100kHz. An endpoint straight line, curve (B), depicts the ideal linear phase response of the filter. It is described by:

$$\text{phase shift} = 180° - F\ (f / fc)\ ;\ f \leq fc \qquad (1)$$

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor together with the specified deviation from the ideal straight line allows the calculation of the phase at a given frequency . Note, the maximum phase non linearity, figure 1, occurs at the vicinity of f = 0.25 fc, and = 0.75 fc.

Example: The phase shift at 70kHz of the LTC1264-7 shown in figure 1 is:

$$\text{phase shift} = 180° - 407°\ (70\text{kHz} / 100\text{kHz}) \pm \text{non linearity}$$
$$= -104.9° \pm 0.7\% \quad \text{or} \quad -104.9° \pm .73°$$

Note 2: Group Delay and Group Delay Deviation are calculated from the measured Phase Factor and Phase Deviation specifications.

PHASE RESPONSE IN THE PASSBAND
LTC1264-7, FCLK=2.5MHz, RATIO=25:1

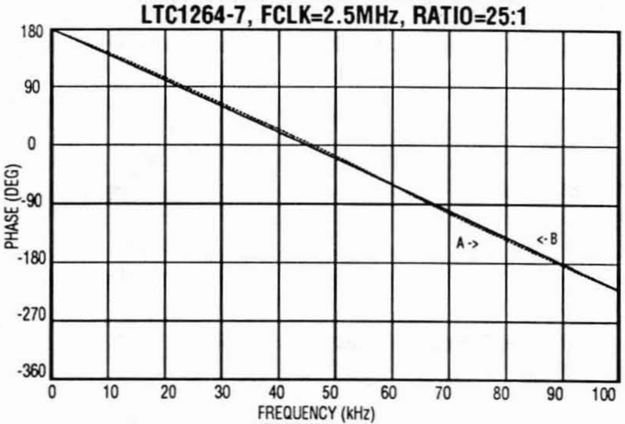
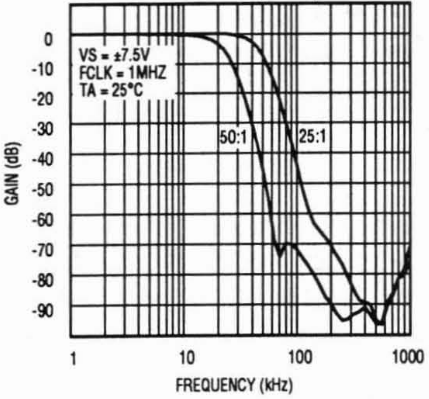
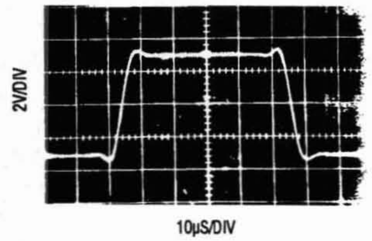


FIGURE (1)

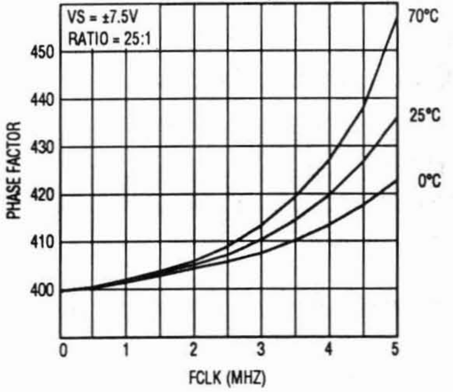
Gain vs Frequency



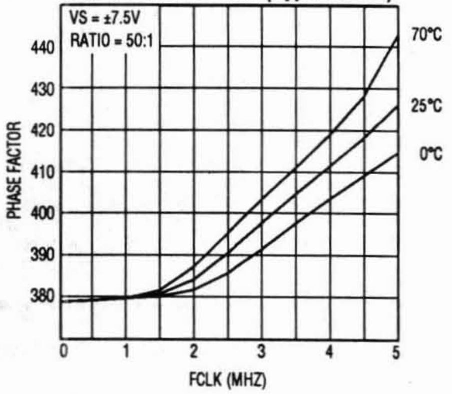
Transient Response
Input = 10kHz, ±3V, fclk = 2.5MHz



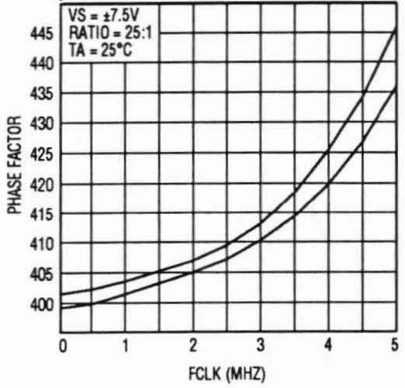
Phase Factor vs Fclk (Typical Unit)



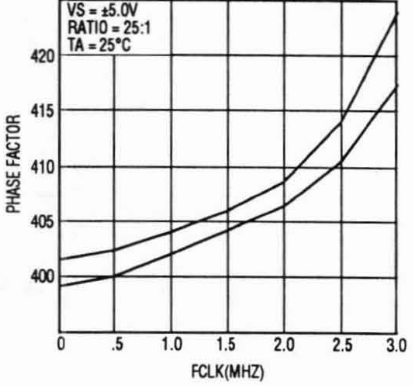
Phase Factor vs Fclk (Typical Unit)



Phase Factor vs Fclk
(Min and Max Representative Units)



Phase Factor vs Fclk
(Min and Max Representative Units)



PRELIMINARY

LT1271

4A High Efficiency Switching Regulator

August 1991

FEATURES

- Wide Input Voltage Range 3.5V-30V
- Low Quiescent Current — 7mA
- Internal 4A Switch
- Very Few External Parts Required
- Self Protected Against Overloads
- Shutdown Mode Draws Only 100µA Supply Current
- Flyback Regulated Mode Has Fully Floating Outputs
- Comes in Standard 5-Pin Package
- Can Be Externally Synchronized (See LT1072 Data Sheet)

APPLICATIONS

- Boost Converter
- High Efficiency Buck Converter
- PC Power Supply with Multiple Outputs
- Battery Upconverter
- Negative to Positive Converter

USER NOTE:

This data sheet is only intended to provide specifications, graphs, and a general functional description of the LT1271. Application circuits are included to show the capability of the LT1271. A complete design manual (AN-19) should be obtained to assist in developing new designs. This manual contains a comprehensive discussion of both the LT1070 and the external components used with it, as well as complete formulas for calculating the values of these components. The manual can also be used for the LT1271 by factoring in the higher switch current rating and higher operating frequency.

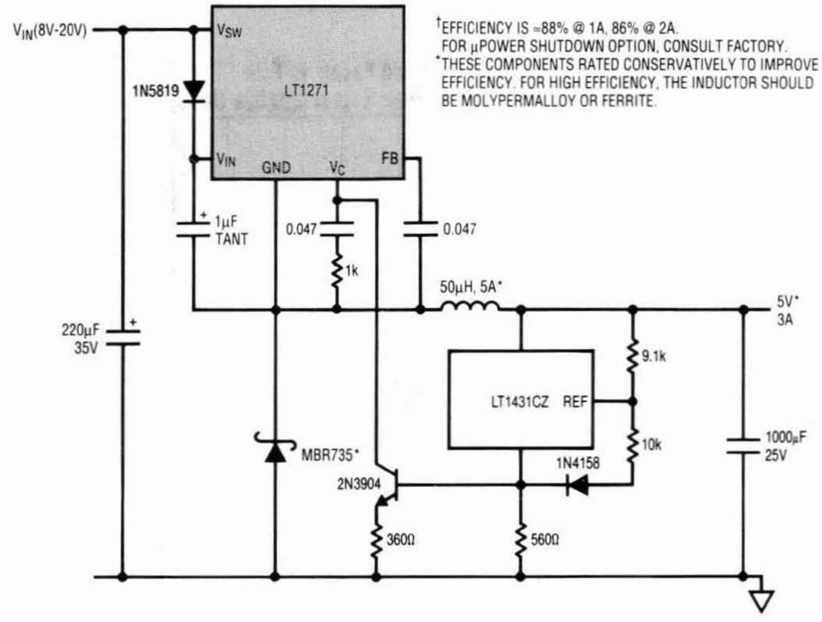
DESCRIPTION

The LT1271 is a monolithic high power switching regulator. Identical to the popular LT1070, except for switching frequency (60kHz) and slightly lower switch current, it can be operated in all standard switching configurations including buck, boost, flyback, and inverting. A high current, high efficiency switch is included on the die along with all oscillator, control, and protection circuitry. Integration of all functions allows the LT1271 to be built in a standard TO-220 power package. This makes it extremely easy to use and provides "bust proof" operation similar to that obtained with 3-pin linear regulators.

The LT1271 operates with supply voltages from 3.5V to 30V, and draws only 7mA quiescent current. By utilizing current mode switching techniques, it provides excellent AC and DC load and line regulation.

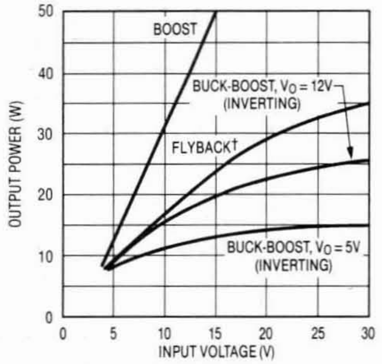
The LT1271 uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 100µA typical for standby operation.

High Efficiency† Buck Converter



†EFFICIENCY IS ≈88% @ 1A, 86% @ 2A.
FOR µPOWER SHUTDOWN OPTION, CONSULT FACTORY.
*THESE COMPONENTS RATED CONSERVATIVELY TO IMPROVE EFFICIENCY. FOR HIGH EFFICIENCY, THE INDUCTOR SHOULD BE MOLYPERMALLOY OR FERRITE.

Maximum Output Power

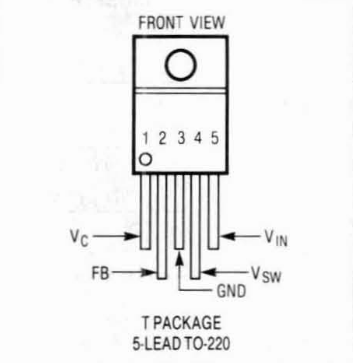


BUCK MODE OUTPUT POWER ≈ (3.5A)(V_{OUT})
†TRANSFORMER TURNS RATIO MUST BE OPTIMUM TO ACHIEVE FULL POWER.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 30V
Switch Output Voltage 60V
Feedback Pin Voltage (Transient, 1ms) .... ±15V
Operating Junction Temperature Range
(Oper.) .... 0°C to +100°C
(Short Ckt.) .... 0°C to +125°C
Storage Temperature Range .... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LT1271CT

ELECTRICAL CHARACTERISTICS

$V_{IN} = 15V$, $V_C = 0.5V$, $V_{FB} = V_{REF}$, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
		$V_C = 0.8V$	●	1.214	1.244	1.274	V
I_B	Feedback Input Current	$V_{FB} = V_{REF}$			350	750	nA
			●			1100	nA
gm	Error Amplifier Transconductance	$\Delta I_C = \pm 25\mu A$		3000	4400	6000	µmho
			●	2400		7000	µmho
	Error Amplifier Source or Sink Current	$V_C = 1.5V$		150	200	350	µA
			●	120		400	µA
	Error Amplifier Clamp Voltage	Hi Clamp, $V_{FB} = 1V$		1.8		2.3	V
		Lo Clamp, $V_{FB} = 1.5V$		0.25	0.38	0.52	V
	Reference Voltage Line Regulation	$3V \le V_{IN} \le V_{MAX}$, $V_C = 0.8V$	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	$0.9V \le V_C \le 1.4V$		500	800		V/V
	Minimum Input Voltage		●		2.8	3.0	V
I_Q	Supply Current	$3V \le V_{IN} \le V_{MAX}$, $V_C = 0.6V$			7	10	mA
	Control Pin Threshold	Duty Cycle = 0		0.8	0.9	1.08	V
			●	0.6		1.25	V
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage	$I_{FB} = 50\mu A$		15	16.3	17.6	V
			●	14		18	V
V_{FB}	Change in Flyback Reference Voltage	$0.05 \le I_{FB} \le 1mA$		4.5	6.8	8.5	V
	Flyback Reference Voltage Line Regulation	$I_{FB} = 50\mu A$ $3V \le V_{IN} \le V_{MAX}$			0.01	0.03	%/V
	Flyback Amplifier Transconductance (gm)	$\Delta I_C = \pm 10\mu A$		150	300	650	µmho
	Flyback Amplifier Source and Sink Current	$V_C = 0.6V$ Source	●	15	32	70	µA
		$I_{FB} = 50\mu A$ Sink	●	25	40	70	µA
BV	Output Switch Breakdown Voltage	$3V \le V_{IN} \le V_{MAX}$ $I_{SW} = 5mA$	●	60	75		V

ELECTRICAL CHARACTERISTICS $V_{IN} = 15V$, $V_C = 0.5V$, $V_{FB} = V_{REF}$, switch pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SAT}	Output Switch (Note 1) "On" Resistance		●		0.2	0.33	Ω
	Control Voltage to Switch Current Transconductance				6.4		A/V
I_{LIM}	Switch Current Limit (Note 2)	Duty Cycle = 50% Duty Cycle = 80%	● ●	4 3.2		8 8	A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				25	40	mA/A
f	Switching Frequency		 ●	50 50	60	70 70	kHz kHz
DC (max)	Maximum Switch Duty Cycle			85	92	95	%
	Flyback Sense Delay Time				1.5		μs
	Shutdown Mode Supply Current	$3V \le V_{IN} \le V_{MAX}$, $V_C = 0.05V$			100	400	μA
	Shutdown Mode Threshold Voltage	$3V \le V_{IN} \le V_{MAX}$	 ●	100 50	150	250 300	mV mV

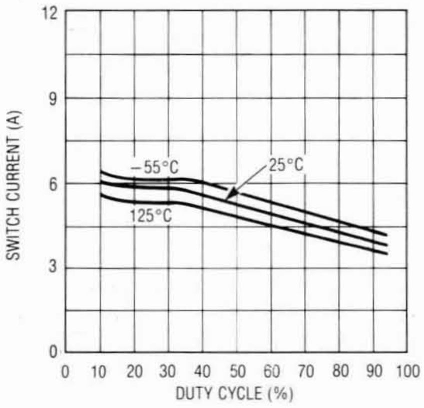
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Measured with V_C in hi clamp, $V_{FB} = 0.8V$.

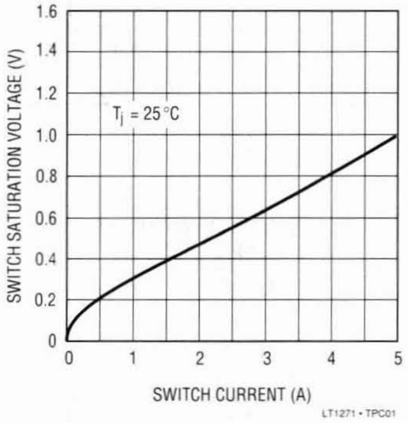
Note 2: For duty cycles (DC) between 50% and 85%, minimum guaranteed switch current is given by $I_{LIM} = 2.67\ (2 - DC)$ for the LT1271.

TYPICAL PERFORMANCE CHARACTERISTICS

Switch Current Limit vs Duty Cycle

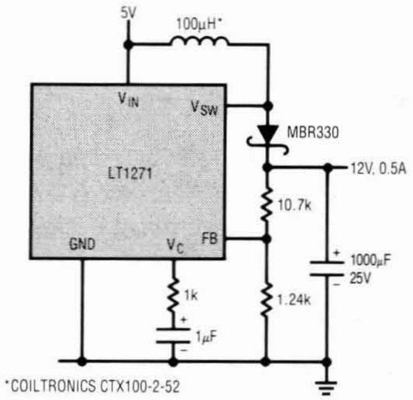


Switch Saturation Voltage



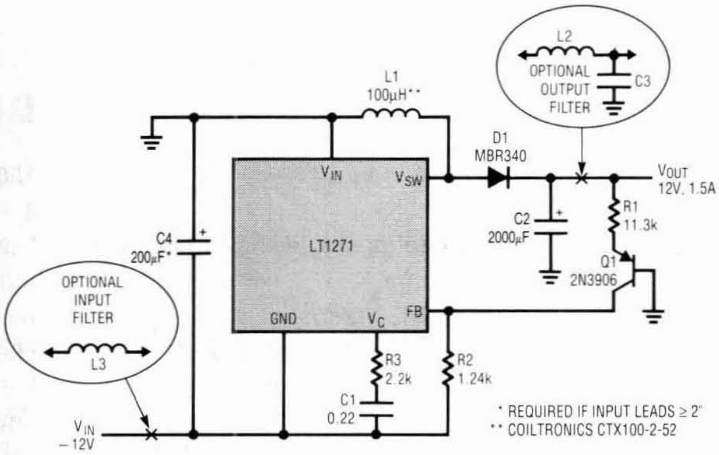
TYPICAL APPLICATIONS

Boost Converter (5V to 12V)


5V
100μH*
VIN
VSW
MBR330
LT1271
12V, 0.5A
10.7k
GND
VC
FB
1000μF
25V
1k
1.24k
1μF

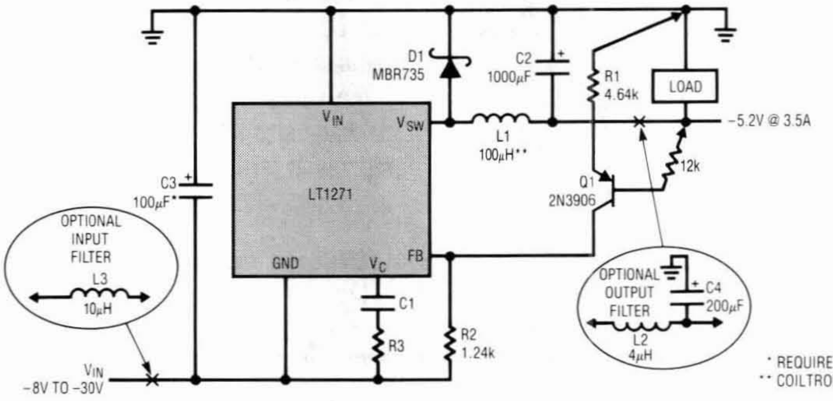
*COILTRONICS CTX100-2-52

Negative to Positive Buck-Boost Converter


L2
OPTIONAL
OUTPUT
FILTER
C3
L1
100μH**
D1
MBR340
VOUT
12V, 1.5A
VIN
VSW
C2
2000μF
R1
11.3k
C4
200μF*
LT1271
Q1
2N3906
OPTIONAL
INPUT
FILTER
GND
VC
FB
L3
R3
2.2k
R2
1.24k
C1
0.22
VIN
–12V

* REQUIRED IF INPUT LEADS ≥ 2"
** COILTRONICS CTX100-2-52

Negative Buck Converter


D1
MBR735
C2
1000μF
R1
4.64k
LOAD
VIN
VSW
L1
100μH**
–5.2V @ 3.5A
12k
Q1
2N3906
C3
100μF*
LT1271
OPTIONAL
INPUT
FILTER
L3
10μH
GND
VC
FB
C1
R3
R2
1.24k
OPTIONAL
OUTPUT
FILTER
C4
200μF
L2
4μH
VIN
–8V TO –30V

* REQUIRED IF INPUT LEADS ≥ 2"
** COILTRONICS CTX100-2-52

PRELIMINARY

LTC1291

Single Chip 12-Bit Data Acquisition System

November 1991

FEATURES

- Built-in Sample and Hold
- Single Supply 5V Operation
- Direct 3 Wire Interface to most MPU Serial Ports and and all MPU Parallel Ports
- Two Channel Analog Multiplexer
- Analog Inputs Common-Mode to Supply Rails

KEY SPECIFICATIONS

Resolution	12 Bits
Fast Conversion Time	12μS Max Over Temp.
Low Supply Currents	6.0mA

DESCRIPTION

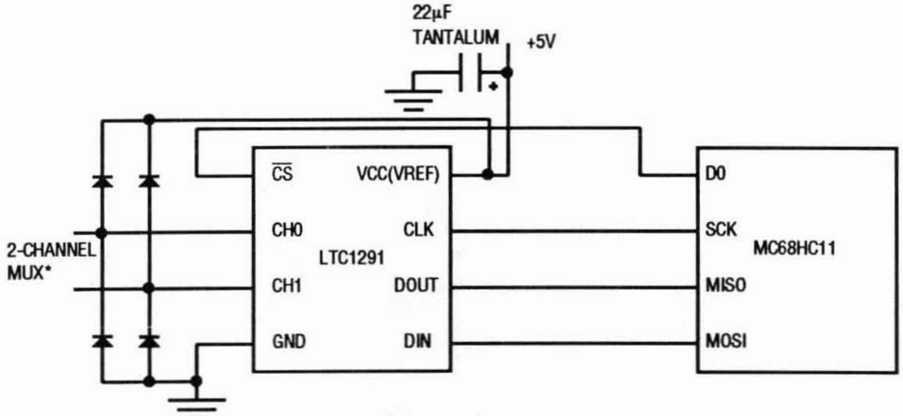
The LTC1291 is a data acquisition system which contains a serial I/O sucessive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform a 12-bit unipolar A/D conversion. The input multiplexer can be configured for either single-ended or differential inputs. An on-chip sample and hold is included on the (+) input. When the LTC1291 is idle it can be powered down in applications where low power consumption is desired. All these features are packaged in an 8-pin DIP.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing data to be transmitted over three wires. Given the accuracy, ease of use and small package size this device is well suited for digitizing analog signals in remote applications where minimum number of interconnects and power consumption are important.

LTCMOS is a trademark of Linear Technology

TYPICAL APPLICATION

2-Channel 12-Bit Data Aquisition System



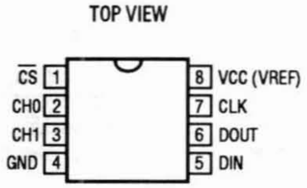
* FOR OVERVOLTAGE PROTECTION LIMIT THE INPUT CURRENT TO 15mA PER PIN OR CLAMP THE INPUTS TO Vcc AND GND WITH 1N4148 DIODES. CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED CHANNEL OR THE OTHER CHANNEL IS OVERVOLTAGED (VIN< GND OR VIN > Vcc).

ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage V_{CC} to GND 12V
Voltage
  Analog Inputs .... -0.3V to V_{CC}+0.3V
  Digital Inputs .... -0.3V to 12V
  Digital Outputs .... -0.3V to V_{CC}+0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1291BC,LTC1291CC,LTC1291DC ...... 0°C to 70°C
  LTC1291BI, LTC1291CI,LTC1291DI ...... -40°C to 85°C
  LTC1291BM,LTC1291CM,
  LTC1291DM..-55°C to 125°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION



J8 PACKAGE CERAMIC DIP
N8 PACKAGE PLASTIC DIP

ORDER PART NUMBER
LTC1291BMJ
LTC1291CMJ
LTC1291DMJ
LTC1291BIJ
LTC1291CIJ
LTC1291DIJ
LTC1291BIN
LTC1291CIN
LTC1291DIN
LTC1291BCN
LTC1291CCN
LTC1291DCN

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 3)

FINAL

PARAMETER	CONDITIONS		LTC1291B MIN	LTC1291B TYP	LTC1291B MAX	LTC1291C MIN	LTC1291C TYP	LTC1291C MAX	LTC1291D MIN	LTC1291D TYP	LTC1291D MAX	UNITS
Offset Error	(Note 4)	●			± 3.0			± 3.0			± 3.0	LSB
Linearity Error (INL)	(Notes 4 and 5)	●			± 0.5			± 0.5			± 0.75	LSB
Gain Error	(Note 4)	●			± 0.5			± 1.0			± 4.0	LSB
Minimum Resolution for Which No Missing Codes are Guaranteed		●			12			12			12	BITS
Analog and REF Input Range	(Note 7)		-0.05V to V_{CC} + 0.05V			-0.05V to V_{CC} + 0.05V			-0.05V to V_{CC}+ 0.05V			V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			± 1			± 1			± 1	µA
	On Channel = 0V Off Channel = 5V	●			± 1			± 1			± 1	µA
Off Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			± 1			± 1			± 1	µA
	On Channel = 0V Off Channel = 5V	●			± 1			± 1			± 1	µA

AC CHARACTERISTICS (Note 3)

FINAL

				LTC1291B LTC1291C LTC1291D			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNITS**
F_{CLK}	Clock Frequency	V_{CC} = 5V (Note 6)		0.1		1.0	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			2.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		18 CLK + 500ns			Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		160	300	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		80	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		80	200	ns
t_{hDI}	Hold Time, D_{IN} after CLK↑	V_{CC} = 5V (Note 6)		50			ns
t_{hDO}	Time Output Data Remains Valid After CLK↓				130		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	50	ns
t_{suDI}	Setup Time, D_{IN} Stable before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ Before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	V_{CC} = 5V (Note 6)		500			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V (Note 6)		18			CLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel			100		pF
		Analog Inputs Off Channel			5		pF
		Digital Inputs			5		pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 5V and CLK = 1.0MHz unless otherwise specified. The ● indicates specs which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 4: One LSB is equal to V_{CC} divided by 4096. For example, when V_{CC} = 5V, 1 LSB = 5V/4096 = 1.22mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

Note 7: Two on-chip diodes are tied to each analog input which will conduct for analog voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperature, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

Note 8: Channel leakage current is measured after the channel selection.

DIGITAL AND DC ELECTRICAL CHARACTERISTICS(Note 3) FINAL

						LTC1291B LTC1291C LTC1291D		
SYMBOL	**PARAMETER**	**CONDITIONS**			**MIN**	**TYP**	**MAX**	**UNITS**
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V		●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V		●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$		●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V		●			- 2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = -10µA V_{CC} = 4.75V, I_O = -360µA		 ●	 2.4	4.7 4.0		V µA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA		●			0.4	V
I_{OZ}	High Z Output Leakage	$V_{OUT} = V_{CC}$, $\overline{CS}$ High V_{OUT} = 0V, $\overline{CS}$ High		● ●			3 - 3	µA µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V				-20		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$				20		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High		●		6	12	mA
		$\overline{CS}$ High Power Shutdown	LTC1291BC, LTC1291CC, LTC1291DC, LTC1291BI, LTC1291CI, LTC1291DI	●		5	10	µA
		CLK Off	LTC1291BM, LTC1291CM, LTC1291DM	●		5	15	µA

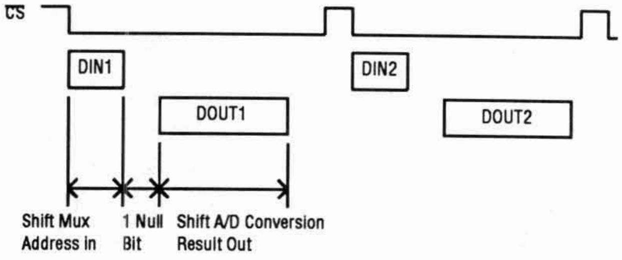
PIN FUNCTIONS

#	PIN	FUNCTION	DESCRIPTION
1	$\overline{CS}$	Chip Select Input	A logic low on this input enables the LTC1291.
2,3	CH0, CH1	Analog Inputs	These inputs must be free of noise with respect to GND.
4	GND	Analog Ground	GND should be tied directly to an analog ground plane.
5	D_{IN}	Digital Data Input	The multiplexer address is shifted into this input.
6	D_{OUT}	Digital Data Output	The A/D conversion result is shifted out of this output.
7	CLK	Shift Clock	This clock synchronizes the serial data transfer.
8	$V_{CC}(V_{REF})$	Positive Supply and and Reference Voltage	This pin provides power and defines the span of the A/D converter. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

APPLICATIONS INFORMATION

SERIAL INTERFACE

The LTC1291 communicates with microprocessors and other external circuitry via a synchronous, half duplex, four wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

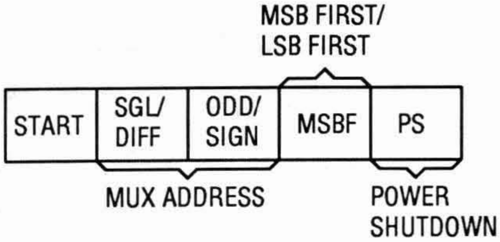


APPLICATIONS INFORMATION

The input data is first received and then the A/D conversion result is transmitted (half duplex). Because of the half duplex operation D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}). Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1291 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1291 in preparation for the next data exchange.

INPUT DATA WORD

The LTC1291 four bit data word is clocked into the D_{IN} input on the rising edge of the clock after chip select goes low and the start bit has been recognizied. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The input word is defined as follows:



START BIT

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeroes which precede this logical one will be ignored. After the start bit is received the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

MUX ADDRESS

The bits of the input word following the START BIT assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and - signs in the selected row of the following table. In single ended mode, all input channels are measured with respect to GND. Only the + inputs have sample and holds. Signals applied at the -inputs must not change more than the required accuracy during the conversion.

MULTIPLEXER CHANNEL SELECTION

MUX ADDRESS		CHANNEL #		GND
SGL/ DIFF	ODD/ SIGN	0	1	
1	0	+		-
1	1		+	-
0	0	+	-	
0	1	-	+	

MSB FIRST/LSB FIRST (MSBF)

The output data of the LTC1291 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zereos will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line (See operating sequence).

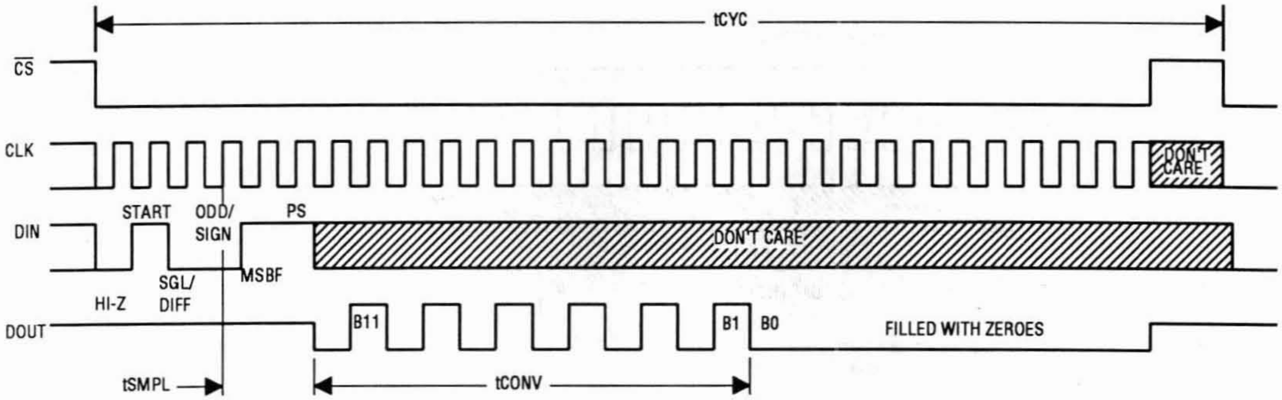
POWER SHUTDOWN

The power shutdown feature of the LTC1291 is activated by making the PS bit a logical zero. If $\overline{CS}$ remains low after the PS bit has been received, a 12-bit D_{OUT} word with all logical ones will be shifted out followed by logical zeroes till $\overline{CS}$ goes high. Then the D_{OUT} line will go into its high impedance state. The LTC1291 will remain in the shutdown mode tell the next $\overline{CS}$ cycle. There is no warm up or wait period required after coming out ot the power shutdown cycle so a conversion can commence after $\overline{CS}$ goes low (See power shutdown operating sequence).

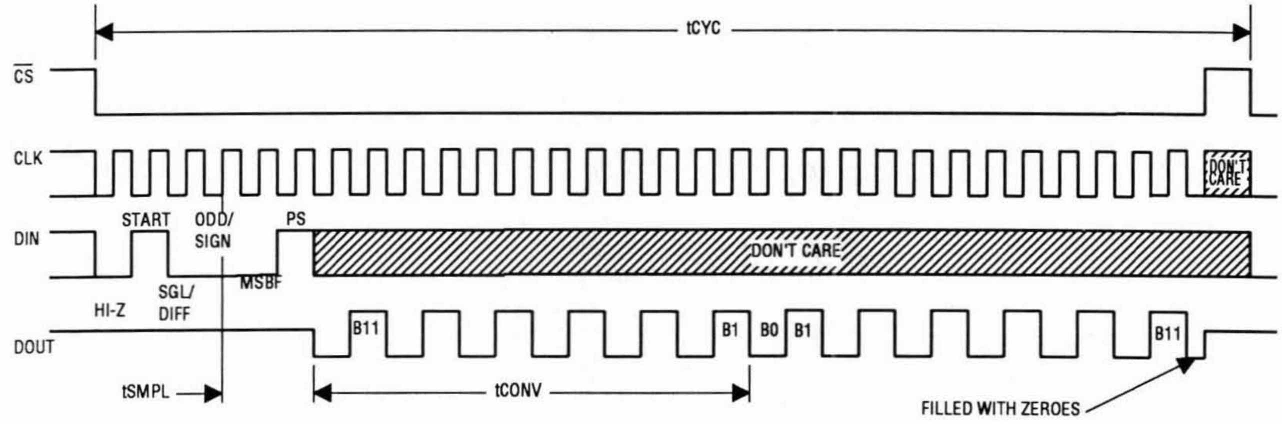
APPLICATIONS INFORMATION

Operating Sequence
(Example: Differential Inputs (CH0+, CH1-))

MSB FIRST DATA (MSBF=1)

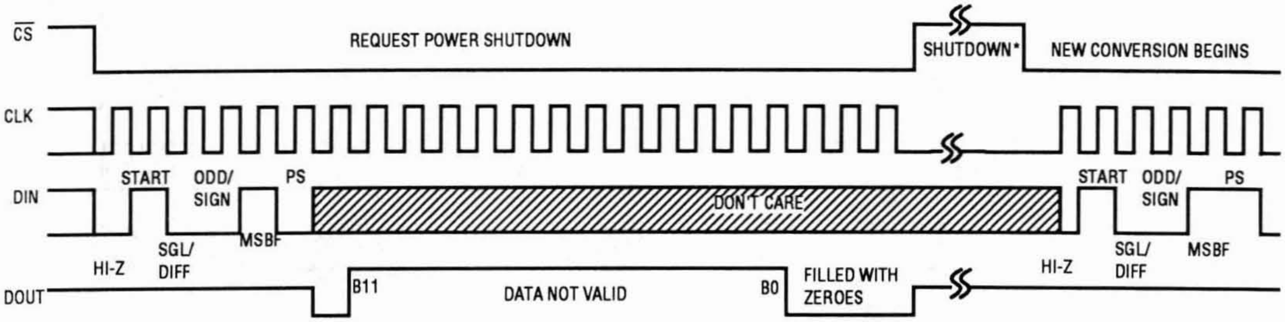

tCYC
CS
CLK
DON'T CARE
DIN
START
ODD/
SIGN
PS
DON'T CARE
SGL/
DIFF
MSBF
HI-Z
DOUT
B11
B1
B0
FILLED WITH ZEROES
tSMPL
tCONV

LSB FIRST DATA (MSBF=0)


tCYC
CS
CLK
DON'T CARE
DIN
START
ODD/
SIGN
PS
DON'T CARE
SGL/
DIFF
MSBF
HI-Z
DOUT
B11
B1
B0
B1
B11
tSMPL
tCONV
FILLED WITH ZEROES

APPLICATIONS INFORMATION

Power Shutdown Operating Sequence
(Example: Differential Inputs (CH0+,CH1-) and MSB First Data)


CS
REQUEST POWER SHUTDOWN
SHUTDOWN*
NEW CONVERSION BEGINS
CLK
DIN
START
ODD/
SIGN
PS
SGL/
DIFF
MSBF
DON'T CARE
START
ODD/
SIGN
PS
SGL/
DIFF
MSBF
HI-Z
DOUT
B11
DATA NOT VALID
B0
FILLED WITH
ZEROES
HI-Z

* Stopping the clock will help reduce power consumption
CS can be brought high once DIN has been clocked in

PRELIMINARY

LT1330

5V RS232 Transceiver with 3V Logic Interface and One Receiver Active in SHUTDOWN

June, 1992

FEATURES

- **3V Logic Interface**
- ESD Protection over ±10kV
- Uses Small Capacitors (0.1µF, 0.2µF, 1.0µF)
- One Low Power Receiver Remains Active while in SHUTDOWN
- Pin Compatible with LT1137 and LT1237
- Operates to 120kbaud
- CMOS Comparable Low Power: 30mW
- Easy PC Layout Flow Through Architecture
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Absolutely No Latchup
- 60µA Supply Current in SHUTDOWN
- Available in SO Package

APPLICATIONS

- Notebook Computers
- Palmtop Computers

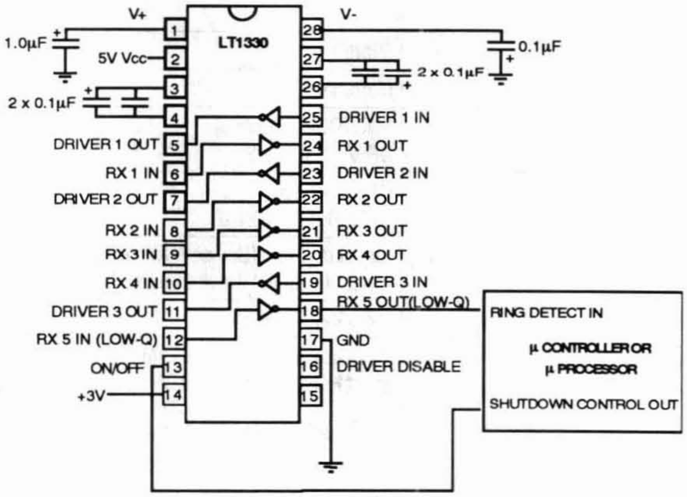
DESCRIPTION

The LT1330 is a three driver, five receiver RS232 transceiver with low supply current. Designed to interface with new 3V logic, the LT1330 operates with both a +5V power supply and a 3V logic power supply. The chip may be shut down to micropower operation with one receiver remaining active to monitor RS232 inputs such as ring detect from a modem.

The LT1330 is fully compliant with all EIA RS232 specifications. Additionally, the RS232 line input and output pins are resilient to multiple +/-10kV ESD strikes. This eliminates the need for costly transorbs on line pins for the RS232 part.

The LT1330 operates to 120 kilobaud even while driving high capacitive loads. During shutdown, driver and receiver outputs are at a high impedance state allowing devices to be paralleled.

Typical Application


V+
V-
LT1330
1.0µF
5V Vcc
2 x 0.1µF
0.1µF
2 x 0.1µF
DRIVER 1 OUT
RX 1 IN
DRIVER 2 OUT
RX 2 IN
RX 3 IN
RX 4 IN
DRIVER 3 OUT
RX 5 IN (LOW-Q)
ON/OFF
+3V
DRIVER 1 IN
RX 1 OUT
DRIVER 2 IN
RX 2 OUT
RX 3 OUT
RX 4 OUT
DRIVER 3 IN
RX 5 OUT(LOW-Q)
GND
DRIVER DISABLE
RING DETECT IN
µ CONTROLLER OR
µ PROCESSOR
SHUTDOWN CONTROL OUT
1
2
3
4
5
6
7
8
9
10
11
12
13
14
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16
17
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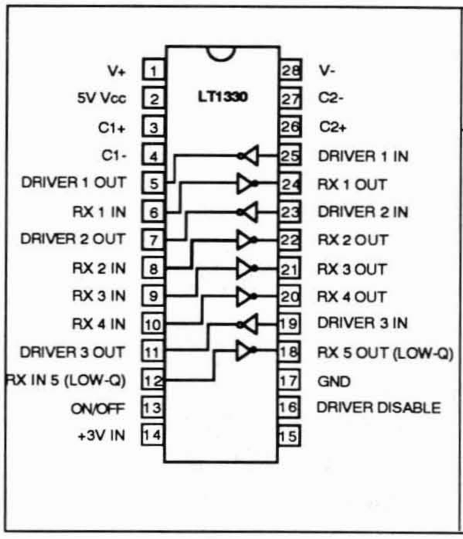
28

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Vcc) 6V
Supply Voltage (+3 Vin) 6V
V+ .... +13.2V
V- .... -13.2V
Input Voltage
  Driver .... V+ to V-
  Receiver .... +30V to -30V
Output Voltage
  Driver .... -55°C to 125°C
  Receiver .... 0°C to 70°C
Short Circuit Duration
V+ 30s
V- 30s
Driver Output .... Indefinite
Receiver Output .... Indefinite
Operating Temperature Range
  LT1330I .... -40°C to 85°C
  LT1330C .... 0°C to 70°C
Storage Temperature Range .... -65°C to 150°C
Lead Temperature (Soldering, 10 sec.) .... 300°C

PACKAGE/ORDER INFORMATION


LT1330
V+ 1
5V Vcc 2
C1+ 3
C1- 4
DRIVER 1 OUT 5
RX 1 IN 6
DRIVER 2 OUT 7
RX 2 IN 8
RX 3 IN 9
RX 4 IN 10
DRIVER 3 OUT 11
RX IN 5 (LOW-Q) 12
ON/OFF 13
+3V IN 14
15
DRIVER DISABLE 16
GND 17
RX 5 OUT (LOW-Q) 18
DRIVER 3 IN 19
RX 4 OUT 20
RX 3 OUT 21
RX 2 OUT 22
DRIVER 2 IN 23
RX 1 OUT 24
DRIVER 1 IN 25
C2+ 26
C2- 27
V- 28

ORDER PART NUMBER
LT1330IJ LT1330CJ LT1330CN LT1330CS

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V+ Output				8.6		V
V- Output				- 7.0		V
Supply Current (V_{CC})	(Note 3)			6	9	mA
Supply Current (+3V)	(Note 4)			0.1	1	mA
Supply Current when OFF (V_{CC})	SHUTDOWN (Note 5) DRIVER DISABLE	●		0.06 3	0.150	mA mA
Supply Rise Time SHUTDOWN to Turn On	C1=C2=0.2uF C+=1.0μF, C-=0.1μF			2 0.2		ms ms
ON/OFF Pin Thresholds	Input Low Level (Device SHUTDOWN) Input High Level (Device Enabled)	● ●	 2.0	1.4 1.4	0.8	V V
ON/OFF Pin Current	$0V \le V_{ON/OFF} \le 5V$	●	- 15		80	μA
Driver Disable Pin Thresholds	Input Low Level (Drivers Enabled) Input High Level (Drivers Disabled)	● ●	 2.0	1.4 1.4	0.8	V V
DRIVER DISABLE Pin Current	$0V \le V_{DRIVER\ DISABLE} \le 5V$	●	- 10		500	μA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Voltage Swing	Load = 3k to GND Positive Negative	● ●	5.0 -5.0	7.3 -6.5		V V
Logic Input Voltage Level	Input Low Level (V_{OUT}=High) Input High Level (V_{OUT}=Low)	● ●	 2.0	1.4 1.4	0.8	V V
Logic Input Current	0.8V ≤ V_{IN} ≤ 2.0V	●		5	20	µA
Output Short Circuit Current	V_{OUT} = 0V			17		mA
Output Leakage Current	SHUTDOWN Vout = ±30V (Note 5)	●		10	100	µA
Slew Rate	R_L=3k, C_L=51pF R_L=3k, C_L=2500pF		 4	15 15	30	V/µs V/µs
Propagation Delay	Output Transition t_{HL} High to Low (Note 6) Output Transition t_{LH} Low to High			0.6 0.5	1.3 1.3	µS µS
Any Receiver						
Input Voltage Thresholds	Input Low Threshold (V_{OUT}= High) Input High Threshold (V_{OUT}= Low)		0.8	1.3 1.7	 2.4	V V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance			3	5	7	kΩ
Ouput Leakage Current	SHUTDOWN (Note) 0 ≤ V_{OUT} ≤ V_{CC}	●		1	10	µA
Receivers 1 Through 4						
Output Voltage	Output Low, I_{OUT} = -1.6mA Output High, I_{OUT} = 160µA (Pin 14 = 3V)	● ●	 2.7	0.2 2.9	0.4	V V
Output Short Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V		-10 10	-20 20		mA mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 7) Output Transition t_{LH} Low to High			250 350	600 600	nS nS
Receiver 5 (LOW Q-CURRENT RX)						
Output Voltage	Output Low, I_{OUT} = -500µA Output High, I_{OUT} = 160µA (Pin 14 = 3V)	● ●	 2.7	0.2 2.9	0.4	V V
Output Short Circuit Current	Sinking Current, V_{OUT} = Vcc Sourcing Current, V_{OUT} = 0V		-2 2	-4 4		mA mA
Propagation Delay	Output Transition t_{HL} High to Low (Note 7) Output Transition t_{LH} Low to High			1.0 1.0	3 3	µS µS

The ● denotes specifications which apply over the operating temperature range. (0 °C ≤ T_A ≤ 70° C for commercial grade, -40°C ≤ T_A ≤ 85°C for industrial grade, and -55°C ≤ T_A ≤ 125°C for military grade.)

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/OFF}$=3V.

Note 3: Supply current is measured as the average over sever charge pump burst cycles. C+=1.0µF, C-=0.1µF, C1=C2=0.2µF. All outputs are open, with all driver inputs tied high.

Note 4: +3V supply current is measured with all receiver outputs low.

Note 5: Supply current measurements in SHUTDOWN are performed with $V_{ON/OFF}$ ≤ 0.1V. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE}$ ≥ 3V.

Note 6: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing. (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V)

Note 7: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold. (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V)

PIN FUNCTIONS

V_{CC}: +5V Input supply pin. This pin should be decoupled with a 0.1uF ceramic capacitor.

+3V Input: Logic supply pin for all RS232 receivers. Like V_{CC}, the +3V input should be decoupled with a 0.1μF ceramic capacitor. May also be connected to +5V.

GND: Ground Pin.

On/Off: TTL/CMOS compatible operating mode control. A logic low puts the device in the low power SHUTDOWN mode with all drivers and four receivers in a high impedance state. A logic high fully enables the transceiver.

DRIVER DISABLE: An alternate control for the charge pump and RS232 drivers. A logic high on this pin shuts down the charge pump and places all drivers in a high impedance state. All receivers remain active under these conditions. Floating the pin or forcing a logic low level fully enables the transceiver.

V+: Positive supply output. $V+ \approx 2V_{CC} - 1.5V$. This pin requires an external storage capacitor, $C \geq 1.0\mu F$, tied to ground or +5V. Larger value capacitors may be used to reduce supply ripple. The ratio of the capacitors on V+ and V- should be greater than 5 to 1.

V-: Negative supply output. $V- \approx -(2V_{CC}-2.5V)$. This pin requires an external storage capacitor, $C \geq 0.1\mu F$. To reduce supply ripple, increase the size of the storage capacitor.

C1+;C1-;C2+;C2-: Commutating capacitor inputs require two external capacitors, $C \geq 0.2\mu F$. One from C1+ to C1- and another from C2+ to C2-. The capacitor's effective series resistance should be less than 2Ω. For $C \geq 1\mu F$, low ESR tantalum capacitors work well, although ceramic capacitors may be used with a minimal reduction in charge pump compliance.

DRIVER IN: RS232 driver input pins. These inputs are TTL/CMOS compatible. Unused inputs should be connected to V_{CC}.

DRIVER OUT: Driver outputs at RS232 voltage levels. Outputs are in a high impedance state when in SHUTDOWN mode, V_{CC} = 0V, or when the driver disable pin is active. Outputs are fully short circuit protected for Vout from V- + 30V to V+ - 30V. Higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±10kV for human body model discharges.

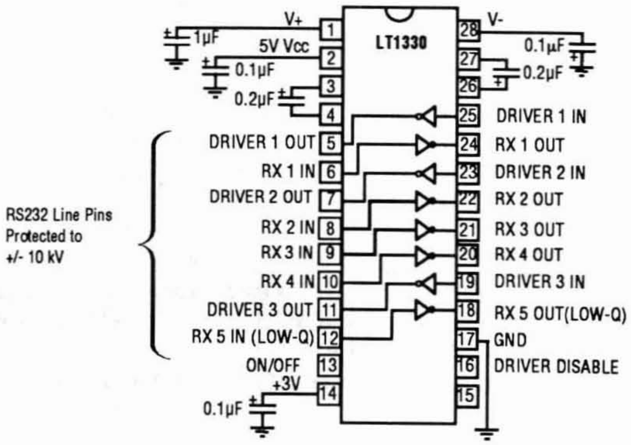
RX IN: Receiver inputs. These pins accept RS232 level signals (±30V) into a protected 5kΩ terminating resistor. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity.

RX OUT: Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance stage when in SHUTDOWN mode to allow data line sharing. Outputs, including LOW-Q RXOUT, are fully short circuit protected to ground or Vcc with the power on, off, or in SHUTDOWN mode.

LOW Q-CURRENT RX IN: Low power receiver input. This special receiver remains active when the part is in SHUTDOWN mode, consuming typically 60μA. This receiver has the same input and protection characteristics as the other receivers.

LOW Q-CURRENT RX OUT: Low power receiver output. This pin produces the same TTL/CMOS output voltage levels with slightly decreased speed and drive current.

ESD Test Circuit



PRELIMINARY

LTC1485

Differential Bus Transceiver

September 1991

FEATURES

- Low Power : Icc=2.5mA typ.
- Designed for RS485 or RS422 applications.
- Single +5V supply.
- -7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- Power up/down glitch free driver outputs permit live insertion or removal of package.
- Driver maintains high impedance in Three-state or with the power off.
- Combined impedance of a driver output and receiver allows up to 32 transceivers on the bus.
- 70 mV typical input hysteresis.
- 28 nS typical driver propagation delays with 5 nS skew.
- Pin compatiable with the SN75176A and DS75176A.

APPLICATIONS

- Low Power RS485/RS422 Transceiver
- Level translator

DESCRIPTION

The LTC1485 is a low power differential bus/line transceiver designed for multipoint data transmission standard RS485 applications with extended common mode range (+12V to -7V). It also meets the requirements of RS422.

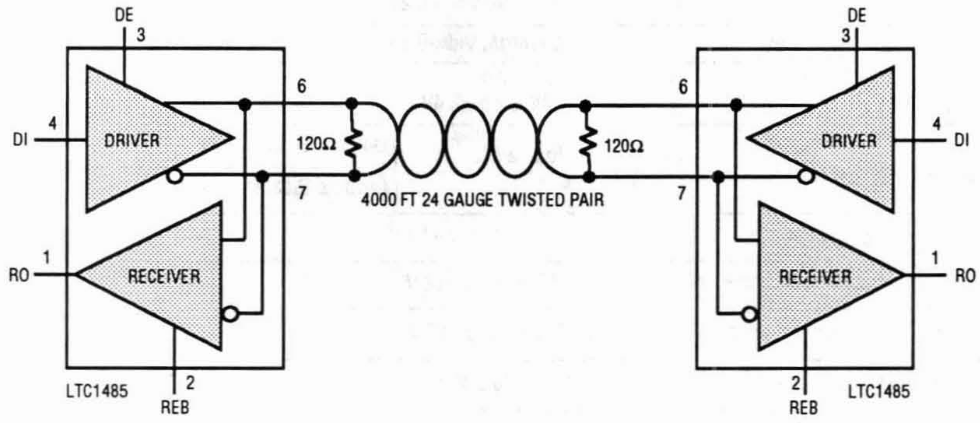
The CMOS design offers significant power savings over its bipolar counterpart without sacrificing ruggedness against overload or ESD damage.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state.

The receiver has a fail safe feature which guarantees a high output state when the inputs are left open.

Both AC and DC specifications are guaranteed from 0°C to 70°C and 4.75V to 5.25V supply voltage range.

TYPICAL APPLICATION

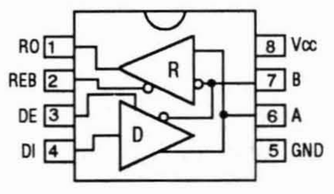


ABSOLUTE MAXIMUM RATINGS

(Note1)

Supply Voltage (Vcc)...12V
Control Input Voltages......................-0.5V to Vcc+0.5V
Control Input Currents..........................-50mA to 50mA
Driver Input Voltages........................-0.5V to Vcc+0.5V
Driver Input Currents............................-25mA to 25mA
Driver Output Voltages...±14V
Receiver Input Voltages.......................................±14V
Receiver Output Voltages.................-0.5V to Vcc+0.5V

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1485CN8
LTC1485CS8
LTC1485IN8
LTC1485IS8

DC ELECTRICAL CHARACTERISTICS

Vcc = 5V ± 5% , 0°C ≤ Temp. ≤ 70°C (Note 2 &3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Vod1	Differential Driver Output Voltage (unloaded)	Io = 0				5	V
Vod2	Differential Driver Output Voltage (with load)	R = 50 Ω ; (RS422)		2			V
		R = 27 Ω ; (RS 485); Figure1		1.5		5	V
ΔVod	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27 Ω or R = 50 Ω Figure 1				0.2	V
Voc	Driver Common Mode Output Voltage					3	V
Δ|Voc|	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States					0.2	V
Vih	Input High Voltage	DI, DE, REB		2.0			V
Vil	Input Low Voltage					0.8	V
Iin1	Inout Current					±2	µA
Iin2	Input Current (A, B)	Vcc=0 or 5.25V	Vin = 12V			+1.0	mA
			Vin = -7V			-0.8	mA
Vth	Differential Input Threshold Voltage for Receiver	-7V ≤ Vcm ≤ 12V		-0.2		+0.2	V
ΔVth	Receiver Input Hysteresis	Vcm = 0V			70		mV
Voh	Receiver Output High Voltage	Io=-4mA, Vid=+0.2V		3.5			V
Vol	Receiver Output Low Voltage	Io=+4mA, Vid=-0.2V				0.4	V
Iozr	Three-State Output Current at Receiver	Vcc = Max. 0.4V ≤ Vo ≤2.4V				±1	µA
Icc	Supply Current	No Load; DI=GND or Vcc	Outputs Enabled		2.7		mA
			Outputs Disabled		2.5		mA
Rin	Receiver Input Resistance	-7 V ≤ Vcm ≤ +12 V		12			KΩ
Iosd1	Driver Short-Circuit Current, Vout=high	-7 V ≤ Vo ≤ +12 V				250	mA
Iosd2	Driver Short-Circuit Current, Vout=low	-7 V ≤ Vo ≤ +12 V				250	mA
Iosr	Receiver Short-Circuit Current	0 V ≤ Vo ≤ Vcc		7		85	mA
Ioz	Driver Tri-State Output Current	Vo = -7V to 12V				±100	µA

SWITCHING CHARACTERISTICS Vcc = 5V ± 5% , 0°C ≤ Temp. ≤ 70°C (Note 2 &3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	Rdiff = 54 Ω C_{L1} = C_{L2} = 100pF (Figures 2&5)		28		nS
t_{PHL}	Driver Input to Output			28		nS
t_{SKEW}	Driver Output to Output			5		nS
tr , tf	Driver Rise or Fall Time			20		nS
t_{ZH}	Driver Enable to Output High	C_L = 100 pF (Figures 4&6) S2 closed		40		nS
t_{ZL}	Driver Enable to Output Low	C_L = 100 pF (Figures 4&6) S1 closed		40		nS
t_{LZ}	Driver Disable Time from Low	C_L = 15 pF (Figures 4&6) S1 closed		40		nS
t_{HZ}	Driver Disable Time from High	C_L = 15 pF (Figures 4&6) S2 closed		40		nS
t_{PLH}	Receiver Input to Output	Rdiff = 54Ω C_{L1} = C_{L2} = 100pF (Figures 2&7)		25		nS
t_{PHL}	Receiver Input to Output			25		nS
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew			13		nS
t_{ZL}	Receiver Enable to Output Low	C_L = 15pF (Figures 3&8) S1 closed		20		nS
t_{ZH}	Receiver Enable to Output High	C_L = 15pF (Figures 3&8) S2 closed		20		nS
t_{LZ}	Receiver Disable from Low	C_L = 15pF (Figures 3&8) S1 closed		20		nS
t_{HZ}	Receiver Disable from High	C_L = 15pF (Figures 3&8) S2 closed		20		nS

Note 1 : "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed.

Note 2 : All currents into device pins are positive ; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3 : All typicals are given for Vcc = 5 V and Temp. = 25 °C.

PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1	RO	Receiver output. If the receiver output is enabled (REB low), then if A>B by 200mV, R will be high. If A < B by 200mV, then R will be low.
2	REB	Receiver output enable. A low enables the receiver output, R. A high input forces the receiver output into a high impedance state.
3	DE	Driver outputs enable. A high on DE enables the driver outputs,A and B. A low input will force the driver outputs into a high impedance state.
4	DI	Driver input. If the driver ouputs are enabled (DE high), then a low on D forces the driver outputs A low and B high. A high on D will force A high and B low.
5	GND	Ground Connection.
6	A	Driver output / Receiver input.
7	B	Driver output / Receiver input.
8	Vcc	Positive supply ; 4.75V ≤ Vcc ≤ 5.25V

TEST CIRCUITS

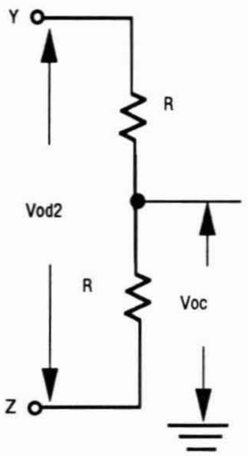

Y
R
Vod2
R
Voc
Z

Figure 1. Driver DC Test Load

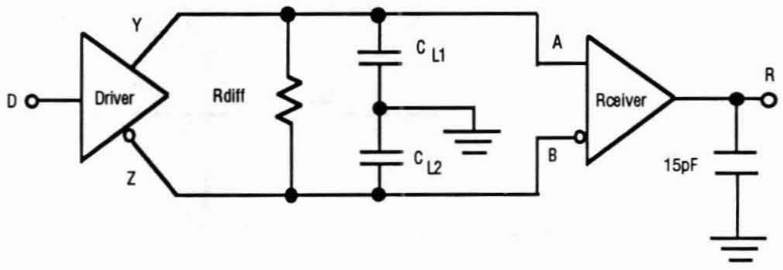

D
Driver
Y
Z
Rdiff
C L1
C L2
A
B
Rceiver
R
15pF

Figure 2. Driver/Receiver Timing Test Circuit

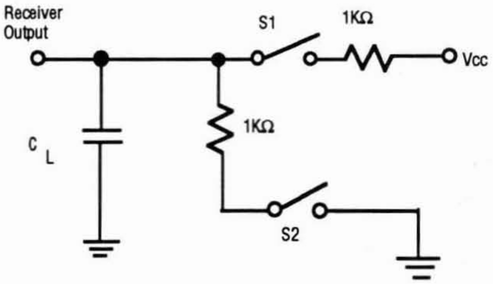

Receiver Output
C L
S1
1KΩ
Vcc
1KΩ
S2

Figure 3. Receiver Timing Test Load

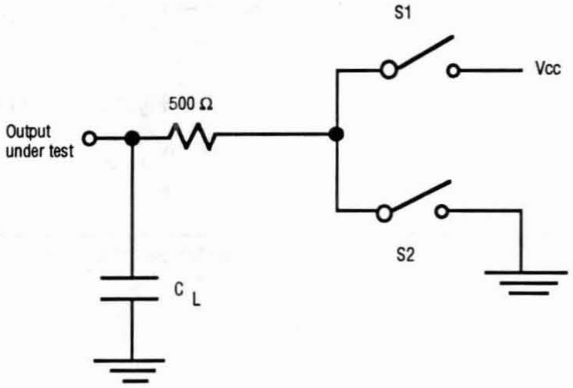

S1
Vcc
500 Ω
Output under test
S2
C L

Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

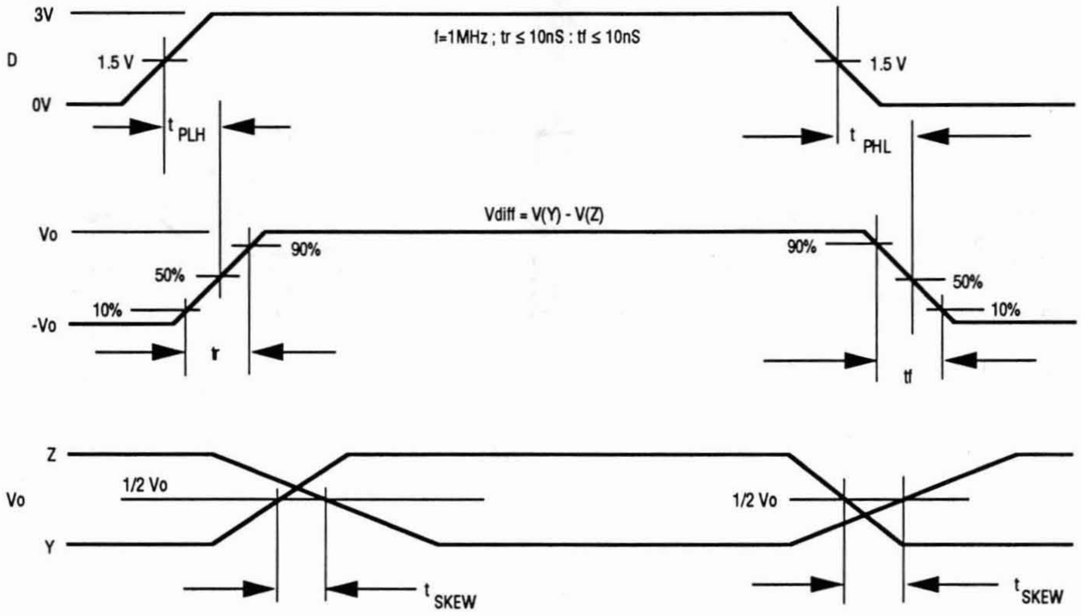

3V
D
1.5 V
0V
f=1MHz ; tr ≤ 10nS : tf ≤ 10nS
1.5 V
t PLH
t PHL
Vdiff = V(Y) - V(Z)
Vo
90%
50%
10%
-Vo
tr
90%
50%
10%
tf
Z
1/2 Vo
Vo
Y
1/2 Vo
t SKEW
t SKEW

Figure 5. Driver Propagation Delays

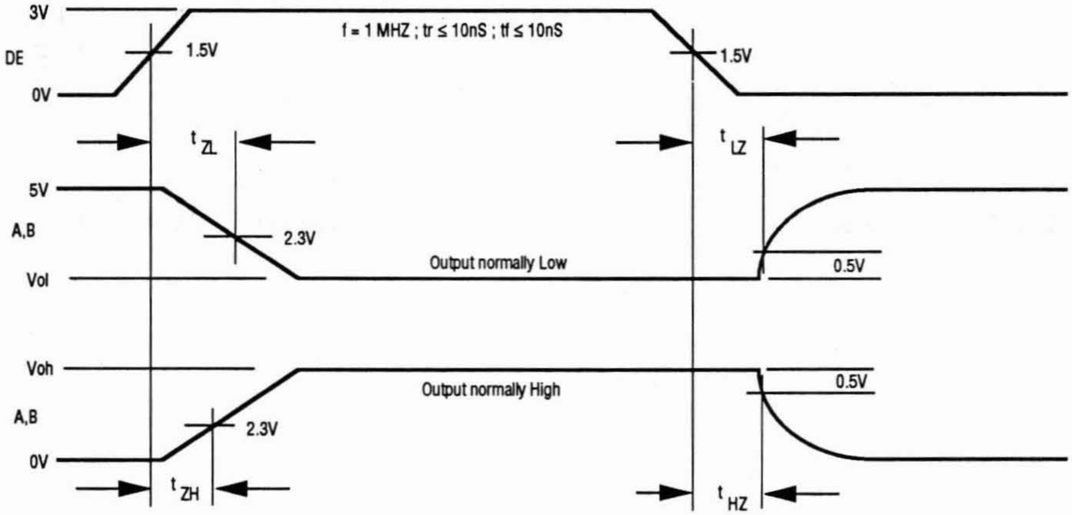

3V
DE
0V
1.5V
f = 1 MHZ ; tr ≤ 10nS ; tf ≤ 10nS
1.5V
t ZL
t LZ
5V
A,B
2.3V
Vol
Output normally Low
0.5V
Voh
Output normally High
0.5V
A,B
2.3V
0V
t ZH
t HZ

Figure 6. Driver Enable and Disable Times

SWITCHING TIME WAVEFORMS

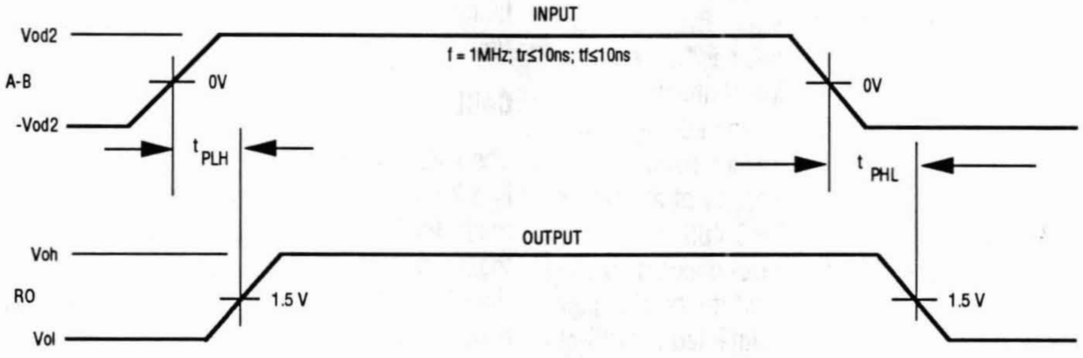

INPUT
f = 1MHz; tr≤10ns; tf≤10ns
Vod2
A-B
-Vod2
0V
0V
t PLH
t PHL
OUTPUT
Voh
RO
Vol
1.5 V
1.5 V

Figure 7. Receiver Propagation Delays

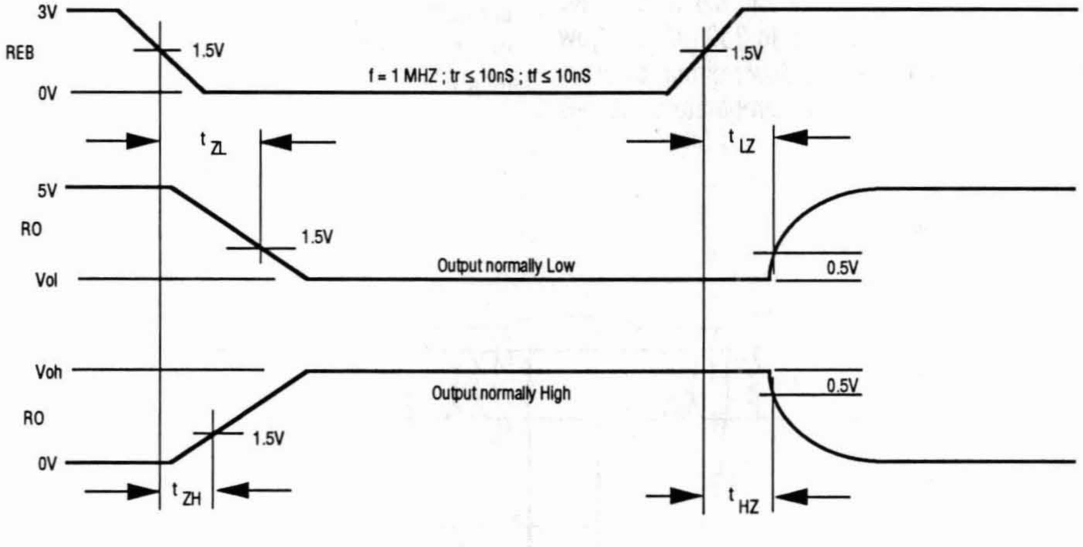

3V
REB
0V
1.5V
1.5V
f = 1 MHZ ; tr ≤ 10nS ; tf ≤ 10nS
t ZL
t LZ
5V
RO
Vol
1.5V
Output normally Low
0.5V
Voh
RO
0V
Output normally High
0.5V
1.5V
t ZH
t HZ

Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

TYPICAL APPLICATION

A typical connection of the LTC1485 is shown in Figure 1. Two twisted pair wires connect up to 32 driver/receiver pairs for half duplex data transmission. There are no restrictions on where the chips are connected to the wires, and it isn't necessary to have the chips connected at the ends. However, the wires must be terminated only at the ends with a resistor equal to their characteristic impedance, typically 120 Ω. The input impedance of a receiver is typically 20 kΩ to GND, or 0.6 unit RS-485 load, so in practice 50 to 60 transceivers can be connected to the same wires. The optional shields around the twisted pair help reduce unwanted noise, and are connected to GND at one end.

THERMAL SHUTDOWN

The LTC1485 has a thermal shutdown feature which protects the part from excessive power dissipation. If the outputs of the driver are accidently shorted to a power supply or low impedance source, up to 250 mA can flow through the part. The thermal shutdown circuit disables the driver outputs when the internal temperature reaches 150 C and turns them back on when the temperature cools to 130 C. If the outputs of two or more LTC1485 drivers are shorted directly, the driver outputs can not supply enough current to activate the thermal shutdown. Thus, the thermal shutdown circuit will not prevent contention faults when two drivers are active on the bus at the same time.

CABLES AND DATA RATE

The transmission line of choice for RS-485 applications is a twisted pair. There are coaxial cables (twinaxial) made for this purpose that contain straight pairs, but these are less flexible, more bulky, and more costly than twisted pairs. Many cable manufacturers offer a broad range of 120 Ω cables designed for RS-485 applications.

Losses in a transmission line are a complex combination of DC conductor loss, AC losses (skin effect), leakage, and AC losses in the dielectric. In good polyethylene cables such as the Belden 9841, the conductor losses and dielectric losses are of the same order of magnitude, leading to relatively low over all loss (Figure 2).

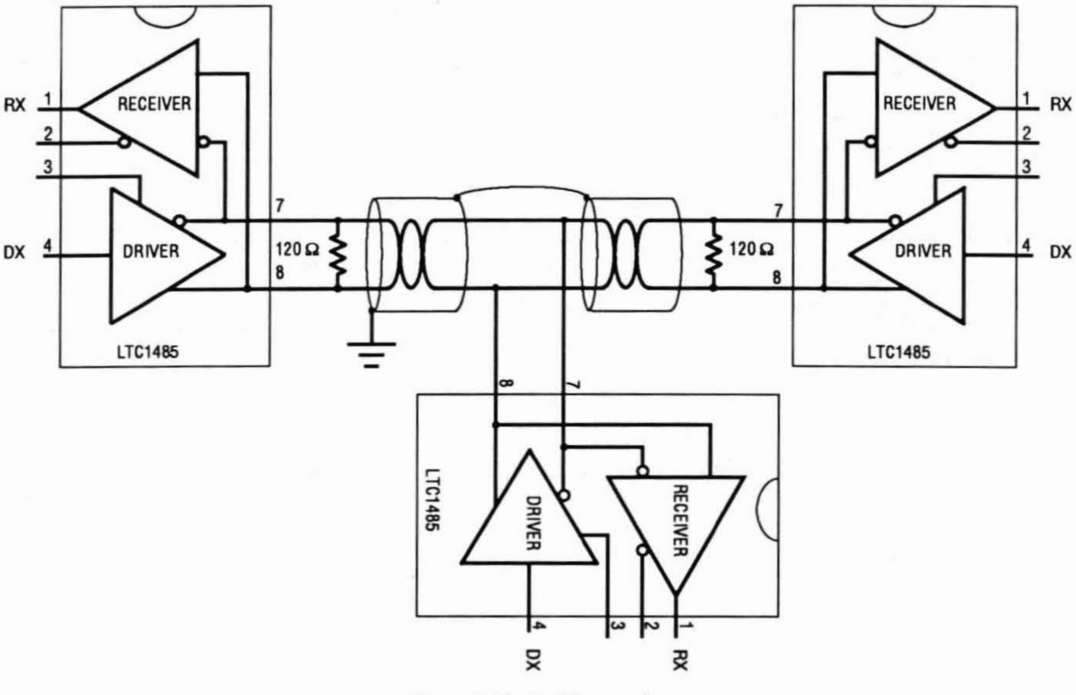


Figure 1. Typical Connection

APPLICATIONS INFORMATION

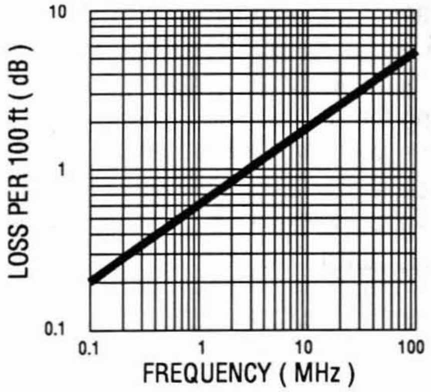


Figure 2 Attenuation - vs - Frequency For Belden 9481

When using low loss cables, Figure 3 can be used as a guideline for choosing the maximum line length for a given data rate. With lower quality PVC cables, the dielectric loss factor can be 1000 times worse. PVC twisted pairs have terrible losses at high data rates (> 100 kbs), and greatly reduce the maximum cable length. At low data rates however, they are acceptable and much more economical.

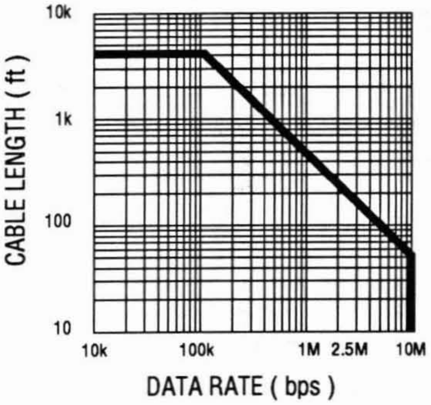


Figure 3 Cable Length - vs - Data Rate

CABLE TERMINATION

The proper termination of the cable is very important. If the cable is not terminated with it's characteristic impedance, distorted waveforms will result. In severe cases, distorted (false) data and nulls will occur. A quick look at the output of the driver will tell how well the cable is terminated. It is best to look at a driver connected to the end of the cable, since this eliminates the possibility of getting reflections from two directions. Simply look at the driver output while transmitting square wave data. If the cable is terminated properly, the waveform will look like a square wave (Figure 4).

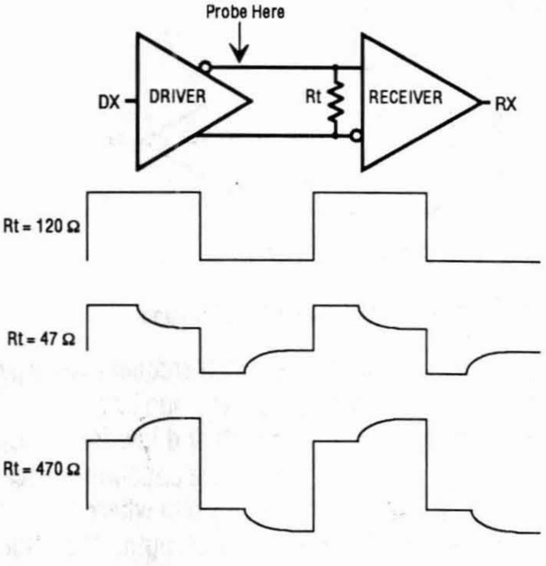


Figure 4 Termination Effects

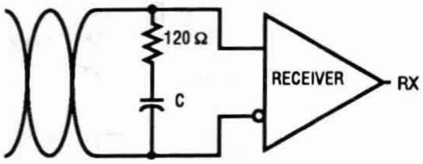
If the cable is loaded excessively (47 Ω), the signalinitially sees the surge impedance of the cable and jumps to an initial amplitude. The signal travels down the cable and is reflected back out of phase because of the mistermination. When the reflected signal returns to the driver, the amplitude will be lowered. The width of the

APPLICATIONS INFORMATION

pedestal is equal to twice the electrical length of the cable (about 1.5 ns / foot) . If the cable is lightly loaded (470 Ω), the signal reflects in phase and increases the amplitude at the driver output. An input frequency of 30 kHz is adequate for tests out to 4000 ft. of cable.

AC CABLE TERMINATION

Cable termination resistors are necessary to prevent unwanted reflections, but they consume power. The typical differential output voltage of the driver is 2 V when the cable is terminated with two 120 Ω resistors, causing 33 mA of DC current to flow in the cable when no data is being sent. This DC current is about10 times greater than the supply current of the LTC1485. One way to eliminate the unwanted current is by AC coupling the termination resistors as shown in Figure 5.



C = Line Length (ft) x 16.3 pF

Figure 5 AC Coupled Termination

The coupling capacitor must allow high-frequency energy to flow to the termination, but block DC and low frequencies. The dividing line between high and low frequency depends on the length of the cable. The coupling capacitor must pass frequencies above the point where the line represents an electrical one-tenth wavelength. The value of the coupling capacitor should therefore be set at 16.3 pF per foot of cable length for 120 Ω cables. With the coupling capacitors in place, power is consumed only on the signal edges, and not when the driver output is idling at a 1 or 0 state. A 100 nF capacitor is adequate for lines up to 4000 ' in length. Be aware that the power savings start to decrease once the data rate surpasses 1/(120 Ω x C).

RECEIVER OPEN-CIRCUIT FAIL-SAFE

Some data encoding schemes require that the output of the receiver maintains a known state (usually a logic 1) when the data is finished transmitting and all drivers on the line are forced into tri-state. The receiver of the LTC1485 has a fail-safe feature which guarantees the output to be in a logic 1 state when the receiver inputs are left floating (open-circuit). However, when the cable is terminated with 120 Ω, the differential inputs to the receiver are shorted together, not left floating. Because the receiver has about 70 mV of hysteresis, the receiver output will maintain the last data bit received.

If the receiver output must be forced to a known state, the circuits of Figure. 6 can be used.

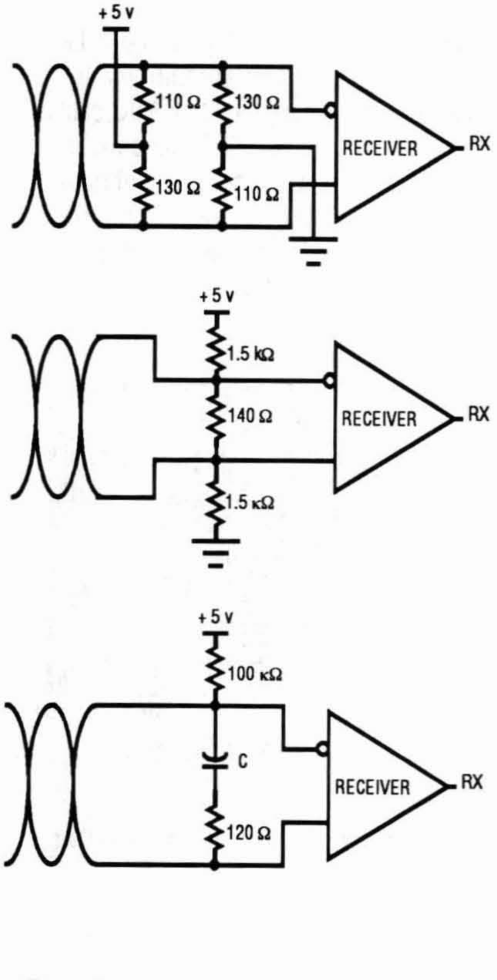


Figure 6. Forcing '0' When All Drivers Are Off

APPLICATIONS INFORMATION

The termination resistors are used to generate a DC bias which forces the receiver output to a known state, in this case a logic 0 .The first method consumes about 208 mW and the second about 8 mW. The lowest power solution is to use an AC termination with a pull-up resistor. Simply swap the receiver inputs for data protocols ending in logic 1.

FAULT PROTECTION

All of LTC's RS-485 products are protected against ESD transients up to 2 kV using the human body model (100 pF,1.5 kΩ). However, some applications need more protection. The best protection method is to connect a bidirectional TransZorb from each line side pin to ground (Figure 7).

A TransZorb is a silicon transient voltage suppressor that has exceptional surge handling capabilities, fast response time, and low series resistance. They are available from General Semiconductor Industries and come in a variety of breakdown voltages and prices. Be sure to pick a breakdown voltage higher than the common mode voltage required for your application (typically 12 V). Also, don't forget to check how much the added parasitic capacitance will load down the bus.

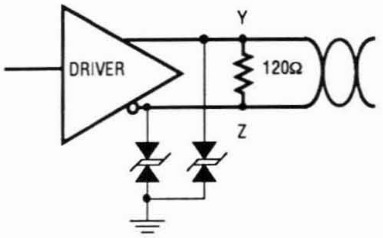
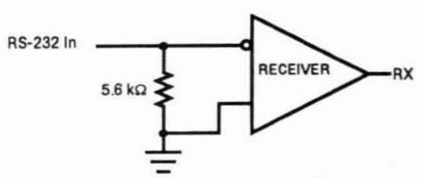


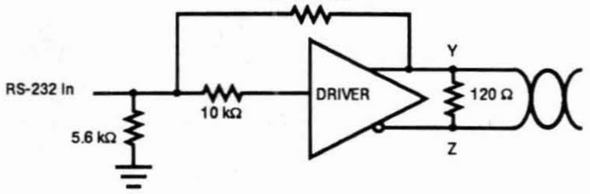
Figure 7. ESD Protection With TransZorbs

TYPICAL APPLICATIONS

RS-232 Receiver



RS-232 To RS-485 Level Translator With Hysteresis



Hysteresis = 10 kΩ * | Vy - Vz | / R = 19 k / R

NOTES

SECTION 14—PACKAGE DIMENSIONS

SECTION 14 - PACKAGE DIMENSIONS

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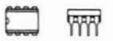
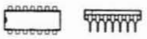
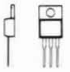
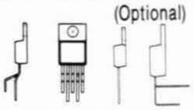
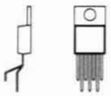
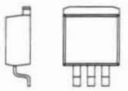
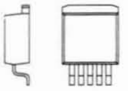
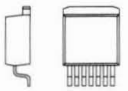
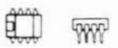
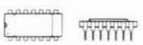
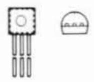
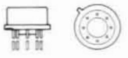
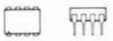
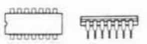
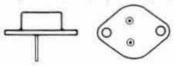
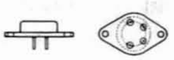
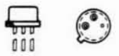
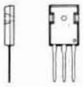
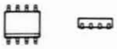
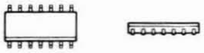
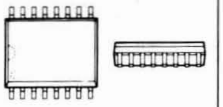
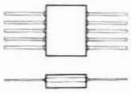
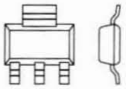
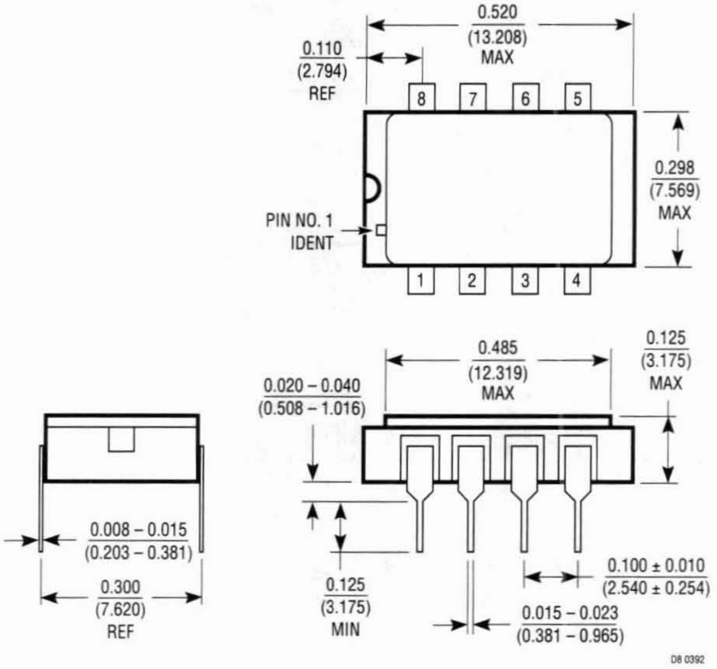
PACKAGE CROSS REFERENCE

		LTC	NSC	SIG	MOT	TI	SG	RAYTH	PMI	MAXIM
	Plastic DIP 8 Lead	N-8	N N-8	N	P1	P	M	P, NB	P	PA
	Plastic DIP 14, 16, 18, 20, 24, and 28 Lead	N	N N-14	N	P2	N NE NG	N	P, N	P	PD, PE, PN, PP, PG, PI
	TO-220 3 Lead	T	T	—	T	KC	P	—	—	AR
	TO-220 5 Lead	T	T	—	—	KV	P	—	—	—
	TO-220 7 Lead	Y	—	—	—	—	—	—	—	—
	Plastic DD 3 Lead	M	—	—	—	—	—	—	—	—
	Plastic DD 5 Lead	Q	—	—	—	—	—	—	—	—
	Plastic DD 7 Lead	R	—	—	—	—	—	—	—	—
	Side Brazed Hermetic DIP 8 Lead	D-8	D	I	L	—	—	—	—	DA
	Side Brazed Hermetic DIP 14, 16, 18 and 20 Lead	D	D	I	L	—	—	—	YB QB XB	DD, DE, DN, DP
	TO-92 3 Lead	Z	Z	—	P	LP	—	—	—	ZR
	TO-5, TO-39, TO-96, TO-99, TO-100 and TO-101	H	H	—	G H	—	T	T H	H J K	VR, TA, TB
	Ceramic DIP 8 Lead	J-8	J J-8	F	U	JG	Y	DE	Z	JA
	Ceramic DIP 14, 16, 18, 20, 24, and 28 Lead	J	J J-14	F	L	J	J	DB DC J	Y Q X	JD, JE, JN, JP, JG, JI

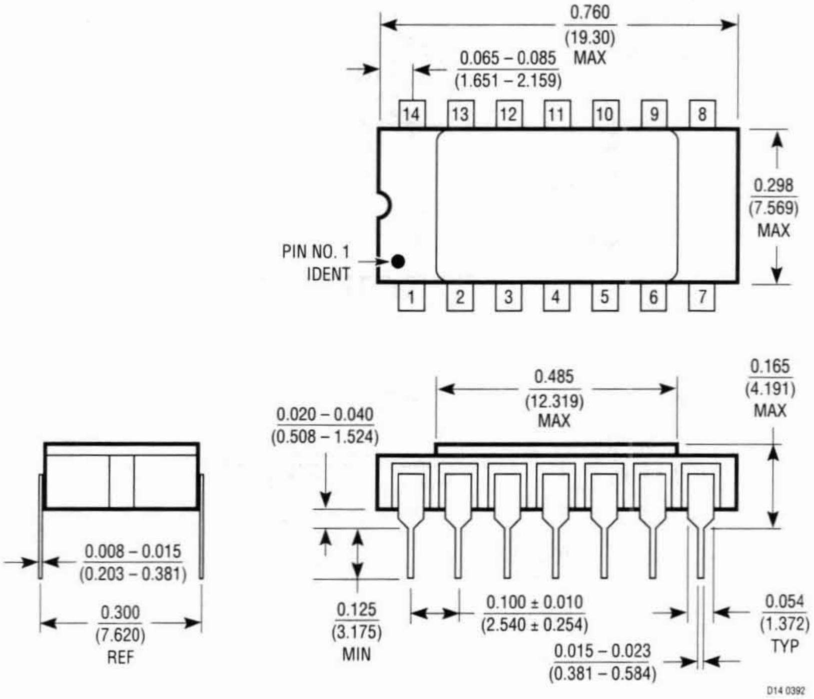
PACKAGE CROSS REFERENCE

		LTC	NSC	SIG	MOT	TI	SG	RAYTH	PMI	MAXIM
	TO-3 (Steel) 2 Lead	K	K Steel	—	K	—	K	—	—	KR
	(Aluminum)	—	K	—	K	—	—	—	—	KR
	TO-3 4 Lead	K	K	—	—	KJ	K	—	—	—
	TO-46 2, 3, 4 Lead	H	H	—	—	—	T	—		—
	TO -52 3 Lead									SR
	TO-3P 3 Lead	P	—	—	—	—	—	—	—	—
	Plastic SO 8 Lead	S-8	M	D	D	D	—	—	—	SA
	Plastic SO 14, 16 Lead	S	M	D	D	D	—	—	—	SD SE
	Plastic SOL 16, 18, 20, 24, 28 Lead	S	M	D	D	D	—	—	—	WE, WN, WP, WF, WG, WI
	10 Lead Cerpac	W	W	H	F	W	F	—	RC	—
	SOT-223 3 Lead	ST	—	—	—	—	—	—	—	—
PROPRIETARY DEVICE PREFIXES		LT LTC	LF LP LH MF LM	NE SE	MC	TL	SG	RM RC	OP REF CMP	MAX

D Package
8-Lead Sidebrazed

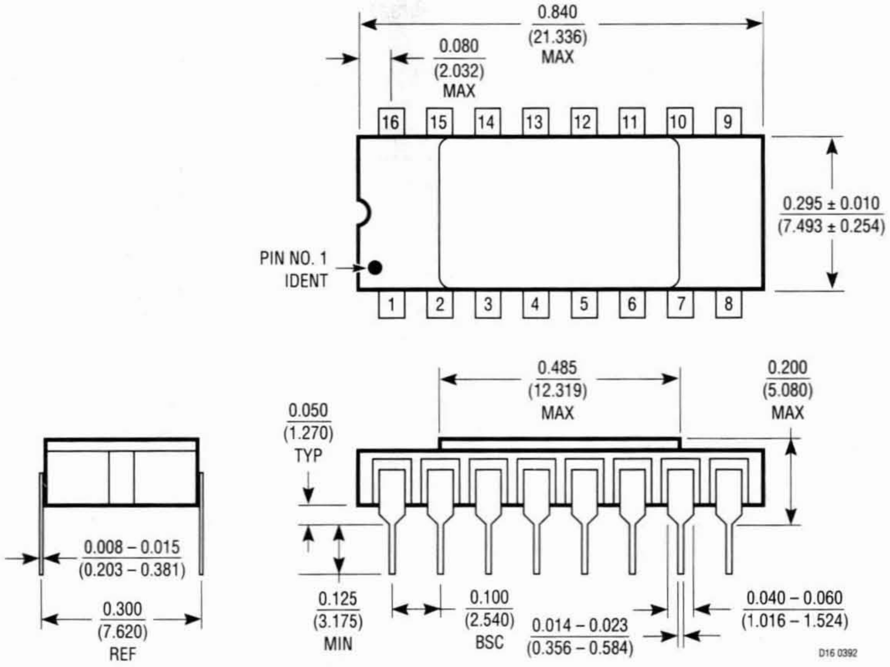

0.520
(13.208)
MAX
0.110
(2.794)
REF
8
7
6
5
0.298
(7.569)
MAX
PIN NO. 1
IDENT
1
2
3
4
0.485
(12.319)
MAX
0.125
(3.175)
MAX
0.020 – 0.040
(0.508 – 1.016)
0.008 – 0.015
(0.203 – 0.381)
0.300
(7.620)
REF
0.125
(3.175)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
0.015 – 0.023
(0.381 – 0.965)
D8 0392

D Package
14-Lead Sidebrazed

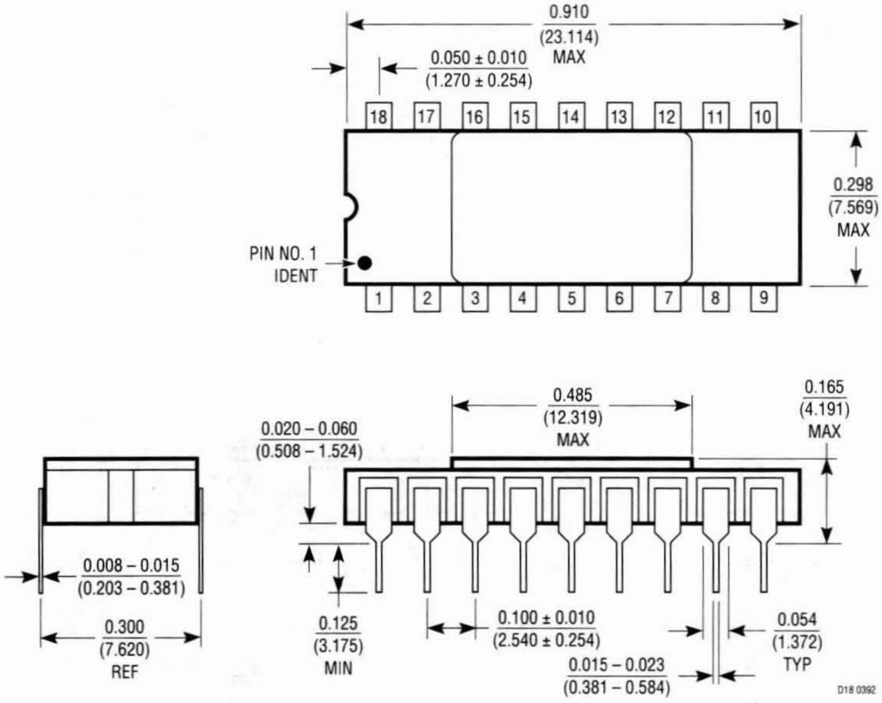

0.760
(19.30)
MAX
0.065 – 0.085
(1.651 – 2.159)
14
13
12
11
10
9
8
0.298
(7.569)
MAX
PIN NO. 1
IDENT
1
2
3
4
5
6
7
0.485
(12.319)
MAX
0.165
(4.191)
MAX
0.020 – 0.040
(0.508 – 1.524)
0.008 – 0.015
(0.203 – 0.381)
0.300
(7.620)
REF
0.125
(3.175)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
0.054
(1.372)
TYP
0.015 – 0.023
(0.381 – 0.584)
D14 0392

PACKAGE DIMENSIONS

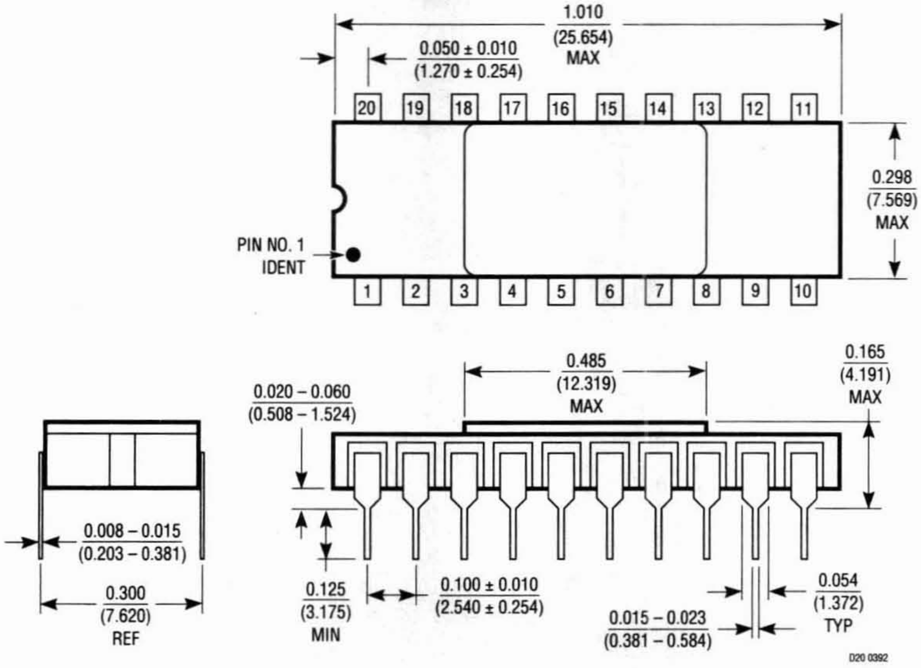
D Package
16-Lead Sidebrazed


0.840
(21.336)
MAX
0.080
(2.032)
MAX
16
15
14
13
12
11
10
9
0.295 ± 0.010
(7.493 ± 0.254)
PIN NO. 1
IDENT
1
2
3
4
5
6
7
8
0.485
(12.319)
MAX
0.200
(5.080)
MAX
0.050
(1.270)
TYP
0.008 – 0.015
(0.203 – 0.381)
0.300
(7.620)
REF
0.125
(3.175)
MIN
0.100
(2.540)
BSC
0.014 – 0.023
(0.356 – 0.584)
0.040 – 0.060
(1.016 – 1.524)
D16 0392

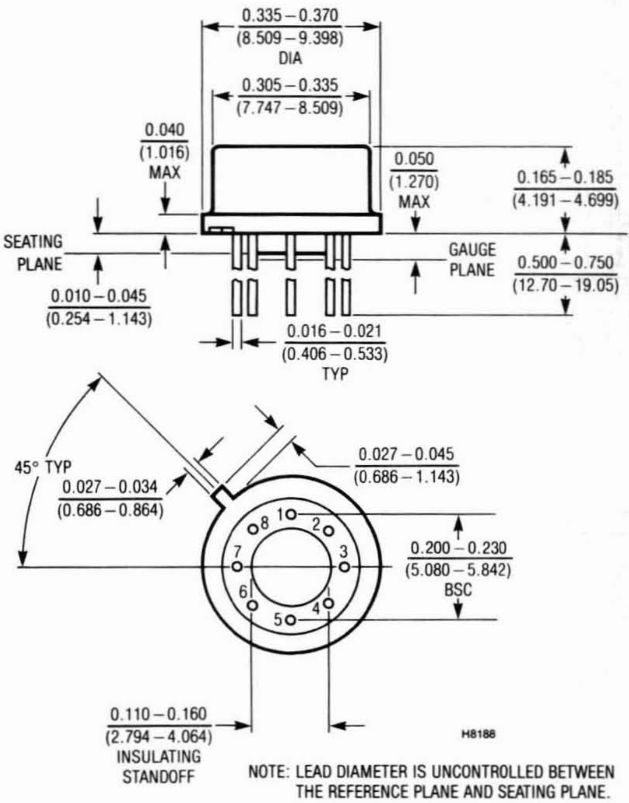
D Package
18-Lead Sidebrazed


0.910
(23.114)
MAX
0.050 ± 0.010
(1.270 ± 0.254)
18
17
16
15
14
13
12
11
10
0.298
(7.569)
MAX
PIN NO. 1
IDENT
1
2
3
4
5
6
7
8
9
0.485
(12.319)
MAX
0.165
(4.191)
MAX
0.020 – 0.060
(0.508 – 1.524)
0.008 – 0.015
(0.203 – 0.381)
0.300
(7.620)
REF
0.125
(3.175)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
0.015 – 0.023
(0.381 – 0.584)
0.054
(1.372)
TYP
D18 0392

D Package
20-Lead Sidebrazed

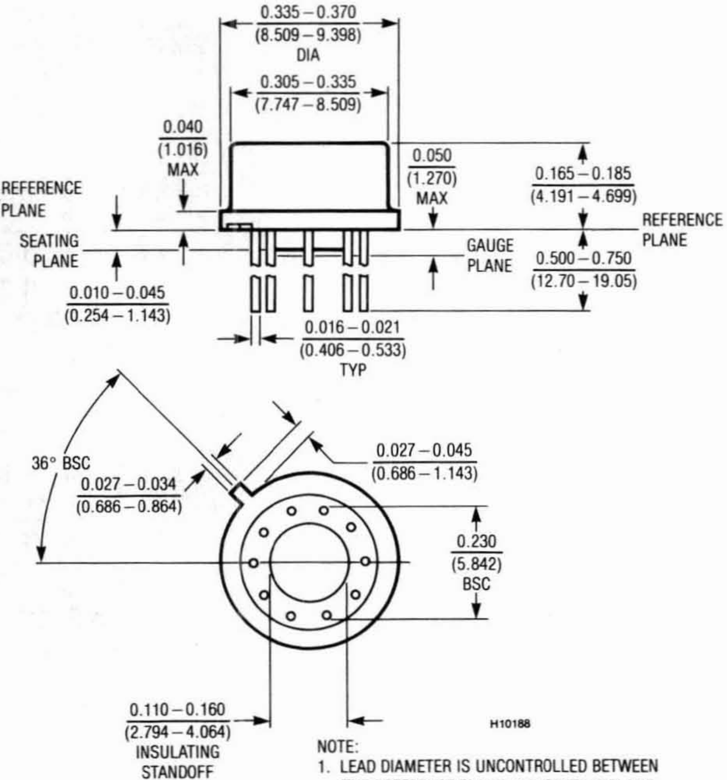

1.010
(25.654)
MAX
0.050 ± 0.010
(1.270 ± 0.254)
20 19 18 17 16 15 14 13 12 11
1 2 3 4 5 6 7 8 9 10
PIN NO. 1
IDENT
0.298
(7.569)
MAX
0.485
(12.319)
MAX
0.165
(4.191)
MAX
0.020 – 0.060
(0.508 – 1.524)
0.008 – 0.015
(0.203 – 0.381)
0.300
(7.620)
REF
0.125
(3.175)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
0.054
(1.372)
TYP
0.015 – 0.023
(0.381 – 0.584)
D20 0392

H Package
8-Lead TO-5 Metal Can


0.335 – 0.370
(8.509 – 9.398)
DIA
0.305 – 0.335
(7.747 – 8.509)
0.040
(1.016)
MAX
0.050
(1.270)
MAX
0.165 – 0.185
(4.191 – 4.699)
REFERENCE
PLANE
SEATING
PLANE
GAUGE
PLANE
0.500 – 0.750
(12.70 – 19.05)
0.010 – 0.045
(0.254 – 1.143)
0.016 – 0.021
(0.406 – 0.533)
TYP
45° TYP
0.027 – 0.034
(0.686 – 0.864)
0.027 – 0.045
(0.686 – 1.143)
1 2 3 4 5 6 7 8
0.200 – 0.230
(5.080 – 5.842)
BSC
0.110 – 0.160
(2.794 – 4.064)
INSULATING
STANDOFF
H8188

NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

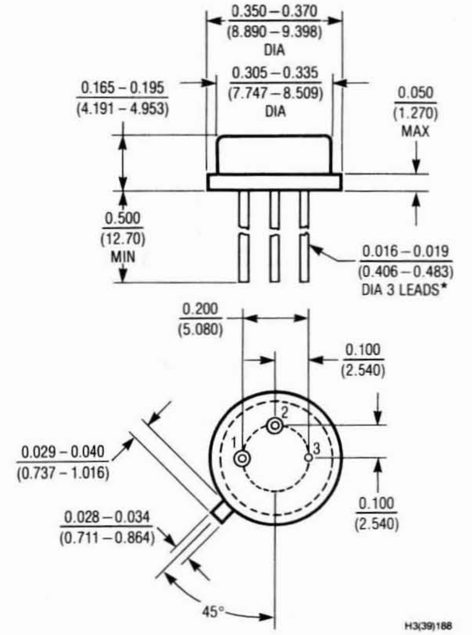
H Package
10-Lead TO-5 Metal Can


0.335 – 0.370
(8.509 – 9.398)
DIA
0.305 – 0.335
(7.747 – 8.509)
0.040
(1.016)
MAX
0.050
(1.270)
MAX
0.165 – 0.185
(4.191 – 4.699)
REFERENCE
PLANE
SEATING
PLANE
GAUGE
PLANE
0.500 – 0.750
(12.70 – 19.05)
0.010 – 0.045
(0.254 – 1.143)
0.016 – 0.021
(0.406 – 0.533)
TYP
36° BSC
0.027 – 0.034
(0.686 – 0.864)
0.027 – 0.045
(0.686 – 1.143)
0.230
(5.842)
BSC
0.110 – 0.160
(2.794 – 4.064)
INSULATING
STANDOFF
H10188

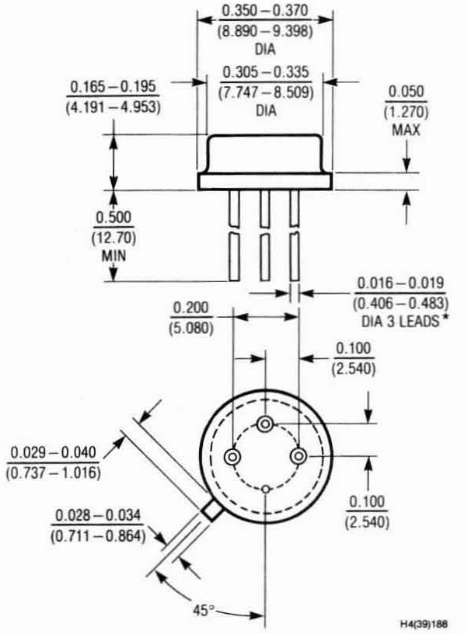
NOTE:
1. LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.

PACKAGE DIMENSIONS

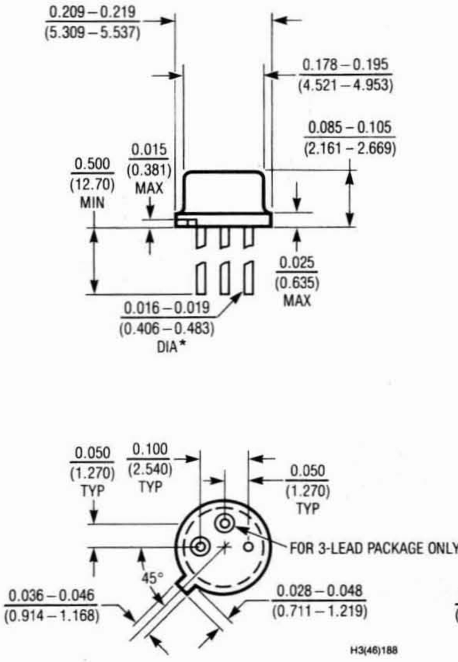
H Package
3-Lead TO-39 Metal Can


0.350 – 0.370
(8.890 – 9.398)
DIA
0.305 – 0.335
(7.747 – 8.509)
DIA
0.165 – 0.195
(4.191 – 4.953)
0.050
(1.270)
MAX
0.500
(12.70)
MIN
0.016 – 0.019
(0.406 – 0.483)
DIA 3 LEADS*
0.200
(5.080)
0.100
(2.540)
2
1
3
0.029 – 0.040
(0.737 – 1.016)
0.028 – 0.034
(0.711 – 0.864)
0.100
(2.540)
45°
H3(39)188

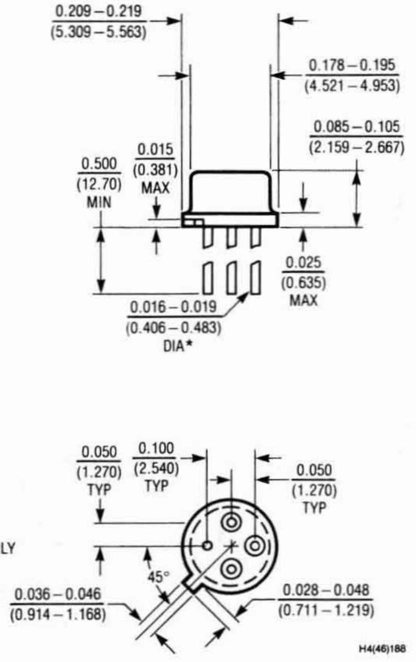
H Package
4-Lead TO-39 Metal Can


0.350 – 0.370
(8.890 – 9.398)
DIA
0.305 – 0.335
(7.747 – 8.509)
DIA
0.165 – 0.195
(4.191 – 4.953)
0.050
(1.270)
MAX
0.500
(12.70)
MIN
0.016 – 0.019
(0.406 – 0.483)
DIA 3 LEADS*
0.200
(5.080)
0.100
(2.540)
0.029 – 0.040
(0.737 – 1.016)
0.028 – 0.034
(0.711 – 0.864)
0.100
(2.540)
45°
H4(39)188

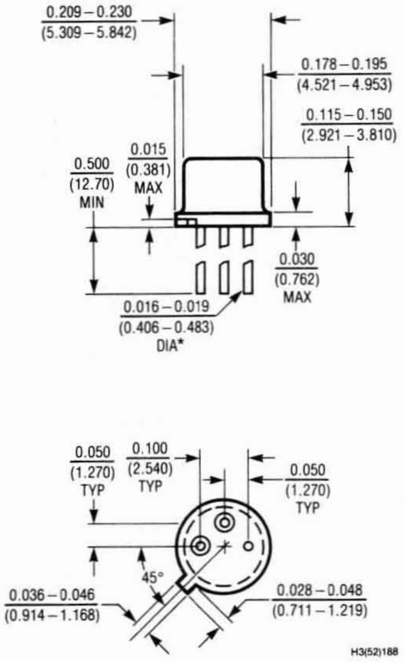
H Package
2-Lead and 3-Lead TO-46 Metal Can


0.209 – 0.219
(5.309 – 5.537)
0.178 – 0.195
(4.521 – 4.953)
0.085 – 0.105
(2.161 – 2.669)
0.500
(12.70)
MIN
0.015
(0.381)
MAX
0.025
(0.635)
MAX
0.016 – 0.019
(0.406 – 0.483)
DIA*
0.050
(1.270)
TYP
0.100
(2.540)
TYP
0.050
(1.270)
TYP
FOR 3-LEAD PACKAGE ONLY
45°
0.036 – 0.046
(0.914 – 1.168)
0.028 – 0.048
(0.711 – 1.219)
H3(46)188

H Package
4-Lead TO-46 Metal Can

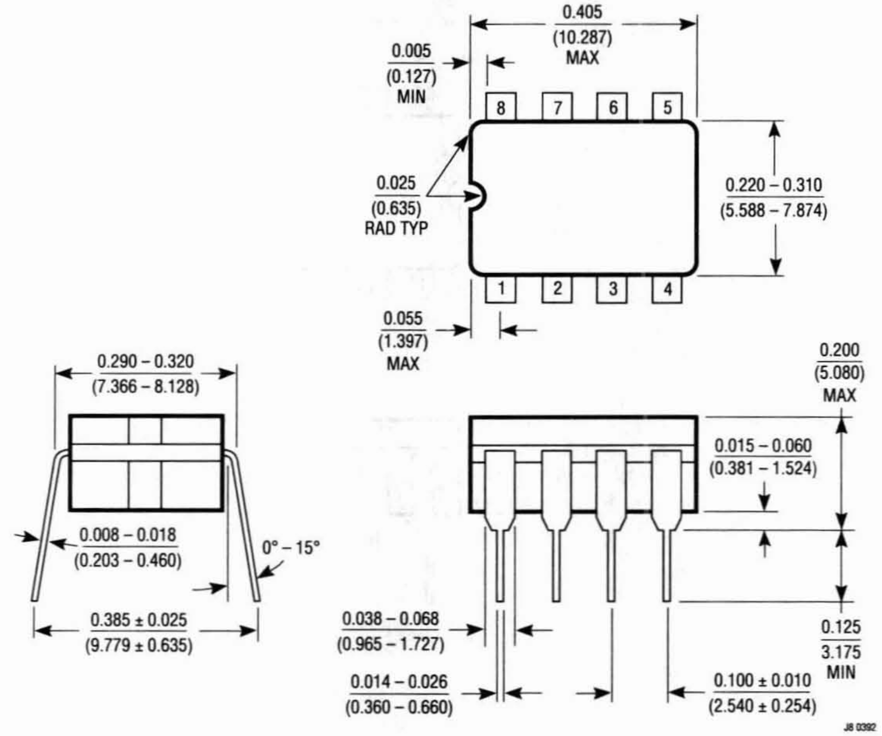

0.209 – 0.219
(5.309 – 5.563)
0.178 – 0.195
(4.521 – 4.953)
0.085 – 0.105
(2.159 – 2.667)
0.500
(12.70)
MIN
0.015
(0.381)
MAX
0.025
(0.635)
MAX
0.016 – 0.019
(0.406 – 0.483)
DIA*
0.050
(1.270)
TYP
0.100
(2.540)
TYP
0.050
(1.270)
TYP
45°
0.036 – 0.046
(0.914 – 1.168)
0.028 – 0.048
(0.711 – 1.219)
H4(46)188

H Package
3-Lead TO-52 Metal Can

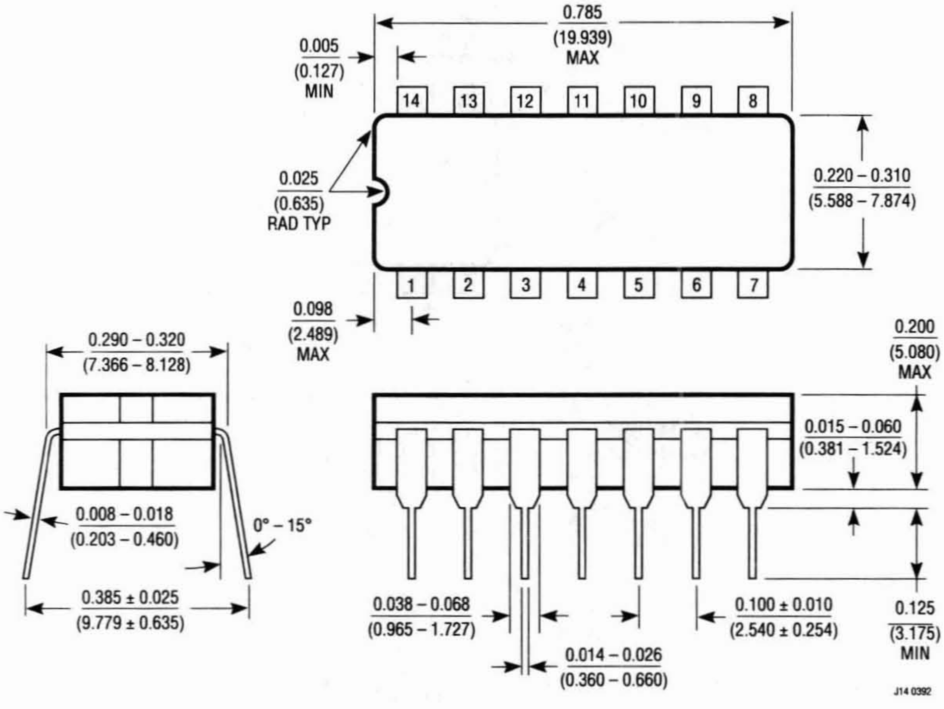

0.209 – 0.230
(5.309 – 5.842)
0.178 – 0.195
(4.521 – 4.953)
0.115 – 0.150
(2.921 – 3.810)
0.500
(12.70)
MIN
0.015
(0.381)
MAX
0.030
(0.762)
MAX
0.016 – 0.019
(0.406 – 0.483)
DIA*
0.050
(1.270)
TYP
0.100
(2.540)
TYP
0.050
(1.270)
TYP
45°
0.036 – 0.046
(0.914 – 1.168)
0.028 – 0.048
(0.711 – 1.219)
H3(52)188

* FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

J Package
8-Lead Cerdip

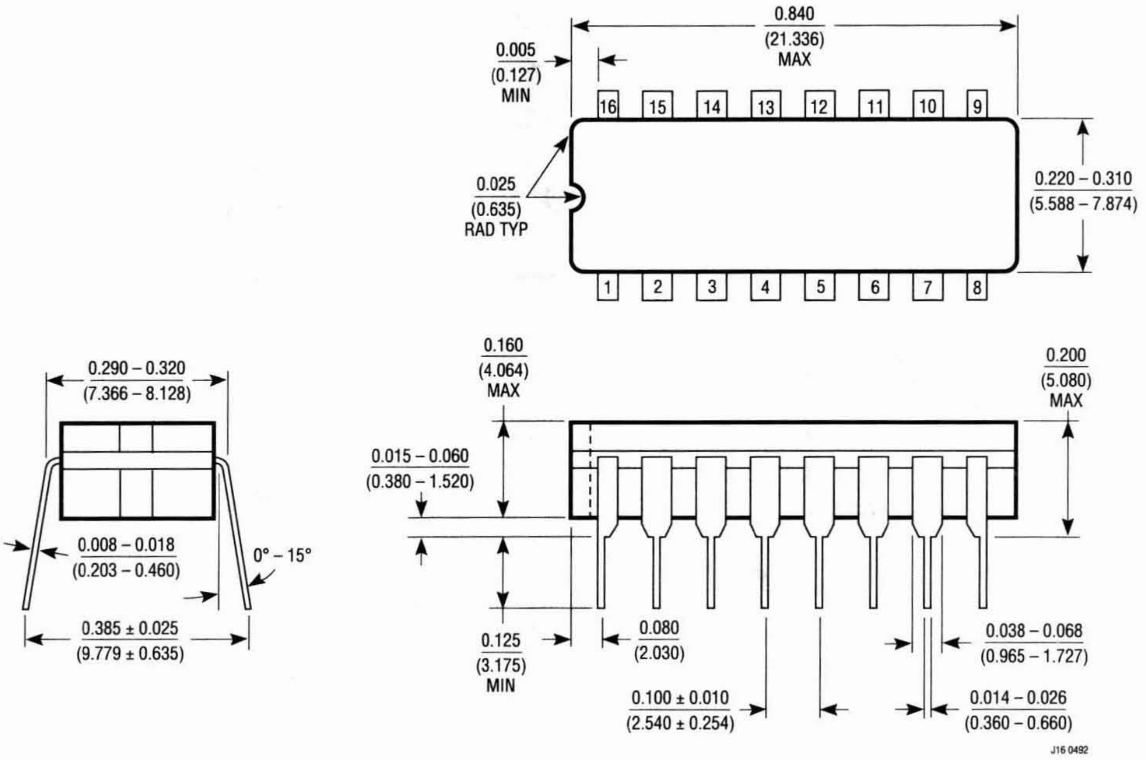

0.405
(10.287)
MAX
0.005
(0.127)
MIN
8
7
6
5
0.025
(0.635)
RAD TYP
0.220 – 0.310
(5.588 – 7.874)
1
2
3
4
0.055
(1.397)
MAX
0.290 – 0.320
(7.366 – 8.128)
0.200
(5.080)
MAX
0.015 – 0.060
(0.381 – 1.524)
0.008 – 0.018
(0.203 – 0.460)
0° – 15°
0.385 ± 0.025
(9.779 ± 0.635)
0.038 – 0.068
(0.965 – 1.727)
0.125
3.175
MIN
0.014 – 0.026
(0.360 – 0.660)
0.100 ± 0.010
(2.540 ± 0.254)
J8 0392

J Package
14-Lead Cerdip


0.785
(19.939)
MAX
0.005
(0.127)
MIN
14
13
12
11
10
9
8
0.025
(0.635)
RAD TYP
0.220 – 0.310
(5.588 – 7.874)
1
2
3
4
5
6
7
0.098
(2.489)
MAX
0.290 – 0.320
(7.366 – 8.128)
0.200
(5.080)
MAX
0.015 – 0.060
(0.381 – 1.524)
0.008 – 0.018
(0.203 – 0.460)
0° – 15°
0.385 ± 0.025
(9.779 ± 0.635)
0.038 – 0.068
(0.965 – 1.727)
0.100 ± 0.010
(2.540 ± 0.254)
0.125
(3.175)
MIN
0.014 – 0.026
(0.360 – 0.660)
J14 0392

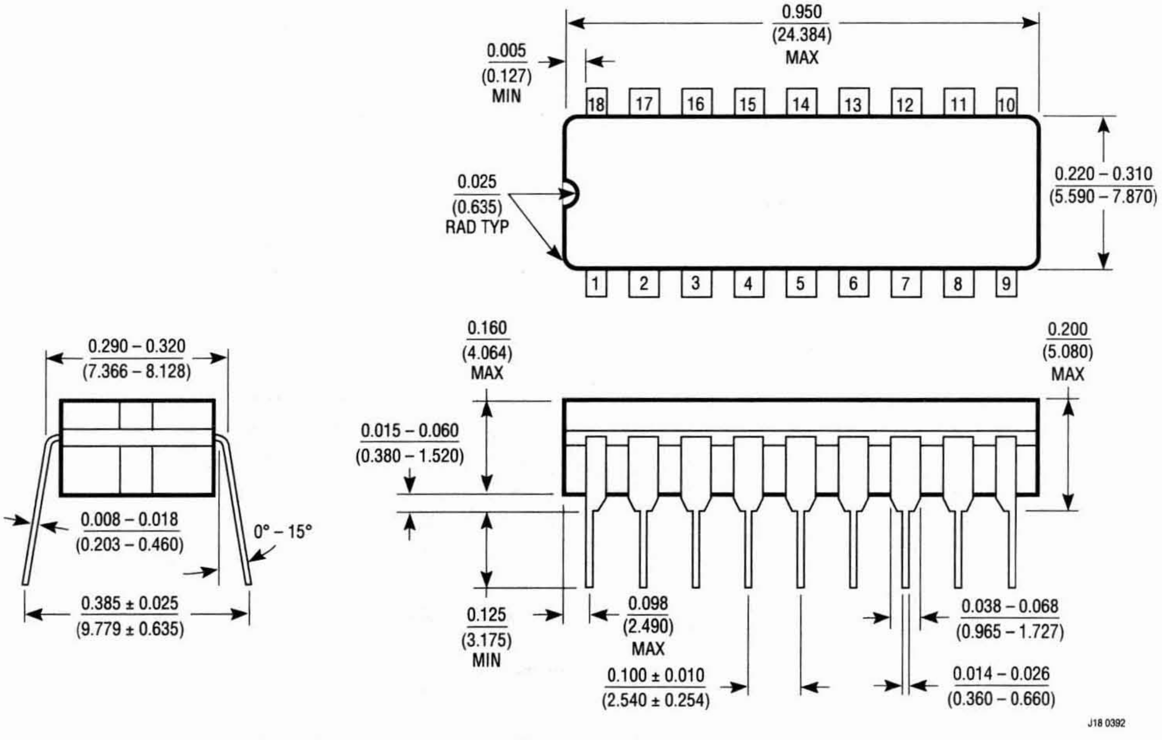
PACKAGE DIMENSIONS

J Package
16-Lead Cerdip



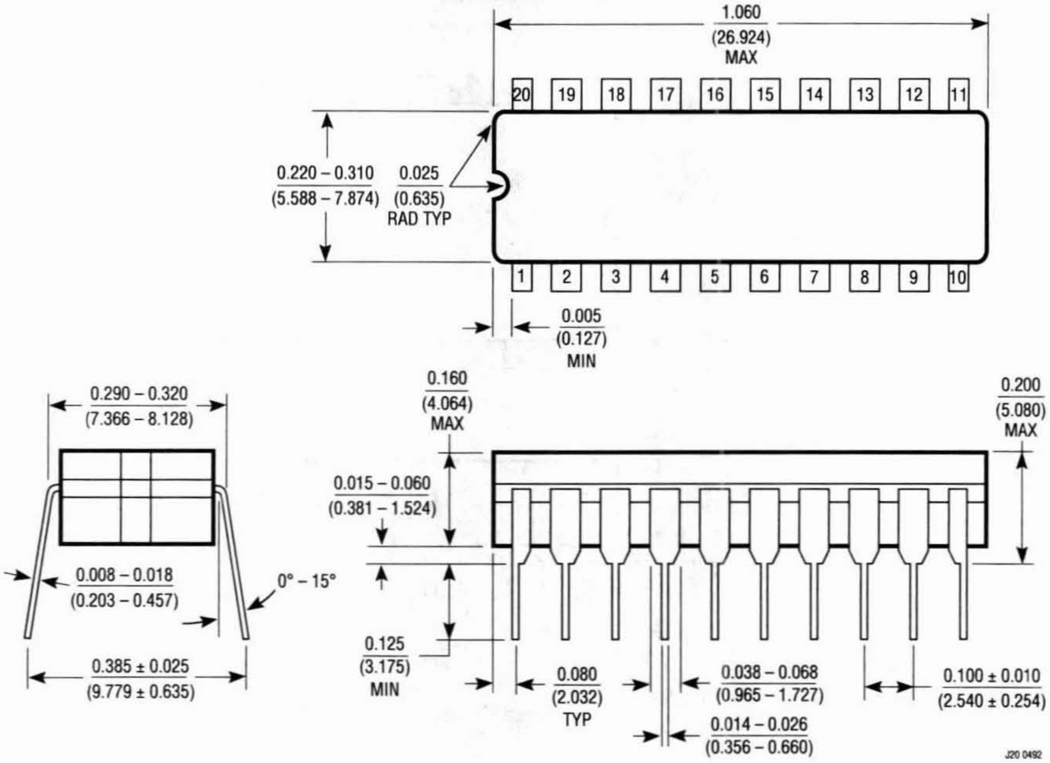
0.840
(21.336)
MAX
0.005
(0.127)
MIN
16
15
14
13
12
11
10
9
0.025
(0.635)
RAD TYP
0.220 – 0.310
(5.588 – 7.874)
1
2
3
4
5
6
7
8
0.290 – 0.320
(7.366 – 8.128)
0.160
(4.064)
MAX
0.200
(5.080)
MAX
0.015 – 0.060
(0.380 – 1.520)
0.008 – 0.018
(0.203 – 0.460)
0° – 15°
0.385 ± 0.025
(9.779 ± 0.635)
0.125
(3.175)
MIN
0.080
(2.030)
0.038 – 0.068
(0.965 – 1.727)
0.100 ± 0.010
(2.540 ± 0.254)
0.014 – 0.026
(0.360 – 0.660)
J16 0492

J Package
18-Lead Cerdip

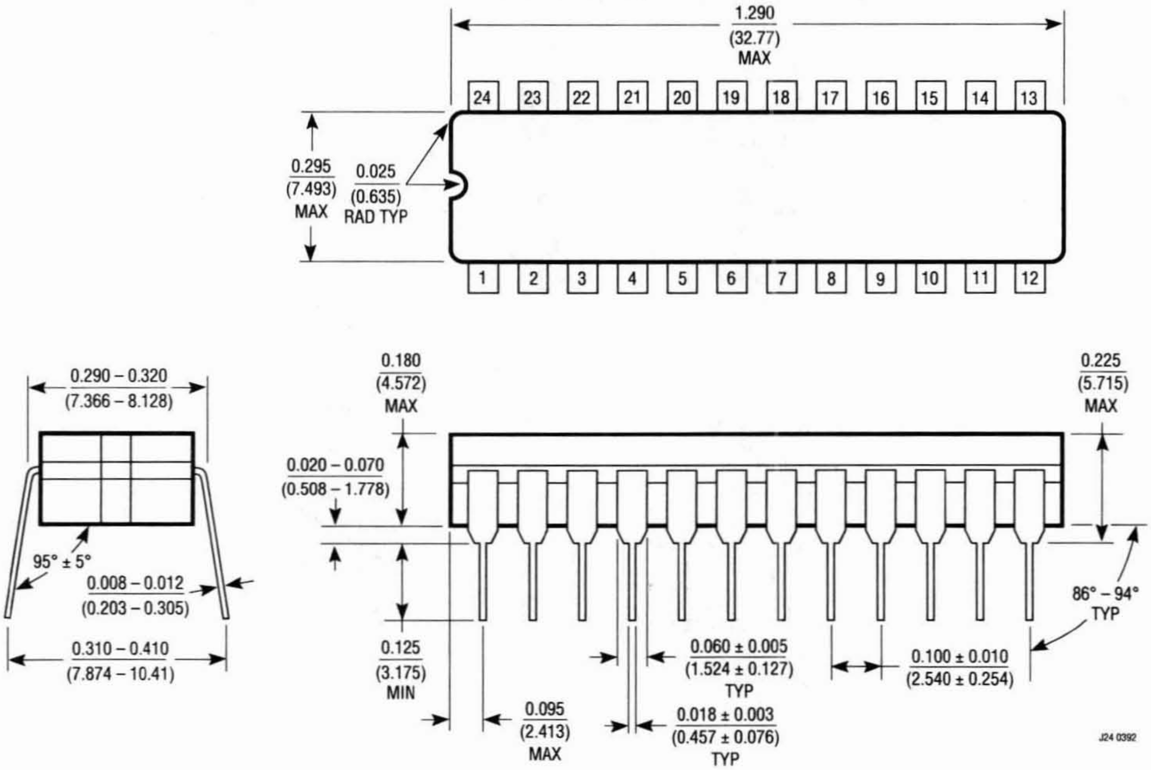


0.950
(24.384)
MAX
0.005
(0.127)
MIN
18
17
16
15
14
13
12
11
10
0.025
(0.635)
RAD TYP
0.220 – 0.310
(5.590 – 7.870)
1
2
3
4
5
6
7
8
9
0.290 – 0.320
(7.366 – 8.128)
0.160
(4.064)
MAX
0.200
(5.080)
MAX
0.015 – 0.060
(0.380 – 1.520)
0.008 – 0.018
(0.203 – 0.460)
0° – 15°
0.385 ± 0.025
(9.779 ± 0.635)
0.125
(3.175)
MIN
0.098
(2.490)
MAX
0.038 – 0.068
(0.965 – 1.727)
0.100 ± 0.010
(2.540 ± 0.254)
0.014 – 0.026
(0.360 – 0.660)
J18 0392

J Package
20-Lead Cerdip

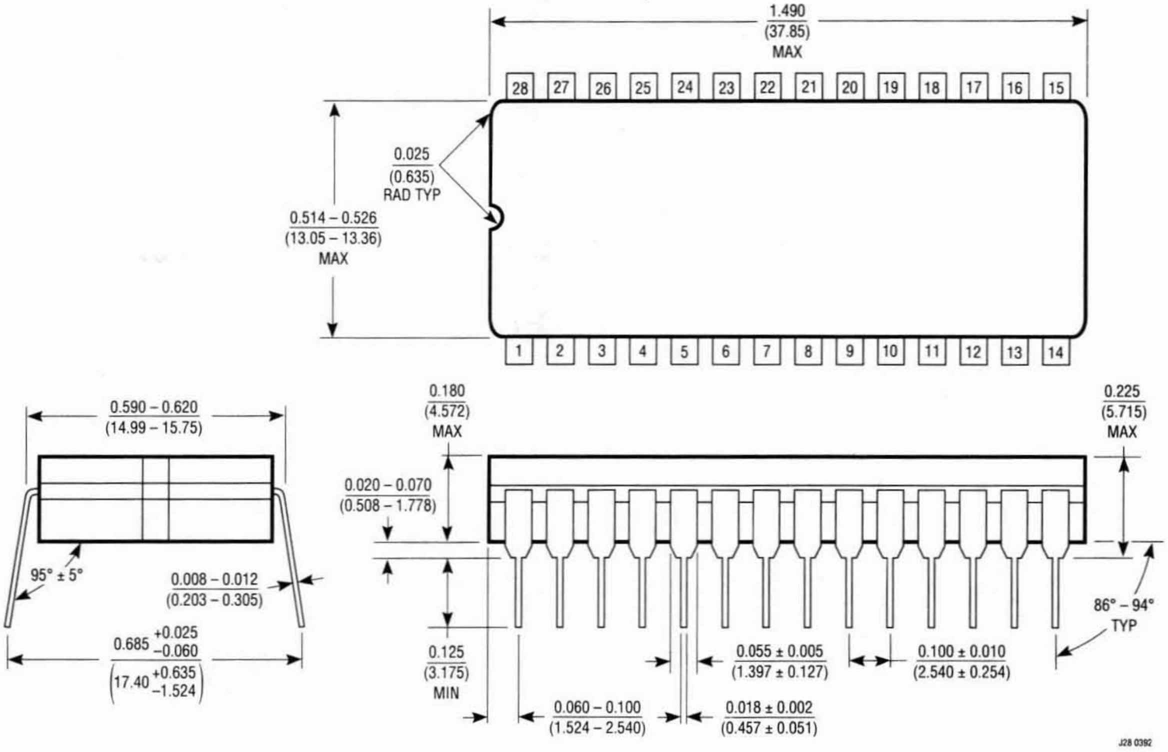

1.060
(26.924)
MAX
20
19
18
17
16
15
14
13
12
11
0.220 – 0.310
(5.588 – 7.874)
0.025
(0.635)
RAD TYP
1
2
3
4
5
6
7
8
9
10
0.005
(0.127)
MIN
0.290 – 0.320
(7.366 – 8.128)
0.160
(4.064)
MAX
0.200
(5.080)
MAX
0.015 – 0.060
(0.381 – 1.524)
0.008 – 0.018
(0.203 – 0.457)
0° – 15°
0.125
(3.175)
MIN
0.385 ± 0.025
(9.779 ± 0.635)
0.080
(2.032)
TYP
0.038 – 0.068
(0.965 – 1.727)
0.100 ± 0.010
(2.540 ± 0.254)
0.014 – 0.026
(0.356 – 0.660)
J20 0492

J Package
24-Lead Cerdip

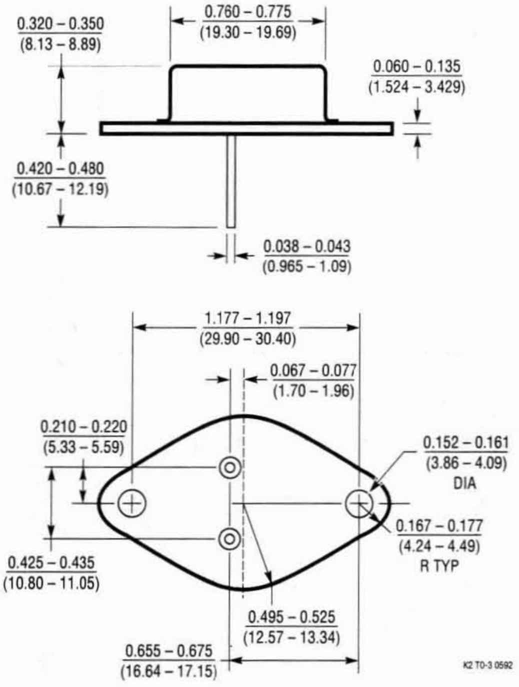

1.290
(32.77)
MAX
24
23
22
21
20
19
18
17
16
15
14
13
0.295
(7.493)
MAX
0.025
(0.635)
RAD TYP
1
2
3
4
5
6
7
8
9
10
11
12
0.290 – 0.320
(7.366 – 8.128)
0.180
(4.572)
MAX
0.225
(5.715)
MAX
0.020 – 0.070
(0.508 – 1.778)
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
0.310 – 0.410
(7.874 – 10.41)
0.125
(3.175)
MIN
86° – 94°
TYP
0.060 ± 0.005
(1.524 ± 0.127)
TYP
0.100 ± 0.010
(2.540 ± 0.254)
0.095
(2.413)
MAX
0.018 ± 0.003
(0.457 ± 0.076)
TYP
J24 0392

PACKAGE DIMENSIONS

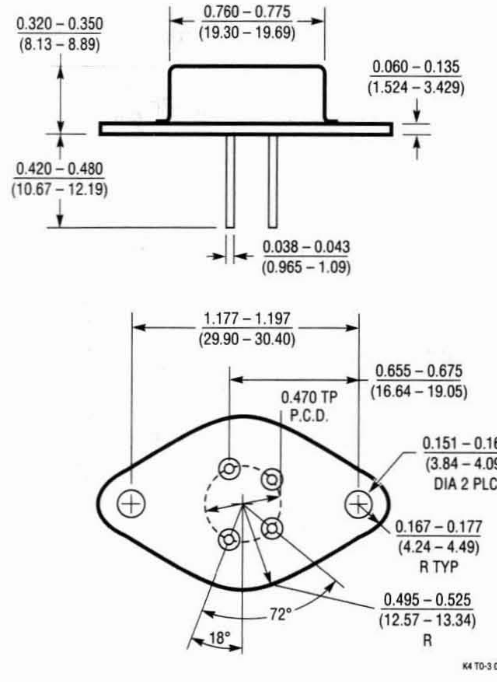
J Package
28-Lead Cerdip


1.490
(37.85)
MAX
28 27 26 25 24 23 22 21 20 19 18 17 16 15
0.025
(0.635)
RAD TYP
0.514 – 0.526
(13.05 – 13.36)
MAX
1 2 3 4 5 6 7 8 9 10 11 12 13 14
0.590 – 0.620
(14.99 – 15.75)
95° ± 5°
0.008 – 0.012
(0.203 – 0.305)
0.685 +0.025 −0.060
(17.40 +0.635 −1.524)
0.180
(4.572)
MAX
0.020 – 0.070
(0.508 – 1.778)
0.125
(3.175)
MIN
0.060 – 0.100
(1.524 – 2.540)
0.055 ± 0.005
(1.397 ± 0.127)
0.018 ± 0.002
(0.457 ± 0.051)
0.100 ± 0.010
(2.540 ± 0.254)
0.225
(5.715)
MAX
86° – 94°
TYP
J28 0392

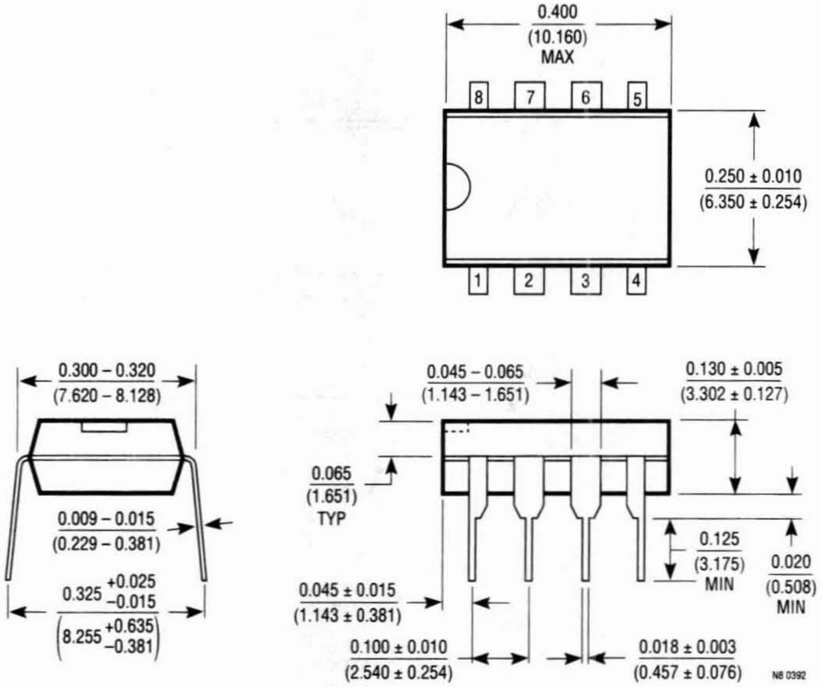
K Package
2-Lead TO-3 Metal Can


0.320 – 0.350
(8.13 – 8.89)
0.760 – 0.775
(19.30 – 19.69)
0.060 – 0.135
(1.524 – 3.429)
0.420 – 0.480
(10.67 – 12.19)
0.038 – 0.043
(0.965 – 1.09)
1.177 – 1.197
(29.90 – 30.40)
0.067 – 0.077
(1.70 – 1.96)
0.210 – 0.220
(5.33 – 5.59)
0.152 – 0.161
(3.86 – 4.09)
DIA
0.167 – 0.177
(4.24 – 4.49)
R TYP
0.425 – 0.435
(10.80 – 11.05)
0.495 – 0.525
(12.57 – 13.34)
0.655 – 0.675
(16.64 – 17.15)
K2 TO-3 0592

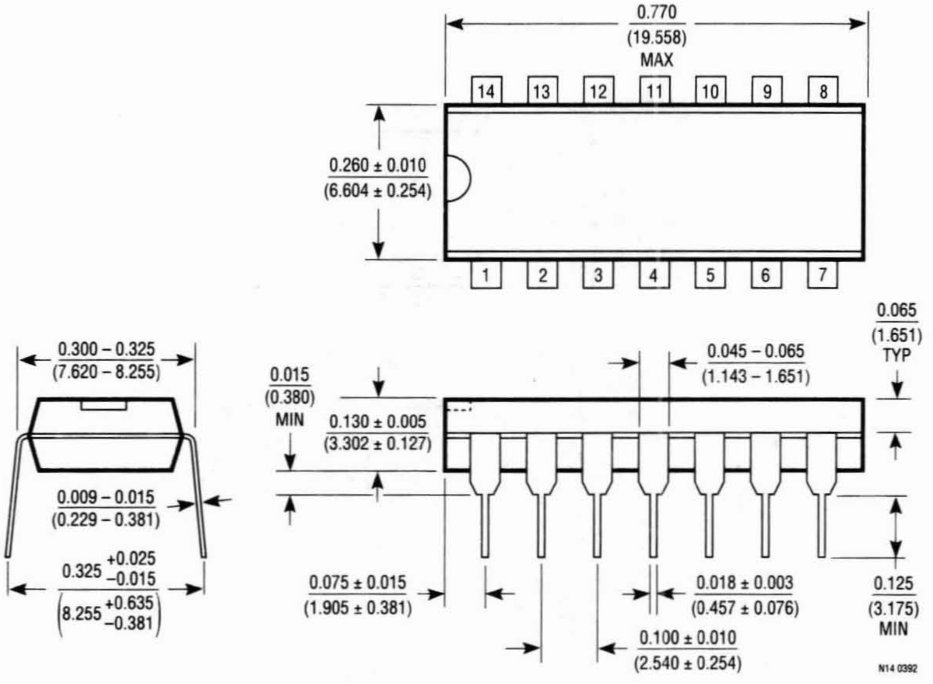
K Package
4-Lead TO-3 Metal Can


0.320 – 0.350
(8.13 – 8.89)
0.760 – 0.775
(19.30 – 19.69)
0.060 – 0.135
(1.524 – 3.429)
0.420 – 0.480
(10.67 – 12.19)
0.038 – 0.043
(0.965 – 1.09)
1.177 – 1.197
(29.90 – 30.40)
0.655 – 0.675
(16.64 – 19.05)
0.470 TP
P.C.D.
0.151 – 0.161
(3.84 – 4.09)
DIA 2 PLC
0.167 – 0.177
(4.24 – 4.49)
R TYP
72°
18°
0.495 – 0.525
(12.57 – 13.34)
R
K4 TO-3 0592

N Package
8-Lead Molded DIP

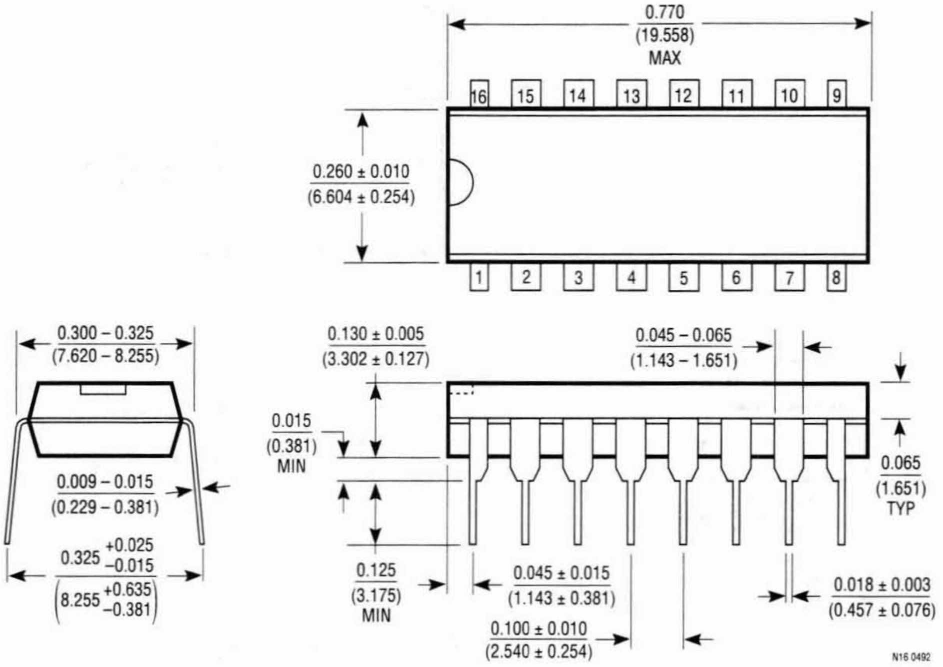

0.400
(10.160)
MAX
8
7
6
5
1
2
3
4
0.250 ± 0.010
(6.350 ± 0.254)
0.300 – 0.320
(7.620 – 8.128)
0.009 – 0.015
(0.229 – 0.381)
0.325 +0.025 −0.015
(8.255 +0.635 −0.381)
0.045 – 0.065
(1.143 – 1.651)
0.130 ± 0.005
(3.302 ± 0.127)
0.065
(1.651)
TYP
0.125
(3.175)
MIN
0.020
(0.508)
MIN
0.045 ± 0.015
(1.143 ± 0.381)
0.100 ± 0.010
(2.540 ± 0.254)
0.018 ± 0.003
(0.457 ± 0.076)
N8 0392

N Package
14-Lead Molded DIP

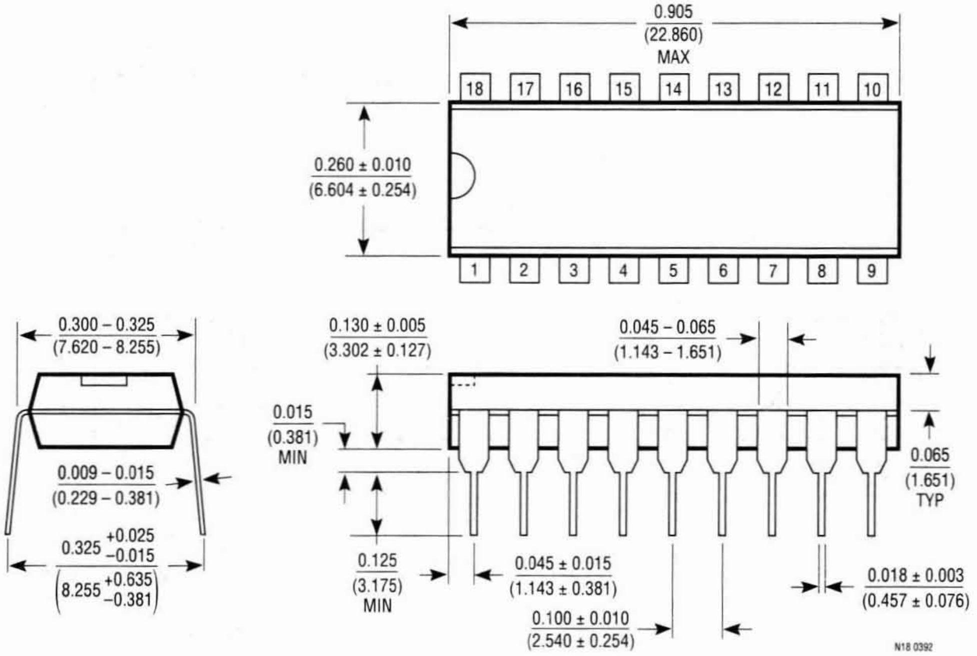

0.770
(19.558)
MAX
14
13
12
11
10
9
8
1
2
3
4
5
6
7
0.260 ± 0.010
(6.604 ± 0.254)
0.300 – 0.325
(7.620 – 8.255)
0.009 – 0.015
(0.229 – 0.381)
0.325 +0.025 −0.015
(8.255 +0.635 −0.381)
0.015
(0.380)
MIN
0.130 ± 0.005
(3.302 ± 0.127)
0.045 – 0.065
(1.143 – 1.651)
0.065
(1.651)
TYP
0.075 ± 0.015
(1.905 ± 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.125
(3.175)
MIN
0.100 ± 0.010
(2.540 ± 0.254)
N14 0392

PACKAGE DIMENSIONS

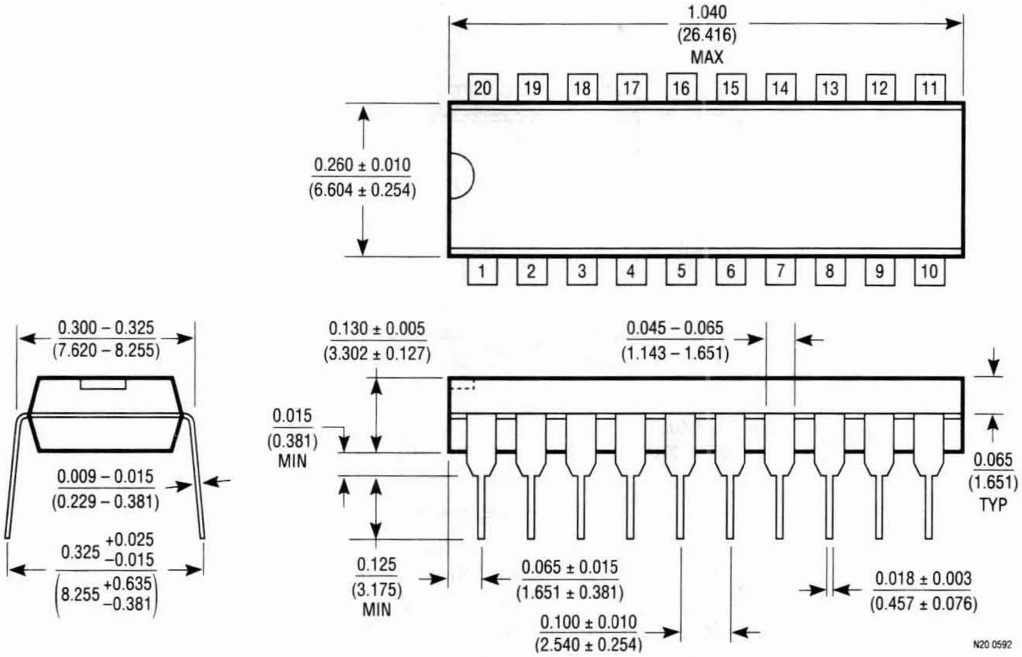
N Package
16-Lead Molded DIP


0.770
(19.558)
MAX
16
15
14
13
12
11
10
9
0.260 ± 0.010
(6.604 ± 0.254)
1
2
3
4
5
6
7
8
0.300 – 0.325
(7.620 – 8.255)
0.130 ± 0.005
(3.302 ± 0.127)
0.045 – 0.065
(1.143 – 1.651)
0.015
(0.381)
MIN
0.065
(1.651)
TYP
0.009 – 0.015
(0.229 – 0.381)
0.325 +0.025 −0.015
(8.255 +0.635 −0.381)
0.125
(3.175)
MIN
0.045 ± 0.015
(1.143 ± 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
N16 0492

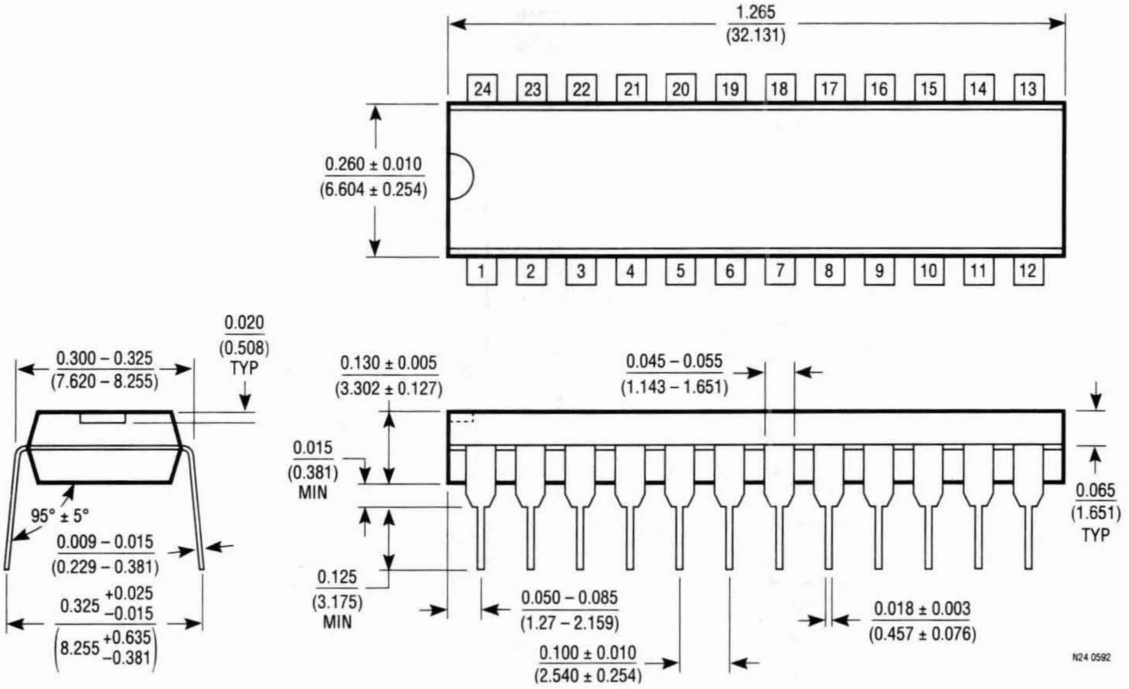
N Package
18-Lead Molded DIP


0.905
(22.860)
MAX
18
17
16
15
14
13
12
11
10
0.260 ± 0.010
(6.604 ± 0.254)
1
2
3
4
5
6
7
8
9
0.300 – 0.325
(7.620 – 8.255)
0.130 ± 0.005
(3.302 ± 0.127)
0.045 – 0.065
(1.143 – 1.651)
0.015
(0.381)
MIN
0.065
(1.651)
TYP
0.009 – 0.015
(0.229 – 0.381)
0.325 +0.025 −0.015
(8.255 +0.635 −0.381)
0.125
(3.175)
MIN
0.045 ± 0.015
(1.143 ± 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
N18 0392

N Package
20-Lead Molded DIP

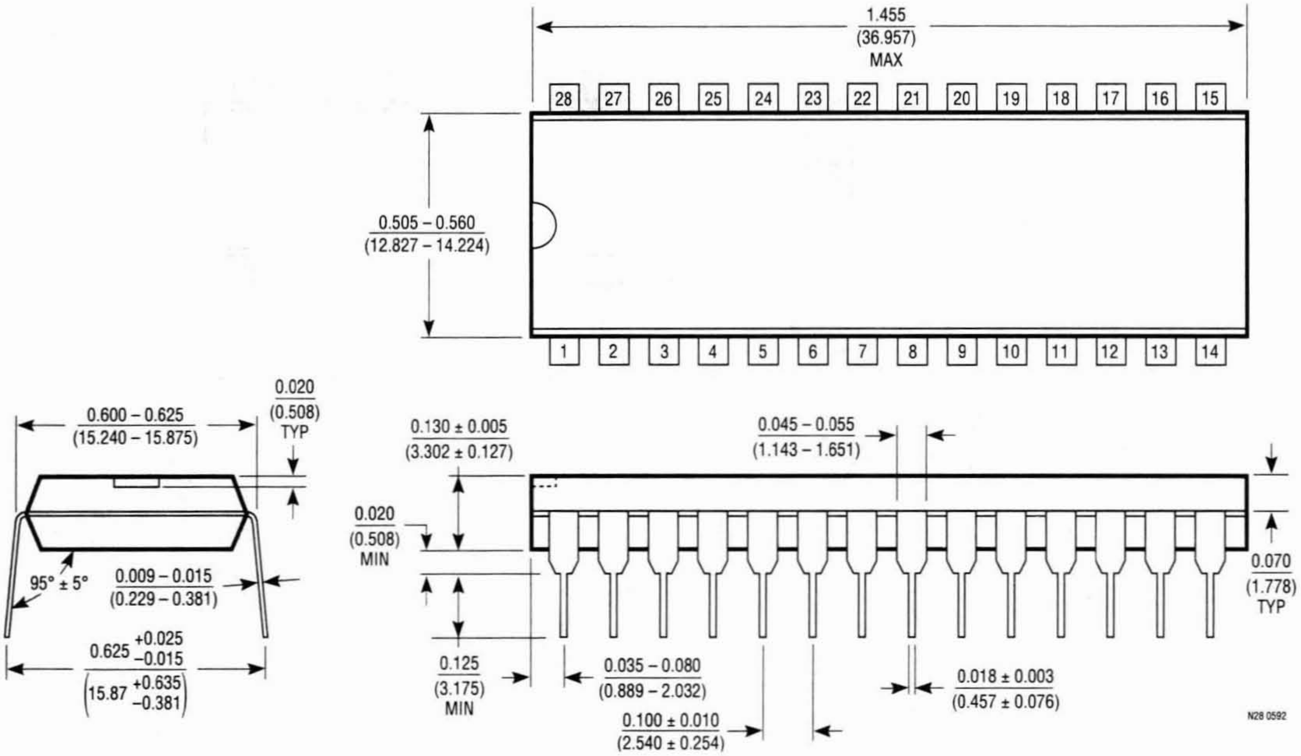

1.040
(26.416)
MAX
20 19 18 17 16 15 14 13 12 11
0.260 ± 0.010
(6.604 ± 0.254)
1 2 3 4 5 6 7 8 9 10
0.300 – 0.325
(7.620 – 8.255)
0.009 – 0.015
(0.229 – 0.381)
0.325 +0.025 −0.015
(8.255 +0.635 −0.381)
0.130 ± 0.005
(3.302 ± 0.127)
0.015
(0.381)
MIN
0.125
(3.175)
MIN
0.045 – 0.065
(1.143 – 1.651)
0.065
(1.651)
TYP
0.065 ± 0.015
(1.651 ± 0.381)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
N20 0592

N Package
24-Lead Molded DIP

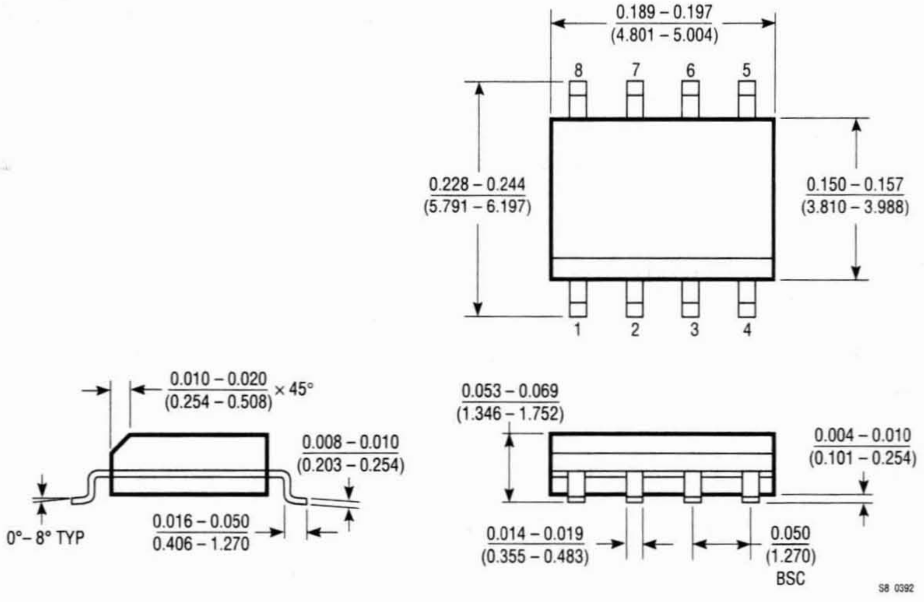

1.265
(32.131)
24 23 22 21 20 19 18 17 16 15 14 13
0.260 ± 0.010
(6.604 ± 0.254)
1 2 3 4 5 6 7 8 9 10 11 12
0.020
(0.508)
TYP
0.300 – 0.325
(7.620 – 8.255)
95° ± 5°
0.009 – 0.015
(0.229 – 0.381)
0.325 +0.025 −0.015
(8.255 +0.635 −0.381)
0.130 ± 0.005
(3.302 ± 0.127)
0.015
(0.381)
MIN
0.125
(3.175)
MIN
0.045 – 0.055
(1.143 – 1.651)
0.065
(1.651)
TYP
0.050 – 0.085
(1.27 – 2.159)
0.018 ± 0.003
(0.457 ± 0.076)
0.100 ± 0.010
(2.540 ± 0.254)
N24 0592

PACKAGE DIMENSIONS

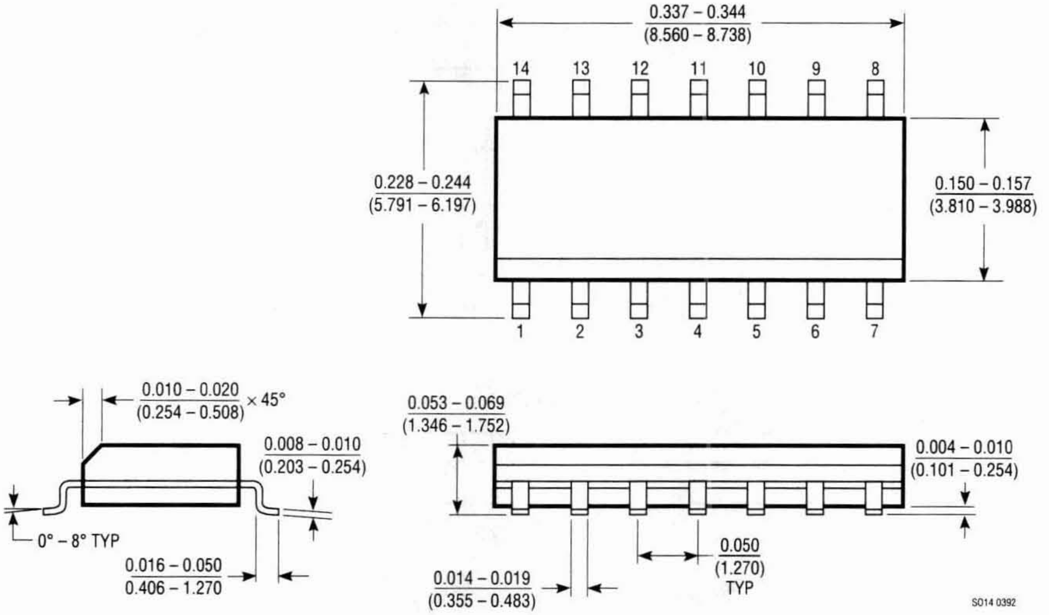
N Package
28-Lead Molded DIP


1.455
(36.957)
MAX
28
27
26
25
24
23
22
21
20
19
18
17
16
15
0.505 – 0.560
(12.827 – 14.224)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
0.020
(0.508)
TYP
0.600 – 0.625
(15.240 – 15.875)
95° ± 5°
0.009 – 0.015
(0.229 – 0.381)
0.625 +0.025 −0.015
(15.87 +0.635 −0.381)
0.130 ± 0.005
(3.302 ± 0.127)
0.045 – 0.055
(1.143 – 1.651)
0.020
(0.508)
MIN
0.125
(3.175)
MIN
0.035 – 0.080
(0.889 – 2.032)
0.100 ± 0.010
(2.540 ± 0.254)
0.018 ± 0.003
(0.457 ± 0.076)
0.070
(1.778)
TYP
N28 0592

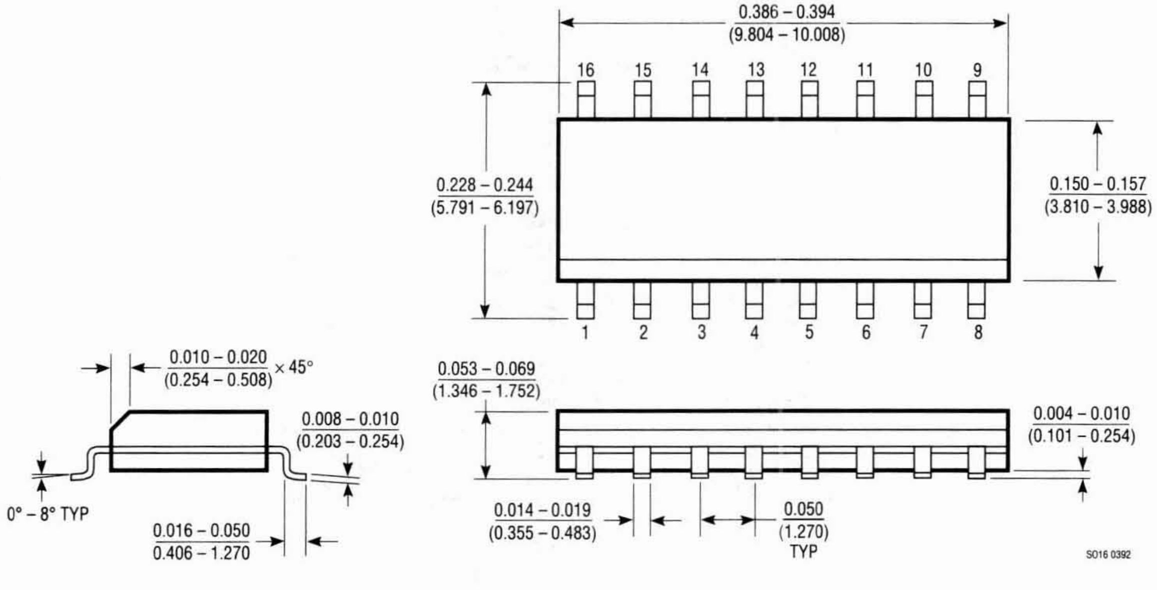
SO Package
8-Lead Small Outline


0.189 – 0.197
(4.801 – 5.004)
8
7
6
5
0.228 – 0.244
(5.791 – 6.197)
0.150 – 0.157
(3.810 – 3.988)
1
2
3
4
0.010 – 0.020
(0.254 – 0.508) × 45°
0.008 – 0.010
(0.203 – 0.254)
0°– 8° TYP
0.016 – 0.050
0.406 – 1.270
0.053 – 0.069
(1.346 – 1.752)
0.004 – 0.010
(0.101 – 0.254)
0.014 – 0.019
(0.355 – 0.483)
0.050
(1.270)
BSC
S8 0392

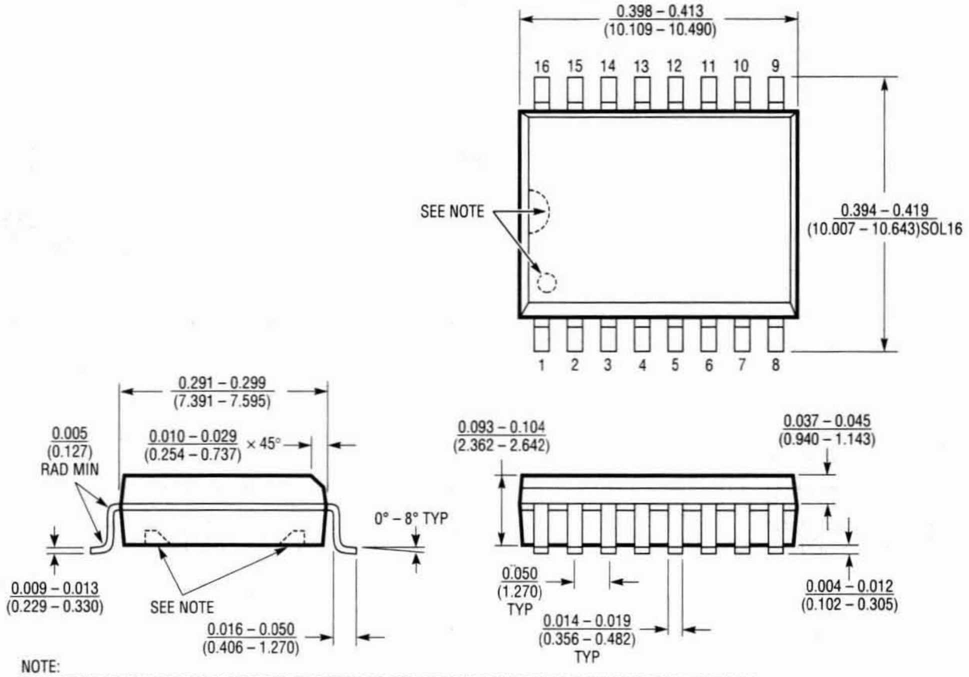
SO Package
14-Lead Small Outline


0.337 – 0.344
(8.560 – 8.738)
14 13 12 11 10 9 8
0.228 – 0.244
(5.791 – 6.197)
0.150 – 0.157
(3.810 – 3.988)
1 2 3 4 5 6 7
0.010 – 0.020
(0.254 – 0.508) × 45°
0.008 – 0.010
(0.203 – 0.254)
0° – 8° TYP
0.016 – 0.050
0.406 – 1.270
0.053 – 0.069
(1.346 – 1.752)
0.004 – 0.010
(0.101 – 0.254)
0.050
(1.270)
TYP
0.014 – 0.019
(0.355 – 0.483)
SO14 0392

SO Package
16-Lead Small Outline


0.386 – 0.394
(9.804 – 10.008)
16 15 14 13 12 11 10 9
0.228 – 0.244
(5.791 – 6.197)
0.150 – 0.157
(3.810 – 3.988)
1 2 3 4 5 6 7 8
0.010 – 0.020
(0.254 – 0.508) × 45°
0.008 – 0.010
(0.203 – 0.254)
0° – 8° TYP
0.016 – 0.050
0.406 – 1.270
0.053 – 0.069
(1.346 – 1.752)
0.004 – 0.010
(0.101 – 0.254)
0.014 – 0.019
(0.355 – 0.483)
0.050
(1.270)
TYP
SO16 0392

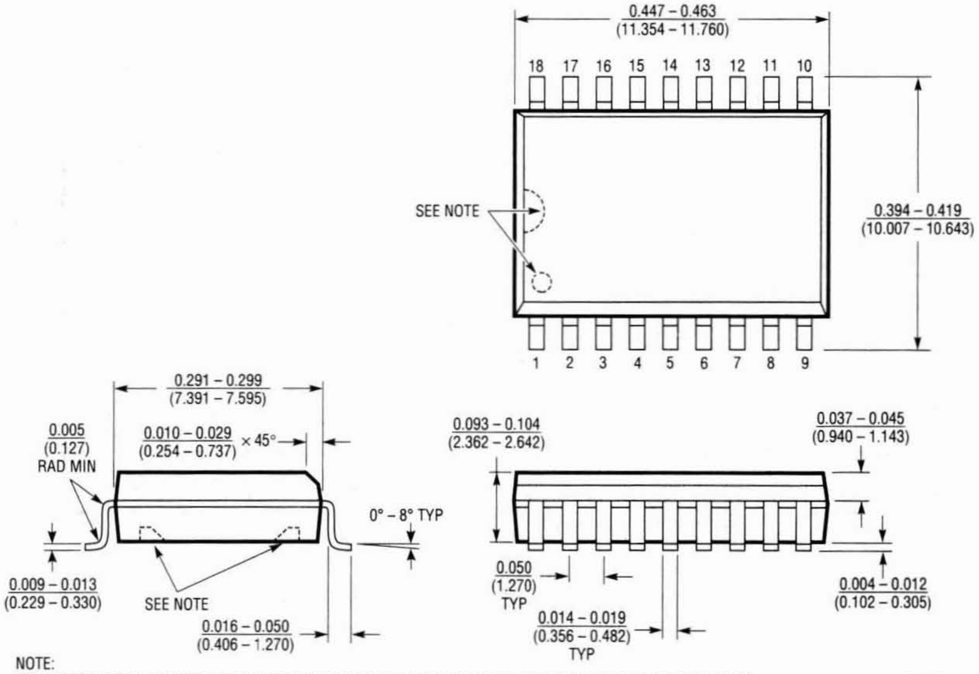
SOL Package
16-Lead Small Outline (Wide)


0.398 – 0.413
(10.109 – 10.490)
16 15 14 13 12 11 10 9
SEE NOTE
0.394 – 0.419
(10.007 – 10.643)SOL16
1 2 3 4 5 6 7 8
0.291 – 0.299
(7.391 – 7.595)
0.005
(0.127)
RAD MIN
0.010 – 0.029
(0.254 – 0.737)
× 45°
0° – 8° TYP
0.009 – 0.013
(0.229 – 0.330)
SEE NOTE
0.016 – 0.050
(0.406 – 1.270)
0.093 – 0.104
(2.362 – 2.642)
0.037 – 0.045
(0.940 – 1.143)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.482)
TYP
0.004 – 0.012
(0.102 – 0.305)

NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

SOL16 0392

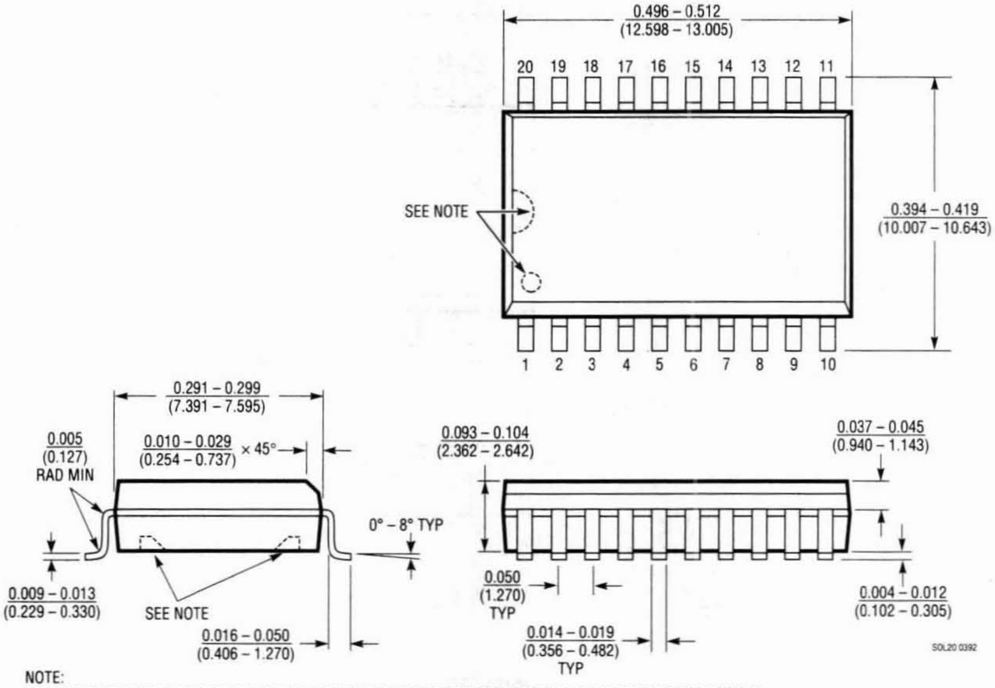
SOL Package
18-Lead Small Outline (Wide)


0.447 – 0.463
(11.354 – 11.760)
18 17 16 15 14 13 12 11 10
SEE NOTE
0.394 – 0.419
(10.007 – 10.643)
1 2 3 4 5 6 7 8 9
0.291 – 0.299
(7.391 – 7.595)
0.005
(0.127)
RAD MIN
0.010 – 0.029
(0.254 – 0.737)
× 45°
0° – 8° TYP
0.009 – 0.013
(0.229 – 0.330)
SEE NOTE
0.016 – 0.050
(0.406 – 1.270)
0.093 – 0.104
(2.362 – 2.642)
0.037 – 0.045
(0.940 – 1.143)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.482)
TYP
0.004 – 0.012
(0.102 – 0.305)

NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

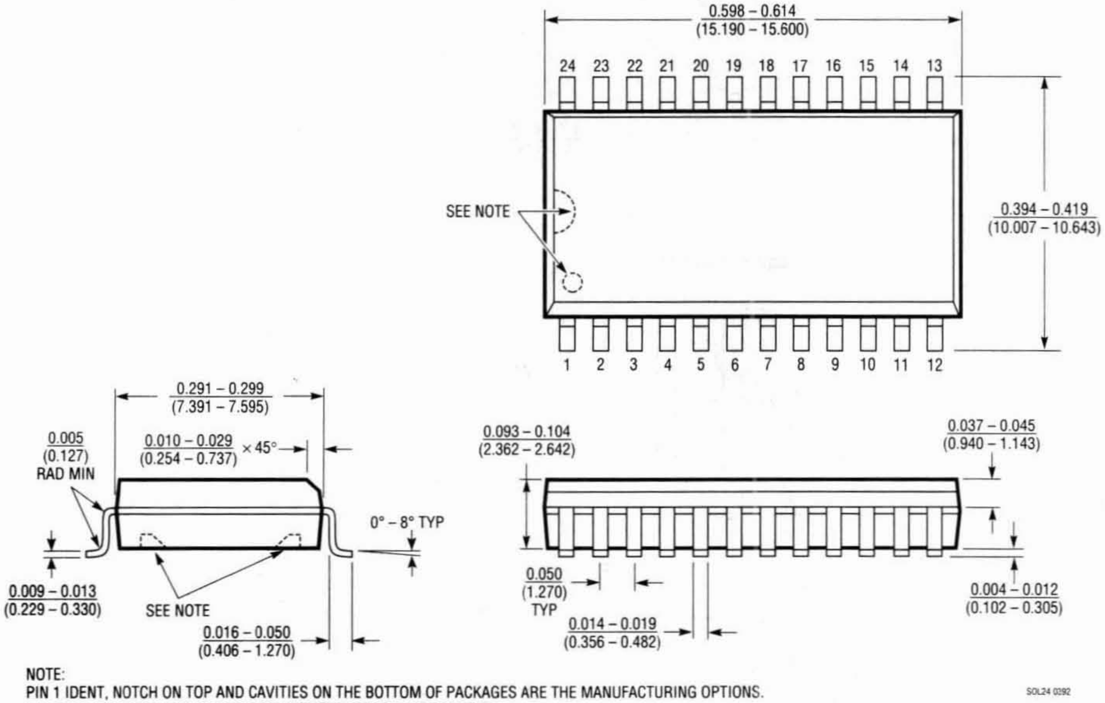
SOL18 0392

SOL Package
20-Lead Small Outline (Wide)


0.496 – 0.512
(12.598 – 13.005)
20 19 18 17 16 15 14 13 12 11
SEE NOTE
0.394 – 0.419
(10.007 – 10.643)
1 2 3 4 5 6 7 8 9 10
0.291 – 0.299
(7.391 – 7.595)
0.005
(0.127)
RAD MIN
0.010 – 0.029
(0.254 – 0.737)
× 45°
0° – 8° TYP
0.009 – 0.013
(0.229 – 0.330)
SEE NOTE
0.016 – 0.050
(0.406 – 1.270)
0.093 – 0.104
(2.362 – 2.642)
0.037 – 0.045
(0.940 – 1.143)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.482)
TYP
0.004 – 0.012
(0.102 – 0.305)
SOL20 0392

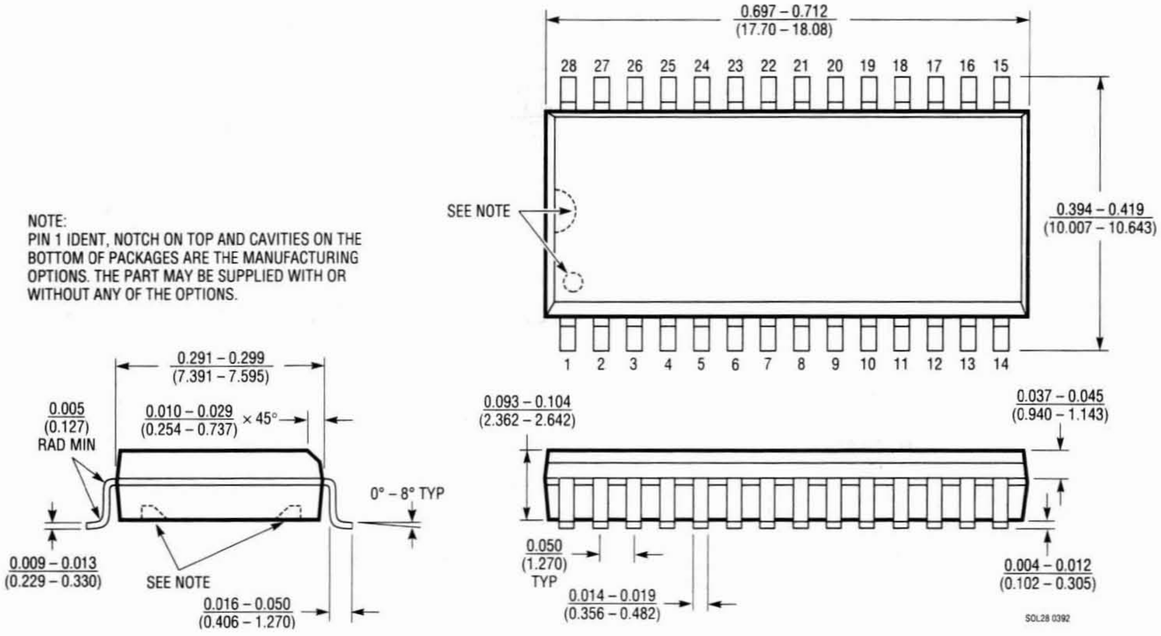
NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

SOL Package
24-Lead Small Outline (Wide)


0.598 – 0.614
(15.190 – 15.600)
24 23 22 21 20 19 18 17 16 15 14 13
SEE NOTE
0.394 – 0.419
(10.007 – 10.643)
1 2 3 4 5 6 7 8 9 10 11 12
0.291 – 0.299
(7.391 – 7.595)
0.005
(0.127)
RAD MIN
0.010 – 0.029
(0.254 – 0.737)
× 45°
0° – 8° TYP
0.009 – 0.013
(0.229 – 0.330)
SEE NOTE
0.016 – 0.050
(0.406 – 1.270)
0.093 – 0.104
(2.362 – 2.642)
0.037 – 0.045
(0.940 – 1.143)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.482)
0.004 – 0.012
(0.102 – 0.305)
SOL24 0392

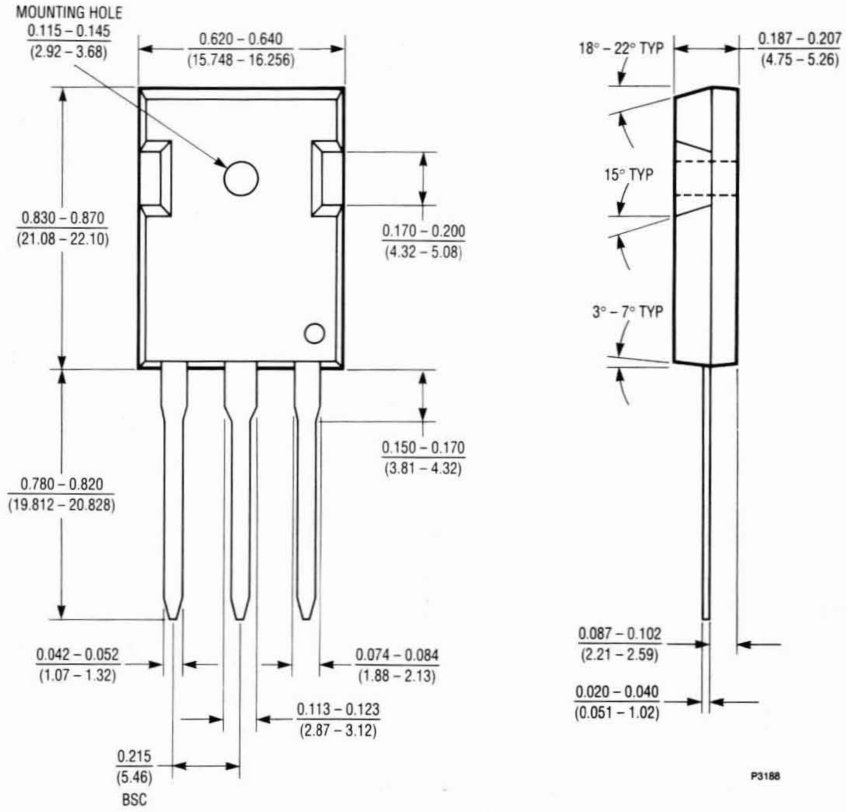
NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

SOL Package
28-Lead Small Outline (Wide)

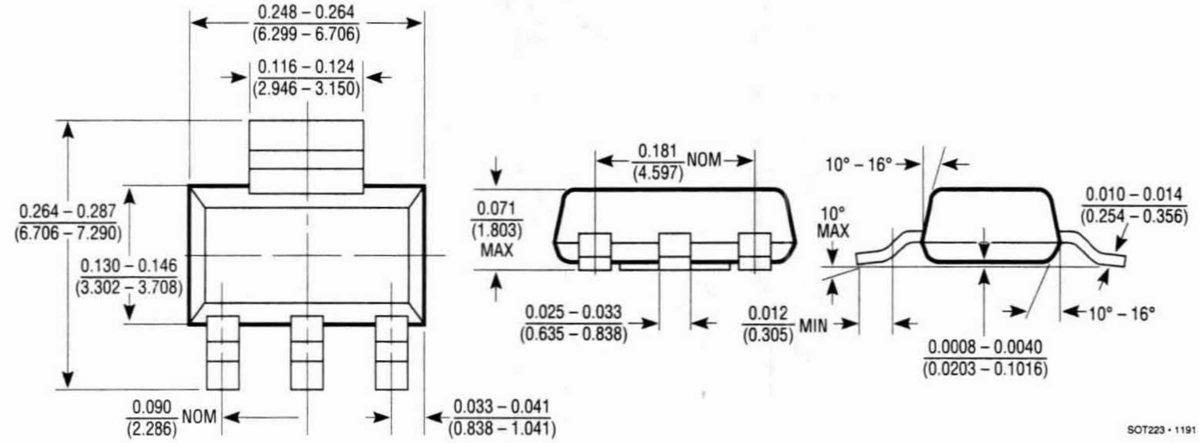

0.697 – 0.712
(17.70 – 18.08)
28 27 26 25 24 23 22 21 20 19 18 17 16 15
SEE NOTE
0.394 – 0.419
(10.007 – 10.643)
1 2 3 4 5 6 7 8 9 10 11 12 13 14
0.291 – 0.299
(7.391 – 7.595)
0.005
(0.127)
RAD MIN
0.010 – 0.029
(0.254 – 0.737)
× 45°
0° – 8° TYP
0.009 – 0.013
(0.229 – 0.330)
SEE NOTE
0.016 – 0.050
(0.406 – 1.270)
0.093 – 0.104
(2.362 – 2.642)
0.037 – 0.045
(0.940 – 1.143)
0.050
(1.270)
TYP
0.014 – 0.019
(0.356 – 0.482)
0.004 – 0.012
(0.102 – 0.305)
SOL28 0392

NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

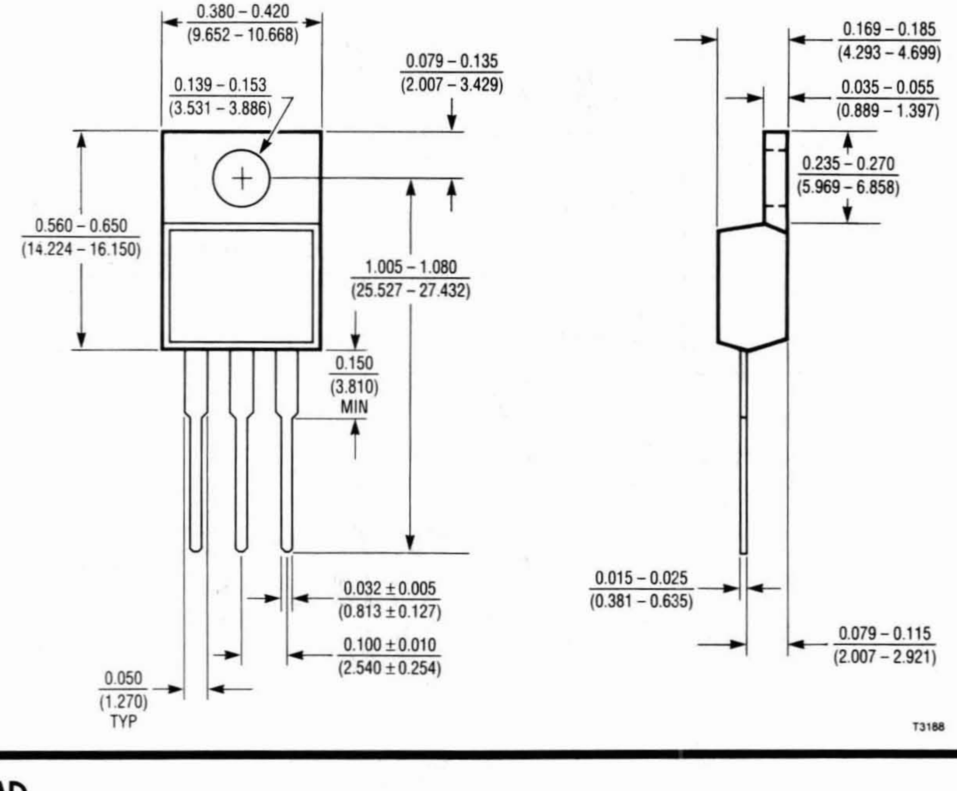
P Package
3-Lead TO-247


MOUNTING HOLE
0.115 – 0.145
(2.92 – 3.68)
0.620 – 0.640
(15.748 – 16.256)
0.830 – 0.870
(21.08 – 22.10)
0.170 – 0.200
(4.32 – 5.08)
0.150 – 0.170
(3.81 – 4.32)
0.780 – 0.820
(19.812 – 20.828)
0.042 – 0.052
(1.07 – 1.32)
0.074 – 0.084
(1.88 – 2.13)
0.113 – 0.123
(2.87 – 3.12)
0.215
(5.46)
BSC
18° – 22° TYP
0.187 – 0.207
(4.75 – 5.26)
15° TYP
3° – 7° TYP
0.087 – 0.102
(2.21 – 2.59)
0.020 – 0.040
(0.051 – 1.02)
P3188

ST Package
3-Lead Plastic SOT-223

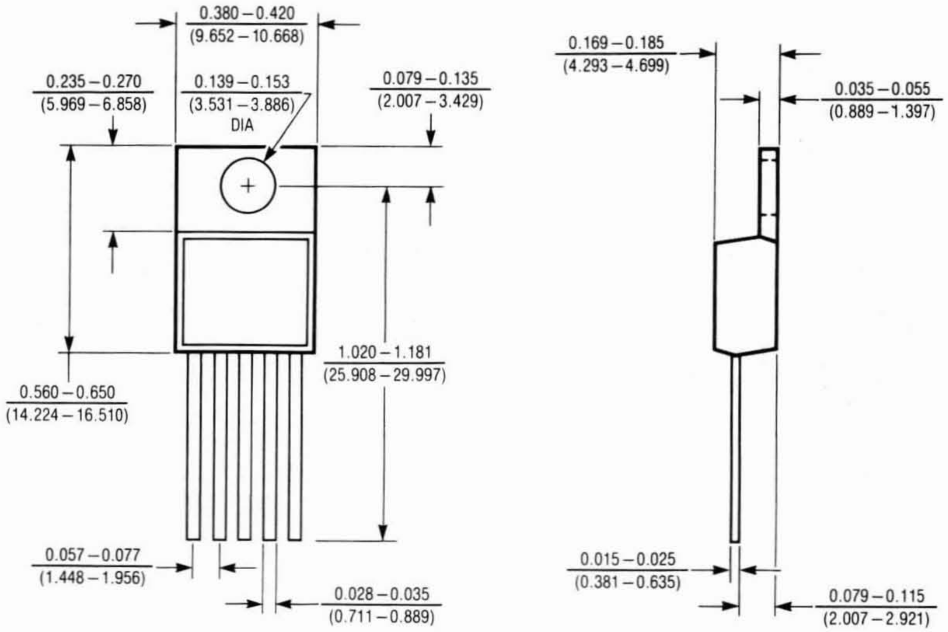

0.248 – 0.264
(6.299 – 6.706)
0.116 – 0.124
(2.946 – 3.150)
0.264 – 0.287
(6.706 – 7.290)
0.130 – 0.146
(3.302 – 3.708)
0.090
(2.286)
NOM
0.033 – 0.041
(0.838 – 1.041)
0.071
(1.803)
MAX
0.181
(4.597)
NOM
0.025 – 0.033
(0.635 – 0.838)
0.012
(0.305)
MIN
10° – 16°
10°
MAX
0.010 – 0.014
(0.254 – 0.356)
10° – 16°
0.0008 – 0.0040
(0.0203 – 0.1016)
SOT223 • 1191

T Package
3-Lead TO-220

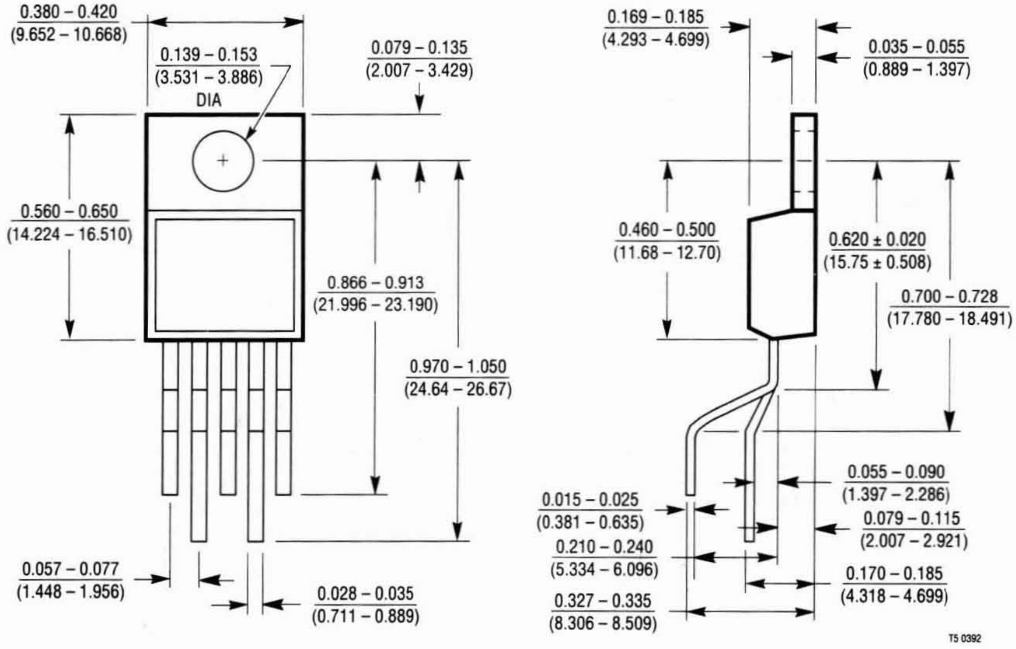

0.380 – 0.420
(9.652 – 10.668)
0.139 – 0.153
(3.531 – 3.886)
0.079 – 0.135
(2.007 – 3.429)
0.560 – 0.650
(14.224 – 16.150)
1.005 – 1.080
(25.527 – 27.432)
0.150
(3.810)
MIN
0.032 ± 0.005
(0.813 ± 0.127)
0.100 ± 0.010
(2.540 ± 0.254)
0.050
(1.270)
TYP
0.169 – 0.185
(4.293 – 4.699)
0.035 – 0.055
(0.889 – 1.397)
0.235 – 0.270
(5.969 – 6.858)
0.015 – 0.025
(0.381 – 0.635)
0.079 – 0.115
(2.007 – 2.921)
T3188

PACKAGE DIMENSIONS

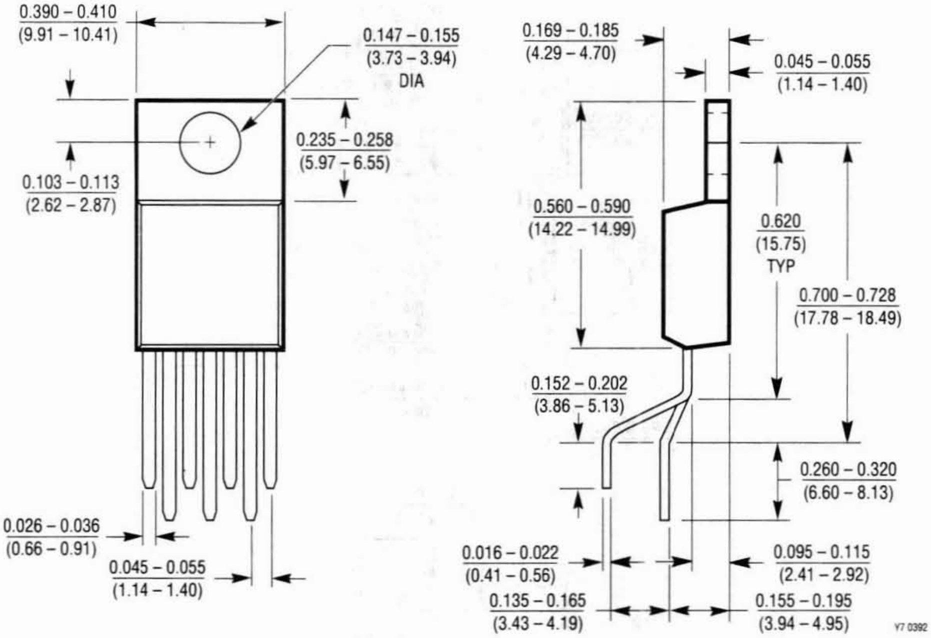
T Package
5-Lead TO-220 (Straight Lead)


0.380 – 0.420
(9.652 – 10.668)
0.235 – 0.270
(5.969 – 6.858)
0.139 – 0.153
(3.531 – 3.886)
DIA
0.079 – 0.135
(2.007 – 3.429)
0.169 – 0.185
(4.293 – 4.699)
0.035 – 0.055
(0.889 – 1.397)
1.020 – 1.181
(25.908 – 29.997)
0.560 – 0.650
(14.224 – 16.510)
0.057 – 0.077
(1.448 – 1.956)
0.028 – 0.035
(0.711 – 0.889)
0.015 – 0.025
(0.381 – 0.635)
0.079 – 0.115
(2.007 – 2.921)
T5(S)289

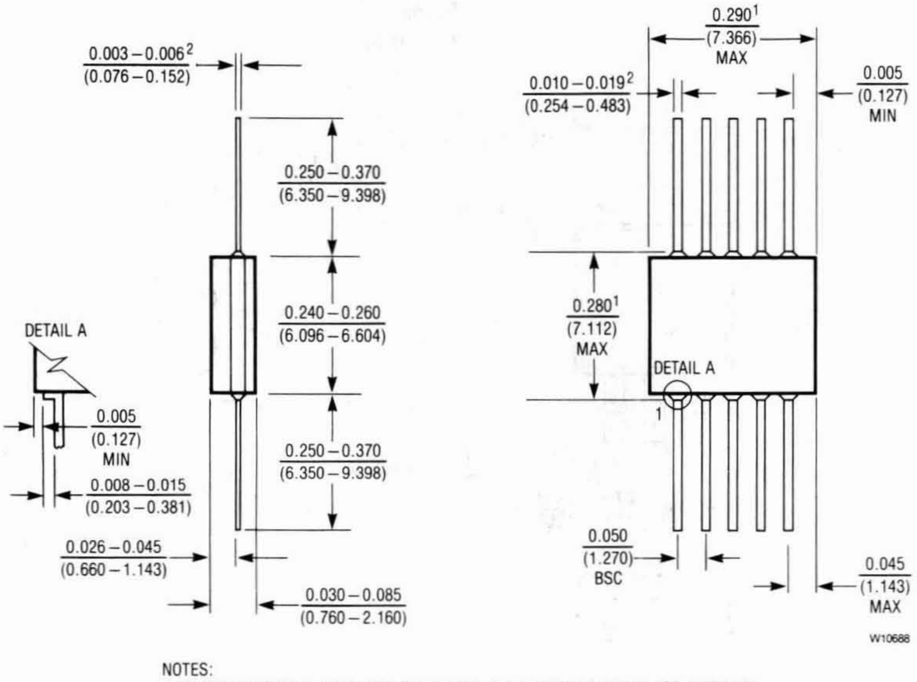
T Package
5-Lead TO-220


0.380 – 0.420
(9.652 – 10.668)
0.139 – 0.153
(3.531 – 3.886)
DIA
0.079 – 0.135
(2.007 – 3.429)
0.169 – 0.185
(4.293 – 4.699)
0.035 – 0.055
(0.889 – 1.397)
0.560 – 0.650
(14.224 – 16.510)
0.866 – 0.913
(21.996 – 23.190)
0.970 – 1.050
(24.64 – 26.67)
0.460 – 0.500
(11.68 – 12.70)
0.620 ± 0.020
(15.75 ± 0.508)
0.700 – 0.728
(17.780 – 18.491)
0.055 – 0.090
(1.397 – 2.286)
0.015 – 0.025
(0.381 – 0.635)
0.079 – 0.115
(2.007 – 2.921)
0.210 – 0.240
(5.334 – 6.096)
0.170 – 0.185
(4.318 – 4.699)
0.327 – 0.335
(8.306 – 8.509)
0.057 – 0.077
(1.448 – 1.956)
0.028 – 0.035
(0.711 – 0.889)
T5 0392

Y Package
7-Lead TO-220

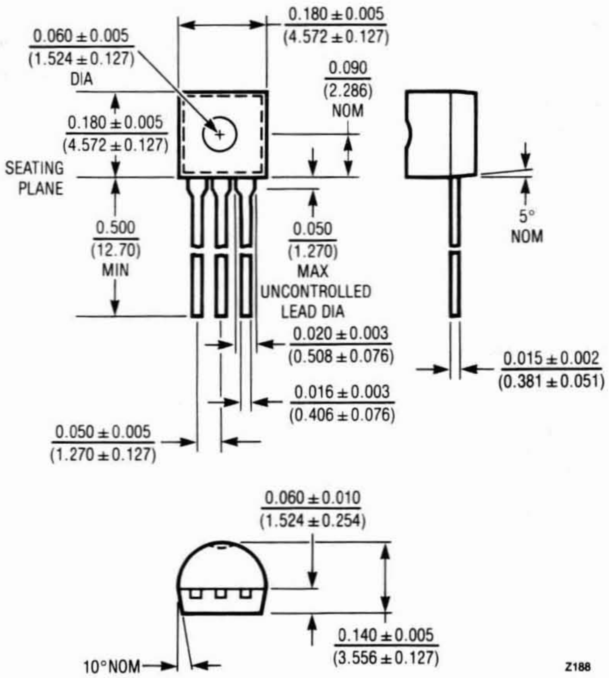

0.390 – 0.410
(9.91 – 10.41)
0.147 – 0.155
(3.73 – 3.94)
DIA
0.169 – 0.185
(4.29 – 4.70)
0.045 – 0.055
(1.14 – 1.40)
0.235 – 0.258
(5.97 – 6.55)
0.103 – 0.113
(2.62 – 2.87)
0.560 – 0.590
(14.22 – 14.99)
0.620
(15.75)
TYP
0.700 – 0.728
(17.78 – 18.49)
0.152 – 0.202
(3.86 – 5.13)
0.260 – 0.320
(6.60 – 8.13)
0.026 – 0.036
(0.66 – 0.91)
0.045 – 0.055
(1.14 – 1.40)
0.016 – 0.022
(0.41 – 0.56)
0.095 – 0.115
(2.41 – 2.92)
0.135 – 0.165
(3.43 – 4.19)
0.155 – 0.195
(3.94 – 4.95)
Y7 0392

W Package
10-Lead Flatpack (Cerpak)

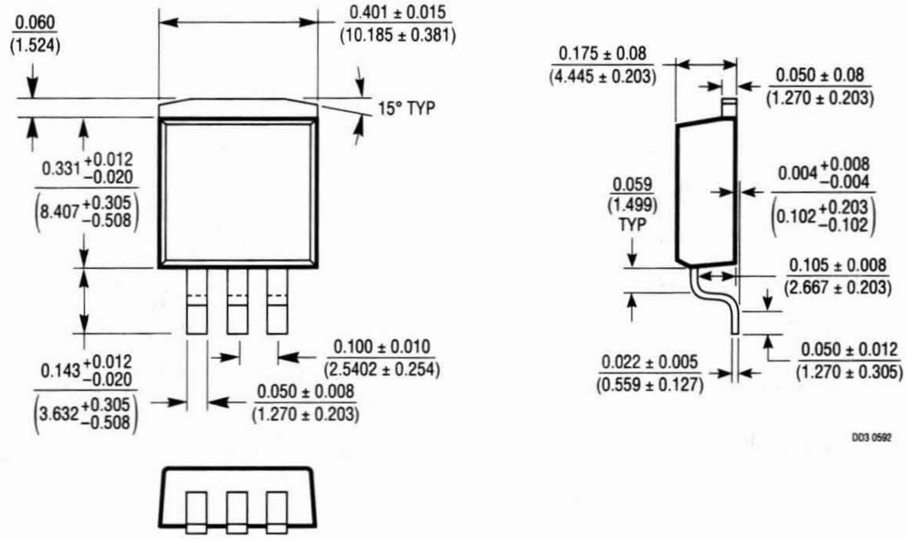

0.003 – 0.006²
(0.076 – 0.152)
0.290¹
(7.366)
MAX
0.010 – 0.019²
(0.254 – 0.483)
0.005
(0.127)
MIN
0.250 – 0.370
(6.350 – 9.398)
0.240 – 0.260
(6.096 – 6.604)
0.280¹
(7.112)
MAX
DETAIL A
DETAIL A
1
0.005
(0.127)
MIN
0.008 – 0.015
(0.203 – 0.381)
0.250 – 0.370
(6.350 – 9.398)
0.050
(1.270)
BSC
0.026 – 0.045
(0.660 – 1.143)
0.045
(1.143)
MAX
0.030 – 0.085
(0.760 – 2.160)
W10688

NOTES:
1. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
2. INCREASE DIMENSIONS BY 0.003 (0.076) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED).

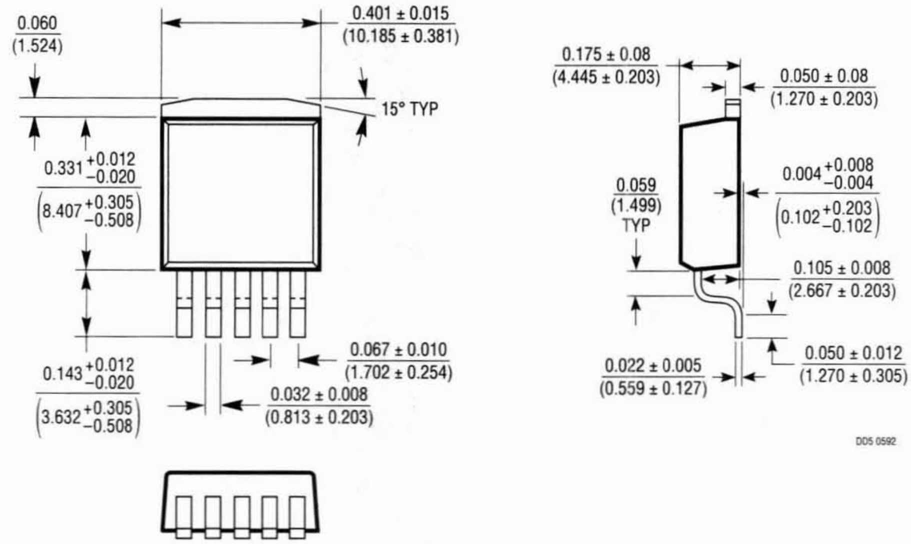
Z Package
3-Lead TO-92


0.060 ± 0.005
(1.524 ± 0.127)
DIA
0.180 ± 0.005
(4.572 ± 0.127)
0.090
(2.286)
NOM
0.180 ± 0.005
(4.572 ± 0.127)
SEATING
PLANE
0.500
(12.70)
MIN
0.050
(1.270)
MAX
UNCONTROLLED
LEAD DIA
5°
NOM
0.020 ± 0.003
(0.508 ± 0.076)
0.015 ± 0.002
(0.381 ± 0.051)
0.016 ± 0.003
(0.406 ± 0.076)
0.050 ± 0.005
(1.270 ± 0.127)
0.060 ± 0.010
(1.524 ± 0.254)
0.140 ± 0.005
(3.556 ± 0.127)
10° NOM
Z188

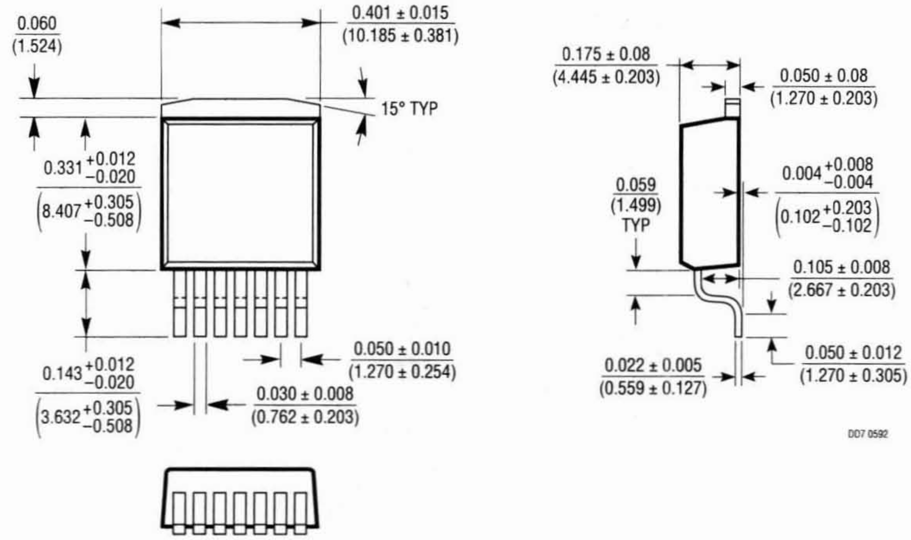
DD Package
3-Lead Plastic


0.060
(1.524)
0.401 ± 0.015
(10.185 ± 0.381)
15° TYP
0.175 ± 0.08
(4.445 ± 0.203)
0.050 ± 0.08
(1.270 ± 0.203)
0.331 +0.012 −0.020
(8.407 +0.305 −0.508)
0.059
(1.499)
TYP
0.004 +0.008 −0.004
(0.102 +0.203 −0.102)
0.105 ± 0.008
(2.667 ± 0.203)
0.100 ± 0.010
(2.5402 ± 0.254)
0.143 +0.012 −0.020
(3.632 +0.305 −0.508)
0.050 ± 0.008
(1.270 ± 0.203)
0.022 ± 0.005
(0.559 ± 0.127)
0.050 ± 0.012
(1.270 ± 0.305)
DD3 0592

DD Package
5-Lead Plastic


0.060
(1.524)
0.401 ± 0.015
(10.185 ± 0.381)
15° TYP
0.331 +0.012 −0.020
(8.407 +0.305 −0.508)
0.143 +0.012 −0.020
(3.632 +0.305 −0.508)
0.067 ± 0.010
(1.702 ± 0.254)
0.032 ± 0.008
(0.813 ± 0.203)
0.175 ± 0.08
(4.445 ± 0.203)
0.050 ± 0.08
(1.270 ± 0.203)
0.059
(1.499)
TYP
0.004 +0.008 −0.004
(0.102 +0.203 −0.102)
0.105 ± 0.008
(2.667 ± 0.203)
0.022 ± 0.005
(0.559 ± 0.127)
0.050 ± 0.012
(1.270 ± 0.305)
DD5 0592

DD Package
7-Lead Plastic


0.060
(1.524)
0.401 ± 0.015
(10.185 ± 0.381)
15° TYP
0.331 +0.012 −0.020
(8.407 +0.305 −0.508)
0.143 +0.012 −0.020
(3.632 +0.305 −0.508)
0.050 ± 0.010
(1.270 ± 0.254)
0.030 ± 0.008
(0.762 ± 0.203)
0.175 ± 0.08
(4.445 ± 0.203)
0.050 ± 0.08
(1.270 ± 0.203)
0.059
(1.499)
TYP
0.004 +0.008 −0.004
(0.102 +0.203 −0.102)
0.105 ± 0.008
(2.667 ± 0.203)
0.022 ± 0.005
(0.559 ± 0.127)
0.050 ± 0.012
(1.270 ± 0.305)
DD7 0592

SECTION 15—APPENDICES

SECTION 15—APPENDICES

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Quality and Reliability Assurance Programs

Linear Technology Corporation has a wide ranging program integrating vendor participation, design engineering, and manufacturing to produce the most reliable and highest quality linear integrated circuits available on the market. Our modern manufacturing facility in Milpitas, California is DESC Class S and Class B line certified. We have successfully completed over 90 major OEM quality system surveys to MIL-Q-9858 and MIL-I-45208 including achieving several major customer quality awards. Our Quality and Reliability Assurance Programs are summarized below:

- **Wafer Fabrication** — A modern class 100 area modular clean room construction with full environmental monitors. Emphasis is placed on statistical quality control, CV plots, SEM monitors and on our proprietary dual layer passivation system.
- **SPC (Statistical Process Control)** — LTC is committed to SPC as the cornerstone of our continuous quality improvement and Total Quality Management System (TQMS) programs. SPC is fully implemented in all manufacturing areas.
- **Assembly and End of Line** — Incoming inspection of all materials and piece-parts, line surveillance and process control monitors.
- **Testing** — Incoming inspection and acceptance of all offshore lots prior to release to test. LTX testers, multipass testing with closed loop binning to reduce outgoing electrical defective levels. Many “beyond data sheet” tests and full temperature QA lot buy-offs are performed as standard processing.
- **Traceability** — A backside or side mark is placed on all units, where space permits, to give information on each unit to identify the wafer fab lot, assembly, end of line (e.o.l.) and test lots. The information provided exceeds the seal week traceability control required by MIL-STD-883.
- **ESD (Electro Static Discharge)** — A full program is in place from design through manufacturing. Products are fully characterized to MIL-STD-883 (Method 3015) and strict controls on handling and packaging are observed.
- **Training and Certification** — Operator training has been established for all operations and recertification is performed every 6 months.
- **Major Change Control** — Major change controls are in place to notify our customers in accordance with MIL-M-38510, LTC internal specifications, or specific customer specifications as required.
- **Quality Assurance** — Full monitoring and reporting of quality data with emphasis on statistical process control charts and continuous quality improvement. Refer to our section on Quality Assurance Program.
- **Failure Analysis and Reporting** — A full analytical lab and formal program exists to record, analyze and take appropriate corrective action on all returns. A report is generated and sent to the customer stating our findings and action.
- **Reliability Flows** — Linear Technology reliability flows include Class S and Class B JAN-38510, Standard Military Drawings (SMD), DESC Drawings, 883, R-Flow, and Hi-Rel (Source Controlled Drawings). In addition, specialized processing such as SEM, PIND and other tests can be performed as required.
- **Reliability Monitor** — LTC has a unique reliability structure built into each wafer that is used to obtain rapid feedback on reliability. This data is obtained in less than 1 week, versus 40 weeks for a typical reliability audit. See the LTC Reliability Program for more details. LTC has a comprehensive reliability monitor program for plastic packaged devices. A variety of tests are performed on every 1 week date code, for every package type and lead count and real time feedback to the assembly facilities.
- **Reliability Reporting** — Data is gathered on a monthly basis for selected package/product combinations. This data is summarized each quarter and published in a Reliability Data Pack showing Operating Life, 85/85, HAST, Autoclave, Temperature Cycle, Thermal Shock, 883 Group C, and 883 Group D summary data. Copies of Reliability Data Pack summaries are available by writing or calling Linear Technology, 1630 McCarthy Blvd., Milpitas, CA 95035, (800) 637-5545.

INTRODUCTION

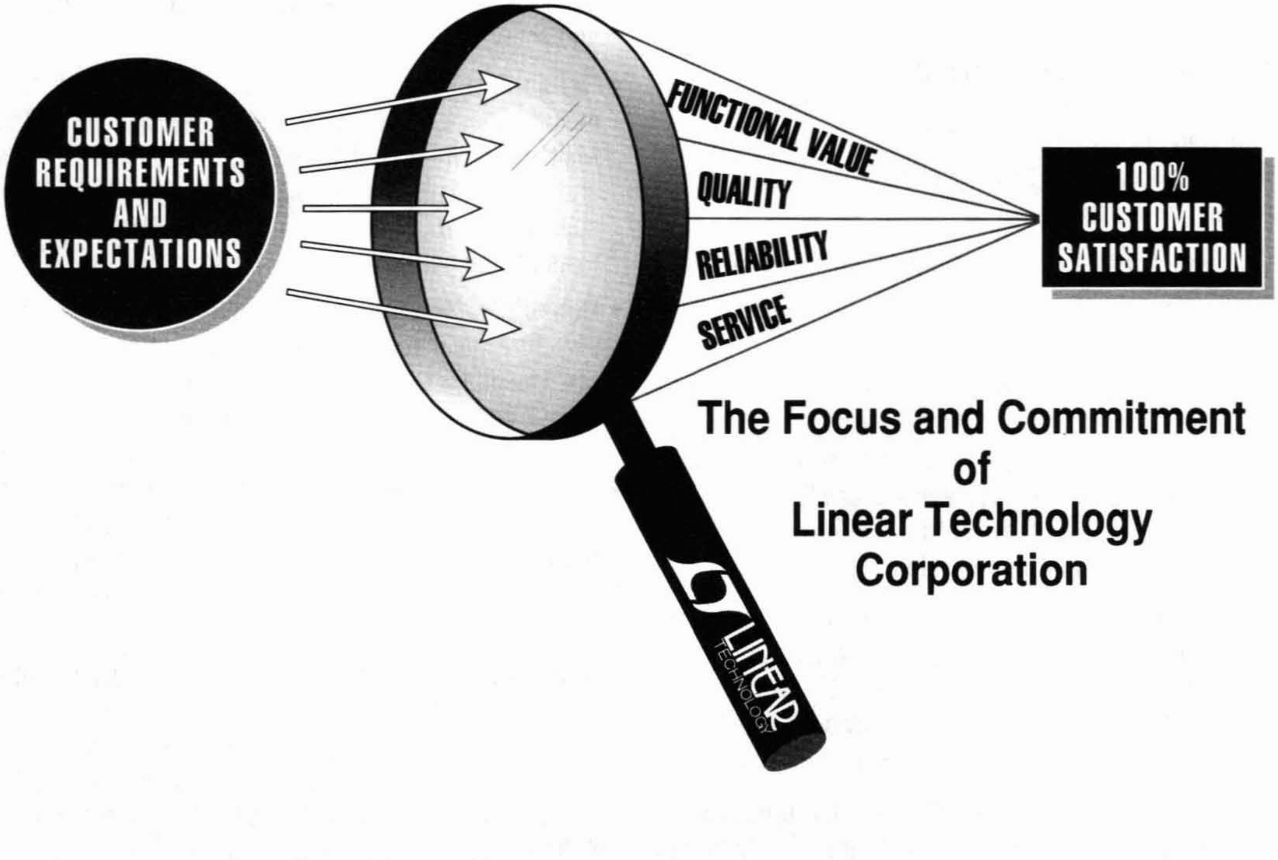
In 1981, Linear Technology Corporation was founded with the intention of becoming a world leader in high performance analog semiconductors. To achieve this goal Linear Technology Corporation committed itself to consistently meet its customers' needs in four areas:

- ☐ Functional Value
- ☐ Quality
- ☐ Reliability
- ☐ Service

Linear Technology Corporation has achieved its primary goal and is now focused to achieve 100% customer satisfaction.

This brochure defines the key elements of Linear Technology Corporation's Reliability Assurance Program which is divided into three groups:

- ☐ Reliability Planning
- ☐ Manufacturing for Reliability
- ☐ Reliability Assessment and Improvement


CUSTOMER REQUIREMENTS AND EXPECTATIONS
FUNCTIONAL VALUE
QUALITY
RELIABILITY
SERVICE
100% CUSTOMER SATISFACTION
LINEAR TECHNOLOGY

The Focus and Commitment of Linear Technology Corporation

RELIABILITY PLANNING

Reliability planning takes three forms at Linear Technology Corporation (LTC). The first is the establishment of the reliability requirements for a product to be released to manufacturing. The second is the definition and implementation of a predictive reliability system. The third is designing for reliability, which includes new product development, materials selection, and construction techniques.

We fully realize that the cost of failure in the field is many orders of magnitude more than the initial component cost. Therefore, the goal of the reliability planning process is to provide reliable product to reduce the cost of ownership to our customers.

Reliability Criteria

A key element of reliability planning is LTC's internal specification entitled "Quality Assurance/Reliability Assurance Qualification Requirement". It contains a complete description of the interrelationships of the various groups involved in meeting LTC's reliability objectives and defines the guidelines for release decisions which affect quality and reliability of the device.

Predictive Reliability System

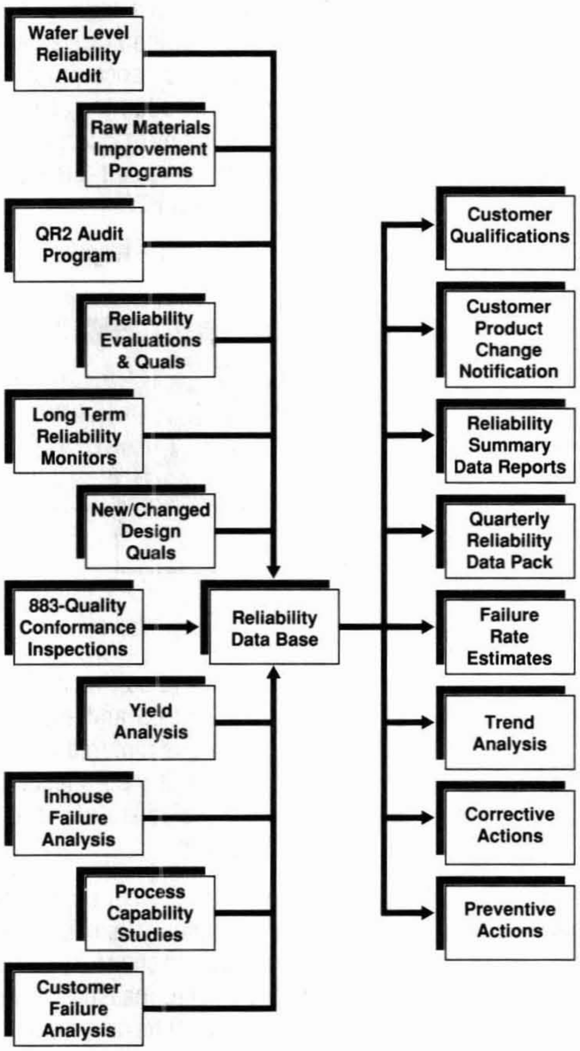
LTC has developed a predictive reliability system which combines quality and reliability information in a database to provide reliability summaries and trend analysis. A block diagram of the system is shown on this page.

Designing for Reliability

Considerable planning goes into the design of LTC's products. This planning includes device layout considerations, selection of input and output protection schemes, selection of fab processing technology, and specification of materials and manufacturing techniques.

A stringent set of bipolar and CMOS design rules have been established to enhance reliability and optimize manufacturability through robust design. At the design stage, the reliability of the circuit is heavily dependent on layout considerations. The rules for thickness and width of metallization have been defined to minimize the current density and prevent electromigration. Current density calculations are required to be performed on all products to ensure that the designs are conservative. The routing of the metal pattern is designed to eliminate potential inversion or leakage failures and guard ring structures are used where appropriate. The positions of bonding pads are carefully selected to optimize device performance and also to fit easily into a variety of packages without creating potential bond loop problems that could result in shorted wires.

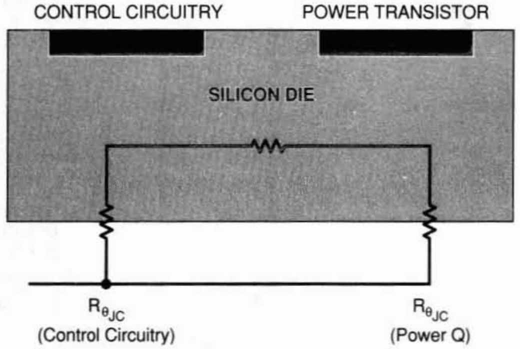
The Predictive Reliability System


Wafer Level Reliability Audit
Raw Materials Improvement Programs
QR2 Audit Program
Reliability Evaluations & Quals
Long Term Reliability Monitors
New/Changed Design Quals
883-Quality Conformance Inspections
Reliability Data Base
Yield Analysis
Inhouse Failure Analysis
Process Capability Studies
Customer Failure Analysis
Customer Qualifications
Customer Product Change Notification
Reliability Summary Data Reports
Quarterly Reliability Data Pack
Failure Rate Estimates
Trend Analysis
Corrective Actions
Preventive Actions

The thermal layout of our circuits also receives considerable attention to minimize parametric drift and optimize performance. In the case of voltage regulators, for any given power dissipation there will be some temperature difference between the power transistor and the control circuitry, due to their separation on the die. This temperature difference is a desirable situation which is used to reduce the power transistor's temperature affect on the control circuitry. Additionally, the power transistor has a higher maximum junction temperature rating than that of the control circuitry and may be allowed to run warmer without degradation. Such LTC products are also designed for maximum efficiency to reduce power dissipation and thereby improve reliability and reduce the cost of heat sinking in the customer's product.

All of our voltage regulators include thermal limiting in the circuitry to shut down the device if the temperature exceeds the safe operating conditions. Additional insurance is provided by employing short circuit current protection to safeguard against catastrophic failure. The philosophy of incorporating fault tolerant designs with innovative circuit protection concepts is a fundamental design rule at LTC.

Thermal Resistance Model of LTC's Voltage Regulators



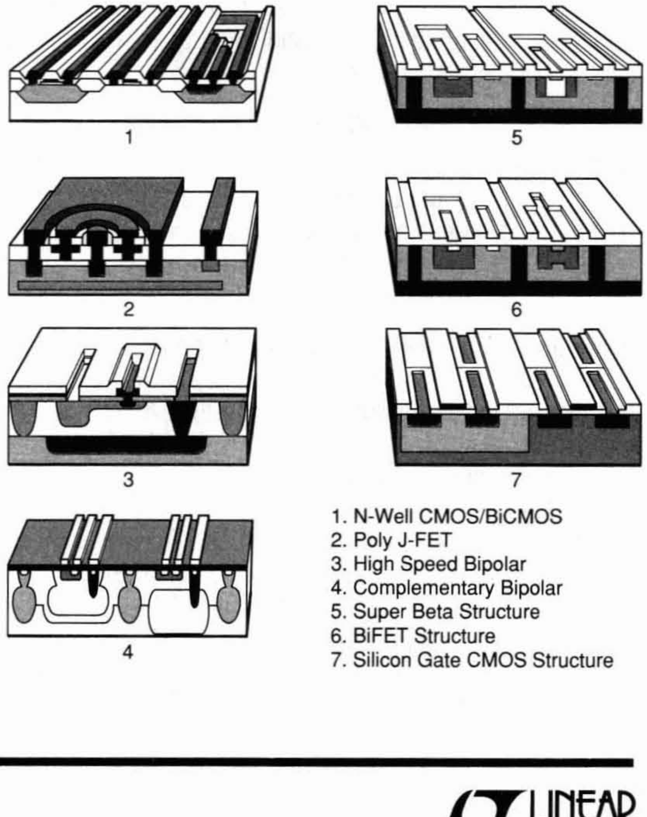
Another major design consideration in circuit reliability is tolerance to electrostatic discharge (ESD) and electrical overstress (EOS). ESD is a problem encountered both in normal handling and circuit assembly. It also affects the reliability of the final product when cables are exposed to ESD such as in line drivers and receivers.

The implementation of ESD protection structures in linear integrated circuits is much more difficult than in digital circuits. The linear circuit must provide protection for electrical overstress while maintaining the ability to measure current levels in the picoamp range. Interface circuits have input and output connections that normally operate at voltages in excess of the power supply, thereby precluding the use of clamp structures to the power supply for ESD protection. LTC, using a combination of circuit design and proprietary structures, provides high levels of overstress immunity to its devices which enhances their reliability. As a goal, all devices are designed for a minimum of 2,000 volts ESD protection with some devices achieving 5,000 volts to 10,000 volts ESD protection.

Linear circuits with total supply currents in the microamp range cannot tolerate leakages induced by contamination. Whether the circuit is Bipolar, CMOS or Complementary Bipolar, the circuit must withstand high operating voltage and high temperature for thousands of hours without leakage currents degrading device performance. LTC uses advanced process techniques to shield the die from sodium contamination while preventing electron accumulation causing surface inversions. This, combined with continuous monitoring of the assembly process, ensures high reliability devices.

LTC utilizes state-of-the-art processes in manufacturing its products. Our high voltage Bipolar process provides high gain, low noise general purpose devices as well as high power integrated circuits. CMOS can provide high complexity ICs with a large digital content. Complementary Bipolar, a new process developed in-house by LTC, provides high speed NPNs and PNPs on the same monolithic die. Complementary Bipolar enables an expanded product range for linear circuits and is suitable for very high speed amplifiers, general purpose linear signal processing or even high speed D/A converters. All of these products are characterized by high reliability, low power consumption and the ability to operate from a wide range of power supplies and over a wide range of ambient temperatures.

LTC's Process Structures



1. N-Well CMOS/BiCMOS
2. Poly J-FET
3. High Speed Bipolar
4. Complementary Bipolar
5. Super Beta Structure
6. BiFET Structure
7. Silicon Gate CMOS Structure

In order to ensure that device performance and reliability goals are achieved on new products, design review meetings are held regularly during the design and development phase.

Material Selection

LTC has selected assembly processes and materials that are closely matched to achieve the highest reliability level in both ultra precision and high power devices. Compatibility between the different package elements, such as the molding compound and lead frame, are carefully researched and qualified. The choice of materials and assembly processes are especially critical in surface mount devices, which must maintain reliability after being subjected to harsh board soldering environments. At LTC we are using the latest state-of-the-art assembly equipment and materials to guarantee reliability. Our low stress epoxy molding compound is extremely low in ionic impurities.

Similar improvements have been made in hermetic packages in the modern low temperature glass ceramic seals and improved die attach materials.

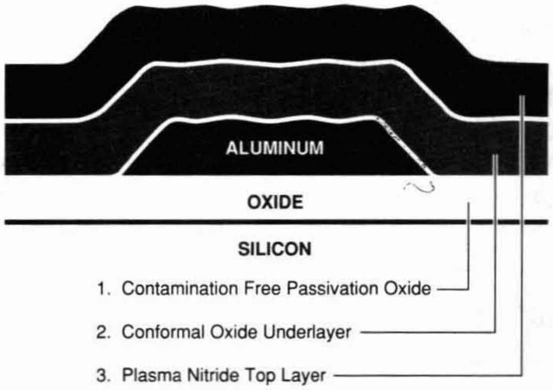
To protect the die from degradation before assembly, and from the long term effects of the package environment, LTC has developed a proprietary dual layer passivation. This dual layer passivation system is free from cracks and pinhole defects and offers an outstanding moisture barrier without detrimental side affects to device performance.

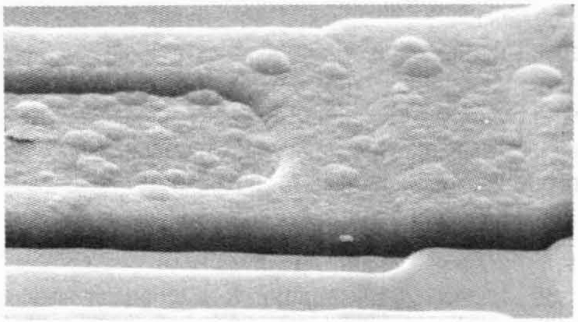
Design of Experiments

LTC is committed to the use of design of experiments (DOE) when developing new products and processes. We firmly believe that design of experiments will be the new industry standard for product and process development.

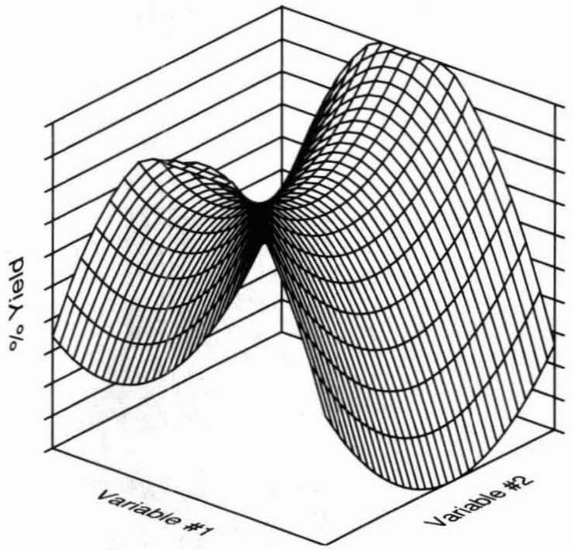
DOE has been successfully utilized on numerous products and processes at LTC. DOE, coupled with response surface methodology, has provided LTC the ability to solve complex problems that were previously unsolvable. We have used DOE to characterize wafer fab processes and provided this information to our IC designers which enabled them to produce devices that were less sensitive to manufacturing variations.

LTC's Dual Layer Passivation System


ALUMINUM
OXIDE
SILICON
1. Contamination Free Passivation Oxide
2. Conformal Oxide Underlayer
3. Plasma Nitride Top Layer



Response Surface Model of PIND Yield after Welding Operation



MANUFACTURING FOR RELIABILITY

LTC is keenly aware of the influence which the manufacturing process has on the quality and reliability of the finished product. For this reason, LTC has placed critical emphasis on the manufacturing facility and associated process controls. LTC's claims of outstanding manufacturing capability and controls are validated by the fact that we achieved Class S Certification by DESC in November of 1987.

LTC's strategy in manufacturing for reliability includes the use of automated state-of-the-art equipment, protection of the product as it moves through manufacturing, effective inspection and screening, device traceability and statistical process control. These and other similar tight controls are applied from wafer fabrication through product shipment.

Wafer Fab

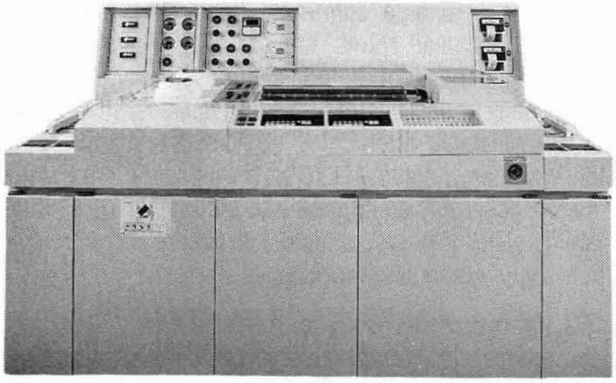
In wafer fabrication, the key to a reliable process is process control. Two major thrusts of process control in the wafer fab are the application of statistical process control (SPC) and the use of automated processing equipment. Automated equipment employing cassette-to-cassette wafer transfer, proximity mode aligners and projection steppers have significantly reduced handling related defects.

Projection Stepper

UltraStep 990
Stepper

Microprocessor controlled furnaces are used to eliminate the effects of process variations and human errors. Thin film processing employs fully automated sputtering and metal etch systems.

Automated Metal Etch System



All of these equipment enhancements work together to yield a process that is consistent and repeatable with a minimum of wafer handling. Quality control monitors and inspections at various points in the process, coupled with the use of control charting throughout the fab area, ensure consistent processing. The quality of the oxide is checked regularly using C-V plots to check for contamination and surface state anomalies. Scanning electron microscope inspection is performed periodically each day to ensure the integrity of the metallization system.

Assembly

The introduction of new equipment and techniques in the assembly process has had a tremendous impact on device reliability. The use of automated equipment has reduced the handling and subsequent damage of die and wafers. In situations where die or wafers must be handled, vacuum wands and vacuum pens have replaced tweezers and thereby decreased damage due to scratches. Automated wire bonding machines have produced more consistent wire bonding quality and improved productivity.

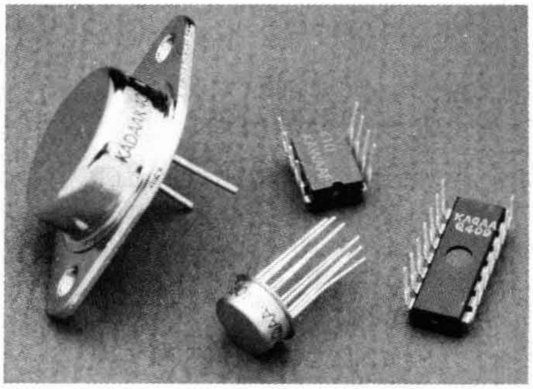
All products receive a thorough visual inspection per Mil-Std-883 Method 2010 Condition B or an equivalent visual criteria prior to encapsulation.

High Speed Automatic Bonder

Traceability

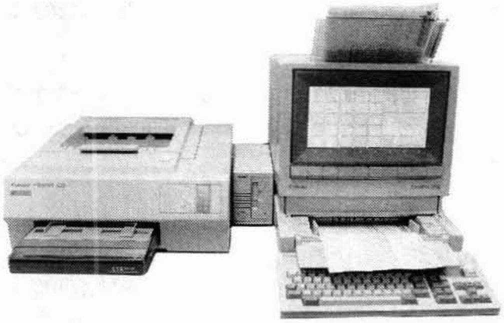
LTC has an outstanding traceability control system. A backside mark or a side mark is used to code information including the country of assembly, assembly facility, exact assembly lot seal date, wafer fab lot, die type and revision. Additionally, this backside mark will identify any non-standard processing which may have been required using a custom flow. At the wafer level, each wafer is laser scribed to include the fab run number and wafer serial number. This traceability benefit is offered as a standard feature on all packages where space allows and is part of the "added value" of LTC products.

Traceability Control Using Backside Mark or Side Mark Coding



To enhance traceability, LTC is using the latest state-of-the-art document archival system. This computerized system incorporates a document scanner which digitizes and compresses documents to be stored on optical disks. As the documents are stored, their ID number, date, and classification are recorded in the system's database to facilitate retrieval. This system allows fab travelers, test travelers and other critical documents to be retrieved in minutes as opposed to hours or days.

Optical Disk Archive System



Reliability Screening

Although our standard product families are recognized for their very low infant mortality, customer requested additional reliability screening can be provided by LTC. This added reliability screening for commercial or industrial level products is offered for both hermetic and plastic devices and is designated as our "R" flow process signified by a /R symbol as a suffix to the part number.

The "R" flow includes temperature cycle, burn-in and QA testing at 0°C, +25°C, and +70°C. A simplified flowchart of the "R" flow is shown in Table 1 at the end of this brochure. The hermetic devices are also offered as JAN Class S or Class B, Standardized Military Drawings (SMDs) and also as Mil-Std-883 devices.

LTC offers a cost effective reliability screen for hermetic product using the Mil-Std-883 screening and quality conformance inspection. This flow is defined in our "Mil-Std-883" brochure and depicted in a brief flow diagram shown in Table 2 at the end of this brochure.

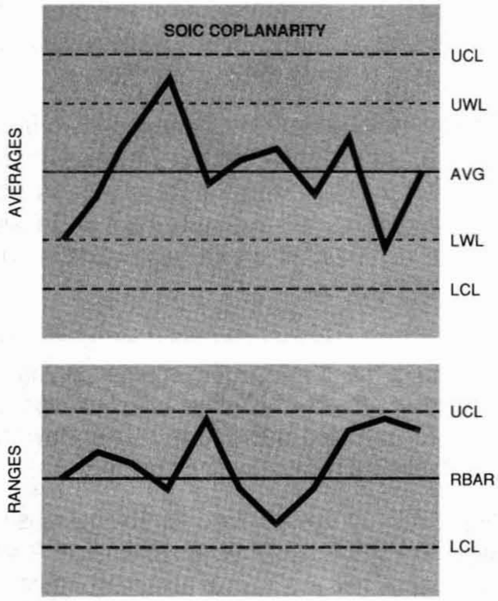
The Mil-Std-883 burn-in at 125°C for 160 hours is roughly equivalent to 80,000 hours or approximately 9 years of continuous operation at a normal operating temperature of around 55°C (Assuming an activation energy of 1.0 electron volts).

Whether testing plastic or hermetic devices, the engineers at LTC routinely add tests in addition to the standard data sheet tests. These added tests are used to detect potential flaws that could impact reliability and provide additional device compatibility with subtle application related performance characteristics. Examples of such additional tests are the exercising of thermal shutdown mode of regulators prior to burn-in or the stressing of on-chip capacitors with voltages in excess of the device maximum rating to induce failure in substandard lots.

Data sheet electrical parameters are measured before and after the specified stress testing to ensure the electrical integrity of the devices.

Statistical Process Control

At LTC we believe that quality and reliability should be built into a product as opposed to simply screening out bad devices. Statistical Process Control (SPC) is ideally suited to our manufacturing goals. SPC has enabled us to run processes with uniform and centered distributions which have not only optimized yields, but have also produced a finished product that is rugged and reliable.



Example of Control Chart for SOIC Coplanarity

Control charting at all critical processes is used to identify the need for corrective action before an out of control situation occurs, thus reducing the overall process variation. LTC has an active SPC program. The generic process from wafer fabrication through shipping has been flow charted with critical nodes defined. The Control Plan Detail outlines the various attributes of the activities surrounding that particular activity. Organization for SPC is comprised of the:

- ☐ Steering Committee
- ☐ SPC Quality Control Teams (QCTs)
- ☐ Process/Preventive Action Teams (PATs)

The Steering Committee provides the leadership for the SPC process, while the QCTs are responsible for the implementation and maintenance of SPC within their respective operational groups. PATs are formed by the QCTs to implement certain initial or corrective measures with specific stated goals, using SPC tools. There are four QCTs in place:

- ☐ Wafer Fab
- ☐ Quality and Reliability
- ☐ Local Assembly
- ☐ End-of-Line (which includes Test, Mark, Pack, Product and Test Engineering)

Since by definition, a PAT functions until its stated goal is attained, their number and tasks are constantly changing. We have had as many as 23 active PATs which include operators and maintenance personnel.

Training is provided in-house for a majority of the Company's employees, who receive test materials and 135 to 279 hours of instruction in one or more of the following courses:

- ☐ Basic SPC
- ☐ Advanced SPC
- ☐ Design of Experiments
- ☐ Team Organization

An important aspect of the SPC program at LTC involves the use of Design of Experiments to solve specific problems, develop new products/processes, and characterize new products and/or processes.

LTC is driving SPC beyond our own factory. A Preferred Supplier Program has been implemented with our raw materials suppliers, wherein parameters deemed critical to the manufacturing process at LTC are controlled statistically by the raw material supplier. Evidence of this control is supplied to LTC on a regular basis. This system of customer-supplier cooperation ensures the integrity of the materials and maintains a mutual focus on improvement.

RELIABILITY ASSESSMENT AND IMPROVEMENT

LTC combines a traditional approach to reliability which incorporates product qualification and long term reliability assessment with a "leading edge" approach, which incorporates wafer level reliability testing and in line assembly reliability monitoring.

Qualification Testing

Before a new product can be released to production, strict qualification testing requirements must be met. These same qualification requirements apply to new processes, new materials, new designs and major changes in any of these areas. The guidelines for qualification of process or product changes are detailed in Mil-M-38510. At LTC we adhere to those guidelines and in many cases impose additional testing per our own requirements. Examples of some of the qualification tests which are used by LTC are shown in Table 3 at the end of this brochure.

As part of new product qualification, LTC performs ESD sensitivity classification testing of devices to Method 3015 of Mil-Std-883. This ESD sensitivity testing uses both the human body model and the machine model. During this rigorous testing, every pin combination on at least 3 devices is subjected to 3 positive pulses followed by 3 negative pulses at the specified voltage increment with a 1 second cool down period between pulses. Following this ESD testing, the device is tested for opens or shorts on a curve tracer and then must pass the full data sheet limits on the automatic test equipment.

Additionally, for CMOS circuits, latch-up testing is performed on every pin to determine the device's ability to source or sink current without destructive latch-up. We require new LTC products to handle increasingly high currents without latch-up and subsequently meet all data sheet parameters.

Reliable radiation hardened devices are produced by LTC using a proprietary process technology designed to meet or exceed 100k RADS total dose. Qualification testing of these devices using a Cobalt 60 source has demonstrated excellent results on a number of products. Data sheets for our RAD hard product line are available from your local sales representative.

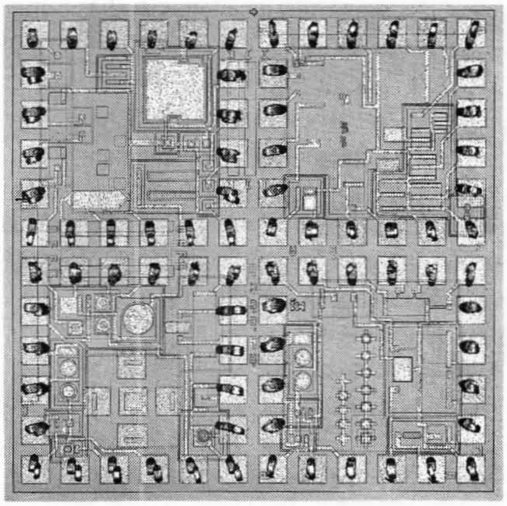
Wafer Level Reliability Assessment

As an additional reliability control, LTC has innovated a strategy for auditing the wafer fab process. Diagnostic structures, in addition to the device structures, are specifically designed as either Bipolar or CMOS reliability test patterns and are stepped into all wafers. These structures are tested during fabrication using a parametric analyzer. Then these test vehicles are used to investigate and detect potential yield and reliability hazards after assembly.

The Bipolar Process version of this structure is optimized to accelerate, under temperature and bias, the two most common failure mechanisms in linear circuits, namely mobile positive ions and surface charge-induced inversions. This three terminal structure is scribed from a wafer and assembled in an either hermetic or plastic package. These devices are burned-in for a predetermined temperature and time. The same structures becomes sensitive to either failure mechanism depending upon the bias scheme used during burn-in. A limit is defined for the leakage current change during burn-in; a failure indicates a wafer fab problem which will be addressed by the process engineering group.

The CMOS Process version allows measurements of thresholds of various sizes and kinds of N-Channel and P-Channel MOSFETs. Body effects, L effective, sheet resistance, zener breakdown voltage, contact metal resistance and impact ionization current are measurable with this chip which is assembled in a twenty lead DIP.

Bipolar Test Pattern



Electrical testing is performed on the structure before and after burn-in. After evaluating any sample population shifts or failures, process engineering is appraised of the results of this process monitor.

The use of test patterns allow any device to be monitored and also gives faster unambiguous feedback than is normally achieved by performing reliability testing on assembled product. Reliability data is generated in less than one week, giving immediate feedback to the production line.

LTC utilizes this new reliability control technique in addition to the conventional reliability audit on randomly pulled finished product. Operating Life tests are performed and the distributions of key parameters before and after testing are evaluated for stability and control.

Quick Reaction Reliability Monitor

As a complement to the wafer level reliability program, a monitor program focused on assembly related issues has been fully implemented. This reliability monitor program, known as the QUICK REACTION RELIABILITY (QR^2) monitor, has been specifically tailored to provide quick feedback of reliability assessment of the assembly operation. The tests in the QR^2 program are designed to identify reliability weaknesses associated with wire bonding, die attach, package encapsulation and contamination related failures. The actual tests performed in the QR^2 Monitor Program are shown in Table 4 at the end of this brochure.

In order to ensure that representative reliability assessment is made, the QR^2 sampling matrix requires QR^2 testing of every date code from each assembly location on each package type and lead count from that assembly location. This provides a weekly snapshot of the reliability of all packages from all assembly locations. The basic strategy is to evaluate as many production lots as possible to provide maximum confidence to our customers.

Should a failure occur during QR^2 testing, the entire production lot is impounded before shipment. Failures are analyzed to determine validity and the root cause of any valid failure. Quite often, additional samples are pulled and tested for an extended period of time. Lots with substandard reliability performance are scrapped. The data generated from this program is used to establish a program for continuous quality improvement with our assembly facilities.

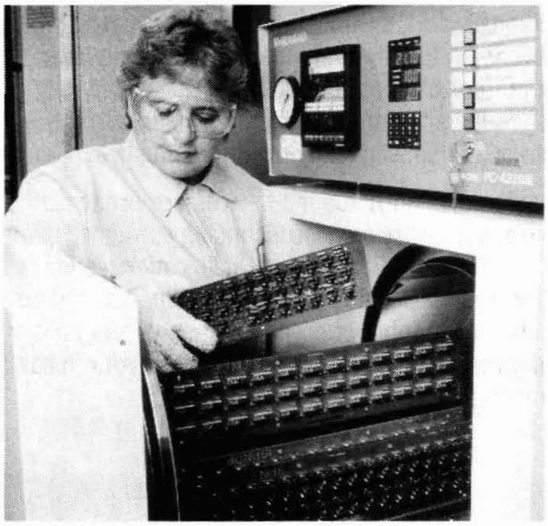
Long Term Reliability Monitor

LTC also conducts a traditional long term reliability monitor program on devices pulled from Boxstock. This long term reliability monitor is used for extended life and end of life approximations such as FIT (failure in time) calculations. The long term reliability monitor also serves as a check against our short term reliability estimates.

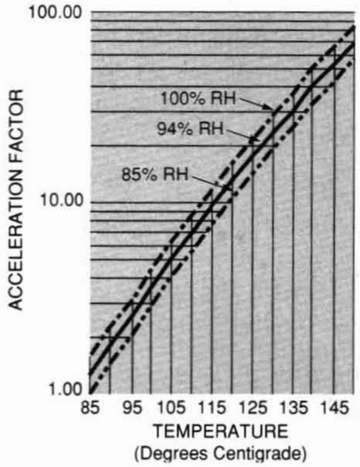
The long term reliability tests are designed to evaluate design, wafer fab and assembly related weaknesses. Industry standard reliability tests and the relatively new HAST (highly accelerated stress test) have been incorporated into this program. The long term reliability monitor tests are shown in Table 5 at the end of this brochure.

The most severe tests for plastic package devices are the temperature and humidity tests, particularly HAST testing. We have included HAST testing in the long term reliability monitor program due to the highly accelerated nature of the this test. This test accelerates the penetration of moisture through the external protective encapsulant or along the interface between the encapsulant and the metallic lead frame. Additionally, the HAST test is conducted with the device under bias. The HAST test places the plastic devices in a humid environment of 85% relative humidity under 45psi of pressure at 130°C to 140°C. Under these conditions, 24 hours of HAST testing at 140°C is roughly equivalent to 1,000 hours of 85°C/85% RH testing. The employment of HAST testing has dramatically reduced the length of time required for qualification.

Qual Samples Being Loaded into the HAST System



Acceleration Factor Using HAST Compared to 85/85



Group C and D Testing

Since LTC is a certified producer of JAN 38510 and 883 product, we perform Group C and D testing regularly on our devices. This data is also incorporated into the reliability datapack in the back of this brochure. The Group C and D test lists are shown in Tables 6 and 7 at the end of this brochure.

Failure Analysis and Corrective Action

LTC is extremely concerned with all failures whether they occur in-house or at a customer location. We have focused significant resources in the area of failure verification and analysis.

LTC offers failure analysis services to its customers, free of charge. In an emergency situation a preliminary failure analysis report can be issued within 24 hours. Our failure analysis database revealed that the vast majority of all devices returned for failure analysis are invalid due to improper application, gross misuse or they are fully functional and meet all data sheet parameters. LTC also offers outstanding applications assistance to help the customer achieve the full value of our products.

Scanning Electron Microscope with X-RAY Dispersive Analysis

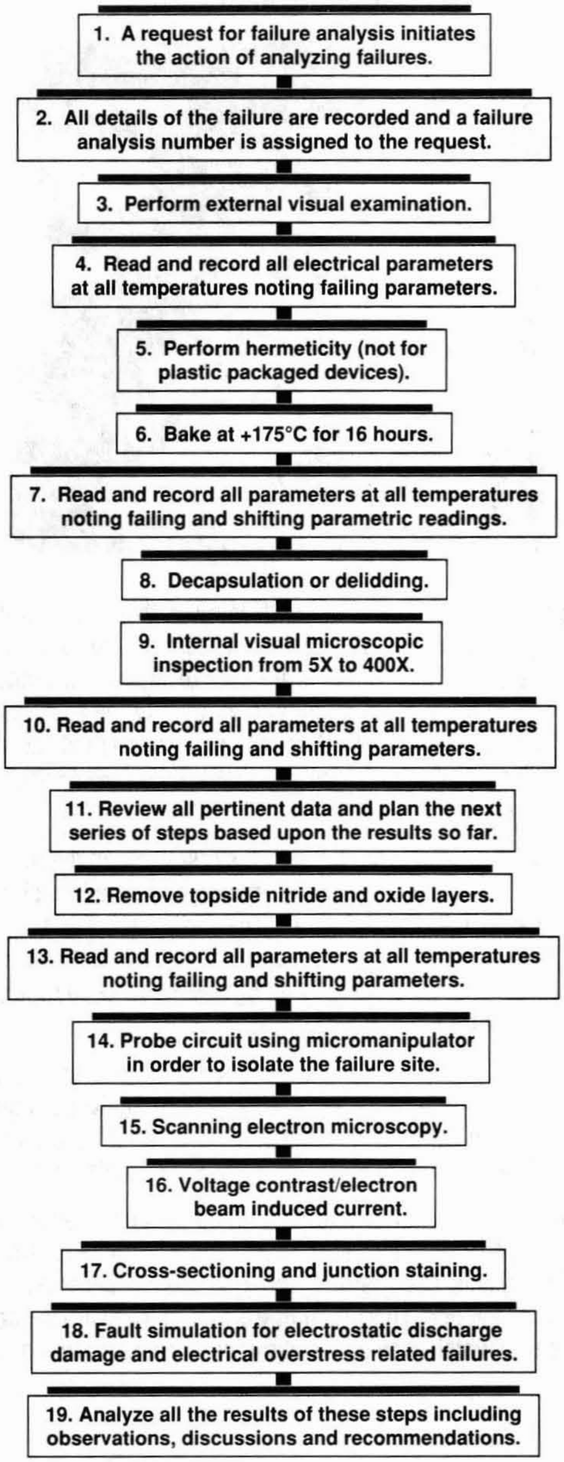
We are equally concerned with failures that are identified during reliability and qualification testing. As with field failures, the in-house failures are analyzed in detail to pinpoint the exact failure mechanism and to identify the root cause. In many cases, where ESD or EOS is the suspected cause of the failure, fault simulation is carried out by over stressing good devices to recreate the fault condition.

LTC has invested in failure analysis resources in the form of experienced, seasoned engineers and equipment such as a full metallurgical lab, IC deprocessing equipment and a scanning electron microscope with voltage contrasts, electron beam induced current (EBIC), energy dispersive x-ray analysis (EDAX), and a computerized database.

All failure analysis reports are documented in detail and distributed appropriately. All valid failure analyses require prompt and effective corrective action which is driven to completion by the quality and reliability organization.

Corrective actions are implemented in accordance with LTC's internal document "Corrective Action Procedure" which details the method and responsibilities for timely corrective action. This procedure is summarized in a separate brochure which is available to our customers upon request.

Typical Failure Analysis Flow



1. A request for failure analysis initiates the action of analyzing failures.
2. All details of the failure are recorded and a failure analysis number is assigned to the request.
3. Perform external visual examination.
4. Read and record all electrical parameters at all temperatures noting failing parameters.
5. Perform hermeticity (not for plastic packaged devices).
6. Bake at +175°C for 16 hours.
7. Read and record all parameters at all temperatures noting failing and shifting parametric readings.
8. Decapsulation or delidding.
9. Internal visual microscopic inspection from 5X to 400X.
10. Read and record all parameters at all temperatures noting failing and shifting parameters.
11. Review all pertinent data and plan the next series of steps based upon the results so far.
12. Remove topside nitride and oxide layers.
13. Read and record all parameters at all temperatures noting failing and shifting parameters.
14. Probe circuit using micromanipulator in order to isolate the failure site.
15. Scanning electron microscopy.
16. Voltage contrast/electron beam induced current.
17. Cross-sectioning and junction staining.
18. Fault simulation for electrostatic discharge damage and electrical overstress related failures.
19. Analyze all the results of these steps including observations, discussions and recommendations.

Failure Rate Calculations

Failure rates at LTC are calculated using Mil-Std-690B which is based upon the exponential distribution model for predicting microelectronic device reliability. Examples of FIT and MTBF (mean time between failure) are shown in the sample calculation below.

Sample Calculation:

Step 1. Calculate Failure Rate at Test Condition (+150°C).

Assume 77 units on Op-Life for 1000 hours with 0 failures:

Device Hours at Test Condition = 77 Units × 1000 Hours equals 77,000 Device Hours at +150°C

$$\text{Fail Rate} = \frac{\text{Value from Table A-1 (Mil-Std-690B)}}{\text{Device Hours}}$$

$$= \frac{91.641}{77{,}000} = 1.19\%\ \text{1K Hours (11,900 FITS)}$$

The Arrhenius model is used to extrapolate a failure rate from an accelerated test condition to a use temperature condition.

Step 2. Calculate Acceleration Factor and Extrapolate Equivalent Failure Rate to +55°C.

Af = Acceleration Factor

$$Af = e^{\frac{E_a}{K}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)}$$

$$Af = e^{\left(\frac{1.0}{0.0000863}\right)\left(\frac{1}{328}-\frac{1}{423}\right)}$$

$$Af = 2791$$

Where:

E_a = Activation Energy (Assume 1.0 eV)
K = Boltzmann's Constant = 8.63×10^{-5} eV/°Kelvin
T_2 = Test Condition Temperature in °Kelvin
T_1 = Use Condition Temperature in °Kelvin
e = 2.71828 (Natural Antilog)

Now the equivalent failure rate is calculated:

$$\text{Failure Rate } (+55^\circ\text{C}) = \frac{\text{Failure Rate at Test Condition}}{\text{Acceleration Factor}}$$

$$= \frac{11{,}900 \text{ FITS}}{2791}$$

$$= 4.2637 \text{ FITS}$$

Finally MTBF is calculated:

$$\text{MTBF} = \frac{100000}{0.000426} = \frac{234{,}700{,}000 \text{ Hours}}{\text{or } 26{,}778 \text{ Years.}}$$

Reliability Datapack

On a quarterly basis, the reliability department compiles and publishes a report which summarizes all the reliability testing results. This report is intended to provide our customers with a means of determining system reliability. The data is presented at +150°C and at +125°C for those customers who wish to perform their own failure rate calculations. This report can be found in the pocket in the back of this brochure.

In addition, up to the minute reliability summary data reports on particular devices can be generated from the computerized reliability database. ESD simulation testing reports and current density calculations of individual device types are also available upon request.

Should you desire additional information, please contact your local LTC representative.

Table 1. "R" Flow for Plastic Dual-In-Line Packages

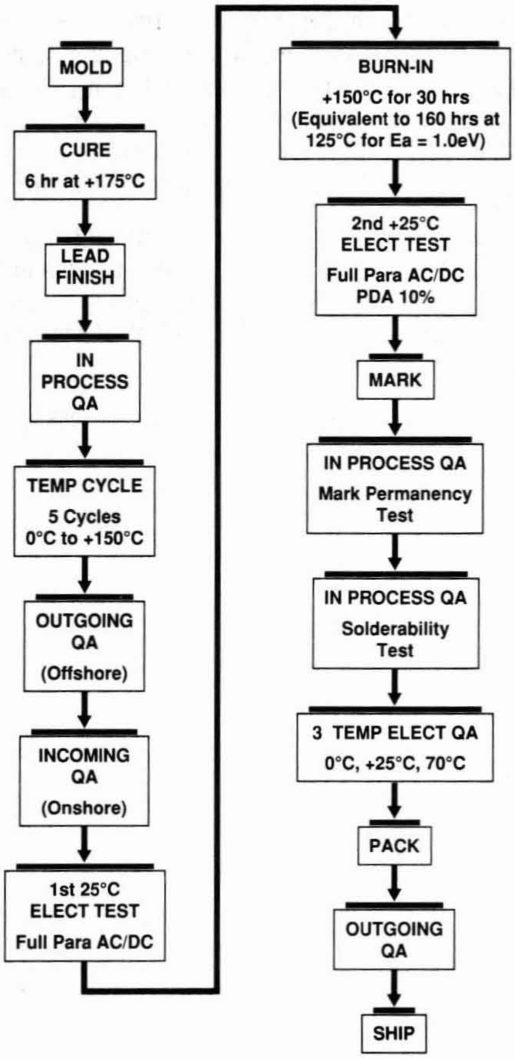

MOLD
CURE
6 hr at +175°C
LEAD FINISH
IN PROCESS QA
TEMP CYCLE
5 Cycles
0°C to +150°C
OUTGOING QA
(Offshore)
INCOMING QA
(Onshore)
1st 25°C ELECT TEST
Full Para AC/DC
BURN-IN
+150°C for 30 hrs
(Equivalent to 160 hrs at 125°C for Ea = 1.0eV)
2nd +25°C ELECT TEST
Full Para AC/DC
PDA 10%
MARK
IN PROCESS QA
Mark Permanency Test
IN PROCESS QA
Solderability Test
3 TEMP ELECT QA
0°C, +25°C, 70°C
PACK
OUTGOING QA
SHIP

Table 2. Screening Flow per Mil-Std-883, Method 5004

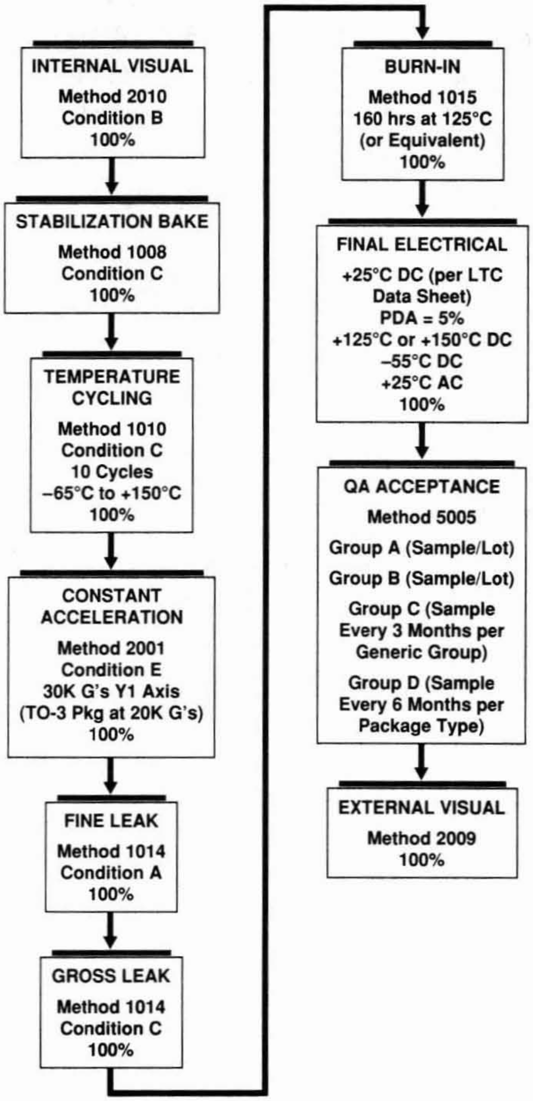

INTERNAL VISUAL
Method 2010
Condition B
100%
STABILIZATION BAKE
Method 1008
Condition C
100%
TEMPERATURE CYCLING
Method 1010
Condition C
10 Cycles
–65°C to +150°C
100%
CONSTANT ACCELERATION
Method 2001
Condition E
30K G's Y1 Axis
(TO-3 Pkg at 20K G's)
100%
FINE LEAK
Method 1014
Condition A
100%
GROSS LEAK
Method 1014
Condition C
100%
BURN-IN
Method 1015
160 hrs at 125°C
(or Equivalent)
100%
FINAL ELECTRICAL
+25°C DC (per LTC Data Sheet)
PDA = 5%
+125°C or +150°C DC
–55°C DC
+25°C AC
100%
QA ACCEPTANCE
Method 5005
Group A (Sample/Lot)
Group B (Sample/Lot)
Group C (Sample Every 3 Months per Generic Group)
Group D (Sample Every 6 Months per Package Type)
EXTERNAL VISUAL
Method 2009
100%

Table 3. Reliability Qualification Test Guidelines for Plastic Packages

TEST	METHOD	CONDITIONS	FULL RELEASE DURATION	CONTINGENT RELEASE DURATION	FULL AND CONTINGENT RELEASE LTPD
High Temperature Bias Operating Life (Op-Life)	Mil-Std-883 Method 1005	Continuous Operation at Max Rated Supply Voltage $T_A = +125°C$ or $T_A = +150°C$	1000 Hours 500 Hours	500 Hours 168 Hours	5%, Acc = 0 5%, Acc = 0
Temperature Humidity Bias Life (85/85)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current $T_A = +85°C$, 85% RH	1000 Hours	500 Hours	5%, Acc = 0
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current $T_A = +140°C$, 85% RH, 3 Atmospheres	Equivalent to 1000 Hours 85/85	Equivalent to 500 Hours 85/85	5%, Acc = 0
Temperature Cycle (T/C)	Mil-Std-883 Method 1010 Condition C	Air-to-Air, –65°C to +150°C, >10 Minutes Dwell Time	1000 Cycles	500 Cycles	5%, Acc = 0
Thermal Shock (T/S)	Mil-Std-883 Method 1011 Condition C	Liquid-to-Liquid, –65°C to +125°C, > 5 Minutes Dwell Time	1000 Cycles	500 Cycles	5%, Acc = 0
Autoclave (Pressure Pot with Bias) (BPPT)	JEDEC Spec 22	Continuous Storage at $T_A = +105°C$, 100% RH, 1.67 Atmospheres, Max Rated Supply Voltage for the Last 3 Hours	350 Hours	350 Hours	5%, Acc = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at $T_A = +121°C$, 100% RH, 2 Atmospheres	350 Hours	350 Hours	5%, Acc = 0
Power Cycle (PW) Regulators Only	Mil-Std-883 Method 1006	Power Cycled "ON" and "OFF" as Required to Cycle Case Temperature Between +60°C and +120°C	50,000 Cycles	10,000 Cycles	15%, Acc = 0
Thermal Resistance (TMLR)	Mil-Std-883 Method 1012 Condition C	Junction to Case or Junction to Ambient as Appropriate	N/A	N/A	15%, Acc = 0
Dye Penetrant (DY)	Mil-Std-883 Method 1014	Immersion in Dye Penetrant at 60 PSIG for 2 Hours Minimum	N/A	N/A	15%, Acc = 0
X-Ray Inspection Radiography (XRAY)	Mil-Std-883 Method 2012	Top View Only	N/A	N/A	15%, Acc = 0

Table 4. Quick Reaction Reliability (QR^2) Monitor Program

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Operating Life Test (Op-Life)	Mil-Std-883 Method 1005	Continuous Operation at Max Rated Supply Voltage, T_A = +125°C or T_A = +150°C	168 Hours	45	5%, Acc = 0
Biased Moisture Life Test (85/85) or	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = +85°C, 85% RH	168 Hours	45	5%, Acc = 0
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = +140°C, 85% RH, 3 Atmospheres	48 Hours	45	5%, Acc = 0
Temperature Cycle (T/C)	Mil-Std-883 Method 1010 Condition C	Air-to-Air, –65°C to +150°C, >10 Minutes Dwell Time	100 Cycles	45	5%, Acc = 0
Thermal Shock (T/S)	Mil-Std-883 Method 1011 Condition B	Liquid-to-Liquid, –65°C to +150°C, >5 Minutes Dwell Time	100 Cycles	45	5%, Acc = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at T_A = +121°C, 100% RH, 2 Atmospheres	48 Hours	45	5%, Acc = 0
X-Ray Inspection Radiography (XRAY)	Mil-Std-883 Method 2012	Top View Only	N/A	45	5%, Acc = 0
Package Separation Visual Inspection	N/A	30X Magnification	N/A	45	5%, Acc = 0
Unmolded Strip Evaluation	N/A	30X Magnification	N/A	1 Strip	N/A
Hot Intermittent Opens Test at Subcontractor	N/A	Automated Electrical Test at +125°C	N/A	250	N/A

Table 5. Long Term Reliability Monitor Program

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Operating Life Test (Op-Life)	Mil-Std-883 Method 1005	Continuous Operation at Max Rated Supply Voltage, T_A = +125°C or T_A = +150°C	1000 Hours	45	5%, Acc = 0
Biased Moisture Life Test (85/85) or	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = +85°C, 85% RH	1000 Hours	45	5%, Acc = 0
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = +140°C, 85% RH, 3 Atmospheres	48 Hours	45	5%, Acc = 0
Temperature Cycle (T/C)	Mil-Std-883 Method 1010 Condition C	Air-to-Air, –65°C to +150°C, >10 Minutes Dwell Time	1000 Cycles	45	5%, Acc = 0
Thermal Shock (T/S)	Mil-Std-883 Method 1011 Condition B	Liquid-to-Liquid, –65°C to +150°C, >5 Minutes Dwell Time	1000 Cycles	45	5%, Acc = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at T_A = +121°C, 100% RH, 2 Atmospheres	1000 Hours	45	5%, Acc = 0

Table 6. Group C per Mil-Std-883C Method 5005

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Group C-1	Mil-Std-883	Continuous Operation at Max Rated			
Operating Life Test	Method 1005	Supply Voltage			
(Op-Life)		$T_A = +125°C$ or	1000 Hours	45	5%, Acc = 0
		$T_A = +150°C$	500 Hours		

Table 7. Group D per Mil-Std-883C Method 5005

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Group D-1	Mil-Std-883	N/A	N/A		
Physical Dimensions	Method 2016			15	15%, Acc = 0
Group D-2	Mil-Std-883		N/A	15	15%, Acc = 0
Lead Integrity	Method 2004	Condition B2 (Lead Fatigue)			
Group D-3	Mil-Std-883			15	15%, Acc = 0
Thermal Shock	Method 1011	Condition B	15 Cycles		
Temperature Cycle	Method 1010	Condition C	100 Cycles		
Moisture Resistance	Method 1004				
Hermeticity	Method 1014				
Visual Exam	Method 1004/10				
End Point Electricals					
Group D-4	Mil-Std-883		N/A	15	15%, Acc = 0
Mechanical Shock	Method 2002	Condition B			
Vib. Variable Frequency	Method 2007	Condition A			
Constant Acceleration	Method 2001	Condition E (Y1 Only)			
Hermeticity	Method 1014				
Visual Exam	Method 1010/11				
End Point Electricals					
Group D-5	Mil-Std-883			15	15%, Acc = 0
Salt Atmosphere	Method 1009	Condition A	24 Hours		
Hermeticity	Method 1014				
Visual Exam	Method 1009				
Group D-6	Mil-Std-883		N/A	3	0
Internal Water Vapor	Method 1018	< 5000ppm			
Group D-7	Mil-Std-883	N/A	N/A		
Adhesion of Lead Finish	Method 2025			15	15%, Acc = 0
Group D-8	Mil-Std-883				
Lid Torque	Method 2024	(Glass Frit Seal Only)	N/A	5	15%, Acc = 0

QUALITY ASSURANCE PROGRAM

At Linear Technology Corporation our overriding commitment is to achieve Excellence in Quality, Reliability and Service (QRS) and total customer satisfaction. We interpret the word "excellence" to mean delivering products that consistently exceed all the requirements and expectations of our customers. The commitment to QRS extends from the President to every employee, from design to product qualification, and from manufacturing to shipping. To meet this commitment, Linear Technology has established a comprehensive program called "Quality for the Nineties."

This program is divided into four separate, but highly interrelated programs, namely Quality Environment, Total Quality Management System (TQMS), Vendor Participation, and Focus for the Nineties.

Quality Environment

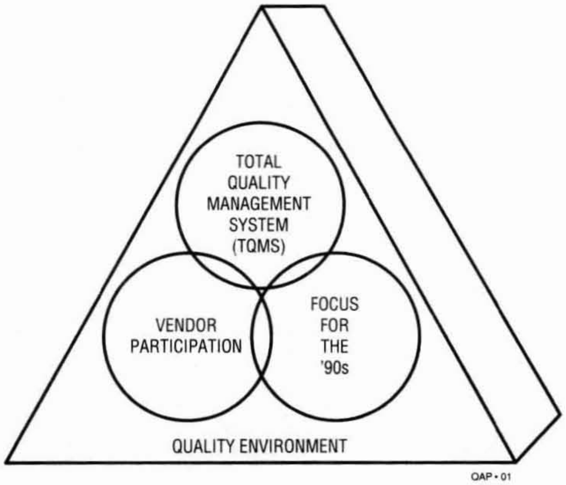
This first program, Quality Environment, serves as the building block for three other programs. It entails establishing an environment that is conductive to the participation of each and every employee in helping to build quality into our products. This program encourages every employee to identify any quality problem and participate in recommending solutions.

A comprehensive operator training and certification program has been established that covers every area of manufacturing from incoming raw material inspection, wafer fabrication, assembly, and test to shipping. Emphasis is placed on compliance with specifications, performance to quality goals, electrostatic discharge damage (ESD) awareness and controls, encouraging operators to think quality and recommend quality improvement ideas.

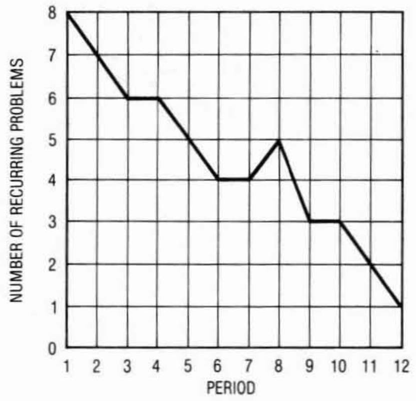
To ensure compliance with specifications, a Quality Audit Team performs a systems audit of key manufacturing areas and suppliers at periodic intervals. Compliance with process specifications and the detailed programs of the Corporate Quality Assurance Policy are verified, and discrepancies reported for quick resolution with special emphasis to eliminate recurring problems. The performance of each area is then rated, providing a strong incentive for each area to excel.

With the philosophy that each department, starting from incoming raw materials, is considered a customer of the preceding department, every effort is made by working closely together to meet or exceed our end-customer requirements and goals.

Quality for the '90s



Systems Quality Audit-Tracking Recurring Problems

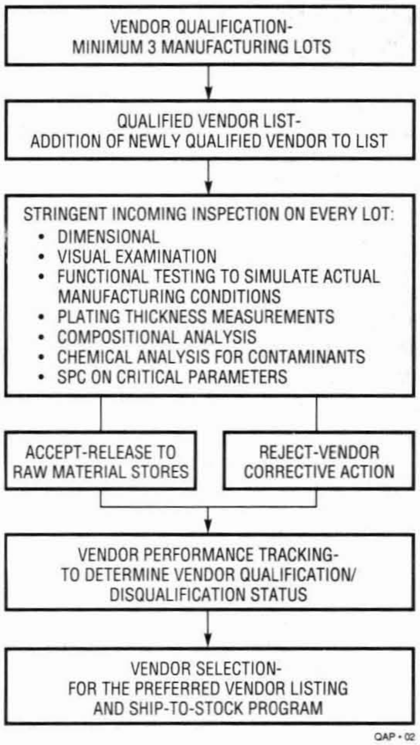


Total Quality Management System (TQMS)

The second program starts with the incorporation of innovative, but conservative, design and layout rules to achieve the best performance without sacrificing quality and reliability. During the design and development cycle, Design, Product, Package, Manufacturing, Quality and Reliability Engineering groups participate in design reviews to ensure that all program aspects are covered; ranging from product performance objectives to ensuring reproducibility and repeatability in wafer fabrication and assembly. Special emphasis is placed on devising input protection circuitry to minimize susceptibility to voltage spikes and ESD, optimizing thermal layout to minimize parametric drift, and optimizing bond pad layout to maximize assembly and electrical test yields, at the same time allowing the die to be assembled in a wide selection of packages.

Once the design is approved, a stringent manufacturing qualification test plan is conducted on the initial engineering runs. The test plan is selected to bring out any weaknesses in the design and any manufacturability problems, and includes reliability stress tests such as high temperature operational life and high temperature humidity bias 85°C/85% RH and HAST (Highly Accelerated Stress Testing) for plastic packages, and MIL-STD-883 method 5005 qualification testing for hermetic packages. Product performance on these tests must be equal to or better than similar products within the same generic group to be considered qualified. Major design, package, material and process changes are also subjected to these same stringent qualification requirements. In addition to achieving the required reliability performance, an engineering change must also achieve manufacturing yield and quality performance levels equal to or better than the original product to be considered qualified.

Raw Material Controls


VENDOR QUALIFICATION-
MINIMUM 3 MANUFACTURING LOTS
QUALIFIED VENDOR LIST-
ADDITION OF NEWLY QUALIFIED VENDOR TO LIST
STRINGENT INCOMING INSPECTION ON EVERY LOT:
• DIMENSIONAL
• VISUAL EXAMINATION
• FUNCTIONAL TESTING TO SIMULATE ACTUAL MANUFACTURING CONDITIONS
• PLATING THICKNESS MEASUREMENTS
• COMPOSITIONAL ANALYSIS
• CHEMICAL ANALYSIS FOR CONTAMINANTS
• SPC ON CRITICAL PARAMETERS
ACCEPT-RELEASE TO RAW MATERIAL STORES
REJECT-VENDOR CORRECTIVE ACTION
VENDOR PERFORMANCE TRACKING-
TO DETERMINE VENDOR QUALIFICATION/
DISQUALIFICATION STATUS
VENDOR SELECTION-
FOR THE PREFERRED VENDOR LISTING
AND SHIP-TO-STOCK PROGRAM
QAP • 02

In manufacturing, process controls start with vendor qualification on raw material piece parts. A Qualified Vendor List is maintained and performance of each vendor is continuously monitored on a Vendor Rating Program. A dimensional, visual, functional and, where applicable, compositional analysis is performed on each direct raw material lot. Automated state-of-the-art wafer fabrication, assembly and test equipment, cassette-to-cassette handling in wafer fabrication and automated handling in assembly are utilized, where possible, to maintain manufacturing consistency and quality. Only fully trained and certified operators are allowed to work on production material.

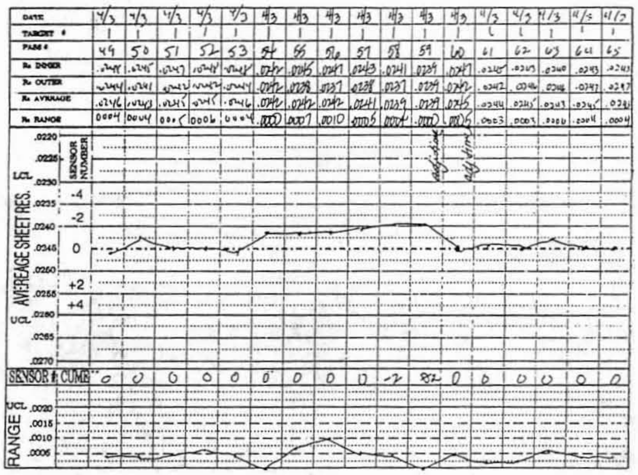
Stringent process controls, typically beyond industry standards, are established for each critical manufacturing step in wafer fabrication, wafer test, assembly, package finishing, mark and pack and shipping as depicted in the Wafer Fabrication, Assembly and Test/End of Line flowcharts.

SEM Monitor of Metallization Quality

The process controls include monitors of critical assembly processes and lot acceptance inspection for operations requiring 100% production inspection. Preseal visual inspection is performed per MIL-STD-883 Method 2010 Test Condition B. Statistical process control techniques are employed in optimizing process parameters, and monitoring process performance through the use of control charts with action limits and upper and lower control limits, and in parametric distribution analysis at electrical test.

Electrical quality is guaranteed by conservative guardbanding on production test programs of a minimum of three machine guardbands, by using state-of-the-art test equipment and 0.04% AQL for lot acceptance testing at 25°C for all military and commercial lots. Additional tests, like rack burn-in, beyond the data sheet specifications on regulator products are performed by exercising the parts in a thermal shutdown mode. These tests are incorporated into the test flow to improve reliability and weed out infant mortality failures. Visual and mechanical quality is optimized by minimizing handling of parts in assembly, test and end of line operations. Lead finish processes have been selected that minimize solderability problems and all lots are subjected to a stringent major visual/mechanical inspection. Administrative errors due to mixed and wrong parts are minimized by strictly adhering to a one lot per station policy, and double checking orders at order entry and shipping. Before shipment of a lot to the customer each lot is inspected to ensure that it meets internal and customer specifications and purchase order requirements. The level of attention paid to each unit is demonstrated by the fact that each unit is traceable to the wafer fabrication lot number via a side or back mark on both 883 and commercial products on all packages, except where there is a physical constraint.

Actual $\overline{X}$ and R Chart of Aluminum Sputter Deposition Using Sensor Number Control



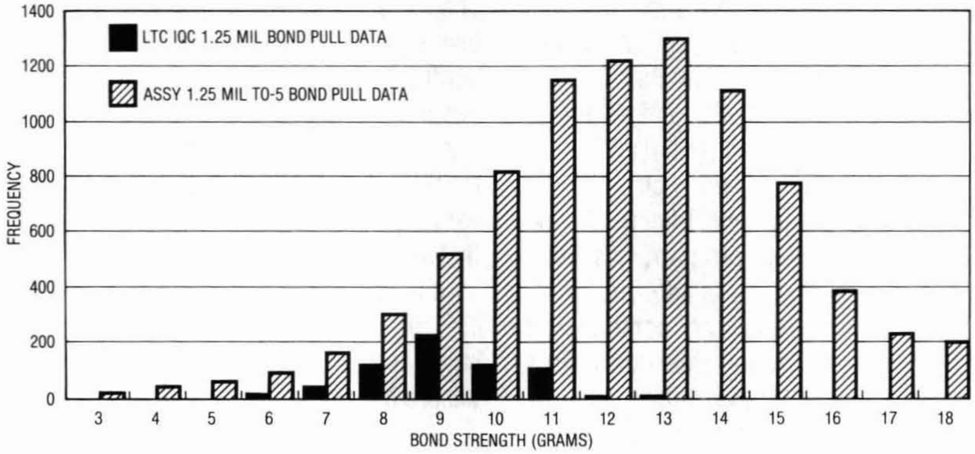
Through the use of automated equipment, strict process controls (utilizing proven statistical process control techniques), periodic systems and quality audits (conducted by the Quality Audit Team), stringent facilities and environmental controls and monitors, Linear Technology is able to ensure quality is built into the product and to guarantee a consistently high quality level.

The manufacturing quality controls are complimented by a reliability audit program designed to weed out design, fabrication, packaging and assembly deficiencies. Additionally, controls are supported by a comprehensive failure analysis and corrective action program designed to provide timely feedback of findings to all operating groups for resolution. The analysis of customer returns, and corrective action taken, completes the closed loop of our Total Quality Management System.

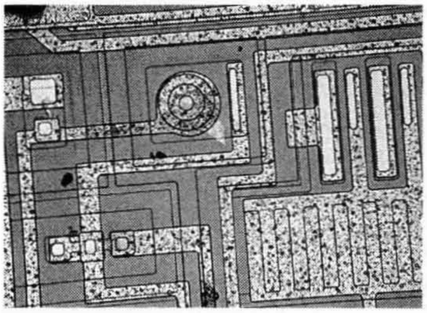
Military and Commerical Products Share the Same Stringent Inspections and Controls

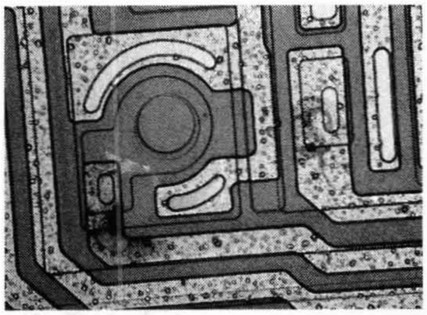
- WAFER FABRICATION PROCESS CONTROLS AND CLASS 100 PROCESSING.
- REGULAR SEM MONITORS.
- PRE-SEAL VISUAL INSPECTION PER MIL-STD-883 METHOD 2010. TEST CONDITION B.
- DIE SHEAR TEST PER MIL-STD-883 METHOD 2019.
- BOND PULL TEST PER MIL-STD-883 METHOD 2011.
- SOLDERABILITY TEST PER MIL-STD-883 METHOD 2003.
- MARK PERMANENCY TEST PER MIL-STD-883 METHOD 2015.
- HERMETICITY TESTING PER MIL-STD-883 METHOD 1014.
- QA ELECTRICAL TEST TO 0.04% AQL AT 25°C, AND TEMPERATURE TESTING.
- EXTERNAL VISUAL PER MIL-STD-883 METHOD 2009.

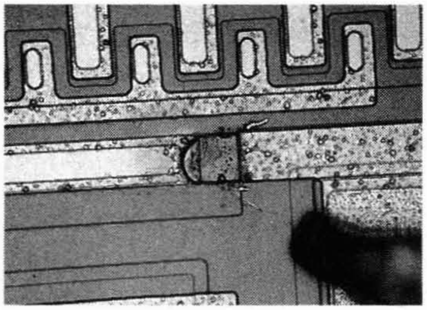
Bond Strength Histogram

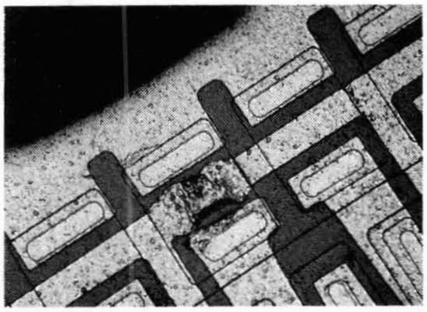


Failure Analysis Photomicrographs









Vendor Participation

The requirements of high quality raw materials for integrated circuit manufacture range from ppb (parts per billion) impurity levels for electronic grade chemicals to ppm (parts per million) defective levels for lead frame packaging materials. It is not only essential, but critical for the semiconductor manufacturer to work closely with their vendors to attain the high quality levels needed in raw materials. At Linear Technology, a program has been established and implemented to allow vendor participation in formulating specifications and establishing percentage defective and lot rejection rate goals. This vendor participation ensures that the direct and raw material quality levels received are consistent with our manufacturing and end-product quality goals. Clearly, achieving optimum quality product requires the use of the best possible materials available and with continuous communication and feedback from our vendors to improve in this key area. A Preferred Vendor Program helps to drive vendors to manufacturing excellence.

Focus for the '90s

The following key quality improvements programs have been established to meet the quality requirements of the '90s.

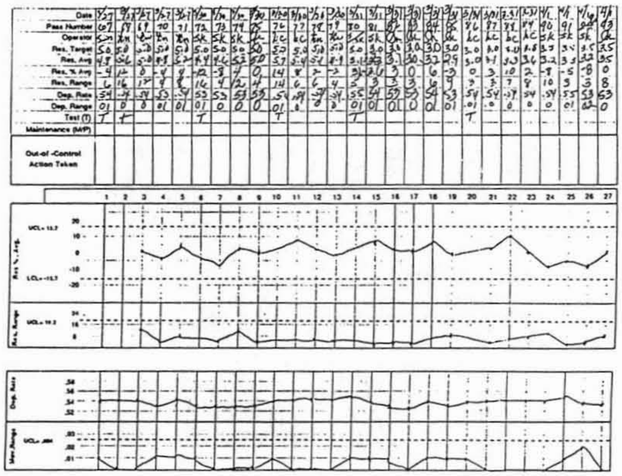
PPM Goals

As demand for quality semiconductor components becomes increasingly more stringent, the percentage goals from the 1970s have given way to ppm goals in the '80s and '90s. At Linear Technology, ppm quality goals are established for every major operation, from incoming inspection to customer returns. Performance to goals is reviewed quarterly and, where goals are not met, quality improvement programs are defined and implemented. Quality goals are updated and tightened on an annual basis, and quality programs are redefined to achieve the new goals established. One of the early benefits of this program is demonstrated by the excellent average outgoing electrical quality (AOQ).

Statistical Process Control (SPC)

The increased reliance on automated manufacturing and test equipment underlines the need for strict process control techniques. SPC is a valuable tool and, at Linear Technology, we realize the importance of these methods. Engineering analysis is performed regularly, using SPC techniques to establish the process capability. Various variable and attribute control charts are used to ensure that processes are within normal limits and action and shutdown limits are established for critical operations. The process capability of key processes are calculated using the Cpk capability index on an ongoing basis to ensure a program for continuous quality improvement.

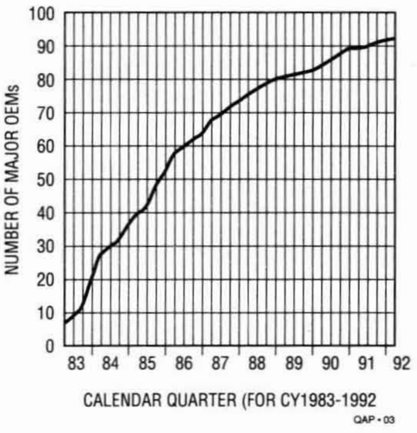
Actual Normalized X and Moving R Chart of Epitaxial Growth Reactor Controlling Resistivity and Deposition Rate



ESD Control

A comprehensive ESD control program has been established which encompasses design, handling, testing, storage, and final packaging for shipment. The program includes the use of grounded table tops, floor mats, wrist straps and heel straps, topical antistatic treatment of floor coverings, banning of static bearing materials from the manufacturing environment, ionizers, and use of conductive or antistatic materials for handling and final packaging. Areas where ESD control must be enforced are designated as ESD Protected areas. ESD awareness training programs help to increase the operator's awareness for successful implementation of this program. Every effort is made to stamp out this silent chip killer. The benefits of this program are improved quality and reliability to the customer.

Quality System Surveys MIL-Q-9858 and MIL-I-45208 Approval

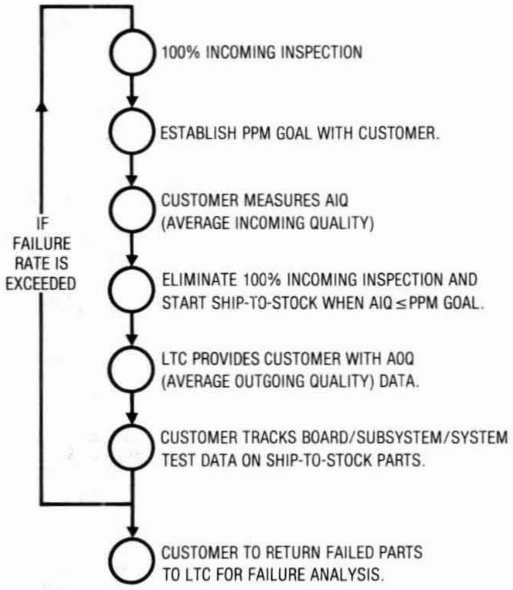


Based on the foregoing quality programs, Linear Technology Corporation is positioned to continuously improve our product quality and exceed the demands of our customer in the '90s and beyond.

Customer Ship-To-Stock Program

Linear Technology is working hand-in-hand with customers to consistently supply high quality products to achieve a ship-to-stock program by eliminating the need to do an incoming inspection. We recognize the benefits to our customers of a ship-to-stock program, namely savings in the need to purchase and maintain incoming test equipment, savings in the need to maintain a safety stock in case of incoming lot rejections, and reduction in board failures and re-work costs because of higher component quality.

Ship-To-Stock Program Flow

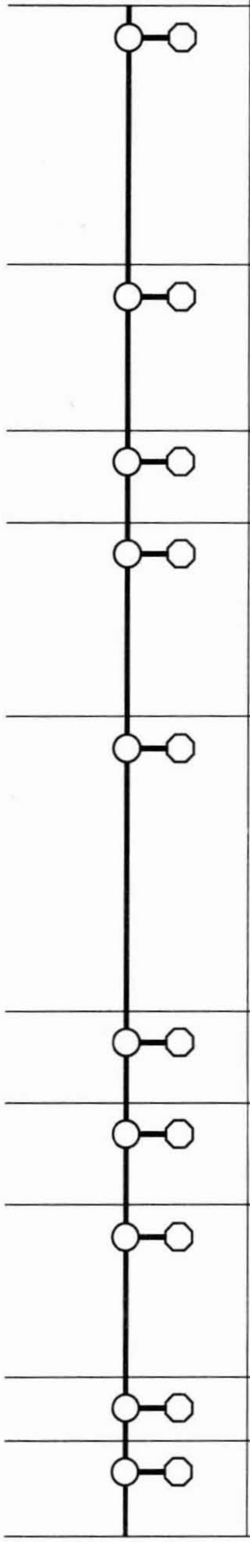

100% INCOMING INSPECTION
ESTABLISH PPM GOAL WITH CUSTOMER.
CUSTOMER MEASURES AIQ (AVERAGE INCOMING QUALITY)
ELIMINATE 100% INCOMING INSPECTION AND START SHIP-TO-STOCK WHEN AIQ ≤ PPM GOAL.
LTC PROVIDES CUSTOMER WITH AOQ (AVERAGE OUTGOING QUALITY) DATA.
CUSTOMER TRACKS BOARD/SUBSYSTEM/SYSTEM TEST DATA ON SHIP-TO-STOCK PARTS.
CUSTOMER TO RETURN FAILED PARTS TO LTC FOR FAILURE ANALYSIS.
IF FAILURE RATE IS EXCEEDED

WAFER FABRICATION FLOWCHART
Generic Bipolar Process

Vendor: Linear Technology Corporation
Package: Plastic DIP
Location of Wafer Fab: Linear Technology Corporation, Milpitas, CA
Assembly: Offshore
Final Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Q.C. Test: Linear Technology Corporation, Milpitas, CA, or Singapore

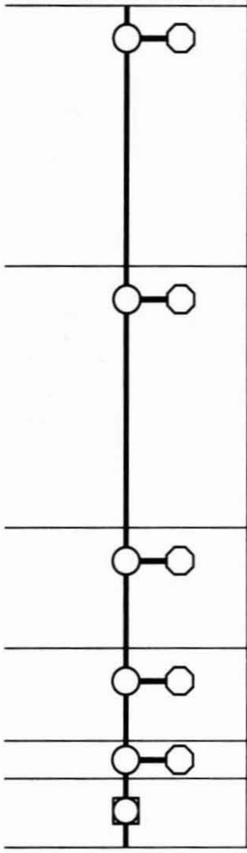
▽ INCOMING
▣ QUALITY INSPECTION AND GATE
○ MANUFACTURING PROCESS
○ QUALITY MONITOR/SURVEILLANCE
☐ REWORK

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
▽	Incoming Raw Material Inspection	Wafers	Visual: Scratches, Pits, Haze, Craters, Dimples, Contamination,	1X Inspection	1.0% AQL to 2.5% AQL Level 1.	% LAR Trend Chart and % Defective Trend Chart
			Oxygen/Carbon Measurement	Infrared Spectrometer	S/S = 2, ACC = 0	
			Resistivity/ Conductivity	Magnetron V/I Meter	S/S = 2, ACC = 0	
			Dimensional	Calipers	2.5% AQL, Level S1	
			Thickness and Taper/Bow	Dial Thickness Gage	2.5% AQL, Level S1	
			Orientation	Break Test	S/S = 1, ACC = 0	
			C of C Verification Against "MPS" Requirements	—	Each Batch	
○		Chemicals	C of C Verification Against "MPS" Requirements	—	Each Batch	
○		Gases	Plus Yearly Gas Analysis			
○—○	Initial Oxidation	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run <2 Defects Per Field of View	Logbook
			Oxide Thickness	Nanospec	3 Wafers/Cycle	
○—○	Collector Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
○	Collector Implant	Implant				Logbook
○—○	Collector Diffusion	Oxidation and Diffusion	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run <2 Defects Per Field	Logbook
		Furnace	Oxide Thickness	Nanospec	2 Wafers/Run	
			R	4 Point Probe	1 Test Wafer/Run	
			XJ	Philtec Groove	1 Test Wafer/ Cycle	



FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	EPI	Deposit EPI Gemini Reactor	Visual	UV Lamp	100% for EPI Spike More Than 5/WFR is Reject	Trend Chart
				Interference Contrast Microscope	More Than 1 Slip and Stacking Fault is Reject	
			R	4 Point Probe	2 Reading/Pass	$X + R_M$
			EPI Thickness	Nicolet	2 Reading/Pass	Trend Chart
	EPI Re-Ox	Oxidation Furnace	Visual	UV Lamp	100%	Logbook
				20X Microscope	2 Wafers/Run <2 Defects Per Field of View	
			Oxide Thickness	Nanospec	2 Wafers/Run	
	Isolation Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	Isolation Predeposition	Boron Deposition Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Trend Chart
				20X Microscope	2 Wafers/Run <4 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	
	Isolation Diffusion	Diffusion Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Logbook
				20X Microscope	2 Wafers/Run <2 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	
			XJ	Philtec Groove	1 Test Chip/Run	Production Logbook
			TOX	Nanospec	2 Product Wafers/ Run	
	Sinker Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	
	Sinker Predeposition	Deposition Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Trend Chart
			R	4 Point Probe	2 Test Wafers/Run	
	Sinker Diffusion	Diffusion Furnace	Visual	UV Lamp	100%	Logbook
				20X Microscope	<3 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	
			TOX	Nanospec	2 Test Wafers/Run	
	Base Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	ISO Diode Check	Curve Tracer BVCSO	BVCSO	Curve Tracer	4 Wafers/Run >1 Per 12 Readings is Fail	Logbook

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
○–○	Base Predeposition	Deposition Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Trend Chart
				20X Microscope	2 Wafers/Run <4 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	$\bar{X} + R$
○–○	Base Diffusion	Diffusion Furnace	Visual	UV Lamp	100% <10 Defects Per Wafer	Trend Chart
				20X Microscope	2 Wafers Per Run <4 Defects Per Field of View	
			R	4 Point Probe	2 Test Wafers/Run	
			TOX	Nanospec	2 Product Wafers Per Run	
○–○	Emitter Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
○–○	CB Diode Check	Curve Tracer	BVCBO	Curve Tracer	<1 Out of 16 Readings is Fail	Logbook
○–○	Emitter Diffusion	Deposition Furnace	R	4 Point Probe	2 Test Chip/Cycle	Logbook
			Beta/LV	Curve Tracer	3 Sites Per Wafer Every Fourth Wafer >2 Readings Out of Spec	
○–○	Contact Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
				Optical Microscope 1000X	Critical Dimension Measure. 2 Wafers Per Run Lot, Accept on 0 Failures	Trend Chart
○–○	Metal Deposition	Deposition Sputter Machine	Visual	UV Lamp	<5 Defects/Wafer 100%	Logbook
			R /Thickness	4 Point Probe	2 Readings/Pass	$X + R_M$
□	Metal Mask	Resist Mask Etchant Bath	Final Inspection	Optical Microscope 200X	"Z" Pattern Scan. 100% of the Wafers	Production Log
				Optical Microscope 1000X	Critical Dimension Measure. 2 Wafers Per Run Lot, Accept on 0 Failures	CD Logbook
○–○	Alloy	Anneal Furnace	Visual	UV Lamp	100% <10 Defects/ Wafer	Logbook
○–○	Electrical Test	To Evaluate Electrical Parameters LOMAC			2 Wafers/Run	Logbook



FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	LPOM	Passivation LPCVD Furnace	Visual	UV Lamp	100%, >2 Color Changes is Fail	Trend Chart
				10X Microscope	3 Wafers/Cycle <3 Defects Per Field of View	
			TOX	Nanospec	3 Wafers/Cycle	$\overline{X} + R$
			Phosphorous Concentration	10:1 HP Etch Rate	3 Wafers/Cycle	Trend Chart
	PEN	PECVD Nitride Deposition	Visual	UV Lamp	100%, >2 Color Changes is Fail	Trend Chart
				10X Microscope	2 Wafers/Run, <5 Defects Per Field of View	
			Thickness	Nanospec	3 Wafers/Cycle	
			Index of Refraction	Ellipsometer	3 Wafers/Cycle	
	Pad Mask	Resist Mask RF Plasma Etch and Oxide Wet Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	Electrical Test	Evaluate Electrical Parameters			100%	Logbook
	Backlap	Disco.	N/A	N/A	N/A	Logbook
	Backside Metal	Backside Metallization	Visual	Un-Aided Eye	100%	Logbook

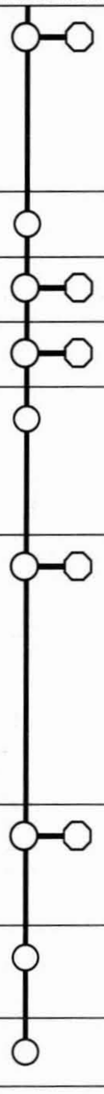
ASSEMBLY FLOWCHART
Plastic DIP

Vendor:	**Linear Technology Corporation**
Package:	**Plastic DIP**
Location of Wafer Fab:	**Linear Technology Corporation, Milpitas, CA**
Assembly:	**Offshore**
Final Test:	**Linear Technology Corporation, Milpitas, CA, or Singapore**
Q.C. Test:	**Linear Technology Corporation, Milpitas, CA, or Singapore**

▽ INCOMING
▣ QUALITY INSPECTION AND GATE
○ MANUFACTURING PROCESS
⬡ QUALITY MONITOR/SURVEILLANCE
□ REWORK

FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
▽	Wafer Sort	Electrical Test Rejects are Red Inked		Wafer Prober		% Defective Trend Chart
○—⬡	Wafer Sort Monitor	Monitor Probing and 2nd Optical Quality	Probe Defects 2nd Optical Defects	3X to 75X Microscope	Minimum of 3 Times Per Shift. S/S = 1, ACC = 0	
○	Kit for Overseas Assembly	Wafers are Kitted with LTC Bonding Diagram and LTC Assembly Traveler				
▽	Incoming Piece Parts Inspection	Lead Frame	Visual	10X to 30X Microscope	1% AQL, Level 2	% LAR Trend Chart
			Mechanical	Optical Comparator, Calipers, X-Ray Fluorescence		
			Functional (Assembly Process Simulation): Bond Pull Test Die Shear Test			
	Incoming Piece/Parts Inspection (Continued)	Molding Compound	Spiral Flow Moldability	Spiral Mold Press	1% AQL, Level 2 8 Drums for Every Transfer	% LAR Trend Chart
		Bonding Wire	Tensile Strength	Tensile Strength Tester	S/S = 1 to 5 Spools Depending on Lot Size, ACC = 0	% LAR Trend Chart X and R Bond STR Chart
		Wire	Elongation	Bonder, Bond Pull Tester		
		Epoxy Die Attach	Bondability	Die Attacher, Die Shear Tester	S/S = 20, ACC = 0	% LAR Trend Chart

FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
○—⬡	Wafer Saw	Die Separation	Alignment Accuracy	TV Alignment Micro Automation on Disco Saw 10X to 30X Microscope		% Defective Trend Chart
	Wafer Saw Monitor		Saw Quality Saw Accuracy	10X to 30X Microscope	Once Every 2 Hours, S/S = 1 Wafer, ACC = 0 S/S = 25 Die, ACC = 0	
○	2nd Optical Inspection	Die Quality	Die Visual Quality	75X Microscope	Every Lot 100% Basis	% LAR and % Unit Defective Trend Chart Yield Analysis
○—⬡	Die Attach	Die Bonded to Lead Frame with Epoxy		Auto Die Bonder		
	Die Attach Monitor		Visual Quality Die Shear Test	10X to 30X Microscope Die Shear Tester	4 Times Per Shift S/S = 20, ACC = 0 Per Bonder	% Defective Trend Chart. X and R Die Shear Strength Chart
○—⬡	Wire Bond	Ball Bonds		Auto Thermosonic Ball Bonder		—
	Wire Bond Monitor		Wire Dress Bond Pull Strength	10X to 30X Microscope Bond Pull Tester	4 Times Per Shift S/S = 25, ACC = 0	% Defective Trend Chart. X and R Die Shear Strength Trend Chart
○	100% 3rd Optical Inspection	Check for Workmanship Quality Prior to Molding	Die, Die Bond, Wire Bond Visual Quality	30X to 60X Microscope	Every Lot 100% Basis	Yield Chart
□	QA 3rd Optical Inspection		Assembly Visual Quality	30X to 60X Microscope	Every Lot LTPD = 5% S/S = 45, ACC = 0	% LAR and % Unit Defective Trend Chart
○—⬡	Mold	Encapsulation with Epoxy Novalac B Composition		Transfer Mold	2 Times Per Shift Per Mold 1 Shot, ACC = 0	
	Mold Monitor	Molding Quality	Visual: Chip, Void and Cracks, Misalignment, etc.	30X to 60X Microscope		% LAR Trend Chart
○	Top Mark	Traceability Mark	Visual Quality	Un-Aided Eye	S/S = 15, ACC = 0	Logbook
○—⬡	Post Mold Bake	Cure Molding Compound		Bake in +175°C Oven for 6 Hours		
	Mold Bake Monitor	Process Monitor	Check Oven Temperature	Mold Cure in Oven	Each Oven at Start and 1 Time Per Shift	% Failed Monitor Trend Chart



FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Deflash	Remove Mold Flash from Package	L/F and Heatsink Must be Free from Mold Flash			
	Deflash Monitor	Process Monitor	Visual: Incomplete Deflash, Package Damage	7X to 30X Microscope	2 Strips Every 2 Hours, ACC = 0	% Unit Defective Trend Chart
	Solder Plate	Lead Finish				
	Solder Plate Inspection	Solder Plate Quality	Coverage, Thickness, Quality	Un-Aided Eye	100%	% Defective Trend Chart
	Solderability Test	Solder Plate Quality	Minimum 95% Coverage	3X to 10X Microscope	S/S = 11, ACC = 0	% LAR Chart
	Trim and Form Singulation	Singulate Unit and Place in Black Conductive Tube				
	Mark	Date Code and Device Marking		Offset Marking with Markem 7226 or Laser Mark	Every Half Hour, S/S = 15 Units, ACC = 0 Per Machine	
	Mark Monitor	Check Marking Quality	Visual: Illegible Mark, Correct Mark, Marking Permanency Test (If Ink Marked)	Un-Aided Eye, 6 Inches Under Normal Room Lighting Method 2015 Mil-Std-883	2 Times Per Shift Per Machine S/S = 20, ACC = 0	% Unit Defective P.A. Trend Chart
	Final Visual Inspection	100% Inspect	Visual: Bent Leads, Mold Flash, Solder Quality, etc.	Un-Aided Eye to 10X Microscope	Every Lot 100% Basis	% LAR and % Unit Defective P.A. Trend Chart
	Pack	Packing and Preparation for Delivery		Antistatic Shipping Tube		
	Ship to LTC					

EOL FLOWCHART
(End of Line)

Vendor:	**Linear Technology Corporation**
Package:	**Plastic DIP**
Location of Wafer Fab:	**Linear Technology Corporation, Milpitas, CA**
Assembly:	**Offshore**
Final Test:	**Linear Technology Corporation, Milpitas, CA, or Singapore**
Q.C. Test:	**Linear Technology Corporation, Milpitas, CA, or Singapore**

▽ INCOMING
⊡ QUALITY INSPECTION AND GATE
○ MANUFACTURING PROCESS
⬡ QUALITY MONITOR/SURVEILLANCE
☐ REWORK

FLOWCHART	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
⊡	LTC Incoming Inspection	Check Quality of Incoming Assembled Material	Package Dimension	Optical Comparator and Calipers	S/S = 2, ACC = 0	% LAR Trend Chart
			External Visual	3X to 30X Microscope	S/S = 76, ACC = 0	
			Mark Permanency (If Ink Mark)	Mil-Std-883 Method 2015	S/S = 4, ACC = 0	
			Solderability	Mil-Std-883 Method 2003	S/S = 3, ACC = 0	
			Die Attach Quality	Pliers	S/S = 5, ACC = 0	
			Lead Fatigue Test	Lead Fatigue Tester	S/S = 10, ACC = 0	
○	100% Class Test	Electrical Test	Test to Guardbanded Data Sheet Test Limits	LTX Integrated Circuit Test System		
⊡	QA Electrical Test at +25°C	Electrical Quality	Test to Guardbanded Data Sheet Test Limits	LTX Integrated Circuit Test System	S/S = 125, ACC = 0	PPM Chart
⊡	QA Electrical Test at +70°C and at 0°C	Electrical Quality	Test to Guardbanded Data Sheet Test Limits	LTX Integrated Circuit Test System	S/S = 125, ACC = 3 Skip Lot	PPM Chart
○	100% External Visual Inspection	Check for Package Quality	Visual: Bent Leads, Lead Form Criteria, Mold Voids/Cracks, etc.	3X Eyepiece		Yield Chart
⊡	QA Post Pack Inspection	Package/ Pack Quality Inspection	Verify Correct Top Mark, Correct Pack Method, Correct Labeling, External Visual Inspection	3X to 10X Microscope Inspection	S/S = 125, ACC = 0	% LAR and PPM P.A. Chart
⊡	QA Shipbench Inspection	Plant Clearance Inspection	Paperwork Check, Verify Correct Part Number and Correct PAR Count	Un-Aided Eye Inspection	LTPD = 2% S/S = 116, ACC = 0	% LAR Trend Chart
○	Ship to Customer					

Linear Technology R-Flow

Reliability has been a key focal point at Linear Technology Corporation since our inception in 1981. Our standard product reliability is monitored closely and we have generated an extensive reliability data base for both hermetic and plastic devices. This data is published on a quarterly basis and we are seeing very low reliability failure rates in the under 1 FIT range at 55°C.*

In response to customer requests, we have added an even higher level of reliability screening for commercial hermetic and plastic components. LTC's R-Flow adds an equivalent 160 hours 125°C burn-in to the standard commercial process flow. Following burn-in, a 100% room temperature test is performed and a 10% PDA (Percent Defective Allowed) is applied. This PDA limit affords an additional level of insurance on a lot-by-lot basis and prevents the occasional disparate lot from being shipped for critical applications. The additional room temperature insertion also decreases the probability of any electrical defectives in the R-Flow lot.

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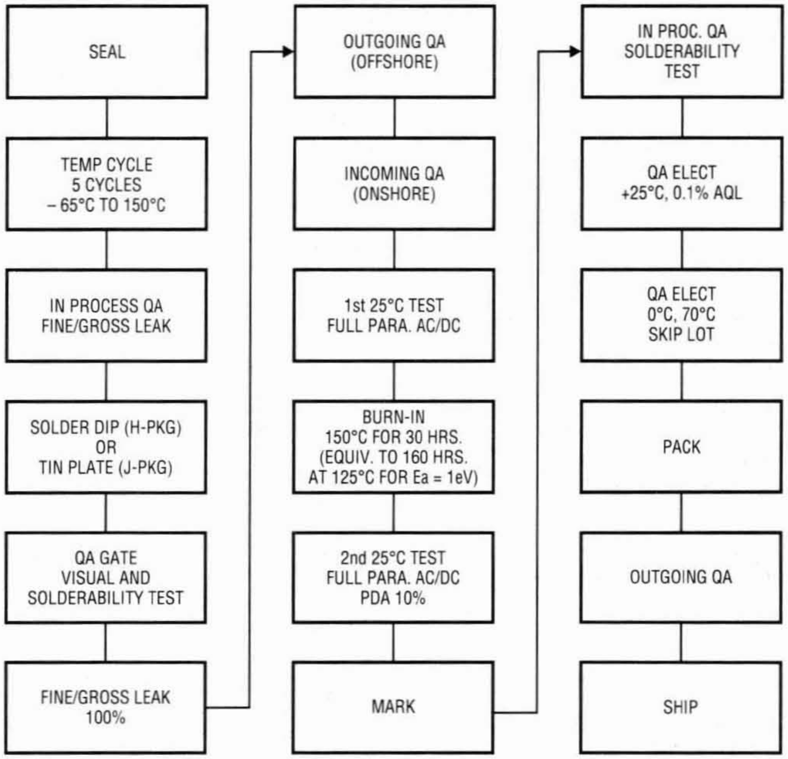
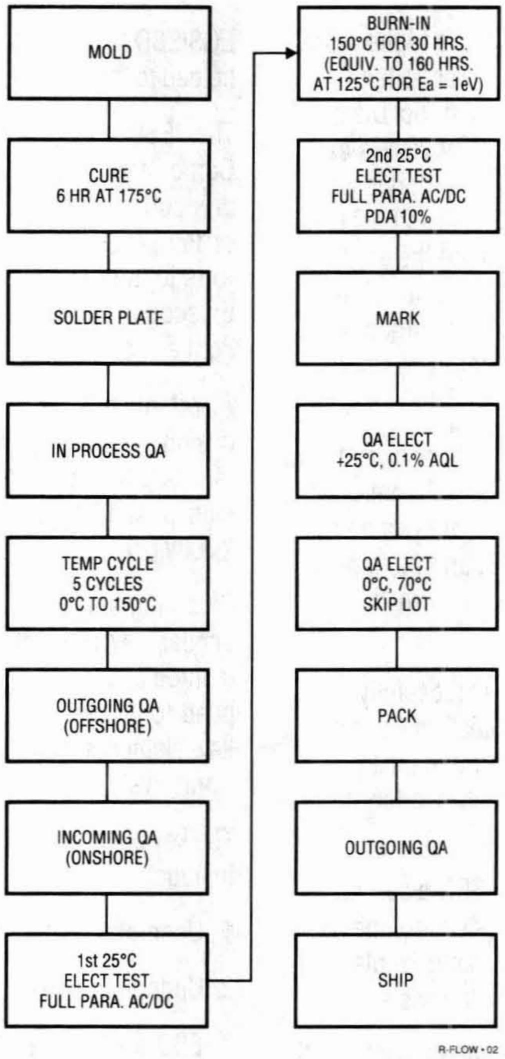
*1 FIT = 1 failure in 10^9 device hours.

R-Flow for TO-5 and CERDIP Packages


SEAL
TEMP CYCLE
5 CYCLES
– 65°C TO 150°C
IN PROCESS QA
FINE/GROSS LEAK
SOLDER DIP (H-PKG)
OR
TIN PLATE (J-PKG)
QA GATE
VISUAL AND
SOLDERABILITY TEST
FINE/GROSS LEAK
100%
OUTGOING QA
(OFFSHORE)
INCOMING QA
(ONSHORE)
1st 25°C TEST
FULL PARA. AC/DC
BURN-IN
150°C FOR 30 HRS.
(EQUIV. TO 160 HRS.
AT 125°C FOR Ea = 1eV)
2nd 25°C TEST
FULL PARA. AC/DC
PDA 10%
MARK
IN PROC. QA
SOLDERABILITY
TEST
QA ELECT
+25°C, 0.1% AQL
QA ELECT
0°C, 70°C
SKIP LOT
PACK
OUTGOING QA
SHIP

R-FLOW • 01

R-Flow for Plastic Dual-In-Line Packages


MOLD
CURE 6 HR AT 175°C
SOLDER PLATE
IN PROCESS QA
TEMP CYCLE 5 CYCLES 0°C TO 150°C
OUTGOING QA (OFFSHORE)
INCOMING QA (ONSHORE)
1st 25°C ELECT TEST FULL PARA. AC/DC
BURN-IN 150°C FOR 30 HRS. (EQUIV. TO 160 HRS. AT 125°C FOR Ea = 1eV)
2nd 25°C ELECT TEST FULL PARA. AC/DC PDA 10%
MARK
QA ELECT +25°C, 0.1% AQL
QA ELECT 0°C, 70°C SKIP LOT
PACK
OUTGOING QA
SHIP
R-FLOW • 02

ESD PROTECTION PROGRAM

Introduction

As integrated circuit technologies achieve higher speed, smaller geometries, lower power and lower voltage, there is a trend toward greater ESD (Electrostatic Discharge Damage) susceptibility. State-of-the-art CMOS ICs can be susceptible to as little as 50V, a static level that is way below the 500V to 15,000V commonly found in an ESD unprotected work environment. As these state-of-the-art ICs get designed into systems, the ESD susceptibility of system hardware also increases proportionately. Industry estimates of losses due to ESD are in the range of a few billion dollars annually.

It has now become increasingly more important for all semiconductor manufacturers and users of semiconductor and other electronic components to fully understand the nature of ESD, the sources of ESD, and its impact on quality and reliability, to effectively deal with this *silent chip killer.*

Linear Technology Corporation has successfully undertaken a simple but effective ESD Protection Program as part of an overall program designed to enhance product quality and reliability. Described in this section are the keypoints of this program.

The objective is to provide increased ESD awareness by showing the sources of ESD in the work environment, and to recommend keypoints for the successful implementation of an ESD program on a company-wide basis.

The end result of a successful ESD program would be the reduction of line failures, final inspection failures and field failures, improved manufacturing yields, improved product quality and reliability and lower warranty costs. We hope that this will help to convince the reader that an ESD Protection Program must be an integral part of every electronic company's product quality and reliability program.

Key Elements of a Successful ESD Protection Program

Recent improvements in failure analysis techniques to correctly identify ESD failures together with an increase in ESD related information from technical publications, EOS/ESD symposiums and vendors have significantly helped to increase ESD awareness.

The ESD Protection Program at Linear Technology Corporation was successfully launched in 1983 when production of ICs was first started. A constant upgrading of the program is still underway. During the ongoing efforts to improve product quality and reliability, previously unrecognized ESD related problems have been brought to light and corrected.

An effective ESD Protection Program must start at product design, and encompass all manufacturing and handling steps up to and including field service and repair. Our design goal is to achieve an ESD susceptibility level of 2,000V or greater.

Since the sources of static in any work environment are similar, key elements of the program successfully implemented at Linear Technology Corporation can also be applied to all users of electronic components. Where these key elements apply, static controls generic to an electronic systems manufacturer are included.

The key elements of a successful ESD Protection Program include:

1. Understanding static electricity.
2. Understanding ESD related failure mechanisms.
3. ESD sensitivity (ESD) testing.
4. Establishing an ESD task force to outline the requirements of the program, sell the program to management, implement the program, review progress against milestones, and follow-up to ensure the program is continuously improved and upgraded. Selecting an ESD coordinator to interface with all departments affected.
5. Conducting a facility evaluation to help identify the sources of ESD and establish static control measures.
6. Setting up an audit program.
7. Selection of ESD protective materials and equipment.
8. Establish a training and ESD awareness program.

What is Static Electricity?

Lightning and sparks from a metallic doorknob during a dry month are examples of static electricity. The magnitude of a static charge is dependent on many variables, among them the size, shape, material composition, surface characteristics and humidity. There are basically three primary static generators, namely triboelectric, inductive and capacitive charging.

Triboelectric Charging

The most common static generator is triboelectic charging. It is caused when two materials (one or both of which are insulators) come in contact and are suddenly separated or rubbed together, creating an imbalance of electrons on the materials and thus static charge.

Some materials readily give up electrons whereas others tend to accumulate excess electrons. The Triboelectric Series lists materials in descending order from positive to negative charging due to this triboelectric effect. A sample triboelectric series is shown here. A material that is higher on the list, e.g., a human body, will become positively charged when rubbed with a material, e.g., polyester, that is lower on the list, due to the transfer of electrons from the human body to the polyester material.

Triboelectric Series

Human Body
↑ Positive + Glass
Mica
Nylon
Wool
Fur
Silk
Aluminum
Paper
Cotton
Steel
Wood
Hard Rubber
Orlon
Polyester
Polyethylene
↓ Negative – PVC (Vinyl)
Teflon

Inductive Charging

Static can also be caused by induction, where a charged surface induces polarization on a nearby material. If there is a path to ground for the induced charge, an ESD event may take place immediately. An example of an induced charge is when the plastic portion of a molded IC package acquires a charge either through triboelectric charging or other means, produces an electrostatic field and induces a charge on the conductive leads of the device. When the device leads are grounded, a short duration damaging static pulse can take place.

Capacitive Charging

The capacitance of a charged body relative in position to another body also has an effect on the static field. To see that this is true, one need only look at the equation Q = CV (charge equals capacitance times voltage). If the charge is constant, voltage increases as capacitance decreases to maintain equilibrium. As capacitance decreases the voltage will increase until discharge occurs via an arc. A low voltage on a body with a high capacitance to ground can become a damaging voltage when the body moves away from the ground plane. For example a 100V charge on a common plastic bag lying on a bench may increase to a few thousand volts when picked up by an operator, due to a decrease in capacitance.

These sources of static can be found almost anywhere in an unprotected work environment, on personnel wearing synthetic clothing and smocks, on equipment with painted or anodized surfaces, and on materials such as carpets, waxed vinyl floors, and ungrounded work surfaces.

Understanding the Failure Mechanisms

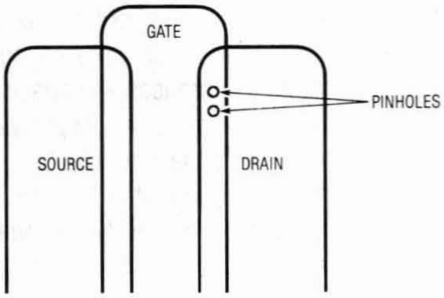
In the past, analysis of electrical failures to pinpoint ESD as a cause was often difficult. But with a better understanding of failure mechanisms and their causes, and the use of more sophisticated techniques like scanning electron microscopy (SEM), pinpointing ESD failures can now be part of a routine failure analysis.

Parametric or functional failure of bipolar and MOS ICs can occur as a result of ESD.

The primary ESD failure mechanisms include:

1. **Dielectric Breakdown:** This is a predominant failure mechanism on MOS devices when the voltage across the oxide exceeds the dielectric breakdown strength. This failure mechanism is basically voltage dependent where the voltage must be high enough to cause dielectric breakdown. As such, the thinner the oxide, the higher the susceptibility to ESD. MOS device failures are characterized by resistive shorts from the input to V_{DD} or V_{SS}.

MOS Transistor Structure
Showing ESD Included Pinholes at Gate Oxide



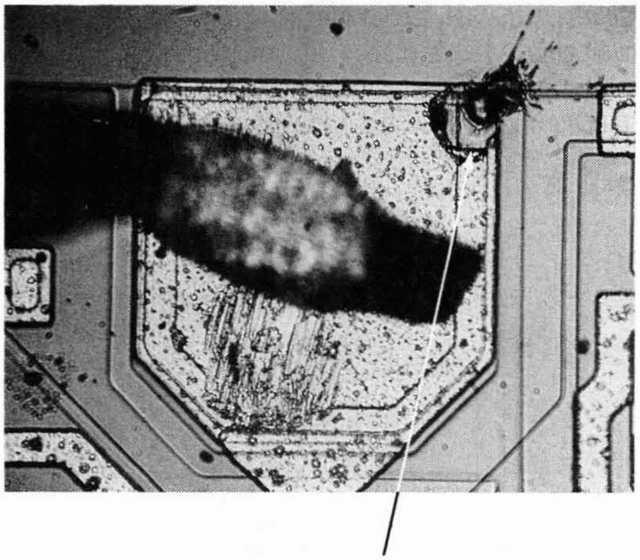
   This failure mechanism can also be found on bipolar ICs which have metallization runs over active semiconductor regions separated by a thin oxide. Device failures are characterized by resistive or high leakage paths.

2. **Thermal Runaway (Second Breakdown):** This failure mechanism results in junction melting when the melting temperature of silicon (1415°C) is reached. This is basically a power dependent failure mechanism, namely the ESD pulse shape, duration and energy can produce power levels resulting in localized heating and eventually junction melting, even though the voltage level is below that required to cause dielectric breakdown. Breakdown of the emitter-base junction of a NPN transistor is a common ESD related failure mode on bipolar ICs, since the highest current density occurs on the smallest current carrying area which is typically the emitter-base junction. Low current gain (h_{FE}) is a very sensitive indicator of emitter-base junction damage on bipolar linear ICs.

3. **Parametric Degradation:** On precision, high speed ICs (e.g., bipolar operational amplifiers with a typical input bias current of 10pA and low input offset voltage of typically $50\mu V$) ESD can cause device degradation, besides functional failures. This can impact electrical performance and adversely affect device reliability.

   This degradation in device parametric performance is far more difficult to pinpoint as an ESD related failure mode. It is also the least understood among the failure modes. The extent of this degradation is dependent on the number of ESD pulses and the level of damage sustained. The first ESD pulse may not cause an IC to fail the electrical data sheet limits, but with each subsequent ESD pulse, the parametric performance can degrade to the point where the device no longer meets the data sheet limits.

   There is a great deal of current research focused on ESD induced latent failures, and there now appears to be more evidence of this type of failure mechanism.



RESISTIVE SHORT ON A
METALLIZATION STRIP OVER
A THIN OXIDE N+ REGION
ON A BIPOLAR IC

ESD Failure Analysis Program

ESD defect identification must be an integral part of a failure analysis program. The key objectives are to help identify the ESD failure mechanism, isolate the cause for failure, and implement corrective action to prevent recurrence. All devices suspected of being damaged by ESD after initial electrical verification, should be failure analyzed.

An ESD failure analysis program is outlined below.

1. Initial electrical test verification.
2. Review device history to determine if there are any similar failures in the past. Review ESD sensitivity data if available.
3. Investigate conditions in any area that can potentially cause ESD damage. Common potential problem areas include:
    - Proper grounding procedures not being followed (e.g., conductive table/floor mats not grounded, personnel not wearing wrist strap, etc.)
    - Improper handling (e.g., handling devices at a non-ESD protected station)
    - Transporting devices in unapproved containers (e.g., in common plastic bags/tubes/tote boxes)
    - Changes in procedures or operation
    - Changes in equipment
    - Design deficiencies
4. Failure analysis sequence:
    - Bench testing and curve tracer analysis
    - Pin-to-pin analysis
    - Internal visual (10 x to 1000 x)
    - Liquid crystal hot spot detection
    - Scanning electron microscopy (SEM), secondary ion mass spectrometry (SIMS), energy dispersive X-ray analysis (EDX), scanning auger microprobe (SAM), radiography, voltage contrast, electron beam induced current (EBIC)
    - Plasma/chemical etching
    - Special fault decoration
    - Micro-sectioning
    - Documentation

    An excellent failure analysis manual is published by the Rome Air Development Center titled "Failure Analysis Techniques—A Procedural Guide."
5. Duplication of failure by stressing identical devices. The same or similar electrical failure mode is a good indicator of an ESD induced failure mode.
6. Implement corrective action to prevent recurrence. Corrective action may include:
    - Component, board, sub-system or system level redesign
    - Improve ESD controls
    - Improve part handling
    - Improve ESD awareness
    - Improve compliance with ESD protection procedures
    - Increase audit frequencies
    - Improve packaging materials and procedures

Corrective action taken by the end user should include a thorough review of electrical and mechanical packaging designs. In addition the end user should consult with the IC manufacturer on their findings, request failure analysis of suspected ESD failures if needed and require the IC manufacturer to take appropriate corrective action on any confirmed ESD failure.

ESD Sensitivity (ESDS) Testing

ESDS testing is crucial in helping the IC designer and the end user evaluate the ESD susceptibility of a particular device. At Linear Technology Corporation ESDS testing is incorporated into the failure analysis program and is performed on each device as part of the product characterization program. The ESDS testing is also part of new product qualification. Linear Technology performs this ESDS testing according to MIL-STD-883 Method 3015.

The ESDS testing provides immediate feedback to the IC designer on any weakness found in the design and permits design correction before product release. The ESDS data collected is also used as baseline data to evaluate the effect of any future design changes on the ESDS testing performance, and to help ensure that the final packaging methods meet MIL-M-38510 requirements. Devices are categorized as either Class One, Class Two or Class Three, each with a susceptibility range from 0 to 2000 volts, above 2000 but below 4000 volts, and above 4000 volts respectively. Topside marking with equilateral triangles is specified by MIL-M-38510.

Since people are considered to be a prime source of ESD, the ESDS test circuit is based on a human ESD model. A 1500Ω resistor and a 100pF capacitor are used in the test circuit. Human capacitance is typically 50pF to 250pF, with the majority of people at 100pF or less, and human resistance ranges from 1000Ω to 5000Ω. An ESD failure is defined as a voltage level which causes sufficient damage to the device such that it no longer meets the electrical data sheet limits.

After initial ESDS testing, it is important that ESDS test monitoring be performed periodically on devices from various lots to determine lot-to-lot variation. The VZAP-2 report titled "Electrostatic Discharge (ESD) Susceptibility of Electronic Devices" published by the Reliability Analysis Center, Rome Air Development Center, contains a wealth of information on ESDS testing data on devices of different process technologies from many manufacturers. The data in this report clearly indicates a large lot-to-lot variation relating to ESD susceptibility on the same device.

Design for ESD Protection

ESD protection designs employed on Linear Technology Corporation devices include:

1. Input clamp diodes
2. Input series resistors to limit ESD current in conjunction with clamp diodes
3. New ESD Structures
4. Eliminating metallization runs over thin oxide regions when they are tied directly to external pins

ESD Task Force

An ESD task force should consist of members from each affected department to do the foundation work, sell the program to management, and implement the program with the following objectives:

1. Develop, approve and implement an ESD control specification covering all aspects of design, ESD protected materials and equipment, and manufacturing
2. Raise the level of ESD awareness
3. Develop a training and certification program
4. Work with all departments on any ESD questions or problems
5. Develop a program to educate and assist sales offices, distributors and customers to minimize ESD
6. Review and qualify new ESD protective materials and equipment, and keep specifications and training program upgraded
7. Measure the cost-to-benefit ratio of the program

Facilities Evaluation

The ESD task force should be responsible for facility evaluation. This evaluation should be guided by the ESD coordinator. The ESD coordinator should be chosen for strong knowledge of ESD controls, and for the ability to effectively interface with all affected departments. The primary objective of the task force is to pinpoint areas that represent sources of static electricity and potential yield losses due to ESD.

A representative, preferably the engineering or production manager, from each of the key manufacturing areas should be represented on this task force. At Linear Technology Corporation this effort is headed by the Quality Assurance Manager and the Package Engineering Manager. The balance of the ESD task force members are the Test Engineering, Product Engineering, and Production Managers.

The only equipment needed for this survey is a field static meter which measures static up to a level of 50kV. Both nuclear and electronic type static meters are available from manufacturers like 3M, Simco, Wescorp, Scientific Enterprises, Voyager Technologies and ACL.

Regardless of area classification, all manufacturing areas can be broken down into the following categories for evaluation purposes.

1. Personnel

Personnel represents one of the largest sources of static, from the type of clothing, smocks and shoes that they wear (for example, polyester or nylon smocks).

2. The Environment

The environment includes the room humidity and floors. Relative humidity plays a major part in determining the level of static generated. For example, at 10-20% RH a person walking across a carpeted floor can develop 35kV versus 1.5kV when the relative humidity is increased to 70%-80%. Therefore the humidity level must be controlled and should not be allowed to fluctuate over a broad range.

Floors also represent one of the greatest contributors of static generation on personnel, moving carts or equipment because of movement across its surface. Carpeted and waxed vinyl floors are prime static generators.

3. Work Surfaces

Painted or vinyl covered table tops, vinyl covered chairs, conveyor belts, racks, carts and shelving are also static generators.

4. Equipment

Anodized surfaces, plexiglass covers, ungrounded solder guns, plastic solder suckers, heat guns and blowers are also static generators.

5. Materials

Look out for common plastic work holders, foam, common plastic tote boxes and packaging containers.

Examples of typical static levels are shown in the table below.

	RELATIVE HUMIDITY	
	10%-20%	70%-80%
Walking across a carpeted floor	35kV	1.5kV
Walking across a vinyl floor	12kV	0.3kV
Picking up a common plastic bag	15kV	0.5kV
Sliding plastic box over bench/conveyor	15kV	2.0kV
Ungrounded solder sucker	8kV	1.0kV
Plastic cabinets	8kV	1.0kV

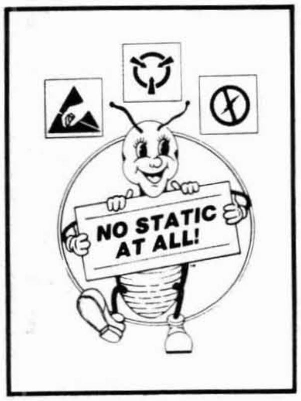
This ESD survey should include all direct and support manufacturing areas where semiconductor and other electronic components are handled, and should be extended to cover distribution and field sales offices, and field service centers. Once the facility evaluation is completed, the results are reviewed by the ESD task force, and controls are selected to combat each potential ESD problem area.

The ESD Protection Program

The degree of static control should be determined by the most static sensitive device or assembly in the operation. Top management support and implementing the same basic controls in all areas with no double standards will help to ensure success.

The basic concept of complete static protection is the prevention of static buildup, the removal of any already existing charges, and the protection of electronic components from induced fields. The first and foremost line of defense is the personnel wrist strap together with grounded conductive or static dissipative table tops, and conductive heel straps and grounded conductive or static dissipative floor mats.

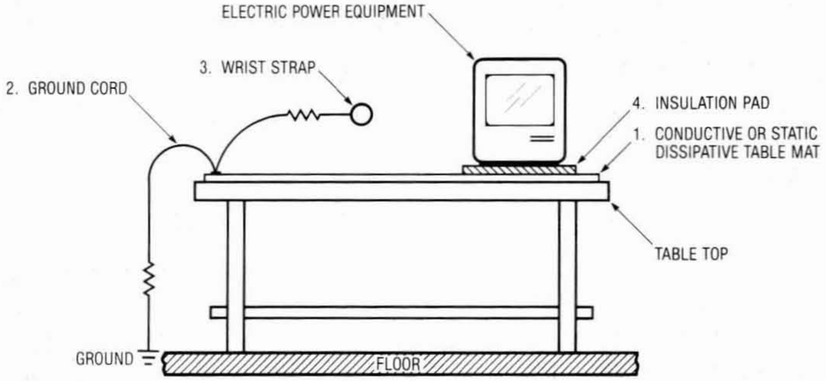
To increase ESD awareness at Linear Technology Corporation, all ESD Protection Areas are marked by an identifying label (for example, label shown below). This label alerts all personnel that ESD protection procedures are enforced in the area.



ESD Protected Workstation

Examples of ESD Protected Workstations are shown in Figures 1 and 2.

Option 1 (Figure 1): All electronic components, sub-assemblies and assemblies must be handled at an ESD Protected Workstation only. The figure illustrates an ESD Protected Workstation consisting of a static dissipative table mat grounded to earth or electrical ground through a 1MΩ series resistor, with the requirement that the operator wears a grounded insulated conductive wrist strap with a 1MΩ series resistor. This 1MΩ series resistor protects the operator from electrical shock, should the operator come in contact with a potentially lethal voltage. Option 1 should be used where the operator does not require a large degree of freedom, e.g., during product inspection, component soldering, board repair, etc.


ELECTRIC POWER EQUIPMENT
3. WRIST STRAP
2. GROUND CORD
4. INSULATION PAD
1. CONDUCTIVE OR STATIC DISSIPATIVE TABLE MAT
TABLE TOP
GROUND
FLOOR

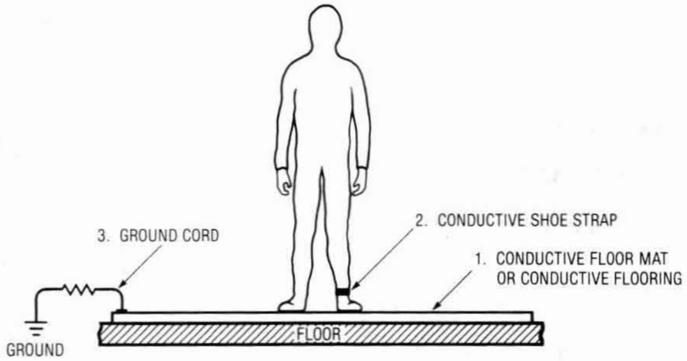
MATERIALS: 1. 1/16″ THICK CONDUCTIVE OR STATIC DISSIPATIVE TABLE MAT WITH SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.

2. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, 1MΩ ± 10%, AND 18AWG OR LARGER INSULATED WIRE.

3. INSULATED CONDUCTIVE WRIST STRAP WITH 1/4W MINIMUM, 1MΩ ± 10%, AND 20AWG OR LARGER INSULATED WIRE. THE CURRENT LIMITING 1MΩ RESISTOR MUST BE LOCATED RIGHT NEXT TO THE WRIST TO PREVENT THE POSSIBILITY OF SHUNTING THE RESISTOR.

4. POWER TEST EQUIPMENT MUST BE CHASSIS GROUNDED VIA A THREE-PRONG PLUG, AND PLACED ON AN INSULATION PAD MADE OF FORMICA, FIBERGLASS OR EQUIVALENT MATERIAL.

Figure 1


2. CONDUCTIVE SHOE STRAP
3. GROUND CORD
1. CONDUCTIVE FLOOR MAT OR CONDUCTIVE FLOORING
GROUND
FLOOR

MATERIALS: 1. OPTIONAL 1/8″ THICK CONDUCTIVE OR STATIC DISSIPATIVE MAT OR CONDUCTIVE FLOORING (e.g., CONDUCTIVE FLOOR TILES) WITH A SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.

2. CONDUCTIVE SHOE STRAP WITH A SURFACE RESISTIVITY OF $< 10^5\Omega$ PER SQUARE.

3. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, 1MΩ ± 10%, AND 18AWG OR LARGER INSULATED WIRE.

Figure 2

Option 2 (Figure 2): Shows an alternate installation method for an ESD Protected Workstation. It consists of a conductive or static dissipative floor mat grounded to earth or electrical ground through a 1MΩ series resistor with the operator wearing a conductive shoe strap. This installation is typically used where the operator needs freedom of movement over a large area, e.g., environmental chamber loading and unloading, electrical testing, etc. To be effective the conductive shoe strap must be attached to the wearer's shoe to maximize contact between the strap and the conductive floor.

Option 3: Utilizes the same conductive or static dissipative floor mat installation as Option 2 with the exception that the operator is grounded via a wrist strap through the equipment ground instead of a conductive shoe strap. It is utilized where an operator is working with a piece of freestanding equipment and does not require a great deal of freedom of movement.

Handling

At Linear Technology Corporation all products are handled, transported and staged in volume conductive tote boxes. This offers maximum protection to the components from triboelectrically generated and inductive static charges. The rule is under no circumstances should components be removed from their approved containers except at an ESD protected workstation.

Final Packaging

Only antistatic and conductive final packaging containers (for example, antistatic or conductive dip tubes, volume conductive carbon loaded plastic bags or metallic film laminate bags, foil lined boxes) are used. Filler (dunnage) material used should be antistatic, non-corrosive, and should not crumble, flake, powder, shred or be of fibrous construction. Conductive packing materials are preferred since they not only prevent buildup of triboelectric charge, but also provide shielding from external fields.

Other ESD Preventative Measures

- Where possible, ban all static bearing materials, e.g., common plastics, styrofoam from the work environment.
- Use only synthetic material smocks with 1% to 2% interwoven steel.
- Ensure all electronic and electro-mechanical equipment is chassis grounded, including conveyor belts, vapor degreasers and baskets, solder pots, etc.
- Tips of hand soldering irons are to be grounded.
- All parts of hand tools (e.g., solder suckers, pliers, etc.) which can be expected to come in contact with electronic components are to be made of conductive material and grounded.
- Conductive shorting bars are to be installed on all terminations for PC boards with electronic components during assembly, loading, inspecting, repairing, soldering, storing and transporting.
- All PC boards with electronic components are not to be handled by their circuitry, connector points or connector pins.
- High velocity air movement is to be delivered through a static neutralizer.
- Air ionizers are to be employed in neutralizing static buildup on insulators if they have to be used or as an extra precautionary measure for extremely sensitive assemblies.
- Do not slide electronic components over a surface.

Air ionizers come in three basic types: nuclear, AC and pulsed DC. These ionizers can neutralize static charges on non-conductive materials by supplying the materials with a stream of both positive and negative ions.

The advantage of the AC or pulsed DC type air ionizer is that there is no recurring annual replacement cost. The disadvantages are: it emits ozone which can damage rubber in equipment; EMI (Electro Magnetic Interference); and an imbalance in the stream of ions if not properly maintained, therefore necessitating frequent preventive maintenance.

The advantages of the nuclear type air ionizer are low maintenance, no ozone, no EMI and no imbalance problems. The disadvantages are that it requires careful handling because of the radioactive source, and the annual recurring cost to replace the radioactive source.

The selection of air ionizers must be done with care with awareness of the above limitations. The squirrel cage ionized air blower has been proven to produce a significantly more even distribution of ion patterns than does a conventional fan blower design.

Maintenance

ESD protective floor and table coverings must be properly maintained. Do not wax over them. Cleaners must not degrade their electrical properties. Vacuum to remove loose particles, followed by a wet mop with a solution of mild detergent and hot water.

Periodic Audits

At Linear Technology Corporation periodic audits are conducted to check on the following at least once a month, unless otherwise noted.

- Compliance with ESD control procedures.
- Ensure that the conductive ground cord connection is intact by measuring the series resistance to ground with an ohmmeter.
- Ensure that wrist straps are still functional by measuring the resistance from the person to ground. The ground lead of the ohmmeter is connected to the ground connection of the wrist strap, and the positive lead is connected to a stainless steel electrode (one inch in diameter, and three inches long #304 stainless steel) which is held by the person. This test method not only checks the resistance of the series resistor, but also resistance through the ground cord and also any contact resistance between the wrist strap and the person's skin. This test procedure is required when wrist straps with an elastic nylon band with interwoven metallic strands are used, since the metallic strands breakdown with prolonged use. This monitor frequency may be shortened depending on audit results.
- Measure the surface resistivity of conductive or static dissipative table tops once every 6 months using ASTM-F-150-72, ASTM-D-257 or ASTM-D-991 test methods as appropriate.

Materials Selection and Specification

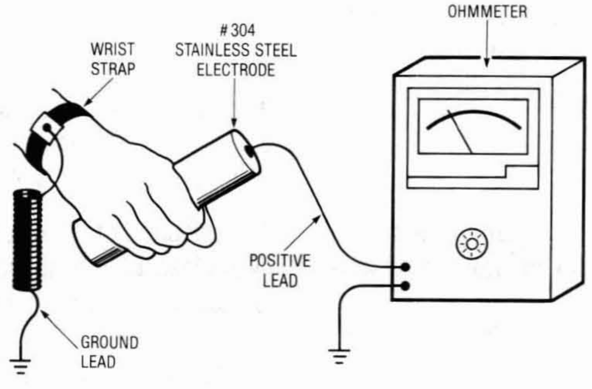
Based on the tremendous amount of ESD protective materials available, it is important that materials are selected based on a stringent qualification. Once the materials have been selected and specifications defined, a material procurement specification needs to be initiated that defines the materials and quality requirements to the vendor. One of the major pitfalls is to procure material in haste, e.g., a wrist strap, only to find out it does not perform reliably.

The SOAR-1 report titled "ESD Protective Material and Equipment: A Critical Review" published by the Rome Air Development Center is an excellent reference on the various types of ESD protective materials available.

At Linear Technology Corporation a minimum of three manufacturing lots from a potential vendor are subjected to qualification testing per the requirements of the material procurement specification for ESD protective materials. The vendor is considered qualified only when all three lots are found to be acceptable. Once vendors have been qualified, all incoming ESD protective materials are subjected to a stringent incoming inspection.

The following table summarizes a sample material and test specification for ESD protective materials.

Wrist Strap Resistance Test Set-Up



MATERIAL	PROPERTIES/DESCRIPTION	TEST METHODS
Wrist Strap	• Insulated coil cord with a 1MΩ ± 10%, ¼W minimum series resistor molded into snap fastener (at wrist end), and an elastic wrist band with inner metallic filaments and insulative exterior.	Measure series resistance with ohmmeter. Apply normal tug to both ends of strap and remeasure series resistance. Resistance must be between 0.8 to 1.2MΩ.
Conductive or Static Dissipative Table and Floor Coverings, Conductive Tote Boxes, Conductive Shoe Straps	• Must not shed particles • Must not support bacterial or fungal growth • Conductive: surface resistivity $<10^5$ Ω/square. Static Dissipative: surface resistivity $>10^5$ and $<10^9$ Ω/square.	Test per ASTM-F-150-72, ASTM-D-257, ASTM-D-991 (for surface resistivity $<10^6$ Ω/square).
Conductive Foam	• Shall not contain more than 30ppm Cl, K, Na when a quantitative chemical analysis is performed • Must not support bacterial or fungal growth	With devices inserted into the foam, the foam must not cause lead corrosion after a 24 hour 85°C/85% RH temperature/humidity storage.
Antistatic and Conductive Dip Tubes	• Must not exhibit an oily-like film	Must meet an Electrostatic Decay test per Federal Test Method Standard 101 Test Method 4046. Material charged to 5000V must be discharged to 1% of its initial value (50V) in 2 seconds after a 24 hour conditioning at 15% relative humidity.
Antistatic and Conductive Bags	• Antistatic bags must meet MIL-B-81705 type 2 • Conductive bags must meet MIL-B-117 and sealing requirements of MIL-B-81705 • Must not support bacterial or fungal growth	Test method for antistatic bags same as for antistatic/conductive dip tubes. Test method for conductive bags same as for conductive table/floor coverings.
Static Eliminators/Ionized Air Blowers	• Ozone level: 0.1ppm maximum for 8 hour exposure • Noise: 60dB maximum • EMI: non-detectable when measured 6 inches away	Voltage Decay test: A non-conductive sheet of material charged to 5kV must be discharged to 1% of its initial value (50V) in 2 seconds at a distance of 2 feet from the ionizer or larger distance if application calls for a larger distance.

Training and Certification Program

The training program should be developed to increase ESD awareness and to assist all personnel in complying with the ESD control specification. The program should include:

1. A discussion on "What is Static Electricity?"
2. How ESD affects ICs
3. Estimated cost of ESD related losses
4. Materials and equipment for controlling static
5. The importance of wearing the wrist strap
6. The importance of an audit program
7. Encourage floor personnel to feedback any ESD potential areas to the ESD task force

ESD training should be incorporated into the personnel training and certification program. At Linear Technology Corporation only fully trained and certified personnel are allowed to do actual production work. To help increase ESD awareness, it is often a good idea to show ESD awareness films and video tapes which are available from a variety of sources (Reference 3 provides a list of films and video tapes). Personnel are retrained and recertified at a minimum frequency of once per year.

Measuring the Benefits

Where possible, the benefits of an ESD Protection Program should be tracked and quantified. The two yardsticks used at Linear Technology Corporation are final test yields and QA electrical average outgoing quality (AOQ). Since the implementation of this program, there has been a significant improvement in final test yields especially on static sensitive CMOS devices. With the elimination of ESD as a potential failure cause, the electrical AOQ has averaged well under 100ppm for all products combined. Improvements such as this help to provide positive feedback to manufacturing and support personnel on the importance of an ESD Protection Program, and also help to ensure its continuing success.

References

1. DOD-STD-1686	Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment.
2. DOD-HDBK-263	Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment.
3. SOAR-1	State-of-the-Art Report ESD Protective Materials and Equipment: A Critical Review, published by the Rome Air Development Center.
4. VZAP-2	Electrostatic Discharge (ESD) Susceptibility Data published by the Rome Air Development Center.
5. EOS-1, EOS-2, etc.	Electrical Overstress/Electrostatic Discharge Symposium Proceedings 1979 to current year.
6. MIL-STD-883	Test Methods and Procedures For Microelectronics
7. MIL-M-38510	Microcircuits, General Specification for
8. MIL-M-55565	Microcircuits, Packaging of
9. MIL-M-81705	Barrier Materials, Flexible, Electrostatic—Free, Heat Sealable
10. FED-STD-101	Preservation, Packaging and Packing Materials Test Procedures; Test Methods. 4046: Electrostatic Properties of

Linear Technology has an active Statistical Process Control (SPC) System. It operates via the interrelated mechanisms of: a structure, control charts with built-in contingency action plans, operational area documentation (flowcharts and control plan details), an SPC training program, each of which is defined in the Company's officially controlled SPC specification.

STRUCTURE

At the core of the SPC system are the Process (or Preventive) Action Teams (PATs). These cross-functional teams are comprised of individuals directly involved with a process element or problem. In a production operation, they typically involve production operators, lead operators, maintenance, engineering, and/or supervision. In a non-production operation, the PATs are comprised of operating employees and representatives of related functions.

Each operating group (e.g., Wafer Fab) has a formal SPC presence in the form of a SPC Quality Control Team (QCT). These SPC QCTs are comprised mostly of the manager and staff of that particular operating unit bearing the responsibility to implement and maintain SPC within their respective areas.

This QCT structure is the leadership of that operating unit, and as such, sanctions the various PATs within its jurisdiction as they implement and maintain SPC and/or solve specific problems in their respective areas. In addition, the QCT conducts monthly reviews of SPC charts, action items, and new programs.

The QCTs, in turn, report to the SPC Steering Committee. This body consists of the President, Chief Operating Officer, Vice President of Operations, Vice President of Quality & Reliability, and the SPC Manager. Thus, it has the corporate leadership responsibility for SPC at Linear Technology.

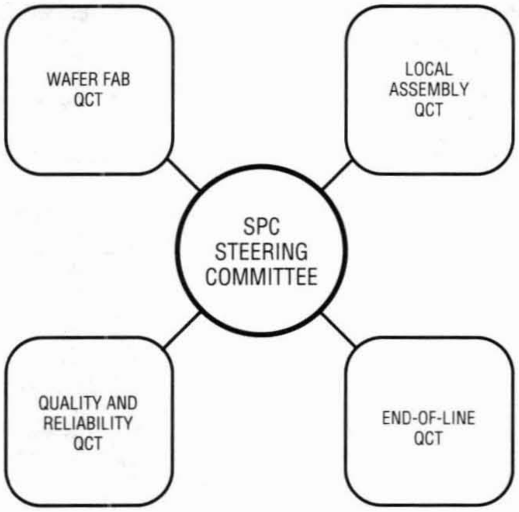


Figure 1. Linear Technology Corporation SPC Quality Control Teams

CONTROL CHARTS

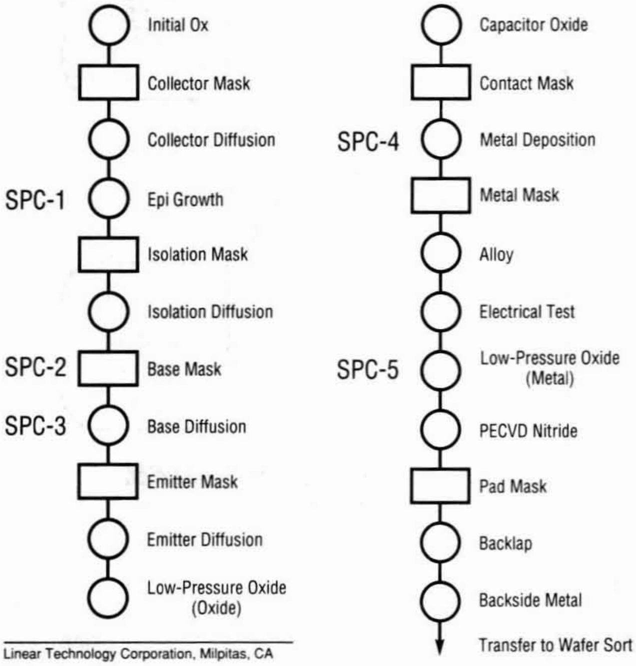
The control charts at Linear Technology are manually charted by the operators to insure they are the custodians of the process, its trends, and defined corrective measures (as opposed to computerized SPC charting).

The contingency action plan, known as the Out-of-Control Action Plan (OCAP), defines the specific corrective actions when the process experiences out-of-control situations. No control chart is put in place without an OCAP. This strategy has in effect empowered the work force, while freeing the Engineering staff for systematic and continuous improvement.

FLOW CHARTS AND CONTROL PLAN DETAILS

The flow charts serve to graphically display the flow of products in each operational area, as well as define and communicate the critical nodes of that operation. The details of each critical node are defined in the Control Plan Detail, which serves as a planning, reporting, and communication tool.

An example of a flow chart and the related Control Plan Detail for one operational area (e.g., The Wafer Fabrication Area) Figure 2, and Table 1 follows:


Initial Ox
Collector Mask
Collector Diffusion
SPC-1
Epi Growth
Isolation Mask
Isolation Diffusion
SPC-2
Base Mask
SPC-3
Base Diffusion
Emitter Mask
Emitter Diffusion
Low-Pressure Oxide (Oxide)
Capacitor Oxide
Contact Mask
SPC-4
Metal Deposition
Metal Mask
Alloy
Electrical Test
SPC-5
Low-Pressure Oxide (Metal)
PECVD Nitride
Pad Mask
Backlap
Backside Metal
Transfer to Wafer Sort

Linear Technology Corporation, Milpitas, CA

Figure 2. General Bipolar Wafer Fabrication Flow Chart

TRAINING PROGRAM

In order to pursue and continue the smooth operation of the SPC System within LTC, an all-encompassing instructional program for employees was initiated according to the following plan.

Each employee designated for SPC training is classified into one of three groups, and attends the specific classroom instruction for that classification. The courses and length of training (hours) for each group are designated in Table 2.

The content of the Training Courses is as follows:

BASIC SPC: Philosophy of SPC, concepts of variation, control, capability; tools and techniques for control and capability, including histograms, capability studies, control charting; basic problem solving, including normality, brainstorming, cause and effect diagramming, Pareto analysis, capability index/ratio.

ADVANCED SPC: Review of basic concepts, fundamentals of Measurement System Evaluation (Gage R&R), process capability studies, determination and use of control charts, i.e., Xbar & R, Median & R, X & Moving R, p, np, u, and c chart techniques. Chart interpretation and the basics of attributes sampling system.

Table 1. Linear Technology Corporation Process Control Plan Detail for Bipolar Wafer Fab

SPC Node and Process	Critical Features	Measurement Method	Sample Size	Sample Frequency	SPC Control System	MSE (Gage R and R)	Process Capability	
							Cp	Cpk
(SPC-1) Epi Growth	Resistivity	4-Point Probe	2	Batch	X and Moving R Chart	Acceptable	1.59-1.89	1.15-1.37
	Deposition Rate (Thickness)	Nicolet	2	Batch	Run Chart	Acceptable		2.54-4.17
(SPC-2) Base Mask	CDs	OSI-VLS1	1 Site/ 5 Wafers	Batch	Xbar and R Chart	Acceptable	1.43	1.22
(SPC-3) Base Deposition	Sheet Resistance	4-Point Probe	3 Sites/ 3 Wafers	Batch	Xbar and R Chart	Acceptable	1.34-1.96	1.29-1.68
(SPC-4) Metal Deposition	Thickness By Resistivity	4-Point Probe	2	Batch	Xbar and R Chart	New Gauge is Now Acceptable	2.23-2.38	2.2-2.3
(SPC-5) LPOM	Thickness	Nanospec	5 Sites/ 3 Wafers	Batch	Xbar and R Chart	Acceptable	0.95	0.74

Table 2.

Group #	Trainee Audience	Basic SPC	Advanced SPC	D.O.E.	TEAM ORG.	TOTAL
1	Engineering (Technical)	15	20	40	4	79
2	Management/Supervision Technicians	15	20	—	4	39
3	Operators	15	—	—	—	15

DESIGN OF EXPERIMENTS: Philosophy and need of experimental design, experimental methodologies utilizing Fisher & Taguchi concepts. Response Surface Methodology for parameters and tolerance designs, including ANOVA, and analysis of co-variance.

TEAM ORGANIZATION: An outline of the SPC organization within Linear Technology, the concepts of the SPC Quality Control Teams (SPC QCTs) and Preventive/Process Action Teams (PATs). Strategies for Detailed Control Plans and Out-of-Control Action Plans (OCAPs). Concepts of team effectiveness.

Manufacturing Excellence

One of the Linear Technology goals is *manufacturing excellence*. The traditional SPC techniques seek to produce processes that are capable and in control. To improve those processes and to determine rational parameters and specification tolerance of new products and processes requires the *Design of Experiments* (DOEs) methodology.

Linear Technology actively pursues the screening techniques described by Fisher as well as the optimization techniques of Box and Taguchi. These latter techniques, known as *Response Surface Methodology* and *Taguchi Methods*, are particularly useful in developing robust products and processes, with a minimum of sensitivity to process variation.

Contribution to Quality

Contribution to quality improvement has evolved from one dominated by ATTRIBUTE INSPECTION (pass/fail) to one involving a mixture of SPC and attribute inspection. As we progress further, the contribution of Design of Experiments will become significant. Products and processes developed using the DOE tools will have the *quality built-in*. The consequence of this built-in quality is predictable performance at the lowest possible cost.

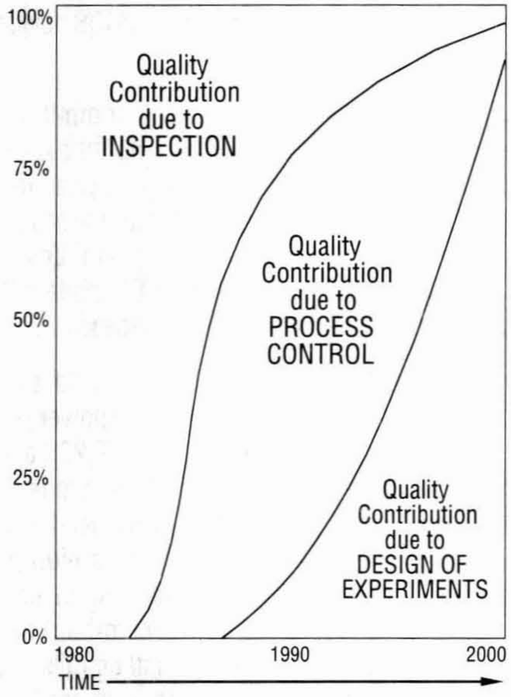


Figure 3. The Semiconductor Quality Evolution

The concepts of SPC and DOE have already been institutionalized within Linear Technology and will provide the methodology to ensure a process of continuing improvement.

SURFACE MOUNT PRODUCTS

Introduction

Linear Technology Corporation was founded in 1981 to address the growing demand for high performance and superior quality linear integrated circuits.

Today, Linear Technology has successfully established a leadership position by introducing and supplying leading edge products in each of the industry's basic functional groups — op amps, comparators, voltage regulators, references, switched-capacitor filters, interface, data conversion, and a variety of special function CMOS devices, in all major package styles.

Early on, Linear Technology made the commitment to provide advanced technology, *surface mount packaging*. This made Linear Technology the first company to offer true precision and high performance linear devices across the full range of functional categories, plus many of the popular second-source devices in JEDEC Standard SO-8, 14, 16 and SOL-16, 18 and 20 pin packages.

The continuing demand for more complete surface mount designs has spurred the introduction of two power surface mount packages by LTC — the 3 lead SOT-223 and the DD package available in 3, 5, and 7 lead versions. Many LTC power products are now being introduced in these packages which, for the first time, enables high power designs to be realized using 100% surface mount devices. Support for Linear Technology's surface mount devices includes service for tape and reel, antistatic rails, quality and reliability data, and data sheets on each product.

Linear Technology intends to address customer demand for surface mount devices where technology and die sizes permit, making the combination of small package size and high performance linear devices readily available to our users.

This section contains information summarizing Linear Technology's capabilities and services for surface mount packaged products, as well as specific device data sheets.

Package Descriptions

Linear Technology's SO packages conform to Standard JEDEC SOIC outlines.

In some instances, an LTC product available in an 8-pin standard DIP package is offered in a 16-pin SOL package. This covers the situation where the die is too large to be accommodated by the smaller SO-8 package. Although it is preferable for an SO-8 device to have the same pinout as the standard 8-pin dual-in-line version, some devices necessitate a rotation of the die to fit in the SO-8 package. Please refer to the applicable SO device data sheet, or consult with the factory to verify exact pinouts for each device.

Electrical Specifications

Wherever possible, electrical specifications for a surface mount technology (SMT) device are the same as the plastic molded equivalent. Exceptions to this are identified by the omission of the standard product electrical grade designator from the part number.

For example:

- LT1013DS8 has the same electrical specifications as LT1013DN8, since the "D" is common to both product numbers.
- LT1012S8 has one or more different electrical specifications than LT1012CN8, as the "C" is missing from this product designator suffix.

Please consult the appropriate SMT package data sheet for complete electrical specifications.

Marking

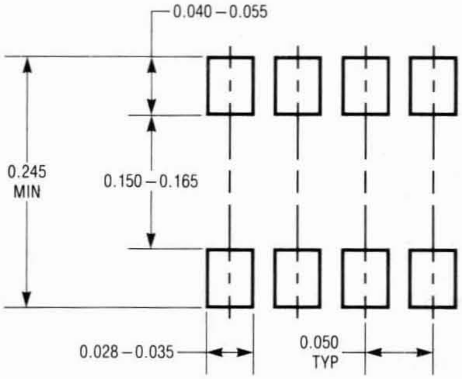
Because of the limited space available for part marking on some SMT packages, abbreviated marking codes are used to identify the device. These codes, if used, are identified in the individual SMT package data sheets.

Lead Finish and Solderability

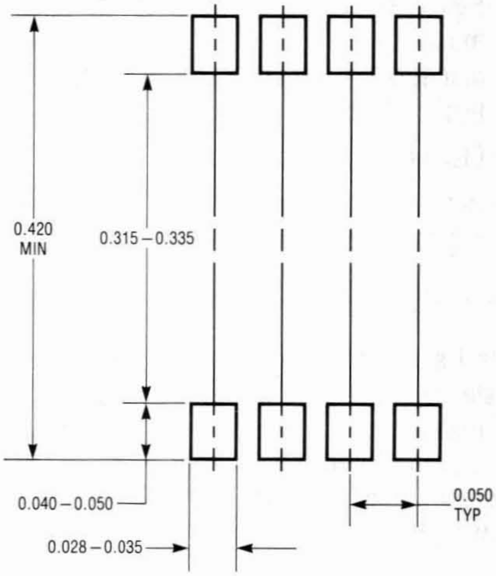
Lead finish is electroplated, lead-tin, with a low carbon content. Solderability meets the requirements of MIL-STD-883C, Method 2003. Recommended solder pads are given in Figure 1.

Recommended Solder Pads

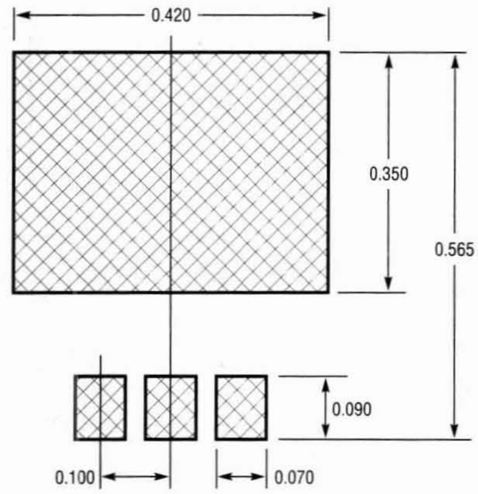
SO-8, SO-14, SO-16


0.040 – 0.055
0.245
MIN
0.150 – 0.165
0.028 – 0.035
0.050
TYP

SOL-16, SOL-18, SOL-20, SOL-24, SOL-28


0.420
MIN
0.315 – 0.335
0.040 – 0.050
0.050
TYP
0.028 – 0.035

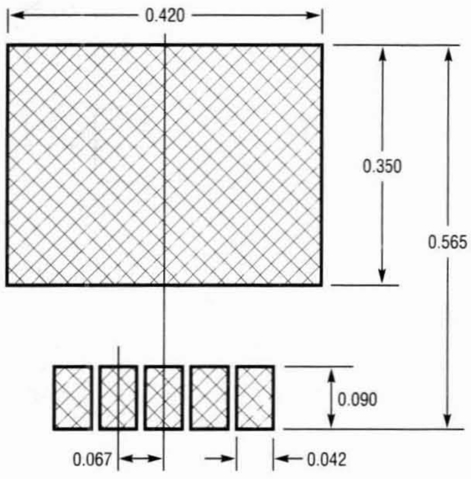
3-Lead DD


0.420
0.350
0.565
0.090
0.100
0.070

NOTE: ALL DIMENSIONS ARE IN INCHES

SMP • 04

5-Lead DD

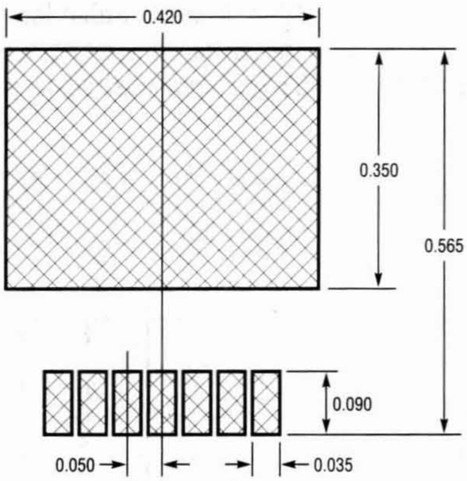

0.420
0.350
0.565
0.090
0.067
0.042

NOTE: ALL DIMENSIONS ARE IN INCHES

SMP • 05

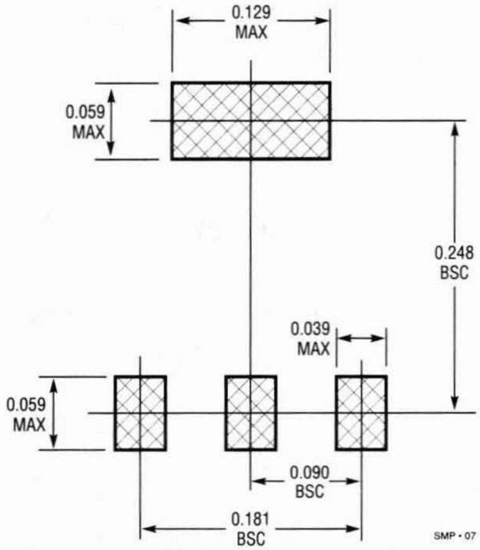
Figure 1. Recommended Solder Pads

7-Lead DD



NOTE: ALL DIMENSIONS ARE IN INCHES

3-Lead SOT-223



NOTE: ALL DIMENSIONS ARE IN INCHES

Figure 1. Recommended Solder Pads (Continued)

Wave and Reflow Soldering

Following are the recommended procedures for soldering surface mount packages to PC boards.

1. Wave Soldering

- Use solder plating boards.
- Dispense adhesive to hold components on board.
- Place components on board.
- Cure adhesive per adhesive manufacturer's specification.
- Foam flux using RMA (Rosin Mildly Activating) flux.
- Wave solder using a dual wave soldering system at 240°C to 260°C for 2 seconds per wave.
- Clean board.

2. Reflow Soldering

- Use solder plating boards.
- Screen solder paste on board.
- Mount components on board.
- Bake for 15-20 minutes at 65°C to 90°C.
- Preheat to within 65°C of the solder temperature.
- Reflow solder paste. The solder paste temperature must be 200°C for at least 30 seconds. LTC recommends vapor phase or infrared reflow systems for best performance.
- Clean boards.
- Hand soldering of DD and SOT-223 packages is not recommended.

Thermal Information

Table 1 shows the range of junction-to-ambient thermal resistance of SO and SOL devices mounted on a PCB of FR4 material with copper traces, in still air at 25°C. θ_{JA} with a ceramic substrate is about 70% of the FR4 value. Maximum power dissipation may be calculated by the following formula:

$$P_{D\,MAX}[TA] = \frac{T_{j\,MAX} - T_A}{\theta_{JA}}$$

where $T_{j\,MAX}$ = Maximum operating junction temperature.

T_A = Desired ambient operating temperature.

θ_{JA} = Junction-to-ambient thermal resistance.

Table 1. Typical Thermal Resistance Values

SO-8	150° to 200°C/W	SOL-18	70° to 100°C/W
SO-14	100° to 140°C/W	SOL-20	70° to 90°C/W
SO-16	90° to 130°C/W	SOL-24	60° to 80°C/W
SOL-16	85° to 100°C/W	SOL-28	55° to 75°C/W

Conditions: PCB mount on FR4 material, still air at 25°C, copper trace.

Thermal resistance for power packages (DD and SOT-223) depends greatly on the individual device type. Please consult the device data sheets for thermal information.

More current data, by device type, may be obtained by contacting Linear Technology Corporation, Marketing Department.

Tape and Reel Packing

Tape and reel packing is available for all SO, SOL, SOT-223 and DD packages in accordance with EIA Specification 481-A. Table 2 lists the applicable tape widths, dimensions, and quantities for all LTC small-outline products. Consult factory for tape and reel pricing and minimum order requirements.

Table 2. Tape and Reel Packing Specifications

PACKAGE	TAPE SIZE	P COMPONENT PITCH	Po HOLE PITCH	REEL DIAMETER	PARTS PER REEL
SO-8	12mm	8mm	4mm	13"	2500
SO-14	16mm	8mm	4mm	13"	2500
SO-16	16mm	8mm	4mm	13"	2500
SOL-16	16mm	12mm	4mm	13"	1000
SOL-18	24mm	12mm	4mm	13"	1000
SOL-20	24mm	12mm	4mm	13"	1000
DD	24mm	16mm	4mm	13"	750
SOT-223	16mm	12mm	4mm	13"	2000

Plastic Tube Packing

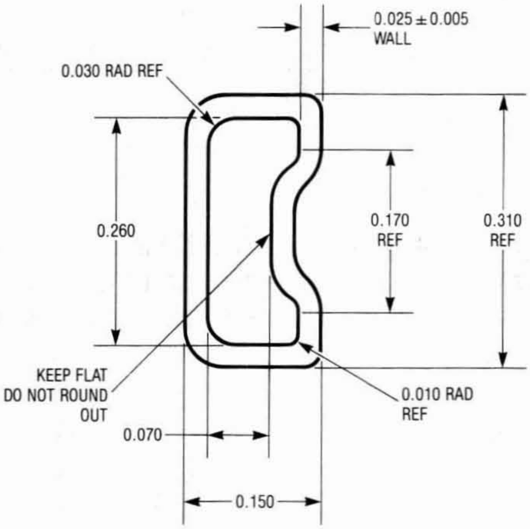
Linear Technology SO, SOL, SOT-223 and DD packaged devices are packed in "antistatic" plastic tubes with the dimensions indicated in Figure 2. Unit quantities per tube are as listed in Table 3.

Table 3. Devices Per Tube

SO-8	100 ea.	SOL-16	47 ea.
SO-14	55 ea.	SOL-18	40 ea.
SO-16	50 ea.	SOL-20	38 ea.
DD	50 ea.	SOL-24	32 ea.
SOT-223	78 ea.	SOL-28	27 ea.

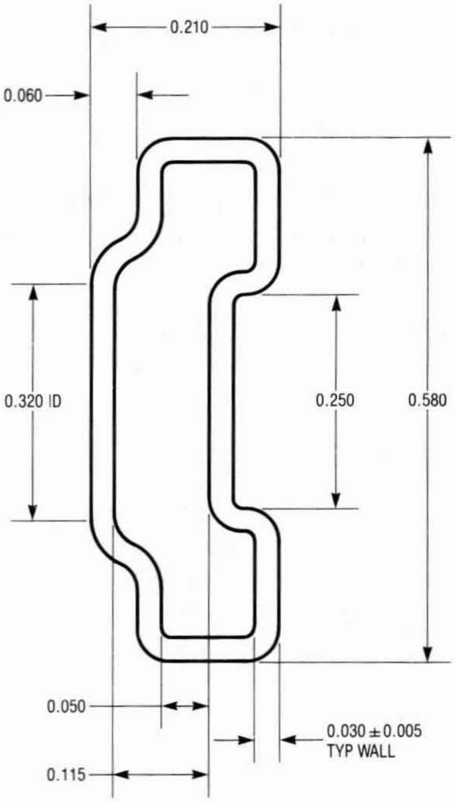
PLASTIC TUBE SPECIFICATIONS

SO Package Shipping Tube


0.025 ± 0.005
WALL
0.030 RAD REF
0.260
0.170
REF
0.310
REF
KEEP FLAT
DO NOT ROUND
OUT
0.010 RAD
REF
0.070
0.150

Length: 20.50 $^{+1/16}_{-1/32}$ inches

SOL Package Shipping Tube


0.210
0.060
0.320 ID
0.250
0.580
0.050
0.030 ± 0.005
TYP WALL
0.115

Length: 20.75 $^{+1/32}_{-1/16}$ inches

Figure 2

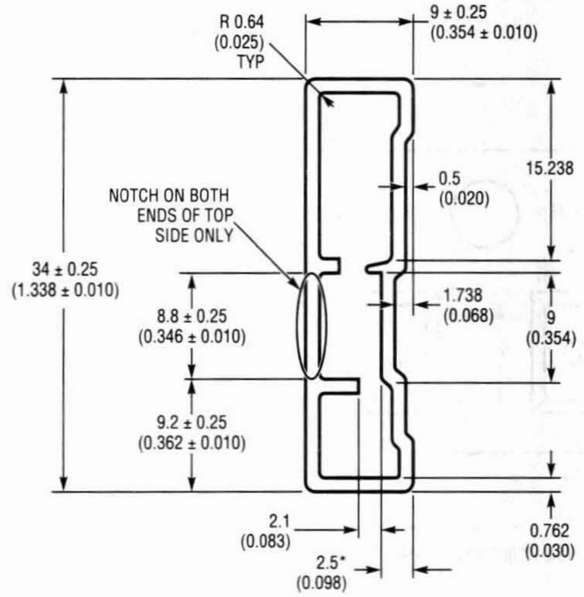
Note 1: Tolerances: ± 0.010 unless otherwise specified.

Note 2: Material: anti-static treated rigid transparent PVC or rigid black conductive.

Note 3: Printing: "LTC logo, Linear Technology Corp., Antistatic" on top side of tube.

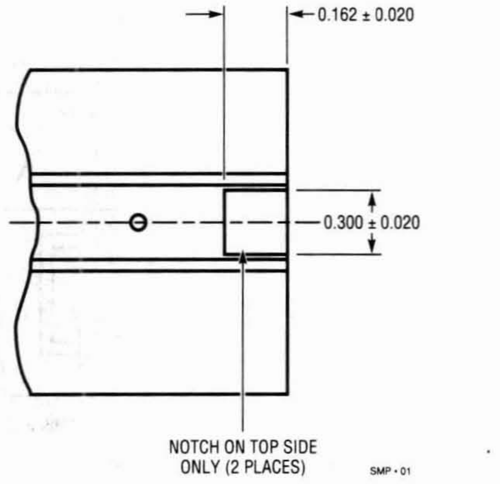
PLASTIC TUBE SPECIFICATIONS

DD Package Shipping Tube


R 0.64
(0.025)
TYP
9 ± 0.25
(0.354 ± 0.010)
15.238
0.5
(0.020)
NOTCH ON BOTH
ENDS OF TOP
SIDE ONLY
34 ± 0.25
(1.338 ± 0.010)
8.8 ± 0.25
(0.346 ± 0.010)
1.738
(0.068)
9
(0.354)
9.2 ± 0.25
(0.362 ± 0.010)
2.1
(0.083)
2.5*
(0.098)
0.762
(0.030)

NOTES:
TUBE LENGTH = 21.65 ± 0.045 INCHES
*CRITICAL DIMENSION

SMP • 09


0.162 ± 0.020
0.300 ± 0.020
NOTCH ON TOP SIDE
ONLY (2 PLACES)
SMP • 01

SOT-223 Package Shipping Tube

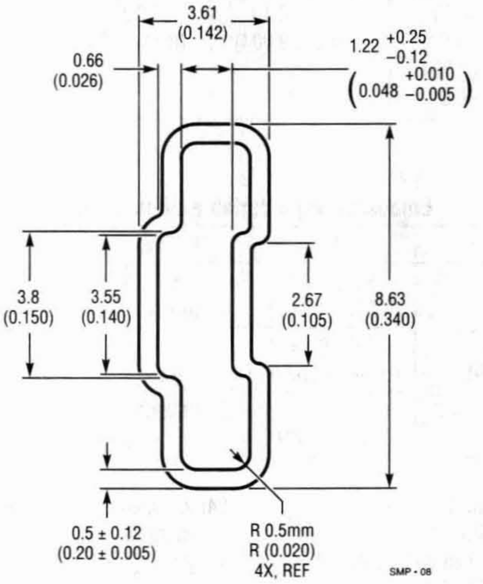
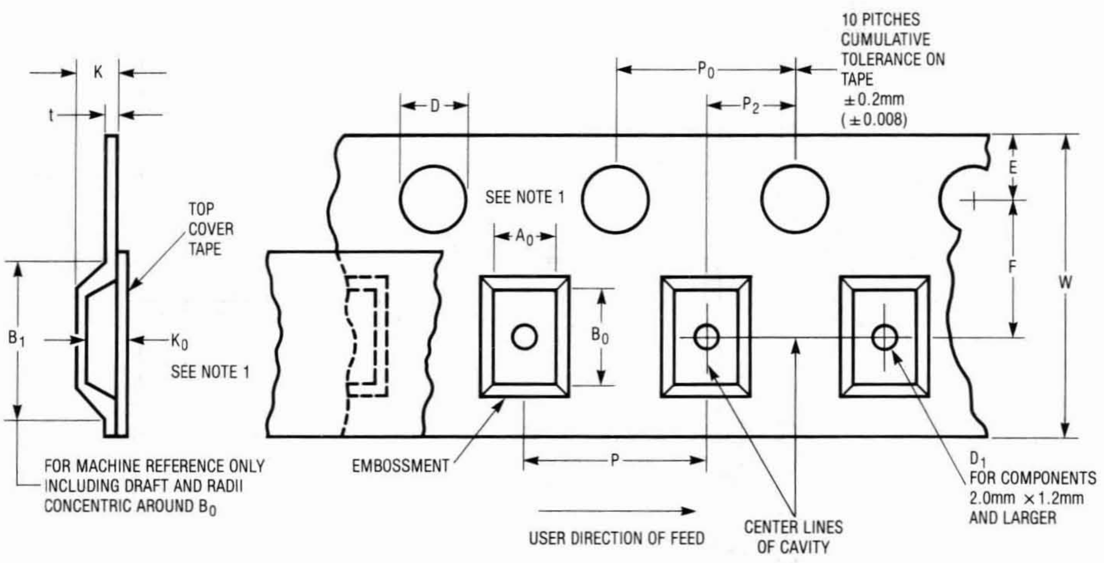

3.61
(0.142)
0.66
(0.026)
1.22 +0.25 −0.12
(0.048 +0.010 −0.005)
3.8
(0.150)
3.55
(0.140)
2.67
(0.105)
8.63
(0.340)
0.5 ± 0.12
(0.20 ± 0.005)
R 0.5mm
R (0.020)
4X, REF
SMP • 08

Figure 2 (Continued)

TAPE AND REEL SPECIFICATIONS

Embossed Carrier Dimensions (12mm, 16mm, 24mm Tape Only)


K
t
TOP COVER TAPE
B_1
K_0
SEE NOTE 1
FOR MACHINE REFERENCE ONLY INCLUDING DRAFT AND RADII CONCENTRIC AROUND B_0
D
P_0
P_2
10 PITCHES CUMULATIVE TOLERANCE ON TAPE ±0.2mm (±0.008)
SEE NOTE 1
A_0
B_0
E
F
W
EMBOSSMENT
P
USER DIRECTION OF FEED
CENTER LINES OF CAVITY
D_1 FOR COMPONENTS 2.0mm × 1.2mm AND LARGER

Embossed Tape — Constant Dimensions

Tape Size	D	E	P_0	t(Max.)	A_0 B_0 K_0
12mm, 16mm, 24mm	1.5 $^{+0.10}_{-0.0}$ 0.059 $^{+0.004}_{-0.0}$	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	0.400 (0.016)	See Note1

Embossed Tape Variable Dimensions

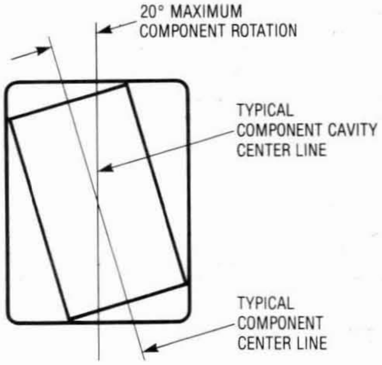
Tape Size	B_1 Max.	D_1 Min.	F	K Max.	P_2	R Min.	W
12mm	8.2 (0.323)	1.5 (0.059)	5.5 ± 0.05 (0.217 ± 0.002)	6.5 (0.177)	2.0 ± 0.05 (0.079 ± 0.002)	30 (1.181)	12.0 ± 0.30 (0.472 ± 0.012)
16mm	12.1 (0.476)		7.5 ± 0.10 (0.295 ± 0.004)	6.5 (0.256)	2.0 ± 0.10 (0.079 ± 0.004)	40 (1.575)	16 ± 0.30 (0.630 ± 0.012)
24mm	20.1 (0.791)		11.5 ± 0.10 (0.453 ± 0.004)			50 (1.969)	24 ± 0.30 (0.945 ± 0.012)

Note 1: A_0 B_0 K_0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) min. to 0.65 (0.026) max. for 12mm tape, 0.05 (0.002) min. to 0.90 (0.035) max. for 16mm tape and 0.050 (0.002) min. to 1.00 (0.039) max. for 24mm tape and larger. The component cannot rotate more than 20° within the determined cavity, see Component Rotation.

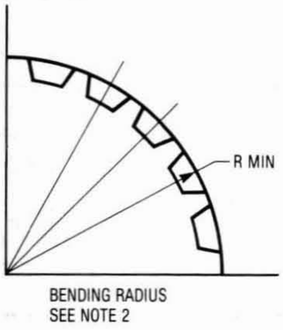
Note 2: Tape and components shall pass around radius "R" without damage.

TAPE AND REEL SPECIFICATIONS

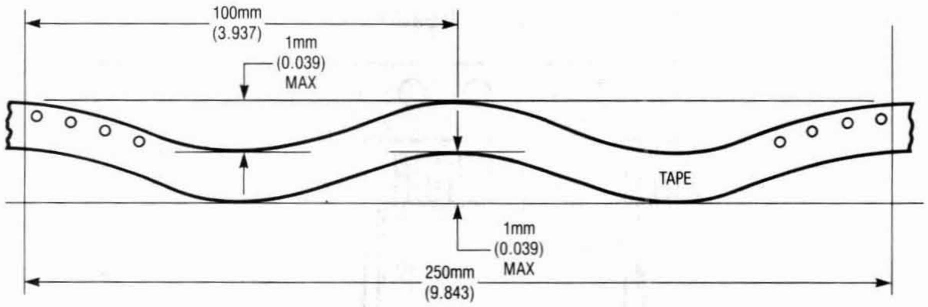
Component Rotation


20° MAXIMUM
COMPONENT ROTATION
TYPICAL
COMPONENT CAVITY
CENTER LINE
TYPICAL
COMPONENT
CENTER LINE

Bending Radius

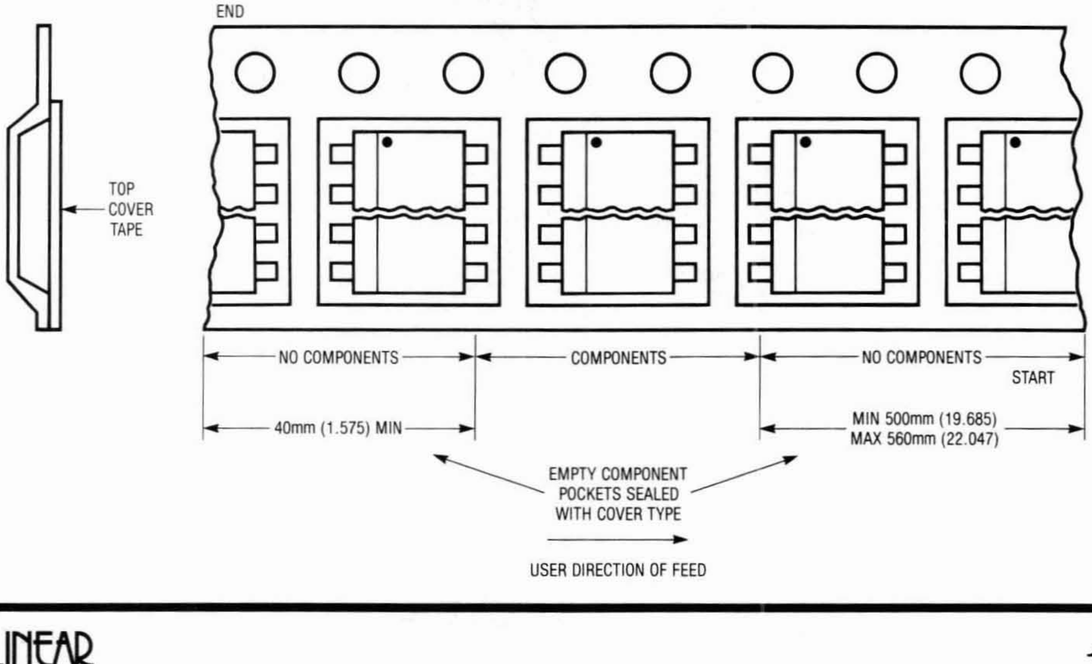

R MIN
BENDING RADIUS
SEE NOTE 2

Tape Camber (Top View)


100mm
(3.937)
1mm
(0.039)
MAX
TAPE
1mm
(0.039)
MAX
250mm
(9.843)

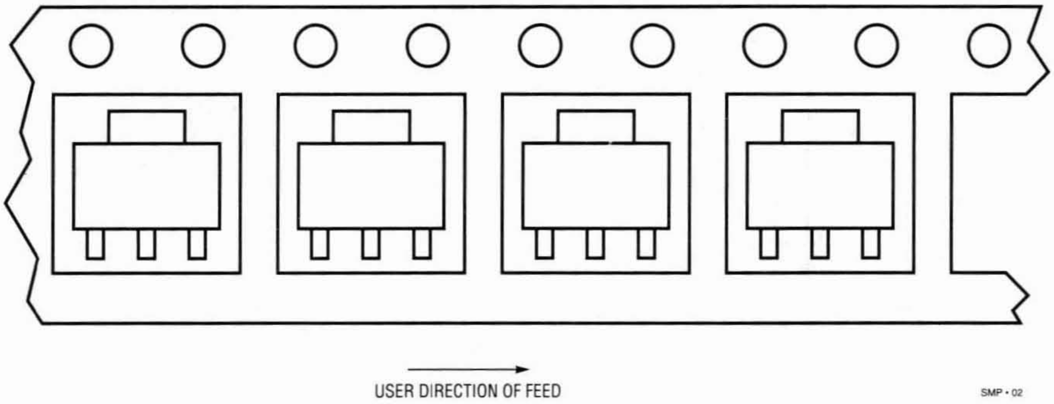
Allowable camber to be 1mm/100mm nonaccumulative over 250mm

Tape Leader (Start/End) Specification (SO Packages)

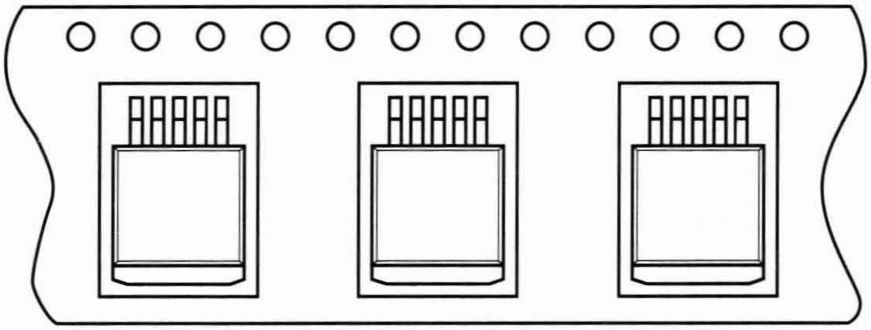

END
TOP
COVER
TAPE
NO COMPONENTS
COMPONENTS
NO COMPONENTS
START
40mm (1.575) MIN
MIN 500mm (19.685)
MAX 560mm (22.047)
EMPTY COMPONENT
POCKETS SEALED
WITH COVER TYPE
USER DIRECTION OF FEED

TAPE AND REEL SPECIFICATIONS

SOT-223 Devices

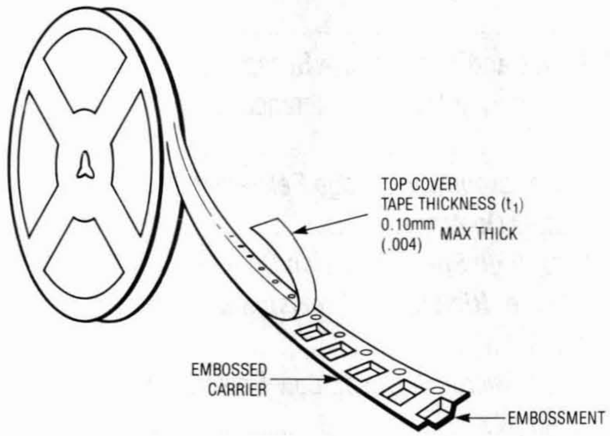

USER DIRECTION OF FEED
SMP • 02

DD Pack Devices

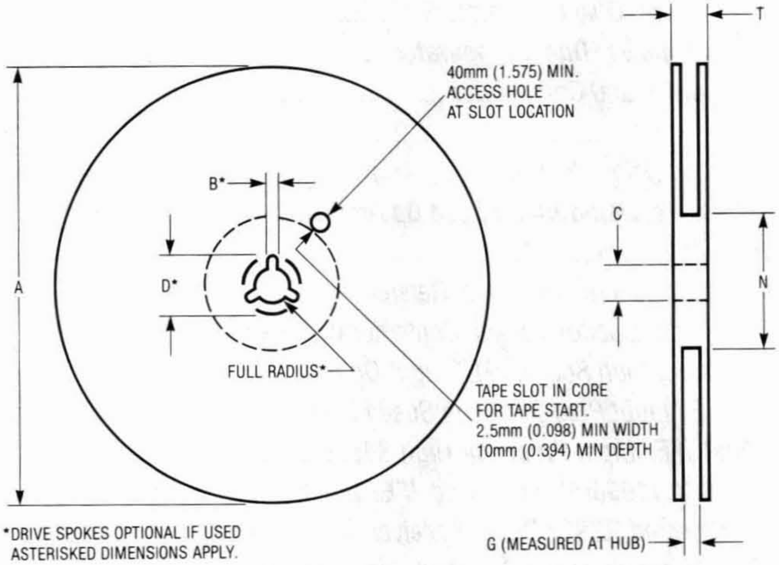


REEL DIMENSIONS

Direction of Feed


TOP COVER
TAPE THICKNESS (t_1)
0.10mm MAX THICK
(.004)
EMBOSSED
CARRIER
EMBOSSMENT

Reel Dimensions


T
40mm (1.575) MIN.
ACCESS HOLE
AT SLOT LOCATION
B*
C
D*
A
N
FULL RADIUS*
TAPE SLOT IN CORE
FOR TAPE START.
2.5mm (0.098) MIN WIDTH
10mm (0.394) MIN DEPTH
G (MEASURED AT HUB)

*DRIVE SPOKES OPTIONAL IF USED
ASTERISKED DIMENSIONS APPLY.

Tape Size	A Max.	B Min.	C	D* Min.	N Min.	G	T Max.
12mm	330 (12.992)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$12.4\ {}^{+2.0}_{-0.0}$ $\left(0.488\ {}^{+0.078}_{-0.0}\right)$	18.4 (0.724)
16mm	360 (14.173)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$16.4\ {}^{+2.0}_{-0.00}$ $\left(0.646\ {}^{+0.078}_{-0.00}\right)$	22.4 (0.882)
24mm	360 (14.173)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$24.4\ {}^{+2.0}_{-0.00}$ $\left(0.961\ {}^{+0.078}_{-0.00}\right)$	30.4 (1.197)

*Metric dimensions will govern.
English measurements rounded and for reference only.

SURFACE MOUNT DATA SHEETS LIST

LF398S8, Precision Sample and Hold Amplifier 9-113
LM318S8, High Speed Op Amp 2-319
LM334S8, Constant Current Source and Temperature Sensor 3-99
LM385S8-1.2/LM385S8-2.5, Micropower Voltage Reference 3-113
LT1001CS8, Precision Op Amp 2-23
LT1004CS8-1.2/LT1004CS8-2.5, Micropower Voltage References 3-25
LT1006S8, Precision, Single Supply Op Amp 2-53
LT1007CS/LT1037CS, Low Noise, High Speed Precision Op Amps 2-69
LT1007CS8/LT1037CS8, Low Noise, High Speed Precision Operational Amplifiers 2-16
LT1009S8, 2.5 Volt Reference 3-31
LT1012S8, Picoamp Input Current, Microvolt Offset, Low Noise Op Amp 2-117
LT1013DS8, Dual Precision Op Amp 2-141
LT1016CS8, Ultra Fast Precision Comparator 6-41
LT1017CS/LT1018CS, Micropower Dual Comparator 6-53
LT1017CS8/LT1018CS8, Micropower Dual Comparator 10-6
LT1020CS, Micropower Regulator and Comparator 4-45
LT1021DCS8, Precision Reference 3-57
LT1028CS, Ultra-Low Noise Precision High Speed Op Amp 2-177
LT1028CS8, Ultra-Low Noise Precision High Speed Op Amp 2-38
LT1030CS, Quad Low Power Line Driver 10-9
LT1034CS8-1.2/LT1034CS8-2.5, Micropower Dual Reference 3-81
LT1054CS/LT1054IS, Switched Capacitor Voltage Converter with Regulator 5-35
LT1055S8/LT1056S8, Precision, High Speed, JFET Input Op Amps 2-231
LT1057S/LT1057IS, Dual JFET Input Precision High Speed Op Amps 2-247
LT1057S8/LT1057IS8, Dual JFET Input Precision High Speed Op Amps 2-44
LT1057S/LT1057IS, LT1058S/LT1058IS, Dual/Quad JFET Input Precision High Speed Op Amps 2-41
LT1080CS/LT1081CS, 5V Powered RS232 Driver/Receiver with Shutdown 10-51
LTC1043CS, Dual Precision Instrumentation Switched-Capacitor Building Block 11-31
LTC1044CS8, Switched Capacitor Voltage Converter 5-21
LTC1052CS, Chopper-Stabilized Op Amp (CSOA™) 2-217
LTC1059CS, High Performance Switched Capacitor Universal Filter 7-11
LTC1060CS, Universal Dual Filter Building Block 7-35
LTC1061CS, High Performance Triple Universal Filter Building Block 7-55
LTC1062CS, 5th Order Lowpass Filter 7-71
OP-07CS8, Precision Op Amp 2-337
SG3524S, Regulating Pulse Width Modulator 5-93

NOTE: Items in **BOLD** are in this Databook Supplement, items not in bold are in 1990 Databook. Most recent products contain the surface mount device specifications in the main data sheet, therefore this list should not be considered representative of our full product offering. Please see the next pages.

Surface Mount Small Outline (SO) and SOT Device Packaging

Linear Technology now offers a continually increasing number of high performance CMOS and bipolar linear devices in surface mount packages. At the time of this printing, the following device types were available from LTC packaged in the SO (Small Outline Package), SOL (Large Outline) and the SOT-223 packages per the JEDEC standard outlines. For pinout configuration and electrical specification limits consult either your LTC sales representative or the factory.

PRODUCT		NOTES	DESCRIPTION
Operational Amplifiers			
LF398	S8	2	Sample & Hold Amp
LM318	S8	2	Fast Op Amp
LT1001C	S8	2	Precision Op Amp
LT1006	S8	2	Precision Single Supply Op Amp
LT1007C	S	2, A	Low Noise, High Speed Op Amp
LT1007C	S8**	5	Low Noise, High Speed Op Amp
LT1008	S8	2	Uncompensated, Picoamp Input Current, Precision Op Amp
LT1012	S8	1, 2	Picoamp Input Current, Precision Op Amp
LT1013D	S8	2, B	Dual Precision Single Supply Op Amp
LT1013I	S8	3, B	Dual Precision Single Supply Op Amp
LT1014D	S	4, 5, A	Quad Precision Single Supply Op Amp
LT1014I	S	3, A	Quad Precision Single Supply Op Amp
LT1028C	S	2, A	50MHz, 11V/µs, 1nV/√Hz Op Amp
LT1037C	S	2, A	High Speed Precision Op Amp
LT1037C	S8**	5	High Speed Precision Op Amp
LT1055	S8	2	JFET Input, High Speed, Precision Op Amp
LT1056	S8	2	JFET Input, High Speed, Precision Op Amp
LT1057	S	2, A	Dual JFET Input, High Speed, Precision Op Amp
LT1057	S8	2, B	Dual JFET Input, High Speed, Precision Op Amp
LT1057I	S	2, A	Dual JFET Input, High Speed, Precision Op Amp
LT1057I	S8	2, D	Dual JFET Input, High Speed, Precision Op Amp
LT1058	S	A	Quad JFET Input, High Speed, Precision Op Amp
LT1058I	S	A	Quad JFET Input, High Speed, Precision Op Amp
LT1077	S8	1	Precision Micropower Op Amp
LT1078	S	3, A	Dual Precision Micropower Op Amp
LT1078	S8	2, B	Dual Precision Micropower Op Amp
LT1078I	S	A	Dual Precision Micropower Op Amp
LT1078I	S8	2, D	Dual Precision Micropower Op Amp
LT1079	S	3, A	Quad Precision Micropower Op Amp
LT1079I	S	A	Quad Precision Micropower Op Amp
LT1097	S8	1	Low Cost, Low Power, Precision Op Amp
LT1115C	S	1, A	50MHz, 11V/µs, 1nV/√Hz Audio Op Amp
LT1122C	S8	1	Fast Settling, JFET Input Op Amp
LT1122D	S8	1	Fast Settling, JFET Input Op Amp
LT1124C	S8	1	Dual Low Noise, High Speed, Precision Op Amp
LT1125C	S	1, A	Quad Low Noise, High Speed, Precision Op Amp
LT1126C	S8	1	Decomp Dual Low Noise, High Speed, Precision Op Amp
LT1127C	S	1, A	Decomp Dual Low Noise, High Speed, Precision Op Amp
LT1178	S	1, A	Dual Precision Micropower Op Amp
LT1179	S	1, A	Quad Precision Micropower Op Amp
LT1190C	S8	1, 5, C	50MHz High Speed Video Op Amp
LT1191C	S8	1, 5, C	90MHz High Speed Video Op Amp
LT1192C	S8	1, 5, C	350MHz ($A_V \geq 25$)High Speed Video Op Amp
LT1193C	S8	1, 5, C	80MHz (Adj Gain) High Speed Video Op Amp
LT1194C	S8	1, 5, C	35MHz ($A_V = 10$) Fixed Differential High Speed Video Op Amp
LT1223C	S8	1	100MHz Current Feedback Amplifier
LT1224C	S8	1	Very High Speed Op Amp
LT1228C	S8	1, 5, C	100MHz Current Feedback Amplifier w/DC Gain Control
LT1229C	S8	1, 5, C	Dual 100MHz Current Feedback Amplifier
LT1230C	S	1, 5, C	Quad 100MHz Current Feedback Amplifier
LTC1047C	S	1, A	Dual Micropower Chopper Stabilized Op Amp w/ Internal Caps
LTC1049C	S8	1	Low Power Chopper Stabilized Amplifier w/ Internal Caps
LTC1050C	S8	1	Chopper Stabilized Op Amp w/Internal Caps
LTC1051C	S	1, A	Dual Chopper Stabilized Op Amp w/Internal Caps
LTC1052C	S	2, A	Low Noise Chopper Stabilized Op Amp
LTC1053C	S	2, A	Quad Precision Chopper Stabilized Op Amp w/ Internal Caps
LTC1150C	S8	1	±15V Chopper Stabilized Op Amp w/Internal Caps
OP-07C	S8	2	Precision Op Amp
OP-470G	S	1	Quad Low Noise, Precision Op Amp
Instrumentation Amps			
LTC1100C	S	1, A	Chopper Stabilized Instrumentation Amp
LT1101	S	3	Precision Micropower Instrumentation Amp
Comparators			
LT1016C	S8	2	High Speed Comparator
LT1016I	S8	6, D	High Speed Comparator
LT1017C	S	2, A	Micropower Dual Comparator
LT1018C	S	2, A	Micropower Dual Comparator
LTC1040C	S	4, 5, A	Micropower Dual Sampling Comparator
Data Acquisition			
LTC1090C	S	4,5,A,C	10-Bit ADC with 8 Ch MUX & S/H
LTC1093C	S	4,5,A,C	10-Bit ADC with 6 Ch MUX & S/H
LTC1099C	S	5, C	8-Bit High Speed ADC with S/H
LTC1099I	S	9, C	8-Bit High Speed ADC with S/H
LTC1290BC	S	5, A, C	12-Bit ADC with 8 Ch MUX & S/H
LTC1290CC	S	5, A, C	12-Bit ADC with 8 Ch MUX & S/H
LTC1290DC	S	5, A, C	12-Bit ADC with 8 Ch MUX & S/H
LTC1294BC	S	5, A, C	12-Bit ADC with 8 Ch MUX & S/H
LTC1294CC	S	5, A, C	12-Bit ADC with 8 Ch MUX & S/H
LTC1294DC	S	5, A, C	12-Bit ADC with 8 Ch MUX & S/H
Regulators*, PWMs, DC to DC Converters			
LT1020C	S	2, A	µPower Low Dropout Regulator w/Comparator
LT1020I	S	2,7,A,D	µPower Low Dropout Regulator w/Comparator
LT1072C	S	4, A	40kHz 1.25A Switching Regulator
LT1072C	S8	3, C	40kHz 1.25A Switching Regulator
LT1076C	R-5	2	2A Step-Down Switching Regulator w/Shutdown, 7-Lead DD Pkg, 5V
LT1086C	M	2	1.5A Low Dropout Regulator, 3-Lead DD Pkg
LT1117C	ST	1	Low Dropout 800mA Adjustable Regulator
LT1117C	ST-5	1	Low Dropout 800mA Regulator, 5V
LT1117C	ST-2.85	1	Active SCSI-2 Terminator, 2.85V
LT1171C	Q	2	100kHz 2.5A Switching Regulator, 5-Lead DD Pkg
LT1172C	S	4, A	100kHz 1.25A Switching Regulator
LT1172C	S8	3, C	100kHz 1.25A Switching Regulator
SG3524	S	2	Pulse Width Modulator
LT1073C	S8, S8-5, S8-12	1	µPower Switching Regulator Works Down to 1V Input. Adjustable & Fixed +5V, +12V Outputs
LT1109C	S8-5, S8-12	1	µPower DC to DC Converter w/Shutdown & 100kHz Switching Frequency, Fixed +5V & +12V Outputs.
LT1110C	S8, S8-5, S8-12	1	µPower DC to DC Converter Works Down to 1V Input. Adjustable & Fixed +5V, +12V Outputs
LT1111C	S8, S8-5, S8-12	1	µPower Switching Regulator Works Down to 2V Input. Adjustable and Fixed +5V, +12V Outputs.
LT1123C	S8-2.85	1	Low Dropout Regulator Driver
LT1172C	S8	1	1.25A High Efficiency 100kHz Switching Reg
LT1173C	S8, S8-5, S8-12	1	µPower Switching Regulator for Inputs Greater Than 2V. Adjustable and Fixed +5V, +12V Versions
LT1271C	Q	2	60kHz 4A Switching Regulator, 5-Lead DD Pkg
LT1432C	S8	2	High Efficiency Switching Regulator Controller

Surface Mount Small Outline (SO) and SOT Device Packaging

PRODUCT		NOTES	DESCRIPTION
Switched Capacitor Converters			
LT1054C	S	2, A	100mA Switched Capacitor Voltage Converter
LT1054I	S	2, A	100mA Switched Capacitor Voltage Converter
LTC1043C	S	2, A	Dual Precision Instrumentation Switched Capacitor Building Block
LTC1044C	S8	2	Switched Capacitor Voltage Converter
LTC1046C	S8	1	50mA Switched Capacitor Voltage Converter
LTC1046CI	S8	1, C	50mA Switched Capacitor Voltage Converter
Switched Capacitor Filters			
LTC1059C	S	2	2nd Order Universal Filter
LTC1060C	S	2, A	Dual 2nd Order Universal Filter
LTC1061C	S	2, A	Triple 2nd Order Universal Filter
LTC1062C	S	2, 7, A	5th Order Lowpass Filter (Patented)
LTC1064C	S	1, 7, A	100kHz Quad 2nd Order Universal Filter
LTC1064-1C	S	1, 7, A	8th Order Cauer Lowpass Filter
LTC1064-2C	S	1, A	8th Order Butterworth Lowpass Filter
LTC1064-3C	S	1, A	8th Order Bessel (Linear Phase) Lowpass Filter
LTC1064-4C	S	1, 7, A	8th Order Cauer/Transitional Lowpass Filter
LTC1064-XXC	S	A	High Speed, Low Noise Quad Semi-Custom Filter
LTC1164C	S	1, 7, A	Low Power Quad 2nd Order Universal Filter
LTC1164-XXC	S	A	Low Power, Low Noise Quad Semi-Custom Filter
References			
LM334	S8	2	Constant Current Source & Temp. Sensor
LM385	S8-1.2	2	1.2V Bandgap Voltage Reference
LM385	S8-2.5	2	2.5V Bandgap Voltage Reference
LM385B	S8-1.2	5, D	1.2V Bandgap Voltage Reference
LM385B	S8-2.5	5, D	2.5V Bandgap Voltage Reference
LT1004C	S8-1.2	2	1.2V Bandgap Voltage Reference
LT1004C	S8-2.5	2	2.5V Bandgap Voltage Reference
LT1004I	S8-1.2	8, D	1.2V Bandgap Voltage Reference
LT1004I	S8-2.5	8, D	2.5V Bandgap Voltage Reference
LT1009	S8	2	2.5V Reference
LT1009I	S8	8, D	2.5V Reference
LT1019C	S8-2.5	4, 5, C	2.5V Buried Zener Precision Reference
LT1019C	S8-4.5	5, C	4.5V Buried Zener Precision Reference
LT1019C	S8-5	5, C	5V Buried Zener Precision Reference
LT1019C	S8-10	5, C	10V Buried Zener Precision Reference
LT1021DC	S8-5	2, C	5V Buried Zener Precision Reference
LT1021DC	S8-7	2, C	7V Buried Zener Precision Reference
LT1021DC	S8-10	2, C	10V Buried Zener Precision Reference
LT1034C	S8-1.2	2, C	Micropower Dual Reference: 1.2V, +7V
LT1034C	S8-2.5	2, C	Micropower Dual Reference: 2.5V, +7V
LT1431C	S8	1, C	Programmable Reference
LT1431I	S8	1, C	Programmable Reference
Interface Circuits			
LT1030C	S	1, 2	Quad Low Power Line Driver
LT1032C	S	4, 5, A	Quad Low Power Line Driver with Response Time Control
LT1039C	S	1, A	3 TX/3 RX RS232 XCVR with Shutdown
LT1039I	S		3 TX/3 RX RS232 XCVR with Shutdown
LT1039C	S16	5, C	3 TX/3 RX RS232 XCVR
LT1080C	S	2, A	Dual RS232 XCVR with +5V to ± 9V Pump & Shutdown
LT1080I	S	9, D	Dual RS232 XCVR with +5V to ± 9V Pump
LT1081C	S	2, A	Dual RS232 XCVR with +5V to ± 9V Pump & Shutdown
LT1081I	S	9, D	Dual RS232 XCVR with +5V to ± 9V Pump
LT1130C	S	1, A	5 TX/5 RX RS232 XCVR with +5V to ± 9V Pump
LT1131C	S	1, A	5 TX/4 RX RS232 XCVR with +5V to ± 9V Pump & Shutdown
LT1132C	S	1, A	5 TX/3 RX RS232 XCVR with +5V to ± 9V Pump
LT1133C	S	1, A	3 TX/5 RX RS232 XCVR with +5V to ± 9V Pump
LT1134C	S	1, A	4 TX/4 RX RS232 XCVR with +5V to ± 9V Pump
LT1135C	S	1, A	5 TX/3 RX RS232 XCVR
LT1136C	S	1, A	4 TX/5 RX RS232 XCVR with +5V to ± 9V Pump & Shutdown
LT1137C	S	1, A	3 TX/5 RX RS232 XCVR with +5V to ± 9V Pump & Shutdown
LT1138C	S	1, A	5 TX/3 RX RS232 XCVR with +5V to ± 9V Pump & Shutdown
LT1139C	S	1, A	4 TX/4 RX RS232 XCVR, +5V/+12V Powered with Shutdown
LT1140C	S	1, A	5 TX/3 RX RS232 XCVR with Shutdown
LT1141C	S	1, A	3 TX/5 RX RS232 XCVR with Shutdown
LT1180C	S	1, A	Dual RS232 XCVR with +5V to ± 9V Pump & Shutdown
LT1181C	S	1, A	Dual RS232 XCVR with +5V to ± 9V Pump
LT1180I	S	1, A	Dual RS232 XCVR with +5V to ± 9V Pump & Shutdown
LT1181I	S	1, A	Dual RS232 XCVR with +5V to ± 9V Pump
LT1280C	S	1, A	Low Power Dual RS232 XCVR with +5V to ±9V Pump & Shutdown
LT1281C	S	1, A	Low Power Dual RS232 XCVR with +5V to ±9V Pump
LT1281I	S	1, D	Low Power Dual RS232 XCVR with +5V to ±9V Pump
LTC485C	S8	1	Ultra Low Power RS485
LTC485I	S8	1	Interface
LTC486C	S	1, A	Ultra Low Power RS485 Interface Device
LTC486I	S	1, A	Ultra Low Power RS485 Interface Device
LTC487C	S	1, A	Ultra Low Power RS485 Interface Device
LTC487I	S	1, A	Ultra Low Power RS485 Interface Device
Analog Switches			
LTC201AC	S	1	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC202C	S	1	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC203C	S	1	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC221C	S	1	Micropower, Low Charge Injection, Quad CMOS Analog Switch with Data Latches
LTC222C	S	1	Micropower, Low Charge Injection, Quad CMOS Analog Switch with Data Latches
Watchdog Timer/Microprocessor Supervisory			
LTC690C	S8	1	Microprocessor Supervisory Circuit
LTC690I	S8	1	Microprocessor Supervisory Circuit
LTC691C	S	1	Microprocessor Supervisory Circuit
LTC691I	S	1	Microprocessor Supervisory Circuit
LTC694C	S8	1	Microprocessor Supervisory Circuit
LTC694I	S8	1	Microprocessor Supervisory Circuit
LTC695C	S	1	Microprocessor Supervisory Circuit
LTC695I	S	1	Microprocessor Supervisory Circuit
LTC699C	S8	1	Microprocessor Supervisory Circuit
LTC1232C	S8	1	Microprocessor Supervisory Circuit
LTC1235C	S	1	Microprocessor Supervisory Circuit

NOTES:

1. See standard data sheet for electrical specs and SO package pinout.
2. Separate data sheet exists for surface mount version of this product (includes specs and pinout).
3. Marketing specification notice exists for this device showing electrical specs and SO pkg pinout.
4. Marketing specification notice exists for this device showing SO package pinout.
5. Meets existing commercial specs over 0°C to 70°C range.
6. Meets existing military specs over 0°C to 70°C range.
7. Meets existing commercial specs over −40°C to 85°C range.
8. Meets existing military specs over −40°C to 85°C range.
9. Meets existing industrial specs over −40°C to 85°C range.

A. SOL (0.300 in. wide) large outline package.
B. Non-standard pinout.
C. Pinout is identical to DIP (through-hole) package.
D. Pinout is identical to commercial temperature surface mount package.

* All TO-220 voltage regulators may be surface mounted using optional "Flow 32" lead bend.
** Data sheet for this product is in process.

INTRODUCTION

Linear Technology Corporation offers a wide variety of precision linear IC's in die form. It is our intent to offer dice electrically tested to levels which can be expected to yield the best possible performance in hybrid circuits. Complicating this task is the fact that many specifications given for our standard packaged products cannot be tested at the wafer level. Further, parameters which are 100% tested at wafer probe testing may shift during the die attach/assembly process.

There is a Dice Products Catalog available that contains ordering information and datasheets for obtaining dice products. Catalogs are available from your local LTC Sales Rep, or from LTC Communications at (800) 637-5545.

GENERAL INFORMATION

Electrical Testing

Dice are 100% tested in wafer form at 25°C to the DC limits shown on the dice data sheet for a given device type. Many LTC packaged products have multiple electrical grades associated with a basic die type. A cross reference appears on each dice data sheet indicating which die product grade should be ordered to optimize candidates to meet the specifications of the desired finished product grade. This information should be used as a guideline only since LTC does not guarantee electrical specifications after assembly. Since electrical testing is done only at 25°C, no absolute guarantee can be made regarding performance at other temperatures. Some LTC products require post-package trimming to overcome certain assembly related parameter shifts. Details on this trimming may be obtained by contacting the factory.

Visual Inspection

Dice are 100% visually inspected in accordance with MIL-STD-883, Method 2010 Condition B.

Chip Dimensions

Chip dimensions are as indicated on individual dice data sheets. Tolerance is ±1 mil. Chip thickness ranges from 12 mils to 20 mils, depending on product type. Bond pad dimensions are 4.5 x 4.5 mils. minimum.

Topside Passivation

Linear Technology products are passivated with a two layer system: A proprietary deposited oxide gives a crack-free conformal coverage of metal and oxide steps. A plasma nitride overcoat protects the die from ionic contamination and scratches during handling, testing and assembly. Note that LTC uses fuse link and zener zap trimming techniques which require windows in the passivation over the trim points. This passivation system is a major contributor to the extremely high reliability demonstrated throughout millions of device-hours of accelerated testing of LTC devices in plastic and hermetic packages.

Topside Metallization

The metallization is a minimum of 11,000 Å thick unless otherwise specified. The quality of the metallization step coverage is monitored via a weekly SEM inspection per MIL-STD-883, Method 2018.

Backside Metal

Most dice product backsides are coated with an alloyed gold layer. There are some CMOS products with no backside metallization. In addition, some voltage regulators may be specially ordered with a chrome-nickle-silver (Cr-Ni-Ag) backside layer. Contact LTC for details on this type of backside layer or to inquire about availability of LTC products with a particular backside metallization.

Backside Potential

Linear Technology products are junction isolated. For proper operation the backside must be electrically connected to the most negative potential seen by the IC (for bipolar products) or the most positive potential (for CMOS products). This information is also given in the individual dice data sheets.

Packaging

Dice are packaged in compartmentalized waffle packs for ease of handling and storage. Each waffle pack contains 100 dice. Special packaging methods are also available by contacting the factory.

Quality Levels of Dice Shipped

Each dice lot is guaranteed to meet the following requirements:

- Internal visual per MIL-STD-883, Method 2010 Condition B: 1.0% AQL Level II.
- Electrical: Due to variations in assembly methods and packaging techniques LTC does not guarantee electrical specifications after assembly. When a determination as to the finished product assembly yield is needed, the lot acceptance testing available at extra cost should be pursued.

Reliability Assurance

In addition to the more conventional reliability audits performed on finished products, LTC has innovated a unique periodic wafer fab reliability audit using a specially designed reliability structure that is stepped into all wafers. The test structure is optimized to accelerate the two primary failure mechanisms in linear circuits, namely mobile positive ions and surface charge-induced inversions. This provides a continuous monitor on the reliability performance of LTC's wafer fab processes and provides immediate feedback to wafer fab typically within one week.

Electrostatic Discharge (ESD) Precautions

Precision linear devices, especially those with very low (pA) input bias current levels and low (<50 microvolts) input offset voltages are susceptible to shifts in electrical performance and ESD damage as a result of improper handling. LTC recommends that ESD precautions, such as grounded conductive work stations, grounded conductive wrist straps and grounded equipment, be taken to prevent ESD damage.

ORDERING INFORMATION

Dice may be ordered by the part number defined in the dice data sheet. Minimum direct dice order, per delivery, is 1000 pieces or $5,000, whichever is greater. In some cases, tighter parameter selections than indicated on the dice data sheets can be obtained by special order. Please contact the factory for details.

Lot Acceptance Testing

Lot acceptance testing (L.A.T.) based on sample assembly and testing is available at extra cost. Sample sizes and acceptable electrical test limits vary from device to device and must be negotiated at the time of quoting. Contact the factory for details.

Application Notes

AN1 **Understanding and Applying the LT1005 Multifunction Regulator**

This application note describes the unique operating characteristics of the LT1005 and describes a number of useful applications which take advantage of the regulator's ability to control the output with a logic control signal.

AN2 **Performance Enhancement Techniques for 3-Terminal Regulators**

This application note describes a number of enhancement circuit techniques used with existing 3-terminal regulators which extend current capability, limit power dissipation, provide high voltage output, operate from 110VAC or 220VAC without the need to switch transformer windings, and many other useful application ideas.

AN3 **Applications for a Switched-Capacitor Instrumentation Building Block**

This application note describes a wide range of useful applications for the LTC1043 dual precision instrumentation switched-capacitor building block. Some of the applications described are ultra high performance instrumentation amplifier, lock-in amplifier, wide range digitally controlled variable gain amplifier, relative humidity sensor signal conditioner, LVDT signal conditioner, charge pump F to V and V to F converters, 12-bit A to D converter and more.

AN4 **Applications for a New Power Buffer**

The LT1010 150μA power buffer is described in a number of useful applications such as boosted op amp, a feed-forward, wideband DC stabilized buffer, a video line driver amplifier, a fast sample-hold with hold step compensation, an overload protected motor speed controller, and a piezoelectric fan servo.

AN5 **Thermal Techniques in Measurement and Control Circuitry**

6 applications utilizing thermally based circuits are detailed. Included are a 50MHz RMS to DC converter, an anemometer, a liquid flowmeter and others. A general discussion of thermodynamic considerations involved in circuitry is also presented.

AN6 **Applications of New Precision Op Amps**

Application considerations and circuits for the LT1001 and LT1002 single and dual precision amplifiers are illustrated in a number of circuits, including strain gauge signal conditioners, linearized platinum RTD circuits, an ultra precision dead zone circuit for motor servos and other examples.

AN7 **Some Techniques for Direct Digitization of Transducer Outputs**

Analog-to-digital conversion circuits which directly digitize low level transducer outputs, without DC preamplification, are presented. Covered are circuits which operate with thermocouples, strain gauges, humidity sensors, level transducers and other sensors.

AN8 **Power Conditioning Techniques for Batteries**

A variety of approaches for power conditioning batteries is given. Switching and linear regulators and converters are shown, with attention to efficiency and low power operation. 14 circuits are presented with performance data.

AN9 **Application Considerations and Circuits for a New Chopper-Stabilized Op Amp**

A discussion of circuit, layout and construction considerations for low level DC circuits includes error analysis of solder, wire and connector junctions. Applications include sub-microvolt instrumentation and isolation amplifiers, stabilized buffers and comparators and precision data converters.

AN 10 **Methods for Measuring Op Amp Settling Time**

Application Note 10 begins with a survey of methods for measuring op amp settling time. This commentary develops into circuits for measuring settling time to 0.0005%. Construction details and results are presented. Appended sections cover oscilloscope overload limitations and amplifier frequency compensation.

AN11 **Designing Linear Circuits for 5V Operation**

This note covers the considerations for designing precision linear circuits which must operate from a single 5V supply. Applications include various transducer signal conditioners, instrumentation amplifiers, controllers and isolated data converters.

AN12 **Circuit Techniques for Clock Sources**

Circuits for clock sources are presented. Special attention is given to crystal-based designs including TXCOs and VXCOs.

AN13 **High Speed Comparator Techniques**

The AN13 is an extensive discussion of the causes and cures of problems in very high speed comparator circuits. A separate applications section presents circuits, including a 0.025% accurate 1Hz-30MHz V to F converter, a 200ns 0.01% sample-hold and a 10MHz fiber optic receiver. Five appendices covering related topics complete this note.

AN14 **Designs for High Frequency Voltage-To-Frequency Converters**

A variety of high performance V to F circuits is presented. Included are a 1Hz to 100MHz design, a quartz stabilized type and a 0.0007% linear unit. Other circuits feature 1.5V operation, sine wave output and non-linear transfer functions. A separate section examines the trade-offs and advantages of various approaches to V to F conversion.

AN15 **Circuitry for Single Cell Operation**

1.5V powered circuits for complex linear functions are detailed. Designs include a V to F converter, a 10 bit A→D, sample-hold amplifiers, a switching regulator and other circuits. Also included is a section on component considerations for 1.5V powered linear circuits.

AN16 **Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers**

This note describes some of the unique IC design techniques incorporated into a fast, monolithic power buffer, the LT1010. Also, some application ideas are described such as capacitive load driving, boosting fast op amp output current and power supply circuits.

AN17 **Considerations for Successive Approximation A→D Converters**

A tutorial on SAR type A→D converters, this note contains detailed information on several 12-bit circuits. Comparator, clocking, and pre-amplifier designs are discussed. A final circuit gives a 12-bit conversion in 1.8μs. Appended sections explain the basic SAR technique and explore DAC considerations.

AN18 **Power Gain Stages for Monolithic Amplifiers**

This note presents output stage circuits which provide power gain for monolithic amplifiers. The circuits feature voltage gain, current gain, or both. Eleven designs are shown, and performance is summarized. A generalized method for frequency compensation appears in a separate section.

AN19 **LT1070 Design Manual**

This design manual is an extensive discussion of all standard switching configurations for the LT1070; including buck, boost, flyback, forward, inverting and "Cuk". The manual includes comprehensive information on the LT1070, the external components used with it, and complete formulas for calculating component values.

AN20 **Applications for a DC Accurate Low-Pass Switched-Capacitor Filter**

Discusses the principles of operation of the LTC1062 and helpful hints for its application. Various application circuits are explained in detail with focus on how to cascade two LTC1062's and how to obtain notches. Noise and distortion performance are fully illustrated.

AN21 **Composite Amplifiers**

Applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. AN21 shows examples of composite approaches in designs combining speed, precision, low noise and high power.

AN22 **A Monolithic IC for 100MHz RMS-DC Conversion**

AN22 details the theoretical and application aspects of the LT1088 thermal RMS-DC converter. The basic theory behind thermal RMS-DC conversion is discussed and design details of the LT1088 are presented. Circuitry for RMS-DC converters, wideband input buffers and heater protection is shown.

AN23 **Micropower Circuits for Signal Conditioning**

Low power operation of electronic apparatus has become increasingly desirable. AN23 describes a variety of low power circuits for transducer signal conditioning. Also included are designs for data converters and switching regulators. Three appended sections discuss guidelines for micropower design, strobed power operation and effects of test equipment on micropower circuits.

AN24 **Unique Applications for the LTC1062 Lowpass Filter**

Highlights the LTC1062 as a lowpass filter in a phase lock loop. Describes how the loop's bandwidth can be increased and the VCO output jitter reduced when the LTC1062 is the loop filter. Compares it with a passive RC loop filter.

Also discussed is the use of LTC1062 as simple bandpass and bandstop filter.

AN25 **Switching Regulators for Poets**

Subtitled "A Gentle Guide for the Trepidatious", this is a tutorial on switching regulator design. The text assumes no switching regulator design experience, contains no equations, and requires no inductor construction to build the circuits described.

Designs detailed include flyback, isolated telecom, off-line, and others. Appended sections cover component considerations, measurement techniques and steps involved in developing a working circuit.

AN26 A collection of interface applications between various microprocessors/controllers and the LTC1090 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN26A	LTC1090	8051
AN26B	LTC1090	68HC05
AN26C	LTC1090	63705
AN26D	LTC1090	COP820
AN26E	LTC1090	TMS7742
AN26F	LTC1090	COP402N
AN26G	LTC1091	8051
AN26H	LTC1091	68HC05
AN26I	LTC1091	COP820
AN26J	LTC1091	TMS7742
AN26K	LTC1091	COP402N
AN26L	LTC1091	HD63705VO
AN26M	LTC1090	TMS320C25
AN26N	LTC1091/92	TMS320C25
AN26O	LTC1090	Z-80
AN26P	LTC1090	HD64180
AN26Q	LTC1091	HD64180
AN26R	LTC1094	TMS320C25

These interface notes demonstrate the ease with which the LTC1090 family can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN27A **A Simple Method of Designing Multiple Order All Pole Bandpass Filters by Cascading 2nd Order Sections**

Presents two methods of designing high quality Switched Capacitor bandpass filters. Both methods are intended to vastly simplify the mathematics involved in filter design by using tabular methods. The text assumes no filter design experience but allows high quality filters to be implemented by techniques not presented before in the literature. The designs are implemented by numerous examples using devices from LTC's Switched Capacitor filter family: LTC1060, LTC1061, and LTC1064. Butterworth and Chebyshev bandpass filters are discussed.

AN28 **Thermocouple Measurement**

Considerations for thermocouple based temperature measurement are discussed. A tutorial on temperature sensors summarizes performance of various types, establishing a perspective on thermocouples. Thermocouples are then focused on. Included are sections covering cold-junction compensation, amplifier selection, differential/isolation techniques, protection, and linearization. Complete schematics are given for all circuits. Processor based linearization is also presented with the necessary software detailed.

AN29 **Some Thoughts on DC-DC Converters**

This note examines a wide range of DC-DC converter applications. Single inductor, transformer, and switched capacitor converter designs are shown. Special topics like low noise, high efficiency, low quiescent current, high voltage, and wide-input voltage range converters are covered. Appended sections explain some fundamental properties of different types of converters.

AN30 **Switching Regulator Circuit Collection**

Switching regulators are of universal interest. Linear Technology has made a major effort to address this topic. A catalog of circuits has been compiled so that a design engineer can swiftly determine which converter type is best. This catalog serves as a visual index to be browsed through for a specific or general interest.

AN31 **Linear Circuits for Digital Systems**

Subtitled "Some Affable Analogs for Digital Devotees," discusses a number of analog circuits useful in predominantly digital systems. Vpp generators for flash memories receive extensive treatment. Other examples include a current loop transmitter, dropout detectors, power management circuits, and clocks.

AN32 **High Efficiency Linear Regulators**

Presents circuit techniques permitting high efficiency to be obtained with linear regulation. Particular attention is given to the problem of maintaining high efficiency with widely varying inputs, outputs and loading. Appendix sections review component characteristics and measurement methods.

AN33 **Converting Light to Digits: LTC1099 Half Flash 8-Bit A/D Converter Digitizes Photodiode Array**

This application note describes a Linear Technology "Half Flash" A/D converter, the LTC1099, being connected to a 256 element line scan photodiode array. This technology adapts itself to hand held (i.e. low power) bar code readers, as well as high resolution automated machine inspection applications.

AN34 **LTC1099 Enables PC Based Data Acquisition Board to Operate DC-20kHz**

A complete design for a data acquisition card for the IBM PC is detailed in this application note. Additionally, C language code is provided to allow sampling of data at speeds of more than 20kHz. The speed limitation is strictly based on the execution speed of the "C" data acquisition loop. A "Turbo" XT can acquire data at speeds greater than 20kHz. Machines with 80286 and 80386 processors can go faster than 20kHz. The computer that was used as a test bed in this application was an XT running at 4.77MHz and therefore all system timing and acquisition time measurements are based on that the 4.77MHz clock speed.

AN35 **Step Down Switching Regulators**

Discusses the LT1074, an easily applied step down regulator IC. Basic concepts and circuits are described along with more sophisticated applications. Six appended sections cover LT1074 circuitry detail, inductor and discrete component selection, current measuring techniques, efficiency considerations and other topics.

AN36 A collection of interface applications between various microprocessors/controllers and the LTC1290 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN36A	LTC1290	8051
AN36B	LTC1290	MC68HC05
AN36C	LTC1290/LTC1090	TMS370
AN36D	LTC1290	COP820C
AN36E	LTC1290	TMS7742
AN36F	LTC1290	COP402N
AN36O	LTC1290	Z-80
AN36P	LTC1290	HD64180

These interface notes demonstrate the ease with which the LTC1290 can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN37 **Fast Charge Circuits For NiCad Batteries**

Safe, fast-charging of NiCad batteries is attractive in many applications. This note details simple, thermally-based fast charge circuitry for NiCads. Performance data is summarized and compared to other charging methods.

AN38 **FilterCAD User's Manual, Version 1.00**

This note is the manual for FCAD, a computer-aided design program for designing filters with LTC's switched capacitor filter family. FCAD helps users design good filters with a minimum amount of effort. The experienced filter designer can use the program to achieve better results by providing the ability to play "what if" with the values and configuration of various components.

AN39 **Parasitic Capacitance Effects in Step-Up Transformer Design**

This note explores the causes of the large resonating current spikes on the leading edge of the switch current waveform. These anomalies are exacerbated in very high voltage designs.

AN40 **Take the Mystery Out of the Switched Capacitor Filter: The System Designer's Filter Compendium**

This note presents guidelines for circuits utilizing LTC's switched capacitor filters. The discussion focuses on how to optimize filter performance by optimizing the printed wiring board, the power supply, and the output buffering of the filter. Many additional topics are discussed such as how to select the proper filter response for the application and how to characterize a filter's T.H.D. for DSP applications.

AN 41 **Questions and Answers on the SPICE Macromodel Library**

This note provides answers to some of the more common questions concerning LTC's Macromodel Library. Topics include hardware and software requirements, model characteristics, and limitations and interpretation of results.

AN 42 **Voltage Reference Circuit Collection**

A wide variety of voltage reference circuits are detailed in this extensive guidebook of circuits. The detailed schematics cover simple and precision approaches at a variety of power levels. Included are 2 and 3 terminal devices in series and shunt modes for positive and negative polarities. Appended sections cover resistor and capacitor selection and trimming techniques.

AN 43 **Bridge Circuits**

Subtitled "Marrying Gain and Balance", this note covers signal conditioning circuits for various types of bridges. Included are transducer bridges, AC bridges, Wien bridge oscillators, Schottky bridges, and others. Special attention is given to amplifier selection criteria. Appended sections cover strain gage transducers, understanding distortion measurements, and historical perspectives on bridge readout mechanisms and Wein bridge oscillators.

AN 44 **LT1074/LT1076 Design Manual**

This note discusses the use of the LT1074 and LT1076 high efficiency switching regulators. These regulators are specifically designed for ease of use. This Application Note is intended to eliminate the most common errors that customers make when using switching regulators as well as offering insight into the inner workings of switching designs. There is an entirely new treatment of inductor design based upon simple mathematical formulas that yield direct results. There are extensive tutorial sections devoted to the care and feeding of the Positive Step-Down (Buck) Converter, the Tapped Inductor Buck Converter, the Positive to Negative Converter and the Negative Boost Converter. Additionally, many trouble-shooting hints are included as well as oscilloscope techniques, soft start architectures, and micropower shutdown and EMI suppression methods.

AN 45 **Measurement and Control Circuit Collection**

A variety of measurement and control circuits are included in this application note. Eighteen circuits, including ultra-low noise amplifiers, current sources, transducer signal conditioners, oscillators, data converters and power supplies are presented. The circuits emphasize precision specifications with relatively simple configurations. Available July, 1991.

AN 46 **Efficiency Characteristics of Switching Regulator Circuits**

Efficiency varies for different DC to DC converters. This application note compares the efficiency characteristics of some of the more popular types. Step-up, step-down, flyback, negative to positive, and positive to negative are shown. Appended sections discuss how to select the proper aluminum electrolytic capacitor and explain power switch and output diode loss calculations.

AN 47 **High Speed Amplifier Techniques**

This application note, subtitled "A Designer's Companion for Wideband Circuitry," is intended as a reference source for designing with fast amplifiers. Approximately 150 pages and 300 figures cover frequently encountered problems and their possible causes. Circuits include a wide range of amplifiers, filters, oscillators, data converters and signal conditioners. Eleven appended sections discuss related topics including oscilloscopes, probe selection, measurement and equipment considerations, and breadboarding techniques. Available August, 1991.

AN 48 **Using the LTC Op Amp Macromodels**

LTC's op amp macromodels are described in detail, along with the theory behind each model and complete schematics of each topology. Extended modeling topics are discussed, such as phase/frequency response modifications and asymmetric slew rate for JFET op amp models. LTC's macromodels are optimized for accuracy and fast simulation times. Simulation times can be further reduced by using streamlining techniques found throughout AN48.

Design Notes

DESIGN NOTE 1
New Data Acquisition Systems Communicate With Microprocessors Over Four Wires

DESIGN NOTE 2
Sampling Of Signals For Digital Filtering And Gate Measurements

DESIGN NOTE 3
Operational Amplifier Selection Guide For Optimum Noise Performance

DESIGN NOTE 4
New Developments In RS232 Interfaces

DESIGN NOTE 5
Temperature Measurement Using The LTC1090/91/92 Series Of Data Acquisition Systems

DESIGN NOTE 6
Operational Amplifier Selection Guide For Optimum Noise Performance

DESIGN NOTE 7
DC Accurate Filter Eases PLL Design

DESIGN NOTE 8
Inductor Selection For LT1070 Switching Regulators

DESIGN NOTE 9
Chopper Amplifiers Complement A DC Accurate Lowpass Filter

DESIGN NOTE 10
Electrically Isolating Data Acquisition Systems

DESIGN NOTE 11
Achieving Microamp Quiescent Current In Switching Regulators

DESIGN NOTE 12
An LT1013 And LT1014 Op Amp SPICE MacroModel

DESIGN NOTE 13
Closed Loop Control With The LTC1090 Series Of Data Acquisition Systems

DESIGN NOTE 14
Extending The Applications Of 5V Powered RS232 Transceivers

DESIGN NOTE 15
Noise Calculations In Op Amp Circuits

DESIGN NOTE 16
Switched-Capacitor Lowpass Filters For Anti-Aliasing Applications

DESIGN NOTE 17
Programming Pulse Generators For Flash EPROMs

DESIGN NOTE 18
A Battery Powered Lap Top Computer Power Supply

DESIGN NOTE 19
A Two-Wire Isolated And Powered 10-Bit Data Acquisition System

DESIGN NOTE 20
Hex Level Shift Shrinks Board Space

DESIGN NOTE 21
Floating Input Extends Regulator Capabilities

DESIGN NOTE 22
New 12-Bit Data Acquisition Systems Communicate With Microprocessors Over Four Wires

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Micropower, Single Supply Applications:
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Complex Data Acquisition System Uses Few Components

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A Single Amplifier, Precision High Voltage Instrument Amp

DESIGN NOTE 26
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DESIGN NOTE 27
Design Considerations For RS232 Interfaces

DESIGN NOTE 28
A SPICE Op Amp Macromodel For The LT1012

DESIGN NOTE 29
A Single Supply RS232 Interface For Bipolar A To D Converters

DESIGN NOTE 30
RS232 Transceiver With Automatic Power Shutdown Control

DESIGN NOTE 31
Isolated Power Supplies For Local Area Networks

DESIGN NOTE 32
A Simple Ultra-Low Dropout Regulator

DESIGN NOTE 33
Powering 3.3V Digital Systems

DESIGN NOTE 34
Active Termination For SCSI-2 Bus

DESIGN NOTE 35
12 Bit 8 Channel Data Acquisition System Interface To IBM PC Serial Port

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Ultra Low Noise Op Amp Combines Chopper And Bipolar Op Amps

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High Dynamic Range Bandpass Filters For Communication

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Low Power CMOS RS485 Transceiver

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Designing With A New Family Of Instrumentation Amplifiers

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Switching Regulator Allows Akalines To Replace NiCads

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Chopper vs Bipolar Op Amps – An Unbiased Comparision

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LT1056 Improved JFET Op Amp Macromodel Slews Asymmetrically

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A Single Ultra-Low Dropout Regulator

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Signal Conditioning For Platinum Temperature Transducers

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Current Feedback Amplifier "Do's and Don't's"

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Switching Regulator Generates Both Positive and Negative Supply with a Single Inductor

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No Design Switching Regulator 5V, 5A Buck (Step Down) Regulator

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DESIGN NOTE 56
3V Operation of Linear Technology Op Amps

DESIGN NOTE 57
Video Circuits Collection

DESIGN NOTE 58
A Simple, Surface Mount Flash Memory Vpp Generator

Applications on Disk

NOISE DISK

This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp.

SPICE MACROMODEL DISK

This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSPICE™ by MicroSim.

FILTERCAD DISK

FilterCAD is a menu-driven filter design aid program which runs on IBM-PCs (or compatibles). This collection of design tools will assist in the selection, design, and implementation of the right switched capacitor filter circuit for the application at hand. Standard classical filter responses (Butterworth, Cauer, Chebyshev, etc.) are available, along with a CUSTOM mode for more esoteric filter responses. SAVE and LOAD utilities are used to allow quick performance comparisons of competing design solutions. GRAPH mode, with a ZOOM function, shows overall or fine detail filter response. Optimization routines adapt filter designs for best noise performance or lowest distortion. A design time clock even helps keep track of on-line hours.

1990
Linear Applications Handbook
1990 Linear Databook
FilterCAD
NOISE
SPICE
FilterCAD
SPICE

SWITCHERCAD DISK

SwitcherCad is a powerful design tool that significantly eases the task of selecting topologies, calculating operating points, and specifying component values and part numbers for DC-to-DC converters. It can cut days off of the design cycle by eliminating the process of wading through multiple data sheets, application notes, and magazine "cookbook" articles searching for answers in a field where the user may have little familiarity. SwitcherCad runs on IBM-PCs and compatibles.

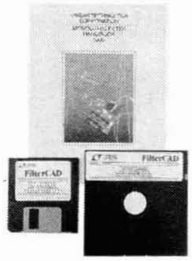
TECHNICAL BOOKS ORDER FORM

Linear Databook — This 1,600 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices.
$10.00

$10.00

Linear Applications Handbook — 928 pages chock full of application ideas covered in-depth through 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels.
$20.00

$20.00



Monolithic Filter Handbook — This 232 page book comes with a disk which runs on PCs. Together, the book and disk assist in the selection, design and implementation of the right switched capacitor filter circuit. The disk contains standard filter responses as well as a custom mode. The handbook contains over 20 data sheets, Design Notes and Application Notes.
$40.00

$40.00

RELIABILITY
ASSURANCE PROGRAM
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Reliability Assurance Program Brochure — A 16 page brochure accompanied by a Reliability Data Pack. The brochure describes LTC's approach to reliability planning, manufacturing process control and reliability assessment. The data pack contains actual test results and failure rate calculations for all device families and package types.
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Free

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Please send me ______ copies of your Monolithic Filter Handbook at $40.00 per copy.

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LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd., Milpitas, CA 95035
Phone: (408) 432-1900
FAX: (408) 434-0507
Telex: 499-3977

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